Hardware Technical Reference Manual

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PACKARD

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Because the HP Vectra PC generates and uses radio frequency energy, it may cause interference with radio and television reception in a residential installation.

Hewlett-Packard provides instructions for using this computer in manuals covering setup, connection of peripheral devices, operation, service, and technical reference.

Installing and using the computer in strict accordance with Hewlett-Packard's instructions will minimize the chances that the HP Vectra PC will cause radio or television interference. However, Hewlett-Packard does not guarantee that the computer will not interfere with radio or television reception.

If you think the computer is causing interference, turn it off to see if radio or television reception improves. If the reception improves, the computer is causing the problem.

To correct interference, take one or more of the following steps:

- Relocate the radio or television antenna
- Move the computer away from the radio or television
- Plug the computer into a different electrical outlet, so that the computer and the radio or television are on separate electrical circuits
- Make sure that all of your peripheral devices are certified Class B by the FCC
- Make sure that you use only shielded cables to connect peripheral devices to your computer
- Consult your computer dealer, Hewlett-Packard, or an experienced radio/television technician for other suggestions.

Electrical Safety

Warning

For user safety, the power cords supplied with this product have grounded plugs. The power cord should be used with properly grounded (3-hole) wall outlets to avoid electrical shock. (You can also use multiple-outlet strips that have their own circuit breakers.)

INTRODUCTION

Audience

This manual is intended to help original equipment manufacturers, independent hardware vendors, and independent software vendors in their design efforts.

Scope of Manual

Chapter 1 gives a system overview of the Hewlett-Packard Vectra RS Personal Computer.

Chapter 2 discusses the Processor/Memory PCA and Cache Memory PCA components, including buses.

Chapter 3 discusses the System Interface PCA components.

Chapter 4 discusses the power supply.

Schematics and a Glossary of terms are also included.

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1

SYSTEM OVERVIEW

1.1 Introduction

This chapter gives an overview of the Hewlett-Packard Vectra RS Personal Computer, a high-performance, industry-standard, floor-mount personal computer based on the Intel 80386 microprocessor. Included in this chapter are system configurations, architecture, specifications, and dimensions, along with references for additional information.

1.1.1 Users

The HP Vectra RS is geared towards users with demanding, computation-intensive tasks requiring great power, fast response time, large mass storage capacity, or expandability. Typical uses include the following:

* Computer-Aided Design/Engineering/Manufacturing
* Multi-Tasking
* Multi-User Operating Systems
* Local-Area Network Servers
* Data Base Management
* Desktop Publishing

1.1.2 Features

The HP Vectra RS has the following standard features:

* Intel 80386 microprocessor
* 9-pin serial port and 25-pin parallel port
* 32-Kbytes of static RAM for cache memory (RS/20C and RS/25C)
* 330-watt (peak) power supply
* Backplane I/O connector slots for up to 8 industry-standard accessory cards
* Disc caching
* Flexible disc controller and drive
* Hard disc controller and drive
* Industry-standard keyboard
* Socket for Intel 80387 coprocessor
* Socket for Weitek 1167 floating point coprocessor (RS/16 and RS/20)
* Socket for Weitek 3167 floating point coprocessor (RS/20C and RS/25C)
* Support for up to 5 mass storage devices
* Support for up to 7 HP-Human Interface Link input devices
* System RAM (1 to 4 Mbytes of 32-bit RAM standard, expandable up to 16 Mbytes)
* Terminal emulation

1.1.3 Compatibility

The HP Vectra RS is designed to be 100% compatible with the industry-standard IBM PC/AT II personal computer and with the HP Vectra family of personal computers. It offers downward compatibility, running industry-standard operating systems (including Microsoft's MS-DOS 3.2, MS-DOS 3.3, OS/2, and Windows 2.0) and industry-standard application software developed for systems based on 8088, 8086, or 80286 microprocessors. It also offers upward compatibility, in that it is designed to run Microsoft Windows/386, UNIX V.3/386, XENIX 386, and future operating systems and applications based on the Intel 80386 microprocessor.

1.2 System Configurations

1.2.1 Basic Configuration

The HP Vectra RS includes certain basic components, including a monitor, keyboard, and the system processing unit (SPU). For additional components, consult your HP representative.

Figure 1-1 shows the basic configuration* for the HP Vectra RS SPU: a power supply, one flexible and one hard disc drive, eight backplane I/O connector slots, and four printed circuit assemblies: the System Interface PCA, the Processor/Memory PCA, the Four-Function Controller PCA, and the Input Device Connector PCA.

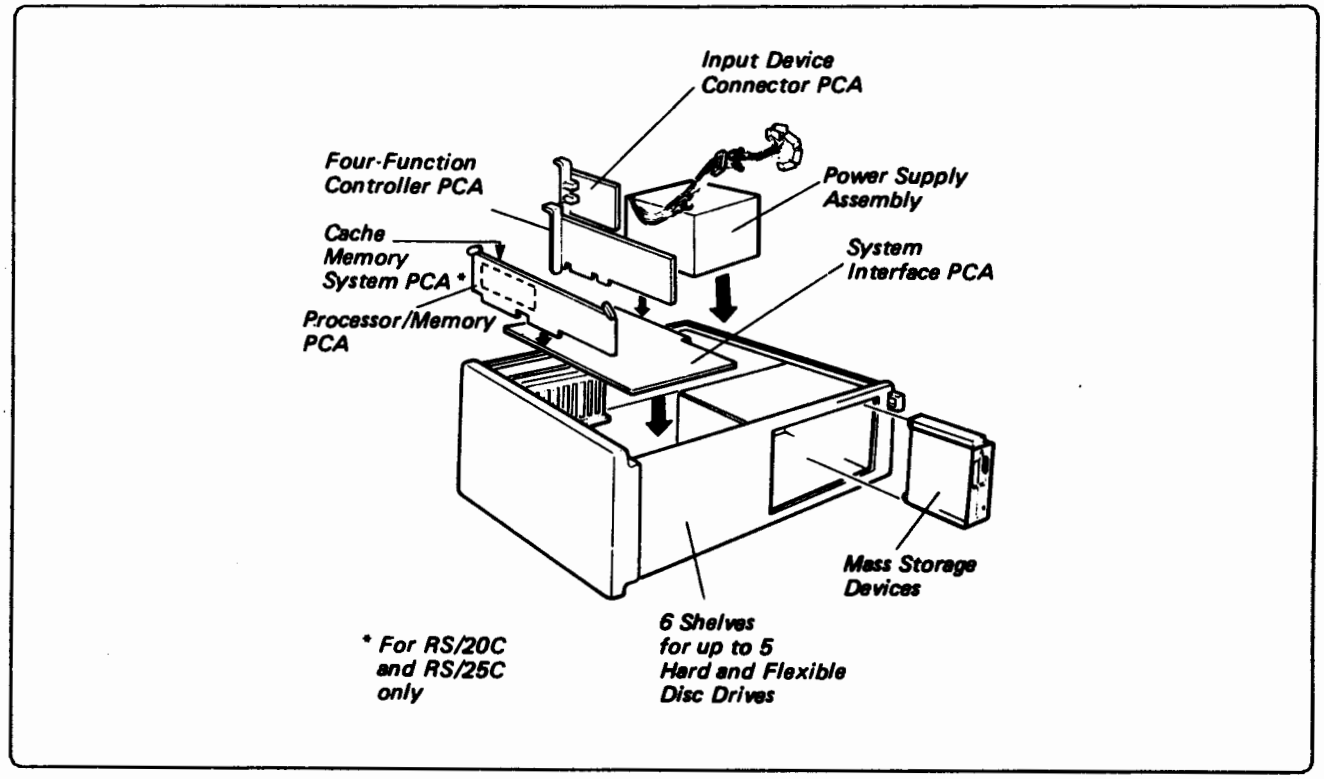


Figure 1-1. Basic Configuration of Vectra RS SPU

* A fifth PCA, the Cache Memory System PCA, is not shown. It plugs into the Processor/Memory PCA and comes only with those models that have cache memory (the RS/20C and RS/25C).

* Items not included in the "OEM" models for the RS/20, RS/20C, and RS/25C are the flexible and hard disc drives and the Four-Function Controller PCA.

1.2.2 Configuration Options

The HP Vectra RS is available in three speeds. The RS/16 operates with the 16-MHz 80386 microprocessor, while both the RS/20 and the RS/20C operate with the 20-MHz 80386 microprocessor. The RS/25C operates with the 25-MHz 80386 microprocessor. Tables 1-1 through 1-4 compare the various model configurations.

Table 1-1. RS/16 Model*

Model	RAM (1)	Hard disc drive	Flexible disc drive
40	1 Mbyte	40 Mbytes	1.2 Mbytes (2)
100	2 Mbytes	103 Mbytes	1.2 Mbytes (2)
106 (3)	2 Mbytes	103 Mbytes	1.2 Mbytes (2)
OEM	1 Mbyte	(4)	(4)

Table 1-2. RS/20 Model*

Model	RAM (1)	Hard disc drive	Flexible disc drive
40	1 Mbyte	40 Mbytes	1.2 Mbytes (2)
100	2 Mbytes	103 Mbytes	1.2 Mbytes (2)
106 (3)	2 Mbytes	103 Mbytes	1.2 Mbytes (2)
150	2 Mbytes	155 Mbytes	1.2 Mbytes (2)
300	2 Mbytes	310 Mbytes	1.2 Mbytes (2)
Power User (5)	4 Mbytes	103 Mbytes	1.2 Mbytes (2) 1.44 Mbytes
OEM	1 Mbyte	(4)	(4)

* Notes for the tables appear after Table 1-4.

Table 1-3. RS/20C Model*

Model (6,7)	RAM (1)	Hard disc drive	Flexible disc drive (2)
100e	1 Mbyte	103 Mbytes	1.2 Mbytes
150e	1 Mbyte	155 Mbytes	1.2 Mbytes
154e	4 Mbytes	155 Mbytes	1.2 Mbytes

Table 1-4. RS/25C Model*

Model (6,7)	RAM (1)	Hard disc drive	Flexible disc drive (2)
100e	1 Mbyte	103 Mbytes	1.2 Mbytes
150e	1 Mbyte	155 Mbytes	1.2 Mbytes
154e	4 Mbytes	155 Mbytes	1.2 Mbytes
304e	4 Mbytes	310 Mbytes	1.2 Mbytes

***Notes for Tables 1-1 to 1-4:**

(1) 32-bit system RAM, expandable to 16 Mbytes. [See the "Main Memory (RAM)" section in the chapter "Processor/Memory PCA."]

(2) Except for the OEM models, the HP Vectra RS comes standard with a 5.25-inch, 1.2-Mbyte flexible disc drive. The HP Vectra RS can support both a 5.25-inch, 360-Kbyte flexible disc drive and a 3.5-inch, 1.44-Mbyte flexible disc drive.

(3) The 106 models feature a video graphics adapter (VGA) accessory card.

(4) The OEM (Original Equipment Manufacturer) models are stripped-down versions of the Vectra RS which do not include hard and flexible disc drives and disc drive controllers.

(5) The RS/20 Power User model comes with both a 5.25-inch, 1.2-Mbyte flexible disc drive and a 3.5-inch, 1.44-Mbyte flexible disc drive. In addition, it comes standard with an 80387 coprocessor, 1 parallel and 3 serial ports, a VGA monitor and accessory card, an HP mouse, and a 40-Mbyte tape backup drive.

(6) The RS/20C and the RS/25C models come with 32 Kbytes of cache memory (static random-access memory). For more information on cache memory, see the "Cache Memory" section in the chapter "Processor/Memory PCA."

(7) " e " indicates an ESDI controller is included.

1.3 System Architecture

This section gives an overview of the HP Vectra RS system architecture. (See Figures 1-2 and 1-3 for a block diagram of the system architecture.)

1.3.1 Hardware

Monitor

Both monochrome and color monitors are available, along with accessory cards for the monitors. The monochrome HP Multimode monitor and accessory card are fully compatible with the industry-standard monochrome modes. The color monitor, the HP Enhanced Graphics Display, supports 16 colors in the text mode and 64 colors in the graphics mode. It is compatible with the industry-standard enhanced graphics adapter (EGA) and video graphics adapter (VGA) accessory cards. The 106 models feature a VGA accessory card.

Keyboard

The HP Vectra RS supports the HP Vectra Enhanced Keyboard, a detachable, 101-key, industry-standard keyboard with separate numeric and cursor control keypads and an industry-standard DIN cable connector. Industry-standard international keyboards (with 102 keys) are also available. (Note: The HP Vectra RS does not support the "Vectra PC Keyboard," used by earlier versions of HP Vectra PCs.)

Hewlett-Packard Human Interface Link Devices

Up to seven Hewlett-Packard Human Interface Link (HP-HIL) devices, such as a mouse, graphics tablet, and barcode reader can be connected simultaneously via the HP-HIL port on the SPU's rear. The HP-HIL keyboard (also known as the "Vectra PC Keyboard") is not supported.

Power Supply

The power supply provides 200 watts of continuous power (330 watts peak).

Backplane I/O

The backplane I/O consists of two 8-bit and six 16-bit I/O connector slots for industry-standard accessory cards. Using a switch on the Processor/Memory PCA, the RS/20, RS/20C, and RS/25C models can set the backplane I/O for a speed greater than 8 MHz, as long as all installed accessory cards run at the greater speed.

Real-Time Clock/CMOS RAM

The real-time clock/CMOS RAM includes 114 bytes of CMOS RAM. A 6-volt lithium battery provides power to the real-time clock/CMOS RAM during power-down and power failures.

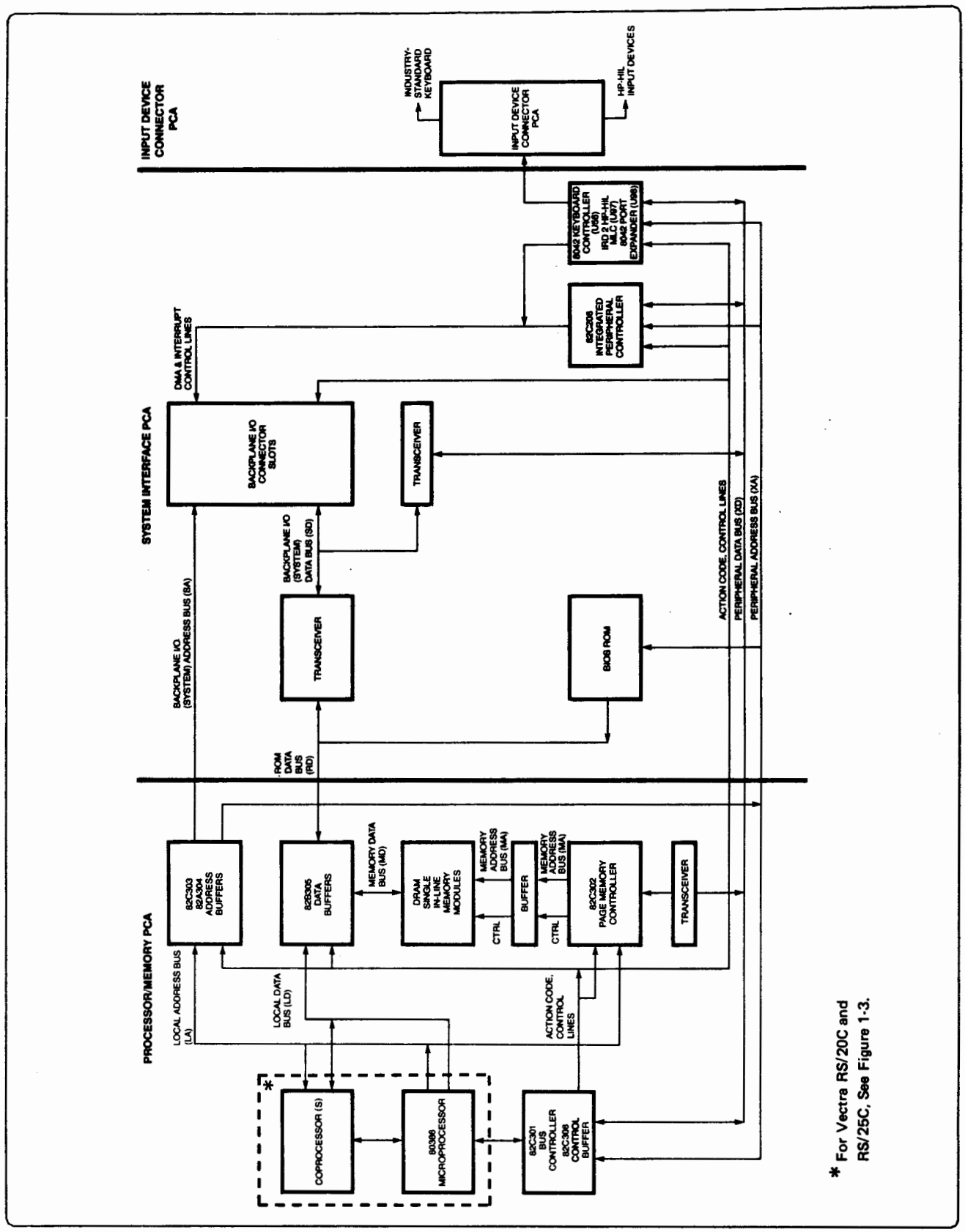


Figure 1-2. HP Vectra RS System Architecture

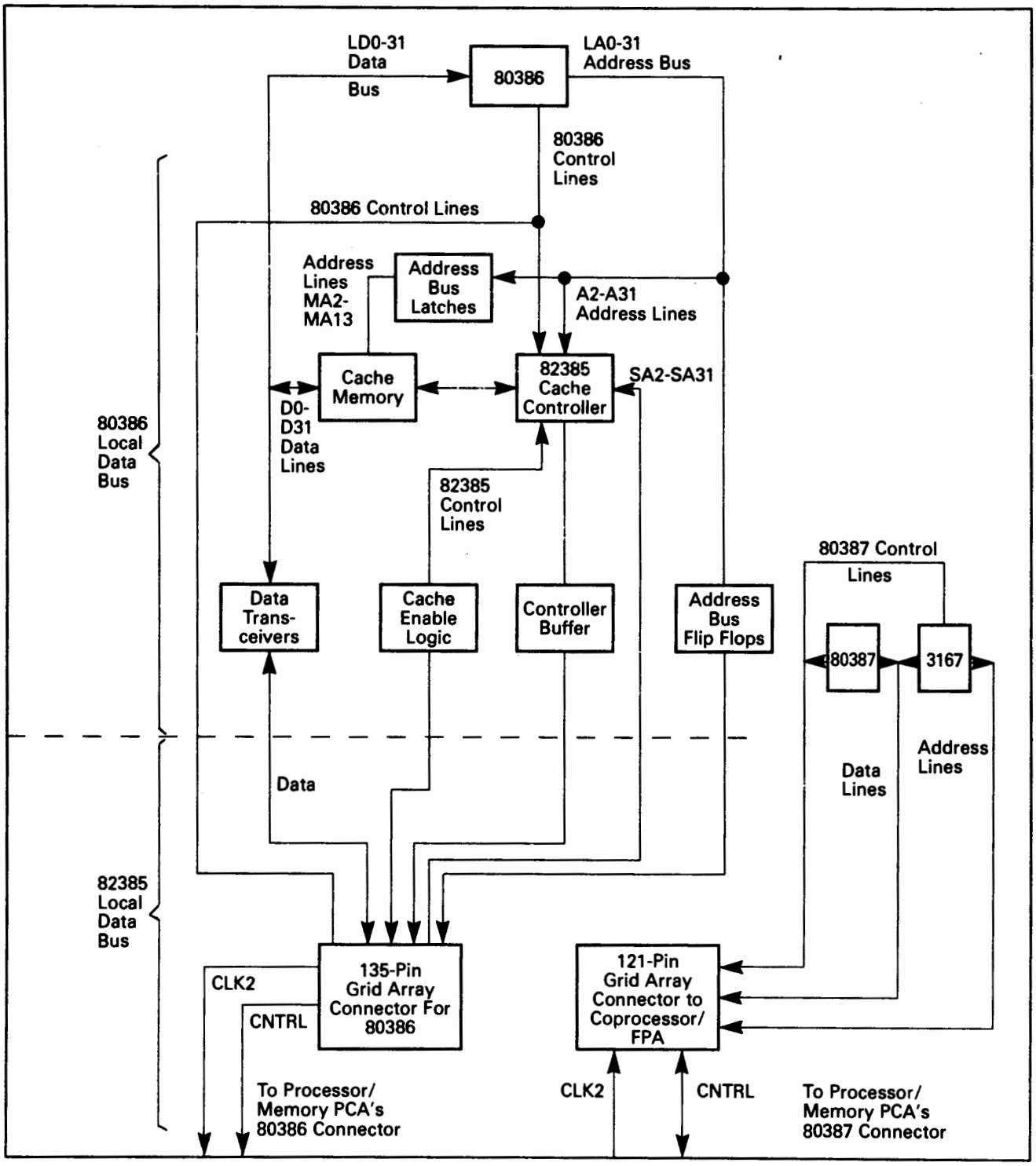


Figure 1-3. Expanded Block Diagram for RS/20C and RS/25C

System Microprocessor

The HP Vectra RS system is based on the 32-bit 80386 microprocessor: a 16-MHz 80386 for the RS/16, a 20-MHz 80386 for the RS/20 and RS/20C, and a 25-MHz 80386 for the RS/25C.

Coprocessor

All Vectra RS models supply a socket for an Intel 80387 coprocessor. The RS/16 and RS/20 supply a socket for a Weitek 1167 floating point coprocessor; the RS/20C and RS/25C supply a socket for a Weitek 3167 floating point coprocessor. Both an 80387 and a Weitek floating point coprocessor may be installed in the Vectra RS PC. A switch setting on the Processor/Memory PCA allows the 80387 to be set to either the synchronous or asynchronous mode, as covered under "Coprocessor" in the chapter "Processor/Memory PCA."

Mass Storage

Except for OEM models, the HP Vectra RS comes standard with a half-height flexible disc drive and, depending on the model, either a half- or full-height hard disc drive. With its six half-height, front-access shelves on the system processing unit, the HP Vectra RS supports up to five mass storage devices.

Four-Function Controller PCA. Except for OEM models, all HP Vectra RS models come standard with a Four-Function Controller PCA. While not a mass storage device itself, the Four-Function Controller PCA supports hard disc, flexible disc, and tape backup drives as well as provides the parallel and serial ports. For the RS/16 and RS/20 model 40, the Four-Function Controller PCA uses an ST-506 hard disc drive controller; for all other models, the Four-Function Controller PCA uses an Enhanced Small Device Interface (ESDI) hard disc drive controller. The Four-Function Controller is not included in the OEM models.

Hard Disc Drives. Model 40 for the RS/16 and RS/20 comes standard with a half-height 40-Mbyte ST-506 hard disc drive unit with an average access time of 28 milliseconds and a maximum data transfer rate of 5 Mbits/second. Except for the OEM models, all other models come standard with a full-height ESDI hard disc drive with an average access time of 17 milliseconds and a maximum data transfer rate of 10 Mbits/second. The HP Vectra RS can support up to two full-height hard disc drives, for a maximum of up to 620 Mbytes.

Flexible Disc Drives. Except for OEM models, all HP Vectra RS models come standard with a 5.25-inch, 1.2-Mbyte half-height flexible disc drive unit. The Power User models have a 3.5-inch, 1.44-Mbyte flexible disc drive as well. All models can support up to four flexible disc drive units, including 5.25-inch, 360-Kbyte flexible disc drive units and 3.5-inch, 1.44-Mbyte flexible disc drive units.

Tape Backup Drives. For hard disc drive backup, all models support an internal 40-Mbyte tape backup drive unit, with an average data transfer rate of 1.7 Mbytes/minute. The RS/16 and RS/20 models support an external 67-Mbyte HP-IB tape backup drive unit, with an average data transfer rate of 2.0 Mbytes/minute.

Flexible Disc Expander PCA. The Flexible Disc Expander (FDE) PCA permits installation of more than two flexible disc-type devices. In addition to the one flexible disc drive that comes standard with most models of the HP Vectra RS, one flexible disc drive or one tape backup drive can be added before the FDE must be used. With the FDE installed, the HP Vectra RS can support up to four flexible disc-type devices.

Security Locks

The HP Vectra RS features dual security locks: one on the front of the SPU to prevent input from the keyboard and other input devices, and one on the SPU's back, to lock the SPU unit cover.

1.3.2 Memory Subsystem

RAM

Depending on the model, the HP Vectra RS comes standard with from 1 to 4 Mbytes of system RAM, expandable on the Processor/Memory PCA to 16 Mbytes. The RAM subsystem uses a combination paged/interleaved architecture which allows for zero wait-state memory access.

ROM

All models come with 64 Kbytes of system (BIOS) ROM, with two sockets available on the System Interface PCA for 32-Kbyte option ROM chips.

Cache

The RS/20C and the RS/25C models come with 32 Kbytes of static RAM cache memory.

1.3.3 Software

The HP Vectra RS comes standard with the following:

* HP Expanded Memory Manager/386

* HP Terminal Program software (emulates the following terminals):
--Digital terminals VT52 and VT100
--HP terminals 150A, 2392A, and 2627A

* HP Vectra Disc Cache Program

* Volume Expansion Utility

1.4 Specifications and Dimensions

1.4.1 System Specifications

Regulatory Compliance

1. Datacomm

   Australian Telecomm Category A license *
   Belgium (RTT)
   Germany (FTZ)
   Nordic Network
   United Kingdom *

2. Ergonomics

   Complies with German Standard ZH1/618*

3. Radio Frequency Interference

   FCC Class B (U.S.A.)
   FTZ 1046/84 Level B Radio Protection Mark (Germany) *
   SABS approval (South Africa) *
   VCCI approval, Class 2 (Japan)

4. Safety Approvals

   BSI certified (United Kingdom) *
   CSA certified (Canada)
   FEI approved (Finland)
   IEC 380/435/950 (International) compliance
   NEMKO exempt (Norway)
   SASO *
   TUV certified (Germany) *
   UL listed (United States)

   * pending

Power Supply Specifications

1. AC Input

   Auto-ranging, world-wide power supply, configured to operate with line voltages of:

   90 to 132 Vac at 47 to 63 Hz or
   198 to 264 Vac at 47 to 63 Hz

2. Heat Output

   910 BTUs/hour maximum

3. Output Power

   200 watts continuous; 330 watts peak (for 10 seconds during hard disc drive spin-up)

4. Power Available to Accessory Cards

   Volts – Maximum Total Current/Average Current per Accessory Card

   +5 Volts – 10.6 Amps/1.3 Amps (RS/16 and RS/20)
   +5 Volts – 7.6 Amps/0.95 Amps (RS/20C and RS/25C)
   +12 Volts – 0.5 Amps/0.06 Amps
   -5 Volts – 0.3 Amps/0.03 Amps
   -12 Volts – 0.3 Amps/0.03 Amps

5. Power Consumption

   Convenience outlet (AC output outlet) used at 150 watts:

   610 watts maximum peak with 110-volt line voltage
   590 watts maximum peak with 220-volt line voltage

   Convenience outlet (AC output outlet) unused:

   460 watts maximum peak with 110-volt line voltage
   440 watts maximum peak with 220-volt line voltage

1.4.2 Environmental Specifications

Temperature Limits

Operating temperature:

+5 to +40 Celsius (+41 to +104 Fahrenheit) at the humidity limits given below

Non-operating temperature (without media in flexible disc drive):

-40 to +70 Celsius (-40 to +158 Fahrenheit)

Humidity Limits (Noncondensing):

Operating relative humidity:

15% to 80%

Non-operating relative humidity

90%

Maximum Altitude at +40 degrees Celsius (+104 degrees Fahrenheit):

Operating altitude: 4.6 kilometers (15,000 feet)

Non-operating altitude: 15.2 kilometers (50,000 feet)

1.4.3 HP Vectra RS Dimensions

General dimensions for the HP Vectra RS are given below.

System Processing Unit Dimensions

Floor-Mount Position

Height	60 centimeters	(24 inches)
Width	21 centimeters	(8.3 inches)
Base Width	35.5 centimeters	(14 inches)
Depth	50 centimeters	(20 inches)
Weight	27 kilograms	(60 pounds) *

*Weight includes floor-mount base, but excludes monitor and keyboard. For the RS/20C and RS/25C, add 204 grams (7.14 ounces) for the Cache Memory System PCA.

Desktop Position

Height	21 centimeters	(8.3 inches)
Width	59.4 centimeters	(23.4 inches)
Depth	50 centimeters	(20 inches)
Weight	26.3 kilograms	(58.5 pounds) **

**Weight excludes floor-mount base, monitor, and keyboard. For the RS/20C and RS/25C, add 204 grams (7.14 ounces) for the Cache Memory System PCA.

Keyboard Dimensions

Height	3.4 centimeters	(1.4 inches)
Width	46.8 centimeters	(18.4 inches)
Depth	19.8 centimeters	(7.8 inches)
Weight	1.9 kilograms	(4.2 pounds)

Cable Lengths

EGA extension cable	2 meters (6.6 feet)
EGA monitor cable	1 meter (3.3 feet)
HP-HIL cable	2.4 meters (8.0 feet)
Keyboard DIN cable	3 meters (9.9 feet)
Mouse cable	2.5 meters (8.25 feet)
Multimode monitor cable	1 meter (3.3 feet) or 3 meters (9.9 feet) models available

1.4.4 I/O Accessory Card Dimensions

Figure 1-4 shows the dimensions of industry-standard backplane I/O accessory cards. The card thickness should be 1.524 mm (0.060 inches).

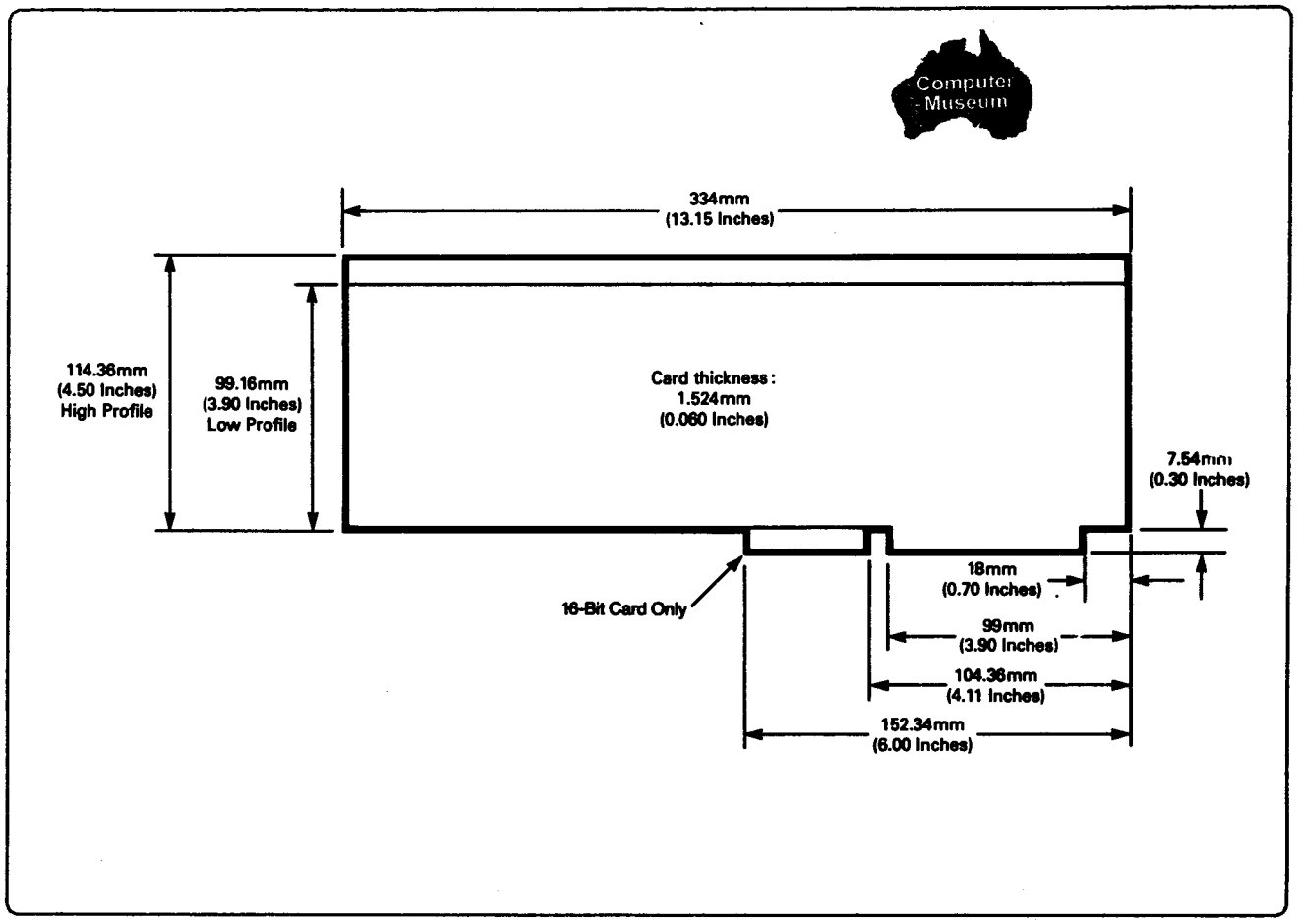


Figure 1-4. Industry-Standard I/O Accessory Card Dimensions

1.5 References

The following documents should be used for detailed information about components and functions discussed in this manual.

- Chips and Technologies series of 82A and 82C technical reference documents.
- *HP-HIL Technical Reference Manual.* HP product number 45918A.
- *HP Vectra Accessories Technical Reference Manual.* HP product number 5061-8983.
  - -- Reference for technical information on accessories for the HP Vectra ES and RS
- *HP Vectra MS-DOS Macro Assembler Manual.* HP product number 45953-90001.
  - -- Reference for the assembler.
- *HP Vectra MS-DOS 3.2 Programmer's Reference Manual.* HP product number 5959-2602.
  - -- Reference for programming the central processing unit, using MS-DOS 3.2.
- *HP Vectra MS-DOS 3.3 User's Reference Manual.* HP product number 45951D.
- *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.* HP product number 45945-90012.
  - -- Reference for the BIOS ROM.
- *Intel 8086 Family User's Manual.*
- *Intel 80386 Hardware Reference Manual.*
  - -- Reference for the 80386 microprocessor and the 80387 coprocessor.
- *Intel 80386 Programmer's Reference Manual.*
  - -- Reference for the 80386 architecture and instruction set.
  - -- Reference for the 80387 coprocessor.
- *Intel 82385 High Performance 32-Bit Cache Controller.*
  - -- Reference for the 82385 cache controller.
- *Intel Microcontroller Handbook.*
- *Intel Microprocessor and Peripheral Handbook. Volume I -- Microprocessor.*
  - -- Reference for the 8237A DMA controller.
- *Intel Microsystem Components Handbook. Microprocessors and Peripherals. Volume II.*
  - -- Reference for the 8042 keyboard controller.
  - -- Reference for the 8254 counter/timer.
  - -- Reference for the 8259A interrupt controller.
- *Microsoft MS-DOS 3.3 Programmer's Reference Manual.*
  - -- Reference for programming the central processing unit, using MS-DOS 3.3.
- *Motorola Single Chip Microcomputer Data, Section C.*
  - -- Reference for the MC146818 real-time clock/CMOS RAM.
- *Weitek WTL 1167 Floating Point Coprocessor.* (Data Sheet)
  - -- Reference for the 1167 floating point coprocessor.
- *Weitek WTL 3167 Floating Point Coprocessor.* (Data Sheet)
  - -- Reference for the 3167 floating point coprocessor.

2

PROCESSOR/MEMORY PRINTED CIRCUIT ASSEMBLY

2.1 Introduction

This chapter describes the Processor/Memory PCA, a surface-mount printed circuit assembly. This board provides the HP Vectra RS with all its RAM, the support circuitry for all buses, and support for the board's subsystems, including cache memory, for those models that feature cache.

For models without cache, Table 2-1 lists the major Processor/Memory PCA components, and Figure 2-1 shows their layout. For models with cache, Table 2-2 lists the major Processor/Memory PCA components, Table 2-3 lists the major Cache Memory System PCA components, and Figures 2-2 and 2-3 show the layout of the components. (For models with cache, the Cache Memory System PCA is connected to the Processor/Memory PCA via pin-grid connectors.)

Figure 2-4 is a block diagram of the Processor/Memory PCA, and Figure 2-5 is a block diagram of the Cache Memory System PCA. A discussion of the main components and their operation follows. (Schematics for the Processor/Memory PCA and the Cache Memory System PCA are given at the end of the chapter.)

Table 2-1. Major Processor/Memory PCA Components (for RS/16 and RS/20)

16 sockets for dynamic RAM modules (J1 to J16)
2 150-pin connectors to System Interface PCA (J17 and J18)
1 switch for various system configurations (SW1)
1 16-MHz system clock (OSC1)
1 32-MHz system clock for RS/16 (OSC2)
1 40-MHz system clock for RS/20 (OSC2)
1 optional oscillator (OSC3) for 80387 coprocessor *
1 14.318-MHz system clock (OSC4)
1 80386 microprocessor (U63)
1 socket for Intel 80387 coprocessor and/or Weitek 1167 floating point coprocessor (XU82)**
1 82301 bus controller (U77)
1 82302 page memory controller (U67)
1 82303 high address buffer (U147)
1 82304 low address buffer (U107)
2 82305 data buffers (U32, U36)
1 82306 control buffer (U122)

* OSC3 is not currently installed or supported.
** An 80387 coprocessor comes standard only with the Power User models.

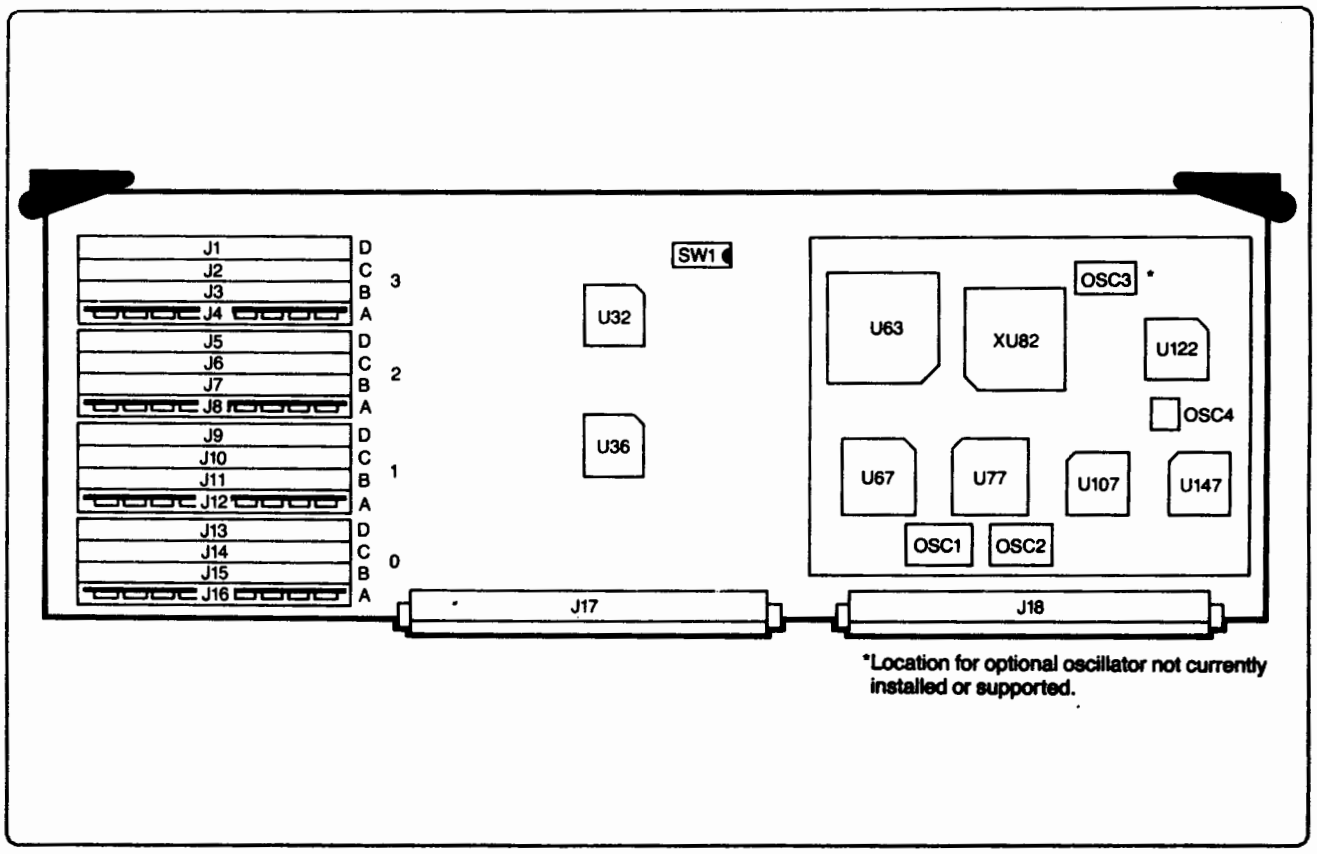


Figure 2-1. Processor/Memory PCA Components (RS/16 and RS/20)

Table 2-2. Major Processor/Memory PCA Components (RS/20C and RS/25C)

16 sockets for dynamic RAM modules (J1 to J16)
2 150-pin connectors to System Interface PCA (J17 and J18)
1 switch for various system configurations (SW1)
1 16-MHz system clock (OSC1)
1 40-MHz system clock for RS/20C (OSC2)
1 50-MHz system clock for RS/25C (OSC2)
1 optional oscillator (OSC3) for 80387 coprocessor *
1 14.318-MHz system clock (OSC4)
2 sockets for Cache Memory System PCA interface to Processor/Memory PCA (U63, XU82)
1 82301 bus controller (U77)
1 82302 page memory controller (U67)
1 82303 high address buffer (U147)
1 82304 low address buffer (U107)
2 82305 data buffers (U32, U36)
1 82306 control buffer (U122)

Table 2-3. Major Cache Memory System PCA Components (for Models with Cache)

1 80386 microprocessor (U1)
1 pin grid array socket for 80387 coprocessor (XU4)**
1 82385 cache controller (U2)
16 static random access memory (SRAM) chips (U17 to U32)
1 pin grid array socket for 3167 floating point coprocessor (XU3)
1 pin grid array socket adapter for interface to Processor/Memory PCA (P1)

* OSC3 is not currently installed or supported.
** An 80387 coprocessor comes standard only with the Power User models.

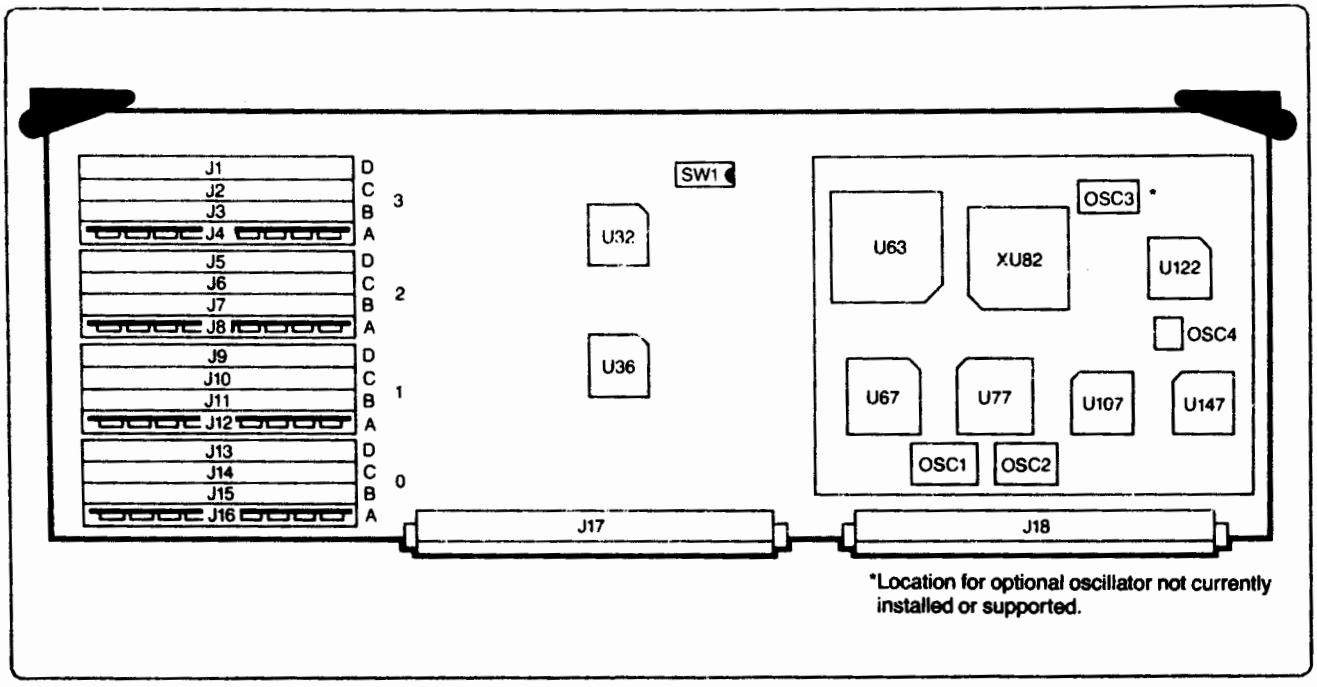


Figure 2-2. Processor/Memory PCA Components (RS/20C and RS/25C)

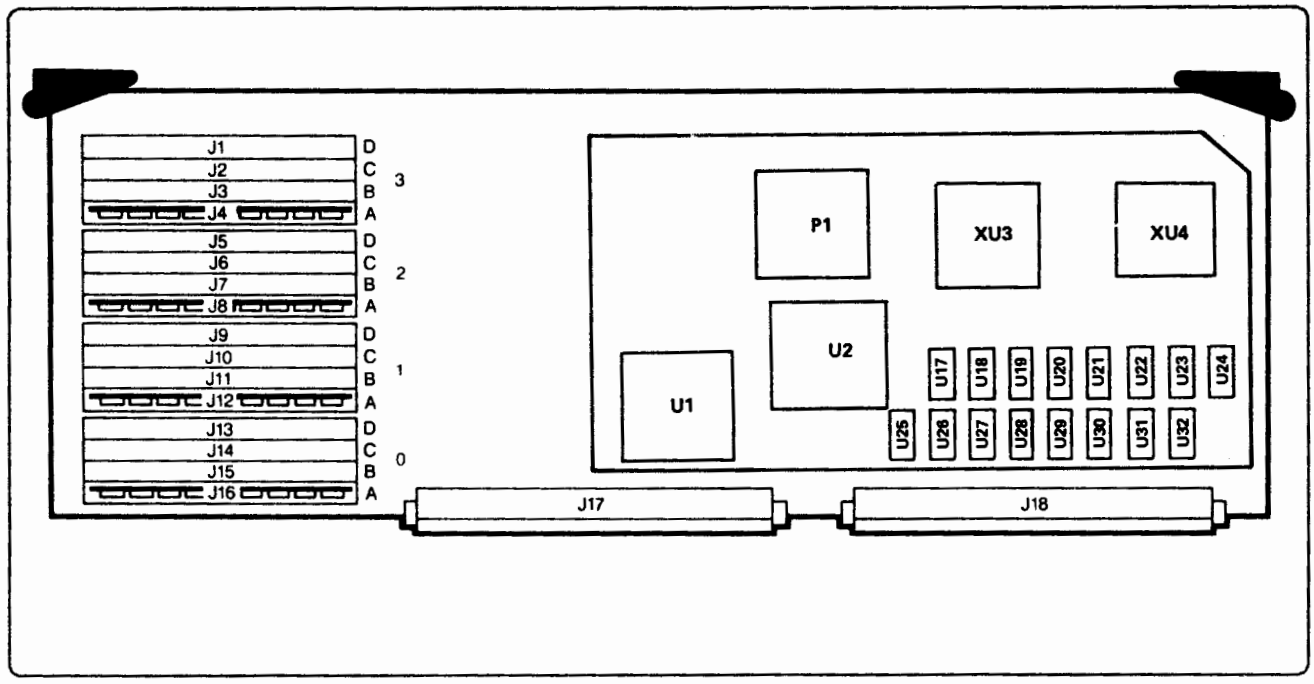


Figure 2-3. Cache Memory System PCA Components (RS/20C and RS/25C)

Note: The Cache Memory System PCA is installed on top of the Processor/Memory PCA.

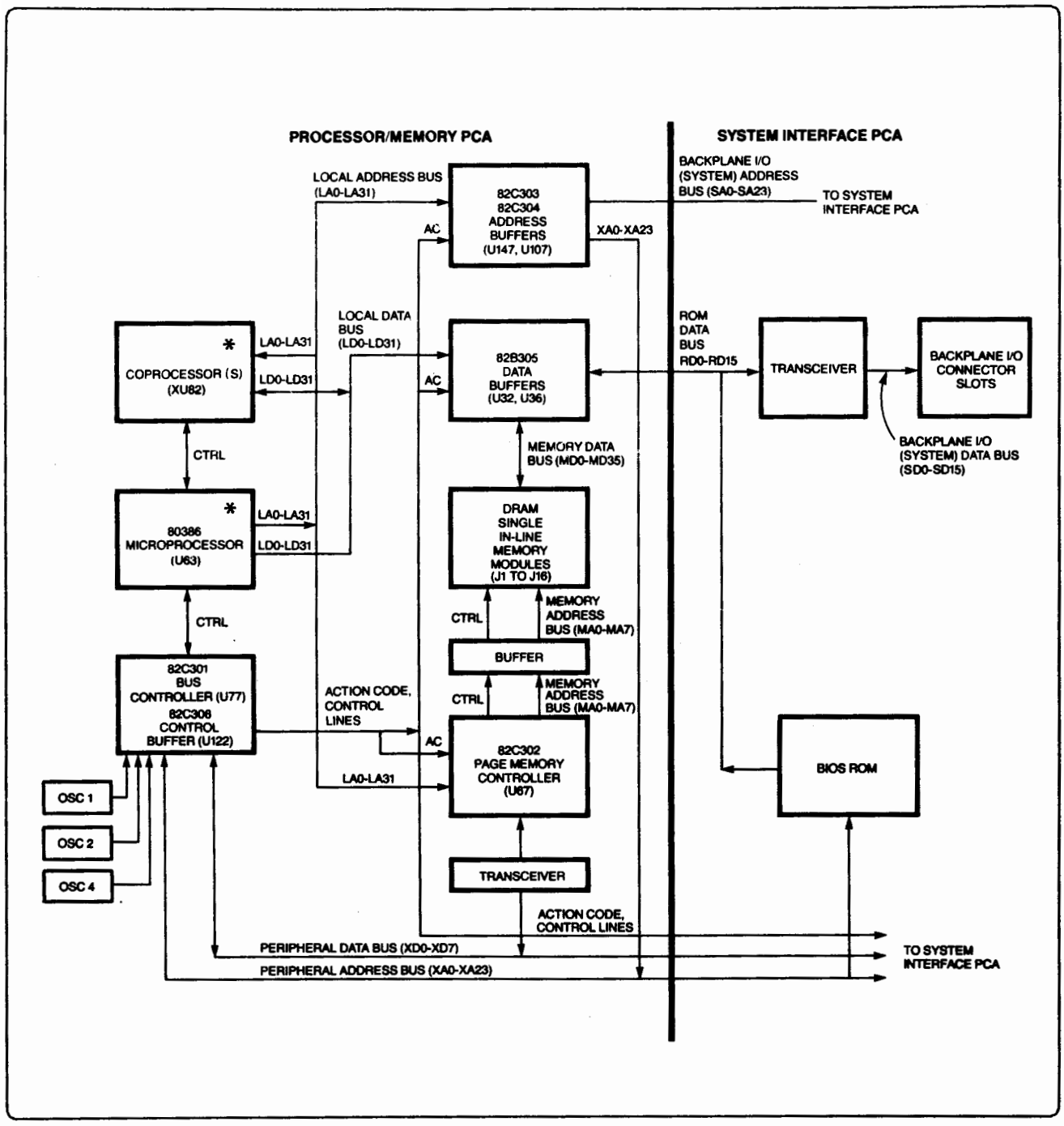
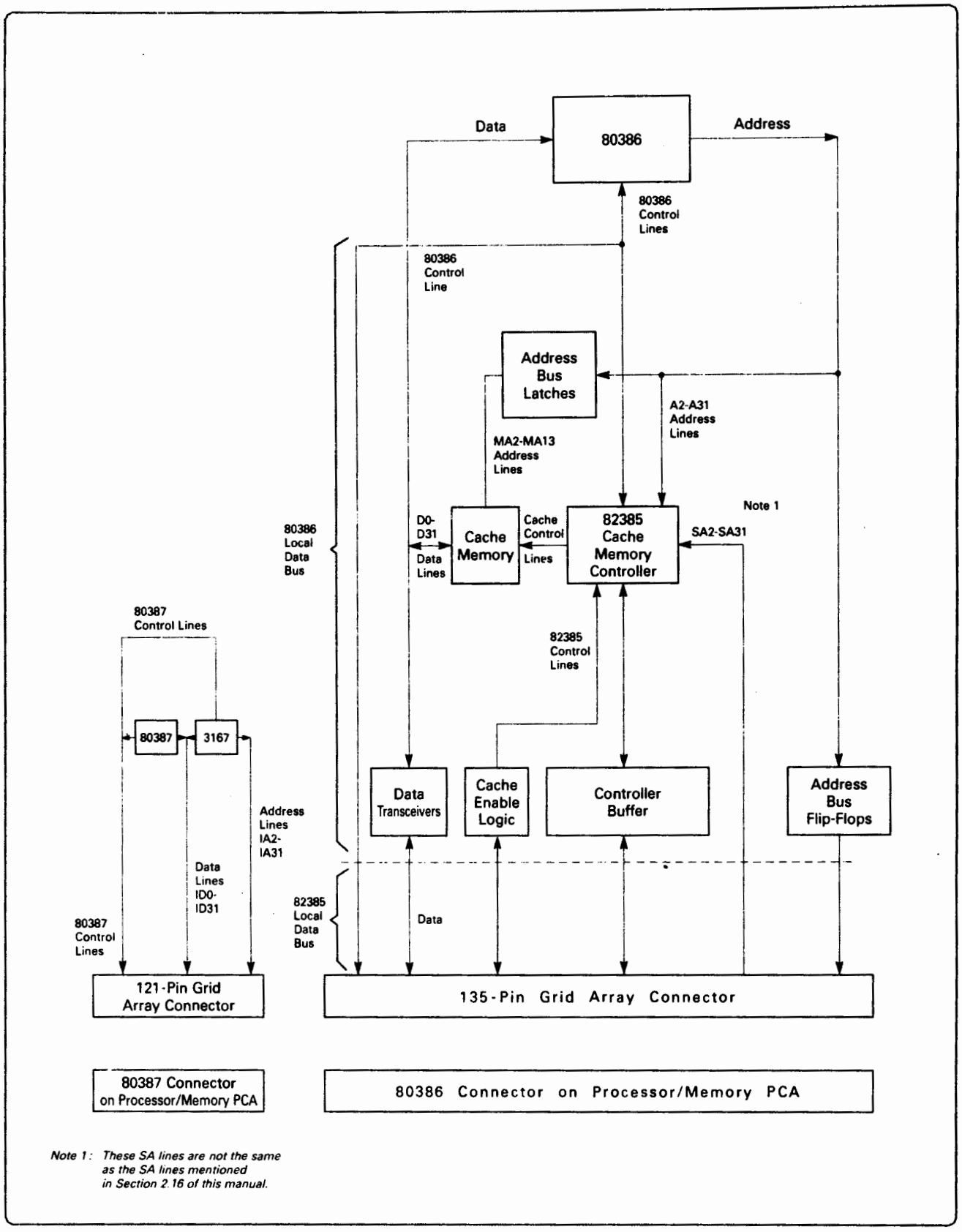


Figure 2-4. Processor/Memory PCA Block Diagram (all models)

* For the RS/20C and RS/25C models, (1) the Cache Memory System PCA is connected onto the Processor/Memory PCA's sockets for the 80386 microprocessor and the 80387 coprocessor, and (2) the 80386 microprocessor and the coprocessors are installed onto the Cache Memory System PCA. (For the RS/20C and RS/25C models, see Figure 2-5 for an extension of this block diagram.)



Note 1: These SA lines are not the same as the SA lines mentioned in Section 2.16 of this manual.

Figure 2-5. Cache Memory System PCA Block Diagram

2.2 System Clocks

The system's main oscillators, located on the Processor/Memory PCA, generate the various system clock signals and are discussed under the components for which they provide clocking. (Other oscillators are part of a particular chip or a family of chips, and are discussed in the sections covering those chips.)

Oscillator 1 (OSC1) provides 16 MHz for the 82301 bus controller's ATCLK1. (For a further discussion, refer to the "Bus Controller" section in this chapter.)

Oscillator 2 (OSC2) on the HP Vectra RS/16 provides 32 MHz for the 82301 bus controller's CLK2IN; on the RS/20 and RS/20C, OSC2 provides 40 MHz for the 82301 bus controller's CLK2IN. For the RS/25C, OSC2 provides 50 MHz for the 82301 bus controller's CLK2IN. (For a further discussion, refer to the "Microprocessor" and "Bus Controller" section in this chapter.)

Oscillator 3 (OSC3) is an optional oscillator that, while not currently installed or supported, could be installed to provide clocking for the 80387 coprocessor's asynchronous mode. (For a further discussion, refer to the "Coprocessor" and "Processor/Memory PCA Switch 1" sections in this chapter.)

Oscillator 4 (OSC4) provides 14.318 MHz to the 82306 control buffer. (For a further discussion, refer to the "Control Buffer" section in this chapter.)

2.3 Microprocessor

The HP Vectra RS/16 uses as its central processing unit the 16-MHz 80386 microprocessor. The HP Vectra RS/20 and RS/20C use the 20-MHz 80386 microprocessor, while the RS/25C uses the 25-MHz 80386 microprocessor. Although the 80386 microprocessor component can support up to 4 gigabytes of dynamic RAM, the 80386 is used in the HP Vectra RS to support up to 16 Mbytes of dynamic RAM. In addition, the 80386 microprocessor provides the following:

* 32-bit registers
* comprehensive instruction set
* direct-memory access (DMA) support capabilities
* downward compatibility with the 8088, 8086, and 80286 microprocessors
* interrupt support capabilities
* multi-tasking support
* operating modes: protected, real-address, and virtual
* separate 32-bit address and data paths
* support for 8-, 16-, and 32-bit data types

Microprocessor Clocking

For all models, OSC2 provides to the 82301 bus controller the CLK2IN signal. In turn, the bus controller provides to the 80386 the CLK2 signal (32 MHz, 40 MHz, or 50 MHz, depending on the model). Internally, the 80386 divides the CLK2 signal down to 16 MHz, 20 MHz, or 25 MHz, respectively.

With all models, as required by some industry-standard operations, slower speeds can be achieved. For the RS/16 and RS/20, when the keyboard's <CTRL>, <Alt>, and backslash < \ > keys are simultaneously pressed, the clock signal to the 82301 bus controller changes from OSC2 to the 16-MHz OSC1. As a result, the CLK2 signal that the bus controller provides to the 80386 is 16 MHz, which the 80386 divides down to 8 MHz. Pressing <CTRL>, <Alt>, and < \ > keys restores the OSC2 signal.

For the Vectra RS/20C and RS/25C, there are two slower speed modes--medium and slow--which can be selected using one of two methods. One method for choosing the desired speed is to use the SETUP program, as described in the Hewlett-Packard manual *Setting Up Vectra RS*. A second method is to type either HPMODE SPEED MEDIUM or HPMODE SPEED SLOW at the MS-DOS prompt, which adds hold states to the microprocessor's cycles. Depending on the instructions executed, the result is a medium speed of 10 MHz for the RS/20C and approximately 12.5 MHz for the RS/25C, and a slow speed of approximately 5.5 MHz for both the RS/20C and RS/25C. With both methods, pressing <CTRL>, <Alt>, and < \ > keys restores the OSC2 signal to its original speed.

Microprocessor Compatibility

By dynamically sizing data, the 80386 microprocessor maintains hardware compatibility with the 8088/8086 and the 80286 microprocessors. The 80386 microprocessor also maintains software compatibility, in that it runs industry-standard application software and operating systems (including MS-DOS 3.2, MS-DOS 3.3, Microsoft OS/2, and Windows 2.0) developed for systems based on 8088, 8086, or 80286 microprocessors. In addition, it runs new application software and operating systems written for it (including UNIX V.3/386, Windows/386, and XENIX 386).

Microprocessor Operating Modes

The 80386 microprocessor offers the following operating modes:

1. Real-Address Operating Mode

The 80386 microprocessor's real-address operating mode is entered when the system processing unit is powered up or a system reset occurs. The real-address operating mode addresses up to 1 Mbyte of system memory and allows 32-bit operands, but does not provide memory protection. Windows 2.0, all versions of MS-DOS, and nearly all industry-standard application software run in the real-address operating mode.

The real-address operating mode is compatible with operating systems written for the 8086 microprocessor. With a few differences (described in the *Intel 80386 Programmer's Reference Manual*), the 80386's real-address object code is compatible with the real-address object code of the 8088, 8086, and 80286 microprocessors.

2. Protected Operating Mode

The 80386 microprocessor's protected operating mode provides addressing beyond 1 Mbyte, and supports programs that use memory above 1 Mbyte (VDisk and Disc Cache, for instance). When the 80386 microprocessor is in the protected operating mode, its object code is compatible with that of an 80286 in the protected operating mode, but not with that of an 80286 in the real-address operating mode. Furthermore, if the 80386 is in the protected operating mode, its object code is not compatible with that of the 8088 or 8086 microprocessors.

3. Virtual-Address Operating Mode

The virtual-address operating mode allows multiple 8086 sessions of 1 Mbyte each and can provide access of up to 64 terabytes of virtual memory addresses. This mode supports 8088 and 8086 applications that run as a subset of the 80386 microprocessor's protected operating mode. In the virtual-address operating mode, the 80386 microprocessor's software and operating systems are compatible with those written for the 8088 and 8086 microprocessors.

Address Pipelining

Address pipelining allows the 80386 microprocessor's bus cycles to be overlapped, increasing bus throughput. For normal operation, address pipelining is enabled when the Processor/Memory PCA's Switch 1, setting 5, is set to the default ON position. Address pipelining is disabled when Switch 1, setting 5, is set to the OFF position.

2.3.1 I/O Address Map

Table 2-4 gives the I/O address map for the central processing unit. The HP Vectra RS uses the first 1024 I/O hex addresses, 000 through 3FF.

Table 2-4. I/O Address Map

Hex Address	I/O Address Description
000-00F	IPC* DMA Controller No. 1 Registers
010-01F	Reserved
020-021	IPC* Interrupt Controller No. 1 Registers
022	82Cxxx Index Register
023	82Cxxx Data Register
024-03F	Reserved
040-043	IPC* Counter/Timer Registers
044-05F	Reserved
060	8042 Keyboard Controller, Data Buffer
061	82301 Bus Controller (Port B) Status Register (Read/Write)
062	8042 Keyboard Controller, Data Buffer
063	82301 Bus Controller (Port B) Status Register (Read/Write)
064	8042 Keyboard Controller, Status/Command Buffer
065	8042 Port Expander (Read/Write)
066	8042 Keyboard Controller, Status/Command Buffer
067	8042 Port Expander (Read/Write)
068	HP 8042 Keyboard Controller Command Register
069	8042 Port Expander (Read/Write)
06A	HP 8042 Keyboard Controller Command Register
06B	Reserved
06C	1RD2 HP-HIL Master Link Controller Register 0
06D	1RD2 HP-HIL Master Link Controller Register 1
06E	1RD2 HP-HIL Master Link Controller Register 2
06F	1RD2 HP-HIL Master Link Controller Register 3
070	Real-Time Clock/CMOS RAM Address (D0 to D6),NMI Enable (D7) (Write)
071	Real-Time Clock/CMOS RAM Data (Read/Write)
072-077	Reserved
078	Hard Reset Enable/Disable (D7) (Write)
079-07F	Reserved
080-08F	IPC* DMA Page Register
090-09A	Reserved
09B	Mode Switch
09C-09F	Reserved

*For further mapping of these addresses, refer to the I/O Address Map for IPC (Integrated Peripheral Controller) components, in the "System Interface Printed Circuit Assembly" chapter.

Table 2-4. I/O Address Map (Continued)

Hex Address	I/O Address Description
0A0-0A1	IPC* Interrupt Controller No. 2 Register
0A2-0BF	Reserved
0C0-0DF	IPC* DMA Controller No. 2 Register
0E0-0EF	Reserved
0F0	Clear 80387 Coprocessor Busy
0F1	Reset 80387 Coprocessor
0F2-0F7	Reserved
0F8-0FF	80387 Coprocessor Command Registers
100-16F	Undefined
170-178	Secondary Hard Disc Drive Controller Registers
179-17F	Reserved
180-1EF	Undefined
1F0-1F8	Primary Hard Disc Drive Controller Registers
1F9-1FF	Reserved
200-207	Game Controller Registers
208-277	Undefined
278-27F	Parallel Port 2
280-2E7	Undefined
2E8-2EF	Serial Port 4
2F0-2F7	Undefined
2F8-2FF	Serial Port 2
300-307	Prototype Card
308-36F	Undefined
370-377	Secondary Flexible Disc Drive Controller Registers
378-37F	Parallel Port 1
380-38F	Synchronous Data Link Controller (SDLC) Registers, Bisynchronous 2
390-39F	Undefined
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Accessory Card
3C0-3CF	Enhanced Graphics Adapter
3D0-3DF	Color/Graphics Video Accessory Card
3E0-3E7	Undefined
3E8-3EF	Serial Port 3
3F0-3F7	Primary Flexible Disc Drive Controller Registers
3F8-3FF	Serial Port 1

2.4 Coprocessor

For models without cache, the HP Vectra RS supplies a socket on the Processor/Memory PCA for the industry-standard coprocessor (the Intel 80387) and/or the Weitek 1167 floating point coprocessor. For models with cache, the Processor/Memory PCA's socket is not used for coprocessors; instead, pin grid array sockets are provided on the Cache Memory System PCA for the Intel 80387 and/or the Weitek 3167.*

The 80387, the 1167, and the 3167 coprocessors are numeric processing units which significantly improve performance of those applications which take advantage of them, such as spreadsheets, and applications for science and engineering (including computer-aided design, engineering, and manufacturing.) The coprocessors interface directly with the 80386 microprocessor; they extend the 80386 instruction set by providing hardware for binary-coded decimal data and the high-precision integer functions and floating-point calculations otherwise performed by software. (Only applications with built-in support for these coprocessors will realize the performance improvements.)

If an 80387 coprocessor is installed, setting 1 of the Processor/Memory PCA's Switch 1 should be set to the OFF position in order to enable it. If the Weitek 1167 or 3167 coprocessor is installed, no settings need to be changed on Switch 1.

Coprocessor Clocking

Clocking for the coprocessor depends on:
(1) the type of coprocessor installed (Weitek 1167 or 3167 -- or the Intel 80387),
(2) the position of the Processor/Memory PCA's Switch 1, setting 6, and
(3) the HP Vectra RS model (RS/16 or RS/20).

If the 80387 coprocessor is installed, and if Switch 1, setting 6 is set to its default ON position, the 80387 operates in the synchronous mode, using the same clock (OSC2) used by the 80386 microprocessor. If Switch 1, setting 6 is set to the OFF position, the 80387 operates at an asynchronous speed setting, using the clock from OSC3, an oscillator that could be installed on the Processor/Memory PCA. (Because this asynchronous mode is not currently supported on HP Vectra RS products, Switch 1, setting 6 should always be set to the ON position.)

No settings need changed on Switch 1 if a 1167 or a 3167 coprocessor is installed, because these coprocessors use the same clock (OSC2) used by the HP Vectra RS's 80386 microprocessor.

* None of the HP Vectra RS models come standard with both coprocessors, but the Power User models do come standard with an 80387 coprocessor. The Intel 80387 coprocessors may be ordered from a local Hewlett-Packard dealter. Order the Weitek 1167 and 3167 coprocessors through MicroWay or a local Hewlett-Packard dealer.

Coprocessor Hardware Compatibility and Interface

The HP Vectra RS numeric coprocessor interface supports the Intel 80387 coprocessor and/or the Weitek coprocessors. (The RS/16 and RS/20 support the Weitek 1167; the RS/20C and RS/25C support the Weitek 3167.) The 80387 coprocessor is compatible with the 8087 and 80287 coprocessor instruction sets. However, the 1167 and 3167 coprocessors are not compatible with the 80387 instruction sets.

Intel 80387 Coprocessor Hardware Interface

If the 80387 coprocessor is installed, in order to enable it, setting 1 of Switch 1 on the Processor/Memory PCA should be set to the OFF position. Immediately after a system power-up or reset, the 80387 indicates its presence to the 80386 microprocessor by sending to the 80386, ERROR#, one of its control signals.* In recognition, the 80386 microprocessor will set the Extension Type (ET) bit of its Control Register 0.

The 80387 coprocessor is directly connected to the 80386 microprocessor via the local address and data bus. Three control signals (BUSY#, PEREQ, and ERROR#) synchronize the transfer of instructions and data between the 80386 and the 80387. When the 80386 selects the 80387, it asserts I/O address bit A31 so that the 80387 acts as an I/O device in a reserved I/O space. (For more information on the 80387 coprocessor, refer to Intel reference manuals.)

Weitek Coprocessor Hardware Interface

The Weitek coprocessor hardware interface is the same for both the 1167 and the 3167. If a Weitek coprocessor is installed, no Switch 1 settings on the Processor/Memory PCA need to be changed to enable it. During the Power-On Self-Test, system software senses the Weitek's presence by reading I/O hex address 009B, bit 2. If bit 2 indicates a low (logical 0), the Weitek is present, but if bit 2 indicates a high (logical 1), the Weitek is not present.

The Weitek coprocessor, a memory-mapped device that communicates with the 80386 microprocessor via the local address and data bus, responds to memory hex addresses C000 0000 through C3FF FFFF. (For more information on the Weitek coprocessor, refer to Weitek reference manuals.)

Coprocessor Operating Modes

Since all memory accesses are handled by the 80386 microprocessor, the 80387 coprocessor works the same whether the 80386 is executing in the real-address, the protected, or the virtual-address operating mode. The Weitek 1167 or 3167 can operate in the protected or virtual-address operating modes.

* The # symbol at the end of the 80386 microprocessor signal names is used by Intel to indicate that the active, or asserted, state occurs when the signal is at low voltage. When no # symbol is present after the signal name, the signal is asserted when at the high-voltage level.

2.5 Memory

2.5.1 Main Memory (DRAM)

The HP Vectra RS main memory (also known as system memory, system RAM, RAM, or DRAM) consists of dynamic RAM chips mounted on single in-line memory modules, available in 256-Kbyte or 1-Mbyte modules. The modules fit into 16 sockets, which are arranged in banks A, B, C, and D. (Refer to the figure in this chapter, "Processor/Memory PCA Component Layout" to locate the banks of sockets.)

Main Memory Configurations

Depending on the model number, the HP Vectra RS comes standard with 1 to 4 Mbytes of main memory. As explained in Table 2-5, this memory is expandable to 16 Mbytes by placing into the sockets even increments of the serial in-line memory modules.

Table 2-5. Main Memory Expansion

For DRAM of:	Insert These Modules*:	In These Sockets:
1 Mbyte	4 256-Kbyte modules	All A sockets
2 Mbytes	8 256-Kbyte modules	All A and B sockets
4 Mbytes	16 256-Kbyte modules or 4 1-Mbyte modules	All 16 sockets All A sockets
8 Mbytes	8 1-Mbyte modules	All A and B sockets
10 Mbytes	8 256-Kbyte modules-- and 8 1-Mbyte modules---	--In A and B (or C and D) sockets --In C and D (or A and B) sockets
16 Mbytes	16 1-Mbyte modules	All 16 sockets

* Contact your local Hewlett-Packard dealer for serial in-line memory module part numbers for the different HP Vectra RS models. Within a pair of banks (A and B, or C and D), the module types must be identical, but each pair of banks can use different types of modules. Bank A must be filled with modules before bank B is filled. If bank C is filled, bank D must also be filled.

Base RAM Configurations

Base RAM, the first 640 Kbytes or 512 Kbytes of main memory, can be configured as required by using the Processor/Memory PCA's Switch 1, setting 3. In the ON position, the main memory's base RAM is set to 640 Kbytes; in the OFF position, base RAM is set to 512 Kbytes.

Main Memory Architecture

The HP Vectra RS has a paged/interleaved main memory architecture, using an 82302 page/interleave memory controller that organizes main memory DRAM to decrease the number of accesses that incur a wait-state penalty.

Paged DRAM is organized into paged rows and columns. One memory strobe (the RAS, or row address strobe) generates the row address of the page; a second memory strobe (the CAS, or column address strobe) generates the column address. If access is required on the same page of DRAM, there may be zero wait states, but if access is required on a different page of DRAM, there is at least one wait state.

Interleaved DRAM is organized into four banks, with each bank having four single in-line memory module sockets. (When only the "A" bank of four sockets is filled, the system operates in the non-interleaved mode.) Because interleaving is done between pairs of banks, for the system to operate in the paged/interleaved mode, either two or four (never three) banks of sockets must be filled. For more information on DRAM, refer to the "Page Memory Controller" section in this chapter.

Memory Map

Figure 2-6 gives the HP Vectra RS memory map. As with industry-standard products, the first 1 Mbyte of main memory is reserved for industry-standard memory. The base RAM (either the first 512 or 640 Kbytes of main memory, depending on how RAM is configured, using Switch 1, setting 3) is used for MS-DOS applications. As shown on Figure 2-6, from hex address 000A 0000 to 000F FFFF, the system reserves main memory for video RAM, ROM on I/O accessory cards, option ROM, and BIOS ROM. Main memory from hex address 0010 0000 to 00FD FFFF is reserved for 32-bit dynamic RAM expansion, using the sockets for the serial in-line memory modules.

Upon power-up, the 64 Kbytes of option ROM at hex address 000E 0000 to 000E FFFF are automatically mapped to hex address 00FE 0000 to 00FE FFFF. Similarly, the 64 Kbytes of BIOS ROM at hex address 000F 0000 to 000F FFFF are automatically mapped to hex address 00FF 0000 to 00FF FFFF. (Option ROMs are also mapped at hex address FFFE 0000 to FFFE FFFF, and BIOS ROMs are also mapped at hex address FFFF 0000 to FFFF FFFF. However, the upper eight bits of these addresses do not appear on the backplane I/O bus.)

For the RS/20C and RS/25C, the non-cacheable areas include hex address 000A 0000 to 000D FFFF and hex address 8000 0000 to FFFF FFFF. All other areas are cacheable.

Cacheable Areas (1)	Hex Addresses	Description	Non-cacheable Areas (1)
×	0000 0000 0009 FFFF	512 or 640 Kbytes of 32-bit DRAM (Base RAM) (2)	
	000A 000C 000B FFFF	128 Kbytes Video RAM	×
	000C 0000 000D FFFF	128 Kbytes ROM on I/O Accessory Cards (includes Video BIOS)	×
×	000E 0000 000E FFFF	64 Kbytes Option ROM	
×	000F 0000 000F FFFF	64 Kbytes BIOS ROM	
×	0010 0000 00FD FFFF	15 Mbytes 32-bit DRAM Expansion	
×	00FE 0000 00FE FFFF	64 Kbytes Option ROM (3)	
×	00FF 0000 00FF FFFF	64 Kbytes BIOS ROM (4)	
	8000 0000 FFFF FFFF	Coprocessor Area	×

(1) RS/20C and RS/25C only.

(2) Base RAM can be configured to either 512 Kbytes or 640 Kbytes, using Switch 1, setting 3, on the Memory/Processor PCA.

(3) Upon power-up, automatically mapped from hex address 000E0000 to 000EFFFF.

(4) Upon power-up, automatically mapped from hex address 00F00000 to 000FFFFF.

Figure 2-6. HP Vectra RS Memory Map

Main Memory Operation

1. Refresh

A refresh cycle begins with the 82206 Integrated Peripheral Controller's OUT1 signal generating a refresh request (REFREQ) to the 82301 bus controller every 15 microseconds. All DRAM is refreshed within 4 milliseconds (for 256-Kbyte DRAM) to 8 milliseconds (for 1-Mbyte DRAM). A refresh cycle for one bank of DRAM requires seven CLK2 cycles, with refreshes to additional banks staggered by one CLK2 cycle, so that four banks take 10 CLK2 cycles to be refreshed.

To perform a refresh, the bus controller generates a hold request (HOLD) to the 80386 microprocessor, which subsequently generates a hold acknowledge (HLDA) to the bus controller. The bus controller then issues a refresh signal (REF*) which goes to the 82302 page memory controller, the 82303 and 82304 address buffers, and the backplane I/O. Upon receiving REF*, the page memory controller strobes the refresh row address into the banks of DRAM. When the address buffers receive the REF* signal, system bus address lines 23 to 12 go low, while system bus address lines 11 to 2 are driven by a 82304 address buffer counter, which represents the refresh row address.

The REF* signal goes to the backplane I/O and indicates to I/O accessory cards that a refresh operation is taking place. In addition, an I/O accessory card can issue a REF* signal to initiate a refresh request to the bus controller, the page memory controller, and the address buffers, independent of the Integrated Peripheral Controller's periodic refresh requests.

2. Access Time

Main memory for the RS/16 and RS/20C uses DRAM with an access time of 100 nanoseconds and a cycle time of approximately 190 nanoseconds. Main memory for the RS/20 and RS/25C uses DRAM with an access time of 80 nanoseconds and a cycle time of approximately 165 nanoseconds. (Hewlett-Packard assumes no responsibility for the access time of memory modules not supplied by HP-approved vendors.)

3. Parity

Parity is generated for each byte of system RAM during write operations, and checked during read operations. If a parity error occurs, a parity check signal LPAR* is generated and sent to the page memory controller, allowing a non-maskable interrupt.

For memory write operations, the write data go through the data buffers, which generate low and high parity bits, PL0-PL3 and PH0-PH3, representing the parity of lower and upper bits of each byte written. PL0-PL3 and PH0-PH3 are exclusive ORed together to form memory parity bits MP0-MP3, representing the parity for byte 0 to 3 for the data being written. MP0-MP3 are then written into the proper parity bits in the DRAM serial in-line memory module banks.

For memory read operations, data from the DRAM are read into the data buffer, which produces parity bits PL0-PL3 and PH0-PH3. These parity bits go to the 82306 control buffer. MP0-MP3 are also read from DRAM and are sent to the control buffer. MP0-MP3 (which represent the parity as determined when the data were written) are compared with PL0-PL3 and PH0-PH3, the parity found when data are read back. The control buffer then produces a parity output signal, LPAR*, sent to the page memory controller, which is active if a parity error exists.

4. Self-tests

Upon power-up, the main memory goes through a self-test, as discussed in the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

* Active low.

2.5.2 Read-Only Memory (ROM)

For all models, the System Interface PCA provides two 32-Kbyte ROM chips (containing the BIOS firmware) and sockets for two 32-Kbyte option ROM chips. (For more information on ROM, refer to the "System Interface Printed Circuit Assembly" chapter.)

2.5.3 Cache Memory (SRAM)

The HP Vectra RS/20C and RS/25C models have cache memory, consisting of 32 Kbytes of static RAM, mounted on the Cache Memory System PCA. While main memory provides numerous slow dynamic RAMs (DRAMs) to store all data, the cache memory provides a few fast static RAMs (SRAMs) to store only that data frequently accessed. By providing fast local storage, cache memory decreases the time it takes the 80386 microprocessor to access data needed for processing. (For more information on cache memory, see the "Cache Controller" and "Cache Bus" sections in this chapter.)

2.6 Page Memory Controller

The 82302 Page Memory Controller (1) controls all main memory accesses from the 80386 microprocessor, direct-memory accesses, and refreshes and (2) organizes the main memory DRAM into paged and interleaved DRAM to decrease the number of accesses incurring a wait state penalty. Clocking for the page memory controller comes from the signal 302CLK2, which originates from the 82301 bus controller.

Refer to Figures 2-7 and 2-8. DRAM chips are physically organized onto a "single in-line memory module." In turn, four of these modules make up a 4-byte-wide bank. Not including parity bits, if the four modules making up a bank use 256-Kbyte DRAM chips, the bank has 1 Mbyte of DRAM; if the four modules making up a bank use 1-Mbyte DRAM chips, the bank has 4 Mbytes of DRAM. (Refer to the "Main Memory" section and the "Main Memory Expansion" table in this chapter for more on DRAM's physical organization.)

As shown in Figure 2-8, the page memory controller logically organizes DRAM as *pages*. For each 256-Kbyte module, there are 512 pages (rows), with each page having 512 bytes (1 byte for each 512 columns). Since a bank has 4 modules, a banked page has 2 Kbytes of dynamic RAM (512 bytes X 4 modules = 2 Kbytes). This paged memory can be accessed as 8-bit bytes, 16-bit words, or 32-bit words.

To access memory, the page memory controller issues to each accessed module a row address and then a column address. The row address indicates the page, while the column address indicates which of the 512 bytes on that page (row) are to be accessed. The row and column addresses are multiplexed over MA0-MA7 and DA8-DA9 from the page memory controller and are latched into a module by the appropriate row address strobe (RAS) and column address strobe (CAS) signals. To achieve 8-bit, 16-bit, or 32-bit operations, the CAS signal is ANDed with the appropriate latch byte enable (LBE) signal from the 82306 control buffer. If the next access is within the current page (row), a new row address does not need to be issued, just a new column address and CAS signal, resulting in fewer wait states.

If more than one bank of sockets are filled with DRAM modules, the page memory controller *interleaves* pages between banks, with even pages on one bank, and odd pages on the next bank. Interleaving requires that two or four (but never one or three) banks of sockets be filled with DRAM modules. Interleaving pages on different banks can minimize the number of row addresses and RAS signals required, as the page memory controller has a separate page register for each bank. If bank A has an even page number as its current page, and bank B has an odd page number as its current page, no new row addresses and RAS signals are needed as long as accesses are within these two pages.

Once the 80386 microprocessor generates a local address, the page memory controller decodes the type of access according to its various configuration registers. These registers determine if a ROM access, an access of the backplane I/O, or a DRAM access is required. If a DRAM access is required, the page memory controller accesses the DRAM according to configuration registers that state what type of DRAMs are used and how many wait states are desired.

In direct-memory accesses (DMA), only 8-bit and 16-bit operations are supported. The address on the local address bus comes from the System Interface PCA's 82206 Integrated Peripheral Controller via the peripheral address bus and the address buffers. The page memory controller decodes the address as it would an access from the 80386 microprocessor.

A refresh access is initiated when the page memory controller receives a REF* input from the 82301 bus controller. (For more information on the 82302 page/interleave memory controller, refer to the Chips and Technologies data sheet, *CS8230: AT/386 CHIPSet.*)

* Active low.

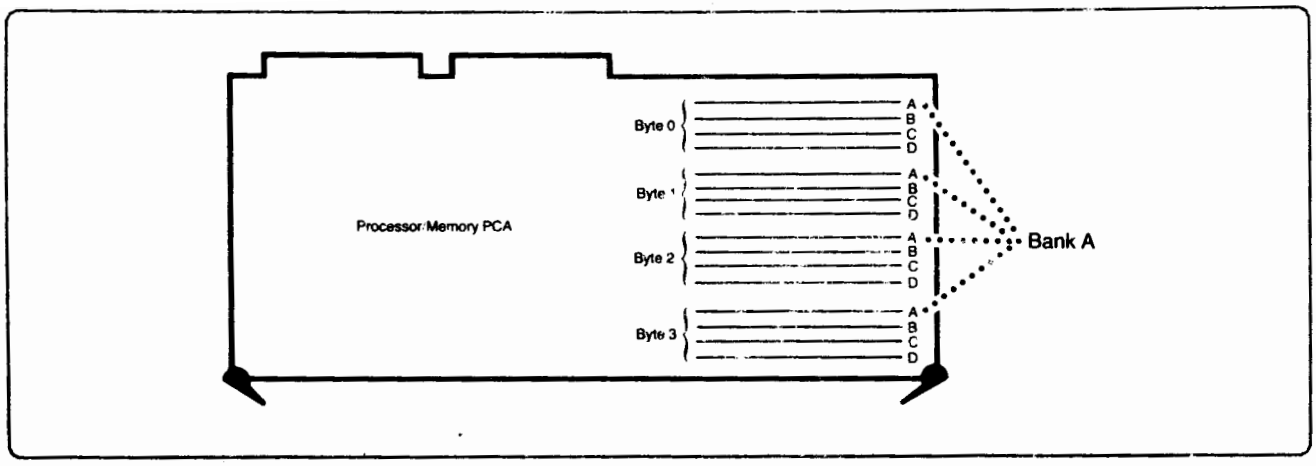
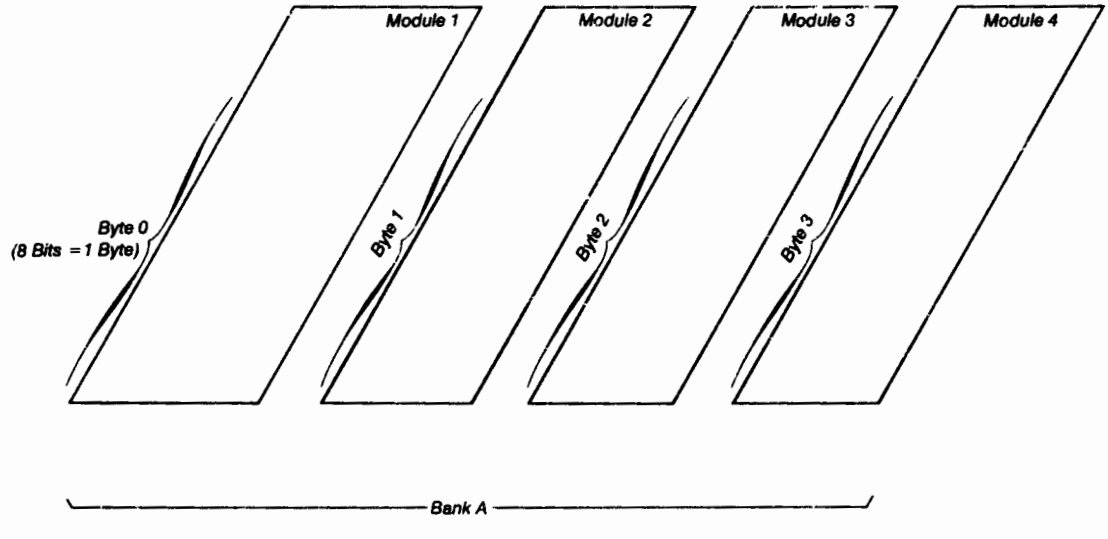


Figure 2-7 (a). DRAM Physical Organization (Board/Module View)



Example 1: Row address strobe (RAS) selects a row from the 512 possible rows on the DRAM chips on module 1. Column address strobe (CAS) selects a column from the 512 possible columns on the DRAM chips on module 1. The conjunction of the row and column address strobes results in an 8-bit (1-byte) access.

Example 2: RAS selects a row from the 512 possible rows on the DRAM chips on modules 1, 2, 3, and 4. CAS selects a column from the 512 possible columns on the DRAM chips on modules 1, 2, 3, and 4. The conjunction of the row and column address strobes, across all four modules, results in a 32-bit (4-byte) access.

Figure 2-7 (b). DRAM Physical Organization (Module/Chip View)

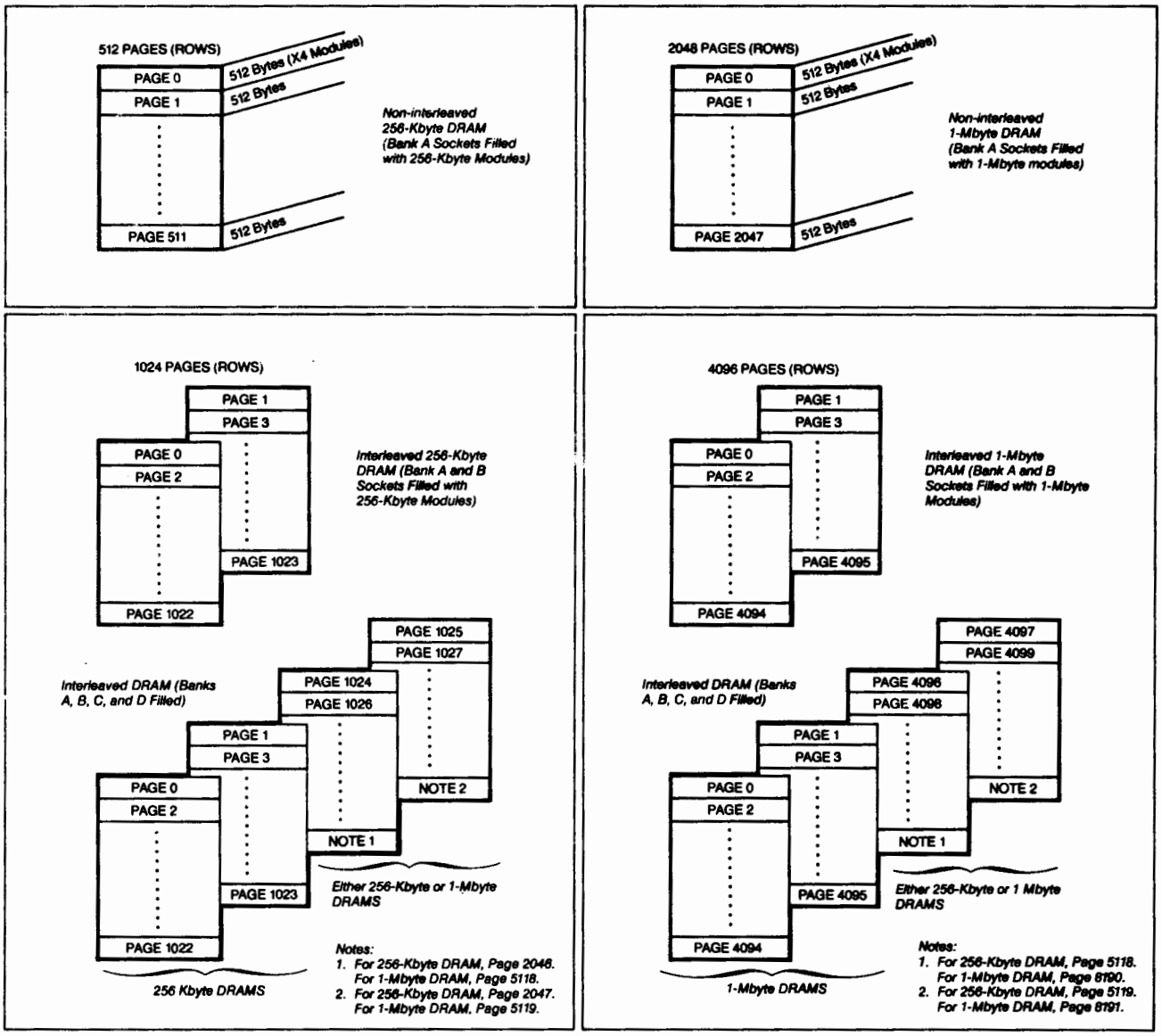


Figure 2-8. DRAM Logical Organization

2.7 Cache Controller

The 82385 Cache Controller uses the 80386 microprocessor's address bus bits to copy data most recently used, *from* the main memory's dynamic RAM (DRAM) *to* the cache memory's static RAM (SRAM). As a result, data that the 80386 microprocessor needs most often are placed in cache memory for fast access by the 80386. [However, when data change in the DRAM as a result of a direct-memory access (DMA) of the DRAM by an I/O device, the 82385 does not copy these data to the SRAM, but rather flushes the out-of-date data from the SRAM.] Clocking for the cache controller, which is the same as that for the 80386 microprocessor, comes from OSC2, but is amplified by a 74AC541.

2.7.1 Cache Controller Structure

Cache Controller Organization of DRAM

The cache controller organizes DRAM by interpreting the state of information from the 80386 microprocessor's 32-bit address bus. By organizing DRAM, the cache controller can quickly determine if instructions and data which the 80386 wants to access are available in SRAM cache memory.

1. The 80386's four gigabytes of possible address space are organized into "pages," where address bus bits A32 to A14 designate which one of 262,144 possible "pages" the 80386 is accessing.
2. Each page has 512 "sets." Address bus bits A13 to A5 determine which one of the 512 sets is accessed by the 80386.
3. Each set, in turn, has eight 32-bit "lines." Address bus bits A4 to A2 determine which one of the eight lines is accessed by the 80386.

Cache Controller Organization of SRAM

The cache controller, which is configured for the two-way set associative mode, organizes SRAM similarly to how it organizes DRAM.

1. The 32 Kbytes of SRAM are organized into two 16-Kbyte "banks," Bank A and Bank B.
2. Each bank, which is the same size as a page of DRAM, is organized into 512 "sets."
3. Each set, in turn, has eight 32-bit "lines."

Cache Controller Directory Organization

For each of the 512 sets within the cache controller, there is a set entry which includes a directory for bank A, a least-recently used bit (LRU), and a directory for bank B. The set entry number points to the same set number in DRAM; only the particular page and line is in question. The LRU bit indicates which bank was least recently used. The bank directories, which track which locations in DRAM are currently copied into SRAM, have three parts:

1. a "tag," an 18-bit number indicating which page of DRAM has that set entry's contents,
2. a "tag valid bit," a bit which indicates that the 18-bit tag is valid, and
3. "line valid bits," 8 bits that indicate which lines in a set are valid. (Within a set, no lines may be valid, or from 1 to 8 lines within a set may be valid.)

2.7.2 Cache Controller Operations

The cache controller operations include the following: (1) read hit, (2) read miss, (3) write hit, (4) write miss, (5) direct-memory access (DMA) of main memory, and (6) cache flush.

(1) Read Hit Operation

If there is both a tag match and a line match, then there is a read hit. The cache controller then allows the 80386 microprocessor to access the appropriate line in SRAM and the data go to the 80386 microprocessor for processing.

(2) Read Miss Operation

If there is a *tag* miss, the cache controller allows a normal DRAM access to occur, and data go over both the 80386/82385 local data buses to the 80386 microprocessor. All control signals from the 80386 microprocessor, such as the memory I/O (M/IO*) and read/write (W/R*) are sent to the 82385 cache controller which, in turn, duplicates these signals on the 80386 local bus.

If there is a tag match, but a *line* miss, the cache controller allows a normal DRAM access to occur, and data go over both the 80386/82385 local data buses to the 80386 microprocessor.

(3) Write Hit Operation

If there is a write hit, the SRAM cache memory location is updated. (When SRAM cache memory is updated, only the active byte enables are selected.)

(4) Write Miss Operation

A write miss operation has no affect on SRAM cache memory or the cache controller. The 80386 performs a normal write to DRAM, and 80386 control lines such as M/IO* and W/R* are sent to the cache controller, which duplicates these signals on the 82385 cache controller's local bus.

(5) Direct-Memory Access Operation

If the DMA controller (discussed in the "DMA Controller" section in the "System Interface PCA chapter) or another bus master writes data into a DRAM location, and those data are also in SRAM cache memory. As a result, the 80386 microprocessor will not read old data from SRAM cache memory.

(6) Cache Flush Operation

When the cache flush input is active, all the tag valid bits in the cache directory are cleared.

2.7.3 Non-Cacheable Memory Areas and Non-Cache Operations

Non-Cacheable Memory Areas

For the RS/20C and RS/25C, the non-cacheable areas of the memory map include hex address 000A 0000 to 000D FFFF and hex address 8000 0000 to FFFF FFFF. Using the non-cacheable access (NCA*) input on the 82385 cache controller tells the cache controller whether the current 80386 address is cacheable or not. This NCA* signal, driven by the NCA_PAL (a signal from programmable array logic), is predefined by the combination of A15 to A23, and A31.

Non-Cache Operations

Certain operations are non-cacheable, including the following:

I/O operations
Interrupt Acknowledge Cycles
Halt/Shutdown

Note:

In all non-cache operations, the 82385 cache controller duplicates the control signals issued by the 80386 microprocessor.

* Indicates active low.

2.8 Bus Controller

The 82301 bus controller works in conjunction with the 82306 control buffer to generate clocking for the 80386 microprocessor, the coprocessor, and the page memory controller. The bus controller also provides the generation and synchronization of control signals for all buses. In addition, it offers an industry-standard Port B register and optional speeds for timing-dependent software.

Bus Controller Clocking

The clock input to the bus controller is provided by ATCLK1 (from the 16-MHz OSC1) and CLK2IN (from OSC2). The bus controller's output CLK2 signal (to the microprocessor, coprocessor, and page memory controller) is 32 MHz for the RS/16 model, 40 MHz for the RS/20 and RS/20C models, and 50 MHz for the RS/25C model. The bus controller's SCLK signal, used in various timing circuits on the Processor/Memory PCA, equals one-half of the CLK2 signal. (By pressing the keys <CTRL>, <Alt>, and < \ >, CLK2 can be derived from OSC1 for a 16-MHz signal.)

The bus controller's ATSCLK signal is provided to the 82306 control buffer and buffered to drive the clock signal SYSCLK, the signal for the industry-standard backplane I/O bus. In addition, ATSCLK is sent to the 82206 Integrated Peripheral Controller. Through software control, ATSCLK's frequency can be selected as (1) 8 MHz, asynchronous with CLK2 or (2) the speed of OSC2, divided by 2, but synchronous with CLK2. (For more information, refer to Chips and Technologies reference manuals.)

Bus Arbitration

The bus controller synchronizes control of all bus activities. For direct-memory accesses (DMA), the bus controller accesses memory as described in the section "DMA Controller" in the "System Interface PCA" chapter. The bus controller also has the following two state machines that control access to devices by the 80386 microprocessor:

1. The *local bus state machine* controls accesses by the 80386 microprocessor to devices on the local bus. It also supports 32-bit transfers between the 80386 and system memory (or memory-mapped I/O), but does not convert the size of data.

2. The *AT (industry-standard) bus state machine* controls the 80386 microprocessor's accesses to devices on non-local buses. It provides sequencing and timing controls (including wait state generation) for status and command phases of the different bus cycles. In addition, it generates action code control signals that go to the data buffers for data size conversions.

Bus Controller Reset Control

When the power supply's PFAIL signal goes high, it generates the bus controller's RESET1* signal, which activates the bus controller's RESET3 and RESET4. Writing FEh to I/O port 64 makes RESET2* go low, activating the bus controller's RESET3.

RESET3 resets the 80386 microprocessor, the Intel 80387, and/or the Weitek coprocessor, and various Processor/Memory PCA timing circuits. RESET4 provides the backplane I/O connector slots with a reset. In addition, it resets the 82302 page memory controller on the Processor/Memory PCA and the following on the System Interface PCA: 82206 Integrated Peripheral Controller, 1RD2 HP-HIL Master Link Controller (MLC), 8042 keyboard controller, and the 8042 port expander.

* Active low.

2.9 Control Buffer

Refer to the figure in this chapter, "Processor/Memory PCA Block Diagram." The 82306 control buffer receives a 14.318 MHz signal (OSC4), which it divides by 12 to generate a 1.19 MHz signal to the 82206 Integrated Peripheral Controller's timer 0, counter 1, and counter 2. The control buffer also provides the byte enable latch which, during memory cycles, holds valid the byte enables from the 80386 microprocessor.

The control buffer checks parity by generating full read/write parity from the 82305 data buffer's partial parity bits. [For more information on parity, refer to the "Main Memory (RAM)" section in this chapter.] In addition, the control buffer provides drivers for control signals on the backplane I/O. Furthermore, the 82306 control buffer generates some of the signals used by the 82301 bus controller to control bus accesses.

2.10 Address Buffers

Refer to the figure in this chapter, "Processor/Memory PCA Block Diagram." The address buffer for the HP Vectra RS consists of an 82303 high address buffer and an 82304 low address buffer, which support transfers over the following buses:

1. LA, the local address bus to the 80386 microprocessor and the coprocessor(s)
2. SA, the system address bus for the backplane I/O
3. XA, the peripheral address bus for the 8042 keyboard controller, the 8042 port expander, 1RD2 HP-HIL MLC, and the 82206 Integrated Peripheral Controller

The 82303 high address buffer acts as a buffer for address bits LA31 through LA12, SA23 through SA12, and XA23 through XA 12. The 82304 low address buffer acts as a buffer for address bits LA11 through LA0, SA11 through SA0, and XA11 through XA0. The 82303 high address buffer provides address decoding signals required by other chips such as the 82302 page memory controller; the 82304 low address buffer provides address decoding signals required by peripheral devices. In addition, the 82304 low address buffer provides refresh address generation for the system address bus.

The high and low address buffers buffer the interface between the LA, SA, and XA buses, according to various control line states. Both the high and low address buffers directly interface to the 24-bit SA bus and the 24-bit XA bus via bidirectional drivers.

2.11 Data Buffers

Refer to the figure in this chapter, "Processor/Memory PCA Block Diagram." The data buffer for the HP Vectra RS consists of two 82305 data buffers, which support transfers over the following buses:

1. LD, the local data bus to the 80386 microprocessor and the coprocessor(s)
2. MD, the memory data bus to the dynamic RAM
3. RD, the ROM data bus connected to the BIOS ROMs
4. SD, the system data bus for the backplane I/O, connected to RD by a transceiver
5. XD, the peripheral data bus for the 8042 keyboard controller, 8042 port expander, 1RD2 HP-HIL MLC, and the 82206 Integrated Peripheral Controller, connected to SD by a transceiver

Via LD and MD, the data buffers support data transfers between (1) the 80386 microprocessor and (2) the system RAM. Via LD, RD, and SD, the data buffers also support data transfers between the 80386 and the industry-standard backplane I/O connector slots. During direct-memory accesses (DMA), the data buffers connect RD to both LD and MD. In addition, the 82305 data buffers provide data bus connections that convert data to a size compatible with backplane I/O operations. (For more information, refer to the Chips and Technologies data sheet, *CS8230: AT/386 CHIPSet.*)

On the RS/20C and RS/25C, as shown in the figure in this chapter, "Cache Memory System PCA Block Diagram," the Cache Memory System PCA has data transceivers which amplify data signals to and from the 80386 microprocessor and the cache memory.

Control of Data Bus Buffers

According to signals received from the bus controller and the page memory controller, the 82305 data buffers determine (1)which data buses are active (i.e., connected) and (2)the subsequent direction for data bus buffer drivers.

Data Conversion

The data buffer converts data to a size permitting the 80386 microprocessor to access the backplane I/O bus. Data are converted via action code control signals from four bus controller lines to the data buffer; these codes control the connection of bus bits between (1)the system data bus for the backplane I/O and (2)either the local data bus or the memory data bus.

2.12 Local Bus

Refer to this chapter's figure, "Processor/Memory PCA Block Diagram." The local bus (LBUS), which connects the 80386 microprocessor to the rest of the system, consists of the local address bus (LA), the local data bus (LD), bus status lines, and bus control lines for the 80386 microprocessor [and the coprocessor(s), if installed].

Separate from the local data bus, the local address bus generates 32-bit addresses. Its 30 address lines (LA31 to LA2) indicate a 4-byte location, from which the local address bus's four byte enables (BE3* to BE0*) select the bytes to be enabled. The 32 local data bus lines (LD31 to LD0) transfer either 8, 16, 24, or 32 bits of data. The local bus status lines (Read/Write, Memory I/O, Data Control, and Lock) establish the type of bus cycle to be performed. The 82301 bus controller and the 82306 control buffer use the local bus control lines to control the bus cycle on a cycle-by-cycle basis.

At the start of a local bus cycle, the 80386 microprocessor places on the local address bus valid address signals which go to: (1) the address buffers and then to other buses and to (2) the 82302 page memory controller, which interfaces with the DRAM and (3) the coprocessor(s). Status signals corresponding to the bus cycle to take place are then sent to the 82301 bus controller, the 82306 control buffer, and the coprocessor(s). Data to/from the 80386 microprocessor are sent over the local data bus to/from the data buffers.

2.13 Memory Bus

Refer to the figure in this chapter, "Processor/Memory PCA Block Diagram." The memory data bus (MD), which via the data buffer interfaces to the local data bus or the ROM data bus, is 36 bits wide (32 data bits, with 4 parity bits). The memory address bus (MA), is a 8-bit bus (MA0 to MA7) from the 82302 page memory controller that accesses a particular DRAM location. (For more information on how memory accesses are performed, refer to the section in this chapter, "Page Memory Controller.")

2.14 Read-Only Memory Data Bus

Refer to the figure in this chapter, "Processor/Memory PCA Block Diagram." All data coming from the BIOS ROMs or option ROMs, or going to or from the peripheral data bus or the backplane I/O data bus, go over the 16-bit ROM data bus (RD).

Via the data buffer, the local data bus and the memory data bus interface with RD. Through a transceiver, RD interfaces with the backplane I/O data bus, which in turn, interfaces with the peripheral data bus through another transceiver.

2.15 Cache Bus

Refer to the figure in this chapter, "Cache Memory System PCA Block Diagram." The HP Vectra RS cache bus (the 82385 Local Data Bus) uses the same clock as the 80386 microprocessor, OSC2. The address lines used to address cache memory (MA2 to MA13), originate from the 80386 address bus. Data from cache memory (D0 to D31) are connected to the 80386 local data bus (D0 to D31). Finally, control lines to cache memory are provided by the 82385 Cache Memory Controller.

2.16 Backplane I/O Bus

Refer to the figure in this chapter, "Processor/Memory PCA Block Diagram." The HP Vectra RS backplane I/O bus, an industry-standard 8-MHz bus (also known as the system bus, or SBUS), is separate from the system's memory bus. It connects, to the rest of the computer system, two 8-bit and six 16-bit backplane I/O connector slots. (Refer to the chapter "System Interface Printed Circuit Assembly" for a discussion of the backplane I/O connector slots.)

The backplane I/O's system address bus (SA) is a 24-bit address bus, connected to the 82303 and 82304 address buffers on the Processor/Memory PCA, for connection to other address buses in the system. Backplane I/O connector slots can receive an address from any of the other address buses or generate an address to any of the other buses, depending on the operation involved. (For more information, refer to the section on "Address Buffers" in this chapter.)

The backplane I/O's system data bus (SD) is a 16-bit data bus over which data to/from the backplane I/O connector slots are sent. These data, in turn, are sent over the ROM data bus to the 82305 data buffers on the Processor/Memory PCA for connection to the rest of the system.

If a backplane I/O connector slot needs control of the system, MASTER* is held low, and an address originating from an I/O accessory card is sent over SA to other address buses in the system. If the 80386 microprocessor needs to access a backplane I/O connector slot, an address is sent over the local address bus, through the address buffers, and then to SA. During direct-memory access (DMA) operations, an address originating from the Integrated Peripheral Controller's DMA controller is sent over the Peripheral Bus to both the SBUS and the local bus.

Backplane I/O Bus Clock

For this section, refer to this chapter's table, "Processor/Memory PCA Switch 1 Settings."

If the Processor/Memory PCA Switch 1, setting 2 is ON, the clock for the backplane I/O bus is asynchronous to the 80386 microprocessor and one-half the speed of OSC1 (8 MHz). If the Processor/Memory PCA Switch 1, setting 2 is OFF, the clock for the backplane I/O bus is synchronous to the 80386 microprocessor and one-half the speed of OSC2: 8 MHz, 10 MHz, or 12.5 MHz, depending on the Vectra RS model. (This option is to be used only if all accessory cards inserted in the backplane I/O connector slots can be run at a speed greater than 8 MHz.)

For all models, the clock driving the 80386 microprocessor may be switched to a 16-MHz clock as required by some industry-standard operations. When this is the case, the backplane I/O bus clock is always 8 MHz, regardless of the position of Switch 1, setting 2.

* Active low.

2.17 Peripheral Bus

Refer to the figure in this chapter, "Processor/Memory PCA Block Diagram." The peripheral bus (XBUS) connects to the 80386 microprocessor the following controllers:

1. 82301 bus controller
2. 82302 page memory controller
3. 82206 Integrated Peripheral Controller (on the System Interface PCA)
4. IRD2 HP-HIL MLC (on the System Interface PCA)
5. 8042 keyboard controller (on the System Interface PCA)
6. 8042 port expander (on the System Interface PCA)

The 24-bit peripheral address bus (XA) connects the controllers to the 82303 and 82304 address buffers on the Processor/Memory PCA, for connection to the local address bus. Via the local address bus and XA, the 80386 microprocessor can access the various controllers' registers.

The 8-bit peripheral data bus (XD) interfaces to the backplane I/O system data bus via a transceiver and allows the 80386 microprocessor to read data from or write data to the controller registers. The backplane I/O (system) data bus, in turn, interfaces with the ROM data bus via another transceiver. Via the data buffer, the ROM data bus then connects to the local data bus or the memory data bus.

During DMA cycles, the 82206 Integrated Peripheral Controller generates a DMA address and sends it over the XA bus, which is connected to the local address bus and the backplane I/O system address bus via the address buffer. The BIOS ROMs are addressed through the XA bus; however, data are read directly over the ROM data bus.

2.18 Processor/Memory PCA Switch 1

The Processor/Memory PCA's Switch 1 is shown in Figure 2-9. Table 2-6 gives its possible settings.

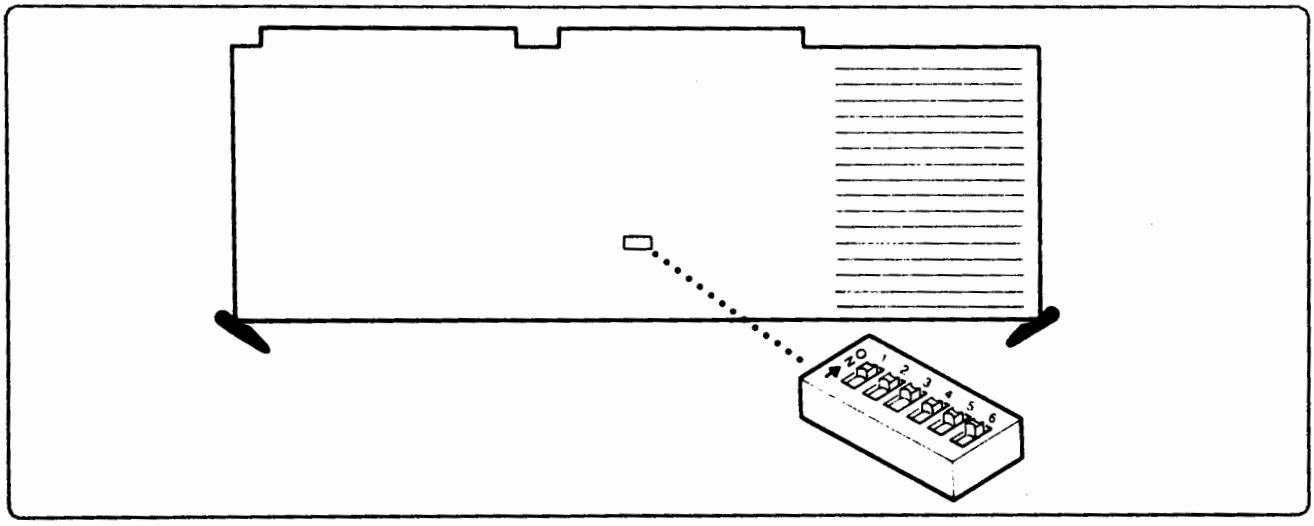


Figure 2-9. Processor/Memory PCA Switch 1

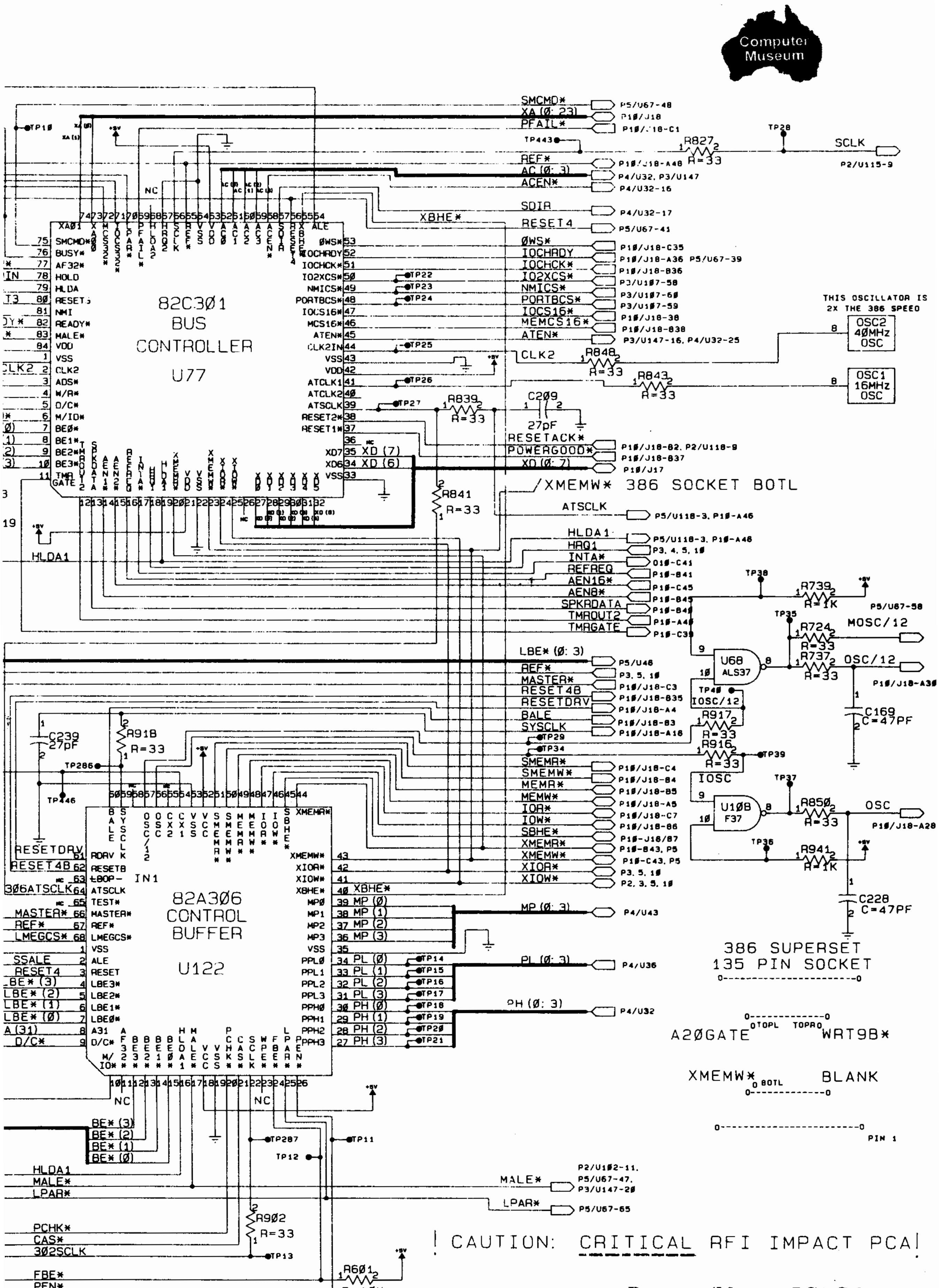
Table 2-6. Processor/Memory PCA Switch 1 Settings

Setting	On (Default Setting)	Off
1*	80387 coprocessor disabled	80387 coprocessor enabled
2	Backplane I/O channel speed: For RS/16 - 8 MHz asynchronous For RS/20 - 8 MHz asynchronous For RS/20C - 8 MHz asynchronous For RS/25C - 8 MHz asynchronous	Backplane I/O channel speed: For RS/16 - 8 MHz synchronous For RS/20 - 10 MHz synchronous** For RS/20C - 10 MHz synchronous** For RS/25C - 12.5 MHz synchronous**
3	Base RAM set to 640 Kbytes	Base RAM set to 512 Kbytes
4	Option ROM enabled	Option ROM disabled. (System will not boot if set to OFF.)
5	80386 microprocessor address pipelining enabled	80386 microprocessor address pipelining disabled. Do not set to OFF.
6*	Synchronous speed setting for 80387 coprocessor, using clock used for 80386 microprocessor (OSC2)	Asynchronous speed setting for 80387 coprocessor (only), using clock from OSC3, the Processor/Memory PCA's optional oscillator***.

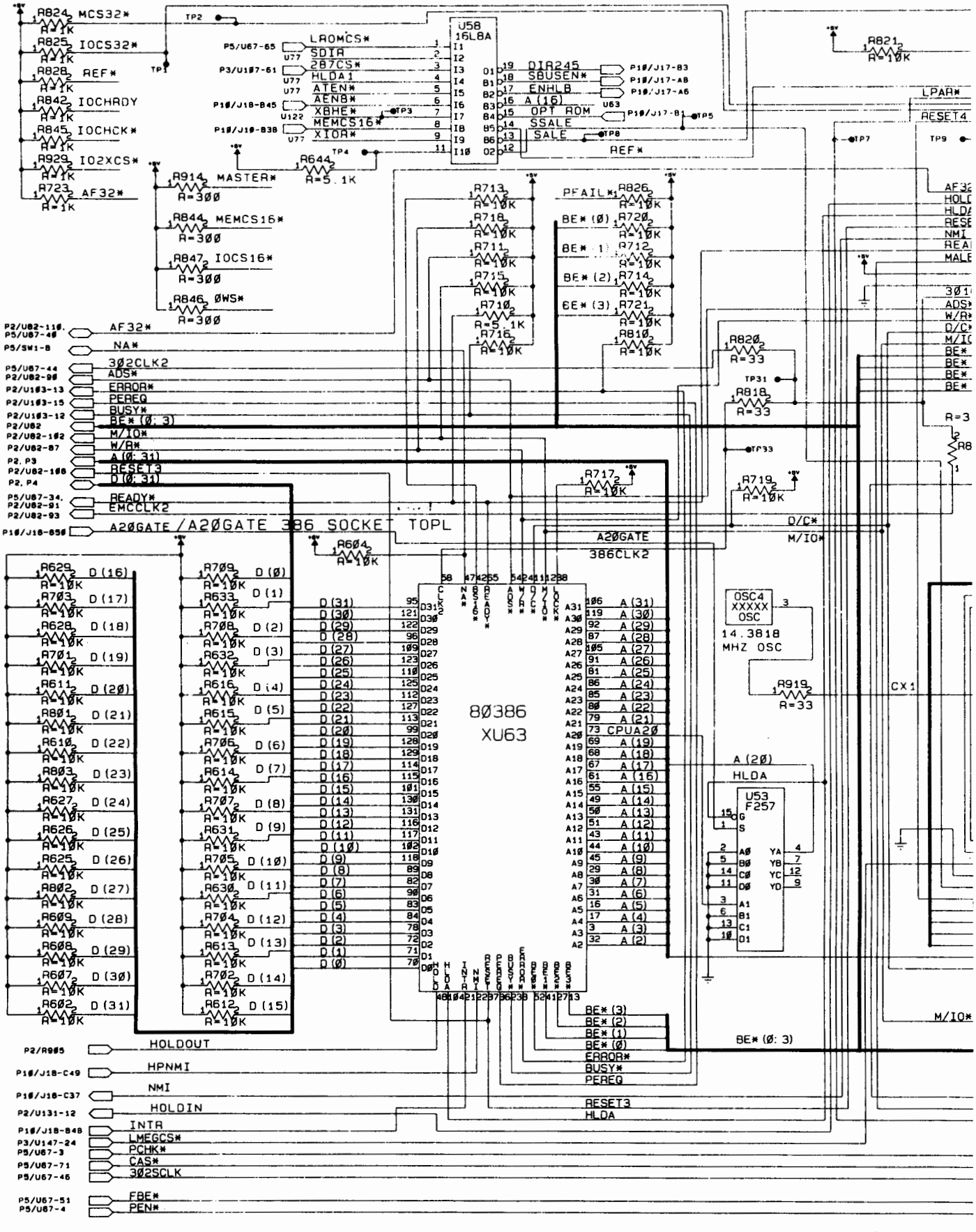
* The Weitek 1167 and 3167 coprocessors are not affected by setting 1 or setting 6.
** To be used ONLY if all accessory cards are capable of operating at the greater speed.
*** Not currently installed or supported. Do not set to OFF.

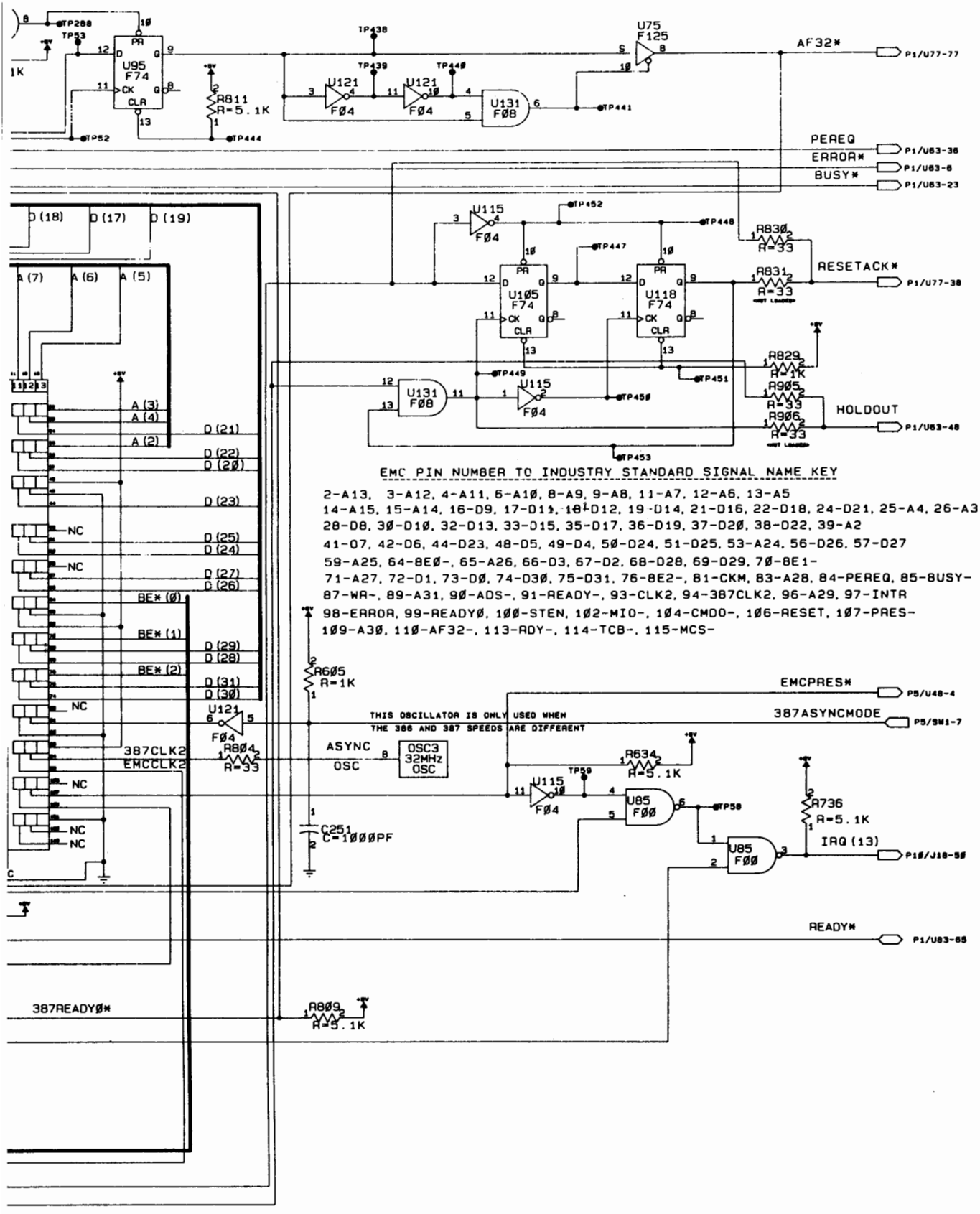
2.19 Processor/Memory PCA and Cache Memory System PCA Schematics

To help understand the Processor/Memory System PCA and Cache Memory System PCA, schematics are given on the following pages. Schematics for the System Interface PCA and the Input Device Connector PCA are given at the end of the chapter, "System Interface PCA." (Hewlett-Packard does not guarantee the accuracy of the schematics.)



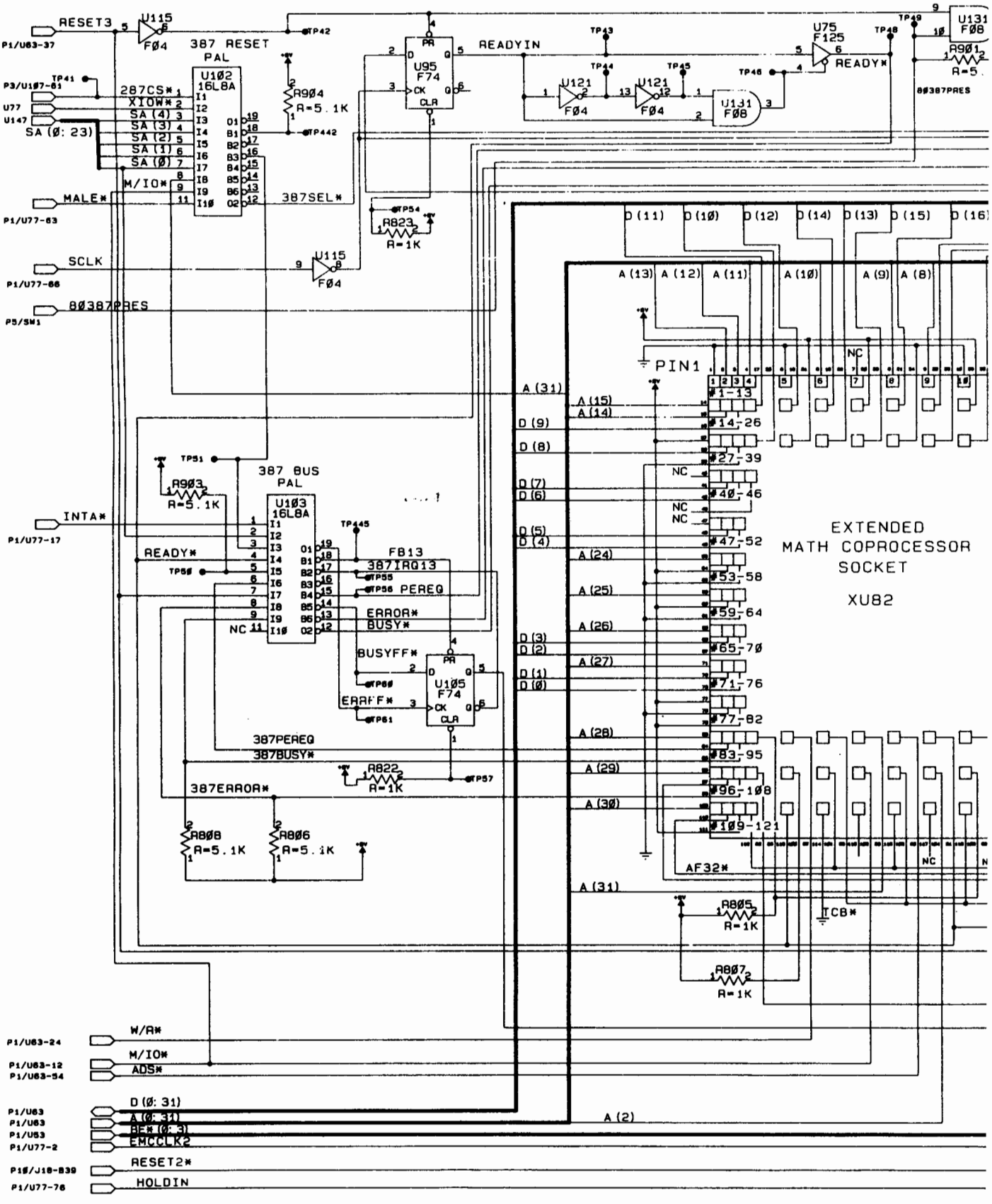
Processor/Memory PCA Schematic

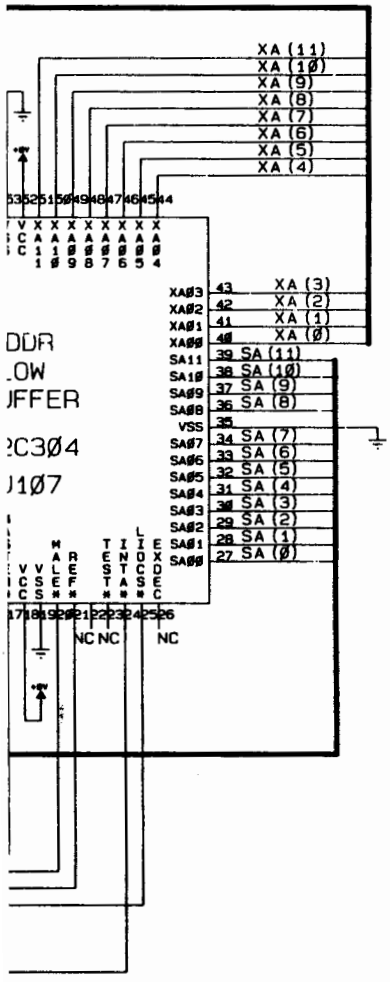

A20GATE /A20GATE 386 SOCKET TOPL
80386
XU63
U58
16L8A
U53
F257
OSC4
XXXXX
OSC
14.3818
MHZ OSC
MCS32*
IOCS32*
REF*
IOCHRDY
IOCHCK*
IO2XCS*
AF32*
MASTER*
MEMCS16*
IOCS16*
ØWS*
LAOMCS*
SDIR
287CS*
HLDA1
ATEN*
AEN8*
XBHE*
MEMCS16*
XIOR*
DIR245
SBUSEN*
ENHLB
A(16)
OPT ROM
SSALE
SALE
REF*
PFAIL*
BE*(Ø)
BE*(1)
BE*(2)
BE*(3)
AF32*
NA*
3Ø2CLK2
ADS*
ERROR*
PEREQ
BUSY*
BE*(Ø:3)
M/IO*
W/R*
A(Ø:31)
RESET3
D(Ø:31)
READY*
EMCCLK2
A20GATE
386CLK2
D/C*
M/IO*
CPUA2Ø
A(2Ø)
HLDA
HOLDOUT
HPNMI
NMI
HOLDIN
INTR
LMEGCS*
PCHK*
CAS*
3Ø2SCLK
FBE*
PEN*
RESET3
HLDA
BE*(3)
BE*(2)
BE*(1)
BE*(Ø)
ERROR*
BUSY*
PEREQ
BE*(Ø:3)
M/IO*



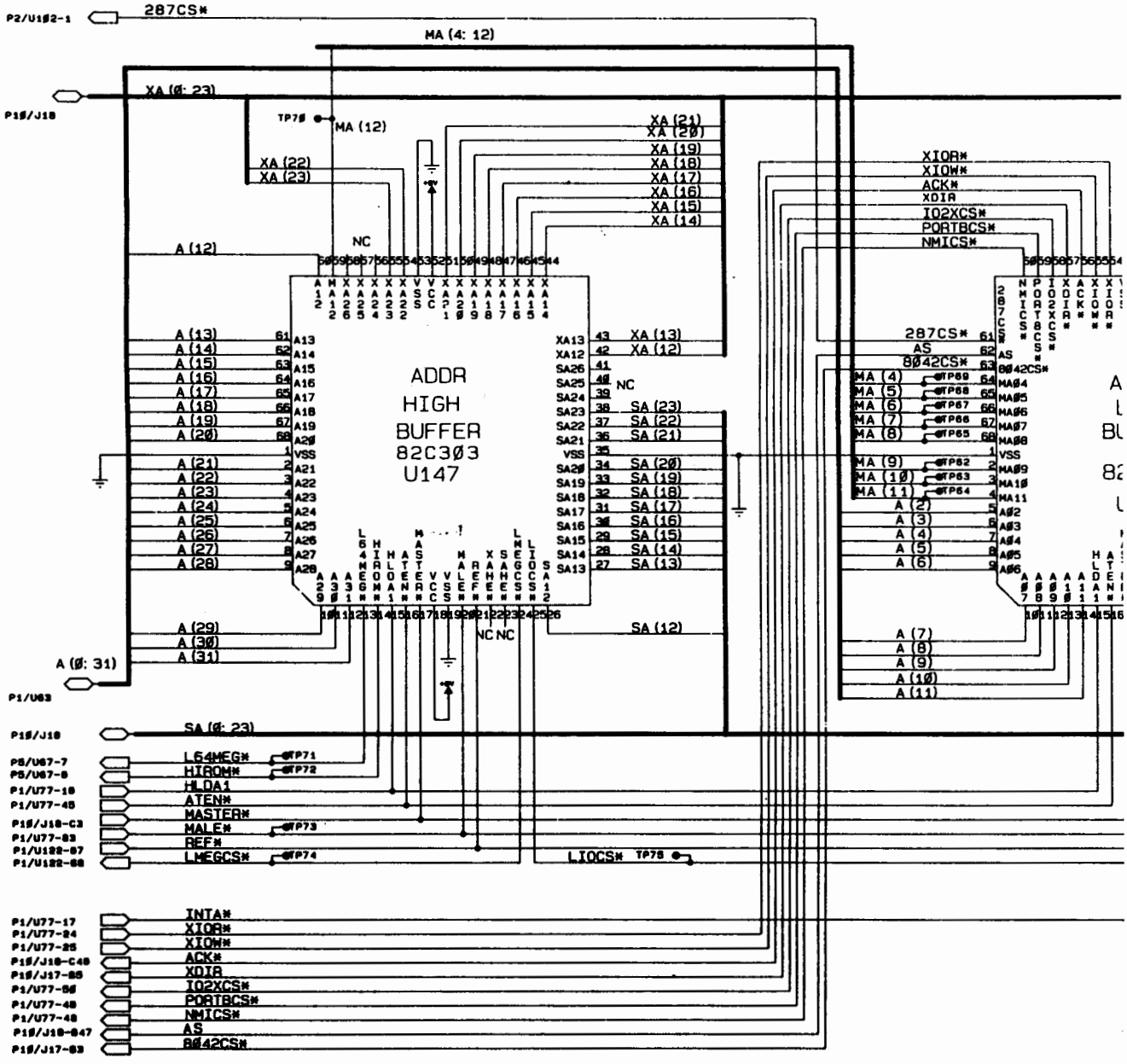
Processor/Memory PCA Schematic

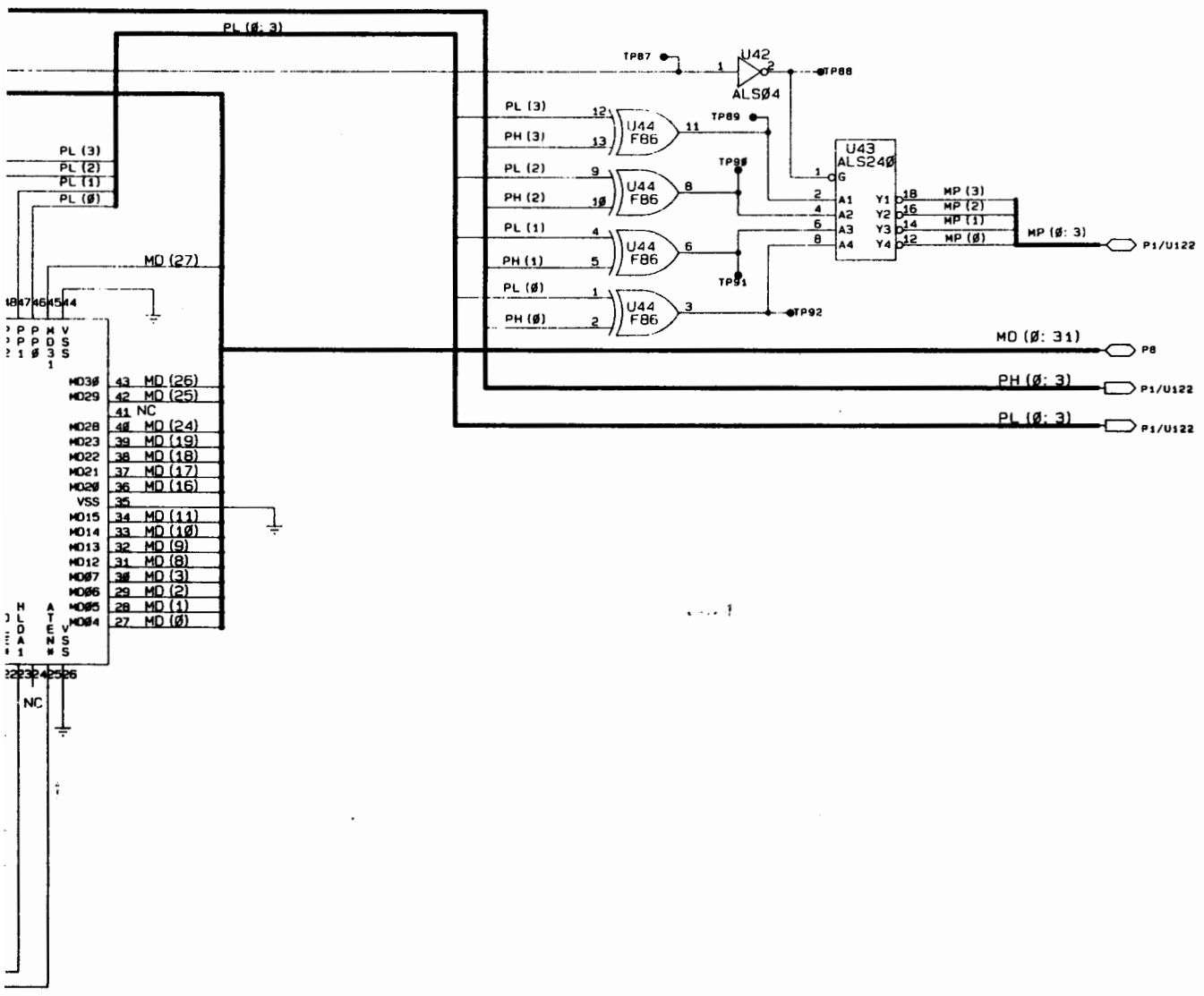
2-37/2-38


RESET3
P1/U63-37
U115
F04
387 RESET
PAL
U102
16L8A
287CS*
XIOW*
SA (4)
SA (3)
SA (2)
SA (1)
SA (0)
SA (0: 23)
M/IO*
MALE*
P1/U77-63
SCLK
P1/U77-66
80387PRES
P5/SW1
INTA*
P1/U77-17
READY*
R904
R=5.1K
R823
R=1K
387SEL*
U95
F74
READYIN
U121
F04
U131
F08
U75
F125
READY*
R901
R=5.
80387PRES
387 BUS
PAL
U103
16L8A
R903
R=5.1K
FB13
387IRQ13
PEREQ
ERROR*
BUSY*
BUSYFF*
ERRFF*
U105
F74
387PEREQ
387BUSY*
R822
R=1K
387ERROR*
R808
R=5.1K
R806
R=5.1K
PIN1
EXTENDED
MATH COPROCESSOR
SOCKET
XU82
#1-13
#14-26
#27-39
#40-46
#47-52
#53-58
#59-64
#65-70
#71-76
#77-82
#83-95
#96-108
#109-121
NC
AF32*
TCB*
R805
R=1K
R807
R=1K
D (11)
D (10)
D (12)
D (14)
D (13)
D (15)
D (16)
A (13)
A (12)
A (11)
A (10)
A (9)
A (8)
A (31)
A (15)
A (14)
D (9)
D (8)
D (7)
D (6)
D (5)
D (4)
A (24)
A (25)
A (26)
D (3)
D (2)
A (27)
D (1)
D (0)
A (28)
A (29)
A (30)
A (31)
A (2)
W/R*
P1/U63-24
M/IO*
P1/U63-12
ADS*
P1/U63-54
D (0: 31)
P1/U63
A (0: 31)
P1/U63
BE* (0: 3)
P1/U63
EMCCLK2
P1/U77-2
RESET2*
P18/J18-B39
HOLDIN
P1/U77-76



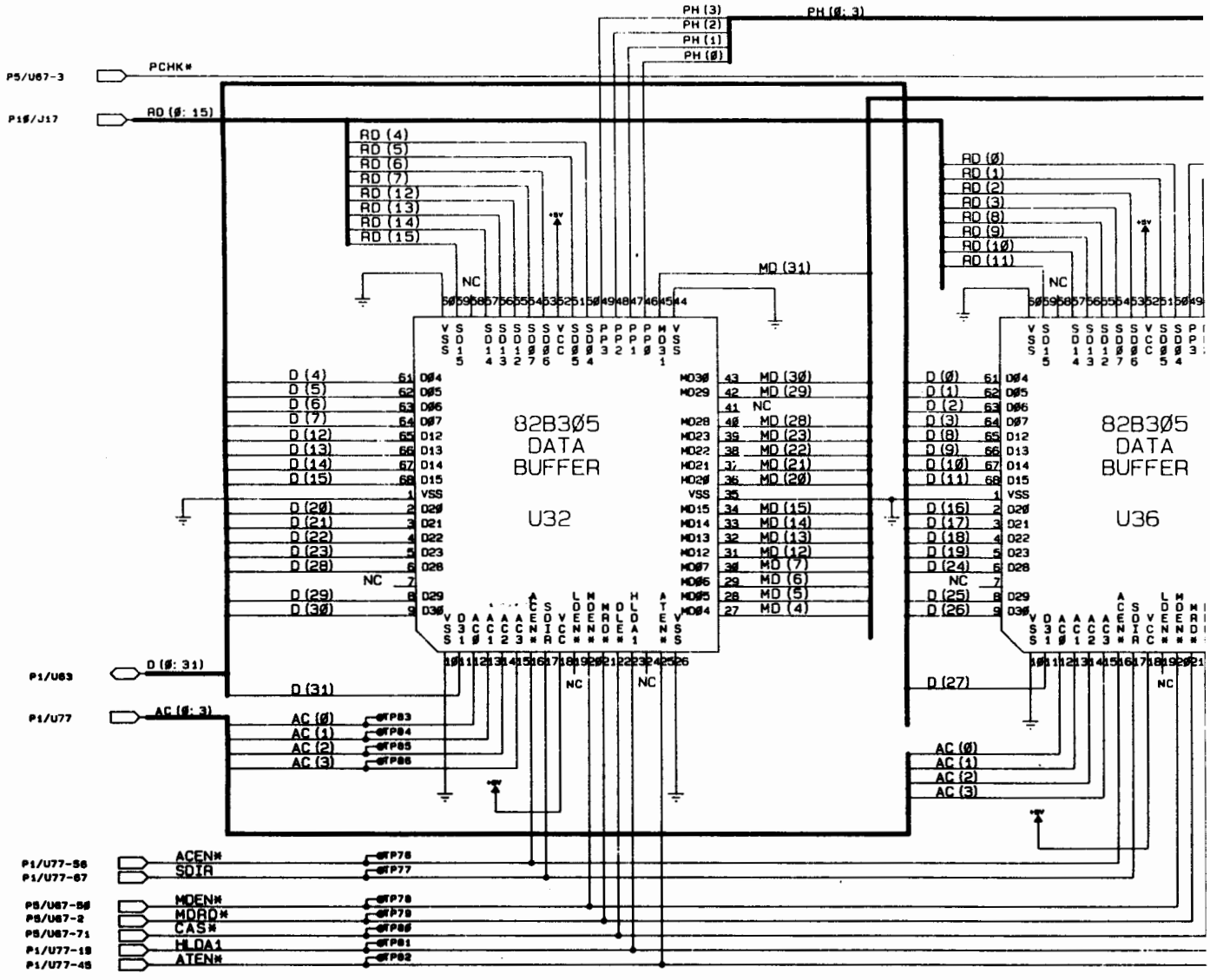
Processor/Memory PCA Schematic

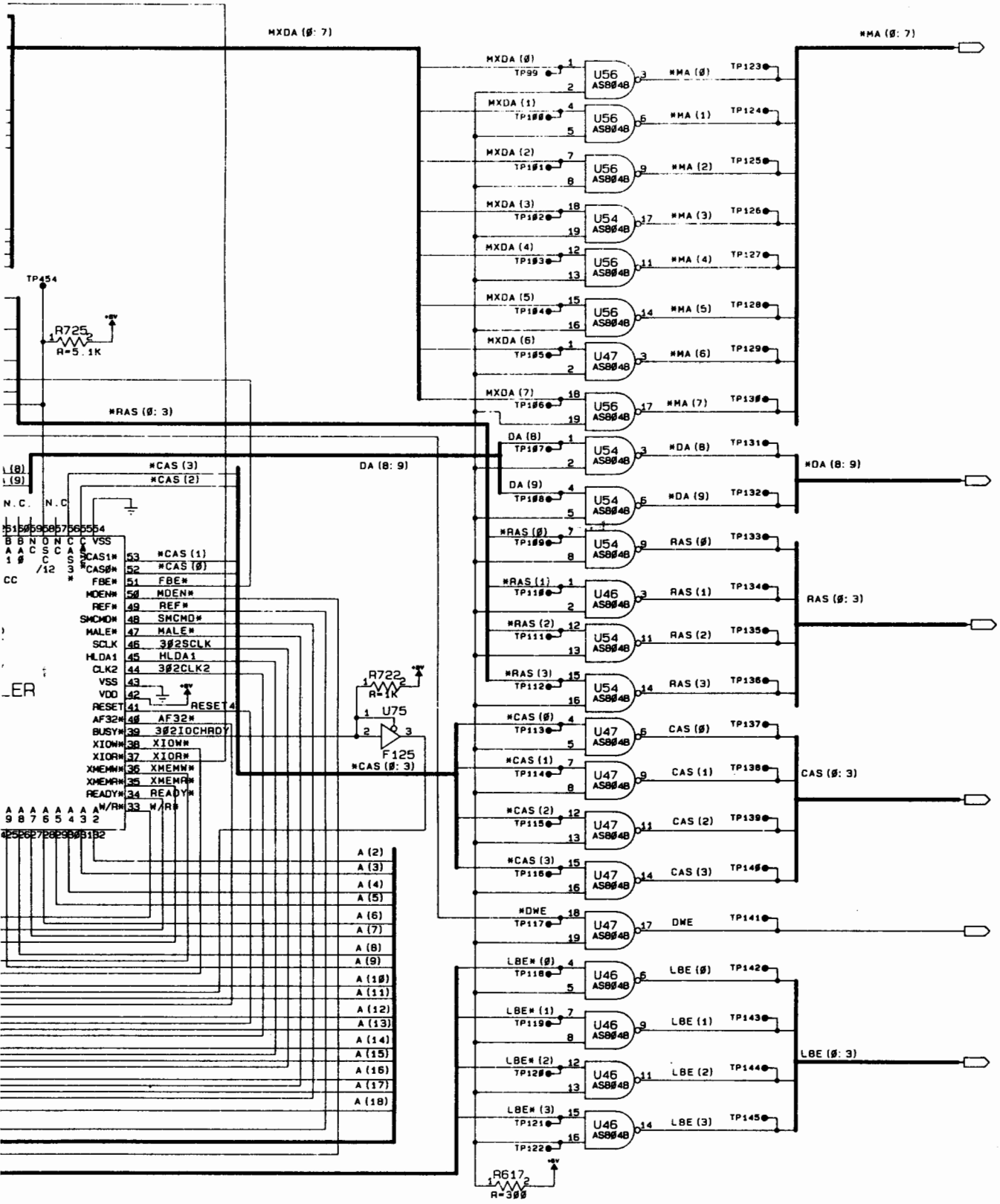

ADDR
HIGH
BUFFER
82C3Ø3
U147
287CS*
MA (4: 12)
XA (Ø: 23)
MA (12)
XA (21)
XA (2Ø)
XA (19)
XA (18)
XA (17)
XA (16)
XA (15)
XA (14)
XA (22)
XA (23)
A (12)
NC
A (13)
A (14)
A (15)
A (16)
A (17)
A (18)
A (19)
A (2Ø)
A (21)
A (22)
A (23)
A (24)
A (25)
A (26)
A (27)
A (28)
A (29)
A (3Ø)
A (31)
A (Ø: 31)
XA (13)
XA (12)
SA (23)
SA (22)
SA (21)
SA (2Ø)
SA (19)
SA (18)
SA (17)
SA (16)
SA (15)
SA (14)
SA (13)
SA (12)
NC NC
XIOR*
XIOW*
ACK*
XDIR
IO2XCS*
PORTBCS*
NMICS*
287CS*
AS
8Ø42CS*
MA (4)
MA (5)
MA (6)
MA (7)
MA (8)
MA (9)
MA (1Ø)
MA (11)
A (2)
A (3)
A (4)
A (5)
A (6)
A (7)
A (8)
A (9)
A (1Ø)
A (11)
SA (Ø: 23)
L64MEG*
HIROM*
HLDA1
ATEN*
MASTER*
MALE*
REF*
LMEGCS*
LIOCS*
INTA*
XIOR*
XIOW*
ACK*
XDIR
IO2XCS*
PORTBCS*
NMICS*
AS
8Ø42CS*



NOTE : MINIMISE THE LENGTH OF THE MP BUS

Processor/Memory PCA Schematic


PH (3)
PH (2)
PH (1)
PH (Ø)
PH (Ø: 3)
P5/U67-3
PCHK*
P1Ø/J17
AD (Ø: 15)
AD (4)
AD (5)
AD (6)
AD (7)
AD (12)
AD (13)
AD (14)
AD (15)
AD (Ø)
AD (1)
AD (2)
AD (3)
AD (8)
AD (9)
AD (1Ø)
AD (11)
+5V
NC
MD (31)
82B3Ø5
DATA
BUFFER
U32
U36
D (4)
D (5)
D (6)
D (7)
D (12)
D (13)
D (14)
D (15)
D (2Ø)
D (21)
D (22)
D (23)
D (28)
D (29)
D (3Ø)
MD (3Ø)
MD (29)
MD (28)
MD (23)
MD (22)
MD (21)
MD (2Ø)
MD (15)
MD (14)
MD (13)
MD (12)
MD (7)
MD (6)
MD (5)
MD (4)
D (Ø)
D (1)
D (2)
D (3)
D (8)
D (9)
D (1Ø)
D (11)
D (16)
D (17)
D (18)
D (19)
D (24)
D (25)
D (26)
D (27)
P1/U83
D (Ø: 31)
D (31)
P1/U77
AC (Ø: 3)
AC (Ø)
AC (1)
AC (2)
AC (3)
P1/U77-56
ACEN*
P1/U77-67
SDIR
P8/U67-56
MDEN*
P8/U67-2
MDRD*
P8/U67-71
CAS*
P1/U77-18
HLDA1
P1/U77-45
ATEN*



Processor/Memory PCA Schematic

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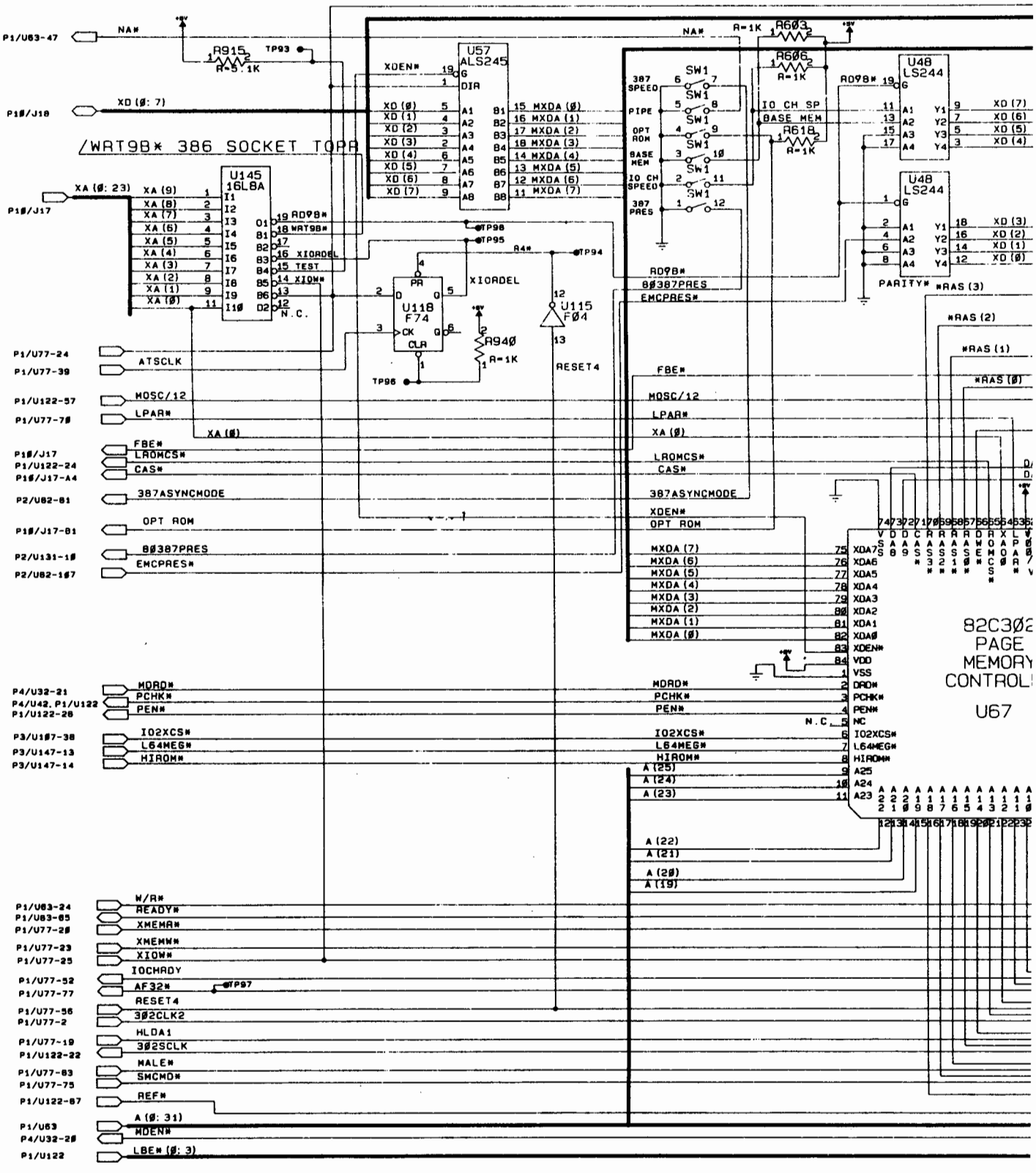
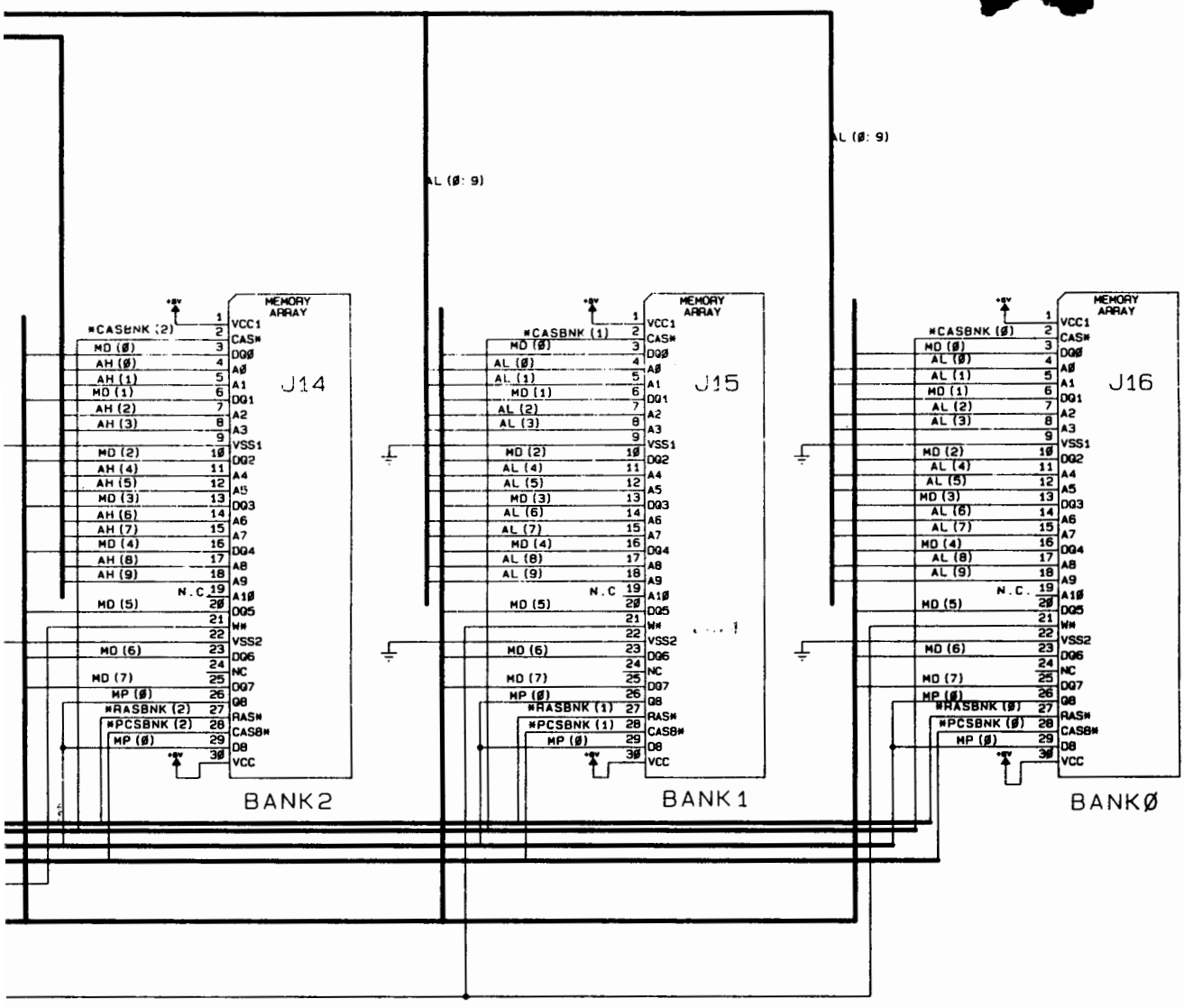
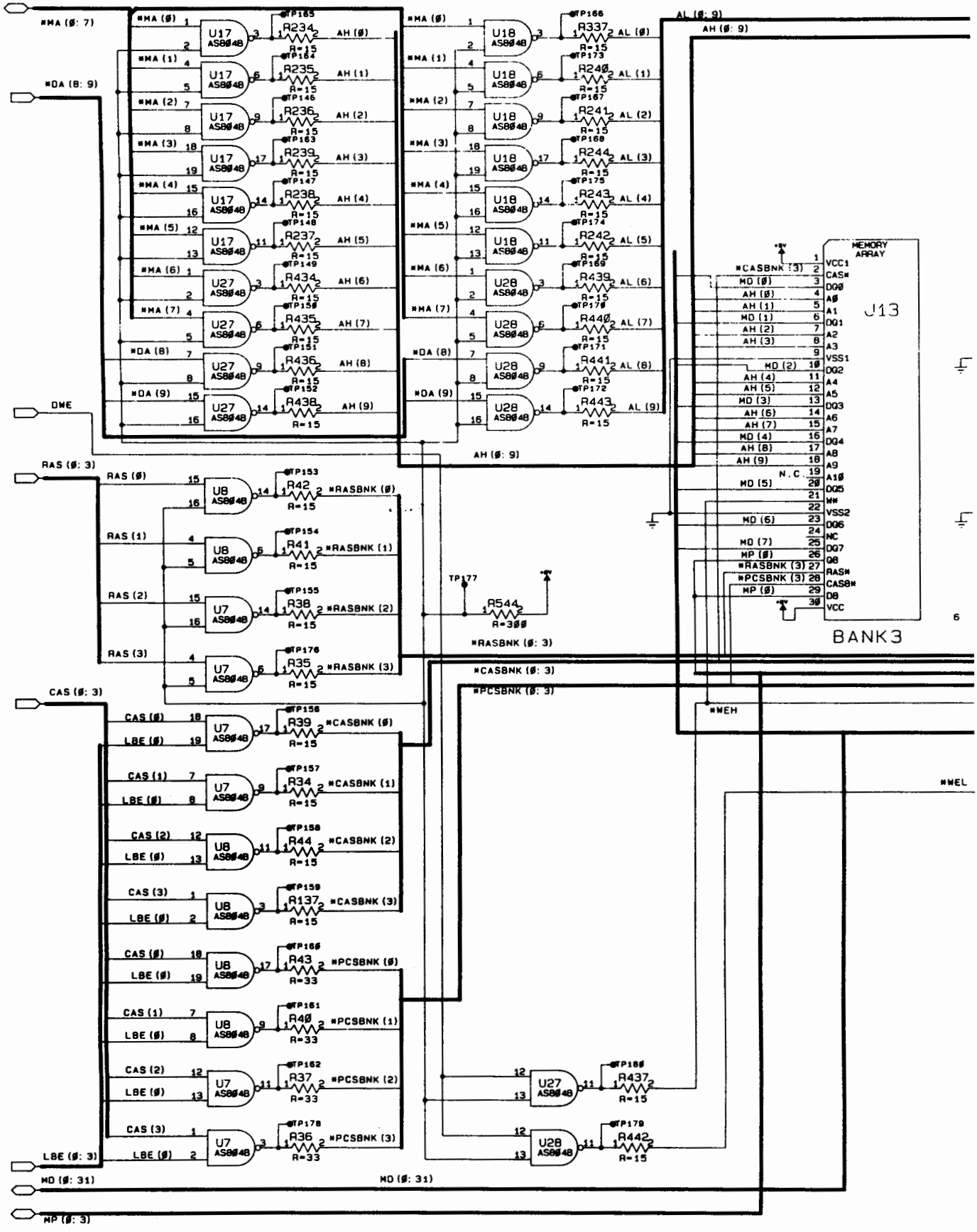
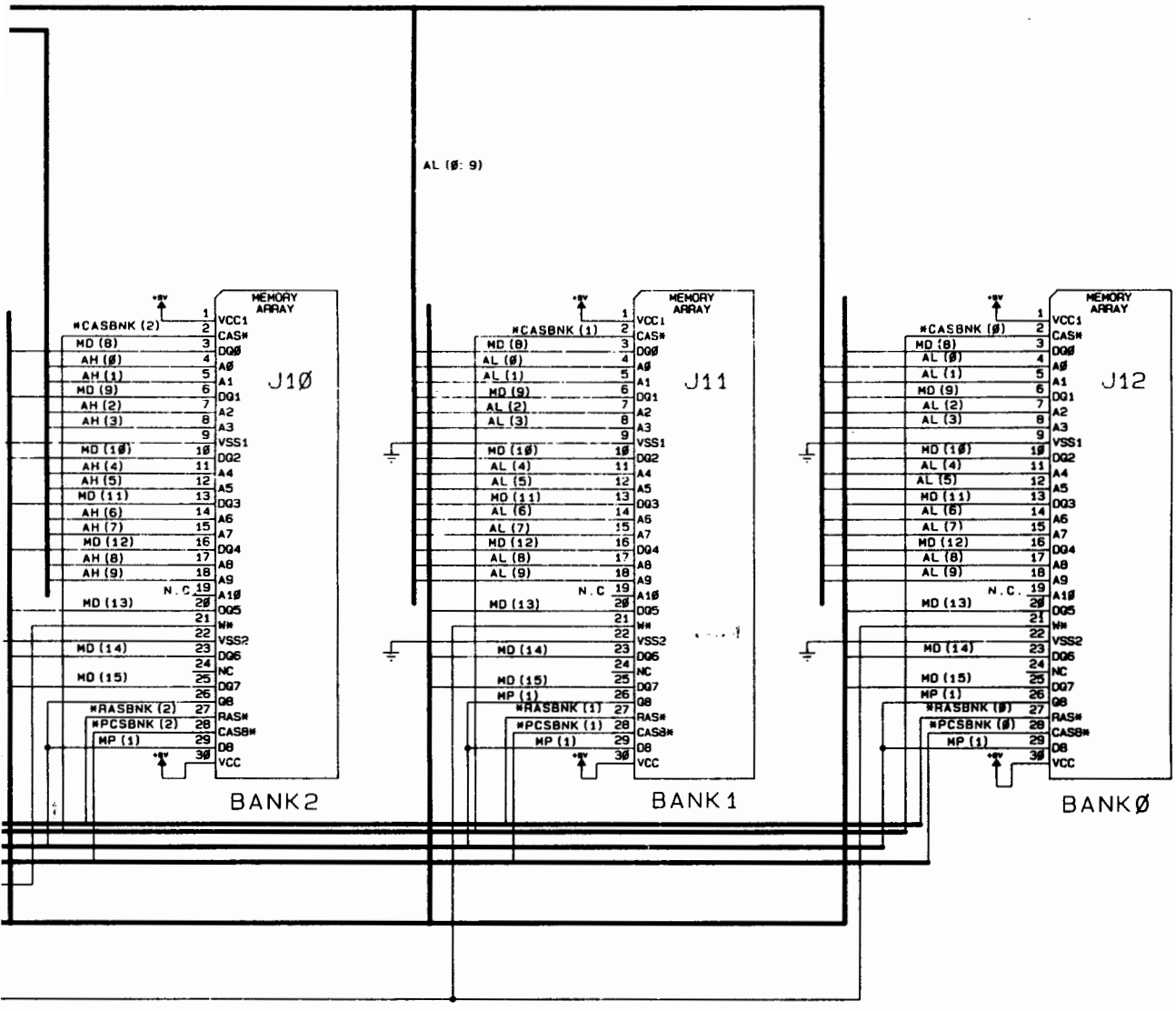

/WRT98* 386 SOCKET TOPA
U145 16L8A
U57 ALS245
U48 LS244
U48 LS244
U118 F74
U115 FØ4
R915 R=5.1K
R603 R=1K
R606 R=1K
R618 R=1K
R94Ø R=1K
SW1
XDEN*
XD (Ø: 7)
XA (Ø: 23)
NA*
RD98*
WRT98*
XIORDEL
XIOW*
TEST
N.C.
ATSCLK
MOSC/12
LPAR*
XA (Ø)
FBE*
LROMCS*
CAS*
387ASYNCMODE
OPT ROM
Ø387PRES
EMCPRES*
MXDA (7)
MXDA (6)
MXDA (5)
MXDA (4)
MXDA (3)
MXDA (2)
MXDA (1)
MXDA (Ø)
MDRD*
PCHK*
PEN*
IO2XCS*
L64MEG*
HIROM*
A (25)
A (24)
A (23)
A (22)
A (21)
A (2Ø)
A (19)
W/R*
READY*
XMEMR*
XMEMW*
XIOW*
IOCHRDY
AF32*
RESET4
3Ø2CLK2
HLDA1
3Ø2SCLK
MALE*
SMCMD*
REF*
A (Ø: 31)
MDEN*
LBE* (Ø: 3)
PARITY*
*RAS (3)
*RAS (2)
*RAS (1)
*RAS (Ø)
82C3Ø2
PAGE
MEMORY
CONTROL
U67



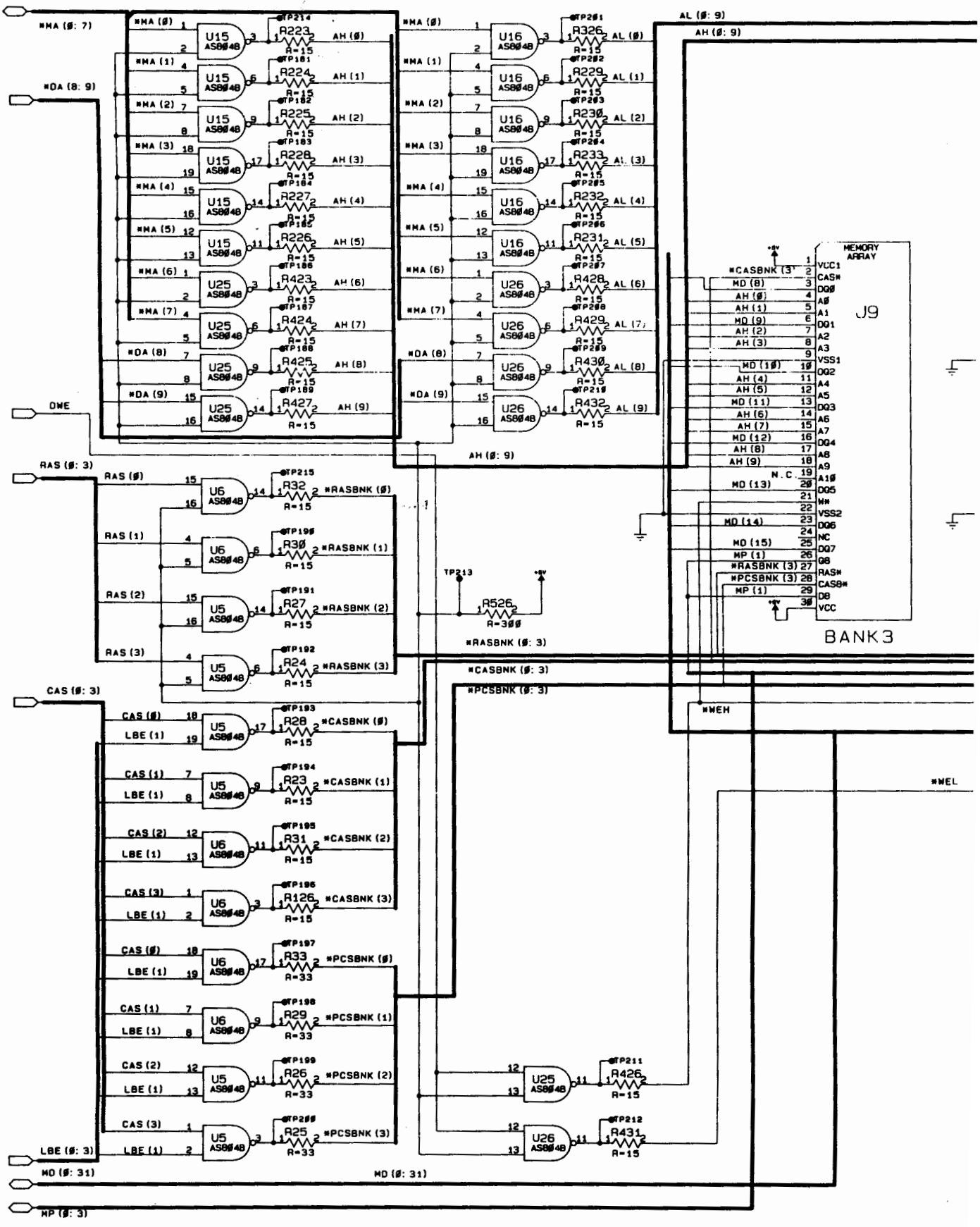
Processor/Memory PCA Schematic

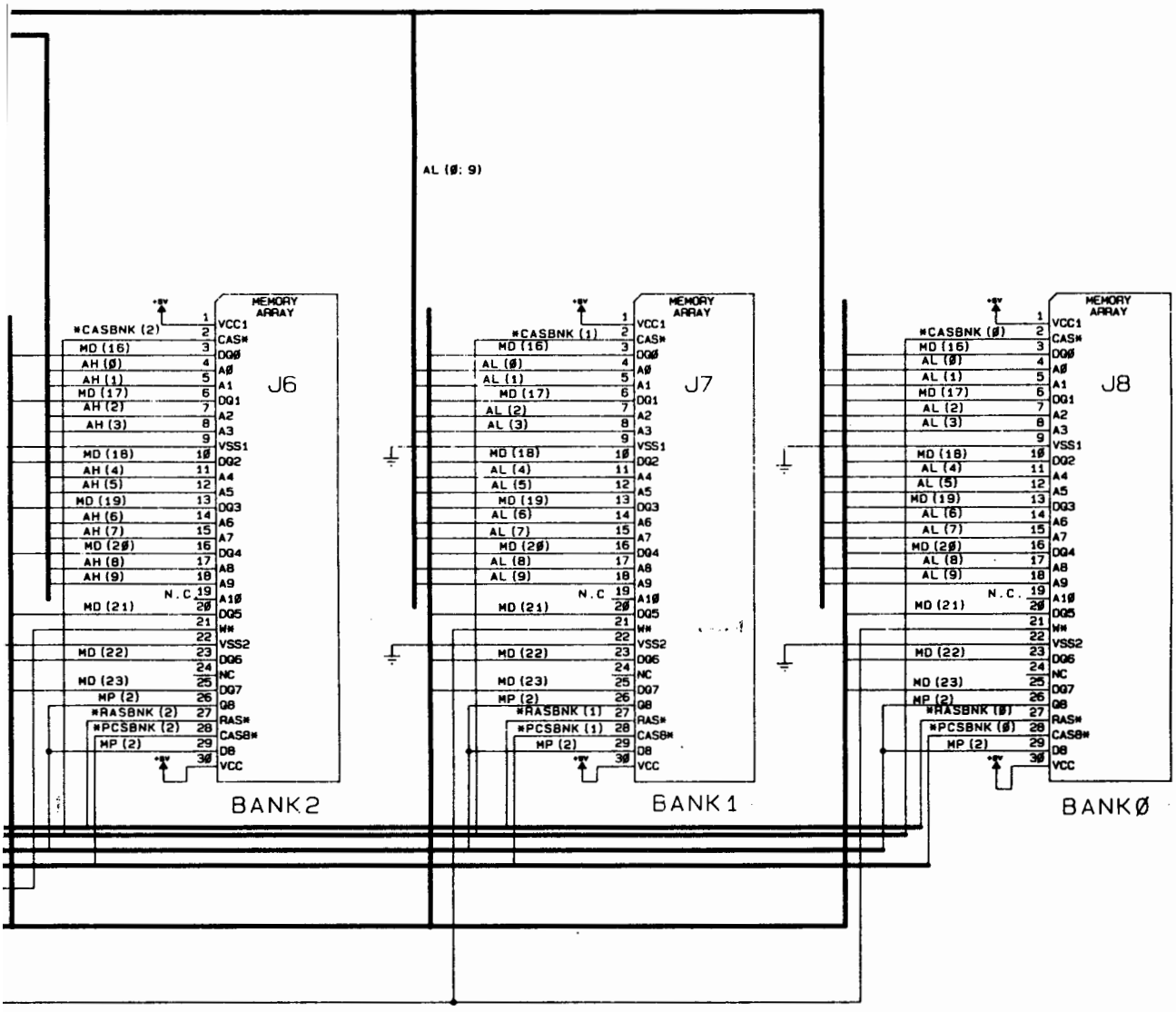
2-45/2-46


*MA (Ø: 7)
*DA (8: 9)
DWE
RAS (Ø: 3)
CAS (Ø: 3)
LBE (Ø: 3)
MD (Ø: 31)
MP (Ø: 3)
AH (Ø: 9)
AL (Ø: 9)
*RASBNK (Ø: 3)
*CASBNK (Ø: 3)
*PCSBNK (Ø: 3)
*WEH
*WEL
MD (Ø: 31)
BANK3
J13
MEMORY ARRAY



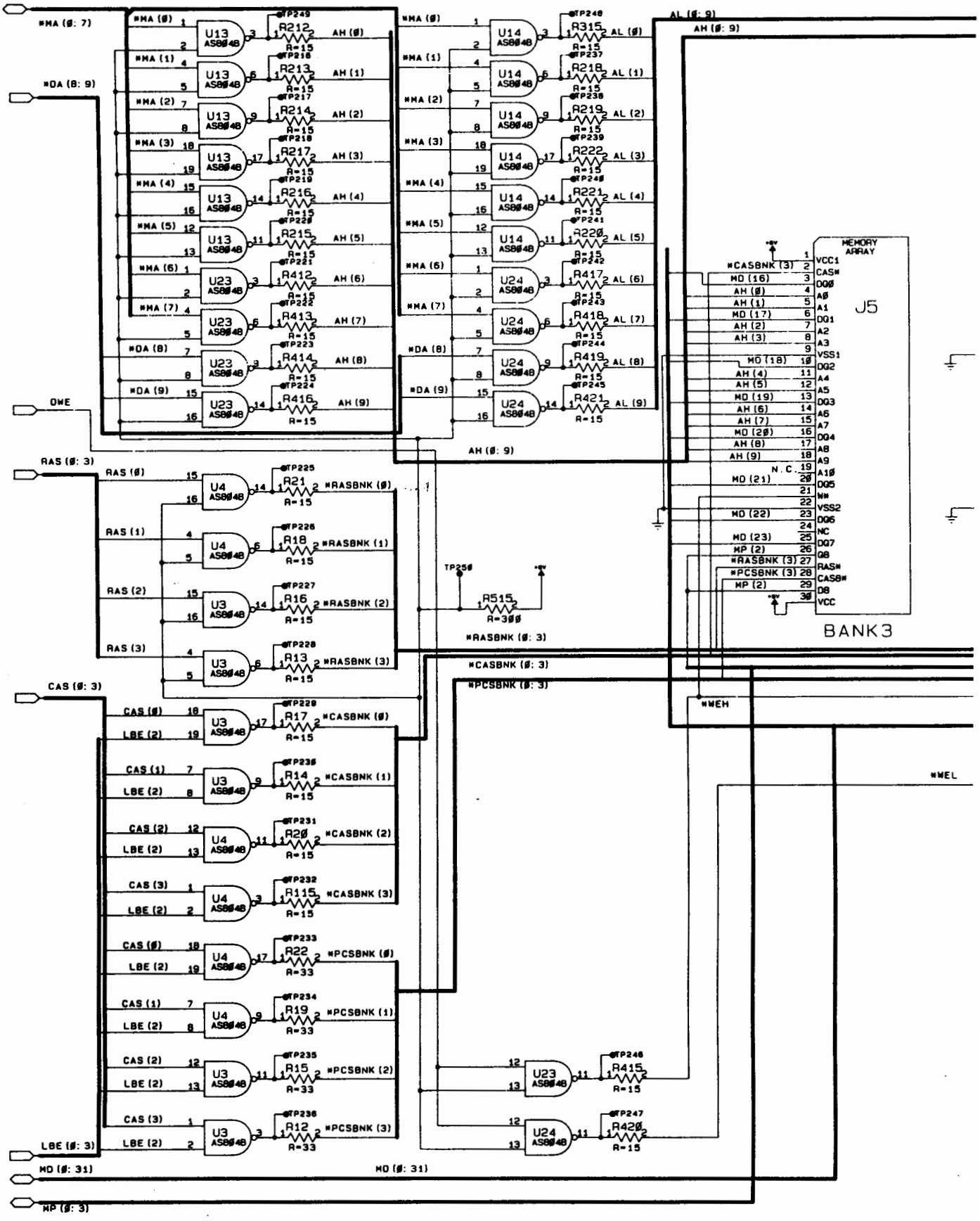
Processor/Memory PCA Schematic

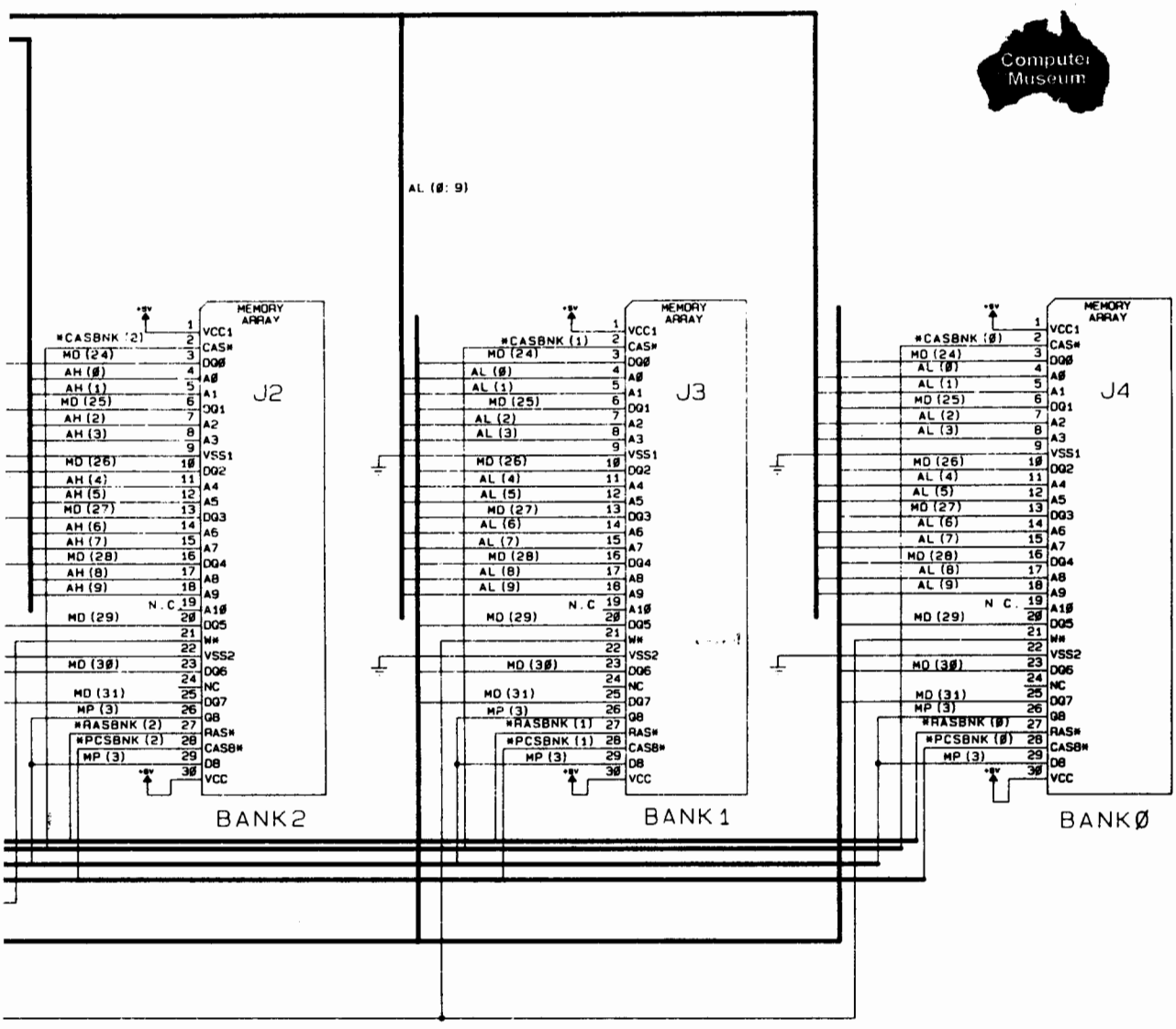

*MA (Ø: 7)
*DA (8: 9)
DWE
RAS (Ø: 3)
CAS (Ø: 3)
LBE (Ø: 3)
MD (Ø: 31)
MP (Ø: 3)
AL (Ø: 9)
AH (Ø: 9)
*CASBNK (3)
MEMORY ARRAY
J9
BANK3
*RASBNK (Ø: 3)
*CASBNK (Ø: 3)
*PCSBNK (Ø: 3)
*WEH
*WEL



Processor/Memory PCA Schematic

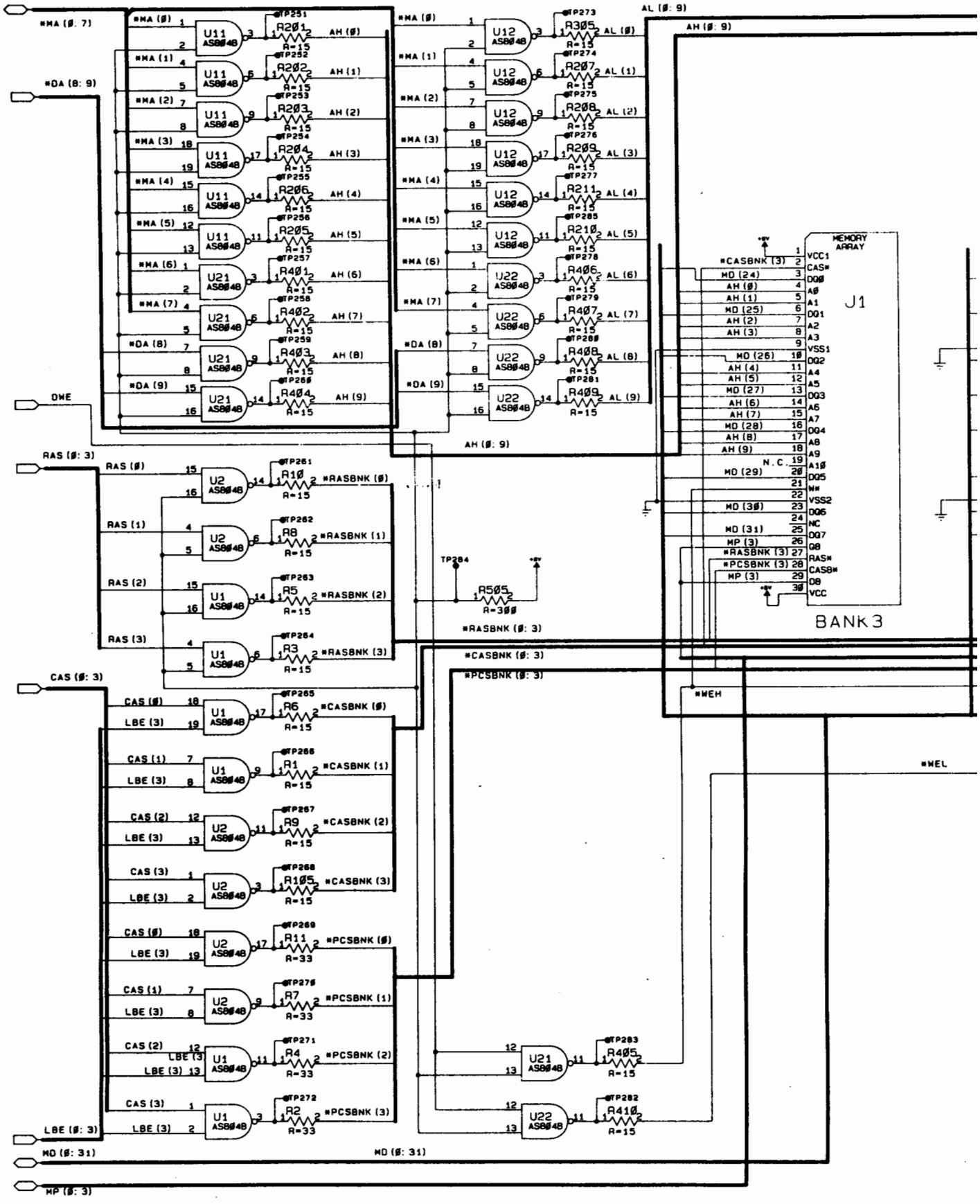
2-49/2-50


*MA (Ø: 7)
*DA (8: 9)
OWE
RAS (Ø: 3)
CAS (Ø: 3)
LBE (Ø: 3)
MD (Ø: 31)
MP (Ø: 3)
AH (Ø: 9)
AL (Ø: 9)
*RASBNK (Ø: 3)
*CASBNK (Ø: 3)
*PCSBNK (Ø: 3)
*WEH
*WEL
MD (Ø: 31)
MEMORY ARRAY
J5
BANK3
N.C.

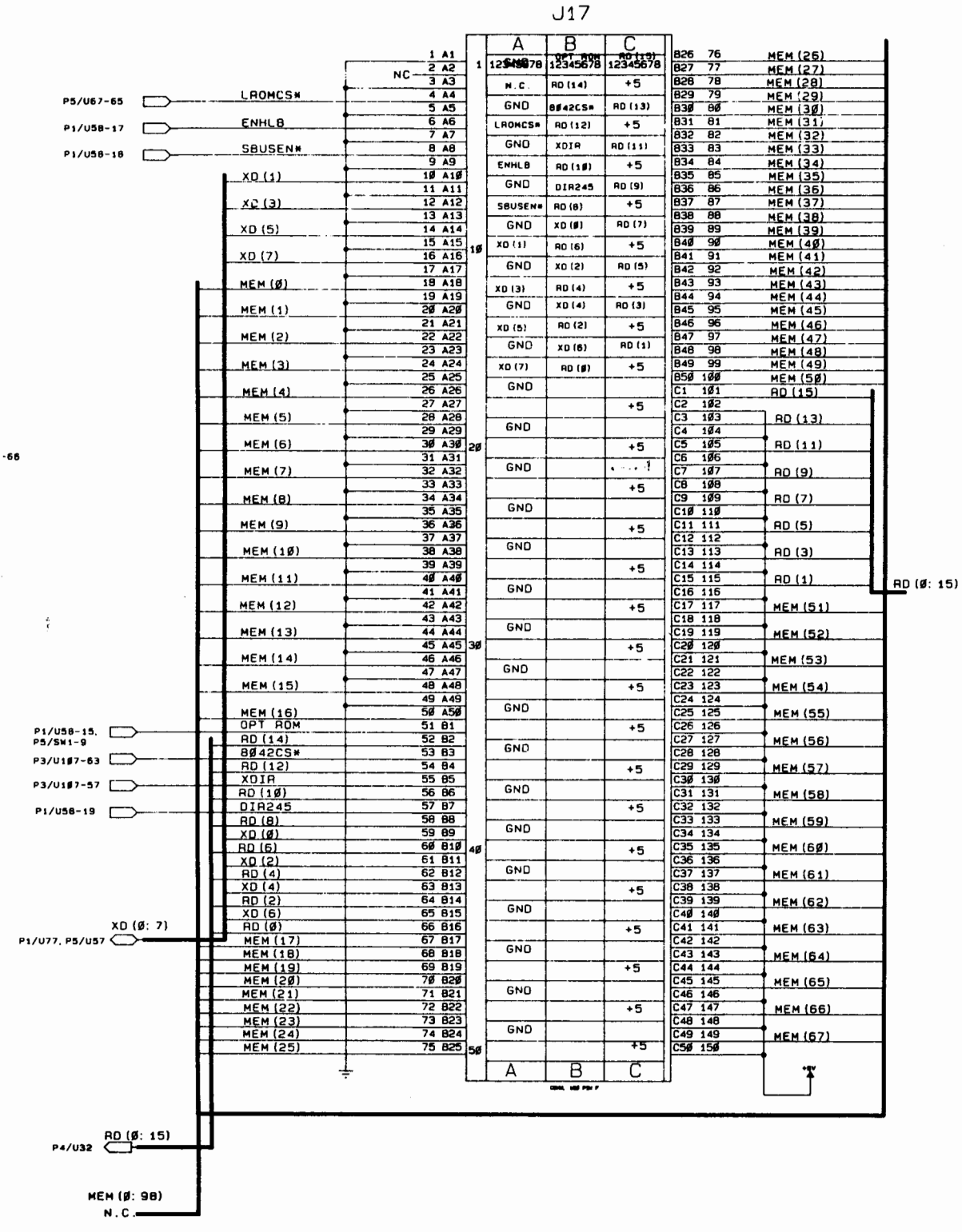


Processor/Memory PCA Schematic

2-51/2-52


*MA (Ø: 7)
*DA (8: 9)
DWE
RAS (Ø: 3)
CAS (Ø: 3)
LBE (Ø: 3)
MD (Ø: 31)
MP (Ø: 3)
AL (Ø: 9)
AH (Ø: 9)
*RASBNK (Ø: 3)
*CASBNK (Ø: 3)
*PCSBNK (Ø: 3)
*WEH
*WEL
MEMORY ARRAY
J1
BANK3
*RASBNK (3)
*PCSBNK (3)
MP (3)
N.C.

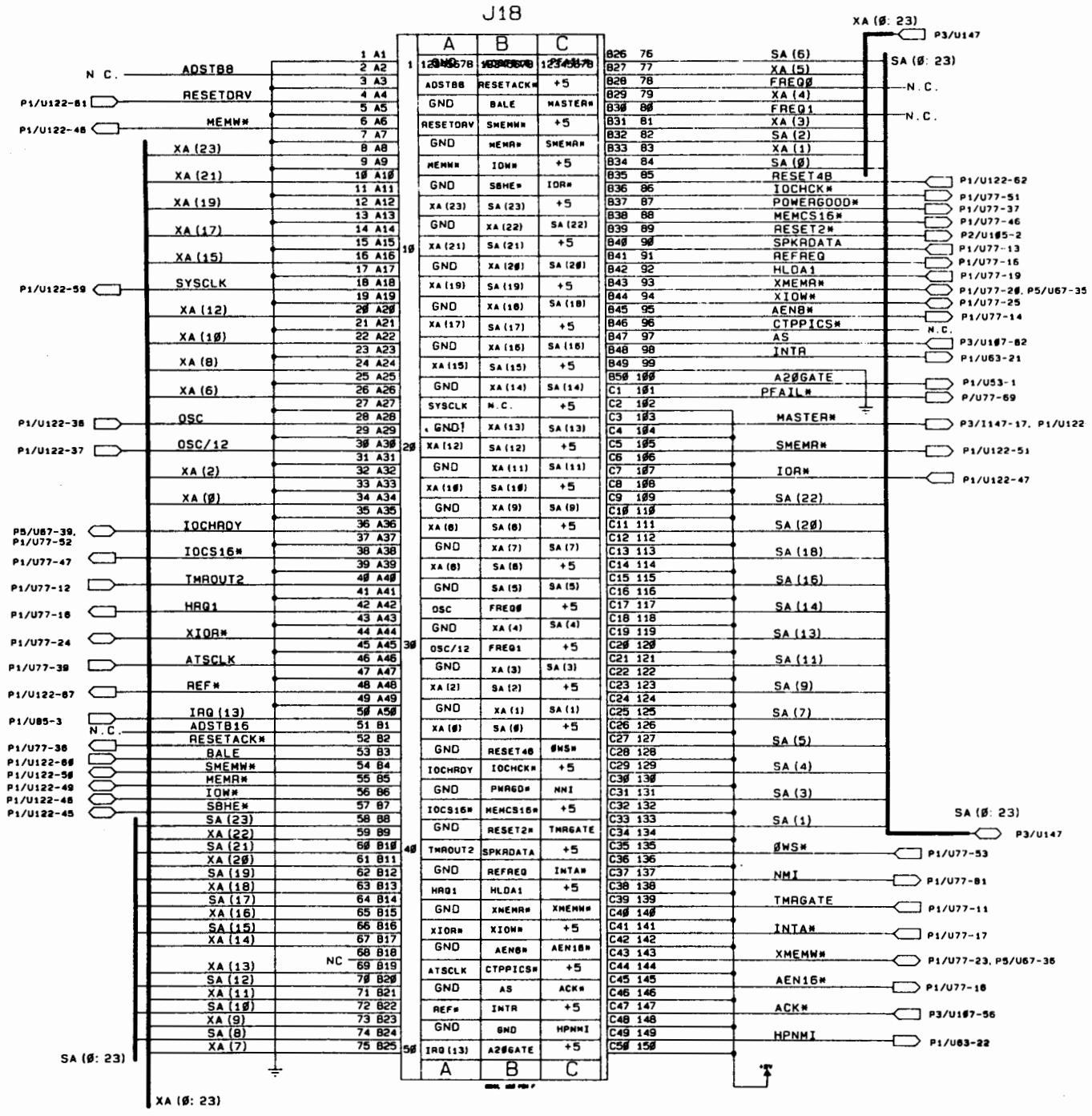
MEMORY/DATABUS CONNECTOR



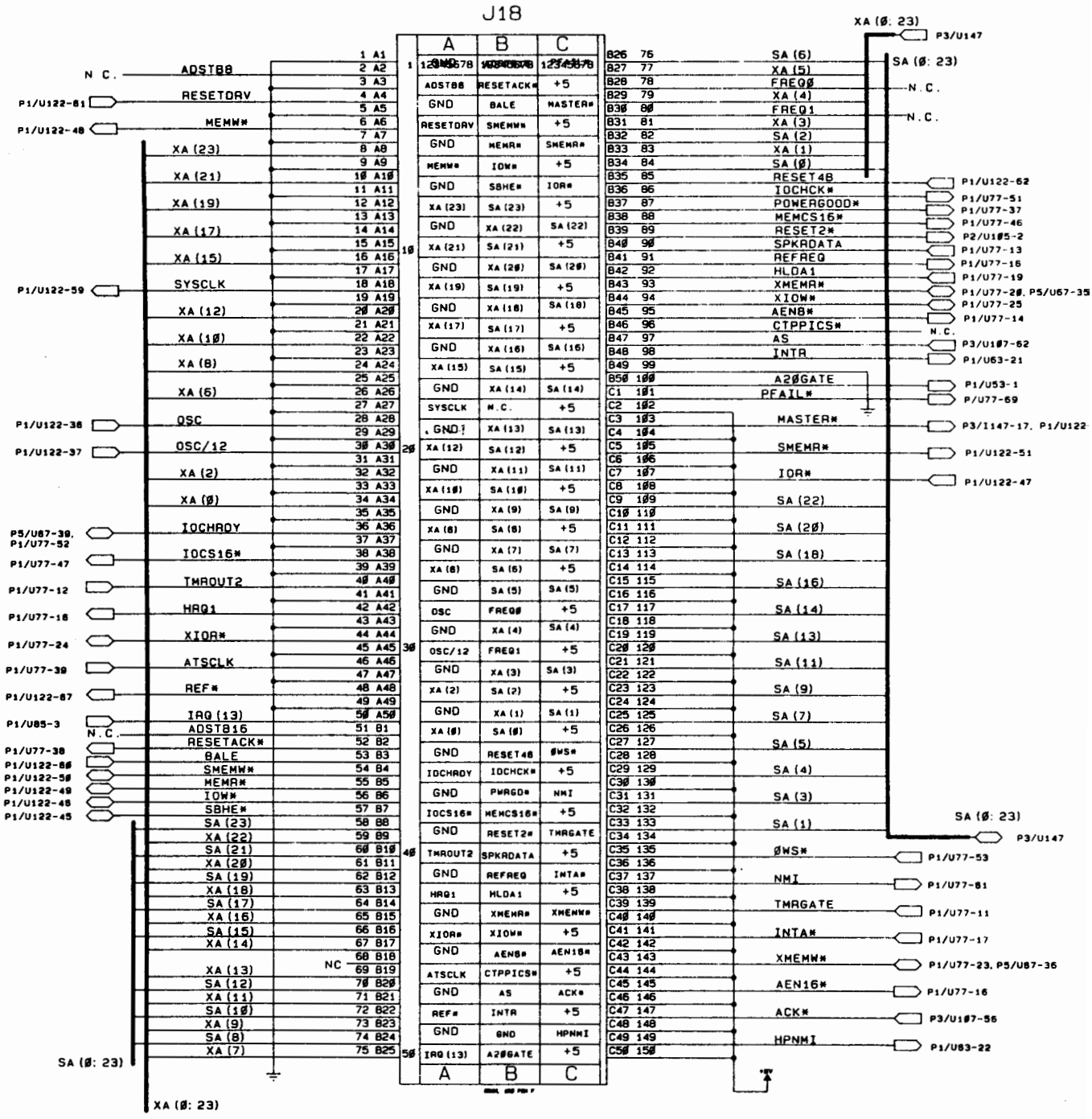
Processor/Memory PCA Schematic

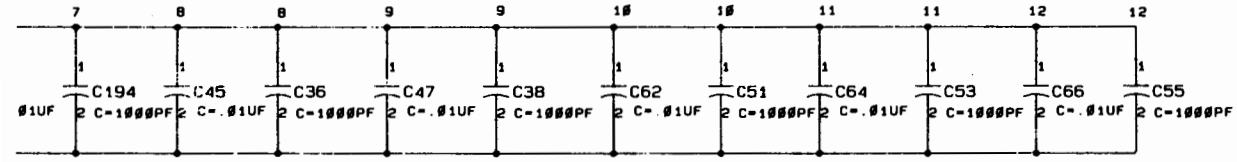
2-53/2-54

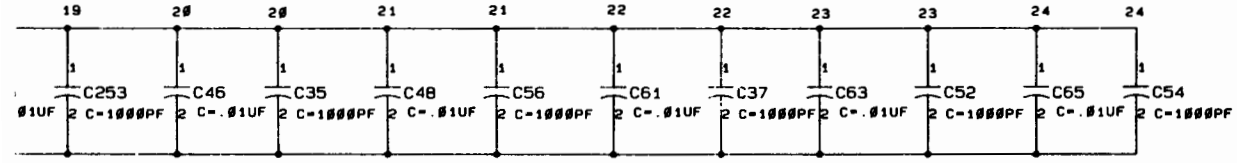
PROCESSOR CONNECTOR



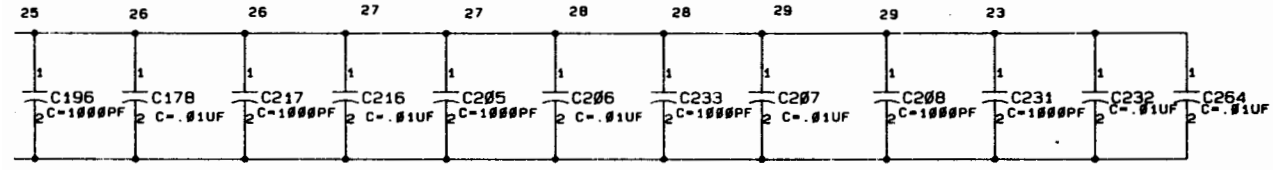
PROCESSOR CONNECTOR





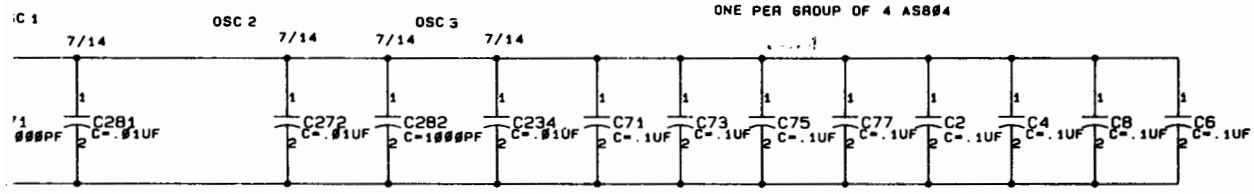


CAPACITOR PAIR TO BE LOCATED WITHIN THE DEVICE OUTLINE---------->



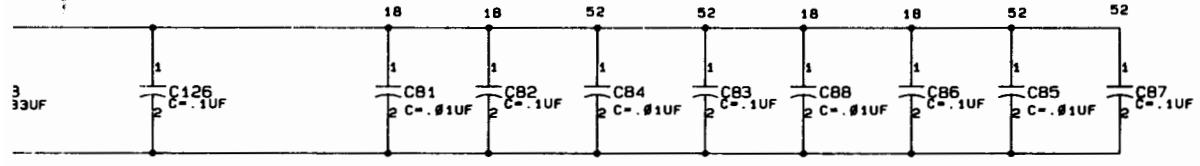
ONE PER GROUP OF 4 AS804

OSC 2 OSC 3

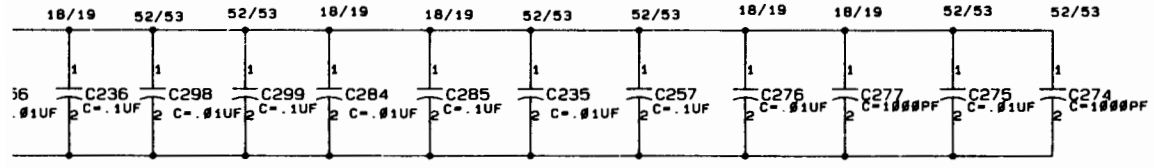


<82B305 PINS>

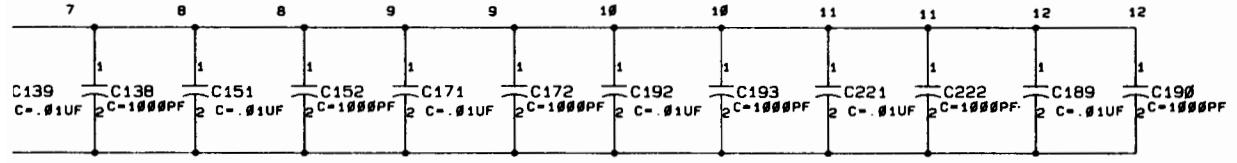
LOWER NIBBLE UPPER NIBBLE

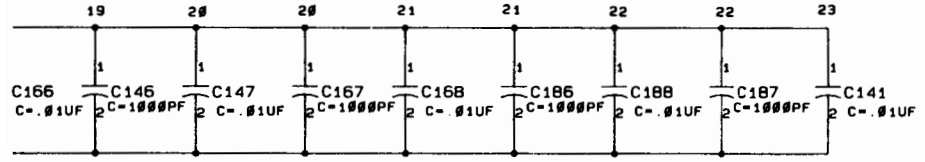


<82C303 PINS> <82C304 PINS> <82C306 PINS>



LOCATED INSIDE OF THE DEVICE OUTLINE---------->





Processor/Memory PCA Schematic

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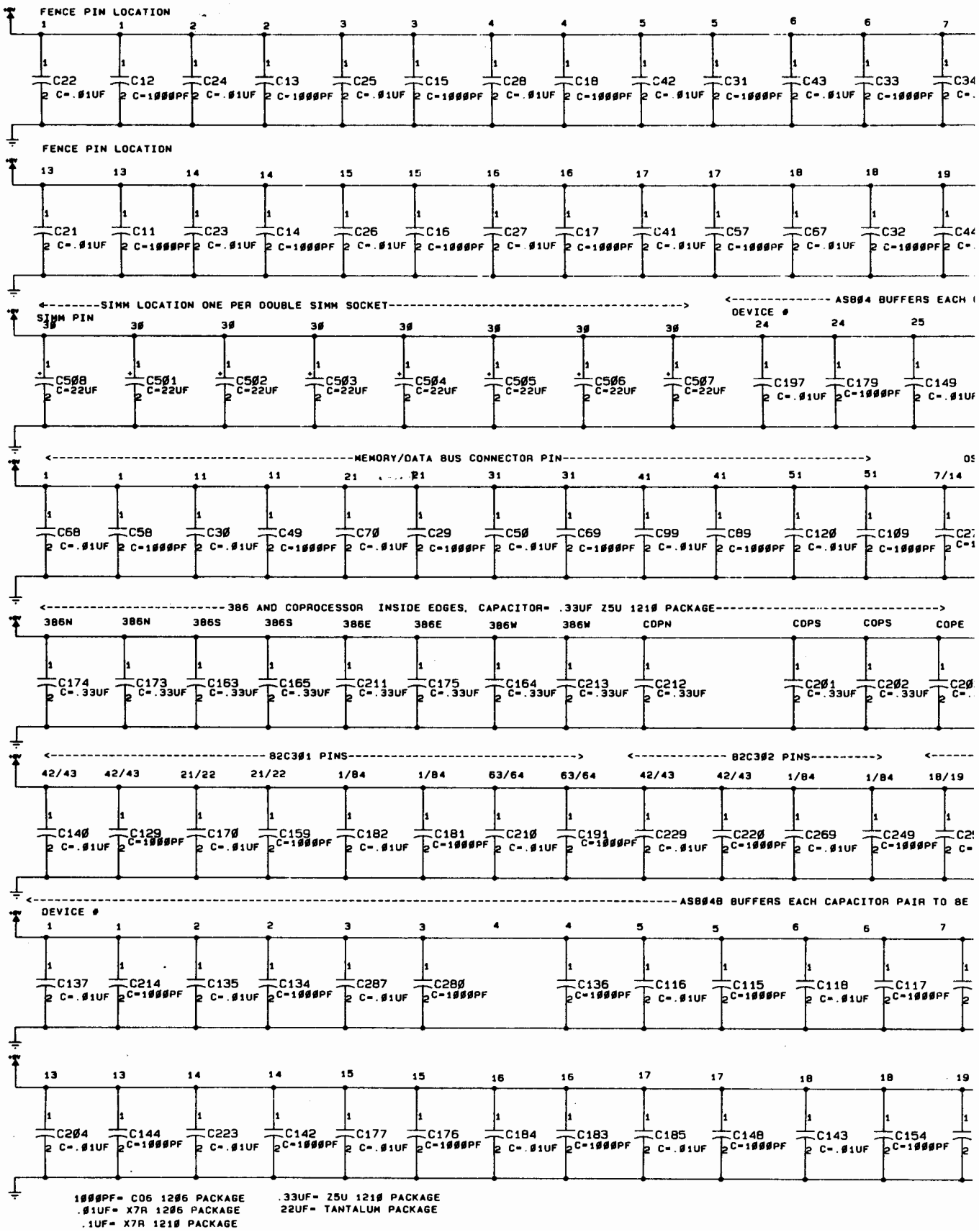
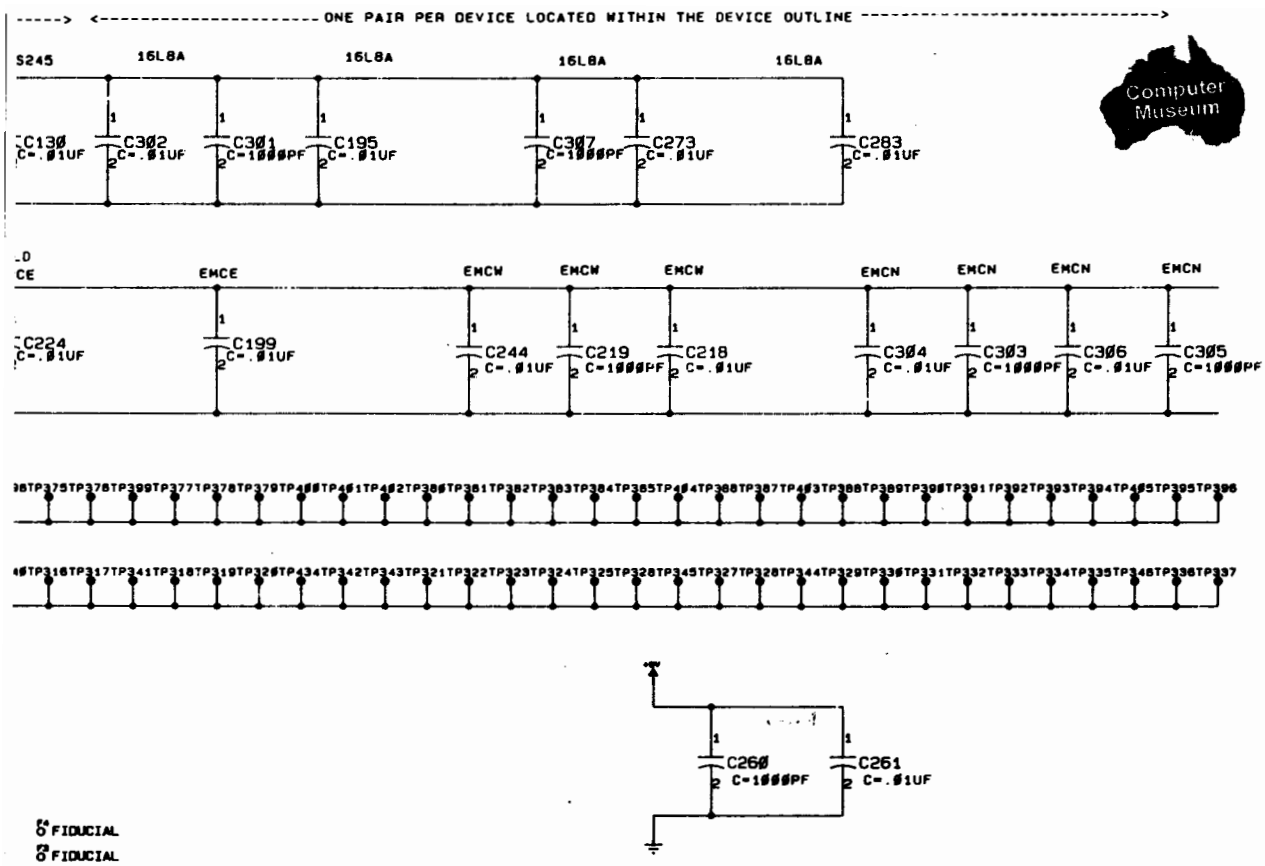

FENCE PIN LOCATION
C22 C=.01UF
C12 C=1000PF
C24 C=.01UF
C13 C=1000PF
C25 C=.01UF
C15 C=1000PF
C28 C=.01UF
C18 C=1000PF
C42 C=.01UF
C31 C=1000PF
C43 C=.01UF
C33 C=1000PF
FENCE PIN LOCATION
C21 C=.01UF
C11 C=1000PF
C23 C=.01UF
C14 C=1000PF
C26 C=.01UF
C16 C=1000PF
C27 C=.01UF
C17 C=1000PF
C41 C=.01UF
C57 C=1000PF
C67 C=.01UF
C32 C=1000PF
SIMM LOCATION ONE PER DOUBLE SIMM SOCKET
AS804 BUFFERS EACH
SIMM PIN
DEVICE #
C508 C=22UF
C501 C=22UF
C502 C=22UF
C503 C=22UF
C504 C=22UF
C505 C=22UF
C506 C=22UF
C507 C=22UF
C197 C=.01UF
C179 C=1000PF
C149 C=.01UF
MEMORY/DATA BUS CONNECTOR PIN
C68 C=.01UF
C58 C=1000PF
C30 C=.01UF
C49 C=1000PF
C70 C=.01UF
C29 C=1000PF
C50 C=.01UF
C69 C=1000PF
C99 C=.01UF
C89 C=1000PF
C120 C=.01UF
C109 C=1000PF
386 AND COPROCESSOR INSIDE EDGES, CAPACITOR= .33UF Z5U 1210 PACKAGE
386N 386N 386S 386S 386E 386E 386W 386W COPN COPS COPS COPE
C174 C=.33UF
C173 C=.33UF
C163 C=.33UF
C165 C=.33UF
C211 C=.33UF
C175 C=.33UF
C164 C=.33UF
C213 C=.33UF
C212 C=.33UF
C201 C=.33UF
C202 C=.33UF
82C301 PINS
82C302 PINS
42/43 42/43 21/22 21/22 1/84 1/84 63/64 63/64 42/43 42/43 1/84 1/84 18/19
C140 C=.01UF
C129 C=1000PF
C170 C=.01UF
C159 C=1000PF
C182 C=.01UF
C181 C=1000PF
C210 C=.01UF
C191 C=1000PF
C229 C=.01UF
C220 C=1000PF
C269 C=.01UF
C249 C=1000PF
AS804B BUFFERS EACH CAPACITOR PAIR TO BE
DEVICE #
C137 C=.01UF
C214 C=1000PF
C135 C=.01UF
C134 C=1000PF
C287 C=.01UF
C280 C=1000PF
C136 C=1000PF
C116 C=.01UF
C115 C=1000PF
C118 C=.01UF
C117 C=1000PF
C204 C=.01UF
C144 C=1000PF
C223 C=.01UF
C142 C=1000PF
C177 C=.01UF
C176 C=1000PF
C184 C=.01UF
C183 C=1000PF
C185 C=.01UF
C148 C=1000PF
C143 C=.01UF
C154 C=1000PF
1000PF= C06 1206 PACKAGE
.01UF= X7R 1206 PACKAGE
.1UF= X7R 1210 PACKAGE
.33UF= Z5U 1210 PACKAGE
22UF= TANTALUM PACKAGE



FENCE PINS

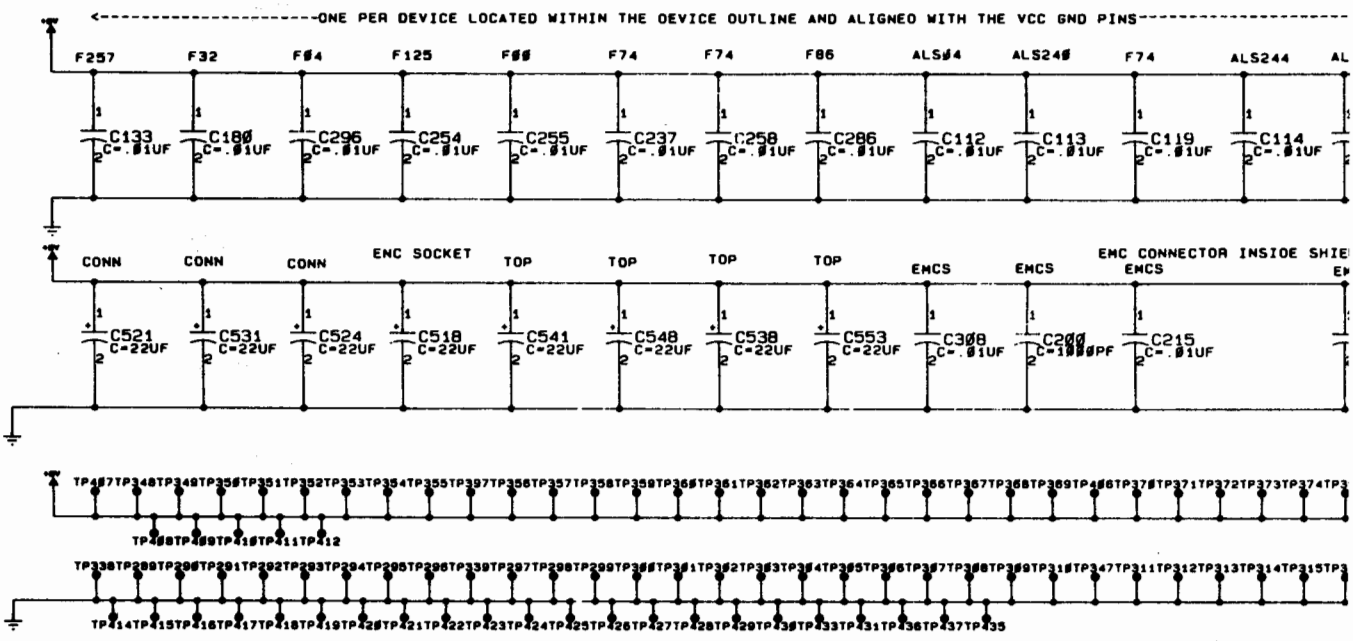
SMALL BREAK-AWAY PADS

TOOLING HOLES

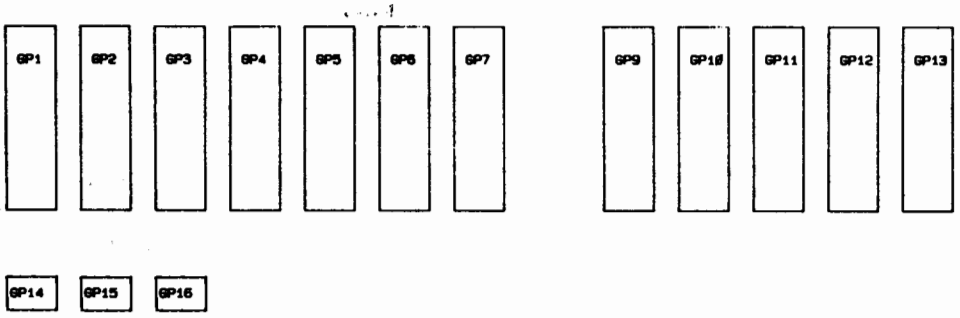
SLOTTED HOLES

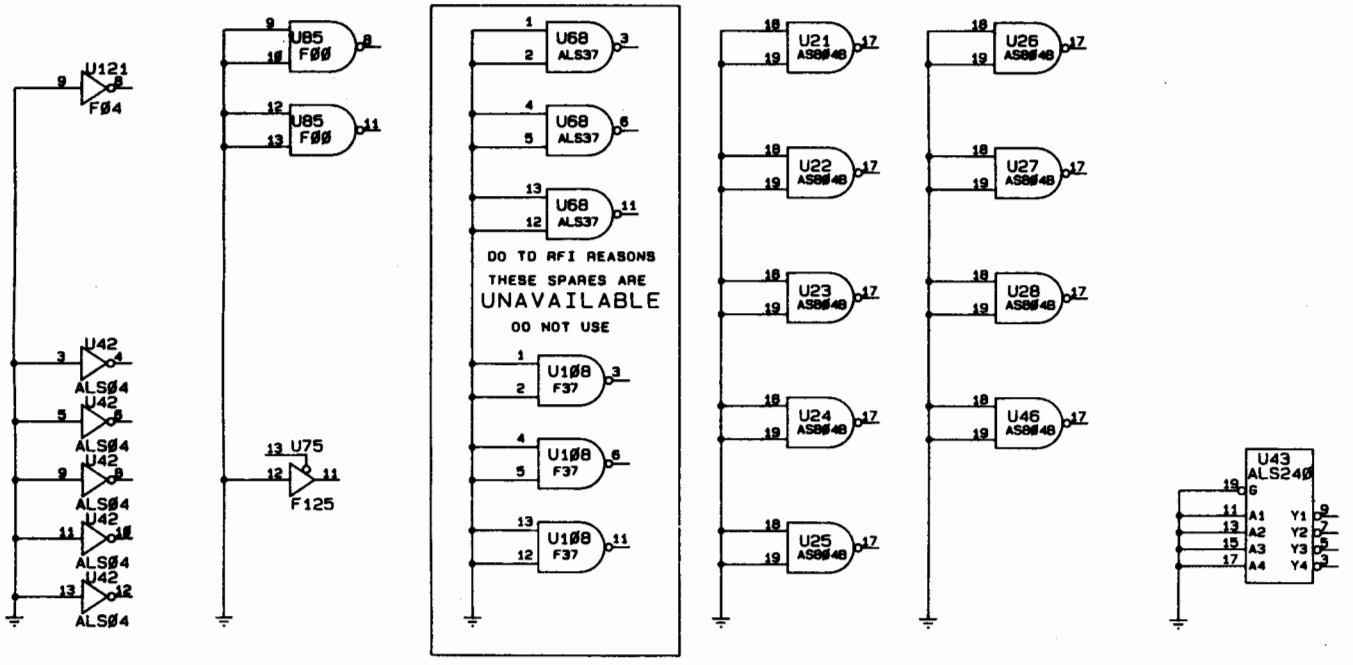
Processor/Memory PCA Schematic

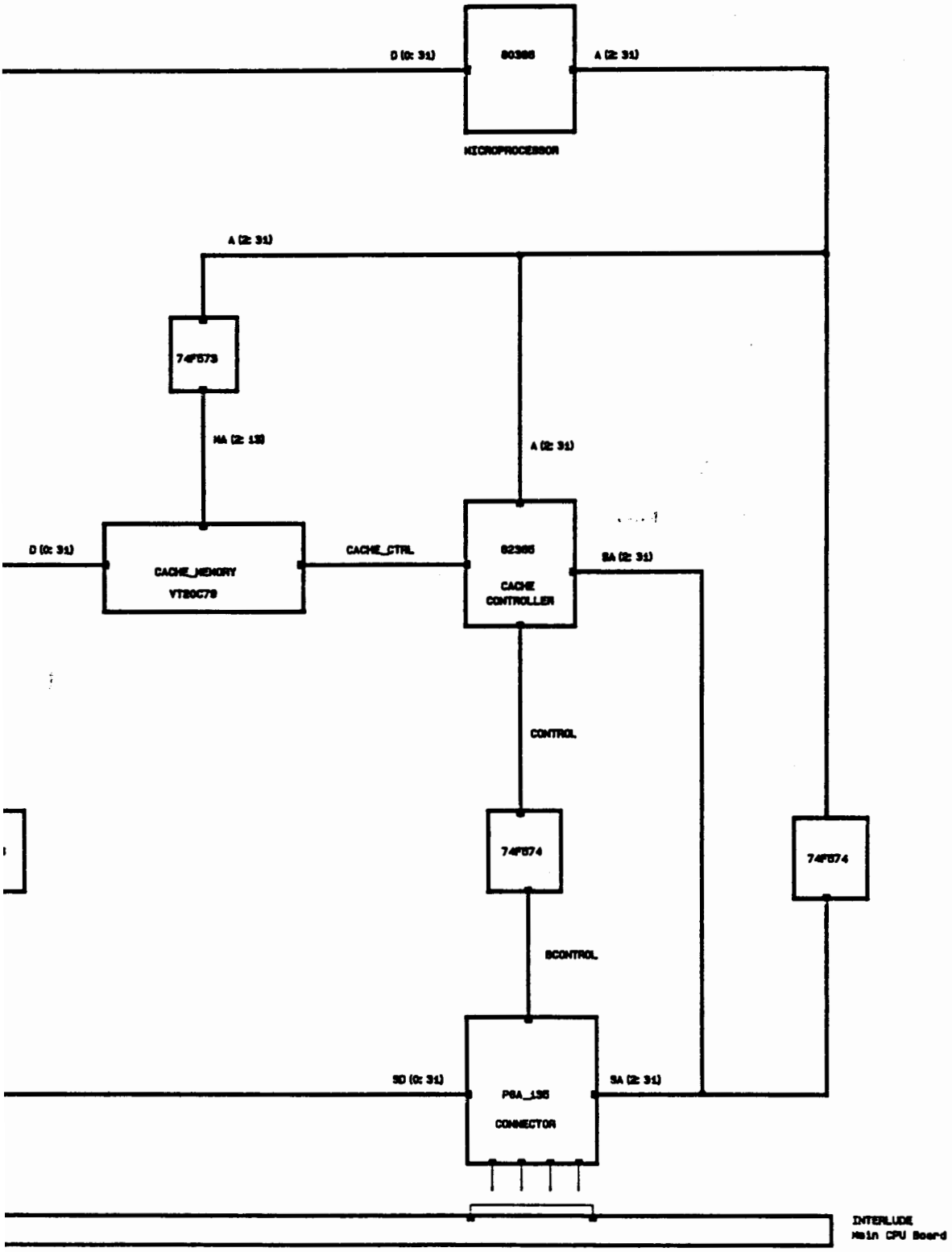
2-57/2-58


ONE PER DEVICE LOCATED WITHIN THE DEVICE OUTLINE AND ALIGNED WITH THE VCC GND PINS
F257
F32
F04
F125
F00
F74
F74
F86
ALS04
ALS240
F74
ALS244
C133 C=.01UF
C180 C=.01UF
C296 C=.01UF
C254 C=.01UF
C255 C=.01UF
C237 C=.01UF
C258 C=.01UF
C286 C=.01UF
C112 C=.01UF
C113 C=.01UF
C119 C=.01UF
C114 C=.01UF
CONN
CONN
CONN
ENC SOCKET
TOP
TOP
TOP
TOP
EMCS
EMCS
EMCS
EMC CONNECTOR INSIDE SHIE
C521 C=22UF
C531 C=22UF
C524 C=22UF
C518 C=22UF
C541 C=22UF
C548 C=22UF
C538 C=22UF
C553 C=22UF
C308 C=.01UF
C200 C=1000PF
C215 C=.01UF

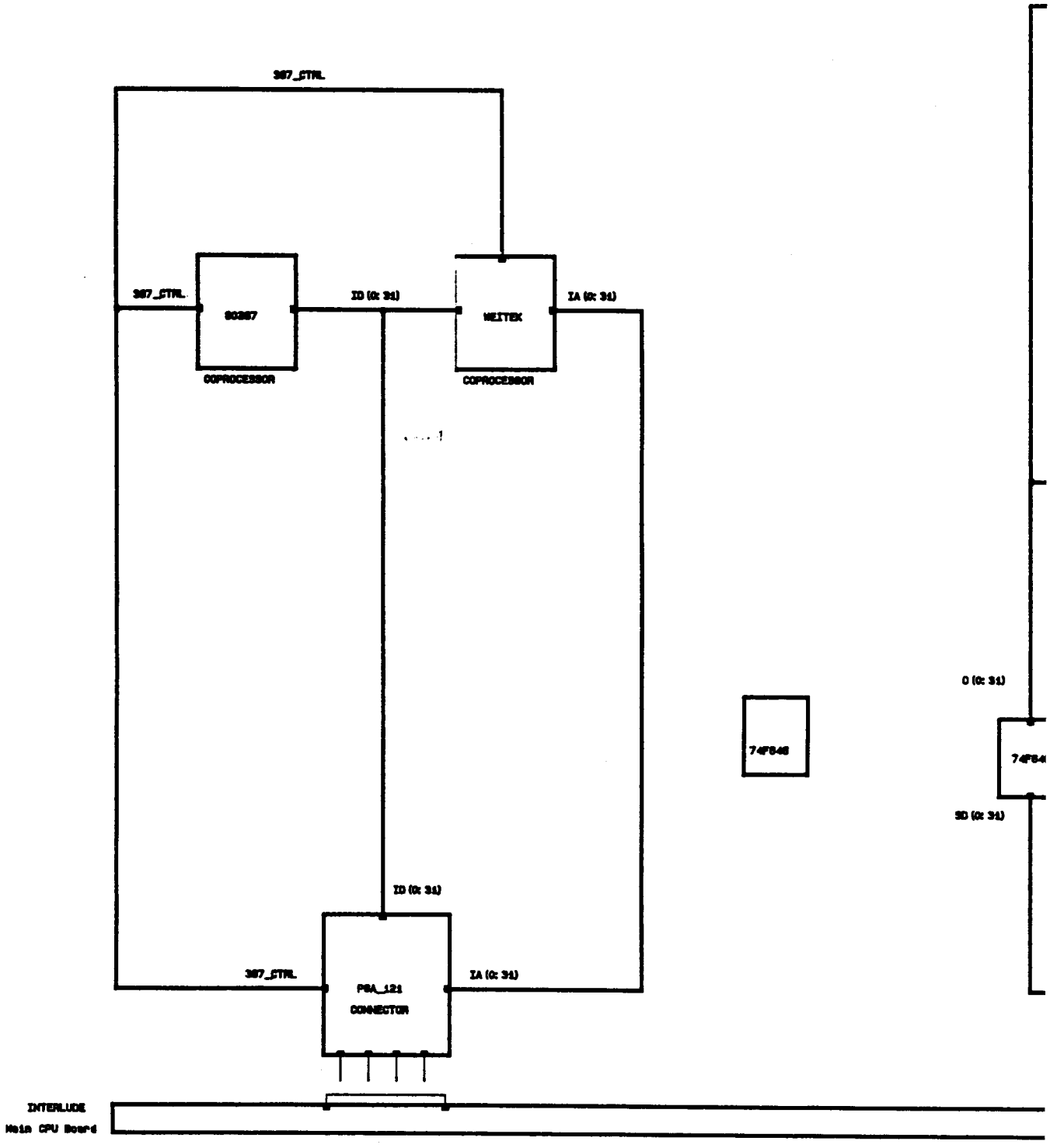
TP407TP408TP409TP410TP411TP412
TP414TP415TP416TP417TP418TP419TP420TP421TP422TP423TP424TP425TP426TP427TP428TP429TP430TP433TP431TP436TP437TP435

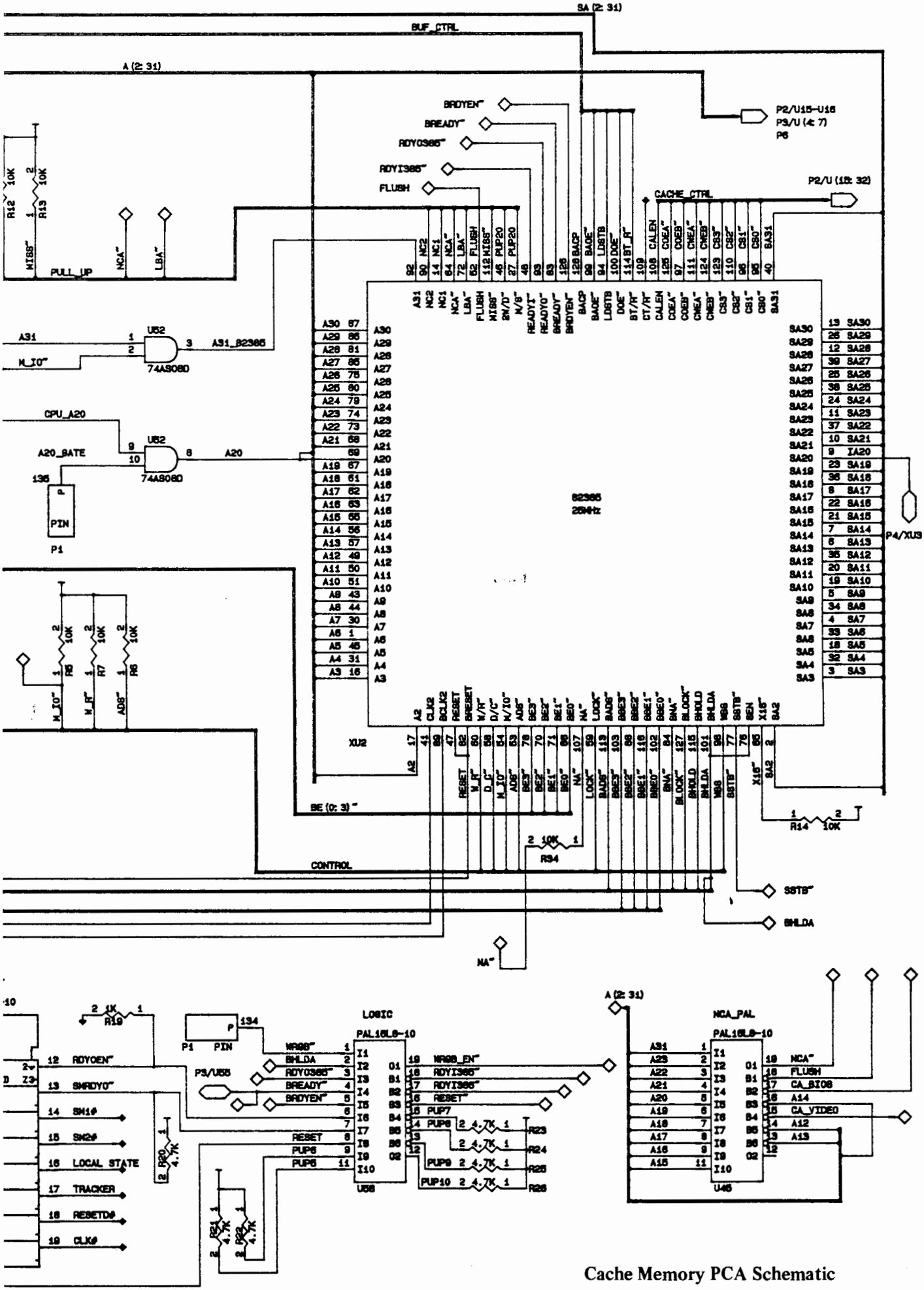

GP1
GP2
GP3
GP4
GP5
GP6
GP7
GP9
GP10
GP11
GP12
GP13
GP14
GP15
GP16


U121 F04
U85 F00
U68 ALS37
U21 AS804B
U26 AS804B
U42 ALS04
U22 AS804B
U27 AS804B
U23 AS804B
U28 AS804B
U24 AS804B
U46 AS804B
U25 AS804B
U75 F125
U108 F37
DO TO RFI REASONS
THESE SPARES ARE
UNAVAILABLE
DO NOT USE
U43 ALS240

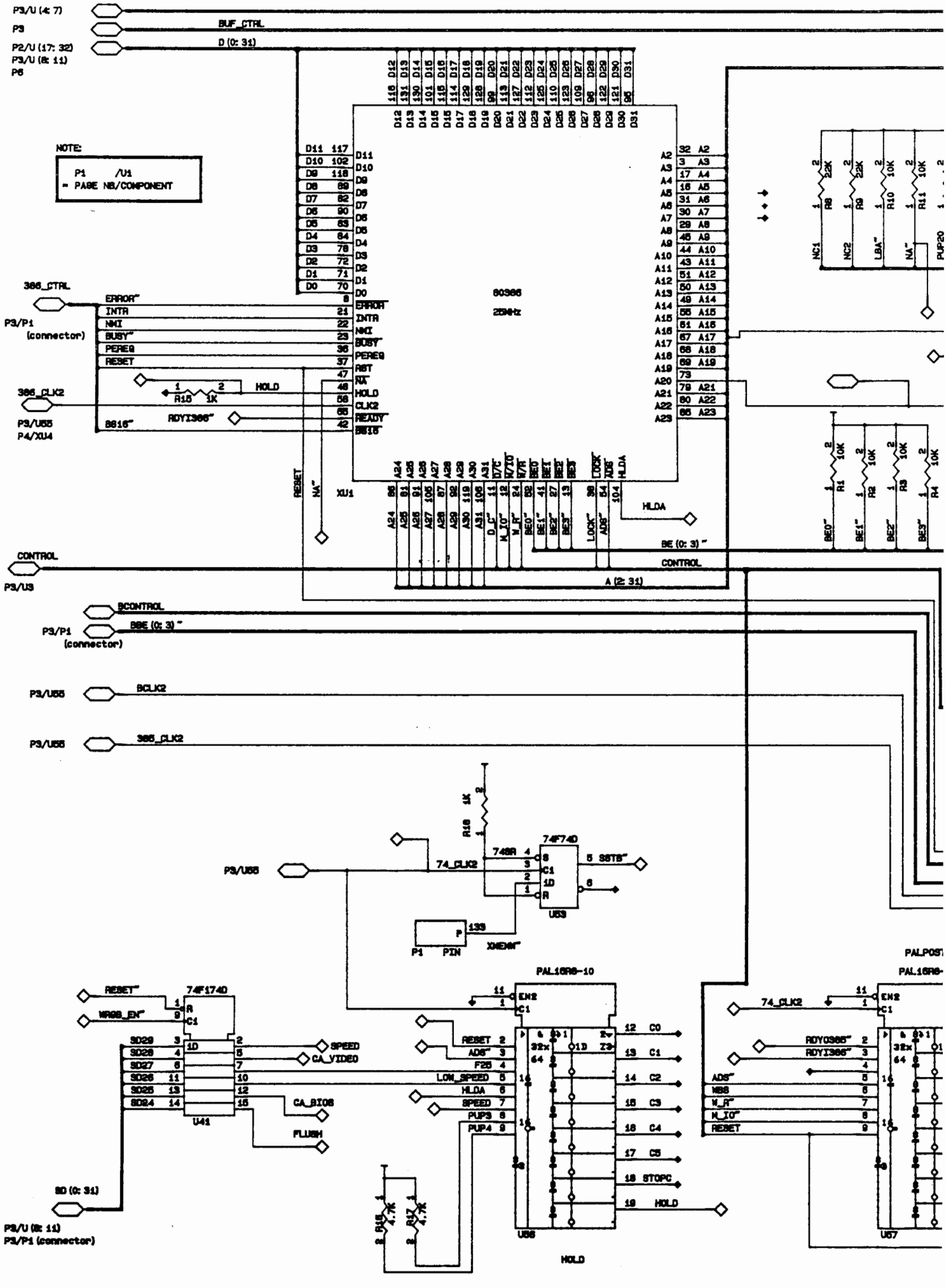


Cache Memory System PCA Schematic


387_CTRL
387_CTRL
80387
COPROCESSOR
ID (0: 31)
WEITEK
COPROCESSOR
IA (0: 31)
74F646
0 (0: 31)
74F64
SD (0: 31)
ID (0: 31)
387_CTRL
P8A_121
CONNECTOR
IA (0: 31)
INTERLUDE
Main CPU Board

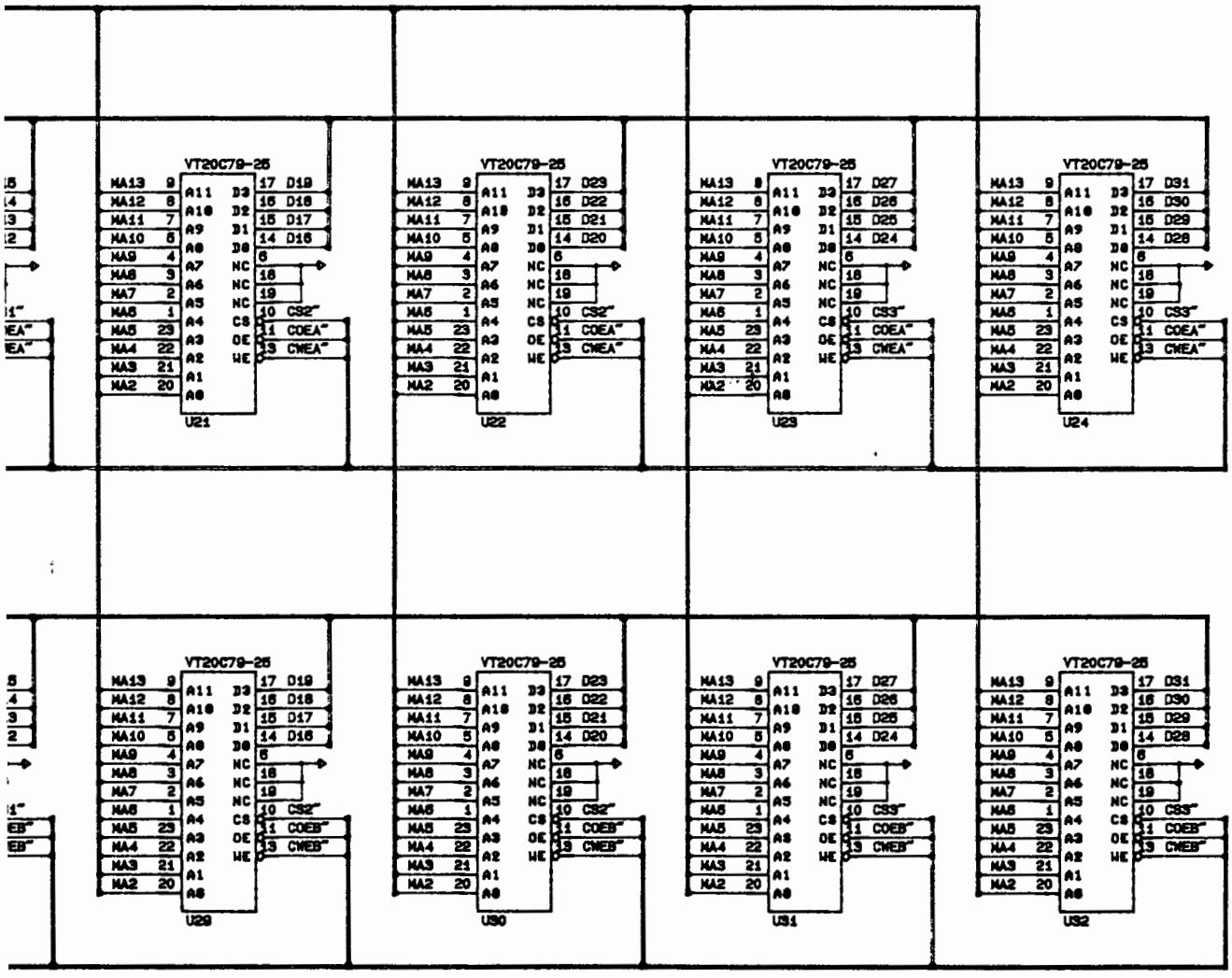


Cache Memory PCA Schematic

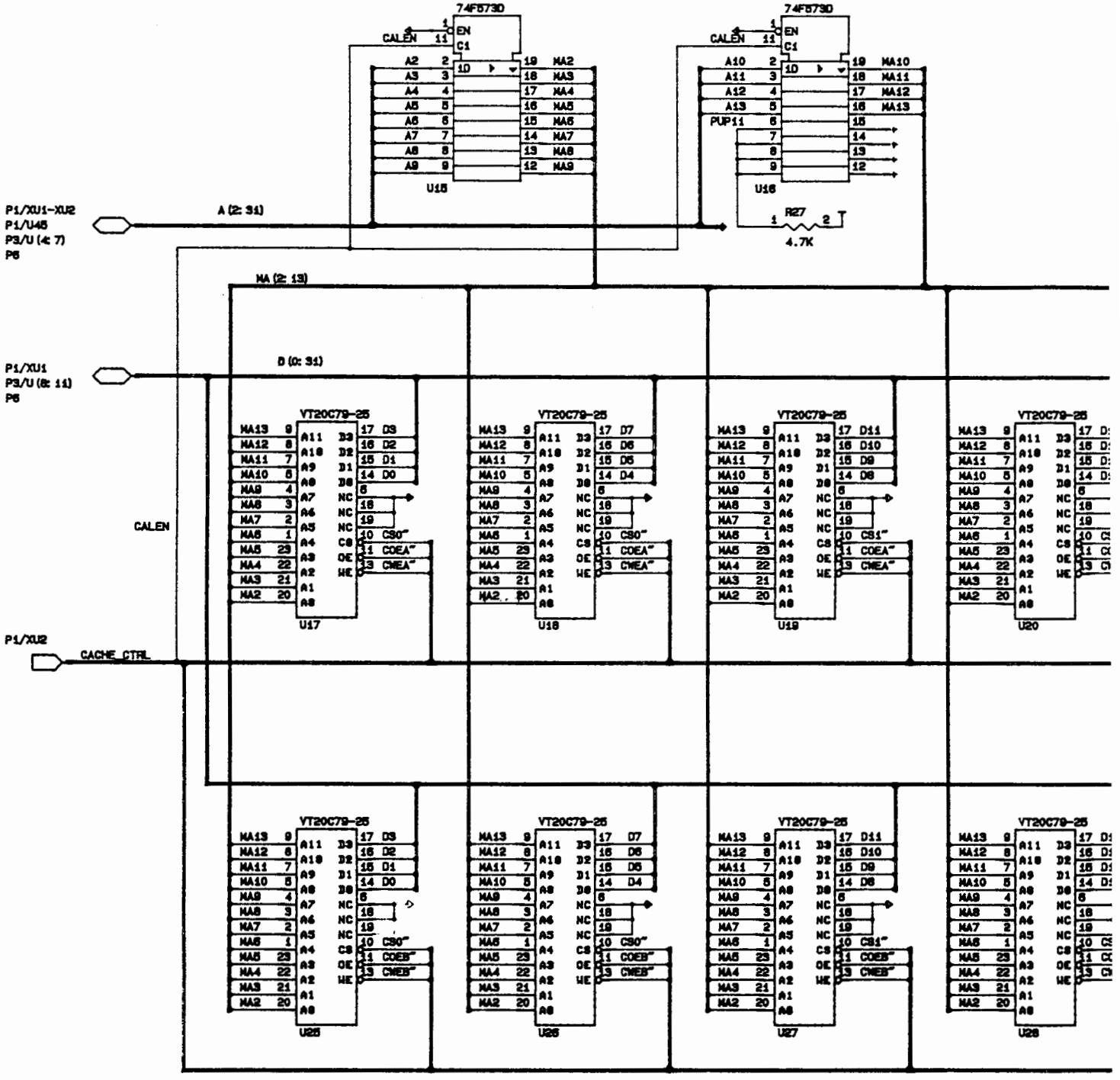

P3/U (4: 7)
P3
P2/U (17: 32)
P3/U (8: 11)
P6
BUF_CTRL
D (0: 31)
NOTE:
P1 /U1
= PASE NB/COMPONENT
386_CTRL
P3/P1
(connector)
ERROR"
INTR
NMI
BUSY"
PEREQ
RESET
386_CLK2
P3/U55
P4/XU4
8816"
HOLD
R15 1K
RDYI386"
80386
25MHz
XU1
RESET
NA"
HLDA
BE (0: 3) "
CONTROL
P3/U3
A (2: 31)
BCONTROL
P3/P1
(connector)
BBE (0: 3) "
P3/U55
BCLK2
P3/U55
386_CLK2
R16 1K
74F74D
74BR
74_CLK2
P3/U55
U59
S8TS"
P1 PIN 139
XMEM"
PAL16R6-10
RESET"
WR88_EN"
74F174D
SD29
SD28
SD27
SD26
SD25
SD24
U41
SPEED
CA_VIDEO
CA_BIOS
FLUSH
SD (0: 31)
P3/U (8: 11)
P3/P1 (connector)
RESET
AD8"
F25
LOW_SPEED
HLDA
SPEED
PUP3
PUP4
R17 4.7K
R18 4.7K
U56
C0
C1
C2
C3
C4
C5
STOPC
HOLD
HOLD
PALPOST
PAL16R6-
74_CLK2
RDYO386"
RDYI386"
AD8"
MB8
M_R"
M_IO"
RESET
U57
R8 22K
R9 22K
R10 10K
R11 10K
NC1
NC2
LBA"
NA"
PUP20
R1 10K
R2 10K
R3 10K
R4 10K
BE0"
BE1"
BE2"
BE3"

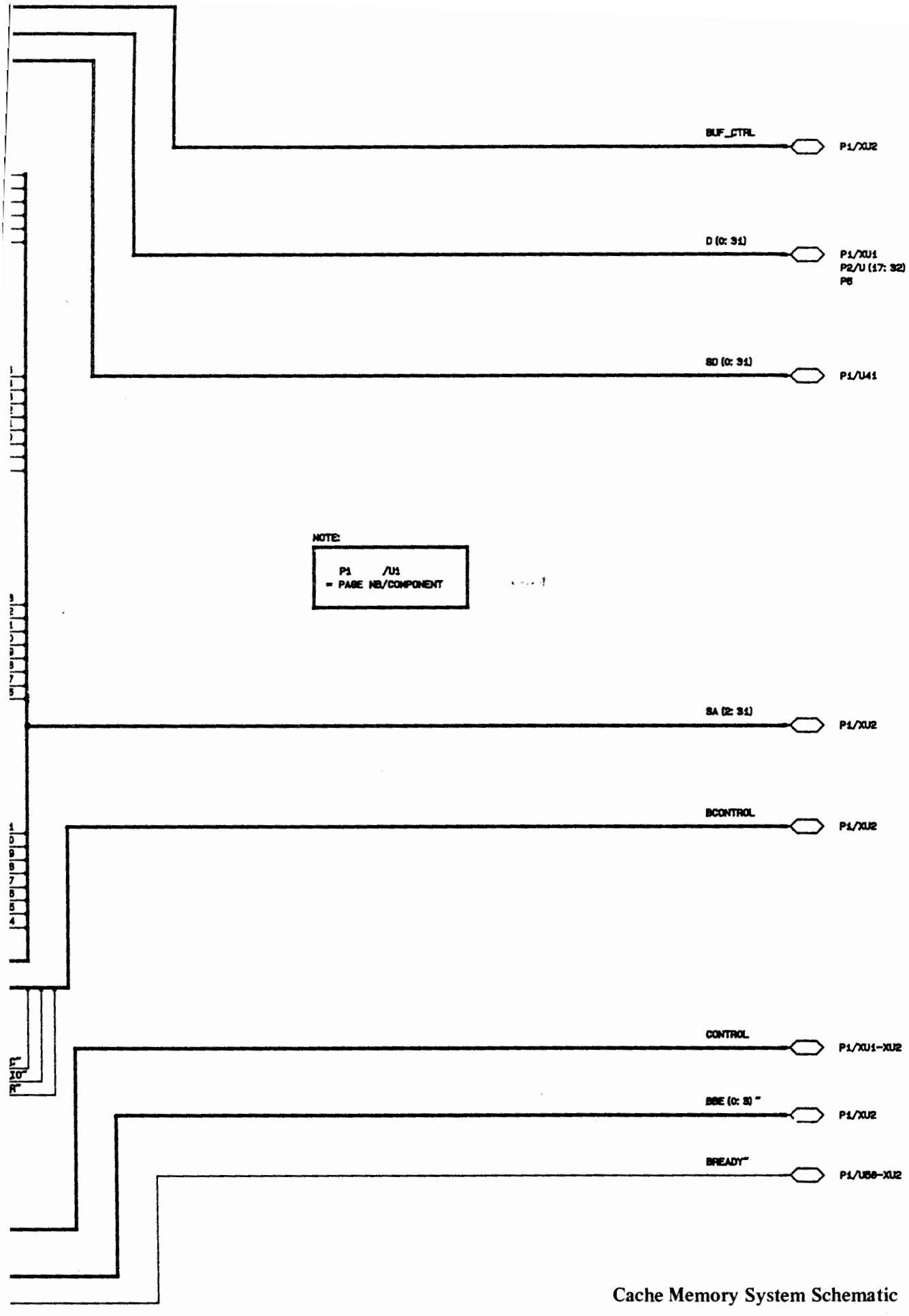
NOTE:

P1 /U1
= PAGE NB/COMPONENT

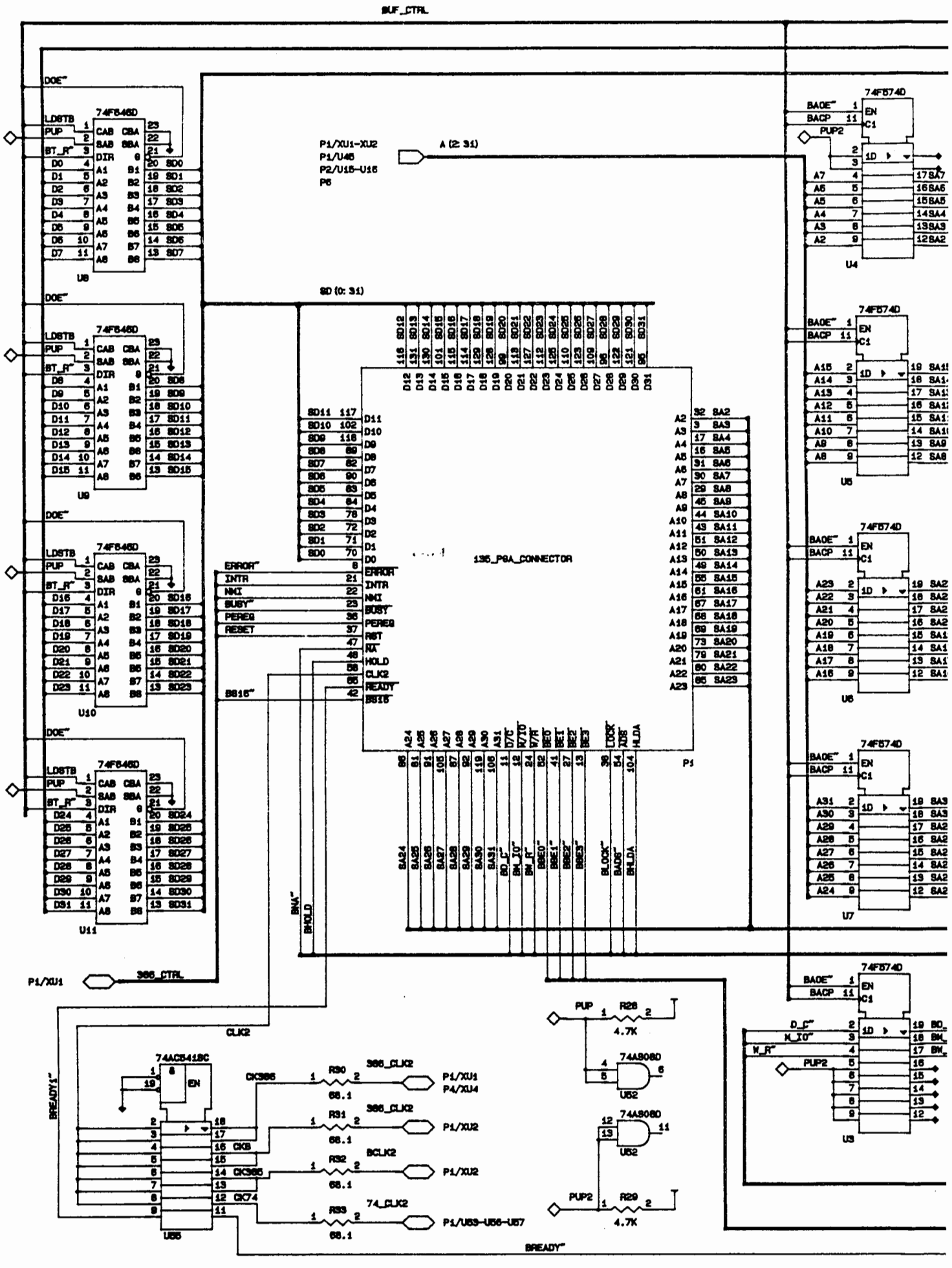


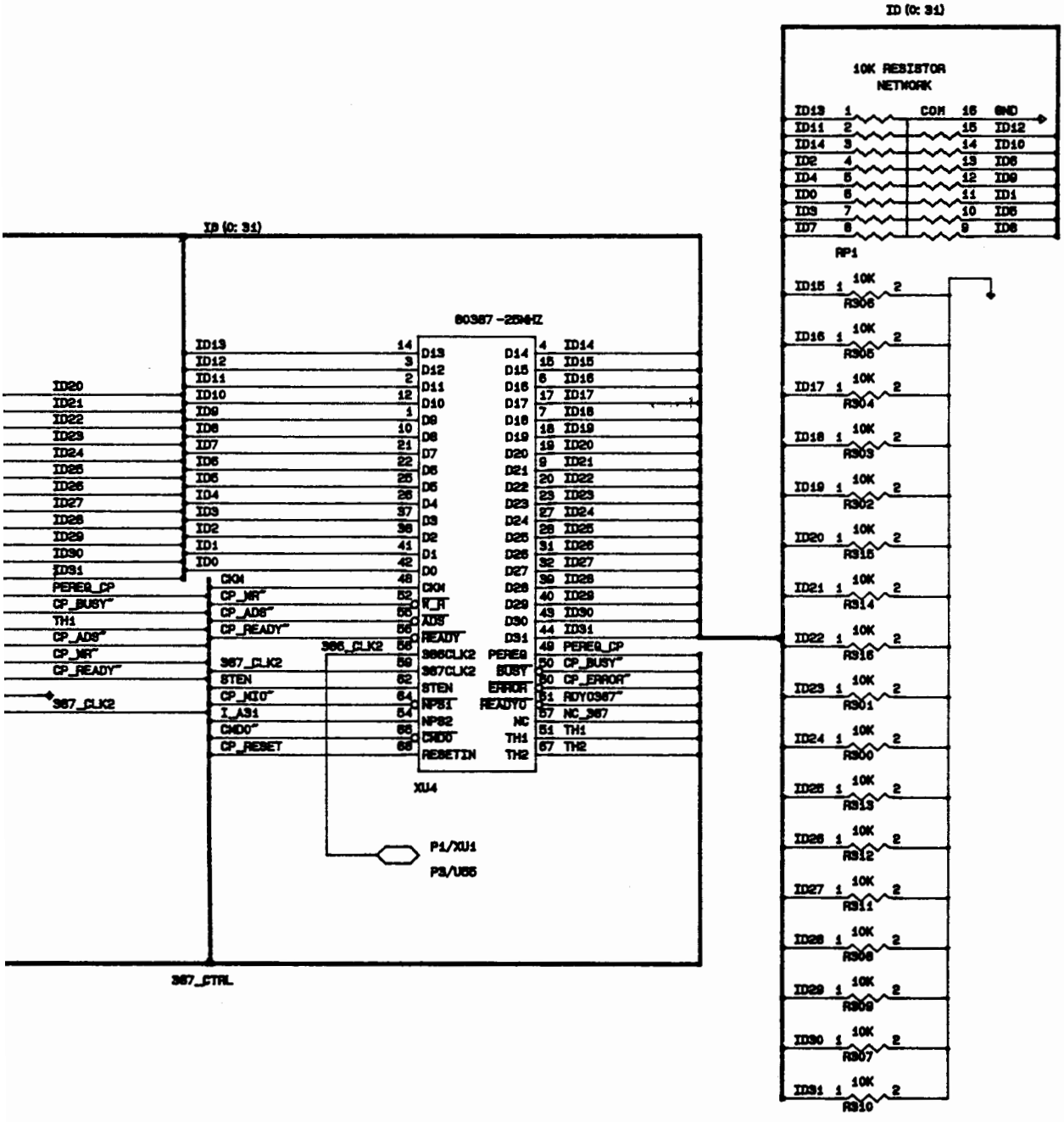
Cache Memory System Schematic


74F573D
U15
U16
CALEN
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
PUP11
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
R27
4.7K
P1/XU1-XU2
P1/U45
P3/U (4: 7)
P6
A (2: 31)
MA (2: 13)
P1/XU1
P3/U (8: 11)
P6
D (0: 31)
CALEN
P1/XU2
CACHE_CTRL
VT20C79-25
U17
U18
U19
U20
U25
U26
U27
U28
CS0"
CS1"
COEA"
CWEA"
COEB"
CWEB"



Cache Memory System Schematic

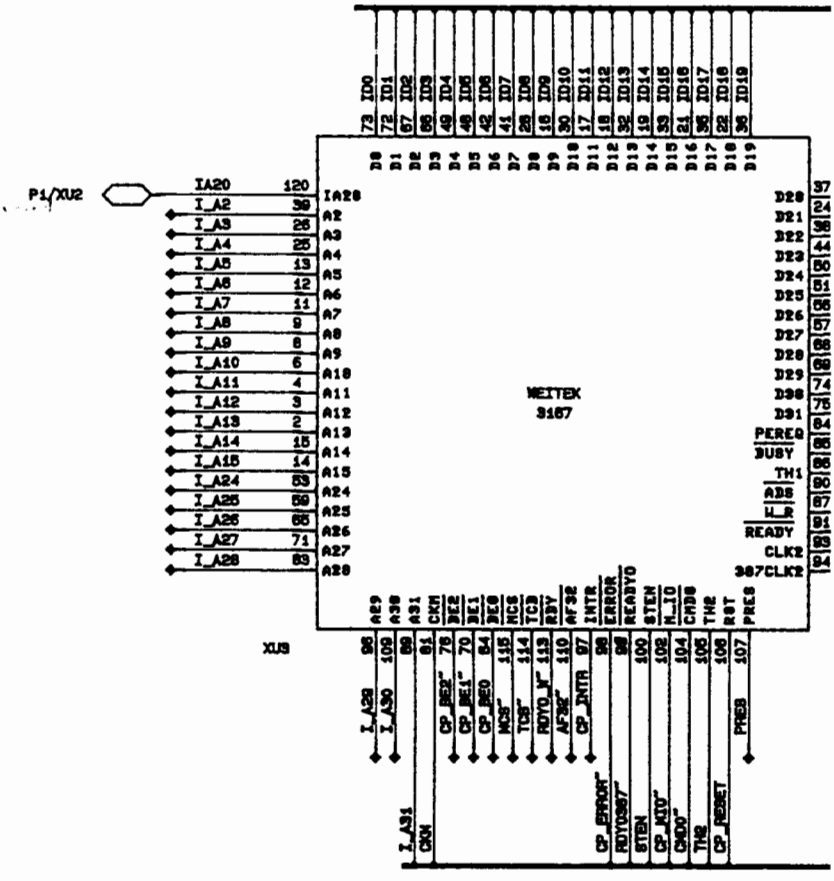

BUF_CTRL
74F646D
U8
U9
U10
U11
74F574D
U4
U5
U6
U7
U3
P1/XU1-XU2
P1/U45
P2/U15-U16
P6
A (2: 31)
SD (0: 31)
135_PGA_CONNECTOR
P1
ERROR"
INTR
NMI
BUSY"
PERER
RESET
HOLD
CLK2
READY"
BS16"
BNA"
BHOLD
366_CTRL
74AC541SC
U55
CK386
CK8
CK74
BCLK2
74_CLK2
386_CLK2
R30
R31
R32
R33
68.1
4.7K
R26
R29
74AS08D
U52
BREADY1"
BREADY"

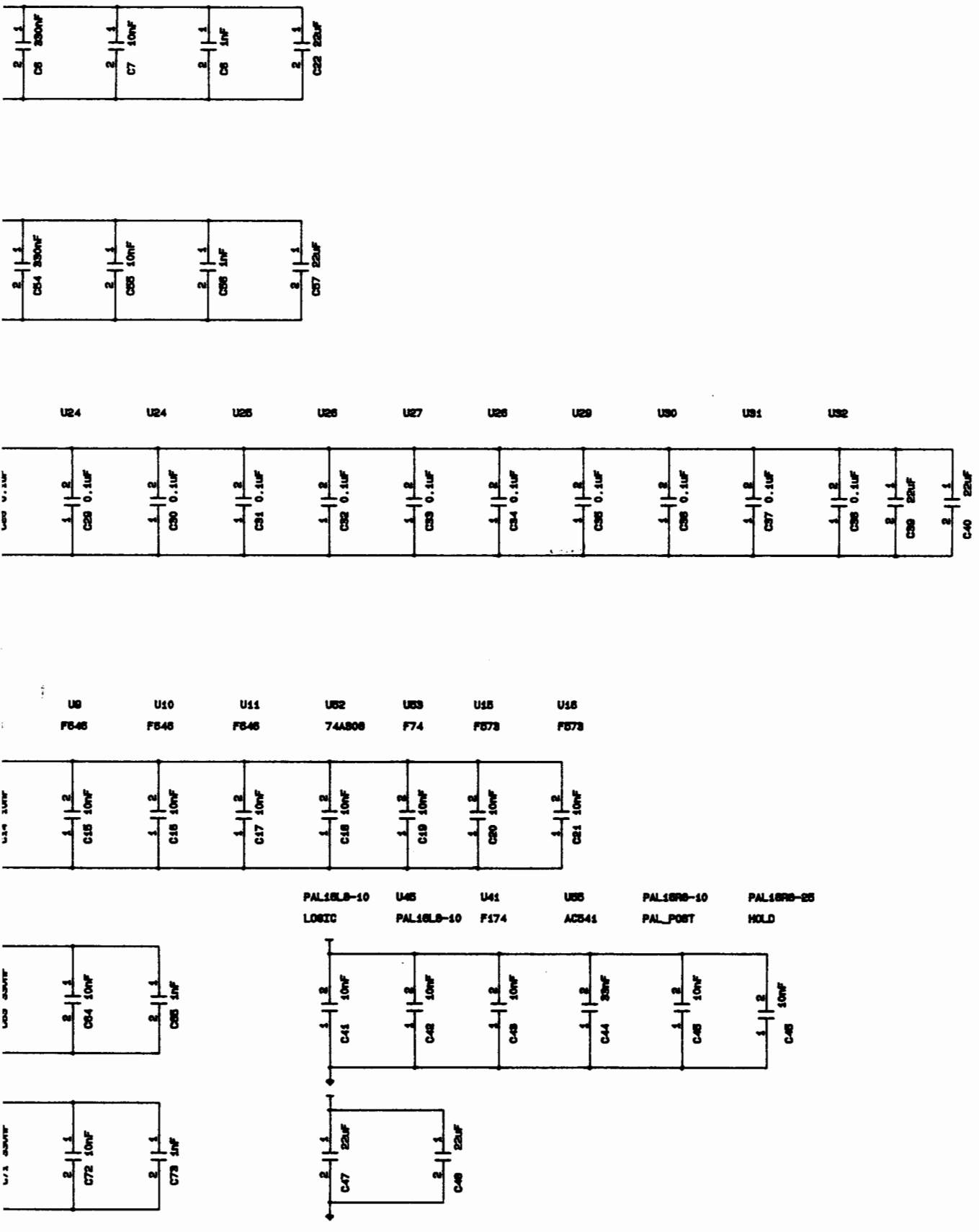


Cache Memory System Schematic

NOTE:

P1 /U1
= PAGE NB/COMPONENT





Cache Memory System Schematic

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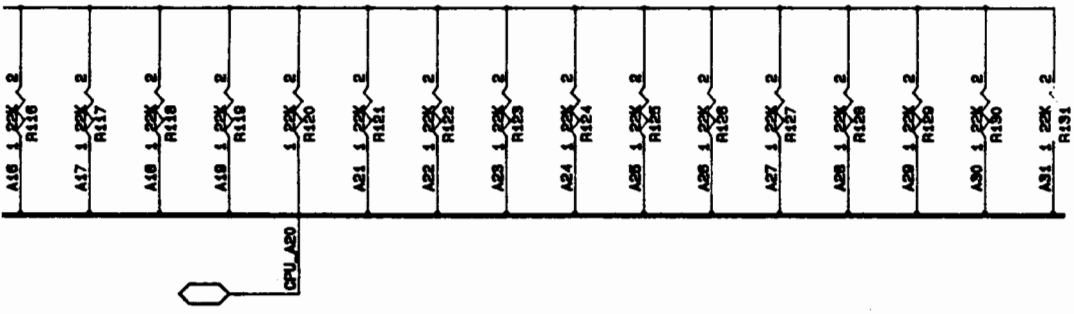
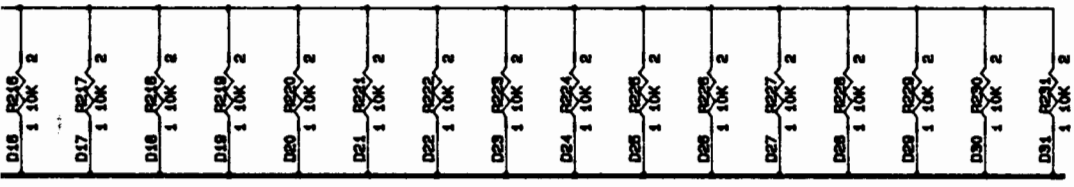
SRAMS VT20C79



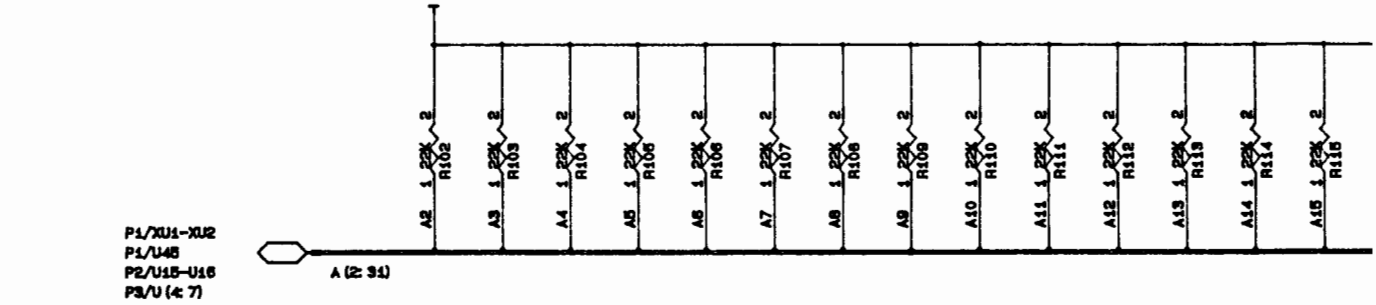


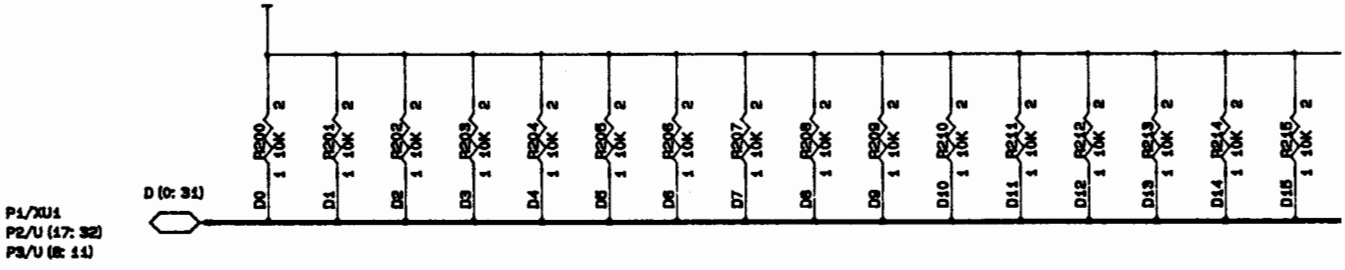
Cache Memory System Schematic

2-71/2-72

NOTE:

P1 /U1
= PAGE NB/COMPONENT





3

SYSTEM INTERFACE PRINTED CIRCUIT ASSEMBLY

3.1 Introduction

This chapter describes the System Interface PCA, a surface-mount printed circuit assembly which provides I/O support circuitry as well as the interconnection point for all other PCAs used in the system processing unit (SPU). Table 3-1 lists the major System Interface PCA components, and Figure 3-1 shows the layout. Figure 3-2 is a block diagram of the System Interface PCA. A discussion of the PCA's main components and their operation follows. (Schematics for the System Interface PCA are given at the end of the chapter.)

Table 3-1. Major System Interface PCA Components

1	power connector (J1)
1	connector slot for Input Device Connector PCA (J2)
1	connector slot for system fan/speaker/keylock assembly (J3)
8	backplane I/O connector slots (J4 to J11)
1	battery, with connector, for backup power to real-time clock/CMOS RAM (BT1, J180)
1	8042 keyboard controller (U56)
1	1RD2 HP-Human Interface Link Master Link Controller (U97)
1	8042 keyboard controller port expander, an HP-proprietary gate array (U98)
2	32-Kbyte BIOS ROMs (U102, U109)
2	sockets for option ROMs* (XU101, XU110)
1	82206 Integrated Peripheral Controller (U105)
2	150-pin connector slots for Processor/Memory PCA (J15, J23)

* Option ROMs are supported, but not installed.

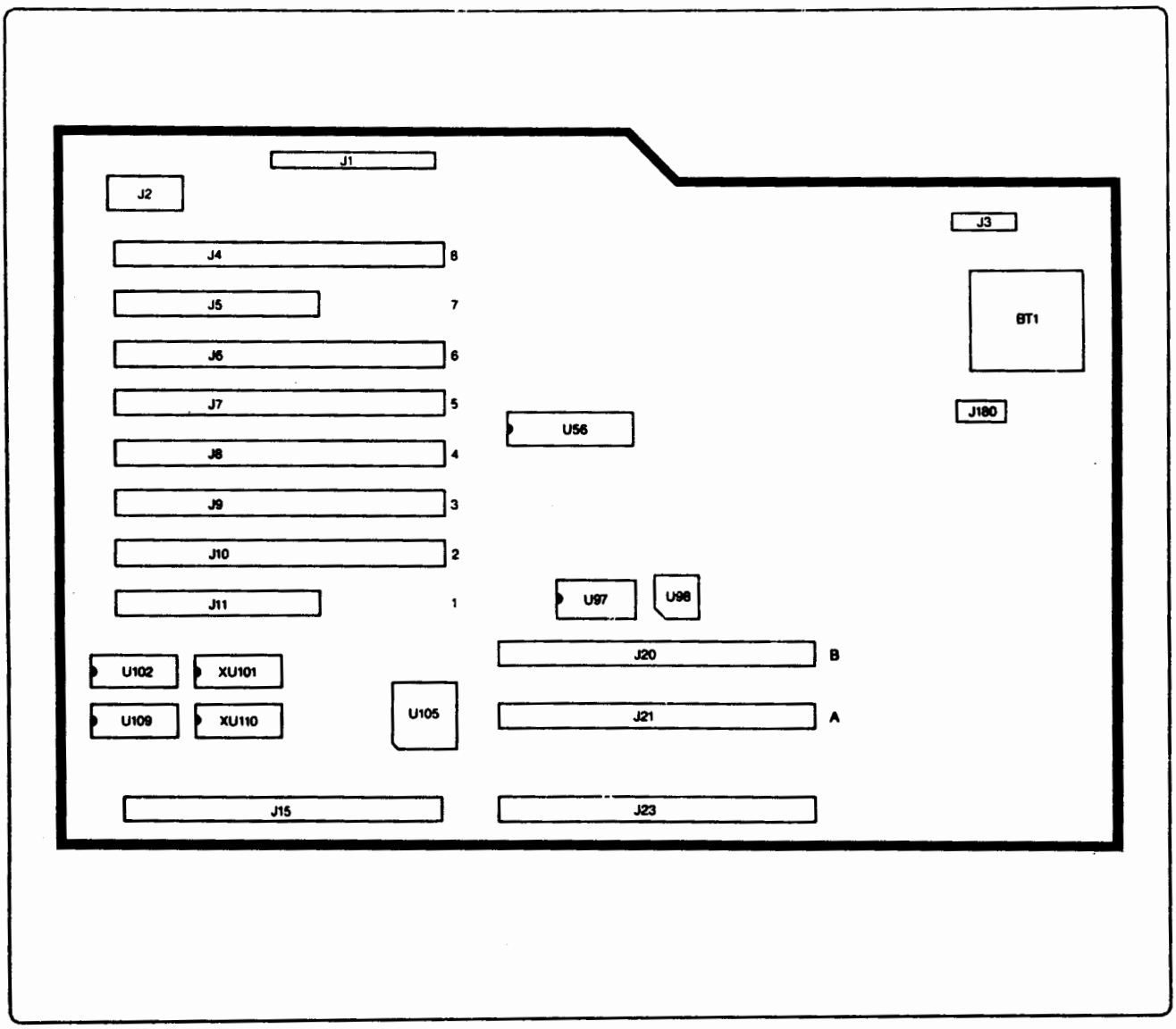


Figure 3-1. System Interface PCA Component Layout

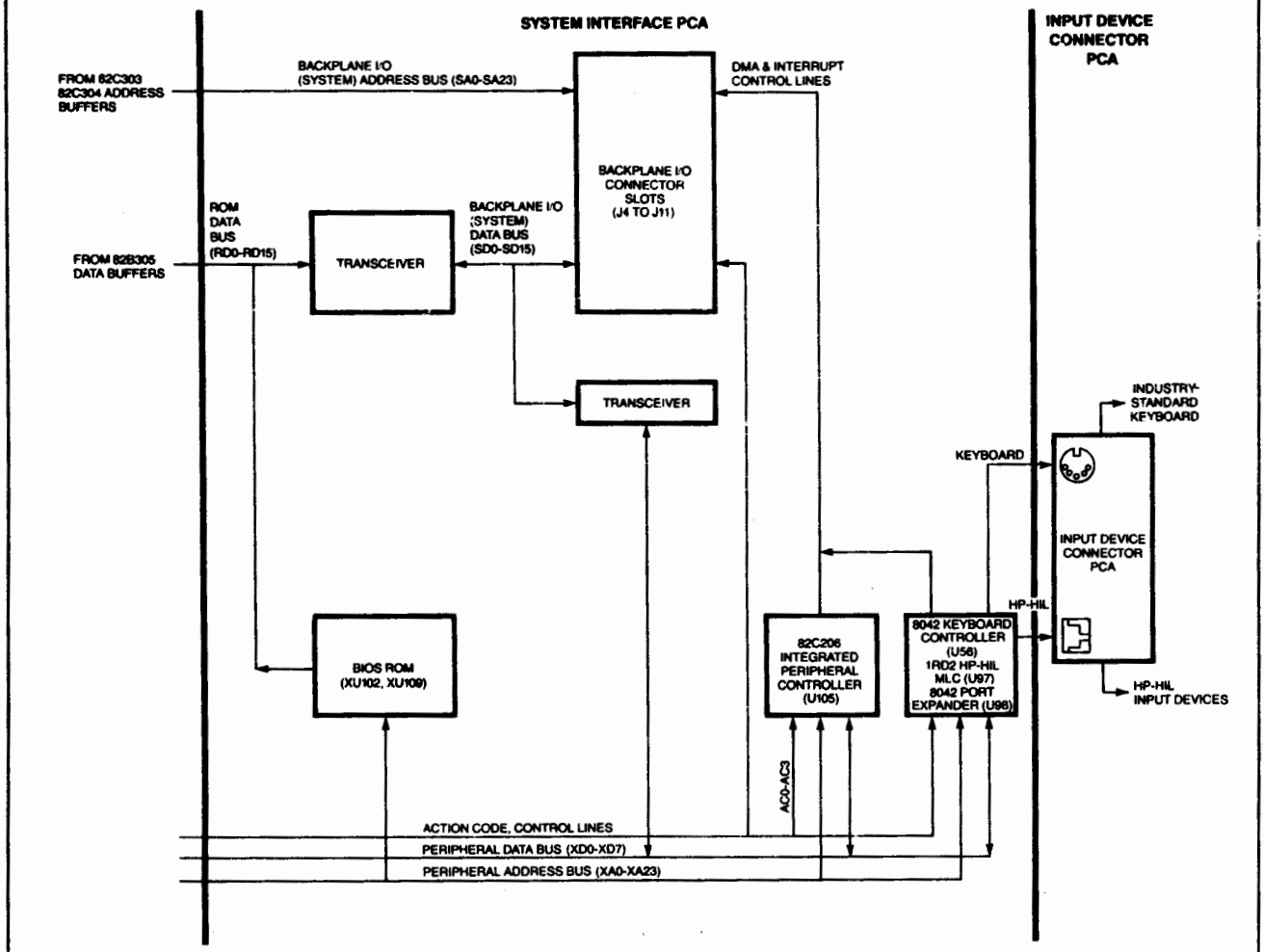


Figure 3-2. System Interface PCA/ Input Device Connector PCA Block Diagram

3.2 Integrated Peripheral Controller

The 82206 Integrated Peripheral Controller (IPC) combines the equivalent of the components in Table 3-2. The IPC top level system -- made up of an internal decode system and a clock and wait-state control system -- interconnects and controls four main IPC subsystems: DMA controller, interrupt controller, counter/timer, and real-time clock/CMOS RAM. Table 3-3 gives the I/O address map for the IPC components. (For more information on the IPC, refer to the Chips and Technologies data book, *82C206 Integrated Peripherals Controller* and the 82C series of technical reference documents.)

Table 3-2. Equivalent Components in the Integrated Peripheral Controller

2 8237A DMA controllers (DMA channels: 4 for 8-bit transfers; 3 for 16-bit transfers)
2 8259A interrupt controllers (13 interrupt request channels)
1 8254 counter/timer (2 counter/timer channels)
1 146818 real-time clock with CMOS RAM
1 74LS612 DMA page register

Table 3-3. I/O Address Map for IPC Components

IPC Component	Hex Address	Register Function
DMA Controller No. 1*	0000	Channel 0 Address (8 bit - DREQ0)
	0001	Channel 0 Count
	0002	Channel 1 Address (8 bit - DREQ1)
	0003	Channel 1 Count
	0004	Channel 2 Address (8 bit - DREQ2)
	0005	Channel 2 Count
	0006	Channel 3 Address (8 bit - DREQ3)
	0007	Channel 3 Count
	0008	Read Status/Write Command
	0009	DMA Request
	000A	Read Command/Write Single Mask Register Bit
	000B	Mode Register
	000C	Byte Pointer Flip-Flop
	000D	Read Temporary Register/Master Clear
	000E	Clear Mode/Clear Mask Register
	000F	Read/Write All Mask Register Bits
Interrupt Controller No. 1	0020	Master Interrupt Controller Register 0
	0021	Master Interrupt Controller Register 1
Configuration Register	0022	82Cxxx Index Register
	0023	82Cxxx Data Register

* See note on opposite page.

Table 3-3. I/O Address Map for IPC Components
(Continued)

IPC Component	Hex Address	Register Function
Counter/Timer	0040	Channel 0 Timer
	0041	Channel 1 Counter
	0042	Channel 2 Counter
	0043	Command Mode Register
Real-Time Clock/ CMOS RAM	0070	RTC/CMOS RAM Address (D0-D6), NMI Enable (D7) (Write)
	0071	RTC/CMOS RAM Data (Read/Write)
DMA Page Register	0081	8-bit DMA Channel 2 A16-A23
	0082	8-bit DMA Channel 3 A16-A23
	0083	8-bit DMA Channel 1 A16-A23
	0087	8-bit DMA Channel 0 A16-A23
	0089	16-bit DMA Channel 6 A17-A23
	008A	16-bit DMA Channel 7 A17-A23
	008B	16-bit DMA Channel 5 A17-A23
	008F	Refresh
Interrupt Controller No. 2	00A0	Slave Interrupt Controller Register 0
	00A1	Slave Interrupt Controller Register 1
DMA Controller No. 2*	00C0	Channel 4 Address (16 bit - Cascade)
	00C2	Channel 4 Count
	00C4	Channel 5 Address (16 bit - DREQ5)
	00C6	Channel 5 Count
	00C8	Channel 6 Address (16 bit - DREQ6)
	00CA	Channel 6 Count
	00CC	Channel 7 Address (16 bit - DREQ7)
	00CE	Channel 7 Count
	00D0	Read Status/Write Command
	00D2	DMA Request
	00D4	Read Command/Write Single Mask Register Bit
	00D6	Mode Register
	00D8	Byte Pointer Flip-Flop
	00DA	Read Temporary Register/Master Clear
	00DC	Clear Mode/Clear Mask Register
	00DE	Read/Write All Mask Register Bits

*Note: I/O registers for DMA controller 1 (for 8-bit transfers) are located on consecutive addresses, while I/O registers for DMA controller 2 are on even-byte addresses. All DMA registers should be loaded with valid parameters after power-up or reset, even if some channels are unused.

3.2.1 DMA Controller

Direct-memory access is provided by the 82206 IPC's DMA controller, which consists of two four-channel DMA controllers (equivalent to two 8237As), the DMA address map, DMA address map selects, and the DMA page register (equivalent to a 74LS612 page register). (Refer to the "I/O Address Map for IPC Components" in this chapter for a breakdown of DMA register assignments.)

DMA Controller Operation

1. Clock Cycle

Depending on the configuration of the IPC DMA configuration registers (022h and 023h), the HP Vectra RS/16 can run from a 4-MHz clock, and the HP Vectra RS/20 can run from a 4-MHz or 5-MHz clock.

2. Operating Conditions

The IPC's DMA controller has three types of operating conditions: program, idle, or active. Once the program condition has been entered to program the DMA controller registers, the DMA controller operates in either the idle or the active condition. In the idle condition, the DMA controller waits for an I/O device to request direct-memory access through one of the 7 DMA channels. When the DMA controller receives a DMA request from an I/O device, it enters the active condition, resolves priority for the channel requesting DMA, and issues HRQ1 (a hold request) to the 82301 bus controller.

The bus controller, in turn, generates a hold request to the 80386 microprocessor, which issues a hold acknowledge (HLDA) after finishing its current operation. By sending out HLDA1 to the IPC, the data buffer, and the address buffer, the bus controller signals to the data and address buffers that the IPC controls the buses.

3. Controller Channels

The DMA controllers (DMA1 and DMA2) generate memory addresses and control signals for transferring data from an I/O device to memory, or from memory to an I/O device, with little intervention from the 80386 microprocessor.

DMA1 (I/O hex address 0000 to 000F) provides four DMA channels, 0 to 3, and supports 8-bit data transfers between 8-bit I/O devices and 8-bit or 16-bit memory. During 8-bit to 16-bit transfers, the bus controller and the data buffers provide the required multiplexing. Throughout the system's 16-Mbyte addresses, each channel can transfer data 8 bits or 16 bits at a time, in blocks as large as 64 Kbytes. (Flexible disc transfers take place with DMA1 channel 2.)

DMA2 (I/O hex address 00C0 to 00DE), provides three DMA channels, 5 to 7, and supports 16-bit data transfers between 16-bit I/O devices and 16-bit memory. (DMA2's Channel 4 cascades DMA1 to DMA2 and is unavailable.) Throughout the system's 16-Mbyte addresses, these 16-bit DMA channels can transfer data 16 bits at a time, in blocks as large as 128 Kbytes, where 128 Kbytes equal one "page." All DMA memory transfers through channels 5 through 7 must occur on even-byte boundaries.

4. Address Generation

Addresses from DMA channels are not incremented or decremented across page boundaries. The DMA page register (hex address 0081 to 008F) supplements direct-memory access, driving upper address lines as required, while the lower address bits are provided by the IPC, which accesses system RAM via the bus controller.

3.2.2 Interrupt Controllers

System (Maskable) Interrupts, from IPC Interrupt Controller

Interrupts to the system's 80386 microprocessor are provided by the 82206 IPC's interrupt controller, equivalent to two 8259s, and consisting of two cascaded 8-input interrupt controllers, INTC1 and INTC2. The interrupt controllers provide 16 interrupt channels, 3 of which are used internally by the IPC, and 13 of which are used for interrupt requests. (Refer to this chapter's "I/O Address Map for IPC Components" for a breakdown of the interrupt controller register assignments.)

The IPC's interrupt controller acts as a system-wide interrupt manager. It accepts requests from I/O devices, resolves priority on pending interrupts, issues interrupt requests to the 80386 microprocessor, and provides a interrupt vector which the 80386 uses as an index to determine which interrupt service routine (ISR) to execute.

For proper operation of the 16 interrupt channels, the interrupt controllers must be programmed for the cascade mode. When cascaded, INTC1 (I/O hex address 0020 to 0021) is the master interrupt controller, and INTC2 (I/O hex address 00A0 to 00A1) is the slave. The interrupt request output signal, INT, is internally connected from INTC2 to INTC1's interrupt request input (IRQ2). For additional information regarding system interrupts, refer to the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

Non-Maskable Interrupts

Besides system interrupts provided by the IPC's 8259 interrupt controllers, the 80386 microprocessor has a non-maskable interrupt (NMI) bit that can be set and reset with system programs. The non-maskable interrupt processes the system response to either memory parity errors or errors signalled by an accessory card through the backplane I/O signal, I/OCHCK*.

The NMI signal is masked from the 80386 microprocessor at system reset. It must be enabled via system software, which is done by setting to a 0, bit 7 of I/O address register 70h. (The same bit 7 can be masked by setting it to a 1.) The 80386 NMI generates interrupt vector number 02, which has an interrupt vector address of 008h to 00Bh. (See Table 3-4, the Interrupt Map.) For additional information regarding NMI programming considerations, refer to the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

Interrupt Map

Table 3-4 provides a complete map of all interrupts in the HP Vectra RS. For a particular interrupt, the table gives the hex interrupt vector number, the hex interrupt vector address, the function of the interrupt, the type of interrupt, and the kind of routine which performs the interrupt.

* Active low.

Table 3-4. Interrupt Map

Interrupt	Address	Function	Type	Routine**
00*	000-003	Divide by Zero	CPU (1)	STD-BIOS
01	004-007	Single Step	CPU (1)	STD-BIOS
02	008-00B	Non-maskable Interrupt	CPU	STD-BIOS
03	00C-00F	Software Breakpoint	CPU (1)	STD-BIOS
04	010-013	Arithmetic Overflow	CPU (1)	STD-BIOS
05	014-017	Print Screen	SW (2)	STD-BIOS
06	018-01B	Invalid Opcode	CPU (1)	STD-BIOS
07	01C-01F	Reserved	CPU (1)	STD-BIOS
08	020-023	IRQ0 (Timer 0 Interrupt)	HW	STD-BIOS
09	024-027	IRQ1 (Keyboard ISR)	HW	STD-BIOS
0A	028-02B	IRQ2 (From Interrupt Cont. No. 2)	HW	STD-BIOS
0B	02C-02F	IRQ3 (Serial Port 2 ISR)	HW (1)	STD-BIOS
0C	030-033	IRQ4 (Serial Port 1 ISR)	HW (1)	STD-BIOS
0D	034-037	IRQ5 (Parallel Port 2 ISR)	HW (1)	STD-BIOS
0E	038-03B	IRQ6 (Flexible Disc Controller ISR)	HW	STD-BIOS
0F	03C-03F	IRQ7 (Parallel Port 1 ISR)	HW (1)	STD-BIOS
10	040-043	Video I/O	SW (2)	STD-BIOS
11	044-047	Equipment Configuration Check	SW (2)	STD-BIOS
12	048-04B	Base Memory Size	SW (2)	STD-BIOS
13	04C-04F	Flexible/Hard Disc Controller I/O	SW (2)	STD-BIOS
14	050-053	Serial Port Driver	SW (2)	STD-BIOS
15	054-057	System Functions	SW (2)	STD-BIOS
16	058-05B	Keyboard I/O	SW (2)	STD-BIOS
17	05C-05F	Parallel Port Driver	SW (2)	STD-BIOS
18	060-063	Reserved	SW (3)	N/A
19	064-067	Boot	SW (2)	STD-BIOS
1A	068-06B	Time and Date	SW (2)	STD-BIOS
1B	06C-06F	Keyboard Break	SW (3)	STD-BIOS
1C	070-073	Timer Tick	SW (3)	STD-BIOS
1D	074-077	Video Parameter Table	PT	STD-BIOS
1E	078-07B	Flexible Disc Parameter Table	PT	STD-BIOS
1F	07C-07F	Video Graphics Character Table	PT	STD-BIOS

* All interrupt vector numbers and interrupt vector addresses are in hex.
** Refer to this chapter's "Read-Only Memory" section for a discussion of STD-BIOS.
CPU = Interrupt of 80386 Microprocessor
HW = Hardware Interrupt
IRQ = Interrupt Request Channel
ISR = Interrupt Service Routine
N/A = Not Applicable
PT = Interrupt Vector Used as Pointer to Data
SW = Software Interrupt
(1) = Unused Interrupt
(2) = Application-Callable Entry Point
(3) = Interrupt Returned

Table 3-4. Interrupt Map (Continued)

Interrupt	Address	Function	Type	Routine**
20*	080-083	DOS Program Terminate	SW	DOS
21	084-087	DOS Function Calls	SW	DOS
22	088-08B	DOS Terminate Address	PT	DOS
23	08C-08F	DOS <CTRL>-<Break> Address	SW	DOS
24	090-093	DOS Critical Error	SW	DOS
25	094-097	DOS Absolute Disc Read	SW	DOS
26	098-09B	DOS Absolute Disc Write	SW	DOS
27	09C-09F	DOS Terminate, Stay Resident	SW	DOS
28-32	0A0-0CB	Reserved for DOS	SW	DOS
33	0CC-0CF	HP-HIL Mouse	SW (2)	EX-BIOS
34-3F	0D0-0FF	Reserved for DOS	SW	DOS
40	100-103	Alternate Fiexible Disc Controller	SW	STD-BIOS
41	104-107	Hard Disc Parameter Table (0)	PT	STD-BIOS
42-45	108-117	Reserved	SW	STD-BIOS
46	118-11B	Hard Disc Parameter Table (1)	PT	STD-BIOS
47-5F	11C-17F	Reserved	SW	STD-BIOS
60-6E	180-1BB	Reserved for User Programs	SW	N/A
6F	1BC-1BF	Default EX-BIOS Entry Point	SW (2)	EX-BIOS
70	1C0-1C3	IRQ8 (Real-time Clock ISR)	HW	STD-BIOS
71	1C4-1C7	IRQ9 (Redirect of IRQ 9 from back-plane I/O to Vector 0A, 28h-2Bh)	HW	STD-BIOS
72	1C8-1CB	IRQ10 (Serial Port 3 ISR)	HW (1)	STD-BIOS
73	1CC-1CF	IRQ11 (Serial Port 4 ISR)	HW (1)	STD-BIOS
74	1D0-1D3	IRQ12 (Reserved)	HW (1)	STD-BIOS
75	1D4-1D7	IRQ13 (Coprocessor(s))	HW	STD-BIOS
76	1D8-1DB	IRQ14 (Hard Disc Controller ISR)	HW (1)	STD-BIOS
77	1DC-1DF	IRQ15 (Reserved)	HW (1)	STD-BIOS
78-7F	1E0-1FF	Not Used	SW	N/A
80-F0	200-3C3	Reserved	SW	N/A
F1-FF	3C4-3FF	Not Used	SW	N/A

* All interrupt vector numbers and interrupt vector addresses are in hex.
** Refer to this chapter's "Read-Only Memory" section for a discussion of STD-BIOS and EX-BIOS.
HW = Hardware Interrupt
IRQ = Interrupt Request Channel
ISR = Interrupt Service Routine
N/A = Not Applicable
PT = Interrupt Vector Used as Pointer to Data
SW = Software Interrupt
(1) = Unused Interrupt
(2) = Application-Callable Entry Point

3.2.3 Real-Time Clock/CMOS RAM

The 82206 IPC provides the system with real-time clock (RTC) and CMOS RAM functions equivalent to those provided by the MC146818 chip. The RTC/CMOS RAM consists of 128 bytes of memory, which include 10 time-of-day clock bytes for real-time clocking, calendar, and alarm functions, 4 bytes for control and status lines, and 114 bytes of CMOS RAM. (See Table 3-5 for the real-time clock/CMOS RAM memory map.)

The 10 bytes for the RTC time-of-day clock provide the time of day, and count seconds, minutes, hours, days, and years. They also provide calendar functions, keeping track of the day of the week and providing automatic leap year compensation. In addition, these bytes provide for programmable interrupt requests (IRQ8) at either a fixed interval (for example, every second), or when a certain time has arrived (in the alarm clock mode).

The 4 bytes for control and status lines control the RTC/CMOS RAM operation and monitor its status.

The 114 bytes of CMOS RAM provide non-volatile memory to store HP Vectra RS system configuration and calibration parameters when power is removed from the system. All the 114 CMOS RAM bytes are either currently used or reserved, with no user-definable bytes. However, applications may read these bytes to determine system configuration, or write to them, providing the byte definitions of Table 3-5 are adhered to. The CMOS RAM bytes are not affected by the RTC and are accessible during the update cycle.

Real-Time Clock/CMOS RAM Operation

When the system power is on, the RTC/CMOS RAM operates from a 32.768 kHz crystal oscillator and gets its power from the system's power supply. During power-on reset, the system software reads the current time and date from the RTC and converts it into the appropriate number of system clock "ticks." From this point on, system time is kept via system clock ticks generated by counter/timer 0.

The RTC/CMOS RAM's 128 locations are accessed by the 80386 microprocessor placing an address (or "index") ranging from 00h to 7Fh on data lines XD0 through XD6 and then writing these seven bits to I/O address 0070h. (Bit 7 is the non-maskable interrupt bit.) When an address strobe is applied to the IPC's Address Strobe input pin, on the falling edge of the address strobe, the address on the data input lines is latched into the RTC's internal Index Address Register. At this point, the 80386 microprocessor can access the desired location by reading from or writing to I/O address 0071h.

When the system power is off, the RTC/CMOS RAM's 32.768 crystal oscillator gets power from the system's battery, keeping track of the time and day and maintaining CMOS RAM. The battery, located on the System Interface PCA, is a 6-volt lithium battery pack with an average life of 2.3 years.

Table 3-5. Real-Time Clock/CMOS RAM Memory Map

Hex Address	Byte Type	Application
00	RTC Register *	Seconds
01	RTC Register *	Seconds alarm
02	RTC Register *	Minutes
03	RTC Register *	Minutes alarm
04	RTC Register *	Hours
05	RTC Register *	Hours alarm
06	RTC Register *	Day of Week
07	RTC Register *	Date of Month
08	RTC Register *	Month
09	RTC Register *	Year
0A	RTC Register *	Status Register A
0B	RTC Register *	Status Register B
0C	RTC Register *	Status Register C
0D	RTC Register *	Status Register D
0E	CMOS RAM Byte *	Diagnostic status byte
0F	CMOS RAM Byte *	Shutdown status byte
10	CMOS RAM Byte	Flexible disc drive type (A: and B:)
11	CMOS RAM Byte	Reserved
12	CMOS RAM Byte	Hard disc drive type (C: and D:)
13	CMOS RAM Byte	Reserved
14	CMOS RAM Byte	Equipment byte
15	CMOS RAM Byte	Low base memory byte
16	CMOS RAM Byte	High base memory byte
17	CMOS RAM Byte	Low expansion memory byte
18	CMOS RAM Byte	High expansion memory byte
19-20	CMOS RAM Bytes	Reserved
21-2D	CMOS RAM Bytes	Reserved
2E-2F	CMOS RAM Bytes	2-byte CMOS checksum
30	CMOS RAM Byte *	Low expansion memory byte
31	CMOS RAM Byte *	High expansion memory byte
32	CMOS RAM Byte *	Century date byte
33	CMOS RAM Byte *	Information flags
34-3F	CMOS RAM Bytes	Reserved
40-7F	CMOS RAM Bytes *	HP-Reserved

* Indicate bytes which are not included in the CMOS checksum calculation.

3.2.4 Counter/Timers

Counter/timers are provided to the system by the 82206 IPC's three 16-bit counters, equivalent to 8254 counter/timers.

Counter/Timer Operation

The counter/timers each operate independently, but are driven by a common clock, TMRCLK (1.19 MHz, derived from OSC4, the 14.318 MHz system timing clock, divided by 12). The minimum time resolvable is approximately 838 nanoseconds (1 input clock cycle), and the maximum time resolvable is 55 milliseconds (65,536 clock cycles).

All counter/timers have the same control logic, which decodes information written to them. The control logic also provides the controls to load, read, and configure the counter/timers, all of which are dedicated to system functions.

Timer 0 (I/O address 0040h) generates the MS-DOS real-time clock interrupt.

Counter 1 (0041h) is dedicated to system RAM refresh, and no attempt should be made to reprogram it.

Counter 2 (0042h) drives the speaker. Under program control, this counter has a gate input, bit 0 of the industry-standard Port B (0061h). Setting this bit to 0 inhibits counting action, turning the speaker off. (Because bit 1 is ANDed with this counter's output, writing a 0 to this bit also disables the speaker.)

A *control/status register* (0043h) holds mode and command information on the counter/timers and monitors counter conditions.

3.3 Keyboard and HP-HIL Circuits

The keyboard and HP-HIL (Hewlett-Packard Human Interface Link) circuits consist of the components given in Table 3-6. Together, the 8042 keyboard controller, the 8042 keyboard controller port expander (an HP-proprietary gate array), and the 1RD2 HP-Human Interface Link Controller (also known as "the Master Link Controller" or MLC) control the interface to the keyboard and other input devices.

Figure 3-3 gives a block diagram of the keyboard and HP-HIL circuits. If an industry-standard keyboard is used, data from it are latched into the keyboard controller, which instructs the 80386 microprocessor to read the data. On the other hand, if HP-HIL input devices are used, data are latched into the 1RD2 HP-HIL MLC, after which the 8042 port expander instructs the 80386 microprocessor to read the data.

Table 3-6. Keyboard and HP-HIL Circuit Components

Input Device Connector PCA
Industry-standard keyboard
8042 keyboard controller, for industry-standard keyboards
8042 keyboard controller port expander gate array
1RD2 HP-HIL Master Link Controller for HP-HIL input devices
HP-HIL connector for HP-HIL input devices
System fan/speaker/keylock assembly

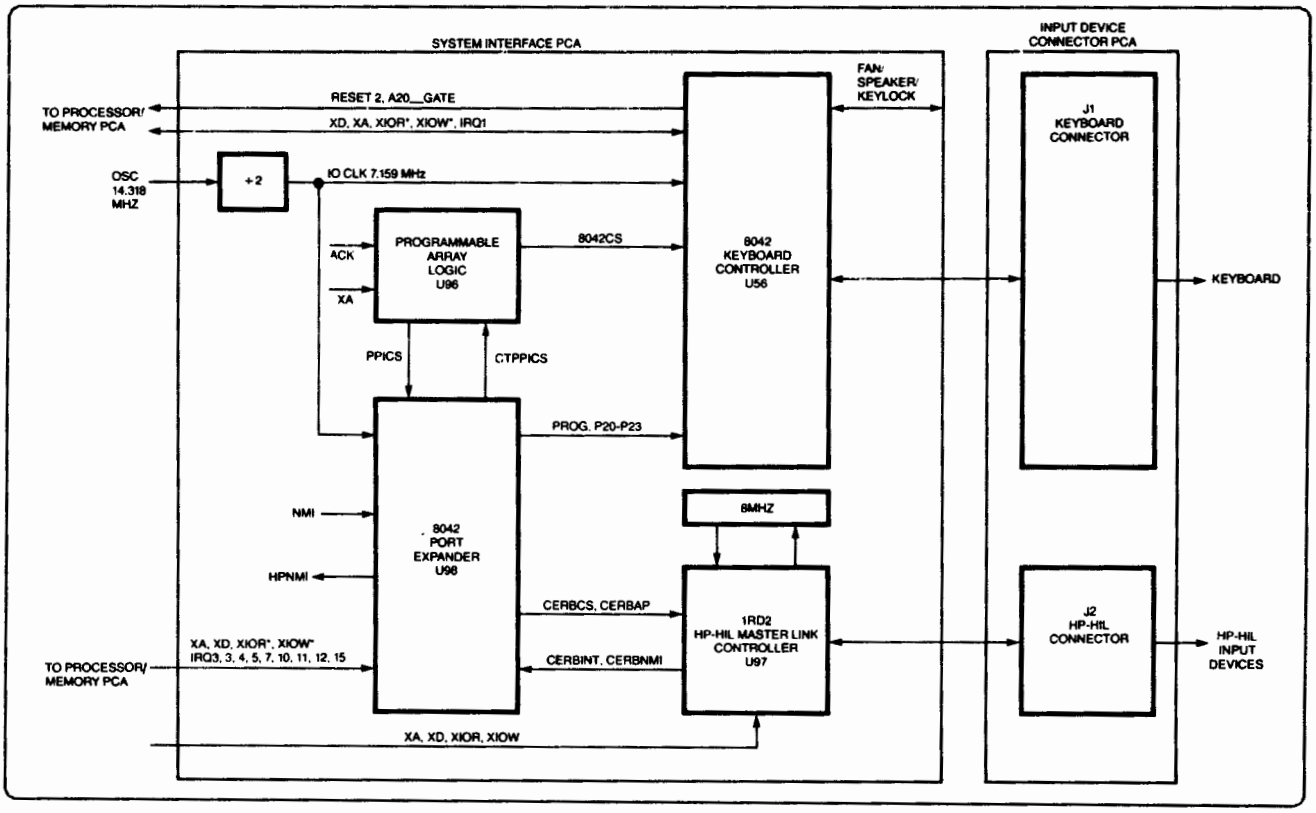


Figure 3-3. Block Diagram of Keyboard and HP-HIL Circuits

3.3.1 Input Device Connector PCA

The Input Device Connector PCA provides an interface between the System Interface PCA and input devices (either industry-standard, or Hewlett-Packard). Table 3-7 gives the major Input Device Connector PCA components, and Figure 3-4 gives the board's component layout. (The schematic for the Input Device Connector PCA is given at the end of the chapter.)

Figure 3-5 gives the Input Device Connector PCA's pin assignments. As shown in Figure 3-5, the Input Device Connector PCA fits into the System Interface PCA's J2 I/O connector slot. The Input Device Connector PCA's industry-standard keyboard DIN connector (J1) provides the interface for keyboard clock and data I/O signals that pass between an industry-standard keyboard and the System Interface PCA. The Input Device Connector PCA's HP-HIL connector (J2) provides the interface for I/O signals that pass between HP-HIL input devices and the System Interface PCA.

Table 3-7. Major Input Device Connector PCA Components

1 card-edge connector to System Interface PCA (J3)
2 fuses rated at 3 Amps, 125 Volts (F1, F2)
1 HP-HIL-E connector for HP-HIL input devices (J2)
1 industry-standard 5-pin keyboard DIN connector (J1)
1 74ALS1035 non-inverting driver (U1)

*Fuses are not user-replaceable items.

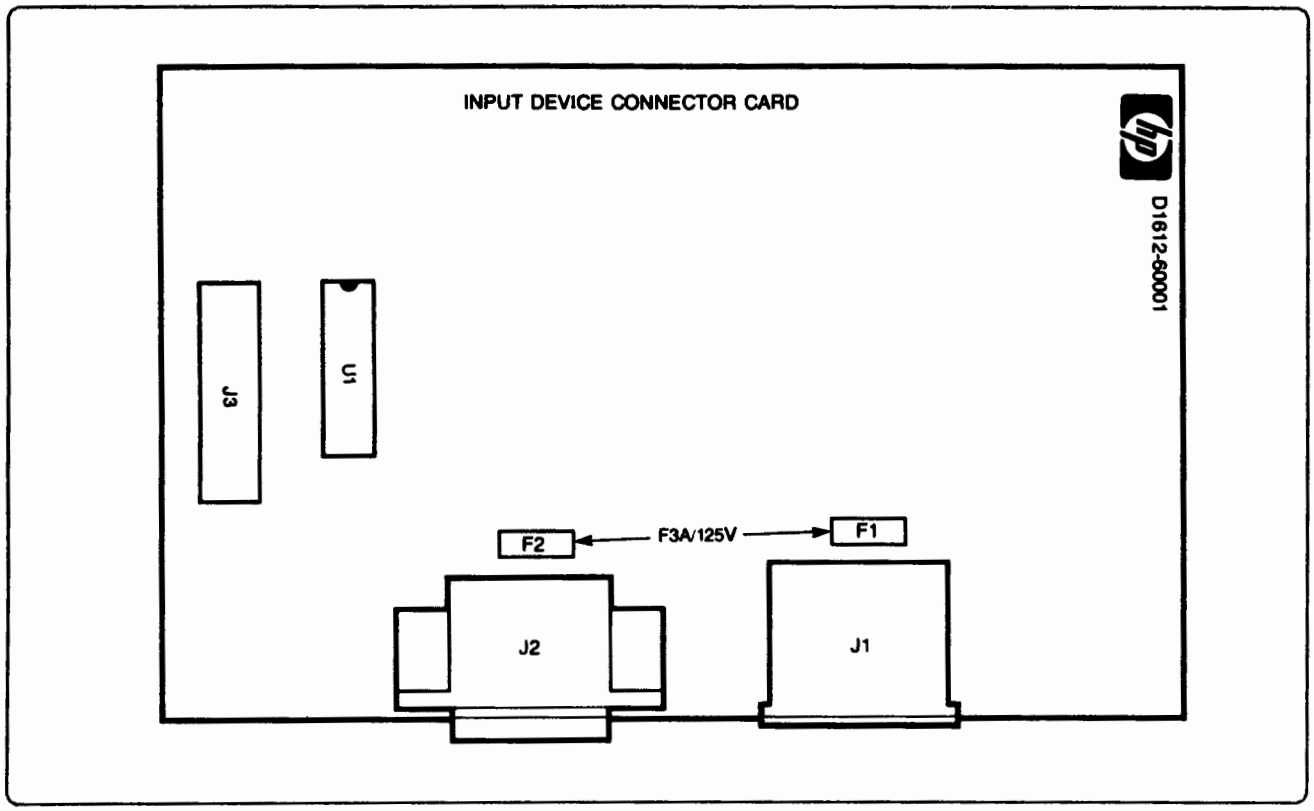


Figure 3-4. Input Device Connector PCA Component Layout

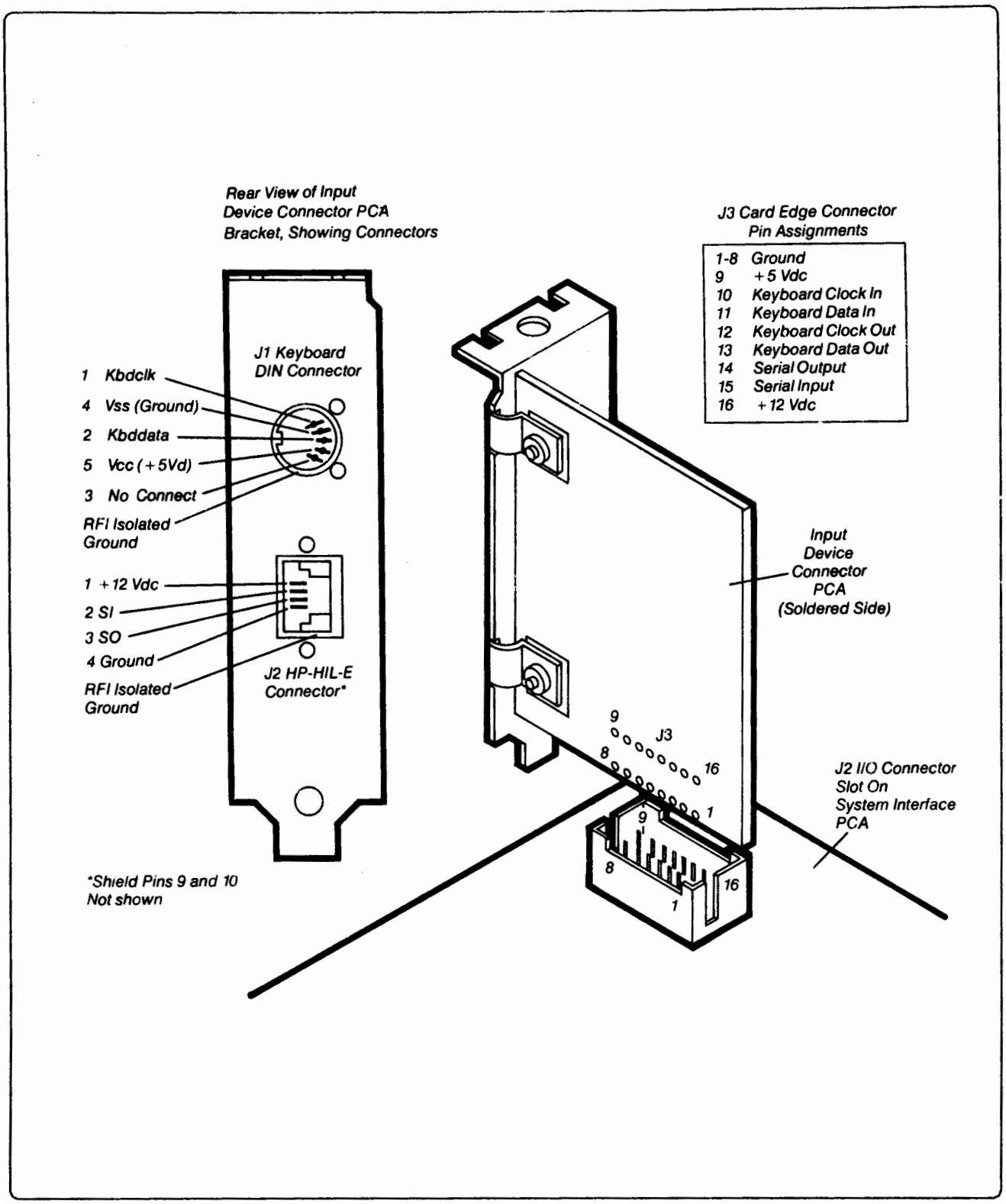


Figure 3-5. Input Device Connector PCA Pin Assignments

3.3.2 Keyboard

The keyboard for the Vectra RS is the industry-standard "HP Vectra Enhanced Keyboard." Figure 3-6 shows the U.S. 101-key version and identifies its reference numbers.

Depending on which of the keyboard keys are pressed, data from the keyboard to the system are sent via the series of hex scan codes shown in Table 3-8. Commands sent from the system to the keyboard are listed and defined in Table 3-9. Codes and commands sent from the keyboard to the system are listed and defined in Table 3-10.

For more information on the keyboard operation and on data and commands sent between the keyboard and the system, refer to the "Keyboard" chapter of the *HP Vectra Accessories Technical Reference Manual*. For a detailed description of the keyboard software interface, and for a more complete listing of commands sent between the keyboard and the system, refer to the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

NOTE

The HP Vectra RS also supports industry-standard international keyboards (with 102 keys), which are available through Hewlett-Packard dealers. The HP Vectra RS does not support the "Vectra PC Keyboard," a keyboard used by earlier versions of HP Vectras.

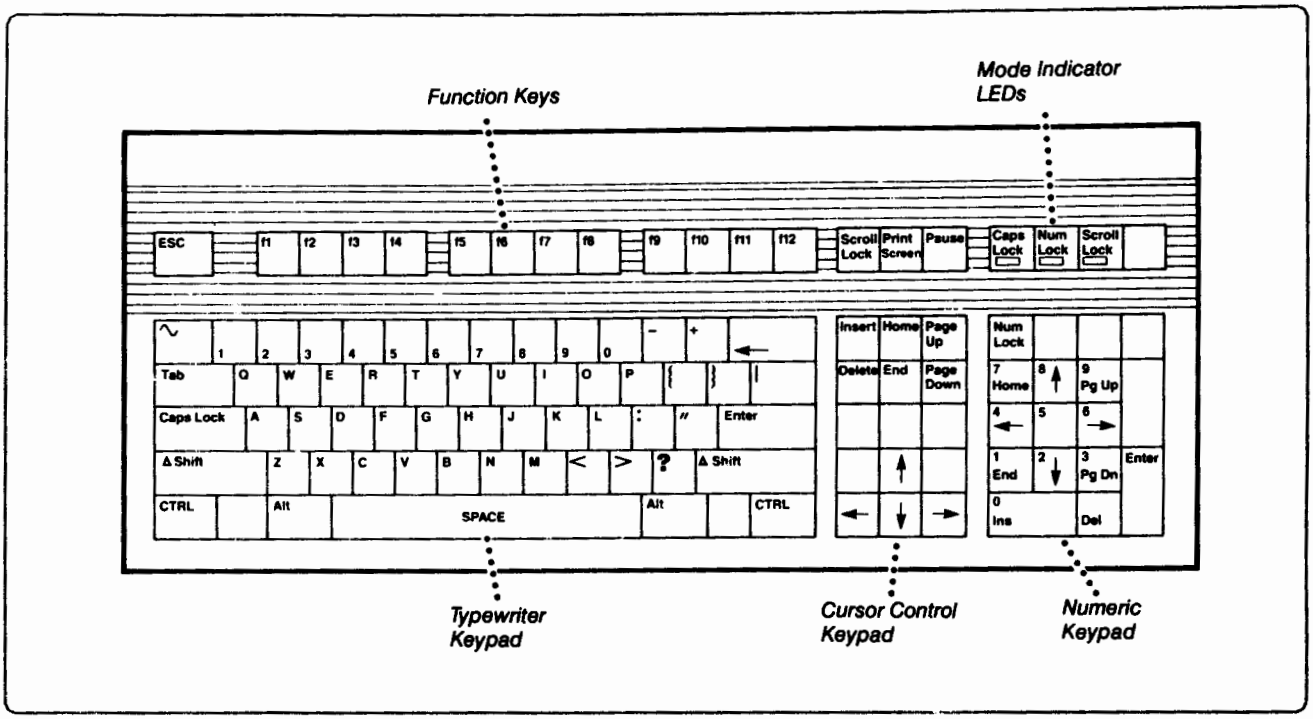


Figure 3-6 (a). HP Vectra Enhanced Keyboard (United States)

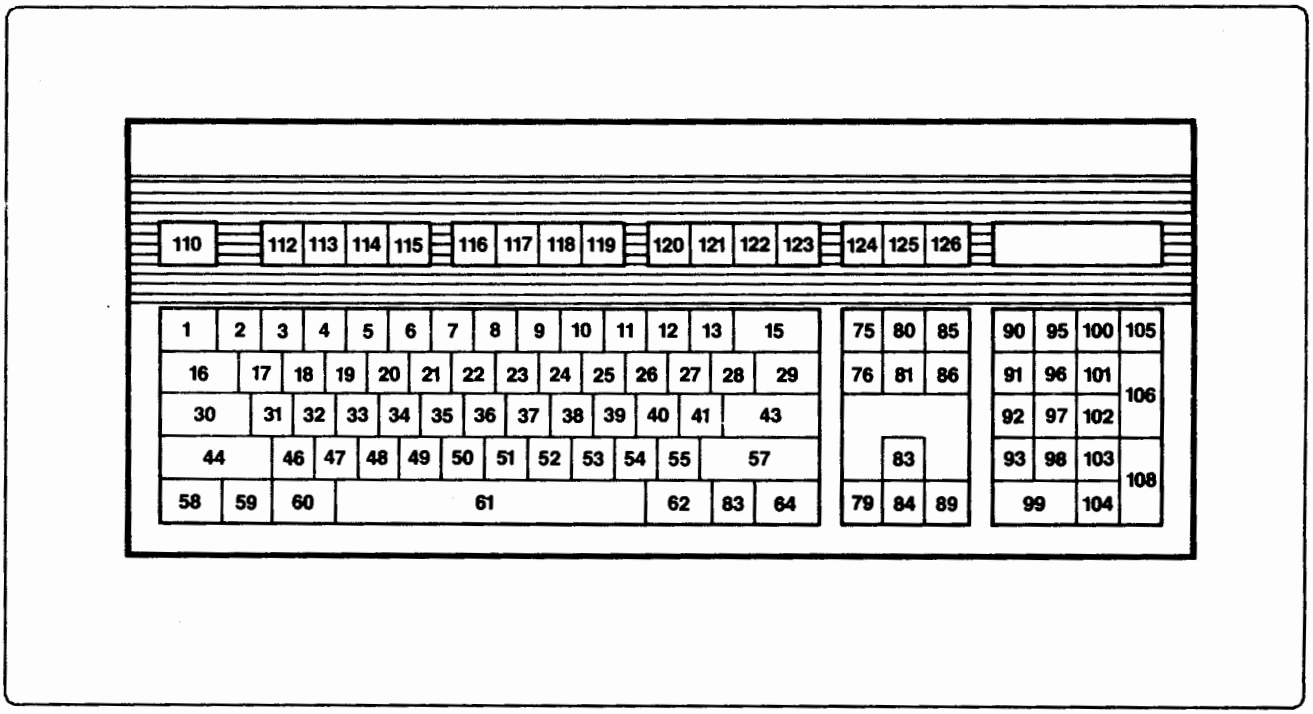


Figure 3-6 (b). Keyboard Reference Numbers

Table 3-8 (a). Keyboard Hex Scan Codes

Key No.	Make Code	Break Code	Key No.	Make Code	Break Code
1	0E	F0 0E	41	52	F0 52
2	16	F0 16	42 **	5D	F0 5D
3	1E	F0 1E	43	5A	F0 5A
4	26	F0 26	44	12	F0 12
5	25	F0 25	45 **	61	F0 61
6	2E	F0 2E	46	1A	F0 1A
7	36	F0 36	47	22	F0 22
8	3D	F0 3D	48	21	F0 21
9	3E	F0 3E	49	2A	F0 2A
10	46	F0 46	50	32	F0 32
11	45	F0 45	51	31	F0 31
12	4E	F0 4E	52	3A	F0 3A
13	55	F0 55	53	41	F0 41
14 #	–	– –	54	49	F0 49
15	66	F0 66	55	4A	F0 4A
16	0D	F0 0D	56 #	–	– –
17	15	F0 15	57	59	F0 59
18	1D	F0 1D	58	14	F0 14
19	24	F0 24	59 ***	5E	F0 5E
20	2D	F0 2D	60	11	F0 11
21	2C	F0 2C	61	29	F0 29
22	35	F0 35	62	E0 11	F0 11
23	3C	F0 3C	63 ***	5F	F0 5E
24	43	F0 43	64	E0 14	E0 F0 14
25	44	F0 44	65 #	– –	– –
26	4D	F0 4D	66 #	– –	– –
27	54	F0 54	67-74 #	– –	– –
28	5B	F0 5B	75	Note (1)	Note (1)
29 *	5D	F0 5D	76-89	Note (1)	Note (1)
30	58	F0 58	90	77	F0 77
31	1C	F0 1C	91	6C	F0 6C
32	1B	F0 1B	92	6B	F0 6B
33	23	F0 23	93	69	F0 69
34	2B	F0 2B	94 #	–	– –
35	34	F0 34	95	Note (2)	Note (2)
36	33	F0 33	96	75	F0 75
37	3B	F0 3B	97	73	F0 73
38	42	F0 42	98	72	F0 72
39	4B	F0 4B	99	70	F0 70
40	4C	F0 4C	100	7C	F0 7C

* 101-key keyboard only. (U.S.)
** 102-key keyboard only.
*** Asian keyboard only.

Not a referenced key number.
(1) See Table 3-8 (b)
(2) See Table 3-8 (c)

Table 3-8 (a). Keyboard Hex Scan Codes

Key No.	Make Code	Break Code	Key No.	Make Code	Break Code
101	7D	F0 7D	114	04	F0 04
102	74	F0 74	115	0C	F0 0C
103	7A	F0 7A	116	03	F0 03
104	71	F0 71	117	0B	F0 0B
105	7B	F0 7B	118	83	F0 83
106	79	F0 79	119	0A	F0 0A
107 #	–	-- --	120	01	F0 01
108	E0 5A	E0 F0 5A	121	09	F0 09
109 #	–	-- --	122	78	F0 78
110	76	F0 76	123	07	F0 07
111 #	–	-- --	124	Note (3)	Note (3)
112	05	F0 05	125	7E	F0 7E
113	06	F0 06	126	Note (4)	Note (4)

Not a referenced key number
(3) See Table 3-8 (d)
(4) See Table 3-8 (e)

Table 3-8 (b). Keyboard Hex Scan Codes

Key No./Code	Base Case *	Shift Case **	Num Lock On
75/Make Code	E0 70	E0 F0 12 E0 70	E0 12 E0 70
/Break Code	E0 F0 70	E0 F0 70 E0 12	E0 F0 70 E0 F0 12
76/Make Code	E0 71	E0 F0 12 E0 71	E0 12 E0 71
/Break Code	E0 F0 71	E0 F0 71 E0 12	E0 F0 71 E0 F0 12
77, 78 #			
79/Make Code	E0 6B	E0 F0 12 E0 6B	E0 12 E0 6B
/Break Code	E0 F0 6B	E0 F0 6B E0 12	E0 F0 6B E0 F0 12
80/Make Code	E0 6C	E0 F0 12 E0 6C	E0 12 E0 6C
/Break Code	E0 F0 6C	E0 F0 6C E0 12	E0 F0 6C E0 F0 12
81/Make Code	E0 69	E0 F0 12 E0 69	E0 12 E0 69
/Break Code	E0 F0 69	E0 F0 69 E0 12	E0 F0 69 E0 F0 12
82 #			
83/Make Code	E0 75	E0 F0 12 E0 75	E0 12 E0 75
/Break Code	E0 F0 75	E0 F0 75 E0 12	E0 F0 75 E0 F0 12
84/Make Code	E0 72	E0 F0 12 E0 72	E0 12 E0 72
/Break Code	E0 F0 72	E0 F0 72 E0 12	E0 F0 72 E0 F0 12
85/Make Code	E0 7D	E0 F0 12 E0 7D	E0 12 E0 7D
/Break Code	E0 F0 7D	E0 F0 7D E0 12	E0 F0 7D E0 F0 12
86/Make Code	E0 7A	E0 F0 12 E0 7A	E0 12 E0 7A
/Break Code	E0 F0 7A	E0 F0 7A E0 12	E0 F0 7A E0 F0 12
87, 88 #			
89/Make Code	E0 74	E0 F0 12 E0 74	E0 12 E0 74
/Break Code	E0 F0 74	E0 F0 74 E0 12	E0 F0 74 E0 F0 12

Not a referenced key number.
* Also applies to when <Shift> and <Num Lock> keys are held down.
** The F0 12/12 shift make and break codes are sent with the other scan codes if the left <Shift> key is held down. If the right <Shift> key is held down, then the F0 59/59 shift make and break codes are sent. Both sets of make and break codes are sent with the other scan codes if both <Shift> keys are held down.

Table 3-8 (c). Keyboard Hex Scan Codes

Key No./Code	Scan Code	Shift Case*
95/Make Code /Break Code	E0 4A E0 F0 4A	E0 F0 12 4A E0 12 F0 4A

* The F0 12/12 shift make and break code is sent with the other scan codes if the left <Shift> key is held down. If the right <Shift> key is held down, then the F0 59/59 shift make and break codes are sent. Both sets of make and break codes are sent with the other scan codes if both <Shift> keys are held down.

Table 3-8 (d). Keyboard Hex Scan Codes

Key No./Code	Scan Code	Ctrl, Shift Case	Alt Case
124/Make Code /Break Code	E0 12 E0 7C E0 F0 7C E0 F0 12	E0 7C E0 F0 7C	84 F0 84

Table 3-8 (e). Keyboard Hex Scan Codes

Key No.	Make Code	Ctrl Key Pressed
126**	E1 14 77 E1 F0 14 F0 77	E0 7E E0 F0 7E

** Not a typematic key. All associated scan codes occur on the key's make code.

Table 3-9. Commands Sent by System to Keyboard

Command	Definition
EDh - Set/Reset Mode Indicators	This command, in conjunction with an option byte that immediately follows it, toggles the keyboard's three mode-indicator LEDs, turning them on and off. Bits 7 through 3 of this option byte are not used, and should be set to 0. Bit 2 controls the <Caps lock> mode indicator, bit 1 controls the <Num lock> mode indicator, and bit 0 controls the <Scroll lock> mode indicator. Setting the respective bits to 1 turns a mode indicator on, while a 0 turns it off.
EEh - Echo	This command is a diagnostic aid. When the system issues this command to the keyboard, the keyboard responds by sending to the system its own Echo command (EEh).
EFh - No Operation	This command is reserved. The system sends this command to the keyboard, which acknowledges receiving the command, but takes no action.
F0h - Select Alternate Scan Codes	This command, in conjunction with an option byte that immediately follows it, instructs the keyboard to select one of three sets of scan codes. When the keyboard receives this command, it clears its output buffer and the typematic key (if one is active). The system then sends an option byte to select the appropriate scan code set: 01h selects set 1, 02h selects set 2, and 03h selects set 3.
F1h - No Operation	This command is reserved. The system sends this command to the keyboard, which acknowledges receiving the command, but takes no action.
F2h - Request Keyboard Identification Information	This command instructs the keyboard to discontinue sending scan codes and to send two keyboard identification bytes. After the first identification byte, the second byte must follow by 500 microseconds or less, after which the keyboard resumes sending scan codes.
F3h - Set Typematic Delay/ Rate	This command, in conjunction with a parameter byte that immediately follows it, alters the keyboard's typematic delay and rate. Bit 7 of this parameter byte is always zero. Bits 6 and 5 alter the delay parameters, and bits 4, 3, 2, 1 and 0 alter the rate parameters.
F4h - Enable	This command enables the keyboard to send scan codes if the transmission of scan codes had been halted.
F5h - Default Disable	This command resets all keyboard parameters to the power-on default state and stops the keyboard from sending scan codes.
F6h - Set Default	This command resets all keyboard parameters to the power-on default state, after which the keyboard sends scan codes.

Table 3-9. Commands Sent by System to Keyboard

Command	Definition
F7h - Set All Keys Typematic	This command clears the keyboard's output buffers. The keyboard then sets all keys to typematic, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.
F8h - Set All Keys Make/Break	This command clears the keyboard's output buffers. The keyboard sets all keys to make/break, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.
F9h - Set All Keys Make	This command clears the keyboard's output buffers. The keyboard sets all keys to make, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.
FAh - Set All Keys Typematic/ Make/Break	This command clears the keyboard's output buffers. The keyboard sets all keys to typematic/make/break, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.
FBh - Set Key Typematic	This command clears the keyboard's output buffers so the keyboard may receive the key identification. The system identifies each key by its scan code set 3 value. Each identified key is set to typematic.
FCh - Set Key Make/ Break	This command clears the keyboard's output buffers so the keyboard may receive the key identification. The system identifies each key by its scan code set 3 value. Each identified key is set to make/break.
FDh - Set Key Make	This command clears the keyboard's output buffers so the keyboard may receive the key identification. The system identifies each key by its scan code set 3 value. Each identified key is set to make.
FEh - Resend	This command, sent by the system's 8042 keyboard controller when it detects an error in data coming from the keyboard, tells the keyboard to resend the last data.
FFh - Reset	This command performs the keyboard's Power-On Reset function. This step takes at least 300 milliseconds, during which time the keyboard is disabled.

Table 3-10. Codes/Commands Sent by Keyboard to System

Command	Definition
00h - Overrun	This character code is placed in position 17 of the keyboard buffer, overlaying the last of the code when the keyboard buffer is full.
AAh - Completion Code	This code is sent after the keyboard has passed its self-test. Any other code tells the system that the keyboard has failed its self-test.
EEh - Echo	This command is a diagnostic aid. After the system has issued its Echo command to the keyboard, the keyboard responds by sending to the system its own Echo command (EEh) and scan codes, if the keyboard has been previously enabled.
F0h - Break Code Prefix	This code is sent when a key is released. The code consists of a two-byte hex prefix, F0, followed by the make code for the released key.
FAh - Acknowledge	This command is sent to the system by the keyboard to acknowledge it has received valid input from the system. The keyboard does not send this command when it receives from the system either an Echo command (EEh) or a Resend command (FEh). If, while the keyboard is sending the acknowledge command, the system interrupts the keyboard with a command, the keyboard discards the acknowledge command. If the new command is recognized, the keyboard accepts the system's new command and processes it. If the command is not recognized, the keyboard sends a Resend command (FEh) to the system.
FCh - Diagnostic Failure	This command is sent if the keyboard detects a malfunction. If the malfunction occurs during the keyboard self-test, the keyboard will stop and wait for a system command or a power-down.
FEh - Resend	This command is sent when the keyboard receives from the system either invalid input, or input with incorrect parity.

3.3.3 Keyboard Controller

The keyboard controller, an 8042 microprocessor, is programmed to provide an interface between the 80386 microprocessor and an industry-standard keyboard, HP-HIL input devices, and the computer's speaker. More specifically, the keyboard controller provides the following:

1. interfaces to the 80386 microprocessor, including logical paths to the 80386 microprocessor and system reboot
2. a communication path between HP-HIL input devices and the computer's BIOS and/or the computer's application programs
3. three output lines and one input line

Keyboard Controller Operation

1. Interface to 80386 Microprocessor

a. Logical path from 8042 Keyboard Controller to 80386 Microprocessor

The *application path*, a direct logic path from the 8042 keyboard controller to the 80386 microprocessor, consists of two 80386 read/write registers and an interrupt line. The first 80386 read/write register, at I/O address 60h, is used for keyboard commands and data, and for keyboard controller data. The second 80386 read/write register, at I/O address 64h, is used to write commands to, and read the status of, the keyboard controller. The output buffer interrupt line (OBFINT) is set to interrupt the 80386 when the keyboard controller places data in the 80386 microprocessor's read register at I/O address 60h.

b. System Reboot

By writing FEh to I/O port 64, RESET2* goes low, activating the 82301 bus controller's RESET3, which resets the 80386 microprocessor and the coprocessor(s), if the 80387 and/or the 1167 coprocessors are installed.

Through its A20_GATE signal, the keyboard controller can also be used to extend the 80386 microprocessor's real-address operating mode, which is limited to 1 Mbyte. When high, A20_GATE enables the 80386 microprocessor's address line A20, extending the 80386's real-address operating mode. When low, A20_GATE forces the 80386 microprocessor's address line A20 to a logical 0.

* Active low.

2. Industry-Standard Keyboard Interface (Clock and Data Signals)

Via the signals KBDCLK (keyboard clock) and KBDDIN (keyboard data in), the 8042 keyboard controller sends clock reference signals and data (commands or status) to the industry-standard keyboard. In return, the keyboard sends to the keyboard controller a clock reference signal, KBDCLKOUT (keyboard clock out) and KBDDOUT (keyboard data out). Each time the user presses or releases a key, the keyboard sends a corresponding 11-bit scan code to the 8042 keyboard controller, in the format shown in Table 3-11. By writing the scan code to its output buffer, the keyboard controller sends the scan code to the 80386 microprocessor, which causes an interrupt of the 80386 (IRQ1). The 80386 then reads the scan code from I/O address 60h.

Table 3-11. Keyboard Scan Code Data Transmission Format

Bit	Definition
1	Start bit (always 1)
2	Data bit 0 (least-significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most-significant bit)
10	Parity bit* (0 or 1)
11	Stop bit (always 1)

* The eight data bits, plus the parity bit, always equal an odd number.

3. HP-HIL Input Device Interface

When, via the HP-HIL connector, an HP-HIL input device sends an input to the 1RD2 HP-HIL MLC, this controller sends an interrupt (CERBINT*) to the 8042 port expander. The 8042 keyboard controller reads this and in turn, generates an interrupt (HPINT) to the 80386 microprocessor. When the 80386 checks the source of the interrupt by reading I/O port 65, and if bits 5 and 4 are zero, then the 80386 reads data from the 1RD2 HP-HIL MLC. (For more information on the HP-HIL interface, refer to the section "HP-HIL" in this chapter.)

4. Speaker Interface

Each time the keyboard controller receives a keyboard character from the industry-standard keyboard, the keyboard controller sends a keyboard click signal (KBCLICK) to the computer's speaker.

5. Keyboard Inhibit Switch Interface

The keyboard controller monitors the keyboard inhibit (KBINH) input line, which comes from the keyboard inhibit keylock switch. When the user turns this SPU front-panel switch to the lock position, the KBINH signal is set to 0. In this case, data from the keyboard are still returned to the keyboard controller, but not sent to the 80386 microprocessor.

3.3.4 Keyboard Controller Port Expander

The 8042 keyboard controller port expander, a Hewlett-Packard proprietary CMOS standard cell chip packaged in a 44-pin plastic-leaded chip carrier, can select one of eight general-purpose I/O interrupts. The 8042 port expander also provides HP-specific keyboard controller functions, as well as extensions for the 8042 keyboard controller's ports. In addition, in conjunction with the 8042 keyboard controller, the 8042 port expander provides the auto-polling frequency and address decoding for the 1RD2 HP-HIL MLC. Pin assignments for the 8042 port expander are described in Table 3-12.

Table 3-12. 8042 Port Expander Pin Assignments

Pin No.	I/O/Power	Pin Name	Pin Definition
1	Ground	GND	Ground
2	Out	CERBAP	Auto-poll frequency for the 1RD2 HP-HIL MLC
3	In	PROG	Program code (keyboard controller address/data strobe)
4-7	I/O Tri-State	P23-P20	Port address and data pins for keyboard controller
8-11	Out Tri-State	IRQ A,C,E,G	Interrupt request pins for backplane I/O channel interrupts 3, 5, 10, 12
12	In with pull-up	CERBINT*	Interrupt pin for 1RD2 HP-HIL MLC
13	In with pull-up	CERBNMI*	Non-maskable interrupt pin for 1RD2 HP-HIL MLC
14-18	In	XA0 to XA4	Peripheral address bus bits 0 to 4
19-22	I/O Tri-State	XD0 to XD3	Peripheral data bus bits 0 to 3
23	Ground	GND	Ground
24-27	I/O	XD7 to XD4	Peripheral data bus bits 7 to 4
28-29	Out	Reserved	Reserved

* Active low.

Table 3-12. 8042 Port Expander Pin Assignments (Continued)

Pin No.	I/O/Power	Pin Name	Pin Definition
30	In	PPICS*	Programmable Peripheral Interface Chip Select
31	Out	CTPPICS*	Custom Task Programmable Peripheral Interface Chip Select
32	In with pull-up	Reserved	Reserved
33	In	IOCLK	Clock input pin
34	In	RESET*	Reset signal
35	Power	VDD	Power pin
36-39	Out Tri-State	IRQ B,D,F,H	Interrupt request pins for backplane I/O channel interrupts 4, 7, 11, 15
40	In	XIOW*	I/O write
41	In	XIOR*	I/O read
42	Out	CERBCS*	1RD2 HP-HIL MLC Chip Select
43	Out	HPNMI	HP non-maskable interrupt
44	In	NMI	Non-maskable interrupt

* Active low.

3.3.5 HP-HIL

The HP-HIL (Hewlett-Packard Human Interface Link) is a Hewlett-Packard proprietary four-wire asynchronous serial interface comprised of: (1) the HP-HIL controller (also known as the Hewlett-Packard 1RD2 HP-HIL MLC), an n-channel metal-oxide semiconductor integrated circuit in a 24-pin dual in-line package and (2) the HP-HIL connector, a shielded 4-pin connector.

The HP-HIL acts as the HP standard interface between the system processing unit and up to seven Hewlett-Packard HIL input devices. An overview of the HP-HIL operation is given below. (For more information, refer to the *HP-HIL Technical Reference Manual.*)

HP-HIL Operation

The HP-HIL enables the user to connect input devices to the SPU by "daisy-chaining" them; i.e., the first input device is plugged into the SPU, the second input device is plugged into the first input device, etc.

NOTE

The keyboard used with the Vectra RS, the HP Vectra Enhanced Keyboard, is not an HP-HIL input device and is not connected to the HP-HIL connector. Input devices that do connect to the HP-HIL connector are mice, graphics tablets, barcode readers, etc.

Refer to the figure in this chapter, "Block Diagram of Keyboard and HP-HIL Circuits" for a block diagram of how the HP-HIL interfaces with the 8042 port expander, the 8042 keyboard controller, and the HP-HIL input devices. Each of the HP-HIL input devices contain a Hewlett-Packard custom chip (the 1RC8 Slave Link Controller, or SLC) and a microprocessor. The 1RC8 handles all HP-HIL communication between the 1RD2 HP-HIL MLC and the microprocessor, which is programmed to handle the hardware for that particular input device.

Approximately 60 times per second, the 1RD2 HP-HIL MLC polls the HP-HIL input devices to collect data from them. If device data are returned, the HP-HIL controller generates an interrupt (CERBINT) and sends it to the 8042 port expander, which sends the interrupt to the 8042 keyboard controller. The keyboard controller recognizes this interrupt and in turn, makes the 8042 port expander generate an interrupt to the 80386 microprocessor (HPINT). The keyboard controller also writes data into the 8042 port expander, signalling that the interrupt is from the 1RD2 HP-HIL MLC. The 80386 is interrupted, recognizes the source of the interrupt, and reads the data from the HP-HIL MLC.

The SPU power supply provides +12 Vdc for the HP-HIL input devices. Each HP-HIL input device internally regulates the +12 Vdc input to +5 Vdc and typically requires 100 mA.

1. 1RD2 HP-HIL Master Link Controller

The 1RD2 HP-HIL Master Link Controller (MLC) interfaces the 80386 microprocessor to HP-HIL input devices, via the HP-HIL connector. The 1RD2 HP-HIL MLC accepts commands from the 80386 and transmits them to the HP-HIL input devices in a fixed format called a "frame." Each frame consists of 15 bits of serial information, including start, stop, command, parity, address, and data bits. Using this same format, the 1RD2 HP-HIL MLC also receives serial data from input devices and relays the data to the 80386 microprocessor. The 1RD2 HP-HIL MLC pin assignments are given in Table 3-13.

Table 3-13. 1RD2 HP-HIL Master Link Controller Pin Assignments

Pin No.	I/O/Power	Pin Name	Pin Definition
1	Out	NMI	Non-Maskable Interrupt
2	Out	INT	Interrupt
3	Power	VDD	+5 V power pin
4	I/O	D0	Data I/O <0>
5	I/O	D1	Data I/O <1>
6	I/O	D2	Data I/O <2>
7	I/O	D3	Data I/O <3>
8	I/O	D4	Data I/O <4>
9	I/O	D5	Data I/O <5>
10	I/O	D6	Data I/O <6>
11	I/O	D7	Data I/O <7>
12	Ground	MOT	Reserved
13	In	A1	Address <1>
14	In	A0	Address <0>
15	In	NRD	Not Read Enable
16	In	NCS	Not Chip Select
17	In	NWR	Not Write Enable
18	Out	SO	Serial data output, HP-HIL
19	In	SI	Serial data input, HP-HIL
20	Ground	GND	Ground
21	In	PON	Power On reset input (active low)
22	In	AP	Auto Poll input (rising edge)
23	Out	CLKO	Oscillator Clock Output
24	In	CLKI	Oscillator Clock Input

2. HP-HIL Connector

The pinout for the HP-HIL connector (J2), which is located on the Input Device Connector PCA, is given in the "Input Device Connector PCA" section. The HP-HIL connector pin assignments are given in Table 3-14.

Table 3-14. HP-HIL Connector Pin Assignments

Pin No.	I/O/Power	Pin Name	Pin Definition
1	Power	VDD	+12 Vdc power pin
2	Input	SI	Serial data HP-HIL input signal
3	Output	SO	Serial data HP-HIL output signal
4	Ground	GND	Ground
9, 10	Shield	SHLD	Path to system for electro-static discharge

3.3.6 System Fan/Speaker/Keylock Assembly

The system fan/speaker/keylock assembly is connected to the system via the System Interface PCA's J3 connector slot. The system fan provides forced convection cooling for the accessory cards and the system printed circuit assemblies. The 2.25-inch, permanent-magnetic speaker for the sound signal is driven by (1) speaker data from the 82301 bus controller, and/or (2) the TRMOUT2 signal from the 82206 Integrated Peripheral Controller, or (3) the 8042 keyboard controller KBCLICK signal. (For more information on the speaker, refer to the "Counter/Timers" section in this chapter.) The keylock, located on the SPU front panel, prevents input from the keyboard and HP-HIL input devices. Table 3-15 gives the pin assignments for the J3 connector for the system fan/speaker/keylock assembly.

Table 3-15. System Fan/Speaker/Keylock Assembly Connector Slot Pin Assignments

Pin No.	Pin Definition
1	System fan voltage (+12 Vdc)
2	Ground
3	No connect
4	Voltage for SPU front panel "ON" light (+5 Vdc)
5	Ground
6	Speaker data
7	Speaker voltage (+5 Vdc)
8	Keylock for keyboard inhibit
9	Ground

3.4 Read-Only Memory

3.4.1 BIOS ROM

BIOS, the basic input/output system, is a collection of standardized routines controlling transfer of characters between the 80386 microprocessor, memory, and such I/O devices as the disc drives, keyboard, monitor, and printer. The BIOS ROM components, which contain the firmware comprising the BIOS memory, increase the BIOS's utilization of I/O devices and optimize the I/O devices' response time.

The HP Vectra RS BIOS ROM components, located on the System Interface PCA, include two 32-Kbyte 27256 EPROMs, for 64 Kbytes of ROM. The EPROM socketed in XU102 (ROM0) is for even-byte data, and the EPROM socketed in XU109 (ROM1) is for odd-byte data. The BIOS ROMs, addressable from hex 000F 0000 to 000F FFFF, are also addressable from hex 00FF 0000 to 00FF FFFF and hex 0FFF F000 to FFFF FFFF.

The physical BIOS ROM components which make up the ROM BIOS logic contain both Standard BIOS (STD-BIOS) and Extended BIOS (EX-BIOS) firmware. STD-BIOS supports the industry-standard BIOS, while EX-BIOS supports a BIOS unique to Hewlett-Packard computers.

ROM BIOS = STD-BIOS + EX-BIOS

BIOS ROM Operation

The HP Vectra RS system memory has locations for the following:

1. ROM BIOS. ROM BIOS memory locations consist of the the STD-BIOS and EX-BIOS interrupt vectors, and data areas loaded into system RAM upon power-up.

2. STD-BIOS. Memory locations for the STD-BIOS data area, the STD-BIOS data expansion area, and the STD-BIOS temporary MS-DOS buffers, all support the industry-standard set of BIOS functions.

3. EX-BIOS. Memory locations for the EX-BIOS data area support those functions unique to HP peripherals.

   (For general memory locations, refer to Chapter 2's "HP Vectra RS Memory Map" and this chapter's "Interrupt Map" table. For details on the BIOS contents, refer to the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*)

Upon power-up, the 80386 microprocessor addresses the system memory at hex address 000F FFF0, the location for part of the BIOS ROM component's software, and executes a series of instructions at this address. These instructions load from the BIOS ROM components, into the system RAM: (1)the ROM BIOS interrupt vectors, (2)ROM BIOS data areas, and (3)certain ROM BIOS functions.

ROM BIOS software components

ROM BIOS software components include interrupt vectors, drivers, and data areas.

1. Interrupt Vectors

An interrupt occurs when the 80386 microprocessor disrupts a routine's normal operation. As defined by the 80386's interrupt structure, each interrupt has an associated interrupt vector. The 80386's interrupt structure supports 256 interrupt vectors, which occupy the first 1024 bytes of system memory from hex address 0000 0000 to 0000 03FF. (For the interrupt vector assignments, refer to the table in this chapter, "Interrupt Map.")

Each interrupt vector consists of two words (four bytes). Each interrupt vector contains the code segment and instruction pointer for the interrupt's service routine. Unused interrupt vectors point to a null routine in the ROM BIOS, which, when required, issues an end-of-interrupt signal to the 82206 Integrated Peripheral Controller and returns. The following interface interrupts require interrupt vectors:

1. Hardware interrupts that indicate a system hardware component or an I/O device requires service.

2. Interrupts of the 80386 microprocessor, which indicate (1)the system software requires recovery from an error condition and (2)other hardware exceptions.

3. Software interrupts (generated by programming and mapped to the same interrupt vectors used for interrupts of the hardware and the 80386 microprocessor), that simulate these interrupts.

2. ROM BIOS Drivers

The ROM BIOS drivers consist of STD-BIOS drivers (which support industry-standard BIOS functions) and EX-BIOS drivers (which support extended BIOS functions and subfunctions unique to Hewlett-Packard computers). Drivers require system RAM data to support one or more application functions (and, in some cases, subfunctions) for performing specific tasks. The ROM BIOS functions perform specific tasks when an application accesses a driver. (For more information on drivers, refer to the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*)

3. Data Areas

To perform their functions, ROM BIOS drivers may require data from either STD-BIOS data areas or EX-BIOS data areas. The data areas provide the means for the ROM BIOS drivers to maintain driver variables, data buffers, etc. The drivers differ in the way they handle data. (For more information, refer to the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*)

3.4.2 Option ROM

The System Interface PCA has two sockets which accept 32-Kbyte option ROM chips: XU110 for option ROM0 and XU101 for option ROM1. If installed, the option ROMs are automatically enabled by default. They are addressable from hex 000E 0000 to 000E FFFF, as well as from hex 00FE 0000 to 00FE FFFF and hex FFFE 0000 to FFFE FFFF. (Via optional I/O accessory cards added on the backplane I/O, up to 128 Kbytes of ROM can also be added, addressable from hex 000C 0000 to 000D FFFF.) Option ROMs can be disabled by setting the Processor/Memory PCA's Switch 1, setting 4, to the OFF position.

3.5 Backplane I/O Connector Slots

The backplane I/O connector slots connect optional industry-standard accessory cards to the HP Vectra RS system. The figure "System Interface PCA Component Layout" in the introduction to this chapter shows the location of the eight backplane I/O connector slots. (Refer to the "Processor/Memory PCA" chapter for a discussion of the backplane I/O bus.)

As shown in Table 3-16, of the eight backplane I/O connector slots, two slots are for 8-bit accessory cards only, and six slots are for 16-bit accessory cards. The slots allow for:

7 DMA channels–four 8-bit and three 16-bit, at 4 MHz
Lines for refresh of dynamic RAM
Generation of wait states
13 interrupt request channels
Control lines for I/O and memory
8-bit or 16-bit data bus
20-bit or 24-bit address bus
Industry-standard 8-MHz timing
I/O speed greater than 8-MHz if all accessory cards can run at the greater speed*

Table 3-16. Backplane I/O Connector Slots

I/O Connector (Slot No.)	Description	No. of Pins
J4 (Slot 8)	16-bit**	98
J5 (Slot 7)	8-bit	62
J6 (Slot 6)	16-bit	98
J7 (Slot 5)	16-bit	98
J8 (Slot 4)	16-bit	98
J9 (Slot 3)	16-bit	98
J10 (Slot 2)	16-bit	98
J11 (Slot 1)	8-bit	62

* Vectra RS/20, RS/20C, and RS/25C only.
** Backplane I/O connector slot for Four-Function Controller PCA, installed at factory. All other backplane I/O connector slots are available for accessory cards.

3.5.1 Pinouts and Signal Assignments for Backplane I/O Connector Slots

Figure 3-7 gives the pinout for the backplane I/O connector slots. The 62-pin slots [slots 1 and 7 (J11 and J5)] are for 8-bit accessory cards; the 98-pin slots [slots 6 through 10 (J10 through J6)] are for 16-bit accessory cards.

Table 3-17 gives the signal assignments for the backplane I/O connector slots. The 8-bit accessory cards inserted in I/O connector slot 1 (J11) or slot 7 (J5) use the "A" and "B" signal assignments shown in Figure 3-7 (a), while the 16-bit accessory cards inserted in I/O connector slots 6 through 10 (J10 through J6) use all the assigned signals. Table 3-18 describes the signal assignments.

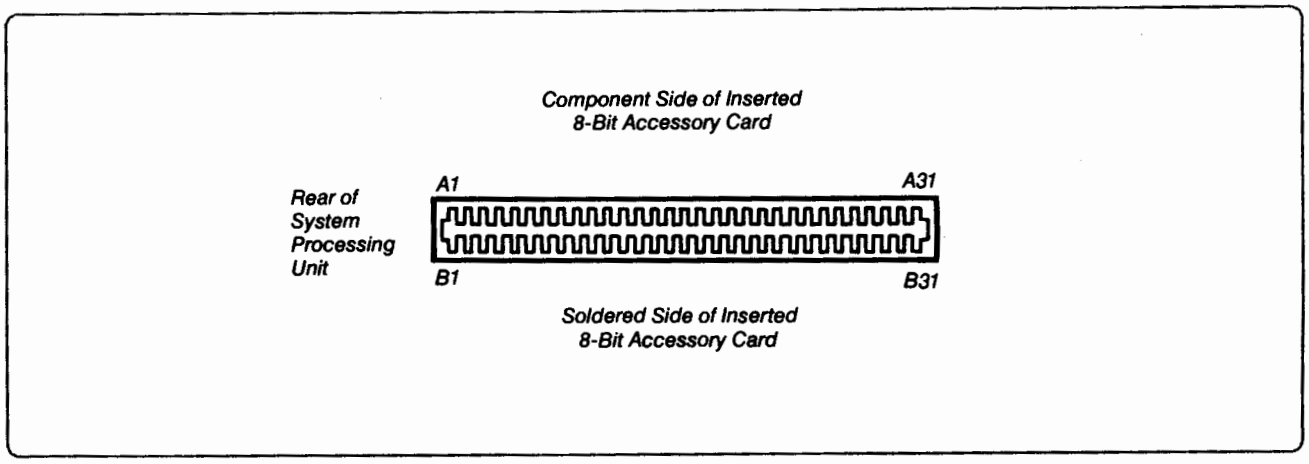


Figure 3-7 (a). 62-Pin Backplane I/O Connector Slot For 8-Bit Accessory Cards [Slot 1 (J11) and Slot 7 (J5)]

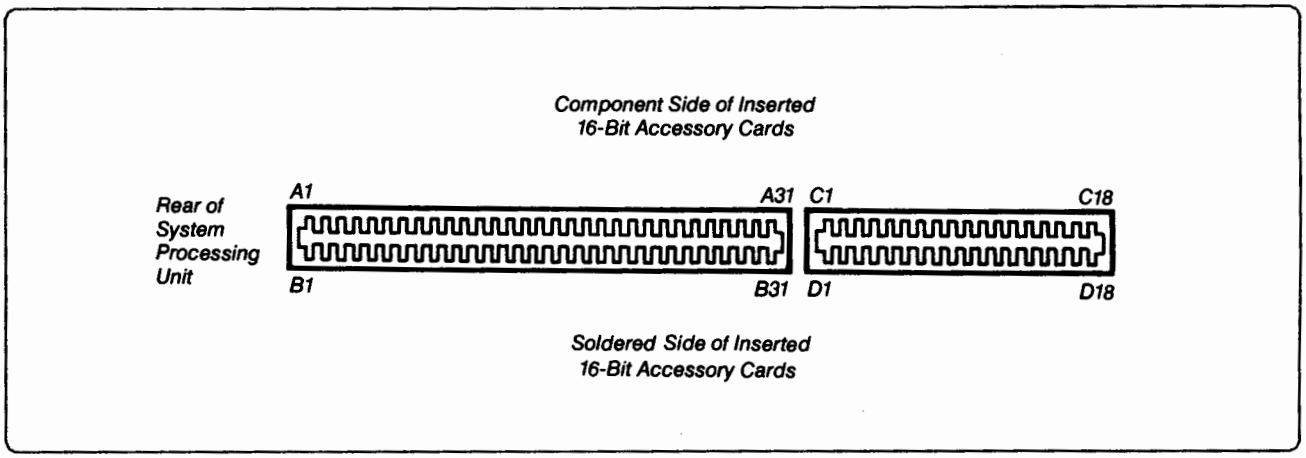


Figure 3-7 (b). 98-Pin Backplane I/O Connector Slot For 16-Bit Accessory Cards [Slots 6 through 10 (J10 through J6)]

Table 3-17. Backplane I/O Connector Slot Signal Assignments

Pin	I/O	Signal Name	Pin	I/O	Signal Name
B1	Ground	GND	A1	In	I/OCHCK*
B2	Out	RESET DRV	A2	I/O	SD7
B3	Power	+5 Vdc	A3	I/O	SD6
B4	In	IRQ9	A4	I/O	SD5
B5	Power	-5 Vdc	A5	I/O	SD4
B6	In	DREQ2	A6	I/O	SD3
B7	Power	-12 Vdc	A7	I/O	SD2
B8	In	0WS*	A8	I/O	SD1
B9	Power	+12 Vdc	A9	I/O	SD0
B10	Ground	GND	A10	In	I/OCHRDY
B11	Out	SMEMW*	A11	Out	AEN
B12	Out	SMEMR*	A12	I/O	SA19
B13	I/O	IOW*	A13	I/O	SA18
B14	I/O	IOR*	A14	I/O	SA17
B15	Out	DACK3*	A15	I/O	SA16
B16	In	DREQ3	A16	I/O	SA15
B17	Out	DACK1*	A17	I/O	SA14
B18	In	DREQ1	A18	I/O	SA13
B19	I/O	REF*	A19	I/O	SA12
B20	Out	SYSCLK	A20	I/O	SA11
B21	In	IRQ7	A21	I/O	SA10
B22	In	IRQ6	A22	I/O	SA9
B23	In	IRQ5	A23	I/O	SA8
B24	In	IRQ4	A24	I/O	SA7
B25	In	IRQ3	A25	I/O	SA6
B26	Out	DACK2*	A26	I/O	SA5
B27	Out	T/C	A27	I/O	SA4
B28	Out	BALE	A28	I/O	SA3
B29	Power	+5 Vdc	A29	I/O	SA2
B30	Out	OSC	A30	I/O	SA1
B31	Ground	GND	A31	I/O	SA0

Notes: (1)An asterisk (*) indicates active low signals.
(2)"A" pins are on the accessory card's component side; "B" pins are on the soldered side.

Table 3-17. Backplane I/O Connector Slot Signal Assignments (Continued)

Pin	I/O	Signal Name	Pin	I/O	Signal Name
D1	In	MEMCS16*	C1	I/O	SBHE*
D2	In	I/OCS16*	C2	I/O	LA23**
D3	In	IRQ10	C3	I/O	LA22**
D4	In	IRQ11	C4	I/O	LA21**
D5	In	IRQ12	C5	I/O	LA20**
D6	In	IRQ15	C6	I/O	LA19**
D7	In	IRQ14	C7	I/O	LA18**
D8	Out	DACK0*	C8	I/O	LA17**
D9	In	DREQ0	C9	I/O	MEMR*
D10	Out	DACK5*	C10	I/O	MEMW*
D11	In	DREQ5	C11	I/O	SD8
D12	Out	DACK6*	C12	I/O	SD9
D13	In	DREQ6	C13	I/O	SD10
D14	Out	DACK7*	C14	I/O	SD11
D15	In	DREQ7	C15	I/O	SD12
D16	Power	+5 Vdc	C16	I/O	SD13
D17	In	MASTER*	C17	I/O	SD14
D18	Ground	GND	C18	I/O	SD15

Notes: (1) An asterisk (*) indicates active low signals.
(2) "C" pins are on the accessory card's component side; "D" pins are on the soldered side.
(3) ** indicates an industry-standard signal name. (In the Vectra RS, these signals are identical in speed to signals SA23 to SA17 and meet all their timing requirements.)

Table 3-18. Backplane I/O Connector Slot Signal Descriptions

Signal Name	Signal Description
AEN	ADDRESS ENABLE informs the system that the DMA controller has control of address and control buses. Active during DMA transfers.
BALE	BUFFERED ADDRESS LATCH ENABLE is from the 82306 control buffer. Its falling edge indicates valid address and control signals. Forced high during DMA cycles.
DACK0,1,2,3*, DACK5,6,7*	DMA ACKNOWLEDGE* signals are used by the Processor/Memory PCA to acknowledge direct-memory access requests.
DREQ0,1,2,3, DREQ5,6,7	DMA REQUEST signals are used by accessory cards to request direct-memory access service or to gain system control. The DMA channels are prioritized, with Channel 0 having the highest priority and channel 7 having the lowest. A DMA request signal must be held high until its corresponding acknowledge signal is asserted.
I/OCHCK*	I/O CHANNEL CHECK* is used by an accessory card to indicate to the system that an error has been detected on the card.
I/OCHRDY	I/O CHANNEL READY synchronizes slow memory or I/O devices during read and write operations. If an accessory card is to extend a read or write operation, it should pull this line low as soon as a valid address and a read or write command is detected. A read or write operation should not be extended to more than 15 SYSCLK cycles. Clock cycles added via this signal are in addition to any added by the system.
I/OCS16*	I/O CHIP SELECT (16 bits)* indicates to the system that an accessory card can perform 16-bit I/O operations. The driver should be an open collector or a tri-state device capable of sinking 20 mA.
IOR*	I/O READ* indicates an I/O read cycle is in progress. IOR* may be driven by a DMA controller or by an external microprocessor (if MASTER* is asserted).
IOW*	I/O WRITE* indicates an I/O write cycle is in progress. IOW* may be driven by a DMA controller or by an external microprocessor (if MASTER* is asserted).
IRQ3,4,5,6,7, IRQ9,10,11,12, IRQ14,15	INTERRUPT REQUEST signals are used by accessory cards to signal request for interrupt service. These edge-sensitive signals are asserted by a low-to-high transition. The signal must be held high until the interrupt is acknowledged. The IRQ signals are prioritized as follows, starting with the highest prioritization: IRQ9, 10, 11, 12, 14, 15, 3, 4, 5, 6, 7.

* Active low.

Table 3-18. Backplane I/O Connector Slot Signal Descriptions (Continued)

Signal Name	Signal Description
LA17 to LA23 (SA17 to SA23)	LINE ADDRESS signals (not to be confused with lines from the local address bus, "LA"), are upper system address lines. When combined with system address lines SA0 to SA19, they produce 16 Mbytes of memory address space. These signals are latched by the accessory card on BALE's trailing edge. LA17 to LA23 may be driven by a DMA controller or the 80836 microprocessor on the I/O channel (if MASTER* is asserted).
MASTER*	MASTER* signal used by an accessory card to disable the 80386 microprocessor and gain control of the system buses. To gain control, one of the DMA channels must be placed in the cascade mode, and the accessory card must issue a DMA request (DREQ) and receive an acknowledge (DACK). The accessory card may then assert MASTER* and gain control of the system. It must wait one clock cycle before attempting to drive the address or data lines, and two clock cycles before issuing a read or write command. Holding this signal low for 15 microseconds or more may cause a memory loss because of the absence of refresh.
MEMCS16*	MEMORY CHIP SELECT (16 bits)* indicates to the system that the accessory card can perform 16-bit memory operations. The driver should be an open collector or a tri-state device capable of sinking 20 mA, and this signal should be derived from LA17 to LA23.
MEMR*	MEMORY READ* indicates a memory read cycle is in progress. MEMR* may be driven by a DMA controller or by an external microprocessor (if MASTER* is asserted).
MEMW*	MEMORY WRITE* indicates a memory write cycle is in progress. MEMW* may be driven by a DMA controller or by an external microprocessor (if MASTER* is asserted).
OSC	OSCILLATOR, a 14.318 MHz timing reference signal with a 50% duty cycle and a period of approximately 70 nanoseconds, is asynchronous with the SYSCLK signal.
REF*	REFRESH*, which indicates a memory refresh operation is in progress, may be driven by a microprocessor on the backplane I/O channel (if MASTER* is asserted).
RESET DRV	RESET DRIVE resets all system devices during power-on resets and indicates low line voltage conditions.

* Active low

Table 3-18. Backplane I/O Connector Slot Signal Descriptions (Continued)

Signal Name	Signal Description
SA0 to SA19	SYSTEM ADDRESS lines, when combined with LA17 to LA23, produce 16 Mbytes of memory address space. SA0 to SA19 begin to change on BALE's rising edge and are latched for the cycle's duration by BALE's falling edge. SA0 to SA19 may be driven by a DMA controller or processor on the backplane I/O channel. The system refresh controller places the refresh address on SA0 to SA7 during refresh cycles.
SBHE*	SYSTEM BUS HIGH ENABLE* indicates that data are to be transferred on SD8 to SD15. SBHE* indicates that a 16-bit transfer or an 8-bit transfer to an odd address (A0=1) is in progress.
SD0 to SD15	SYSTEM DATA bus signals transfer data to and from the system. Sixteen-bit transfers occur on SD0 to SD15. Eight-bit transfers occur on SD0 to SD7, unless SBHE* is asserted, in which case, data are transferred on SD8 to SD15. Sixteen-bit to 8-bit transfers are multiplexed by the backplane state machine into two 8-bit transfers on SD0 to SD7.
SMEMR*	SYSTEM MEMORY READ* indicates a system memory read cycle is in progress. SMEMR* is active if MEMR* is active and the address decode circuit indicates a valid address in the bottom 1 Mbyte of memory space.
SMEMW*	SYSTEM MEMORY WRITE* indicates a system memory write cycle is in progress. SMEMW* is active if MEMW* is active and the address decode circuit indicates a valid address in the bottom 1 Mbyte of memory space.
SYSCLK	SYSTEM CLOCK, the 8-MHz system clock for the 80386 microprocessor, has a 50% duty cycle and a period of approximately 125 nanosec- onds. Can be used to synchronize activities to the 80386 microprocessor.
T/C	TERMINAL COUNT informs the system that the terminal count for one of the DMA channels has been reached.
0WS*	ZERO WAIT STATE* indicates to the system that a read or write operation can take place without additional system-generated wait states. To perform a 16-bit memory cycle with zero wait states, this signal should be asserted as soon as a valid address decode and a read or write command is detected. To shorten cycles for 8-bit devices, 0WS* should be asserted on the falling edge of SYSCLK after detecting a valid address and a read or write command for two wait states. If asserted on the second falling edge of SYSCLK after detecting a valid address and a read or write command, three wait states will be generated for 8-bit devices. The driver should be an open collector or a tri-state device capable of sinking 20 mA.

* Active low

3.5.2 Backplane I/O Timing Diagrams

Table 3-19 and the backplane I/O timing diagrams which follow (Figure 3-8 to Figure 3-13) are included as a guide to general system characteristics. If the following information is to be used by hardware developers or vendors, full qualification of all equipment should be performed to ensure that worst-case timing requirements and parameters are met.

Note: All values are in nanoseconds, except for the value given for Note 45, which is given in microseconds.

Table 3-19. Notes for Timing Diagrams

Figure	Note	Function	Minimum	Maximum
3-8	1	SYSCLK period (8 MHz)	-	125
3-8	2	BALE high from SYSCLK	-	9
3-8	3	BALE low from SYSCLK	-	14
3-8	4	SBHE* low from SYSCLK	-	21
3-8	5	SBHE* invalid from SYSCLK	-	16
3-8	6	SBHE* high from SYSCLK	-	19
3-8	7	SA/LA valid to SYSCLK	5	-
3-8	8	SA/LA tri-state from SYSCLK	-11	23
3-8	9a	SMEMR*/SMEMW* low from SYSCLK (without command delay)	-	25
3-8	9b	SMEMR*/SMEMW* low from SYSCLK (with command delay)	-	21
3-8	10	SMEMR*/SMEMW* high from SYSCLK	-	21
3-8				
3-8	11a	MEMR*/MEMW* low from SYSCLK (without command delay)	-	21
3-8	11b	MEMR*/MEMW* low from SYSCLK (with command delay)	-	17
3-8	12	MEMR*/MEMW* high from SYSCLK	-	16
3-8	13	IOCHRDY setup to SYSCLK	30	-
3-8	14	IOCHRDY hold from SYSCLK	-2	-
3-8	15	MEMCS16*/IOCS16* setup to SYSCLK	48	-
3-8	16	MEMCS16*/IOCS16* hold from SYSCLK	25 (1)	-
3-8	17	0WS* setup to SYSCLK	34	-
3-8	18	0WS* hold from SYSCLK	-1	-
3-8	19	Number of idle states between immediate cycles	2 (1)	-

* Indicates active low.
(1) Typical value.

Table 3-19. Notes for Timing Diagrams (Continued)

Figure	Note	Function	Minimum	Maximum
3-9	20	SD setup to SYSCLK, read cycle	23	-
3-9	21	SD hold from SYSCLK, read cycle	11	-
3-9	22	SD valid from SYSCLK, write cycle	-	47
3-9	23a	SD hold SMEMW* high, write cycle	31.5 (2) 19 (3)	- -
3-9	23b	SD hold from IOW* high, write cycle	36.5 (2) 24 (3)	- -
3-10	24	IOR*/IOW* low from SYSCLK	-	16
3-10	25	IOR*/IOW* high from SYSCLK	-	16
3-11	26	SA0 low to high from SYSCLK	-	48
3-12	27	DREQn hold from DACKn* valid	0	-
3-12	28	DREQn low setup to SYSCLK	0	-
3-12	29	AEN high to SYSCLK	3	-
3-12	30	AEN low from SYSCLK	310 (1)	-
3-12	31	SA/LA valid from SYSCLK	-	90
3-12	32	SA/LA tri-state from SYSCLK	-	85
3-12	33	DACKn* low from SYSCLK	-	105
3-12	34	DACKn* high from SYSCLK	-	105
3-12	35	IOR* low from SYSCLK	-	138
3-12	36	IOR* high from SYSCLK	-	119
3-12	37	CMD (4) driven high from SYSCLK	-	109
3-12	38	T/C delay from SYSCLK	-	60
3-12	39	IOCHRDY setup to SYSCLK	35	-
3-12	40	IOCHRDY hold from SYSCLK	20	-
3-13	41	MEMR* low from SYSCLK	-	21
3-13	42	MEMR* high from SYSCLK	-	16
3-13	43	SA valid after REF* valid	-	64
3-13	44	SA invalid after REF* invalid	-	33
3-13	45	Refresh cycle	15 micro-seconds (1)	-

* Indicates active low.
(1) Typical value.
(2) Value at 8 MHz.
(3) Value at 10 MHz.
(4) CMD = IOR*, IOW*, SMEMR*, or SMEMW*

Note: Except for the value given for Note 45, all values are in nanoseconds.

Figure 3-8. Backplane I/O Timing Diagram -- Common Timing

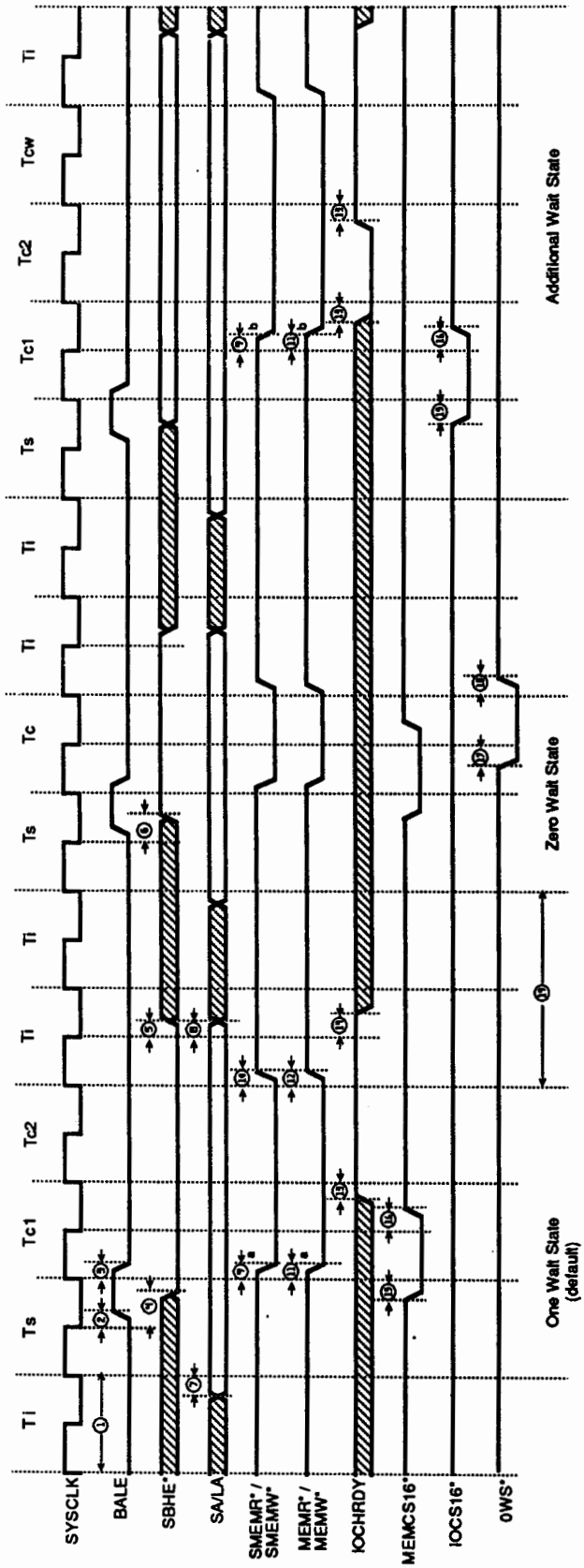


Figure 3-9. Backplane I/O Timing Diagram – Memory Cycle

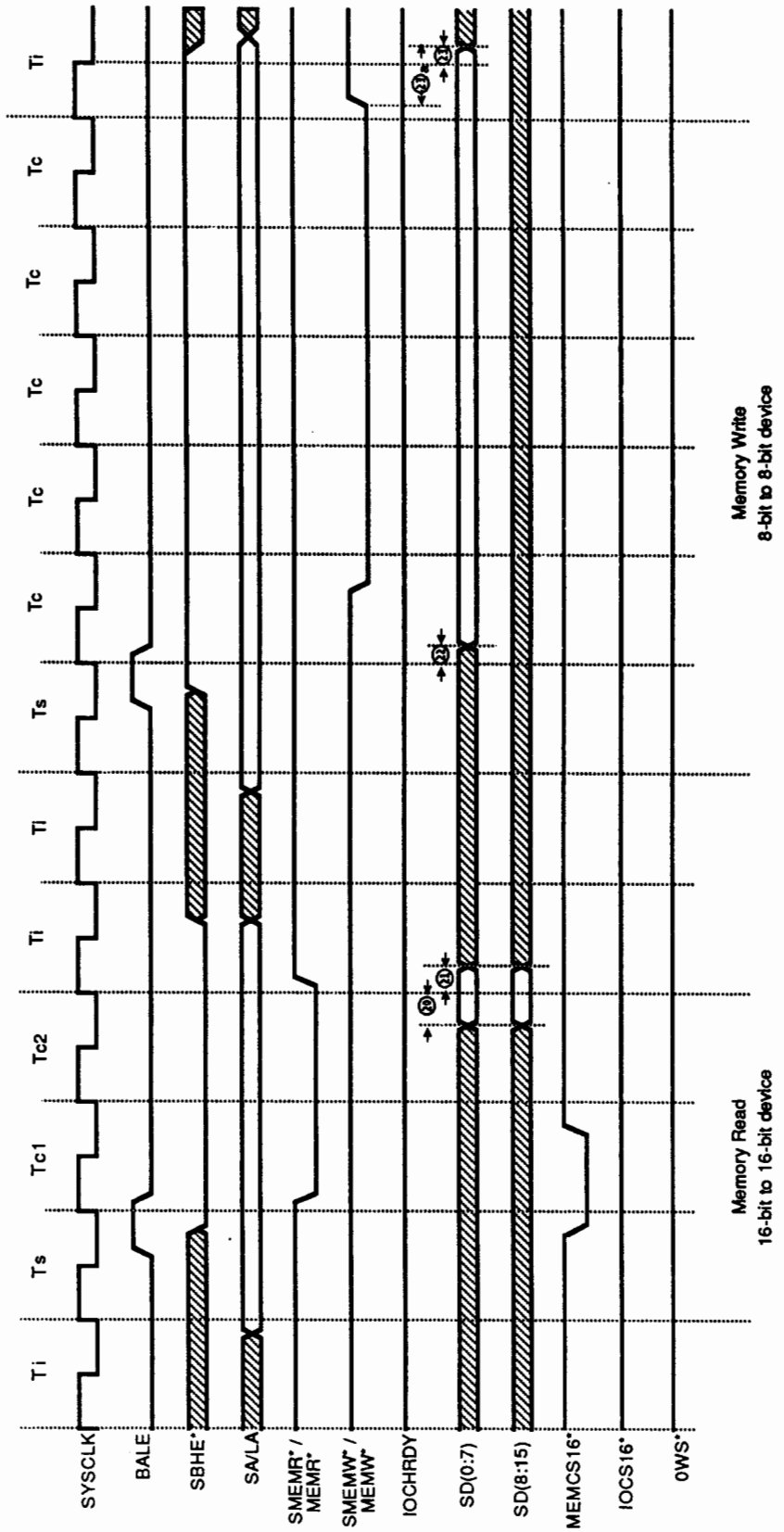


Figure 3-10. Backplane I/O Timing Diagram -- I/O Cycle

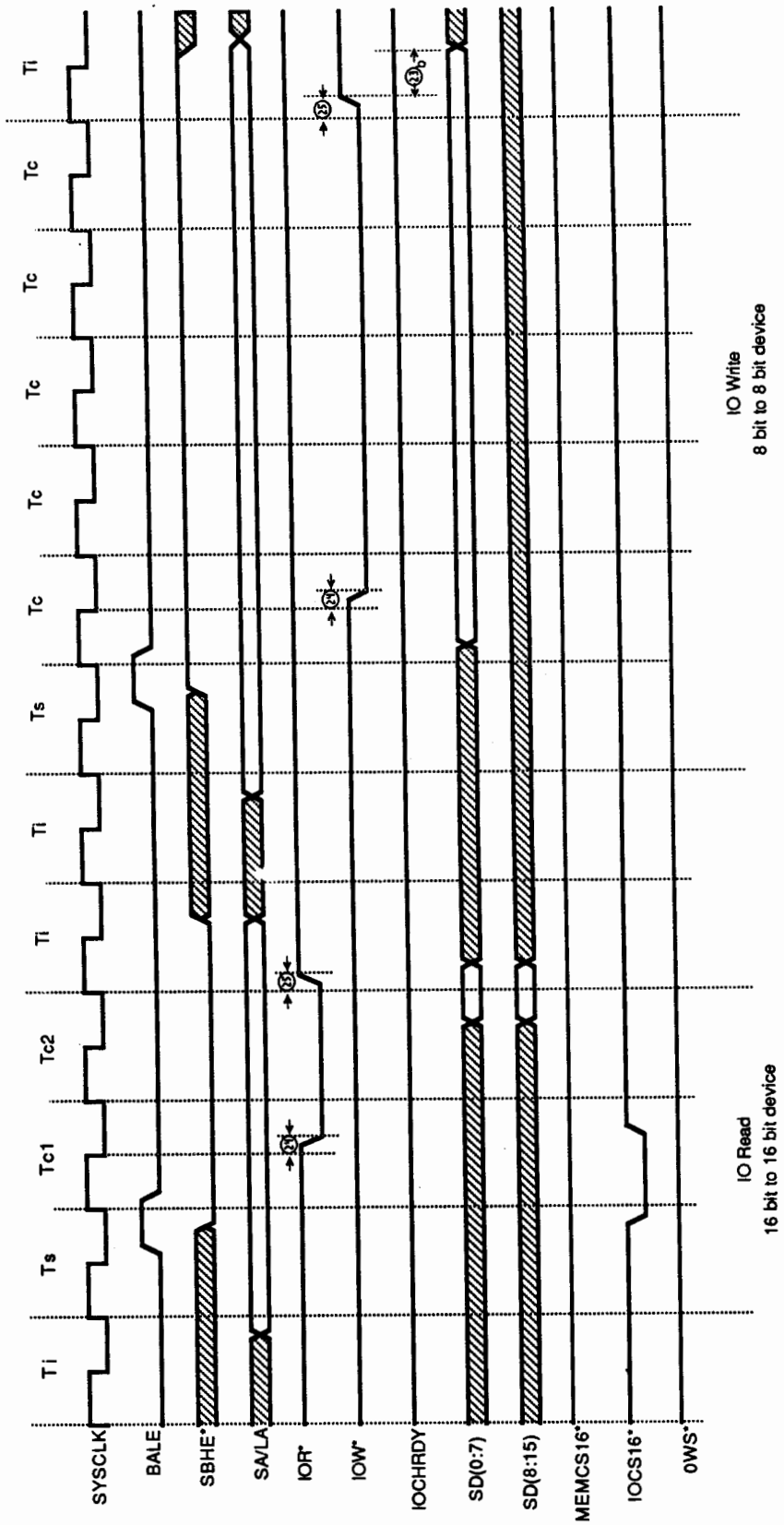


Figure 3-11. Backplane I/O Timing Diagram -- 16-Bit to 8-Bit Cycles

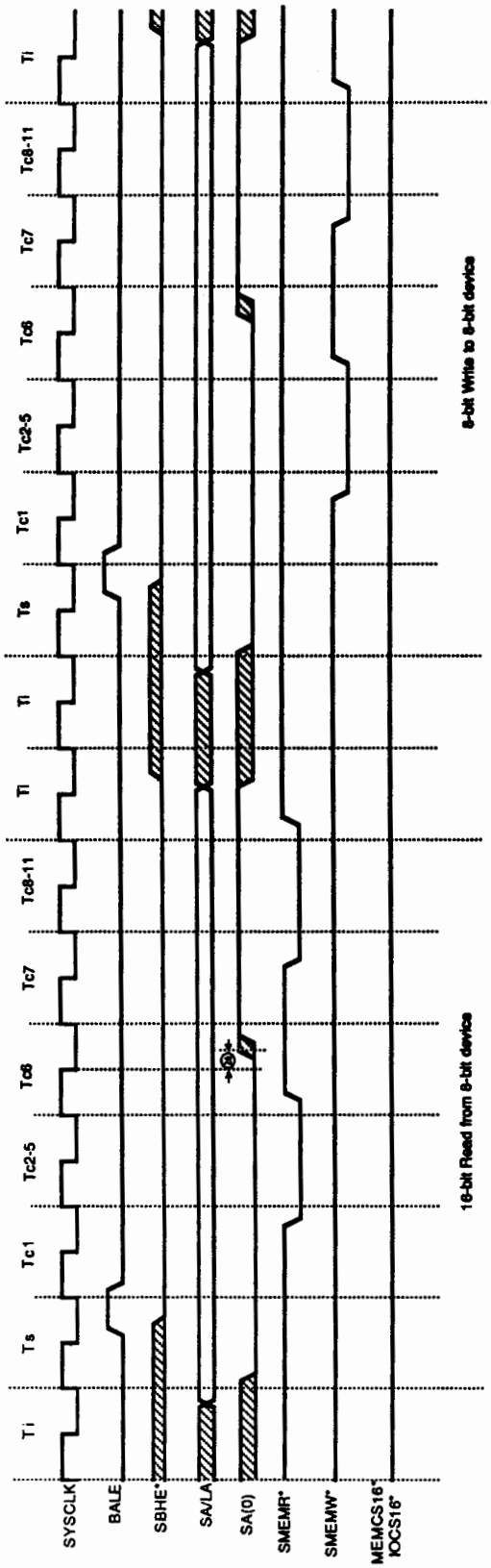


Figure 3-12. Backplane I/O Timing Diagram --
Single Byte/Word DMA Transfer from I/O to Memory

(For example, read from a flexible disc, in uncompressed mode)

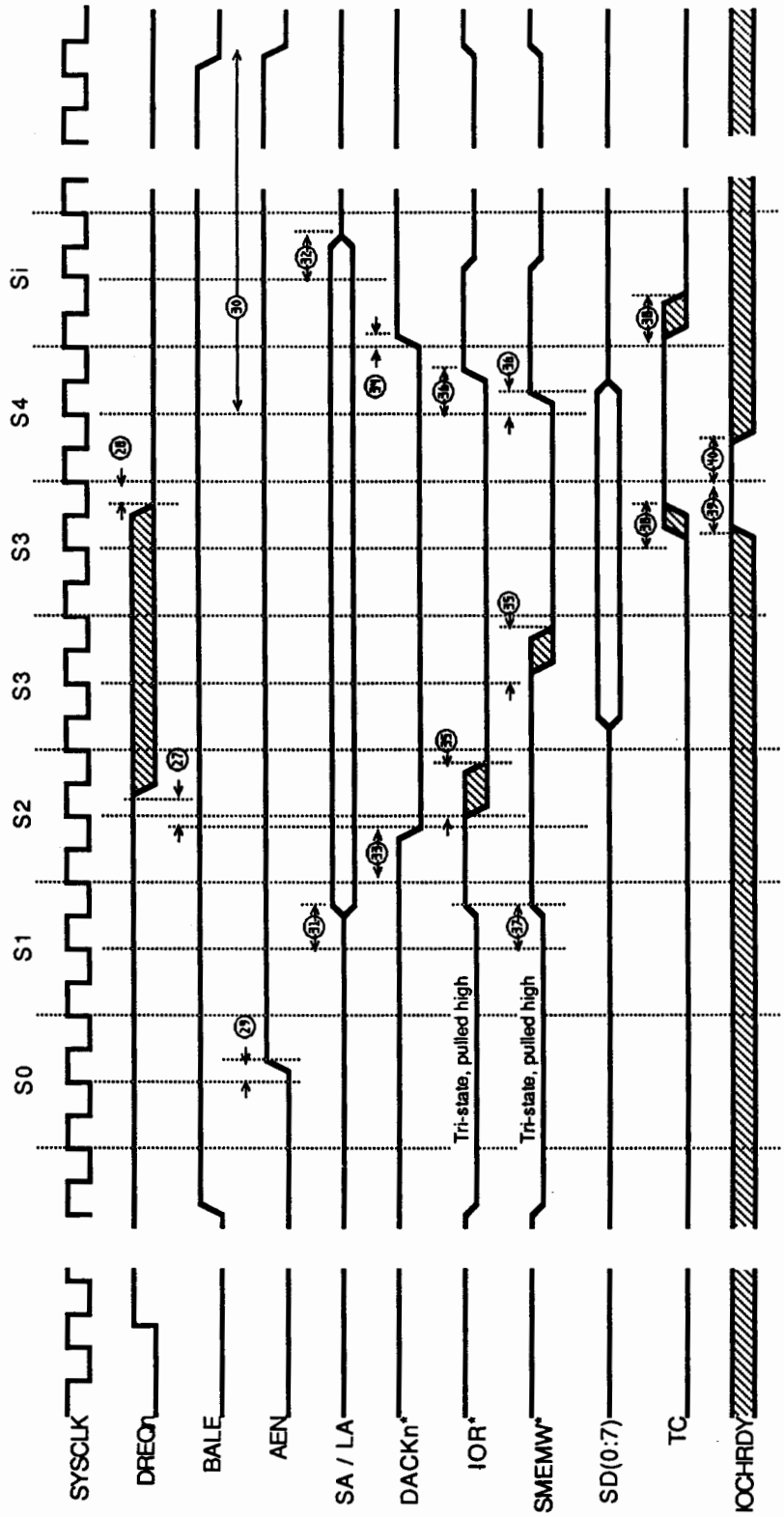
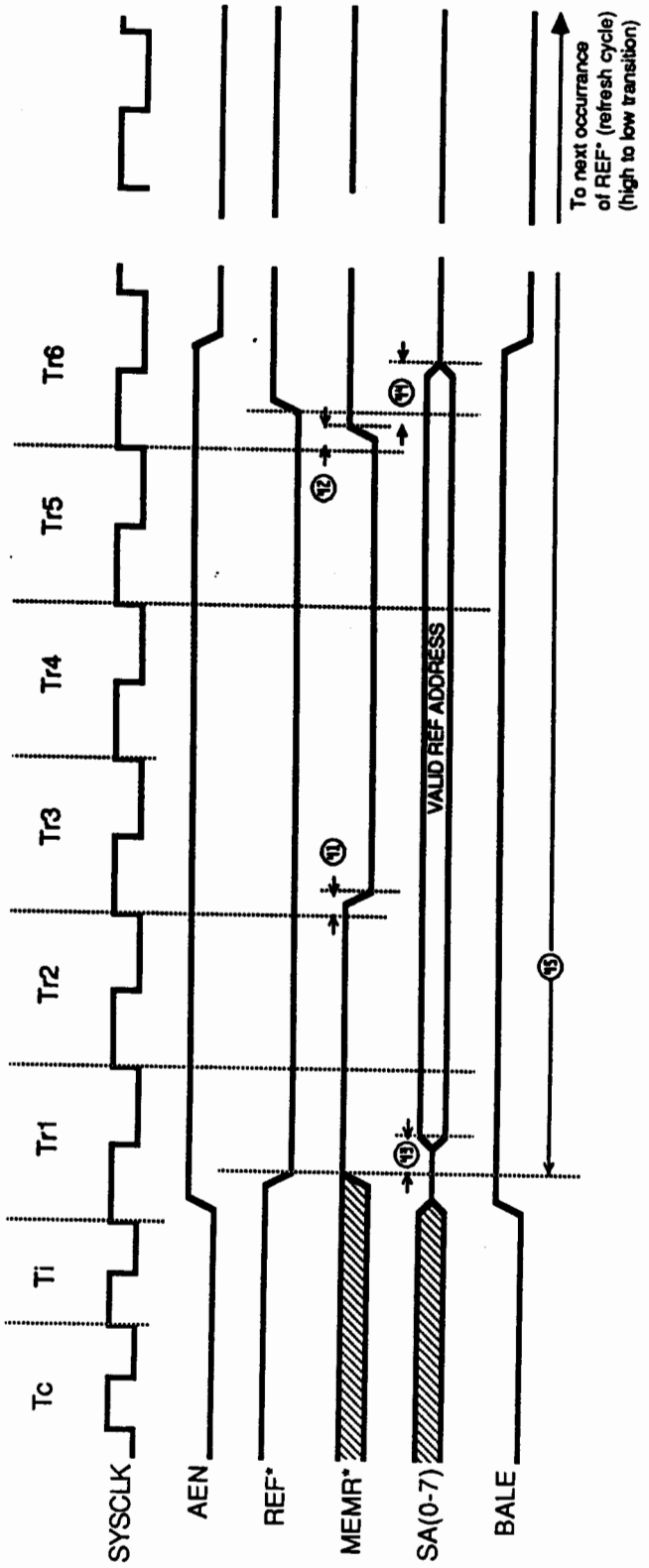
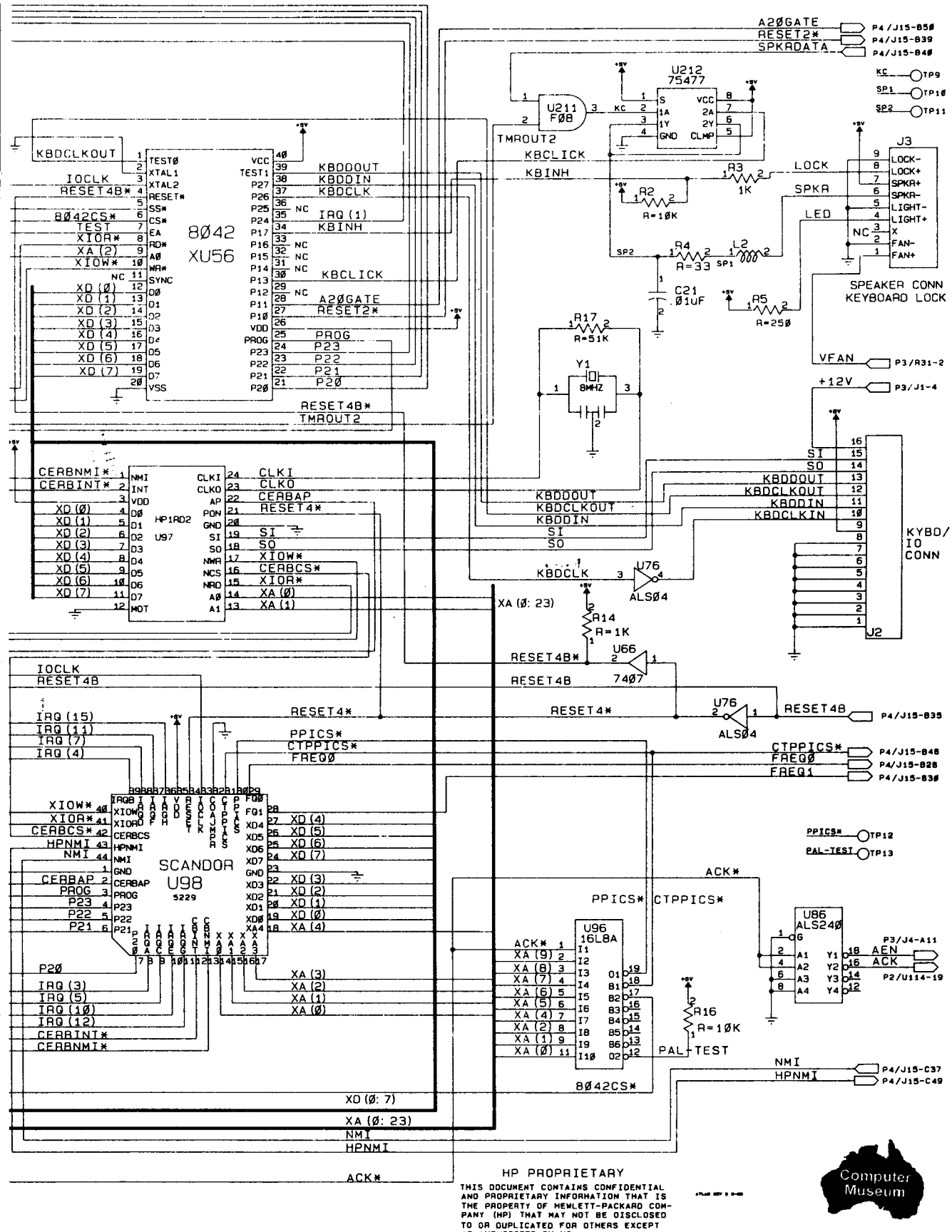


Figure 3-13. Backplane I/O Timing Diagram -- Refresh



3.6 System Interface PCA and Input Device PCA Schematics

To help understand the System Interface PCA and the Input Device Connector PCA, schematics are given on the following pages. Schematics for the Processor/Memory PCA are given at the end of the chapter, "Processor/Memory PCA." (Hewlett-Packard does not guarantee the accuracy of the schematics.)



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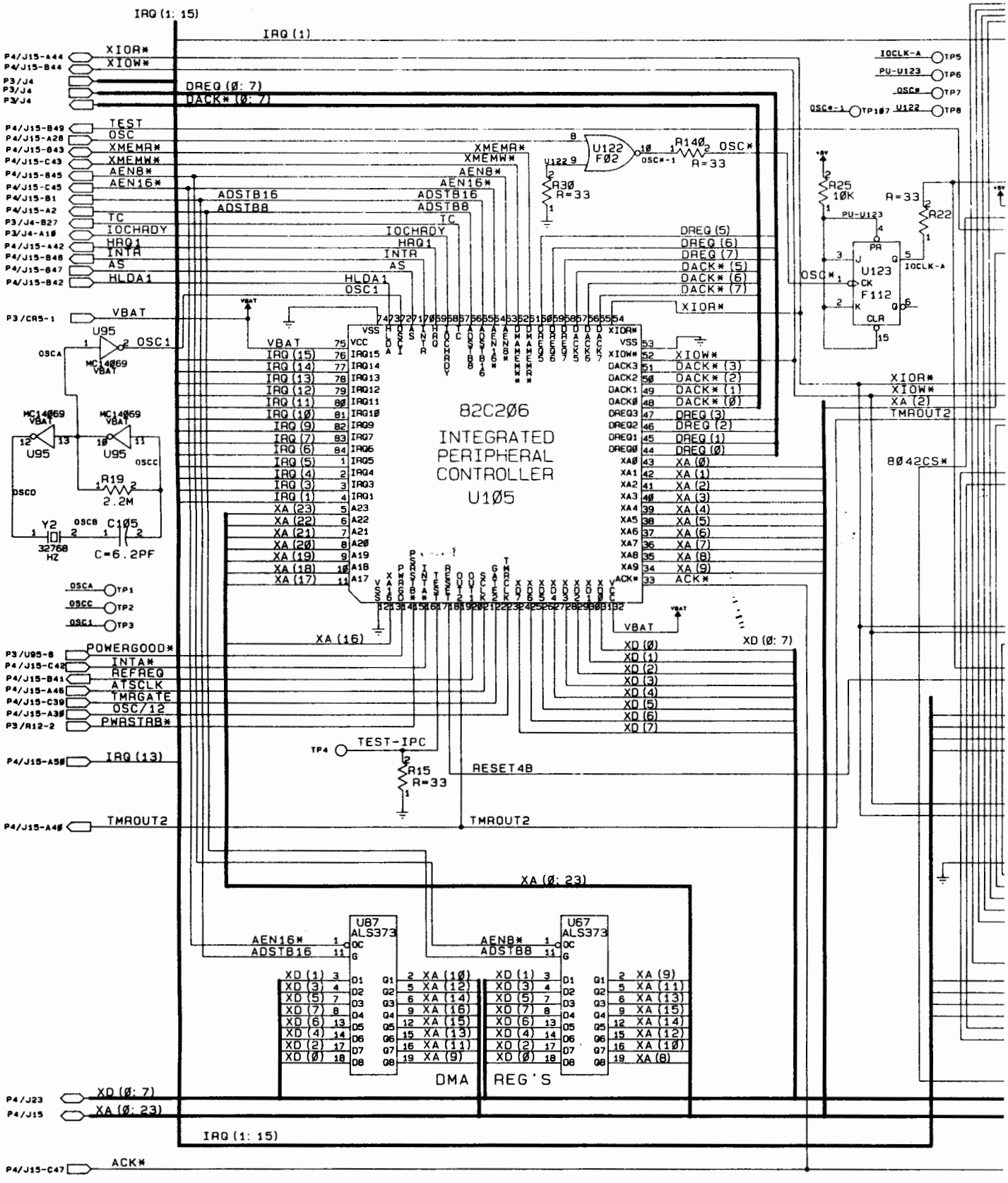
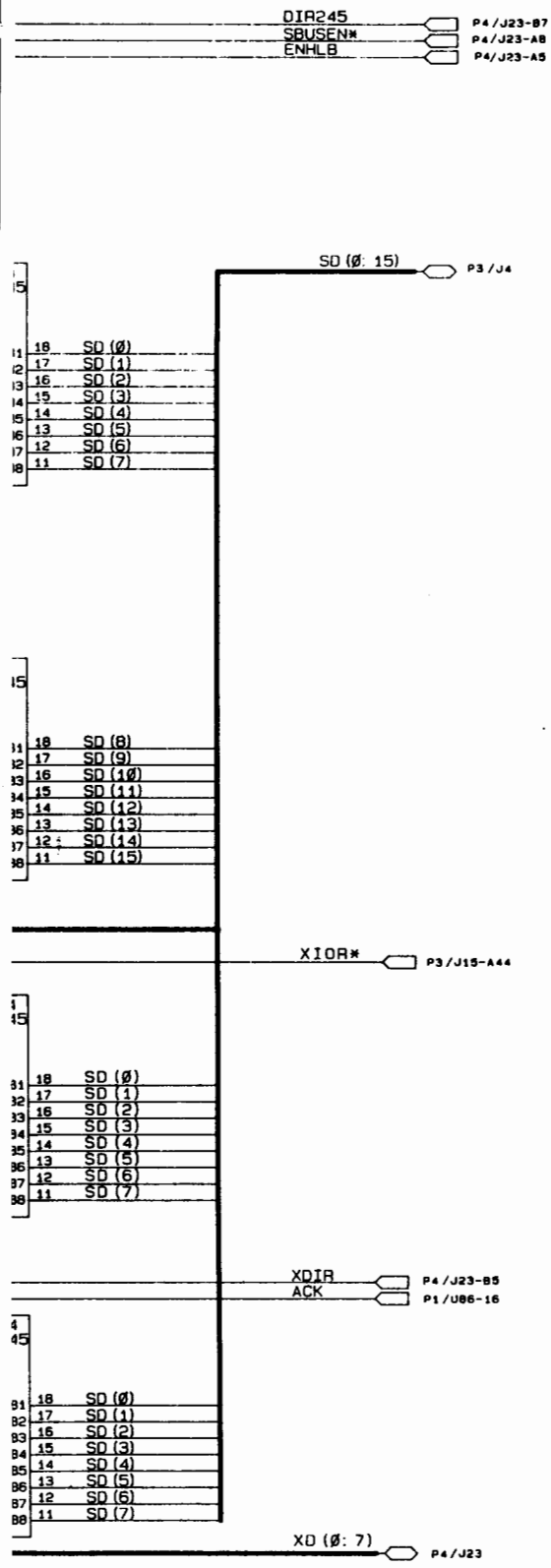
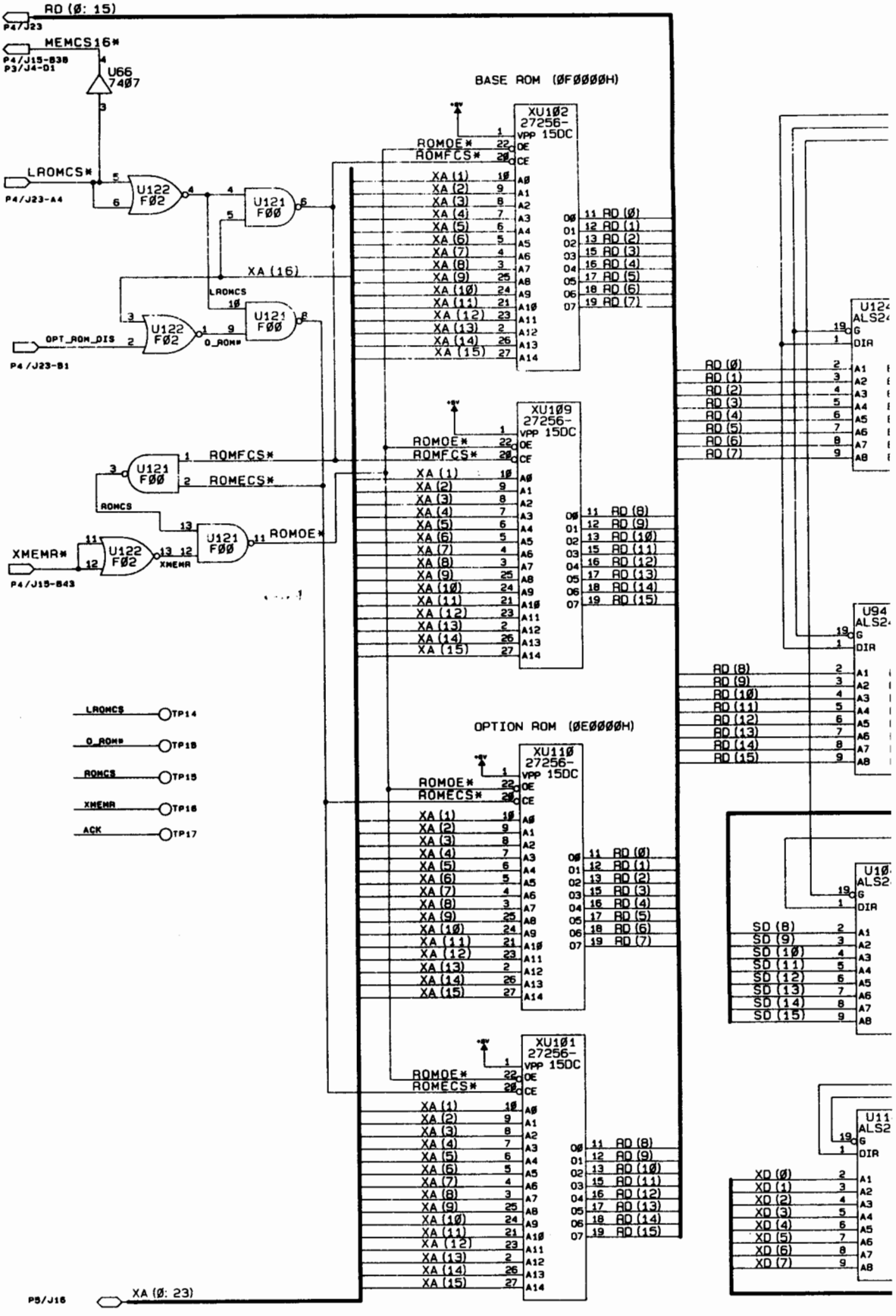
System Interface PCA Schematic

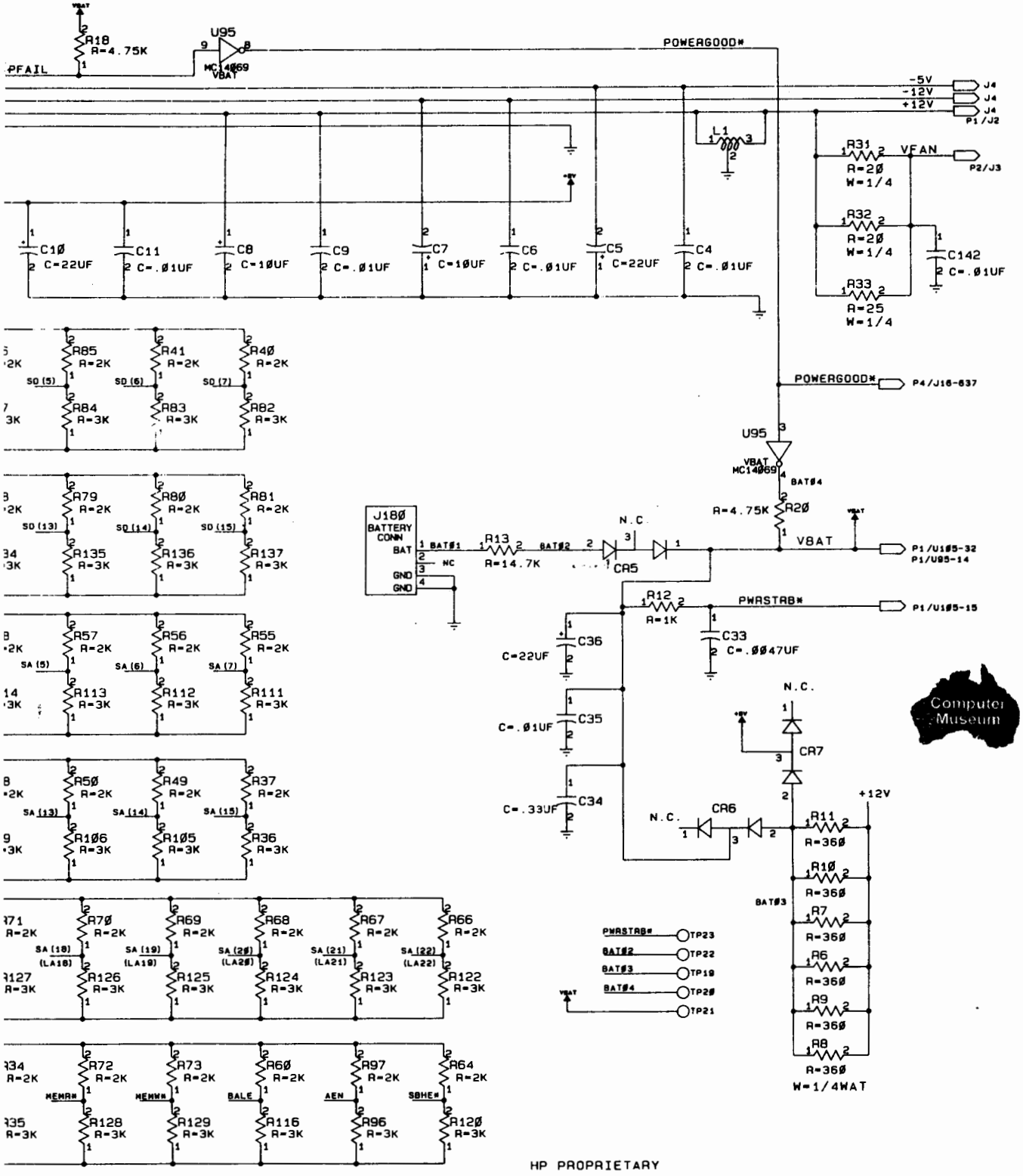

82C206
INTEGRATED
PERIPHERAL
CONTROLLER
U105
IRQ (1: 15)
IRQ (1)
XIOR*
XIOW*
DREQ (Ø: 7)
DACK* (Ø: 7)
TEST
OSC
XMEMR*
XMEMW*
AEN8*
AEN16*
ADSTB16
ADSTB8
TC
IOCHRDY
HRQ1
INTA
AS
HLDA1
OSC1
VBAT
U95
MC14069
OSCA
OSCC
OSCO
R19
2.2M
Y2
32768
HZ
C105
C=6.2PF
POWERGOOD*
INTA*
REFREQ
ATSCLK
TMRGATE
OSC/12
PWRSTRB*
IRQ (13)
TMROUT2
TEST-IPC
RESET4B
XA (16)
XD (Ø: 7)
XA (Ø: 23)
U87
ALS373
U67
ALS373
DMA
REG'S
XD (Ø: 7)
XA (Ø: 23)
ACK*
U122
F02
R140
R=33
R30
R=33
R25
10K
R22
U123
F112
IOCLK-A
PU-U123
OSC*
OSC*-1
8042CS*
XA (2)
TMROUT2



System Interface PCA Schematic

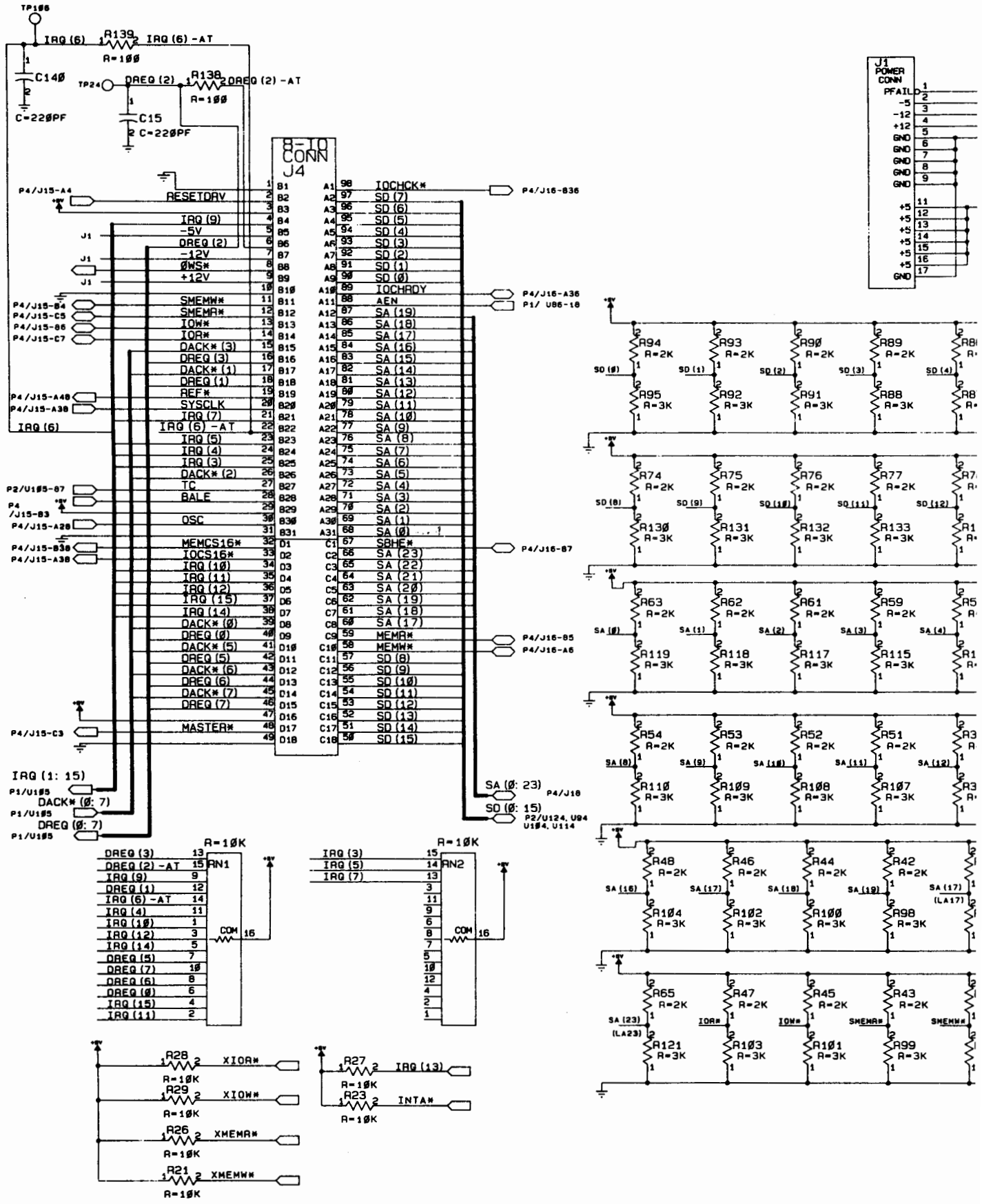
3-55/3-56


BD (Ø: 15)
P4/J23
MEMCS16*
P4/J15-B38
P3/J4-D1
U66
74Ø7
LAOMCS*
P4/J23-A4
U122
FØ2
U121
FØØ
XA (16)
LAOMCS
OPT_ROM_DIS
P4/J23-B1
O_ROM*
ROMFCS*
ROMECS*
ROMCS
XMEMR*
P4/J15-B43
XMEMR
ROMOE*
BASE ROM (ØFØØØØH)
XU1Ø2
27256-
15DC
XU1Ø9
OPTION ROM (ØEØØØØH)
XU11Ø
XU1Ø1
U124
ALS24
U94
U1Ø
U11
LAOMCS
O_ROM*
ROMCS
XMEMR
ACK
TP14
TP15
TP16
TP17
P5/J16
XA (Ø: 23)

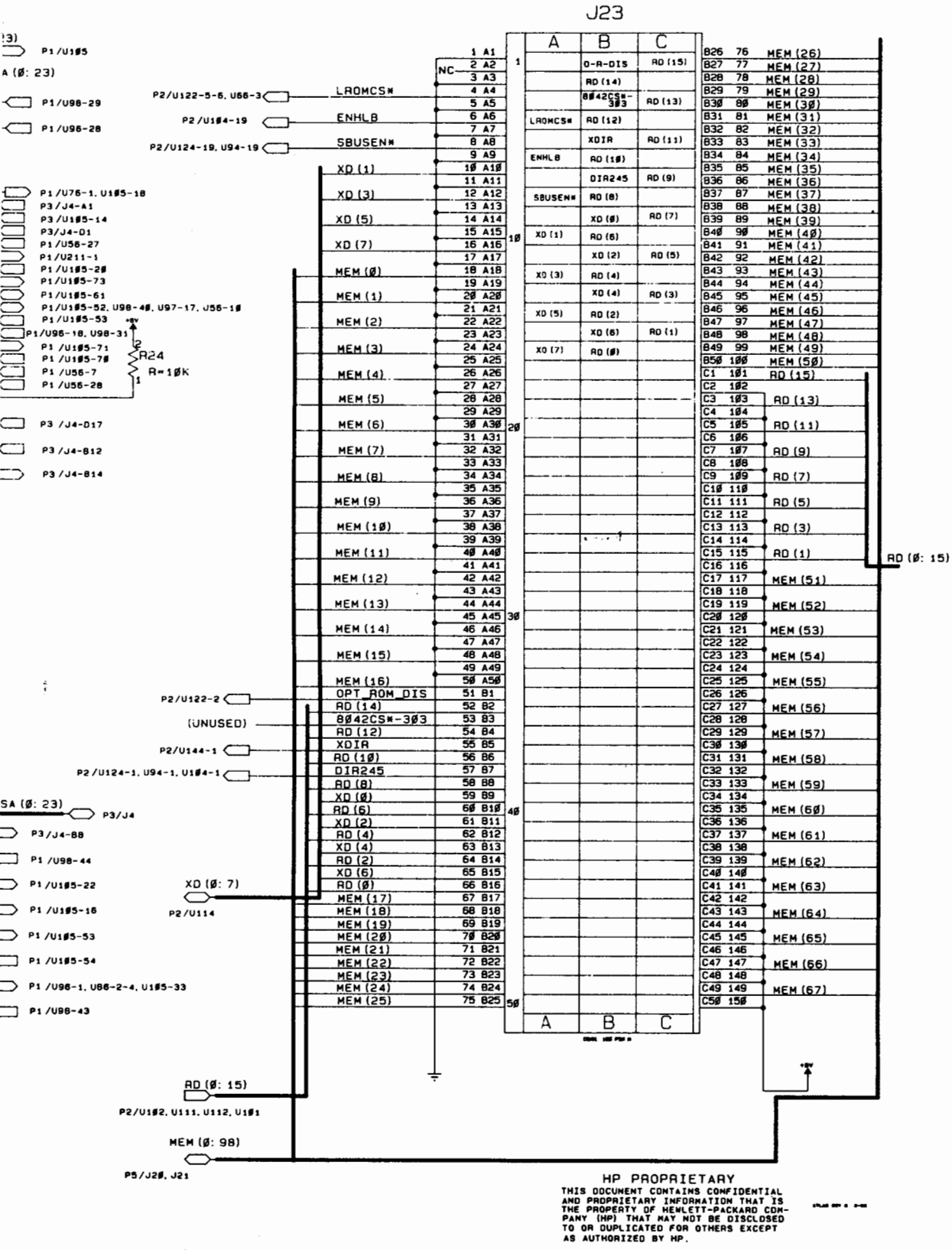


System Interface PCA Schematic

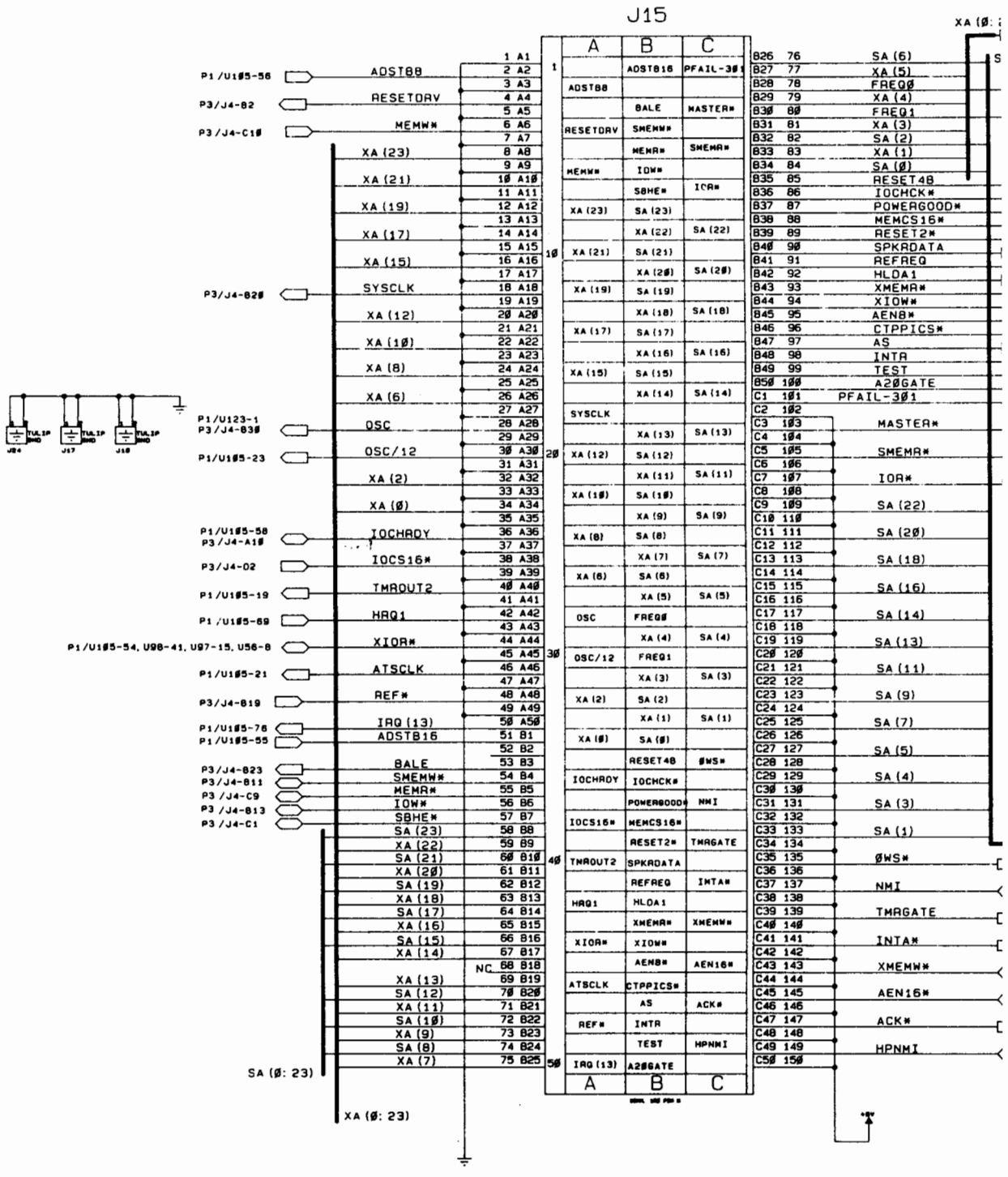
3-57/3-58

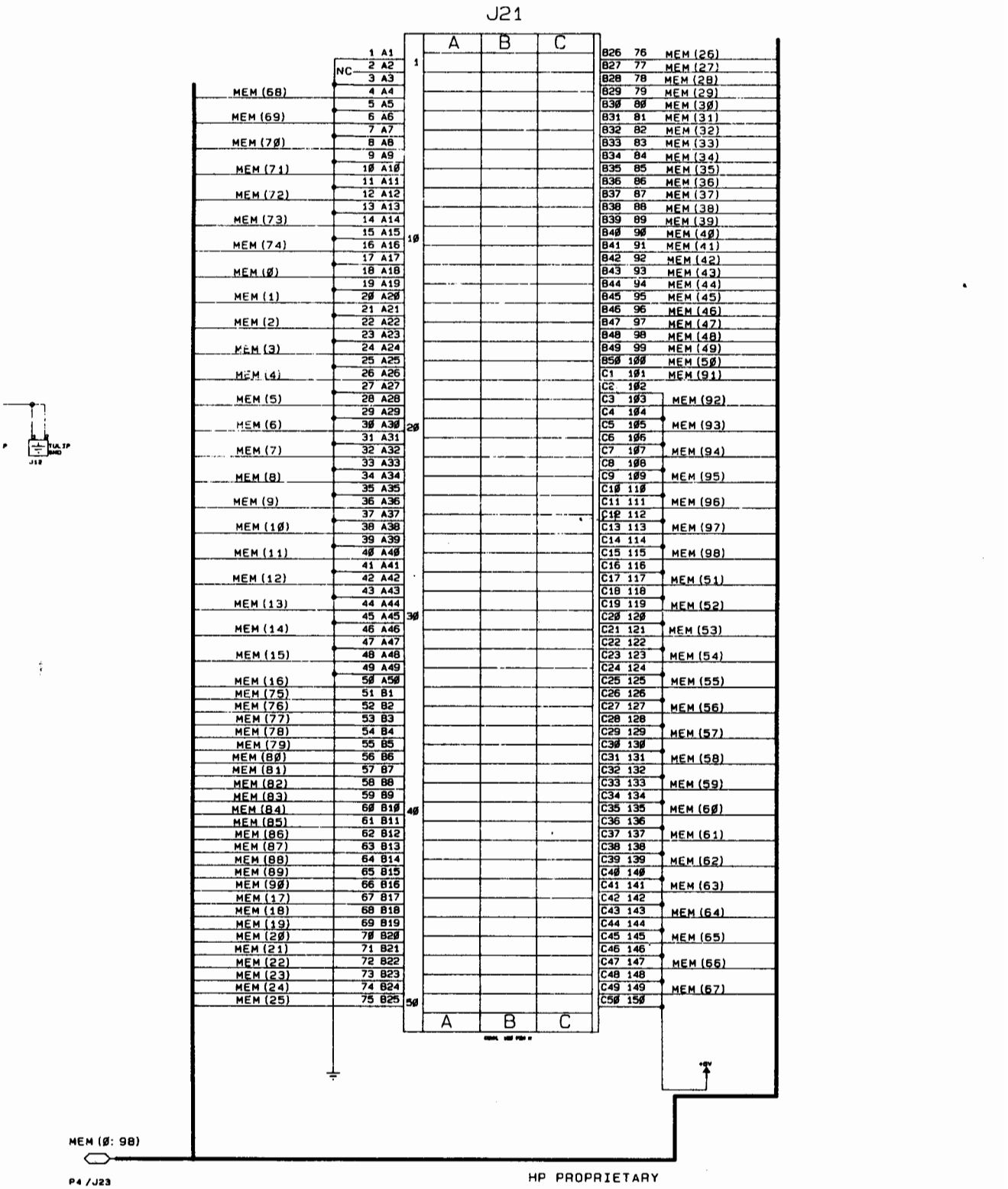

TP1Ø6
IRQ (6)
R139
R=1ØØ
IRQ (6) -AT
C14Ø
C=22ØPF
TP24
DREQ (2)
R138
R=1ØØ
DREQ (2) -AT
C15
C=22ØPF
8-IO CONN J4
P4/J15-A4
RESETDRV
IRQ (9)
-5V
DREQ (2)
-12V
ØWS*
+12V
SMEMW*
SMEMR*
IOW*
IOR*
DACK* (3)
DREQ (3)
DACK* (1)
DREQ (1)
REF*
SYSCLK
IRQ (7)
IRQ (6) -AT
IRQ (5)
IRQ (4)
IRQ (3)
DACK* (2)
TC
BALE
OSC
MEMCS16*
IOCS16*
IRQ (1Ø)
IRQ (11)
IRQ (12)
IRQ (15)
IRQ (14)
DACK* (Ø)
DREQ (Ø)
DACK* (5)
DREQ (5)
DACK* (6)
DREQ (6)
DACK* (7)
DREQ (7)
MASTER*
IOCHCK*
SD (7)
SD (6)
SD (5)
SD (4)
SD (3)
SD (2)
SD (1)
SD (Ø)
IOCHRDY
AEN
SA (19)
SA (18)
SA (17)
SA (16)
SA (15)
SA (14)
SA (13)
SA (12)
SA (11)
SA (1Ø)
SA (9)
SA (8)
SA (7)
SA (6)
SA (5)
SA (4)
SA (3)
SA (2)
SA (1)
SA (Ø)
SBHE*
SA (23)
SA (22)
SA (21)
SA (2Ø)
SA (19)
SA (18)
SA (17)
MEMR*
MEMW*
SD (8)
SD (9)
SD (1Ø)
SD (11)
SD (12)
SD (13)
SD (14)
SD (15)
P4/J16-B36
P4/J16-A36
P1/ U86-18
P4/J16-B7
P4/J16-B5
P4/J16-A5
SA (Ø: 23)
P4/J18
SD (Ø: 15)
P2/U124, U94
U1Ø4, U114
IRQ (1: 15)
P1/U1Ø5
DACK* (Ø: 7)
DREQ (Ø: 7)
J1 POWER CONN
PFAIL
-5
-12
+12
GND
+5
R=1ØK
RN1
RN2
COM
XIOR*
XIOW*
XMEMR*
XMEMW*
INTA*
R=2K
R=3K
IOR*
IOW*
SMEMR*
SMEMW*

CPU CONNECTOR

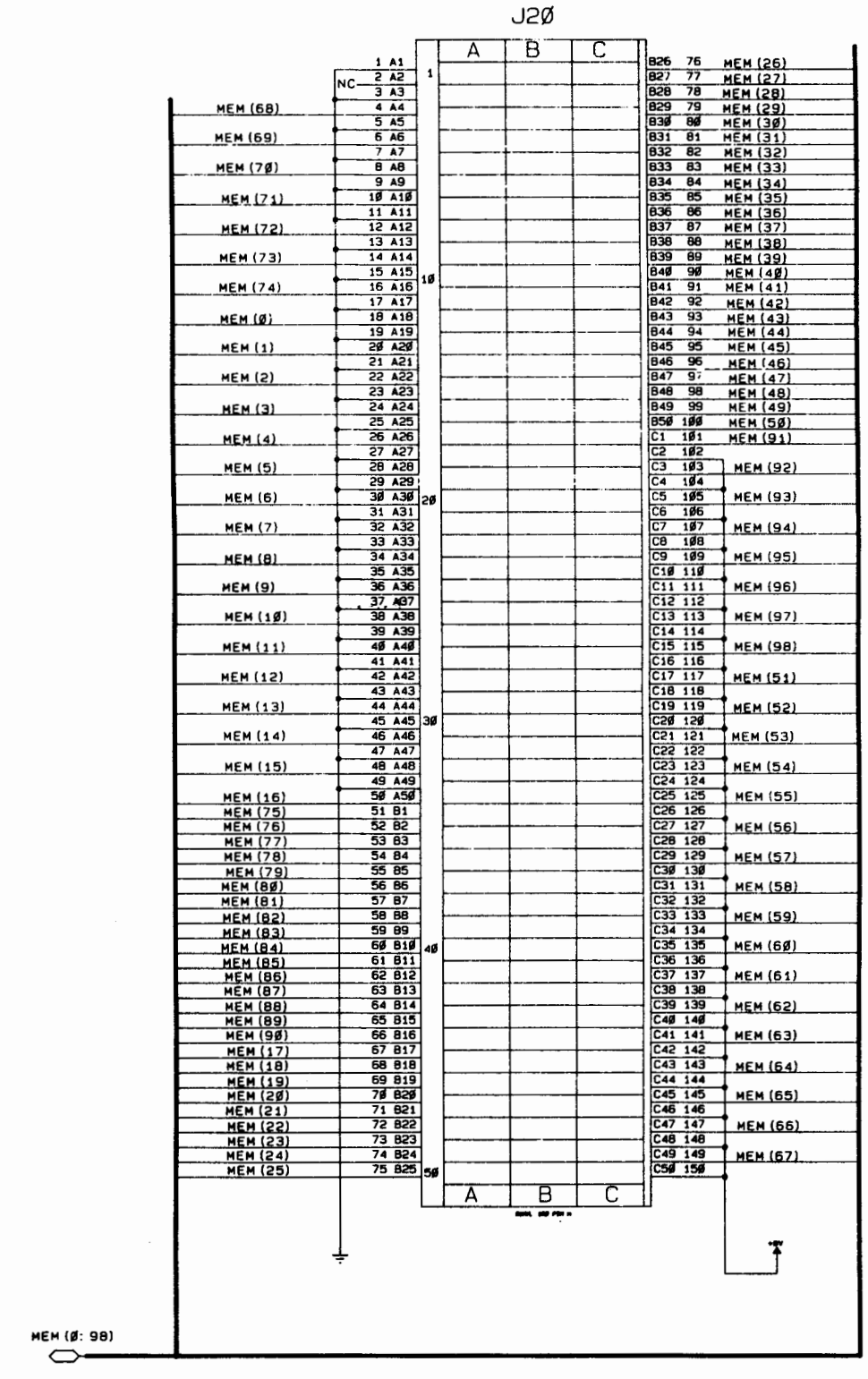


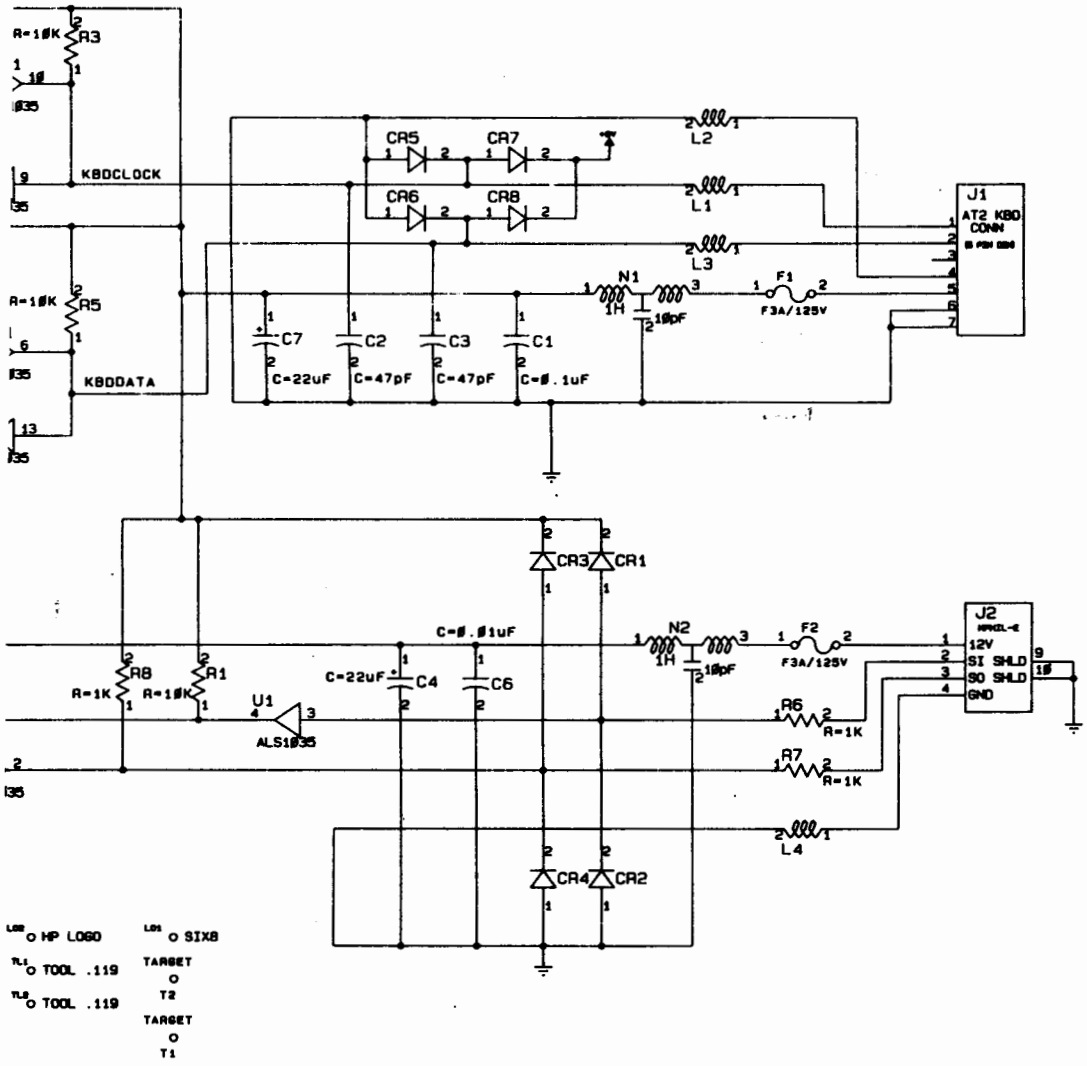
System Interface PCA Schematic


J15
A
B
C
P1/U185-56
ADSTB8
RESETDRV
P3/J4-82
MEMW*
P3/J4-C18
XA (23)
XA (21)
XA (19)
XA (17)
XA (15)
SYSCLK
P3/J4-828
XA (12)
XA (10)
XA (8)
XA (6)
P1/U123-1
P3/J4-838
OSC
OSC/12
P1/U185-23
XA (2)
XA (0)
P1/U185-58
P3/J4-A18
IOCHRDY
IOCS16*
P3/J4-D2
TMROUT2
P1/U185-19
HRQ1
P1/U185-69
XIOR*
P1/U185-54, U98-41, U97-15, U56-8
ATSCLK
P1/U185-21
REF*
P3/J4-819
IRQ(13)
P1/U185-78
ADSTB16
P1/U185-55
BALE
P3/J4-823
SMEMW*
P3/J4-811
MEMR*
P3/J4-C9
IOW*
P3/J4-813
SBHE*
P3/J4-C1
SA (23)
XA (22)
SA (21)
XA (20)
SA (19)
XA (18)
SA (17)
XA (16)
SA (15)
XA (14)
NC
XA (13)
SA (12)
XA (11)
SA (10)
XA (9)
SA (8)
XA (7)
SA (0: 23)
XA (0: 23)
ADSTB16
PFAIL-3@1
BALE
MASTER*
SMEMW*
MEMR*
SMEMR*
IOW*
SBHE*
IOCR*
SA (23)
SA (22)
SA (21)
SA (20)
SA (19)
SA (18)
SA (17)
SA (16)
SA (15)
SA (14)
SA (13)
SA (12)
SA (11)
SA (10)
SA (9)
SA (8)
SA (7)
SA (6)
SA (5)
SA (4)
FREQ@
FREQ1
SA (3)
SA (2)
SA (1)
SA (@)
RESET4@
@WS*
IOCHCK*
POWERGOOD*
NMI
MEMCS16*
RESET2*
TMRGATE
SPKRDATA
REFREQ
INTA*
HLDA1
XMEMR*
XMEMW*
XIOW*
AEN8*
AEN16*
CTPPICS*
AS
ACK*
INTR
TEST
HPNMI
A20GATE
IRQ(13)
PFAIL-3@1
MASTER*
SMEMR*
IOR*
SA (22)
SA (20)
SA (18)
SA (16)
SA (14)
SA (13)
SA (11)
SA (9)
SA (7)
SA (5)
SA (4)
SA (3)
SA (1)
@WS*
NMI
TMRGATE
INTA*
XMEMW*
AEN16*
ACK*
HPNMI
XA (@: 2
S
+5V
J24
J17
J18

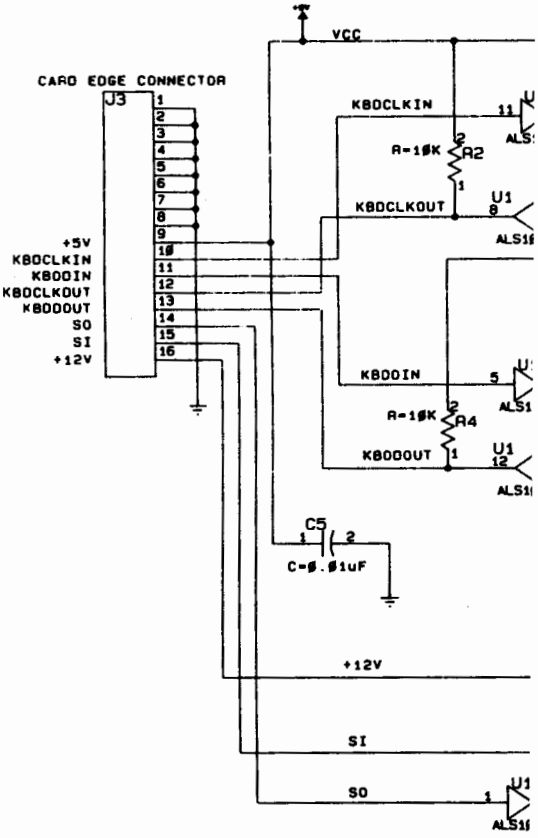


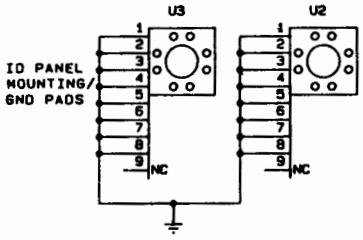
System Interface PCA Schematic

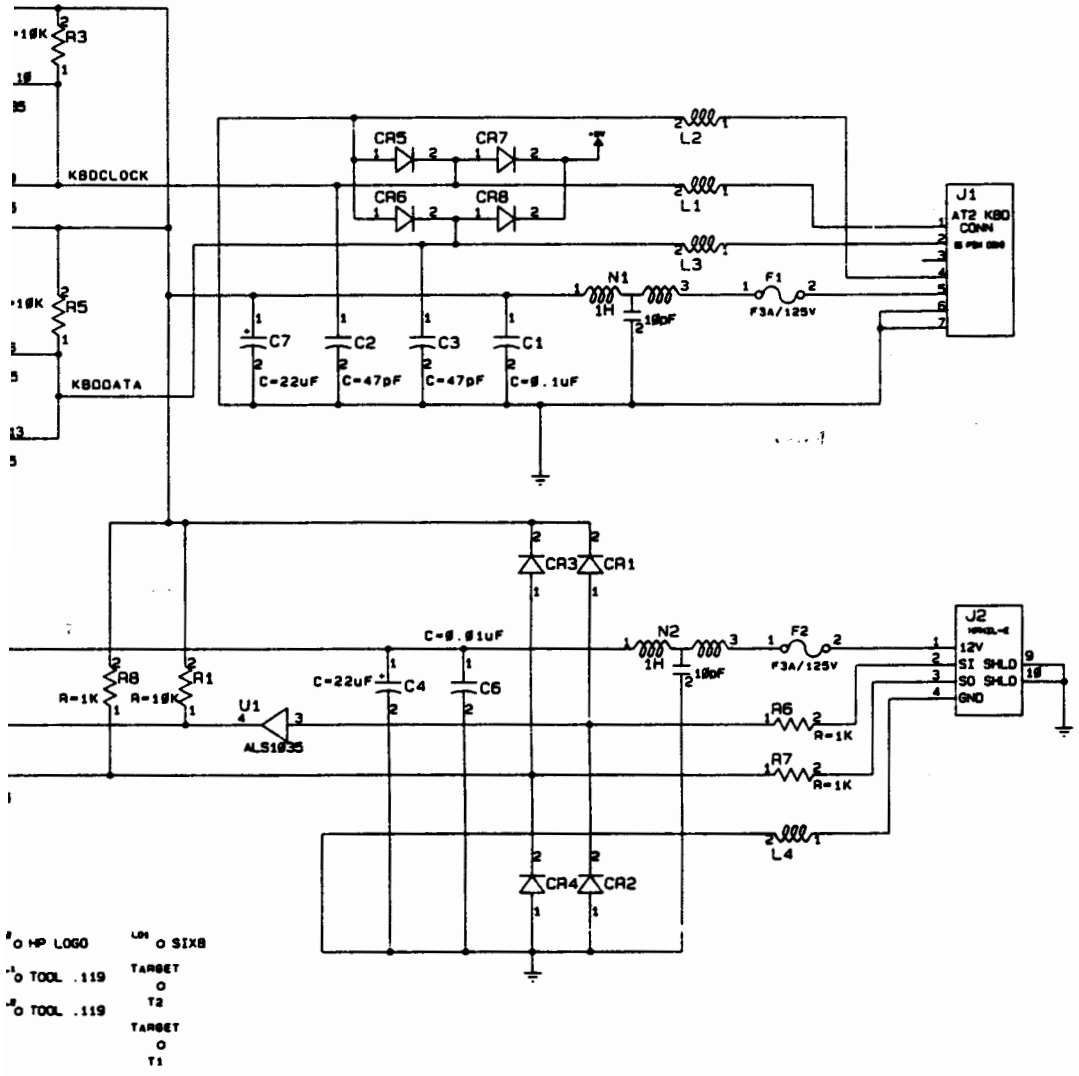

J2Ø
A
B
C
NC
MEM (68)
MEM (69)
MEM (7Ø)
MEM (71)
MEM (72)
MEM (73)
MEM (74)
MEM (Ø)
MEM (1)
MEM (2)
MEM (3)
MEM (4)
MEM (5)
MEM (6)
MEM (7)
MEM (8)
MEM (9)
MEM (1Ø)
MEM (11)
MEM (12)
MEM (13)
MEM (14)
MEM (15)
MEM (16)
MEM (75)
MEM (76)
MEM (77)
MEM (78)
MEM (79)
MEM (8Ø)
MEM (81)
MEM (82)
MEM (83)
MEM (84)
MEM (85)
MEM (86)
MEM (87)
MEM (88)
MEM (89)
MEM (9Ø)
MEM (17)
MEM (18)
MEM (19)
MEM (2Ø)
MEM (21)
MEM (22)
MEM (23)
MEM (24)
MEM (25)
MEM (26)
MEM (27)
MEM (28)
MEM (29)
MEM (3Ø)
MEM (31)
MEM (32)
MEM (33)
MEM (34)
MEM (35)
MEM (36)
MEM (37)
MEM (38)
MEM (39)
MEM (4Ø)
MEM (41)
MEM (42)
MEM (43)
MEM (44)
MEM (45)
MEM (46)
MEM (47)
MEM (48)
MEM (49)
MEM (5Ø)
MEM (91)
MEM (92)
MEM (93)
MEM (94)
MEM (95)
MEM (96)
MEM (97)
MEM (98)
MEM (51)
MEM (52)
MEM (53)
MEM (54)
MEM (55)
MEM (56)
MEM (57)
MEM (58)
MEM (59)
MEM (6Ø)
MEM (61)
MEM (62)
MEM (63)
MEM (64)
MEM (65)
MEM (66)
MEM (67)
MEM (Ø: 98)
P4/J23



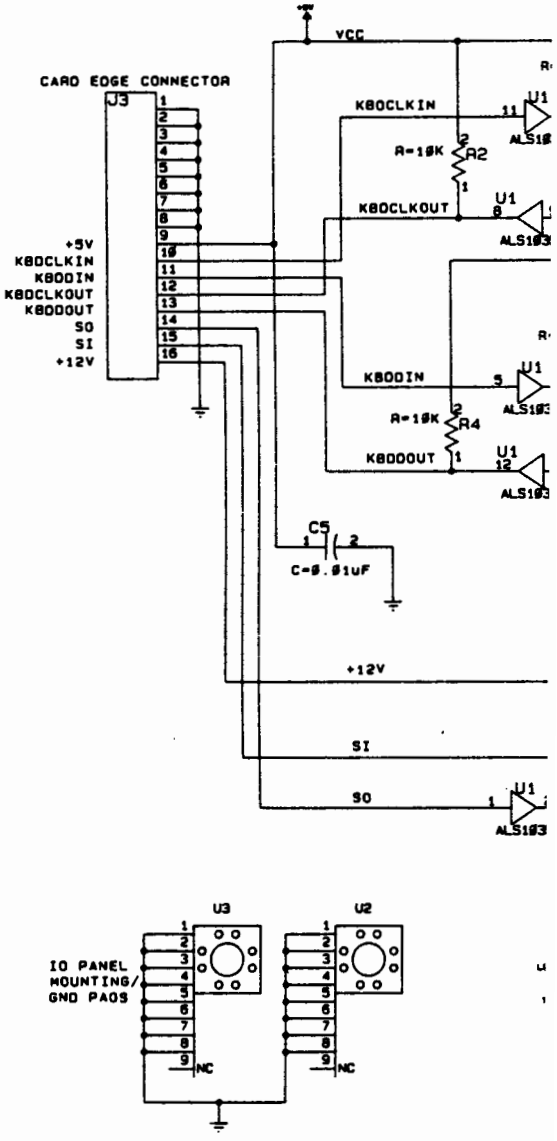
System Interface PCA Schematic


VCC
CARD EDGE CONNECTOR
J3
KBDCLKIN
R=1ØK
R2
KBDCLKOUT
U1
+5V
KBDCLKIN
KBDDIN
KBDCLKOUT
KBDDOUT
SO
SI
+12V
KBDDIN
R=1ØK
R4
KBDDOUT
C5
C=Ø.Ø1uF
+12V
SI
SO
ALS1
NC


U3
U2
ID PANEL
MOUNTING/
GND PADS
NC
NC



Input Device Connector PCA Schematic


VCC
CARD EDGE CONNECTOR
J3
K8OCLKIN
R=1ØK
R2
K8OCLKOUT
U1
ALS1Ø3
+5V
K8OCLKIN
K8OIN
K8OCLKOUT
K8OOOUT
SO
SI
+12V
K8OOIN
R=1ØK
R4
K8OOOUT
C5
C=Ø.Ø1uF
+12V
SI
SO
U3
U2
IO PANEL
MOUNTING/
GND PADS
NC

4

POWER SUPPLY

4.1 Introduction

This chapter describes the HP Vectra RS power supply, the major components of which are given in Table 4-1. (Specifications for the power supply are given in the "System Overview" chapter.)

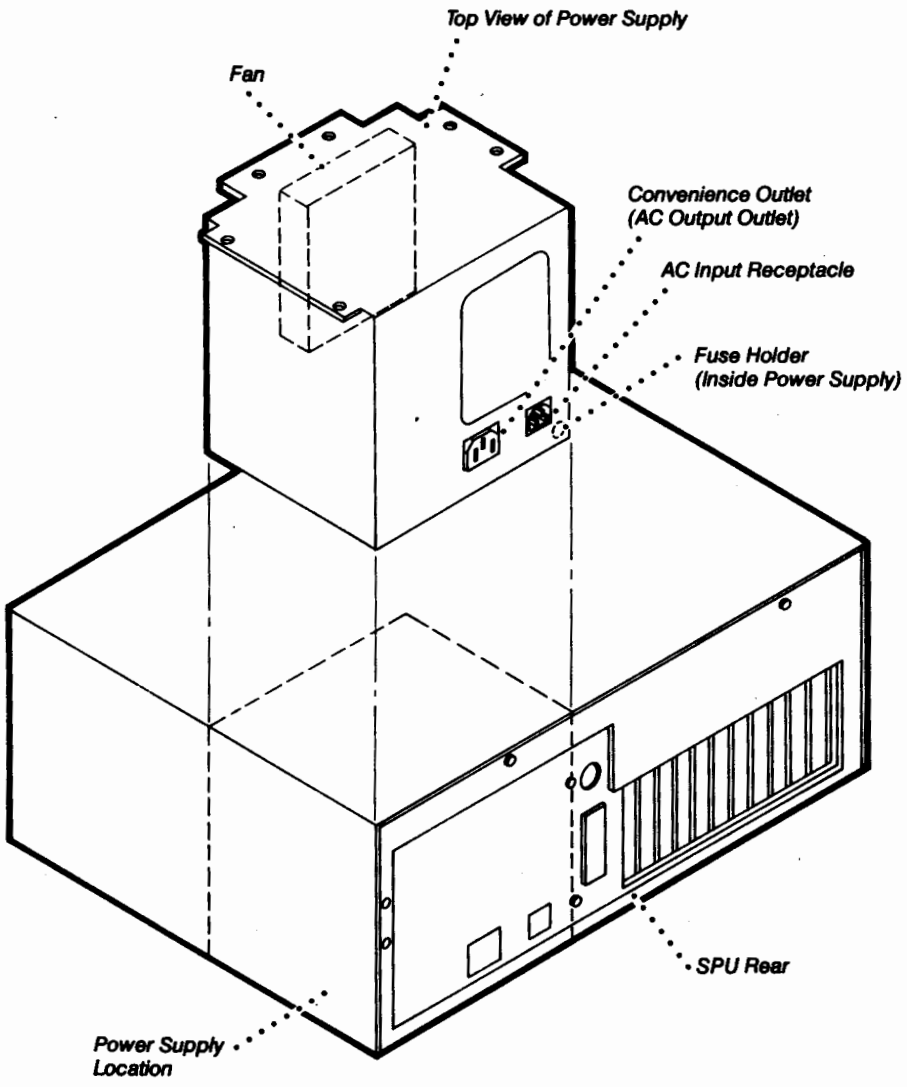
Table 4-1. Major Power Supply Components

AC input receptacle
Convenience outlet (AC output outlet)
Fan
Fuse and fuse holder
On/off switch
Power cables to disc drives
Power connector to System Interface PCA

As shown in Figure 4-1, the power supply is installed in a zinc-plated steel enclosure, located inside the HP Vectra RS system processing unit (SPU). The power supply provides power to the components given in Table 4-2. Through the convenience outlet (also known as the AC output outlet), the power supply can provide AC power to the monitor. (However, in the United States, the EGA and VGA monitors plug into the wall socket only; in Europe, the convenience outlet may be used).

Table 4-2. Components Receiving Power from Power Supply

Backplane I/O
Flexible disc drives
Hard disc drives
Keyboard and other input devices
Printed circuit assemblies
Tape backup drives



Notes :

1. *Monitor can plug into convenience outlet or AC wall socket.*
2. *In U.S., EGA and VGA monitors plug into AC wall socket only. In Europe, the convenience outlet may be used for the EGA monitor.*
3. *Fuse is not a user-replaceable item.*

Figure 4-1 (a) Power Supply Components (Excluding On/Off Switch, Power Cables, and Power Connector)

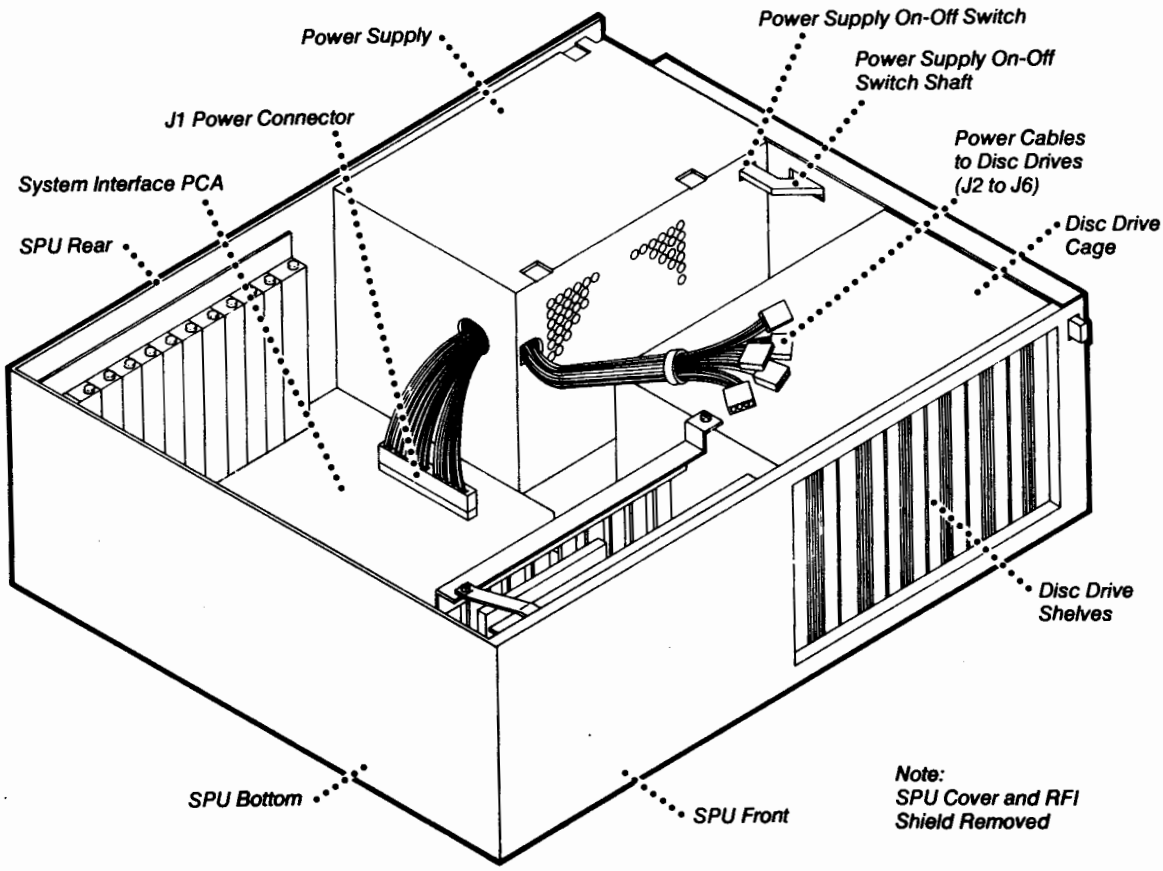


Figure 4-1 (b) Power Supply Component (Including On/Off Switch, Power Cables, and Power Connector)

4.2 Power Supply Line Input

The auto-ranging, world-wide power supply senses the line voltage and frequency and automatically configures itself to operate with one of the two configuration voltages given in Table 4-3.

Table 4-3. Power Supply Voltages

Line Voltage	Line Frequency	Configuration Voltage
90 to 132 VAC	47 to 63 Hz	115 VAC
198 to 264 VAC	47 to 63 Hz	230 VAC

4.3 Power Supply Output

Via the System Interface PCA connector J1, the power supply provides +/- 5 Vdc and +/- 12 Vdc outputs to the System Interface PCA and to the Processor/Memory PCA (via System Interface PCA card edge connectors). Through connector J1, the power supply also provides the PFAIL signal discussed in this chapter's section, "Power Supply Operating Status Indicator."

Through the five identical power cables J2 through J6, shown in Figure 4-1(b), the power supply provides +5 Vdc and +12 Vdc outputs to disc drive devices, according to their power needs. In addition, on the rear of the SPU, as shown in Figure 4-1 (a), the power supply provides the convenience outlet, an AC output outlet which can supply power of up to 150 watts.

Figure 4-2 gives the pinouts for the power supply connectors and cables. Table 4-4 gives the pin assignments per pin. Table 4-5 gives the power supply's output at power-up and 30 seconds after power-up.

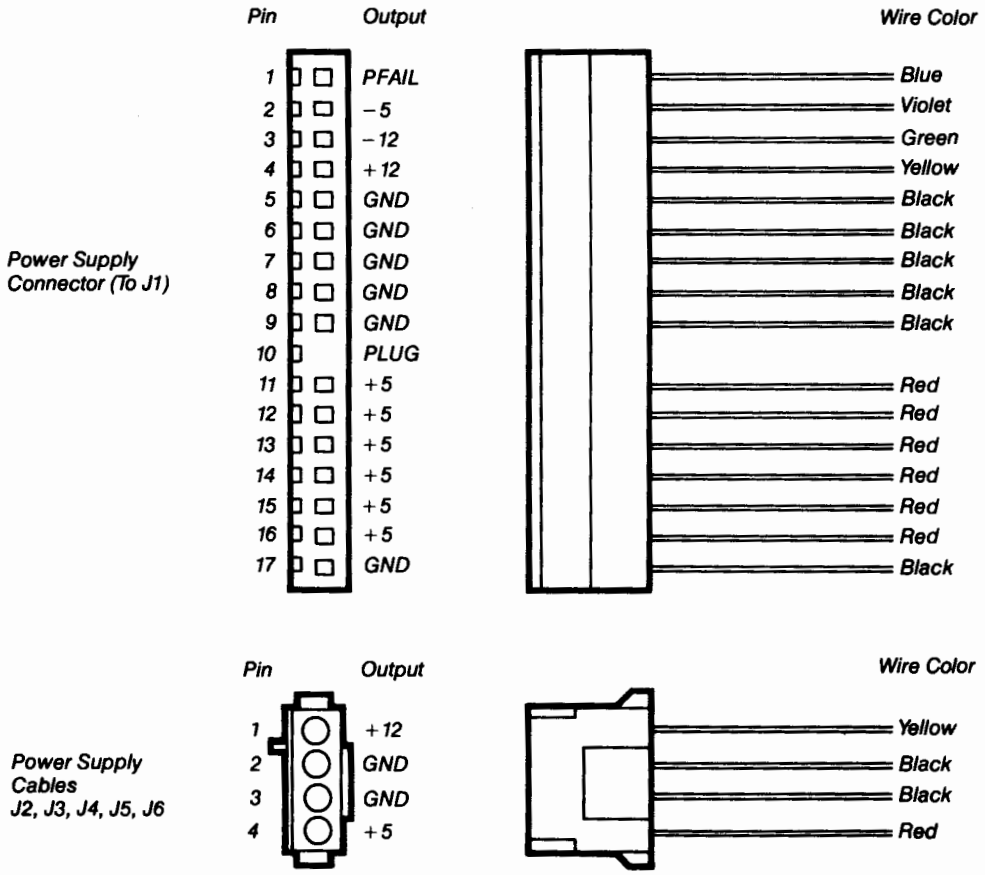


Figure 4-2 Power Supply Connector and Cable Pinouts

Table 4-4 (a). Pin Assignments for Power Supply Connector J1 (To System Interface PCA)

J1 Pins	Vdc Output	Maximum Current Drawn (Per Pin)
1 (Gold Pin)	PFAIL (*)	(*)
2	-5 Vdc	0.3 Amps
3	-12 Vdc	0.3 Amps
4	+12 Vdc	1.7 Amps
5-9	Ground	–
10	No connect	
11-16	+5 Vdc	3.3 Amps
17	Ground	–

*Refer to the section in this chapter, "Power Supply Operating Status Indicator."

Table 4-4 (b). Pin Assignments for Power Supply Cables J2 to J6 (To Disc Drives)

J2 to J6 Pins	Vdc Output	Maximum Current Drawn (Per Pin)*
1	+12 Vdc	5 Amps
2,3	Ground	–
4	+5 Vdc	2 Amps

* Note: During power-up, power supply cables J2 through J6 can draw a total maximum current of 15.5 Amps on the +12 Vdc power supply and 4.2 Amps on the + 5 Vdc power supply.

Table 4-5. Power Supply Rated Output at Power-up and After Power-up

Nominal DC Voltage Output from Power Supply	Voltage Range (Vdc) At Power-up and 30 Seconds After Start-up	Minimum Current (DC Amps) At Power-up and 30 Seconds After Start-up	Maximum Current (DC Amps)		Maximum Voltage Ripple (mV p-p) At Power-up and 30 Seconds After Start-up	Total Power (Watts)	
			At Start-up	30 Seconds After Start-up		At Start-up	30 Seconds After Start-up
+5	+4.85 to +5.25	2.0	24.0	21.0	50		
+12	+11.6 to +12.6	0.0	17.2	7.4	100		
−5	−5.25 to −4.75	0.0	0.3	0.3	50		
−12	−12.6 to −11.4	0.0	0.3	0.3	120		
						10 watts minimum to 332 watts maximum	10 watts minimum to 200 watts maximum

Power to Backplane I/O

Each of the +5 Vdc backplane I/O connector slots can support an average of eight watts per channel. Table 4-6 and 4-7 give the voltage for the backplane I/O connector slots, the maximum total current for the backplane I/O connector slots, and the average current per backplane I/O connector slot.

Table 4-6. Power to RS/16 and RS/20 Backplane I/O Connector Slots

Backplane I/O Voltage	Maximum Total Current for Slots	Average / Slot
+ 5 Vdc	10.6 Amps	1.3 Amps
+12 Vdc	0.5 Amps	0.06 Amps
- 5 Vdc	0.3 Amps	0.03 Amps
-12 Vdc	0.3 Amps	0.03 Amps

Table 4-7. Power to RS/20C and RS/25C Backplane I/O Connector Slots

Backplane I/O Voltage	Maximum Total Current for Slots	Average / Slot
+ 5 Vdc	7.6 Amps	0.95 Amps
+12 Vdc	0.5 Amps	0.06 Amps
- 5 Vdc	0.3 Amps	0.03 Amps
-12 Vdc	0.3 Amps	0.03 Amps

4.4 Power Supply Protection

Line Dropout Protection

Under any condition, including low line power at rated load, the power supply will continue to deliver regulated outputs when a 20 millisecond power line dropout occurs at the input to the power supply.

AC Inrush Current Protection

Under any condition, AC inrush current for the power supply is limited to 40 amps and shall not open the power supply's fuse. (Under any condition, the AC inrush current for the convenience outlet, an AC output outlet on the rear of the SPU, is 30 amps.)

Undercurrent Protection

Any or all power supply outputs may be open without damage to the power supply. (For the +5 Vdc power supply to operate normally, the minimum load is 2 amps.)

Overcurrent Protection

When there exists an overcurrent situation (i.e., a short circuit occurs on the +5 or +12 Vdc outputs), the power supply turns off. To start the power supply again, depress the power supply's ON/OFF switch to the off position, remove the fault, and then turn on the power supply. (The -5 and -12 Vdc outputs are internally protected against a maximum short circuit current of 0.5 amps, and if a short circuit does occur, the power supply does not turn off.)

Overvoltage Protection

Table 4-8 gives the voltage levels which cause a power supply overvoltage situation. If overvoltage occurs on the +5 or +12 Vdc line, within 500 microseconds, the power supply's switch controller turns off all the power supply outputs. To start the power supply again, depress the power supply's ON/OFF switch to the off position, remove the fault, and then turn on the power supply.

If overvoltage occurs on the -5 or -12 Vdc line, the +5 and +12 Vdc outputs will not turn off, as the -5 and -12 Vdc outputs are internally protected to a maximum short circuit current of approximately 0.5 amps. (When the cause of the overvoltage situation is removed, the -5 or - 12 Vdc outputs return to normal operation.)

Table 4-8. Voltage Levels Which Cause Power Supply Overvoltage

Nominal Power Supply Voltage	Maximum Over-Voltage Level
+ 5 Vdc	+ 7 Vdc
+12 Vdc	+17 Vdc
- 5 Vdc	*
-12 Vdc	*

*Inherent overvoltage protection at any voltage level.

Fuse and Fuse Holder

To protect the HP Vectra RS from overvoltage and overcurrent, the power supply has a fuse, rated at eight amps. (The power supply must be removed from the SPU to remove the fuse from the fuse holder, which is inside the power supply, next to the AC input receptacle. The fuse is not a user-replaceable item.)

Fan

The RS/16 and RS/20 SPUs have two fans; the RS/20C and RS/25C SPUs have three fans. All models have a power supply fan to provide at least 52 cubic feet of air per minute to cool the power supply and disc drives. Also, all models have a system fan, provided by the SPU, which cools the printed circuit assemblies. The Vectra RS/20C and RS/25C models have a Cache Memory System PCA, which has its own fan to cool itself.

4.5 Power Supply Operating Status Indicator

The PFAIL signal (pin 1 of the J1 power connector) indicates the power supply's operating status. If the power supply is operating properly, within 100 milliseconds after the +5 Vdc output has reached its minimum sense level, the PFAIL signal goes low to indicate proper power supply operation. If the power supply is not operating properly, the PFAIL signal goes high.

When the AC input voltage either has been removed or has dropped to an insufficient level, the rising edge of the PFAIL signal indicates to the real-time clock and CMOS RAM to go into a power-down mode and operate from the system's battery. When the AC input voltage is replaced or is once again at a sufficient level, PFAIL generates a system reset signal via an interrupt control. Figure 4-3 gives the PFAIL timing diagram.

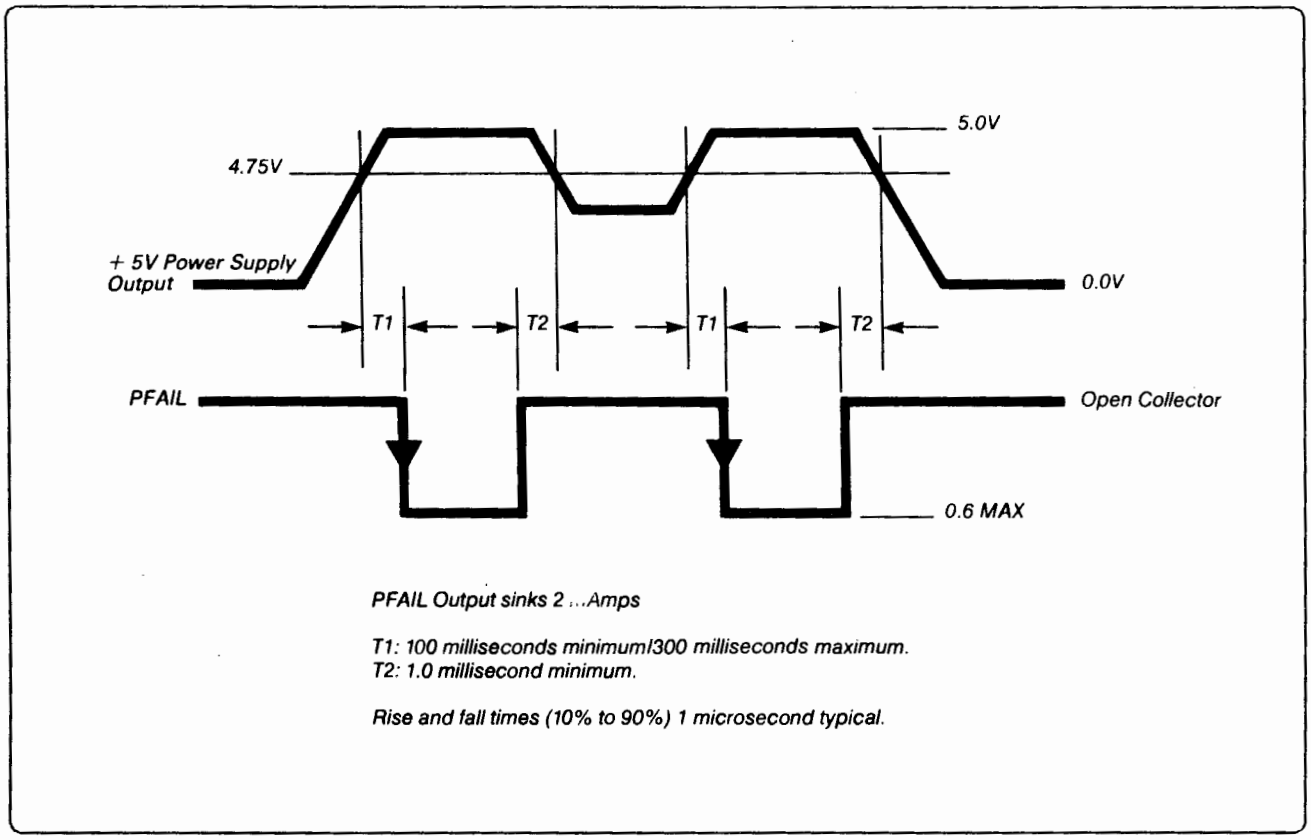


Figure 4-3 PFAIL Timing Diagram

4.6 Battery Power

A system backup battery, located on the System Interface PCA, provides power to the real-time clock and CMOS RAM during power-down and power system failure. The 6-volt lithium battery has an average life of 2.3 years.

GLOSSARY

AAA

Accessory Card - A circuit board containing electronic circuitry that interfaces a peripheral to the system processor board.

Active Low - Signal that must go low to produce an effect. (Same as negative true.)

Adapter - See Accessory Card.

Address Bus - A circuit that carries a binary-coded address from the 80386 microprocessor to other parts of the system.

Application Software - Software that performs application-specific tasks; examples include word processing packages, spreadsheets, and data bases.

Asynchronous Transmission - A mode of transmitting signals, the start time for which is arbitrary, but the time relationship between signals is fixed.

B

Barcode Reader - An input device that is used to scan surfaces having barcodes. The barcode reader converts barcodes into scan code data format, and transmits the scan code to an input interface.

Base RAM - The first 640 Kbytes or 512 Kbytes of main memory (depending on the HP Vectra RS PC configuration). Used for MS-DOS applications.

BIOS - Basic Input/Output System. The BIOS is the code module that contains the drivers that constitute the software interface between the hardware, and the system software and application software.

Bisynchronous - Binary Synchronous. A mode of transmission in which binary characters are synchronized via control signals.

Bits Per Second - A unit of measure; the rate at which a device transmits characters serially.

Block - A group of characters or words treated as a unit.

Boot - The process of initializing the system and loading system software after a reset.

Break Code - The code that is sent by the keyboard to the keyboard controller when a key is released, after having been pressed. For most, but not all keys, the break code consists of hex F0, followed by the key's make code.

BTU - British Thermal Units. A measure of heat.

Buffer - (1) A unit that serves as an interface between dissimilar elements or (2) a register that temporarily holds input or output data.

Bus - A circuit that transmits data or power.

GLOSSARY

C

cache memory - Memory that stores a copy of frequently accessed code and data from main memory in order to increase processing speed.

CAS - Column Address Strobe. A signal that latches a column address into memory.

Central Processing Unit - As used in this manual, the 80386 microprocessor.

Channel - A path for sending signals and data.

Character - A word returned by the keyboard driver indicating a key stroke. The code for a character consists of a keyboard scan code, and either an Extended character (00h) or a character in ASCII (the American Standard Code for Information Interchange.

Checksum - An error-checking protocol used to verify the integrity of a block of data or code. Each byte or word in the block is summed, and then added to a Checksum Byte. The block of data or code is presumed valid if this sum equals a predefined value, usually 0.

Checksum Byte - A byte added to the sum of a block of code or data to produce a valid sum.

CMOS - Complementary metal-oxide semiconductor, a type of technology that uses integrated field-effect transistors in a complementary, symmetrical arrangement.

CMOS RAM - Random-access memory that is powered by either the system power supply or a battery. When the system power is turned off, the contents of the CMOS RAM are preserved by the battery.

Code Segment - The segment address of the code module currently being executed.

Coprocessor - An add-on processor that works with the 80386 microprocessor, providing the hardware to perform numeric functions otherwise performed in software.

CPU - Central Processing Unit (the 80386 microprocessor).

Cursor Control Keypad - The keypad in between the typewriter keypad and the numeric keypad, which controls the position of the cursor.

GLOSSARY

D

Daisy Chain - A method of linking devices together in a serial configuration. If more than one HP-Human Interface Link (HP-HIL) input device is used, they are connected in a daisy chain.

Device - A physical piece of hardware, for example a mouse, keyboard, or printer.

DIN - Acronym for Deutsche Industrie Normenausschuss, a West German association that determines electrical standards. A DIN connector meets the DIN specifications.

Direct-Memory Access - A method for I/O devices to obtain direct access to the main memory, in order to transfer data, without involving the central processing unit.

Divide-By-Zero Interrupt - The 80386 microprocessor executes this interrupt any time a divide-by-zero operation is attempted.

DMA - See Direct-Memory Access.

DOS - Disc Operating System. The software that provides an interface between the hardware, the applications programs, and user-issued commands.

DRAM - See Dynamic RAM.

DREQ - Direct-memory access request.

Driver - (1) A physical device used to control other circuits. (2) A program, accessed by interrupt vectors, that executes other programs to perform specific functions, which may be divided into subfunctions.

Dynamic RAM - Dynamic Random-Access Memory. (Also known as Main Memory, Memory, RAM, System Memory, or System RAM. Not to be confused with CMOS RAM.) Dynamic RAM uses transistors and capacitors, the latter which must be recharged (refreshed).

GLOSSARY

E

EGA - Acronym for Enhanced Graphics Adapter.

EPROM - Erasable Programmable Read-Only Memory. The devices used to store (and erase, if necessary) the industry-standard BIOS code and the HP extensions to the BIOS code.

EX-BIOS - Extended BIOS. A set of proprietary HP drivers that provide support for various system features.

F

Fixed Disc Drive - See Hard Disc Drive.

Flexible Disc Drive - Synonymous with floppy disc drive. A unit with a removable magnetic disc for storing and retrieving data.

Function Keys - The twelve industry-standard keys labeled F1 through F12 on the keyboard.

Functions - Code modules within a driver that perform specific tasks. Individual driver functions are selected when a driver is called.

G

Gate - A combinational logic circuit with one or more input channels and one output channel. The output is determined by the state of the input channels.

Gigabyte - One thousand megabytes, or one million kilobytes.

Graphic Input Device - An input device that generates positional and/or button state data. A mouse, and tablet, are examples of graphic input devices.

Graphics Tablet - A graphic input device that includes a electronic tablet and pen that feed figures or text into the computer. When the graphics pen touches the graphics tablet, a detector registers the coordinates of that point. These coordinates, encoded into binary, generate pulses that are sent to the computer.

GLOSSARY

H

Hard Disc Drive - Synonymous with fixed disc drive. A unit with a non-removable magnetic disc for storing and retrieving data.

Hardware Interrupts - Requests for interrupt service, generated by the hardware components.

Hex - Hexadecimal numbers. Hex numbers represent binary data; they are expressed in base 16 and are represented with numbers 0 to 9 and letters A to F. Throughout this manual, hex numbers are indicated with an lower-case h as their last character (i.e., 17h).

HP-Human Interface Link (HP-HIL) - The electrical interface and communication protocol utilized to connect HP-HIL input devices.

HP-Human Interface Link Master Link Controller - The hardware that provides the electrical interface to the HP-HIL link and which supervises the communication protocol.

HP-IB - Hewlett-Packard Interface Bus

Hz - Hertz. A unit of frequency equal to one cycle per second.

I

Industry-Standard - Compatible with IBM AT personal computers.

Instruction Pointer - The offset from the base of the code segment of the next instruction to be executed.

Instruction Set - A structured set of instructions that concern characters and program definitions, transferred to the computer as operations are executed.

Interrupt of 80386 Microprocessor - A signal which temporarily suspends the 80386 microprocessor's normal execution of a routine, in response to error conditions or processor exceptions.

Interrupt Service Routine (ISR) - Consists of a code module (a group of related instructions for the 80386 microprocessor) and the code module's associated data structure(s), (a related group of data fields) that respond to a hardware interrupt.

Interrupt Vector - A data structure (related group of data fields) used by the 80386 microprocessor to branch to a service routine or an interrupt. Interrupt vectors are located in the first 1024 bytes of system memory. Each interrupt vector occupies two words of memory and includes the interrupt service routine's instruction pointer and code segment.

IPC - The 82C206 Integrated Peripheral Controller.

ISR - Interrupt Service Routine.

GLOSSARY

K

Kbyte - A Kilobyte, a measurement of the physical storage capacity. One Kilobyte equals 1,024 bytes.

Keyboard - The physical keyboard.

Keyboard Controller - The 8042 keyboard controller. The 8042 provides industry-standard keyboard compatibility, and serves as a buffer between the STD-BIOS keyboard drivers and the Input System.

Keylock - (1) The lock on the front of the HP Vectra RS PC's System Processing Unit, which when locked, inhibits inputs from the keyboard or other input devices. (2) The lock on the SPU's back, which prevents the SPU unit cover from being removed.

L

LA - Local Address bus.

LD - Local Data bus.

LED - Light-emitting diode. A semiconductor device that is lit when activated.

GLOSSARY

M

MA - Memory Address bus.

Main Memory - See Dynamic RAM.

Make Code - The code that is sent by the keyboard to the system's keyboard controller when a key is pressed.

Mask - A mask consists of characters that retain or eliminate bits comprising a string (i.e., a set of records) that is stored in memory.

Mbyte - A measurement of the physical storage capacity. One Megabyte equals 1,048,576 bytes, or 1,000 kilobytes. (See Kbyte).

MD - Memory Data bus.

Memory - Main Memory. (See Dynamic RAM.)

Microprocessor - A control unit that accepts a defined set of instructions for execution.

MLC - Master Link Controller.

Mode-Indicator LEDs - The LEDs located on the keyboard that indicate the state of the <Caps lock>, <Num lock>, and <Scroll lock> keyboard modifiers.

Mouse - A graphic input device that reports relative motion coordinates based on its motion. A mouse will also report the state of its buttons.

MS-DOS - See DOS.

Multiplex - The simultaneous transmission of two of more information streams over the same channel.

Multi-Tasking - The ability of a system microprocessor (such as the 80386) to perform multiple tasks nearly simultaneously. By task-switching (quickly dividing the microprocessor's execution time between different tasks), the illusion of simultaneous execution occurs.

GLOSSARY

N

NMI - Non-maskable interrupt, an 80386 interrupt line used to report system error conditions. This interrupt is mapped by the 80386 microprocessor to interrupt vector 02h.

Numeric Keypad - The keypad on the far right of the keyboard, that has keys with numbers and symbols. The numeric keypad can be used for numeric entries only when the <Num Lock> key has been pressed and the <Num Lock> mode-indicator LED is lit. (Otherwise, this keypad functions the same as the cursor control keypad.)

O

OEM - Acronym for Original Equipment Manufacturer.

Operating System - The system software that provides access to system resources for application programs. The operating system manages input and output, data and program files, and system memory.

P

Page - A block of consecutive-byte memory.

Parallel Port - A system I/O port that transmits and receives data a byte at a time. Parallel ports are typically used to interface to printers.

Parity Bit - In the odd parity system used for the HP Vectra RS PC, a bit added to a group of bits, to make an even number of ones sum up to an odd number.

Parity Check - A method for checking if the total number of ones or zeros in a byte or word is even or odd.

PCA - Printed Circuit Assembly.

Polling - The process of periodically determining the status of a device. Polling is used to determine if peripheral devices have data or are ready to accept data in non-interrupt driven systems.

Port - A point at which an input or output contacts with the central processing unit.

Power-On Self-Test - A self-test process that is executed each time the system is powered on when a hard reset occurs.

Processor - See Central Processing Unit and Microprocessor.

GLOSSARY

R

RAM - Random Access Memory. See Dynamic RAM.

RAS - Row Address Strobe. A signal that latches a row address into memory.

RD - Read-only memory Data bus.

Read-Only Memory (ROM) - Read-only memory is memory the contents of which can not be altered. When power is removed from the system, this memory retains its contents.

Real-Time Clock - A clock circuit that maintains the correct time whether the system is on or off. The real-time clock is powered by either the system power supply or the battery. When the system power is turned off, the clock continues to operate from the battery.

ROM - See Read-Only Memory.

ROM BIOS - The set of EX-BIOS and STD-BIOS drivers. These code modules are contained in ROM modules on the Processor Extension Card.

S

SA - System Address bus.

SBUS - Backplane I/O Bus.

Scan Codes - Codes returned by the keyboard to the 80386 microprocessor to indicate key presses (makes) and releases (breaks).

SD - System Data bus.

SDLC - See Synchronous Data Link Controller.

Serial Port - A system I/O port that transmits data *serially*, i.e., one bit at a time.

Single Step Interrupt - An interrupt of the 80386 microprocessor, generated after each instruction if the Single Step flag is set. This interrupt is mapped by the 80386 to interrupt vector 01h.

Software Interrupt - An interrupt generated by an 80386 INT n instruction, where n is the interrupt number.

SPU - System Processing Unit. The physical container for the system's power supply, disc drives, printed circuit assemblies, etc.

Standard-Cell Chip - A semi-custom-made chip that implements a circuit design that has such components as gates, counters, memory, and sometimes, a microprocessor.

GLOSSARY

S (continued)

STD-BIOS - The set of drivers that execute the industry-standard BIOS functions.

Synchronous Data Link Controller - An industry-standard card/protocol used for linking minicomputers with industry-standard mainframes.

Synchronous Transmission - (1) A mode of transmitting signals, in which each signal has a fixed time frame. (2) The sending of signals at the same frequency and phase relationship.

System Memory - See Dynamic RAM.

System RAM - See Dynamic RAM.

System Software - See Operating System.

T

Timer Tick - An interrupt generated by the system timer.

Typematic - Except for the <Pause> key, all keys are *typematic*; i.e., when a key is pressed and held down, the keyboard continues sending the key's make code to the keyboard controller, repeating the key's function until the key is released.

Typematic Delay - The amount of time a key must be held down, before the keyboard enters the typematic or repeat mode. The typematic delay equals

[(1 + binary value of bits 6 and 5 of the parameter byte) X (250 milliseconds)] +/- 20%

Typematic Rate - The rate (1/period) at which make scan codes are sent by the keyboard when the keyboard is in the typematic, or repeat, mode. The period, the interval from one typematic output to the next, equals

[8 + (the binary value of bits 2, 1, and 0 of the parameter byte)] X

[2 raised to the power of the binary value of bits 4 and 3 of the parameter byte] X

0.00417 seconds

GLOSSARY

V

VGA - Acronym for Video Graphics Adapter.

X

XA - Peripheral Address bus.

XD - Peripheral Data bus.

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