HEWLETT-PACKARD

HP Vectra QS Hardware Technical Reference Manual

(HP Vectra QS/16S, QS/16 and QS/20)

HEWLETT PACKARD

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Hewlett-Packard
Grenoble Personal Computer Division,
5, Avenue Raymond Chanas,
38320 Eybens, France.

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Because the HP Vectra QS PC generates and uses radio frequency energy, it may cause interference with radio and television reception in a residential installation.

Hewlett-Packard provides instructions for using this computer in manuals covering setup, connection of peripheral devices, operation, service, and technical reference.

Installing and using the computer in strict accordance with Hewlett-Packard's instructions will minimize the chances that the HP Vectra QS PC will cause radio or television interference. However, Hewlett-Packard does not guarantee that the computer will not interfere with radio or television reception.

If you think the computer is causing interference, turn it off to see if radio or television reception improves. If the reception improves, the computer is causing the problem.

To correct interference, take one or more of the following steps:

- Relocate the radio or television antenna
- Move the computer away from the radio or television
- Plug the computer into a different electrical outlet, so that the computer and the radio or television are on separate electrical circuits
- Make sure that all of your peripheral devices are certified Class B by the FCC
- Make sure that you use only shielded cables to connect peripheral devices to your computer
- Consult your computer dealer, Hewlett-Packard, or an experienced radio/television technician for other suggestions.

Electrical Safety

Warning

For user safety, the power cords supplied with this product have grounded plugs. The power cord should be used with properly grounded (3-hole) wall outlets to avoid electrical shock. (You can also use multiple-outlet strips that have their own circuit breakers.)

INTRODUCTION

Audience

This manual is intended to help original equipment manufacturers, independent hardware vendors, and independent software vendors in their design efforts.

Scope of Manual

Chapter 1 gives a system overview of the Hewlett-Packard Vectra QS Personal Computer.

Chapter 2 discusses the QS/16 and QS/20 Processor/Memory PCA components.

Chapter 3 discusses the QS/16S Processor/Memory PCA components.

Chapter 4 discusses the System Interface PCA components.

Chapter 5 discusses the Power Supply.

Schematics and a Glossary of terms are also included.

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System Overview

1.1 INTRODUCTION

This manual provides information on the Hewlett-Packard Vectra QS/16, QS/20 and QS/16S Personal Computers. The manual refers to these computers using the generic name "HP Vectra QS". Where specific differences occur between the computers, these differences are explained in the text.

This chapter gives an overview of the Hewlett-Packard Vectra QS Personal Computer. It includes system configurations, architecture, and specifications, along with references used in writing this manual.

1.1.1 Users

The HP Vectra QS is a high-performance, industry-standard, desk-top personal computer. The Vectra QS/16 and QS/20 are based on the Intel 80386 microprocessor running at 16 MHz and 20 MHz respectively. The Vectra QS/16S is based on the Intel 80386SX microprocessor running at 16 MHz.

The HP Vectra QS PC is geared towards users with demanding, computation-intensive tasks requiring great power and fast response time. Typical uses include the following:

Computer-Aided Design/Engineering/Manufacturing
Database Management
Desktop Publishing
Local-Area Network Servers

1.1.2 Features

The HP Vectra QS PC has the following features:

80386 microprocessor (QS/16 and QS/20)
80386SX microprocessor (QS/16S)
Socket for numeric coprocessor
System RAM. QS/16 and QS/20: 1 Mbyte of 32-bit RAM, expandable up to 16 Mbytes. QS/16S: 1 Mbyte of 16-bit RAM, expandable up to 8 Mbytes.
Backplane I/O connector slots for up to 7 industry-standard accessory cards
Disc caching
9-pin serial port and 25-pin parallel port
Flexible disc controller and drive
Hard disc controller and drive
Support for up to 3 mass storage devices
Industry-standard keyboard
Support for up to 7 HP-Human Interface Link input devices

1.1.3 Compatibility

The HP Vectra QS PC is designed to be 100% compatible with the industry-standard IBM PC/AT II personal computer and with the HP Vectra family of personal computers.

It offers downward compatibility, running industry-standard operating systems (including MS-DOS 3.2, MS-DOS 3.3, Microsoft OS/2, and Windows 2.0) and industry-standard application software developed for systems based on 8088, 8086, or 80286 microprocessors. It also offers upward compatibility in that it is designed to run Windows/386 and operating systems and applications based on the 80386 microprocessor.

1.1.4 QS/16 Versus QS/20 Versus QS/16S

Table 1-1 lists the differences between the QS/16, QS/20 and QS/16S.

Table 1-1. Differences Between the QS/16, QS/20 and QS/16S

Component	QS/16	QS/20	QS/16S
Processor	80386 @ 16 MHz	80386 @ 20 MHz	80386SX at 16 MHz
Processor clock	32 MHz	40 MHz	32 MHz
Bus controller	82C301 @ 16 MHz	82C301 @ 20 MHz	82C211 @ 16 MHz
Control buffer	82C306	82C306	
Page memory controller	82C302 @ 16 MHz	82C302 @ 20 MHz	82C212 @ 16 MHz
Address buffer	82C303 & 82C304	82C303 & 82C304	82C215
Data buffer	82A305	82B305	
Memory modules	100 ns, max 16 MB	80 ns, max 16 MB	100 ns, max 8 MB

In addition, the Processor/Memory PCA "Switch 1" default settings (see Chapter 2 and 3) and BIOS are different.

80386 Versus 80386SX

Both the 80386SX and the 80386 are 32-bit microprocessors, however:

- The 80386SX has a 16-bit external data bus, compared to 32 bits on the 80386. This means bus access is slower for 32-bit instructions.
- The 80386SX has a 24-bit external address bus, compared to 32 bits on the 80386. This means the 80386SX has a physical memory address space of 16 Mbytes compared with 4 gigabytes on the 80386.

In addition, the QS/16S coprocessor is selected using address line A23. On the QS/16 and QS/20, the coprocessor is selected using address line A31.

1.2 SYSTEM CONFIGURATIONS

1.2.1 Basic Configuration

Figure 1-1 shows the basic configuration of the HP Vectra QS PC System Processing Unit (SPU):

- a power supply
- the System Interface PCA (printed circuit assembly) with seven backplane I/O (PCA) slots
- two other main PCAs (the Processor/Memory PCA and the Four-Function Controller PCA), that plug into the System Interface PCA
- one hard and one flexible disc drive.

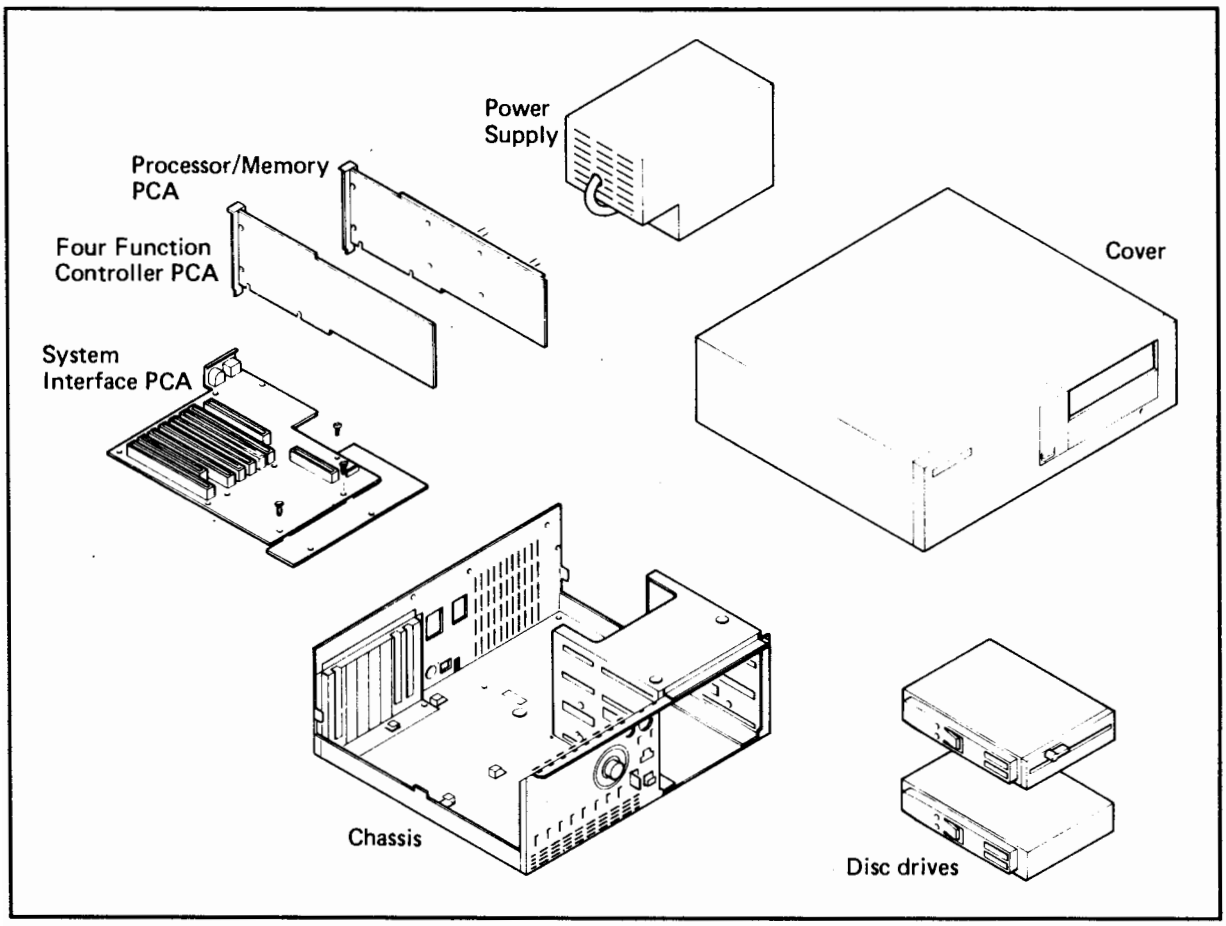

Figure 1-1. Basic Configuration of HP Vectra QS Personal Computer System Processing Unit

1.2.2 Configuration Options

The HP Vectra QS PC comes in several models. Refer to the product data sheet for complete details.

1.3 SYSTEM ARCHITECTURE OVERVIEW

This section gives an overview of the HP Vectra QS PC system architecture.

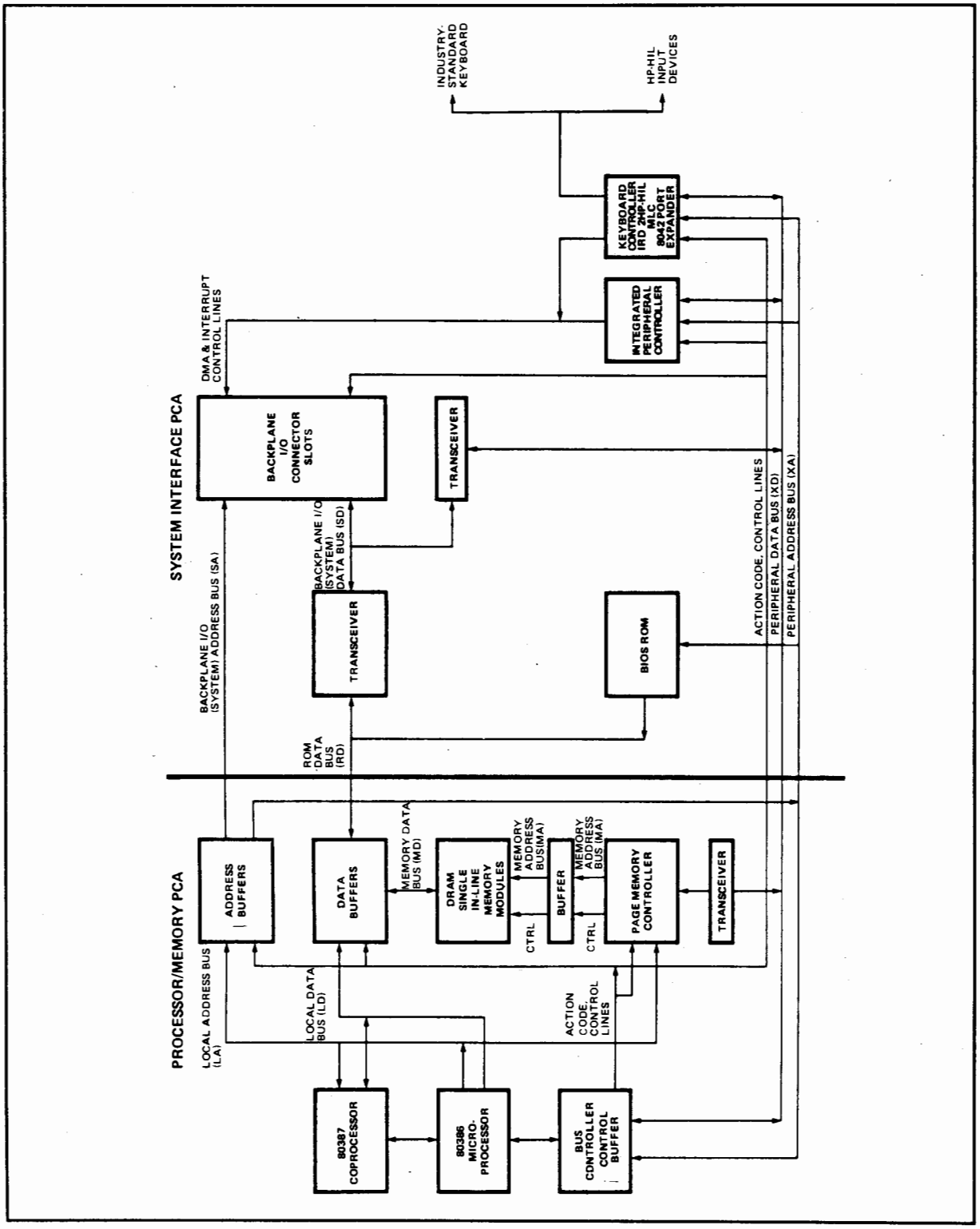

Figure 1-2. HP Vectra QS/16 & QS/20 System Architecture

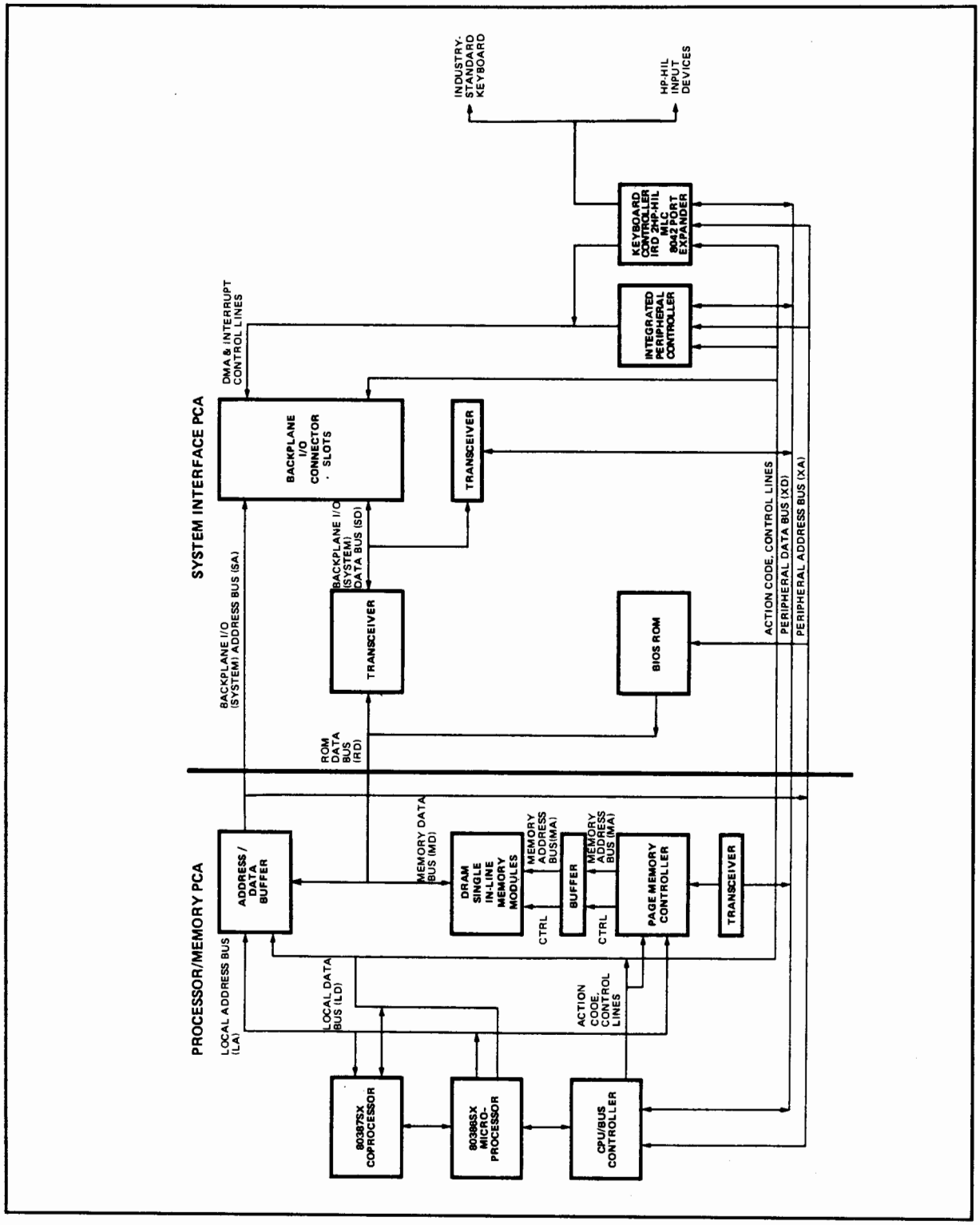

Figure 1-3. HP Vectra QS/16S System Architecture

1.3.1 Hardware

Power Supply. The power supply provides 134 watts of continuous power (176 watts peak).

Backplane I/O. The backplane I/O consists of one 8-bit and six 16-bit I/O connector slots for industry-standard accessory cards operating at 8 MHz (or at 10 MHz on the QS/20).

Real-Time Clock/CMOS RAM. The real-time clock/calendar includes 114 bytes of CMOS RAM. A 6-Volt lithium battery provides power to the real-time clock/CMOS RAM during power-down and power failures.

System Microprocessor. The HP Vectra QS/16 and QS/20 PCs are based on the 32-bit 80386 microprocessor. The QS/16 uses a clock rate of 16-MHz, and the QS/20 uses 20-MHz. The HP Vectra QS/16S is based on the 32-bit, 16 MHz 80386SX microprocessor.

The keyboard can be used to switch the clock rate to 8 MHz.

Coprocessor. The HP Vectra QS supplies a socket for a numeric coprocessor: 80387 on the QS/16 and QS/20, 80387SX on the QS/16S.

The QS/16S coprocessor operates synchronously with the processor clock.

On the QS/16 and QS/20, the coprocessor operates either synchronously with the processor clock or asynchronously, switch selectable (via setting 6 on the Processor/Memory PCA's Switch 1).

Monitor. Both monochrome and color monitors are available, along with accessory cards for the monitors.

Security Lock. The HP Vectra QS PC has an optional security lock that can be fitted to the front of the SPU. It prevents inputs from the keyboard and other devices and also secures the SPU unit cover.

Keyboard. The HP Vectra PC Keyboard is a detachable, 101-key (USASCII) or 102-key (national), industry-standard keyboard. It has separate numeric and cursor control keypads and an industry-standard DIN cable connector.

Hewlett-Packard Human Interface Link Devices. The HP Vectra QS PC has an HP-HIL port which allows up to seven HP-HIL devices (such as a mouse, graphics tablet, and barcode reader) to be operated simultaneously.

Four-Function Controller PCA. The Four-Function Controller PCA supports the HP Vectra QS PC's hard disc, flexible disc, and tape backup drives, as well as a parallel port and a serial port. Depending on the PC model, the controller is either the industry-standard ST-506 controller or the Enhanced Small Device Interface (ESDI) controller.

Hard Disc Drives. The following hard disc drives are supported:

The D1297A 40 Mbyte hard disc drive. This drive has an average access time of 28 milliseconds and a maximum data transfer rate of 5 Mbits/second.

The D1445A 100 Mbyte hard disc drive.

The D1446A 150 Mbyte hard disc drive.

The HP Vectra QS PC can support up to two half-height hard disc drives. (See the data sheet for more information on the available hard disc drive models.)

Flexible Disc Drives. All HP Vectra QS PC models come with either a 5.25-inch, 1.2-Mbyte half-height flexible disc drive unit or a 3.5-inch, 1.44-Mbyte flexible disc drive. All models can support up to two flexible disc drive units.

Tape Backup Drives. For hard disc drive backup, the HP Vectra QS PC supports both an internal 40 Mbyte tape backup drive unit with an average data transfer rate of 1.7 Mbyte/minute, and an external 67 Mbyte tape backup drive unit with an average data transfer rate of 2.0 MB/minute.

1.3.2 Memory Subsystem

RAM. The HP Vectra QS PC comes standard with 1 Mbyte of DRAM, expandable to 8 MB (QS/16S) or 16 Mbyte (QS/16 and QS/20). The DRAM subsystem uses a combination paged/interleaved architecture which allows for zero-wait state memory access.

ROM. All models come with 64 Kbyte of system (BIOS) ROM, with two sockets available for 32-Kbyte option ROM chips (on the System Interface PCA).

1.3.3 Software

The HP Vectra QS PC comes standard with the following:

HP Terminal Program software (for terminal emulation)
Volume Expansion Utility
HP Expanded Memory Manager /386

1.4 SPECIFICATIONS AND DIMENSIONS

1.4.1 System Specifications

Regulatory Compliance

1. Radio Frequency Interference:

   FCC Class B
   FTZ 1046/84 Level B Radio Protection Mark pending
   SABS approval
   VCCI approval

2. Safety approvals:

   UL listed
   CSA, TUV certified (FEI pending)
   IEC 380/435 compliance

3. Datacomm:

   Belgium, Germany Nordic Network, and United Kingdom—pending Australian Telecomm Category A license.

4. Ergonomics:

   Complies with German Standard ZH1/68

Power Supply Specifications

1. AC Input

   Auto-ranging world-wide power supply, configured to operate with line voltages of:

   88 to 132 Vac at 47 to 63 Hz
   175 to 269 Vac at 47 to 63 Hz

2. Heat Output

   710 BTUs/hour maximum

3. Output Power

   176 watts peak (134 watts continuous)

4. Power Available to Accessory Cards

   +5 Volts @ 7.5 Amps
   −5 Volts @ 0.3 Amps
   +12 Volts @ 0.5 Amps
   −12 Volts @ 0.3 Amps

5. Power Consumption

   Convenience outlet unused:

   480 watts maximum peak with 110 volts power supply

   Convenience outlet used:

   630 watts maximum peak with 110 volts power supply

1.4.2 Environmental Specifications

Temperature Limits:

Operating temperature:

+5 to +40 °C (+40 to +104 °F) at the humidity limits given below

Storage temperature:

−40 to +70 °C (−40 to +158 °F)

Humidity Limits (Noncondensing):

5% to 95% relative humidity

Maximum Altitude at 40°C (104°F):

Operating altitude: 4.6 kilometers (15,000 feet)

Non-operating altitude: 15.2 kilometers (50,000 feet)

1.4.3 HP Vectra QS PC Dimensions

System Processing Unit Dimensions:

Height: 17 centimeters (6.7 inches)

Width: 42.5 centimeters (16.7 inches)

Depth: 39 centimeters (15.3 inches)

Weight: 15 kilograms (33 pounds)

Keyboard Dimensions:

Height: 3.4 centimeters (1.4 inches)

Width: 46.8 centimeters (18.4 inches)

Depth: 19.8 centimeters (7.8 inches)

Weight: 1.9 kilograms (4.2 pounds)

Cable Length:

DIN cable: 2 meters (6.6 feet)

HP-HIL cable: 2.4 meters (8.0 feet)

Mouse cable: 2.5 meters (8.25 feet)

Video cable: 1 meter (3.3 feet)

1.4.4 I/O Accessory Card Dimensions

Figure 1-4 shows the dimensions of industry-standard I/O accessory cards.

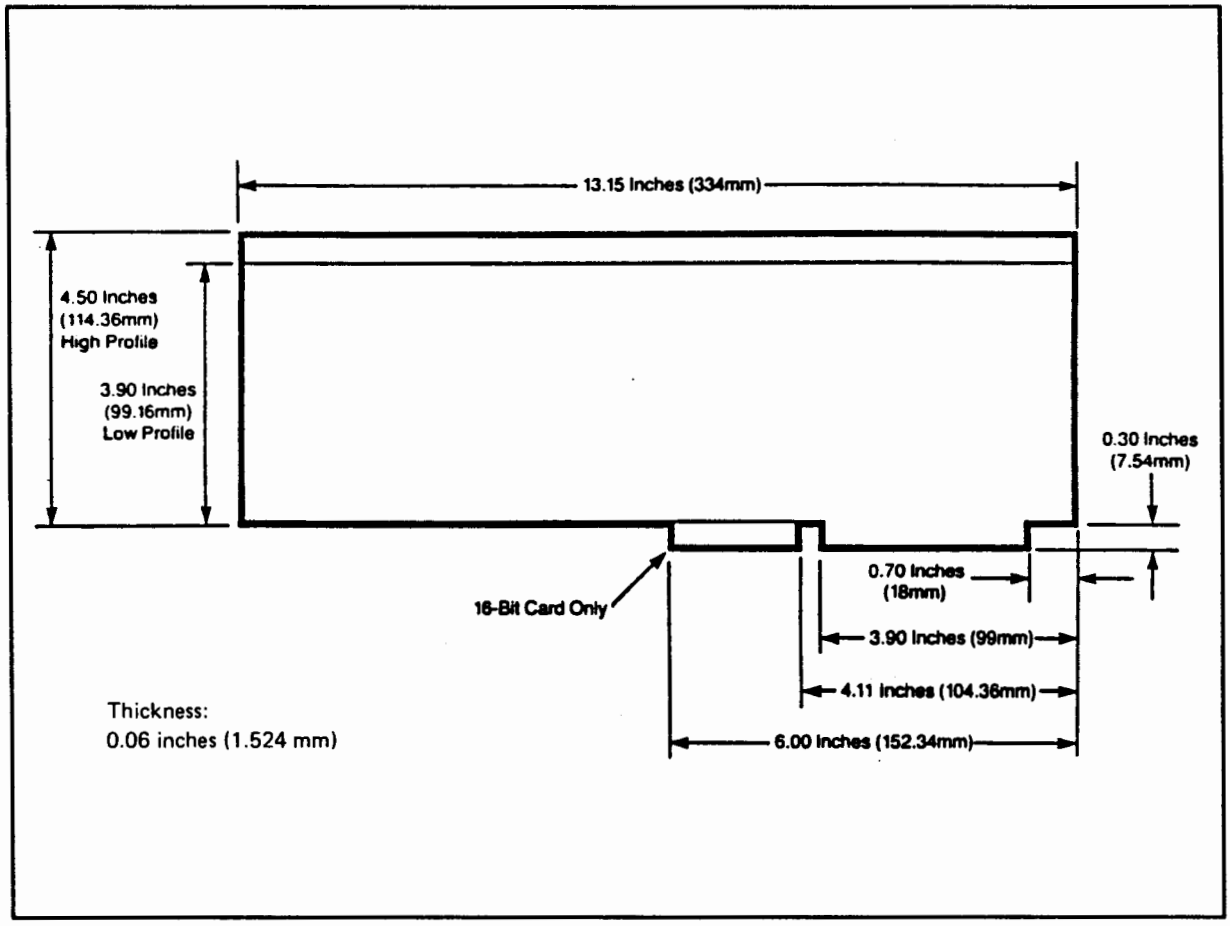

Figure 1-4. Industry-Standard I/O Card Dimensions

1.5 REFERENCES

The following documents should be used for detailed information about components and functions discussed in this manual.

- Chips and Technologies series of 82A and 82C technical reference documents.
- *HP Vectra MS-DOS 3.3 User's Reference Manual.* HP product number 45951D.
- *MS-DOS Macro Assembler Manual.*
- *MS-DOS 3.3 Programmer's Reference Manual.*
- *HP Vectra System BIOS Technical Reference Manual for the Vectra Series of Personal Computers.* HP product number 45945-90012.
- *HP-HIL Technical Reference Manual.* HP product number 45918A.
- *Intel 8086 Family User's Manual.*
- *Intel 80386 Hardware Reference Manual.*
- *Intel 80386SX Hardware Reference Manual.*
- *Intel 80386 Programmer's Reference Manual.*
- *Intel Microcontroller Handbook.*
- *Intel Microprocessor and Peripheral Handbook. Volume I -- Microprocessor.*
- *Intel Microsystem Components Handbook. Microprocessors and Peripherals. Volume II.*
- *Motorola Single Chip Microcomputer Data, Section C.*

2

QS/16 & QS/20 Processor/Memory Printed Circuit Assembly

2.1 INTRODUCTION

This chapter describes the QS/16 and QS/20 Processor/Memory PCA—a six-layer, surface-mount printed circuit assembly which provides the HP Vectra QS (QS/16 and QS/20) PC with all its RAM, the support circuitry for all buses, and support for the board's subsystems.

Below is a list of the major QS/16 & QS/20 Processor/Memory PCA components. Figure 2-1 shows their layout. Figure 2-2 is a block diagram of the QS/16 & QS/20 Processor/Memory PCA.

Major QS/16 & QS/20 Processor/Memory PCA Components:

Component:	Quantity:	QS/16:	QS/20:
Microprocessor	1	80386 @ 16 MHz	80386 @ 20 MHz
Bus controller	1	82C301 @ 16 MHz	82C301 @ 20 MHz
Page memory controller	1	82C302 @ 16 MHz	82C302 @ 20 MHz
High address buffer	1	82A303	82A303
Low address buffer	1	82A304	82A304
Data buffers	2	82A305	82B305
Control buffer	1	82A306	82A306
Backplane clock, OSC1	1	16 MHz	16 MHz
Processor clock, OSC2	1	32 MHz	40 MHz
Coprocessor clock, OSC3	1	32 MHz	32 MHz
System clock, OSC4	1	14.318 MHz	14.318 MHz
Single in-line memory modules	-	100 ns	80 ns
Sockets for single in-line memory module	8		
Connector slot for memory extension PCA (the PCA has 8 sockets for single in-line memory modules)	1		
Dip switch bank for configuration	1		
2-connector slot to System Interface PCA	1		
Socket for 80387 coprocessor	1		

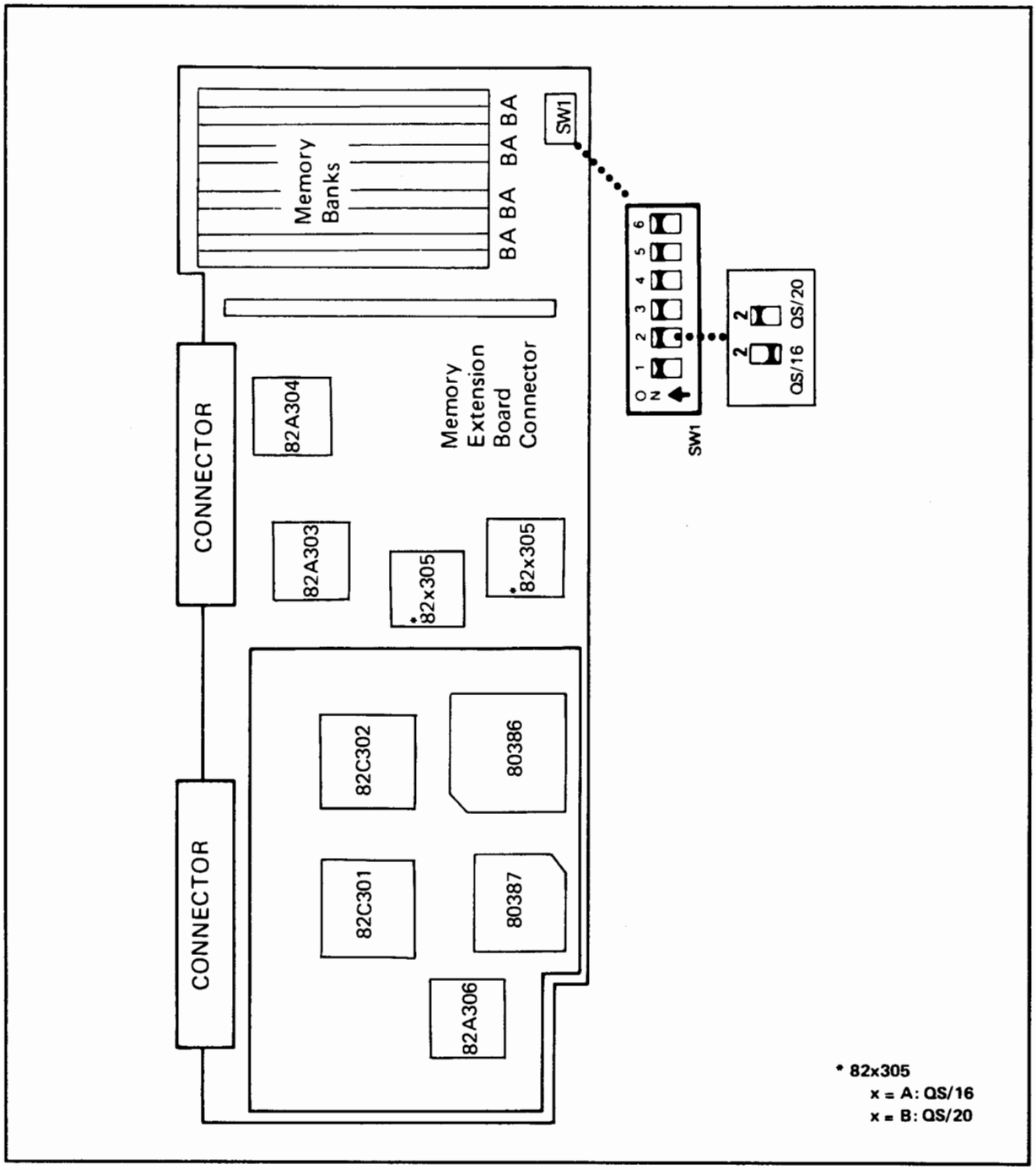

Figure 2-1. QS/16 & QS/20 Processor/Memory PCA Component Layout

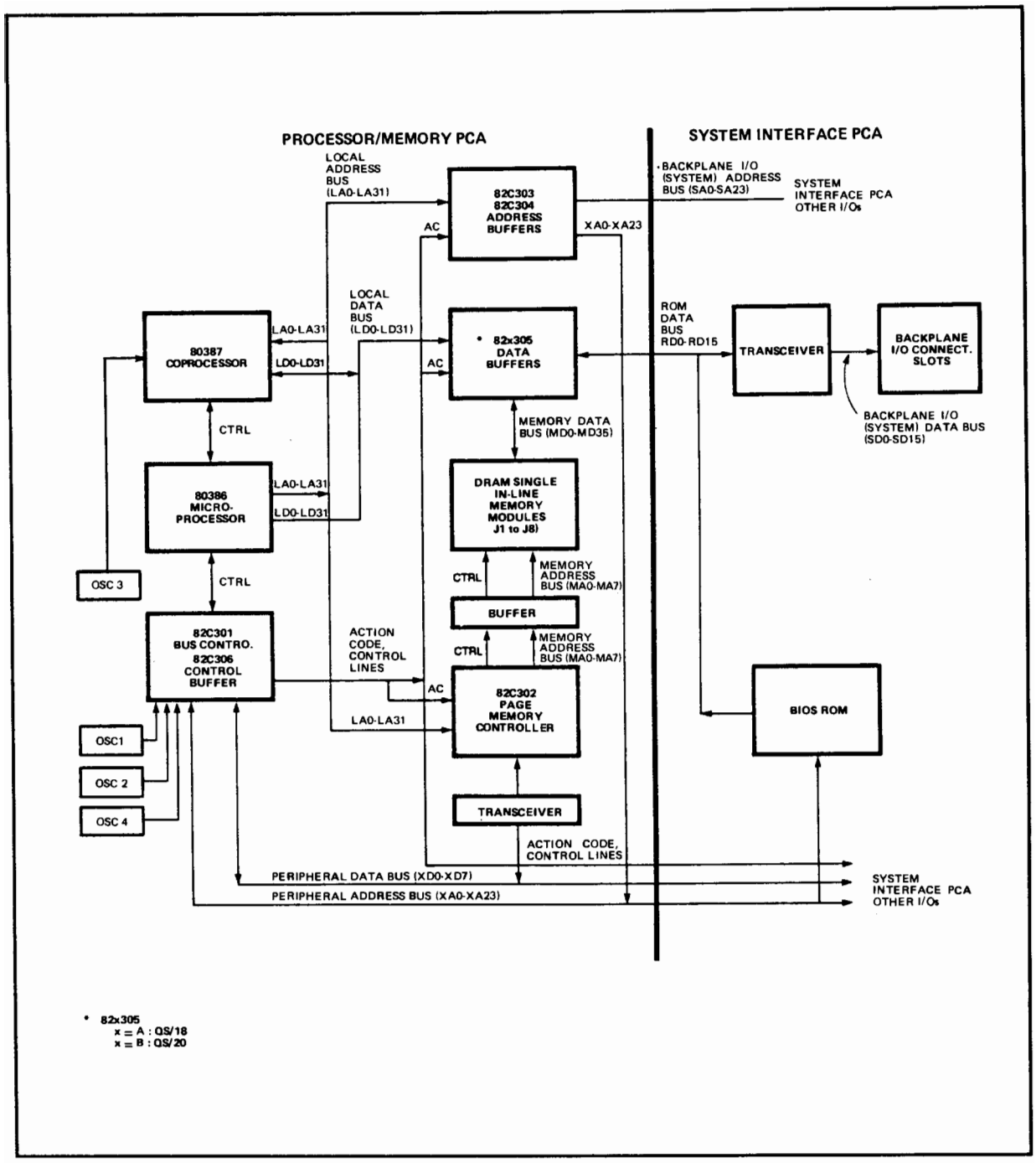

Figure 2-2. QS/16 & QS/20 Processor/Memory PCA Block Diagram

2.2 SYSTEM CLOCKS

The system's main oscillators, located on the QS/16 & QS/20 Processor/Memory PCA, generate the various system clock signals and are discussed under the components for which they provide clocking. (Other oscillators are part of a particular chip or family of chips and are described in the sections covering these chips.)

Oscillator 1 provides 16 MHz for the 82C301 bus controller's ATCLK1. (For further information, see the "Bus Controller" section in this chapter.)

Oscillator 2 provides 32 MHz (QS/16) or 40 MHz (QS/20) for the 82C301 bus controller's CLK2IN. (For further information, see the "Bus Controller" section in this chapter.)

Oscillator 3 is a 32-MHz oscillator which provides clocking for the 80387 coprocessor's asynchronous mode. (For further information, see the "Coprocessor" section in this chapter.)

Oscillator 4 provides 14.318 MHz to the 82A306 control buffer. (For further information, see the "Control Buffer" section in this chapter.)

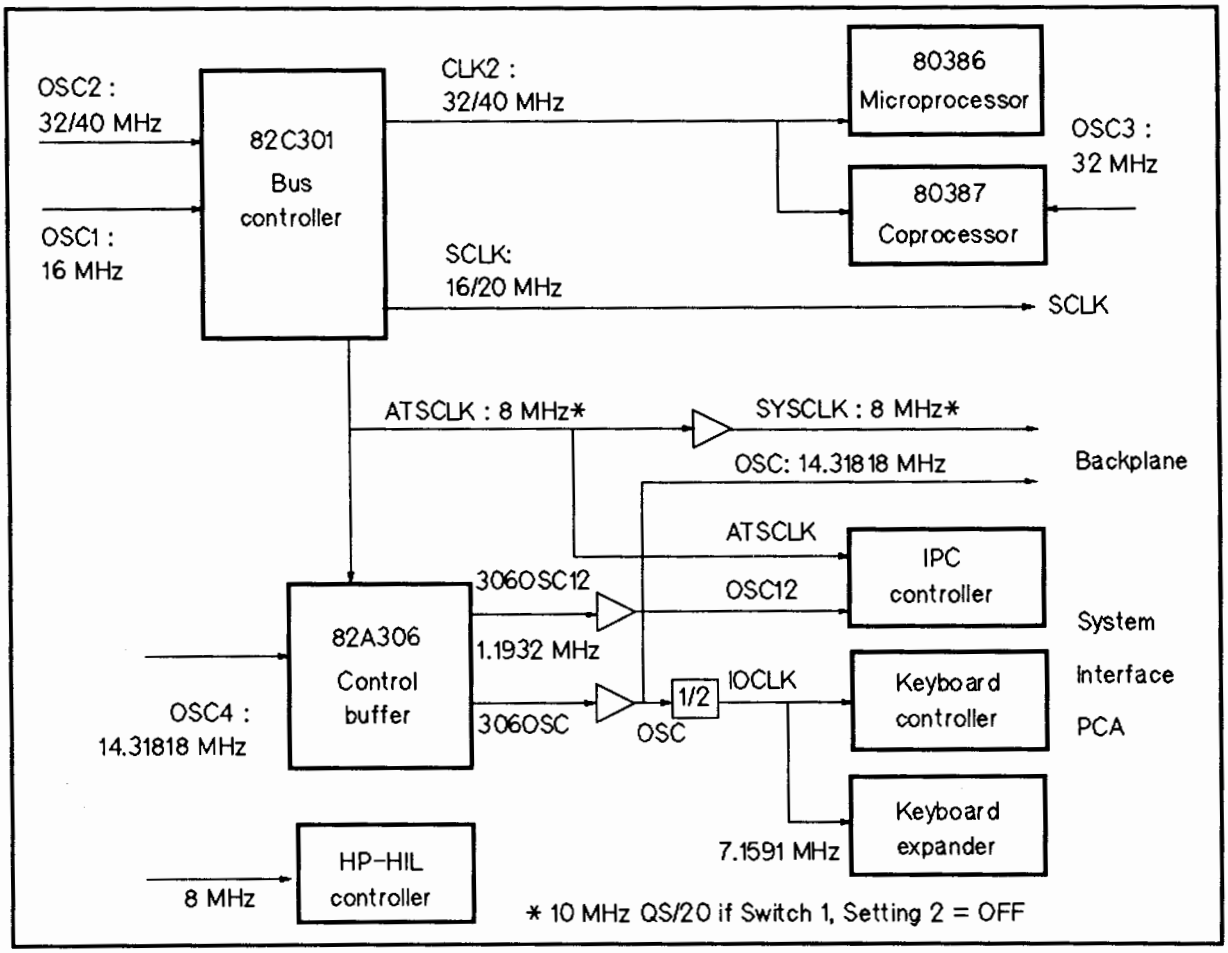

Figure 2-3. QS/16 & QS/20 Processor/Memory PCA Timing

2.3 MICROPROCESSOR

The HP Vectra QS/16 and QS/20 uses the 80386 microprocessor as the central processing unit. It provides the following:

- 4-gigabyte physical memory capacity
- 32-bit registers
- comprehensive instruction set
- downward compatibility with the 8088, 8086 and 80286 microprocessors
- interrupt support capabilities
- processing modes: protected, real-address, and virtual 8086 mode
- separate 32-bit address and data paths
- support for 8-, 16-, and 32-bit data types

Microprocessor Clocking

The HP Vectra QS/16 uses a 16-MHz 80386, which is driven by a 32-MHz clock (OSC2). The HP Vectra QS/20 uses a 20-MHz 80386, which is driven by a 40-MHz clock (OSC2).

OSC2 provides the CLK2 clock signal (32 or 40 MHz) for the 82C301 bus controller. In turn, the bus controller provides the 386CLK2 signal (32 or 40 MHz) for the 80386 microprocessor. The 80386 internally divides the 386CLK2 signal to 16 MHz or 20 MHz. (For more information, see the "Bus Controller" section in this chapter.)

Microprocessor Compatibility

By dynamically sizing data, the 80386 microprocessor maintains hardware compatibility with the 8088, 8086 and the 80286 microprocessors. The 80386 microprocessor also maintains software compatibility, in that it runs industry-standard operating systems (including MS-DOS 3.2, MS-DOS 3.3, Microsoft OS/2, and Windows 2.0) and application software developed for systems based on 8088, 8086, or 80286 microprocessors.

Microprocessor Operating Modes

The 80386 microprocessor offers the following operating modes:

1. Real-Address Operating Mode

   The 80386 microprocessor's real-address operating mode is entered when the SPU is powered up or a system reset occurs. This operating mode addresses up to 1 Mbyte of system memory and allows 32-bit operands, but does not provide memory protection.

   Windows 2.0, all versions of MS-DOS, as well as nearly all industry-standard application software, run in the real-address operating mode.

   The real-address operating mode is compatible with operating systems written for the 8086 microprocessor. With a few differences (described in the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers*), the 80386's real-address object code is compatible with the real-address object code of the 8088, 8086, and 80286 microprocessors.

2. Protected Operating Mode

   The 80386 microprocessor's protected operating mode provides addressing beyond 1 Mbyte, with up to 4 gigabytes of physical memory available, and supports programs that use memory above 1 Mbyte (VDisk and Disc Cache, for instance).

   When the 80386 microprocessor is in the protected operating mode, its object code is compatible with that of the 80286 in protected operating mode, but not with an 80286 in the real-address operating mode. In addition, if the 80386 is in the protected operating mode, its object code is compatible with that of the 8088 or 8086 microprocessor.

3. Virtual-Address Operating Mode

   The virtual-address operating mode allows multiple 8086 sessions of 1 Mbyte each and can provide access up to 64 terabytes of virtual memory addresses. This mode supports 8088 and 8086 applications that run as a subset of the 80386 microprocessor's protected operating mode.

   In the virtual-address operating mode, the 80386 microprocessor's software and operating systems are compatible with those written for the 8088 and 8086 microprocessors.

For more information on the 80386 microprocessor, refer to the *Intel 80386 Hardware Reference Manual.*

2.3.1 I/O Address Map

Appendix A gives the I/O address map for the central processing unit. The HP Vectra QS PC uses the first 1024 I/O hex addresses, 0000 through 03FF.

2.4 COPROCESSOR

The HP Vectra QS PC does not come standard with the coprocessor, but it does provide supporting software and an extended math coprocessor socket in which the coprocessor can be installed.

The industry-standard coprocessor (80387) is a numeric processing unit which significantly improves performance of spreadsheets, CAD/CAE/CAM, engineering, and scientific applications. (Only applications with built-in support for the 80387 will realize these performance improvements.)

The coprocessor interfaces directly with the 80386; it extends the 80386 instruction set by providing hardware for BCD data and the high-precision integer functions and floating-point calculations otherwise performed by software.

If the 80387 coprocessor is installed, setting 1 of Switch 1 on the Processor/Memory PCA's should be set to the OFF position in order to connect it.

(Note that a Weitek floating point accelerator cannot be used.)

Coprocessor Clocking

The 80387 coprocessor can be operated in either the synchronous or the asynchronous mode. (It is recommended that synchronous mode only is used.)

If the Processor/Memory PCA's Switch 1, setting 6, is set to its default ON position, the 80387 operates in the synchronous mode; using the same clock as the 80386 microprocessor.

If Switch 1, setting 6, is set to the OFF position, the 80387 operates asynchronously, using a clock signal from the 32 MHz (OSC3) clock.

Coprocessor Hardware Interface and Compatibility

1. Hardware Interface

   If an 80387 coprocessor is installed, setting 1 of Switch 1 should be set to OFF to enable it.

   Immediately after a system power-up or reset, the 80387 indicates its presence to the 80386 microprocessor by sending it an ERROR# control signal. (The # symbol at the end of the 80386 signal names is used by Intel to indicate that the active or asserted state occurs when the signal is at a low-voltage level.)

   This causes the 80386 to set the Extension Type (ET) bit in its Control Register 0.

   The 80387 coprocessor is directly connected to the 80386 microprocessor via the local address and data bus. Three control signals (BUSY#, PEREQ and ERROR#) synchronize the transfer of instructions and data between the 80386 and the 80387. When the 80386 selects the 80387, it asserts I/O address bit A31 so that the 80387 acts as an I/O device in a reserved I/O space.

2. Compatibility

   The HP Vectra QS PC numeric coprocessor interface supports the 80387 coprocessor. The 80387 coprocessor supports 8087 and 80287 coprocessor instruction sets.

Coprocessor Operating Modes

Since all memory accesses are handled by the 80386 microprocessor, the 80387 works the same whether the 80386 is executing in the real-address, the protected, or the virtual-address operating mode. (For further information on the 80387 coprocessor, refer to Intel reference manuals.)

For further information, refer to the Intel reference manuals.

2.5 MEMORY

2.5.1 Main Memory (RAM)

The HP Vectra QS PC main memory (also known as system memory, or system RAM, or RAM) consists of dynamic RAM chips mounted on single in-line memory modules.

The modules are available in 256-Kbyte or 1-Mbyte modules and fit into sockets. Eight sockets are available on the Processor/Memory PCA (arranged in banks "A" and "B"). An additional eight sockets are available on a plug-in Memory Extension card, arranged in banks "C" and "D". (See the figure in this chapter, "Processor/Memory PCA Component Layout" to locate the banks of sockets.)

Main Memory Configurations

This memory is expandable to 16 Mbyte by placing even increments of modules in the sockets, as shown in Table 2-1.

Table 2-1. QS/16 & QS/20 Main Memory Expansion

For Total DRAM of:	Type of Modules Needed:	Sockets Used:
1 Mbyte	4 256-Kbyte	All "A" sockets
2 Mbytes	8 256-Kbyte	All "A" and "B" sockets
4 Mbytes	4 1-Mbyte	All "A" sockets
4 Mbytes *	16 265-Kbyte	All "A", "B", "C" and "D" sockets **
8 Mbytes	8 1-Mbyte	All "A" and "B" sockets
10 Mbytes	8 256-Kbyte **and** 8 1-MByte	In all "A" and "B" sockets **and** in all "C" and "D" sockets **
16 Mbytes	16 1-Mbyte	All 16 sockets **

Notes:

(*) For improved system performance, it is recommended that 16 256-Kbyte modules are used. (This allows the memory controller to use interleaving mode.)

(**) These configurations require the plug-in Memory Extension card.

Base RAM Configurations

The Processor/Memory PCA's Switch 1, setting 3, can be used to configure the main memory base RAM as required by applications used.

In the ON position, the main memory's base RAM is set to 640 Kbytes; in the OFF position, base RAM is set to 512 Kbytes.

Main Memory Architecture

The HP Vectra QS has a paged/interleaved main memory architecture, using a 82C302 page/interleave memory controller that organizes main memory DRAM to decrease the number of accesses that incur a wait state penalty.

Paged DRAM is organized into paged rows and columns. One memory strobe (the RAS, or row address strobe) generates the row address (or the page address); a second memory strobe (the CAS, or column address strobe) generates the column address.

If access is required on the same page of DRAM, there may be zero wait states as the row address is already strobed (only CAS is generated). But if access is required on a different page of DRAM, there is at least one wait state.

Interleaved DRAM is organized into four banks, with each bank having four single in-line memory module sockets. When only the "A" bank of four sockets is filled, the system operates in the non-interleaved mode. Because interleaving is done between pairs of banks, for the system to operate in the paged/interleaved mode, either two or four (never three) banks of sockets must be filled. (For more information, see the "Page Memory Controller" section in this chapter.)

Memory Map

Figure 2-4 gives the HP Vectra QS PC memory map. As with industry-standard products, the first 1 Mbyte of main memory is reserved for standard memory.

The base RAM (either the first 512 Kbytes or 640 Kbytes of main memory, depending on how the RAM is configured, using Switch 1 setting 3) is used for MS-DOS applications.

From hex address 0A0000 to 0FFFFF, the system reserves main memory for video RAM, I/O adapters, option ROM, and BIOS ROM.

Main memory from hex address 100000 to FDFFFF is reserved for 32-bit dynamic expansion using the serial in-line memory modules.

Upon power-up, the 64 Kbytes of option ROM on the System Interface PCA at hex address 0E0000 to 0EFFFF are automatically mapped to hex address FE0000 to FEFFFF; similarly, the 64 Kbytes of BIOS ROM on the System Interface PCA at hex address 0F0000 to 0FFFFF are automatically mapped to hex address FF0000 to FFFFFF.

(If you have option ROMs, they are also mapped at hex address FFFE0000 to FFFEFFFF, and BIOS ROMs are also mapped at hex address FFFF0000 to FFFFFFFF. However, the upper eight bits of these addresses do not appear on the backplane I/O bus.)

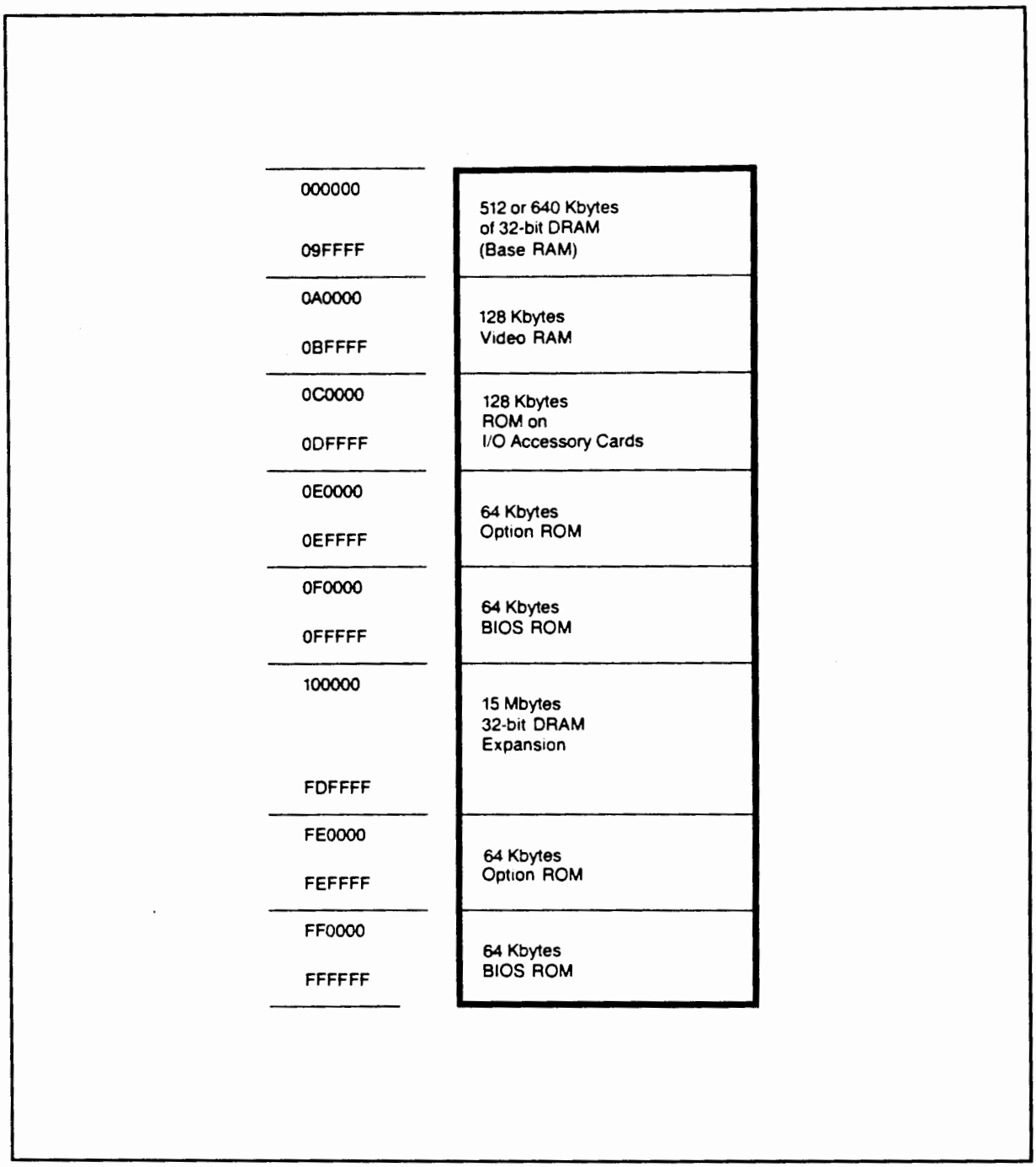

Figure 2-4. HP Vectra QS PC Memory Map

1. Refresh

   All DRAM is refreshed within 4 milliseconds (for 256-Kbyte DRAM) to 8 milliseconds (for 1 Mbyte DRAM). A refresh cycle for one bank of DRAM requires seven 386CLK2 cycles, with refreshes to additional banks staggered by one 386CLK2 cycle, so that four banks take ten 386CLK2 cycles to refresh.

   A refresh cycle begins with the 82C206 IPC's (integrated peripheral controller on the System Interface PCA) OUT1 pin generating a refresh request (REFREQ) to the 82C301 bus controller every 15 microseconds.

   To perform a refresh, the 82C301 bus controller generates a hold request (HOLD) to the 80386 microprocessor, which subsequently generates a hold acknowledge (HLDA) to the bus controller.

   The bus controller then issues a refresh signal (REF*) which goes to the 82C302 page memory controller, the 82A303 and 82A304 address buffers, and the backplane I/O.

   - When the page memory controller receives the REF* signal, it strobes the refresh row address into the banks of DRAM on the processor/memory card.
   - When the address buffers receive the REF* signal: The 82A303 high address buffer sets system address bus lines SA23 to SA12 low. A counter within the 82A304 low address buffer drives the system address bus lines SA11 to SA0, which represents the refresh row address for RAM on the backplane (for I/O accessory cards). Note that the AT standard uses SA0-7 for the refresh operation.

     The REF* signal goes to the backplane I/O and indicates to I/O accessory cards that a refresh operation is taking place.

   In addition, an I/O accessory card can issue a REF* signal to initiate a refresh request to the bus controller, the page memory controller, and the address buffers, independent of the IPC's periodic refresh requests (REFREQ).

2. Access Time

   The main memory for the HP Vectra QS uses DRAM with the following access and cycle time:

PC:	Access Time:	Cycle Time:
QS/16	100 nanoseconds	190 nanoseconds
QS/20	80 nanoseconds	165 nanoseconds

   (Hewlett-Packard assumes no responsibility for the access time of memory modules not supplied by an HP-approved vendor.)

   (*)Active low.

3. Parity

   DRAM uses eight data bits and one parity bit.

   Parity is generated for each byte of DRAM during write operations, and checked during read operations.

   If a parity error occurs, a parity check signal LPAR* is generated by the 82C306 control buffer and sent to the 82C301 bus controller. (LPAR* is also sent to the page memory controller for diagnostic purposes.)

   If parity error detection is enabled, the bus controller generates a non-maskable interrupt (NMI), which is sent to the 80386 microprocessor via the 8042 port expander. (For details, refer to the "Interrupt Controller" section in the "System Interface PCA" chapter.) This operates as follows.

   For memory write operations, the parity is controlled through an external parity generation circuit:

   The data goes through the data buffers, which generate low and high parity bits (PL0-PL3 and PH0-PH3), representing the parity of the lower and upper nibbles (4 bits) of each byte written.

   PL0-PL3 and PH0-PH3 are exclusive ORed together to form memory parity bits MP0-MP3, representing the parity for byte 0 to 3 for the data being written.

   MP0-MP3 are then written into the proper parity bits in the DRAM banks (the MP0-MP3 inputs to the control control buffer are ignored during the write operation). These bits are used to check parity during read operations.

   For memory read operations, the parity is checked by the control buffer:

   The data from the DRAM is read into the data buffer, which produces parity bits PL0-PL3 and PH0-PH3. These parity bits go to the 82A306 control buffer.

   MP0-MP3 (which represent the parity as determined when the data was written) are also read from DRAM and are sent to the control buffer. MP0-MP3 are compared with PL0-PL3 and PH0-PH3, the parity found when data is read back.

   The control buffer then produces a parity output signal, LPAR*, which is active if a parity error exists. LPAR* is sent to the bus controller and page memory controller. (The failing address is latched within the page controller for diagnostic purposes.)

4. Self-tests

   Upon power-up, the main memory goes through a self-test, as discussed in the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

2.5.2 Read-Only Memory

The System Interface PCA provides two 32-Kbyte ROM chips (containing the BIOS firmware) and sockets for two 32-Kbyte option ROM chips. (See the "System Interface PCA" chapter for more information on ROM.)

(*)Active low.

2.6 PAGE MEMORY CONTROLLER

The 82C302 page memory controller:

- Controls all main memory accesses from the 80386 microprocessor, direct memory access refresh requests, and
- Organizes the main memory DRAM into paged and interleaved DRAM to decrease the number of accesses incurring a wait state penalty.

Clocking for the page memory controller comes from the signal 302CLK2, which originated from the 82C301 bus controller.

DRAM chips are physically organized onto single in-line memory modules, which can make up to four 4-byte wide banks: banks A, B, C, and D. If four 256-Kbyte modules are used, a bank has 1 Mbyte of DRAM; if four 1-Mbyte modules are used, a bank has 4 Mbytes of DRAM. (Refer to the "Main Memory" section and the "Main Memory Expansion" table in this chapter for more information on the physical organization of the DRAM.)

The page memory controller logically organizes DRAM as *pages.* For each 256-Kbyte module, there are 512 pages (rows), with each page having 512 bytes (1 byte for each 512 columns). Since a bank has 4 single in-line memory modules, a banked page has 2 Kbytes of dynamic RAM (i.e. 512 bytes x 4 modules = 2 Kbytes). This paged memory can be accessed as 8-bit bytes, 16-bit words, or 32-bit words.

To access memory, the page memory controller issues to each accessed module a row address and then a column address. The row address indicates the page, while the column address indicates which of the 512 bytes on that page (row) are to be accessed.

The row and column addresses are multiplexed over MA0-MA7 and DA8-DA9 from the page memory controller and are latched into a memory module by the appropriate row address strobe (RAS) and column address strobe (CAS) signals.

To achieve 8-bit, 16-bit, or 32-bit operations, the CAS signal is ANDed with the appropriate latch byte enable (LBE) signal from the 82A306 control buffer. If the next access is within the current page (row), a new row address does not need to be issued, just a new column address and CAS signal, resulting in fewer wait states.

If more than one bank of sockets are filled with DRAM modules, the page memory controller *interleaves* the pages between banks, with even pages on one bank, and odd pages on the next bank. Interleaving requires that two or four (but never three) banks of sockets be filled with DRAM modules. If more than one bank of sockets is to be filled, the two banks making up a pair of banks must each use the same type of modules, but two pairs can use different types of modules.

Interleaving pages on different banks can minimize the number of row addresses and RAS signals required, as the page memory controller has a separate page register for each bank. If bank "A" has an even page number as its current page, and bank "B" has the next (odd) page number as its current page, no new row addresses or RAS signals are needed as long as accesses are within these two pages.

Once the 80386 microprocessor generates a local address, the page memory controller decodes the type of access according to its various configuration registers. These registers determine if a ROM access, an access of the backplane I/O, or a DRAM access is required. If a DRAM access is required, the page memory controller accesses the DRAM according to configuration registers that state what type of DRAMs are used and how many wait states are desired.

In direct-memory accesses (DMA), only 8-bit and 16-bit operations are supported. The address on the local address bus comes from the System Interface PCA's 82C206 Integrated Peripheral Controller via the peripheral address bus and the address buffers. The page memory controller decodes the address as it would an access from the 80386 microprocessor.

A refresh access is initiated when the page memory controller receives a REF* input from the 82C301 bus controller. The refresh row address is strobed into each bank with an offset of one 386CLK2 cycle between strobes. (For more information on the 82C302 page/interleave memory controller, consult the Chips and Technologies data sheet, *CS8230: AT/386 CHIPSet.*)

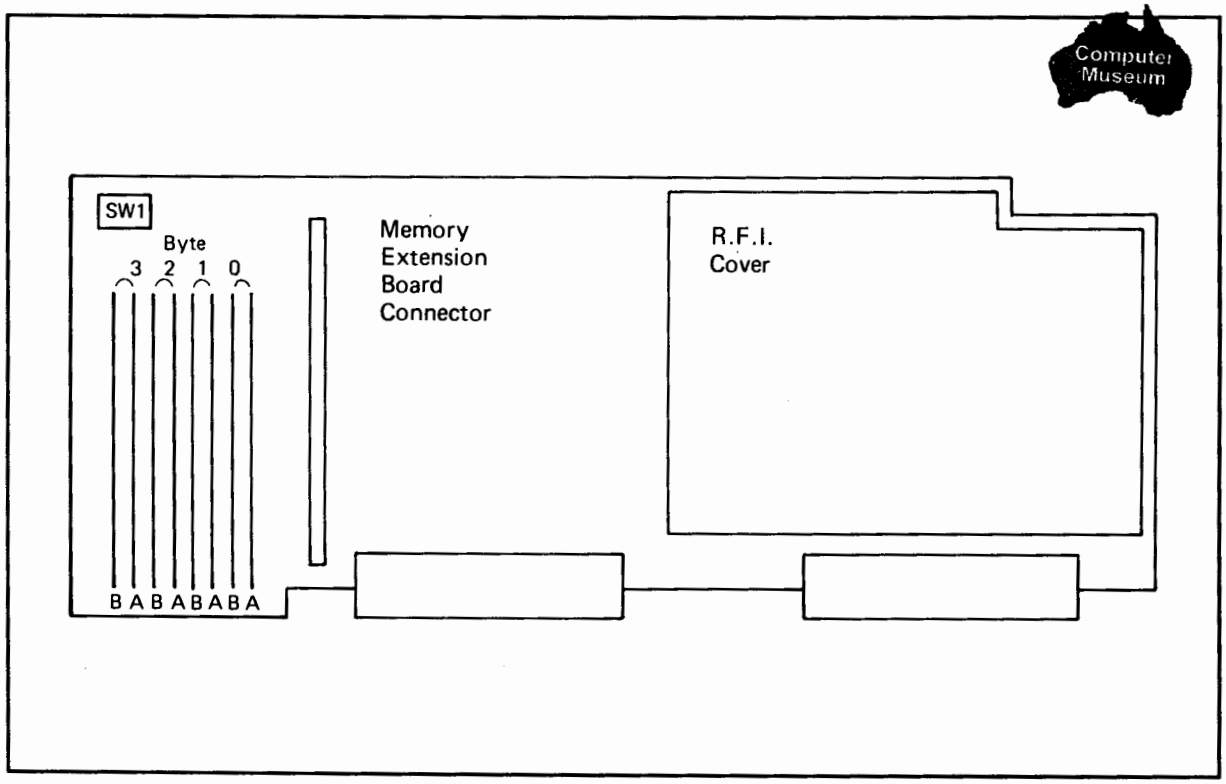

Figure 2-5. QS/16 & QS/20 Physical Organization of DRAM (Board/Memory Modules View)

* Active low

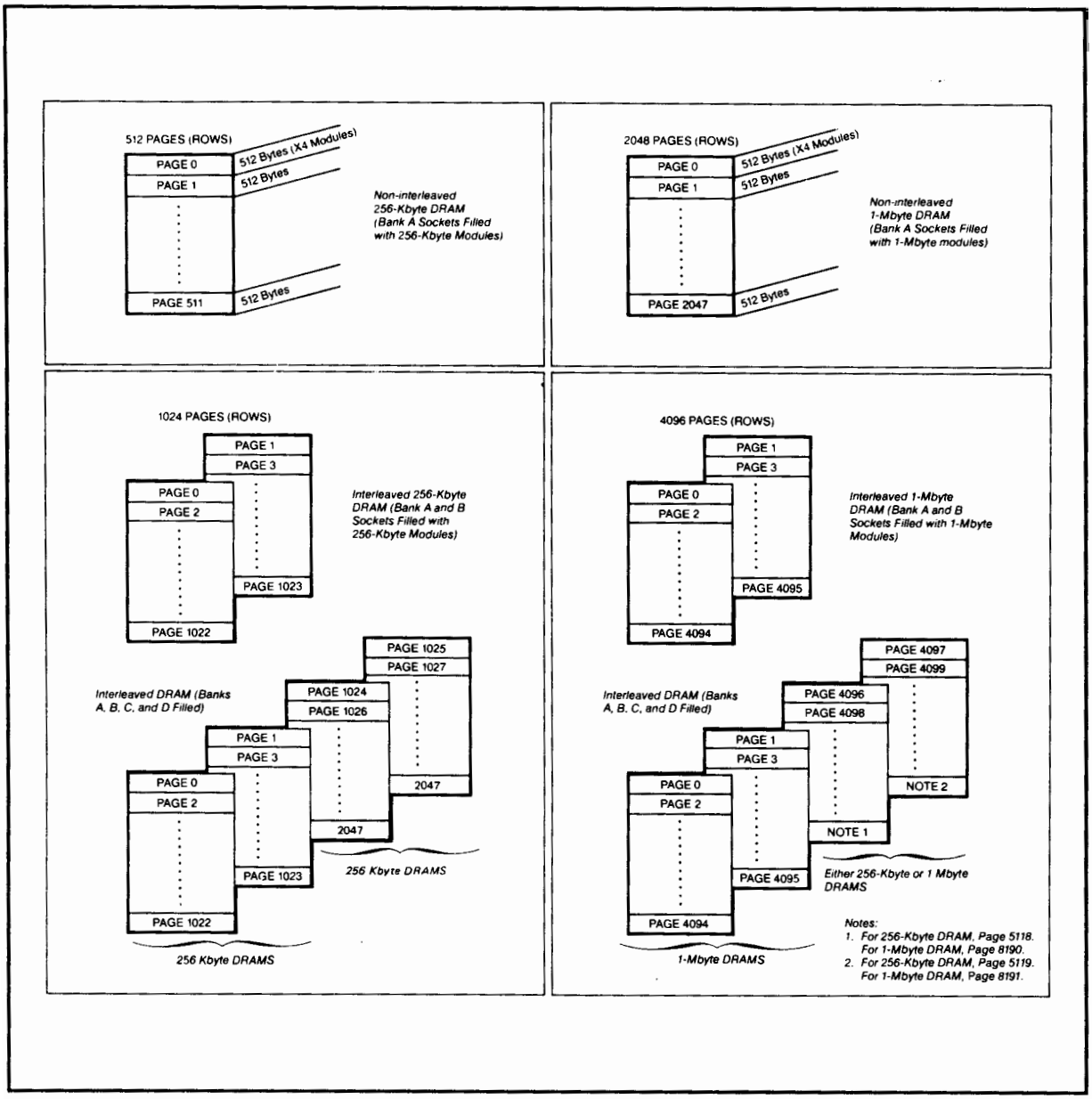

Figure 2-6. Logical Organization of DRAM

2.7 BUS CONTROLLER

The 82C301 bus controller works in conjunction with the 82A306 control buffer to generate clocking for the 80386 microprocessor, the coprocessor, and the page memory controller. The bus controller also provides the generation and synchronization of control signals for all buses. In addition, it offers an industry-standard Port B status register, and optional speeds for timing-dependent software. (For more information, refer to Chips and Technologies Reference Manuals.)

Bus Controller Clocking

The clock input to the bus controller is provided by ATCLK1 (OSC1, 16 MHz) and CLK2IN (OSC2: 32 MHz on QS/16, 40 MHz on QS/20).

The CLK2 output from the bus controller (to the microprocessor [386CLK2], coprocessor [EMCCLK2], and page memory controller [302CLK2]) is derived from OSC2, and is either 32 MHz (QS/16) or 40 MHz (QS/20). Simultaneously pressing Ctrl Alt \ causes CLK2 to be derived from OSC1, for a 16-MHz signal.

The bus controller's SCLK output signal, used in various timing circuits on the Processor/Memory PCA, is equal to one-half the CLK2 signal.

The bus controller's ATSCLK output signal is provided to the 82A306 control buffer and buffered to drive the clock signal SYSCLK, the signal for the industry-standard backplane I/O bus. In addition, ATSCLK is sent to the 82C306 Integrated Peripheral Controller.

Through software control, ATSCLK's frequency can be selected as:

1. Synchronous with CLK2 from OSC2 (that is, CLK2÷4; namely, 8 MHz on the QS/16 and 10 MHz on the QS/20) - default QS/16.
2. Or, ATCLK1÷2 (from OSC1); that is, 8 MHz - default QS/20.

For more information, refer to Chips and Technologies Reference Manuals.

Bus Arbitration

The bus controller synchronizes control of all bus activities. For direct memory accesses (DMA), the bus controller accesses memory as described in the "DMA Controller" section of Chapter 3. The bus controller has the following two state machines that control access to devices by the 80386 microprocessor:

1. The *local bus state machine,* controls accesses by the 80386 to devices on the local bus. It also supports 32-bit transfers between the 80386 and system memory (or memory-mapped I/O), but does no data size conversions.
2. The *AT (industry-standard) bus state machine,* controls the 80386 microprocessor accesses to devices on non-local buses. It provides sequencing and timing controls (including wait state generation) for status and command phases of the different bus cycles. In addition, it generates action control code signals that go to the data buffers for data size conversions.

Bus Controller Reset Control

When the power supply's PFAIL signal goes high (detected at the bus controller's RESET1* pin, see Chapter 5), it activates the bus controller's RESET3 and RESET4.

RESET3 — Resets the 80386 microprocessor, the 80387 coprocessor and various Processor/Memory PCA timing circuits.

RESET4 — Provides the backplane I/O connector slots with a reset for input devices and resets the following:

- 82C302 page memory controller
- 82C206 IPC (integrated peripheral controller)
- 8042 keyboard controller
- 8042 keyboard controller port expander
- HP-HIL master controller (IRD2)

For more details on the PFAIL signal, refer to the chapter *Power Supply.*

Note that simultaneously pressing Ctrl Alt Del causes a soft reset - no reset lines are activated.

However, it is possible to reset the microprocessor by writing FEh to I/O address 64 (within the 8042 keyboard controller on the System Interface PCA). This activates RESET2*, which in turn activates RESET 3. This is provided for compatibility with the AT 286 computers, as it is the only way to return from protected mode to real mode.

* Active low

2.8 CONTROL BUFFER

The 82A306 control buffer receives a 14.318 MHz signal (OSC4), which is divided by 12 to generate a 1.19 MHz signal. This signal is sent to the 82C206 integrated peripheral controller's (on the System Interface PCA) timer 0, counter 1 and counter 2.

The control buffer also provides the byte-enable latch which, during memory cycles, holds valid the byte enables from the 80386 microprocessor.

The control buffer checks parity by generating read parity from the data buffer's partial parity bits. (Write parity is controlled through an external parity generation circuit.) Refer to "Main Memory (RAM)" in this chapter.

In addition, the control buffer provides drivers for control signals on the backplane I/O. Furthermore, the 82A306 control buffer generates some of the signals used by the 82C301 bus controller to control bus accesses.

2.9 ADDRESS BUFFERS

The address buffer for the HP Vectra QS PC comprises an 82A303 high address buffer and an 82A304 low address buffer. They support transfers on the following buses:

- A, the local address bus to the 80386 microprocessor and the coprocessor
- SA, the system address bus for the backplane I/O
- XA, the peripheral address bus for the keyboard controller 8042 keyboard controller port expander, HP-HIL Controller (IRD2), and 82C206 IPC (integrated peripheral controller).

The 82A303 high address buffer acts as a buffer for local address bits A31 through A12, system address bits SA23 through SA12, and peripheral address bits XA23 through XA12.

The 82A304 low address buffer acts as a buffer for address bits A11 through A2, SA11 through SA0, and XA11 through XA0. (XA0 and XA1 are generated by the 82C301 bus controller for use by the AT bus.)

The 82A303 high address buffer provides address decoding signals required by other chips, such as the 82C302 memory controller. The 82A304 low address buffer provides address decoding signals required by peripheral devices. In addition, the 82A304 low address buffer provides refresh address generation for the system address bus (see the "Main Memory Operation" section in this chapter).

The high and low address buffers buffer the interface between the A bus, the SA bus, and the XA bus, according to various control line states. Both the high and low address buffers directly interface to the industry-standard bus (the 24-bit XA bus and SA bus) via bidirectional drivers.

2.10 DATA BUFFERS

The data buffer for the HP Vectra QS PC consists of either two 82A305 data buffers (QS/16) or two 82B305 data buffers (QS/20). The data buffers support data transfers over the following buses:

- D, the local data bus to the 80386 microprocessor and the coprocessor
- MD, the system memory data bus to the dynamic RAM
- RD, the ROM data bus connected to the BIOS ROMs
- SD, the system data bus to the backplane I/O, connected to the RD by a transceiver
- XD, the peripheral data bus to the keyboard controller 8042 keyboard controller port expander, HP-HIL controller (IRD2) and the 82C206 IPC (on the System Interface PCA), connected to SD by a transceiver.

Via D and MD, the data buffers support data transfers between the 80386 microprocessor and the system RAM. Via D, RD and SD, the data buffers also support data transfers between the 80386 and the industry-standard backplane connector slots. During direct-memory accesses, the data buffers connect RD to both D and MD. In addition, the data buffers provide data bus connections that convert data words to a size compatible with backplane I/O operations.

Control of Data Bus Buffers

According to signals received from the bus controller and the page memory controller, the data buffers determine (1)which data buses are active (i.e. connected) and (2)the subsequent direction for data bus buffer drivers.

Data Conversion

The data buffer converts data to a size permitting the 80386 microprocessor to access the I/O bus. Data is converted via action code control signals from four bus controller lines to the data buffer; these codes control the connection of bus bits between (1)the system data bus for the backplane I/O and (2)either the local data bus or the memory data bus.

2.11 LOCAL BUS (LBUS)

The local bus consists of the local address bus (A), the local data bus (D), bus status pins, and bus control pins for the 80386 microprocessor (and the coprocessor, if installed). The local bus connects the 80386 microprocessor and the coprocessor to the rest of the system.

Separate from the local data bus, the local address bus generates 32-bit addresses. Its 30 address lines (A31 to A2) indicate a 4-byte location, from which the local address bus's four byte enable lines (BE3* to BE0*) select the bytes to be enabled. The 32 local data bus lines (D31 to D0) transfer either 8, 16, 24, or 32 bits of data. The local bus status lines (D/C*, M/IO*, W/R* and LOCK*) establish the type of bus cycle to be performed.

The 82C301 bus controller and the 82A306 control buffer use the local bus control pins to control the bus cycle on a cycle-by-cycle basis.

At the start of a local bus cycle, the 80386 microprocessor places on the local address bus (A) valid address signals which go to: (1)the address buffers and then to other buses and to (2)the 82C302 page memory controller, which interfaces with the DRAM, and (3)the coprocessor. Status signals corresponding to the bus cycle to take place are then sent to the 82C301 bus controller, the 82A306 control buffer, and the coprocessor. Data to/from the 80386 microprocessor are sent over the local data bus (D) to/from the data buffers.

2.12 MEMORY BUS

The memory data bus (MD) is 36 bits wide (32 data bits, with 4 parity bits). The system memory data bus interfaces to the local data bus or the ROM data bus, through the data buffer. The Memory Address Bus (MA) is an 10-bit bus (MA0-MA9) from the 82C302 page memory controller that accesses a particular DRAM location. (Row address strobes RAS~0 to RAS~3, column address strobes CAS~0 to CAS~3, and byte enable control signals LBE0 to LBE3 complete the memory address scheme.)

2.13 READ-ONLY MEMORY BUS

All data coming from the BIOS ROMs or option ROMs (on the System Interface PCA), or going to or from the peripheral data bus or the backplane I/O data bus, go over the 16-bit ROM data bus (RD).

Via the data buffer, the local data bus and the system memory data bus interface with the RD. Through a transceiver, RD interfaces with the backplane I/O data bus, which in turn, interfaces with the peripheral data bus through another transceiver.

2.14 BACKPLANE I/O BUS (SBUS)

The HP Vectra QS PC backplane I/O bus, an industry-standard 8-MHz bus (also known as the S-bus, or system bus) is separate from the system memory bus. It connects to the rest of the computer system, one 8-bit and six 16-bit backplane I/O connector slots. Further information is to be found in the chapter "System Interface Printed Circuit Assembly."

The system address bus (SA) is a 24-bit address bus (SA0-SA23), connected to the 82A303 and 82A304 address buffers on the Processor/Memory PCA, for connection to other address buses in the system. Backplane I/O connector slots can receive an address from any of the other address buses or generate an address to any of the other buses, depending on the operation involved. (For more information, see the section on "Address Buffers" in this chapter.)

The system data bus (SD) is a 16-bit data bus (D0-D15) over which data to/from the backplane I/O connector slots are sent. This data, in turn, are sent over the ROM data bus to the data buffers on the Processor/Memory PCA for connection to the rest of the system.

If a backplane I/O connector slot needs control of the system, it holds MASTER* low. After the appropriate protocol has been completed, an address originating from an I/O accessory card is sent over SA to other address buses in the system.

If the 80386 microprocessor needs to access a backplane I/O connector slot, an address is sent over the local address bus, through the address buffers, and then to SA.

During direct-memory access (DMA) operations, an address originating from the integrated peripheral controller's DMA controller is sent over the peripheral bus to both the S-bus and the local bus.

Backplane I/O Bus Clocking

The clock used for the industry-standard I/O backplane depends on the position of Processor/Memory PCA's Switch 1, setting 2.

When setting 2 is in the OFF position (default QS/16), the HP Vectra QS uses a synchronous clock signal generated by the 82C301 bus controller's processor crystal oscillator, OSC2 (32 MHz on a QS/16, 40 MHz on a QS/20), ÷4. That is 8 MHz on a QS/16, and 10 MHz on a QS/20. On a QS/20, this option should only be used if all accessory cards can run at 10 MHz.

When setting 2 is in the ON position (default QS/20), the HP Vectra QS uses an asynchronous clock generated by the 82C301 bus controller's 16 MHz backplane crystal oscillator, OSC1, ÷2. That is, 8 MHz.

2.15 PERIPHERAL BUS

The peripheral bus (also known as the X-bus) connects to the 80386 microprocessor the following controllers:

- 82C301 bus controller on the Processor/Memory PCA
- 82C302 page memory controller on the Processor/Memory PCA
- 82C206 integrated peripheral controller (IPC) on the System Interface PCA
- HP-HIL controller (IRD2) on the System Interface PCA
- 8042 keyboard controller on the System Interface PCA
- 8042 port expander on the System Interface PCA.

The 24-bit peripheral address bus (XA) connects the controllers to the 82A303 and 82A304 address buffers (on the Processor/Memory PCA), for connection to the local address bus (A). Through the local address bus and peripheral address bus, the 80386 microprocessor can access the various controller's registers.

The 8-bit peripheral data bus (XD) accesses the backplane I/O system data bus via a transceiver and allows the 80386 to read data from or write data to the control registers. The backplane I/O (system) data bus, in turn, interfaces with the ROM data bus via another transceiver. Via the data buffer, the ROM data bus then connects to the local data bus or the memory data bus.

During DMA cycles, the 82C206 integrated peripheral controller generates a DMA address and sends it over the XA bus, which is connected to the local address bus and the backplane I/O system address bus via the address bus. The BIOS ROMs are addressed through the XA bus; however, data is read directly over the ROM data bus.

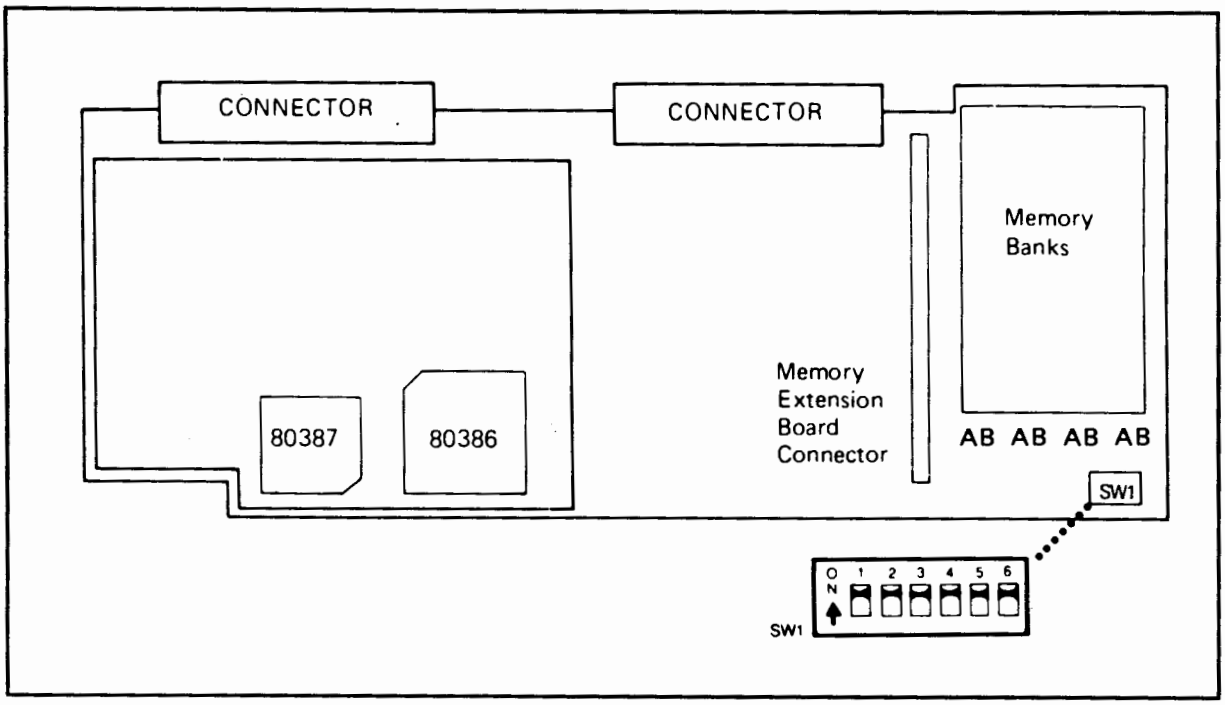

Figure 2-7. QS/16 & QS/20 Processor/Memory PCA Switches

Table 2-2. QS/16 & QS/20 Processor/Memory PCA Default Switch Settings

Switch #	ON	OFF	QS/16	QS/20
1	80387 disabled	80387 enabled	ON	ON
2	Backplane I/O channel speed 8 MHz asynchronous. Derived from the "backplane" oscillator (OSC1)÷ 2	Backplane I/O channel speed 8 MHz (QS/16) or 10 MHz (QS/20*) synchronous. Derived from the clock used by 80386 (OSC2) ÷ 4.	**OFF**	ON
3	Base RAM: 640 KB	Base RAM: 512 KB	ON	ON
4	Option ROM enabled	Option ROM disabled	ON	ON
5	HP Reserved	HP Reserved	ON	ON
6	80387 clock uses same clock as 80386 (OSC2) - synchronous	80387 clock uses the "coprocessor" oscillator (OSC3) - asynchronous	ON	ON

* On the QS/20, switch 2 should only be set to OFF if all accessory cards are designed to run at 10 MHz.

3

QS/16S Processor/Memory Printed Circuit Assembly

3.1 INTRODUCTION

This chapter describes the QS/16S Processor/Memory PCA—a six-layer, surface-mount printed circuit assembly which provides the HP Vectra QS/16S PC with all its RAM, the support circuitry for all buses, and support for the board's subsystems.

Below is a list of the major QS/16S Processor/Memory PCA components. Figure 3-1 shows their layout. Figure 3-2 is a block diagram of the QS/16S Processor/Memory PCA.

Major QS/16S Processor/Memory PCA Components:

Component:	Quantity:	Type:
Microprocessor	1	80386SX @ 16 MHz
CPU/bus controller	1	82C211 @ 16 MHz
Page memory controller	1	82C212 @ 16 MHz
Address and data buffer	1	82C215
Backplane clock, OSC1	1	16 MHz
Processor clock, OSC2	1	32 MHz
System clock, OSC4	1	14.318 MHz
Single in-line memory modules	-	100 ns
Sockets for single in-line memory module	8	
Dip switch bank for configuration	1	
2-connector slot to System Interface PCA	1	
Socket for 80387SX coprocessor	1	

Note: The following components used on the QS/16 & QS/20 Processor/Memory PCA are NOT available on the QS/16S Processor/Memory PCA:

- Coprocessor clock (OSC3) and
- Memory Extension PCA.

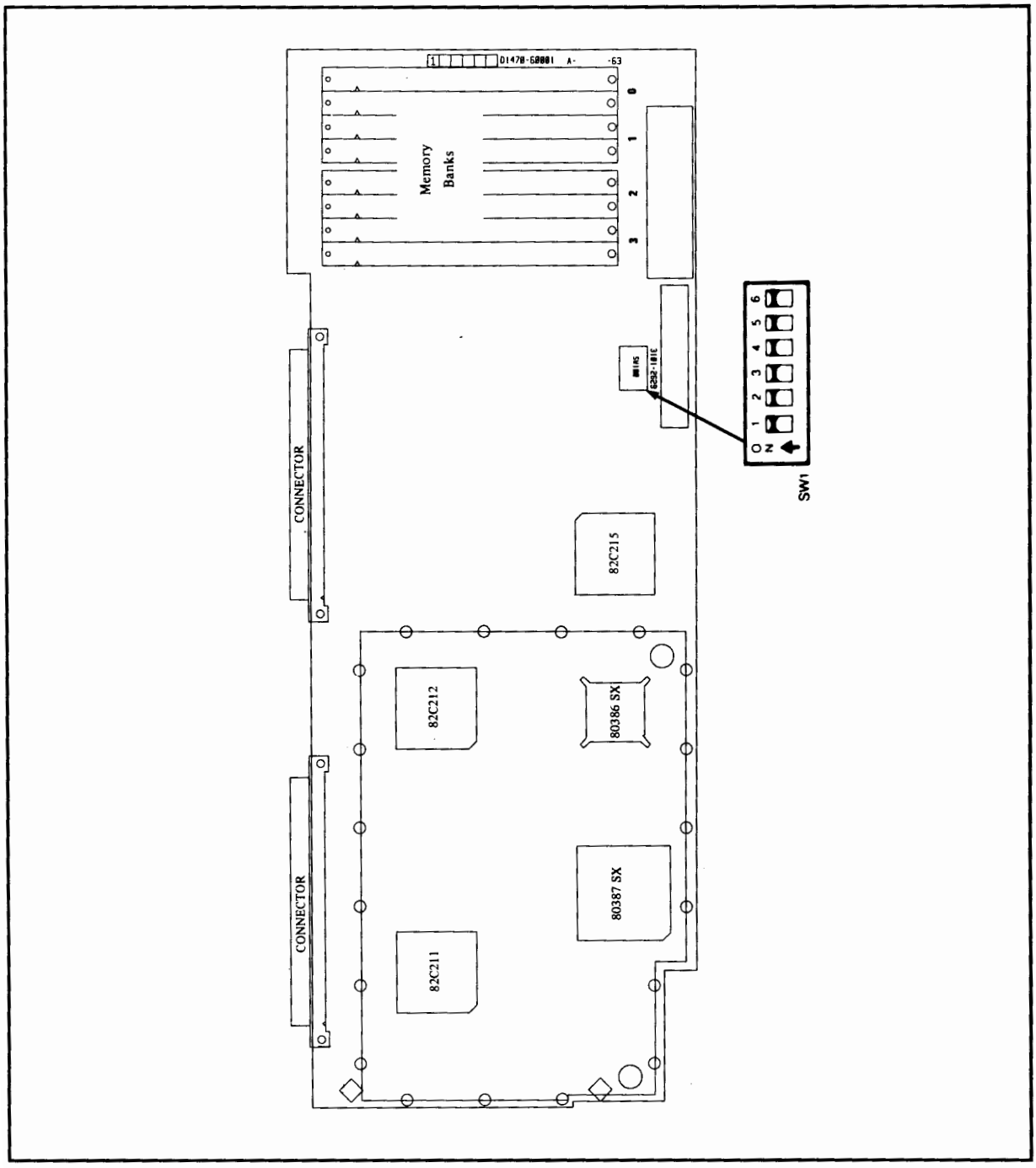

Figure 3-1. QS/16S Processor/Memory PCA Component Layout

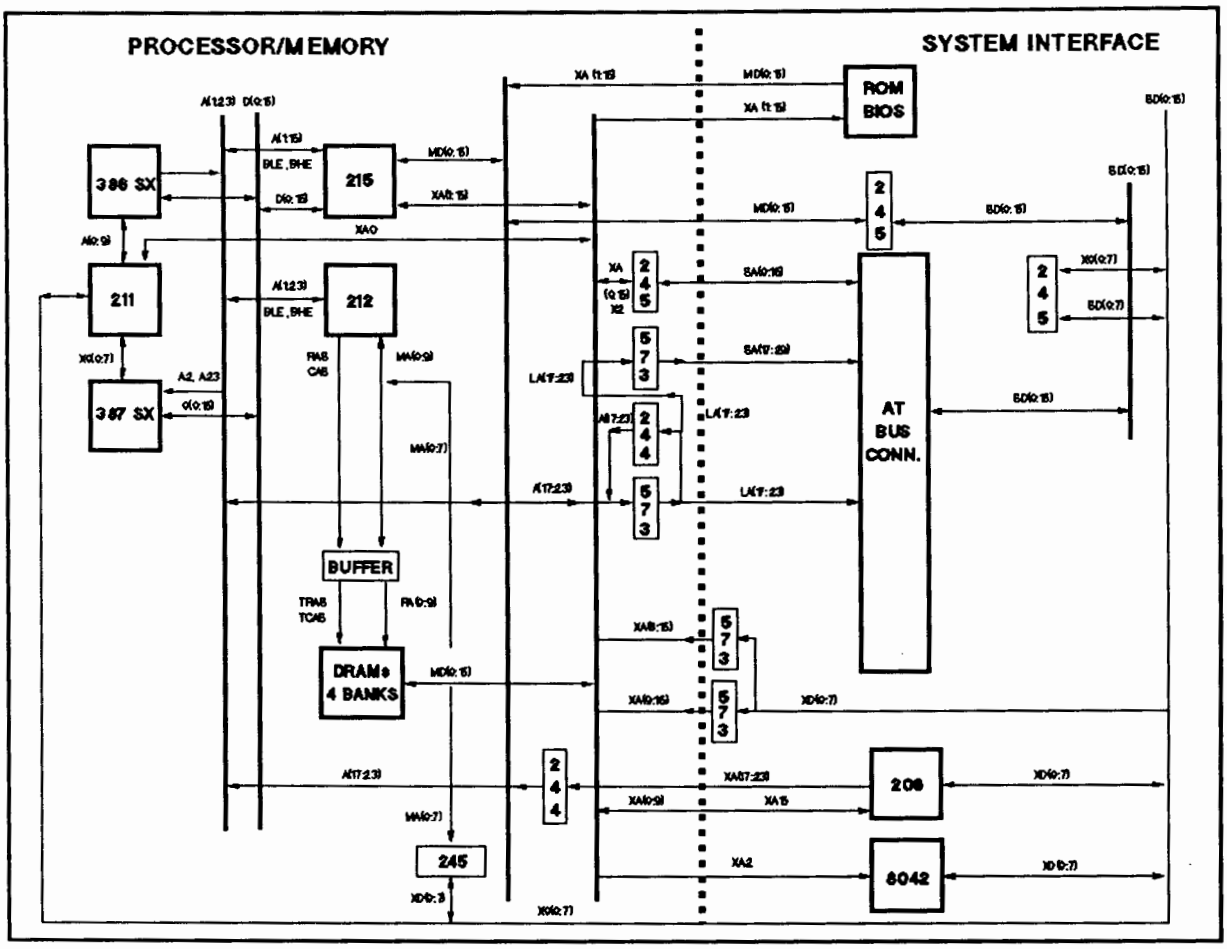

Figure 3-2. QS/16S Processor/Memory PCA Block Diagram

3.2 SYSTEM CLOCKS

The system's main oscillators, located on the QS/16S Processor/Memory PCA, generate the various system clock signals and are discussed under the components for which they provide clocking. (Other oscillators are part of a particular chip or family of chips and are described in the sections covering these chips.)

Oscillator 1 provides 16 MHz for the 82C211 CPU/bus controller.

Oscillator 2 provides 32 MHz for the 82C211 CPU/bus controller.

Oscillator 4 provides 14.318 MHz to the 82C212 page memory controller. This in turn provides the clocking for the integrated peripheral controller, keyboard and HP-HIL controllers on the System Interface PCA. (For further information, see the "Control Buffer" section in this chapter.)

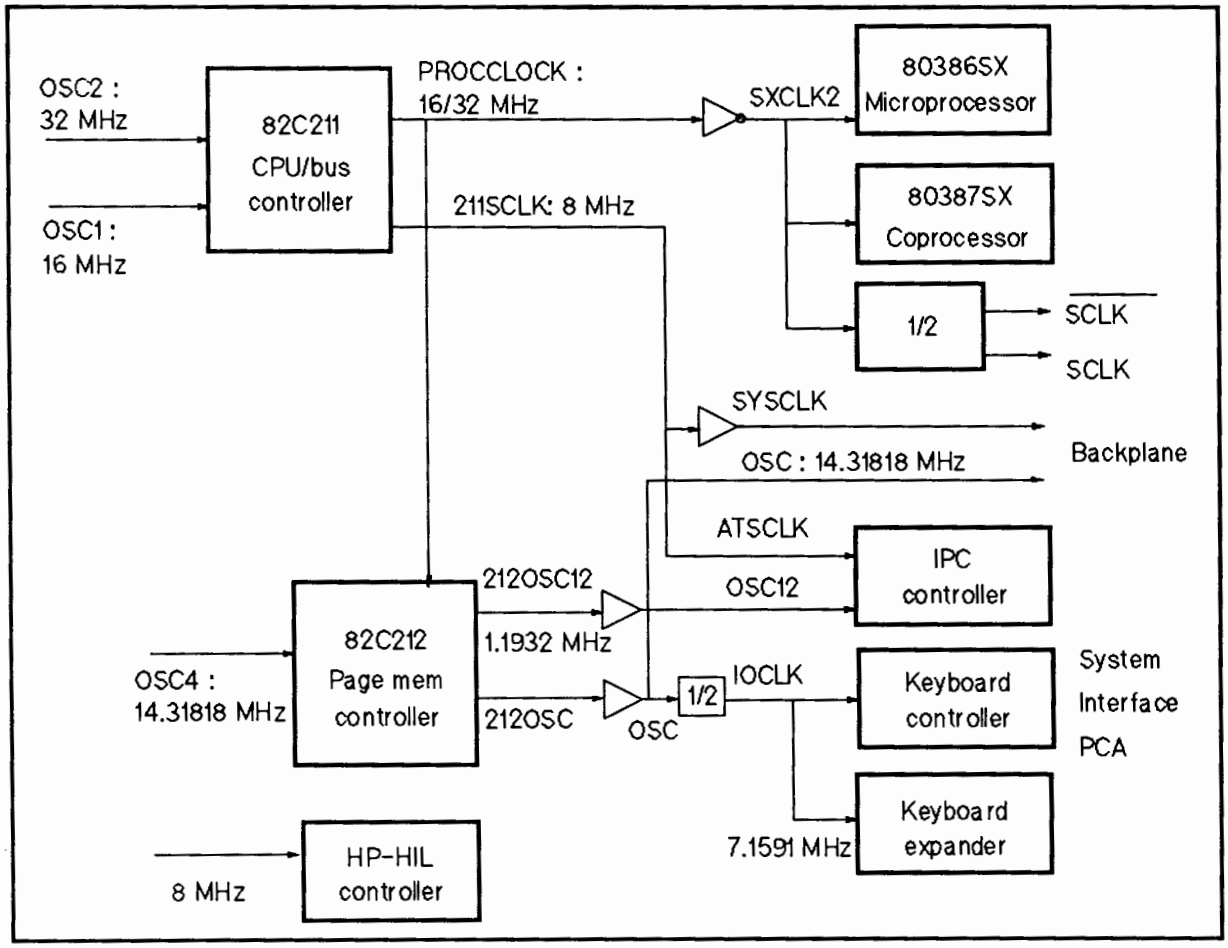

Figure 3-3. QS/16S Processor/Memory PCA Timing

3.3 MICROPROCESSOR

The HP Vectra QS/16S uses the 80386SX microprocessor as the central processing unit. It provides the following:

- 16 MB physical memory capacity.
- 32-bit registers.
- comprehensive instruction set.
- downward compatibility with the 8088, 8086 and 80286 microprocessors, and upward compatible with the 80386 microprocessor.
- interrupt support capabilities.
- processing modes: protected, real-address, and virtual 8086 mode.
- separate 16-bit external data bus and 24-bit external address bus.
- support for 8-, 16-, and 32-bit data types.

Microprocessor Clocking

The HP Vectra QS/16S uses a 16-MHz 80386SX microprocessor, which can also be run at 8 MHz.

The 82C211 CPU/bus controller receives two oscillator inputs, 16 MHz from OSC1 and 32 MHz from OSC2, see Figure 3-3.

The 82C211 CPU/bus controller uses the 32 MHz from OSC2 to generate the signal PROCCLK. However, pressing CTRL Alt \ causes the CPU/bus controller to use the 16 MHz from OSC2÷2 to generate the signal PROCCLK. This is to allow the QS/16S to operate either at 16 MHz or 8 MHz (as PROCCLK is ÷2 within the microprocessor).

The signal PROCCLK is buffered to generate the SXCLK2 signal for the 80386SX microprocessor (and 80387SX coprocessor if fitted).

The 80386SX internally divides the SXCLK2 signal for its own uses.

SXCLK2 also generates the signals SCLK and SCLK# that are used on the Processor/Memory PCA. (For more information, see the "Bus Controller" section in this chapter.)

Microprocessor Compatibility

By dynamically sizing data, the 80386SX microprocessor maintains hardware compatibility with the 8088, 8086, 80286 and the 80386 microprocessors.

The 80386SX microprocessor also maintains software compatibility, in that it runs industry-standard operating systems (including MS-DOS, Microsoft OS/2, and Windows 2.0) and application software developed for systems based on 8088, 8086, 80286 or 80386 microprocessors.

Microprocessor Operating Modes

The 80386SX microprocessor offers the following operating modes:

1. Real-Address Operating Mode

   The 80386SX microprocessor's real-address operating mode is entered when the SPU is powered up or a system reset occurs. This operating mode addresses up to 1 MB of system memory and allows 32-bit operands, but does not provide memory protection.

   Windows 2.0, all versions of MS-DOS, as well as nearly all industry-standard application software, run in the real-address operating mode.

   The real-address operating mode is compatible with operating systems written for the 8086 microprocessor. With a few differences (described in the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers*), the 80386's real-address object code is compatible with the real-address object code of the 8088, 8086, 80286 and 80386 microprocessors.

2. Protected Operating Mode

   The 80386SX microprocessor's protected operating mode provides addressing beyond 1 MB, with up to 16 MB of physical memory available, and supports programs that use memory above 1 MB (VDisk and Disc Cache, for instance).

   When the 80386SX microprocessor is in the protected operating mode, its object code is compatible with that of the 80286 in protected operating mode, but not with an 80286 in the real-address operating mode. In addition, if the 80386SX is in the protected operating mode, its object code is compatible with that of the 8088 or 8086 microprocessor.

3. Virtual-Address Operating Mode

   The virtual-address operating mode allows multiple 8086 sessions of 1 MB each, and can provide access up to 64 terabytes of virtual memory addresses. This mode supports 8088 and 8086 applications that run as a subset of the 80386SX microprocessor's protected operating mode.

   In the virtual-address operating mode, the 80386SX microprocessor's software and operating systems are compatible with those written for the 8088 and 8086 microprocessors.

3.3.1 I/O Address Map

Appendix A gives the I/O address map for the central processing unit. The HP Vectra QS PC uses the first 1024 I/O hex addresses, 0000 through 03FF.

3.4 COPROCESSOR

The HP Vectra QS PC supplies a socket for the industry-standard 80387SX coprocessor. This is a numeric processing unit which significantly improves performance of spreadsheets, CAD/CAE/CAM, engineering, and scientific applications—only applications with built-in support for the coprocessor will have these performance improvements. (Note that a Weitek floating point accelerator cannot be used.)

The coprocessor interfaces directly with the 80386SX; it extends the 80386SX instruction set by providing hardware for BCD data and the high-precision integer functions and floating-point calculations otherwise performed by software.

The HP Vectra QS PC does not come standard with the coprocessor, but it does provide supporting software and an extended math coprocessor socket in which the coprocessor can be installed.

Coprocessor Clocking

The 80387SX coprocessor operates synchronously with the processor clock, see Figure 3-3.

Coprocessor Hardware Interface and Compatibility

1. Hardware Interface

   Immediately after a system power-up or reset, the 80387SX indicates its presence to the 80386SX microprocessor by asserting the NPERR# control signal to the 82C211 CPU/bus controller. (The # symbol at the end of the 80386SX signal names is used by Intel to indicate that the active or asserted state occurs when the signal is at a low-voltage level.)

   Certain software applications may attempt to access the coprocessor even when one is not installed. Consequently, a special circuitry has been developed to prevent the computer from waiting indefinitely for a coprocessor instruction.

   NPERR# must remain asserted after the coprocessor reset signal, RESETIN. Consequently, the NPERR# signal is latched with the RESETIN signal. This latched signal indicates the presence, or otherwise, of the coprocessor. This latched signal is in turn gated with the A23 and M/IO# signals (that select the coprocessor) to control the AF16# signal.

   If an application attempts to access the coprocessor:

   - If the coprocessor is installed, the AF16# signal is set low indicating (to the 82C11 CPU/bus controller) a local bus access. READY# is generated by the coprocessor, allowing the microprocessor to access the coprocessor normally.
   - If a coprocessor is not installed, the AF16# signal is set high indicating (to the 82C11 CPU/bus controller) a peripheral bus access. This causes the AT-state machine to answer READY# after a fixed number of wait states. If this did not occur, the processor would "hang" as the coprocessor is not available to assert the READY#line.

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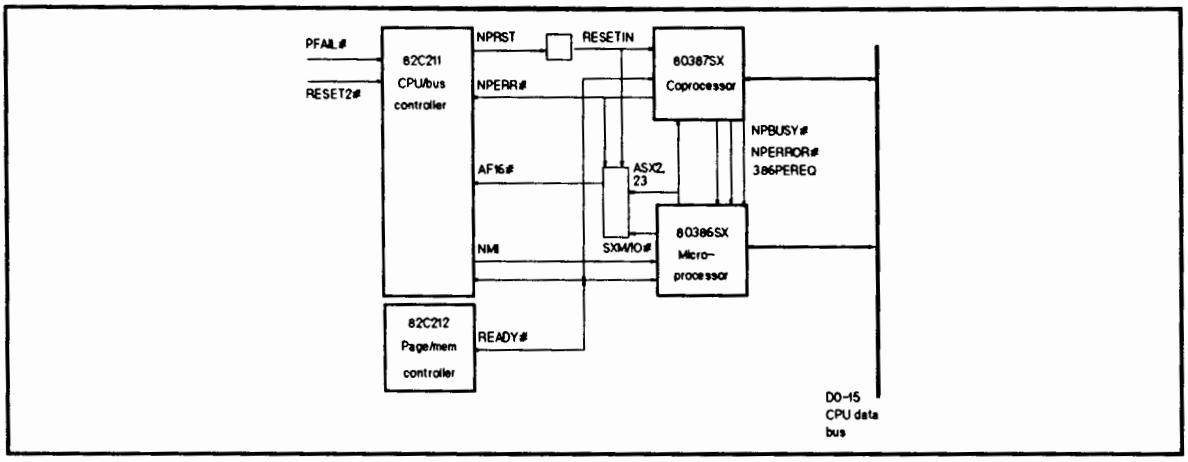

Figure 3-4. Coprocessor Interface

The 80387SX coprocessor is directly connected to the 80386SX microprocessor via the local address and data bus. Three control signals (NPBUSY#, 386PEREQ and NPERROR#) synchronize the transfer of instructions and data between the 80386SX and the 80387SX, see the Intel reference manuals for details.

When the 80386SX selects the 80387SX, it asserts I/O address bit A23 so that the 80387SX acts as an I/O device in a reserved I/O space. Address bit A2 indicates if data or an instruction is being sent to the coprocessor. (For further information, refer to the Intel reference manuals.)

2. Compatibility

   The HP Vectra QS PC numeric coprocessor interface supports the 80387SX coprocessor. The 80387SX coprocessor supports 8087 and 80287 coprocessor instruction sets.

Coprocessor Operating Modes

Since all memory accesses are handled by the 80386SX microprocessor, the 80387SX works the same whether the 80386SX is executing in the real-address, the protected, or the virtual-address operating mode. (For further information on the 80387SX coprocessor, refer to Intel reference manuals.)

3.5 MEMORY

3.5.1 Main Memory (RAM)

The HP Vectra QS PC main memory (also known as system memory, or system RAM, or RAM) consists of dynamic RAM chips mounted on single in-line memory modules.

The modules are available in 256-Kbyte or 1-MB modules and fit into sockets. Eight sockets are available on the QS/16S Processor/Memory PCA Each pair of sockets form a bank, and the banks are labeled "0", "1" "2" and "3". (See the figure in this chapter, "QS/16 Processor/Memory PCA Component Layout" to locate the banks of sockets.)

Main Memory Configurations

This memory is expandable to 8 MB by placing even increments of modules in the sockets, as shown in Table 3-1. Note that this table shows supported memory configurations.

Table 3-1. QS/16S Supported Main Memory Expansion

For Total DRAM of:	Type of Modules Needed:	Sockets Used:
1 MB	4 x 256 KB	All sockets in "0" and "1" banks
2 MB	8 x 256 KB	All sockets in "0", "1", "2" and "3" banks
3 MB	4 x 256 KB **and** 2 x 1 MB	All sockets in "0" and "1" banks, **and** all sockets in "2" bank
4 MB	4 x 1 MB	All sockets in "0" and "1" banks
5 MB	4 x 256 KB **and** 4 x 1 MB	All sockets in "0" and "1" banks, **and** all sockets in "2" and "3" banks
6 MB	6 x 1 MB	All sockets in "0", "1" and "2" banks
8 MB	8 x 1 MB	All sockets in "0", "1", "2" and "3" banks

Base RAM Configurations

The QS/16S Processor/Memory PCA's Switch 1, setting 3, can be used to configure the main memory base RAM as required by applications used.

In the ON position, the main memory's base RAM is set to 640 Kbytes; in the OFF position, base RAM is set to 512 Kbytes.

Main Memory Architecture

The HP Vectra QS/16S has a paged/interleaved main memory architecture, using a 82C212 page/interleave memory controller that organizes main memory DRAM to decrease the number of accesses that incur a wait state penalty.

Paged DRAM is organized into paged rows and columns. One memory strobe (the RAS, or row address strobe) generates the row address (or the page address); a second memory strobe (the CAS, or column address strobe) generates the column address.

If access is required on the same page of DRAM, there may be zero wait states as the row address is already strobed (only CAS is generated). But if access is required on a different page of DRAM, there is at least one wait state.

Interleaved DRAM is organized into four banks, with each bank having two single in-line memory module sockets. Interleaving is only possible for memory configurations with similar pairs of DRAMs, namely 1 MB, 2 MB, 4 MB, 5 MB and 8 MB (see Table 3-1). For more information, see the "Page Memory Controller" section in this chapter.

Memory Map

Figure 3-5 gives the HP Vectra QS PC memory map. As with industry-standard products, the first 1 MB of main memory is reserved for standard memory.

The base RAM (either the first 512 Kbytes or 640 Kbytes of main memory, depending on how the RAM is configured, using Switch 1 setting 3) is used for MS-DOS applications.

From hex address 0A0000 to 0FFFFF, the system reserves main memory for video RAM, I/O adapters, option ROM, and BIOS ROM.

Main memory from hex address 100000 to 7FFFFF is reserved for 16-bit dynamic expansion using the serial in-line memory modules. Main memory from 800000 to FDFFFF can be filled with expansion memory cards plugged in standard I/O slots.

Upon power-up, the 64 Kbytes of option ROM on the System Interface PCA at hex address 0E0000 to 0EFFFF are automatically mapped to hex address FE0000 to FEFFFF; similarly, the 64 Kbytes of BIOS ROM on the System Interface PCA at hex address 0F0000 to 0FFFFF are automatically mapped to hex address FF0000 to FFFFFF.

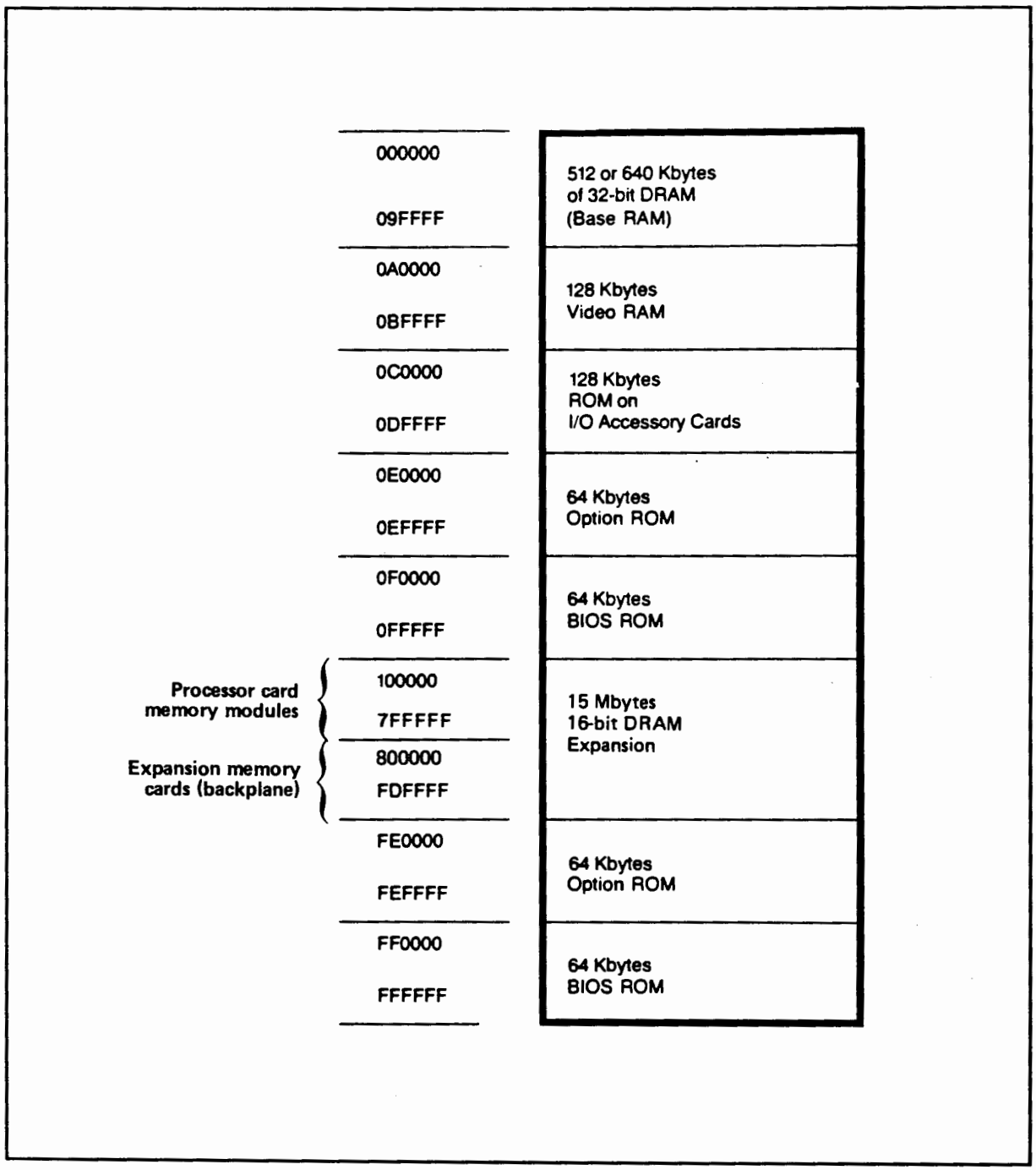

Figure 3-5. HP Vectra QS PC Memory Map

1. Refresh

   All DRAM is refreshed within 4 milliseconds (for 256-Kbyte DRAM) to 8 milliseconds (for 1 MB DRAM).

   A refresh cycle begins with the 82C206 IPC's (integrated peripheral controller on the System Interface PCA) OUT1 pin generating a refresh request (REFREQ) to the 82C211 CPU/bus controller every 15 microseconds.

   To perform a refresh, the 82C211 CPU/bus controller generates a hold request (HOLD) to the 80386SX microprocessor, which subsequently generates a hold acknowledge (HLDA) to the CPU/bus controller.

   When the 82C211 CPU/bus controller receives the HLDA, it puts out the refresh address on A0 to A9 address lines and issues a refresh signal (REF*), which goes to the 82C212 page memory controller and the backplane I/O. The 82C211 CPU/bus controller also issues an address latch enable signal (IALE), which goes to the 82C215 address/data buffer.

   - When the 82C212 page memory controller receives the REF* signal, it uses RAS* to strobe the refresh row address (MA0-9) into the banks of DRAM on the Processor/Memory PCA.
   - When the 82C215 address/data buffer receive the IALE signal, it latches the refresh address lines (A0-9) onto the XA0-9 bus. These signals are buffered to drive system address lines SA0-9, which represents the refresh row address for RAM on the backplane (for I/O accessory cards). Note that the AT standard uses SA0-7 for the refresh operation.

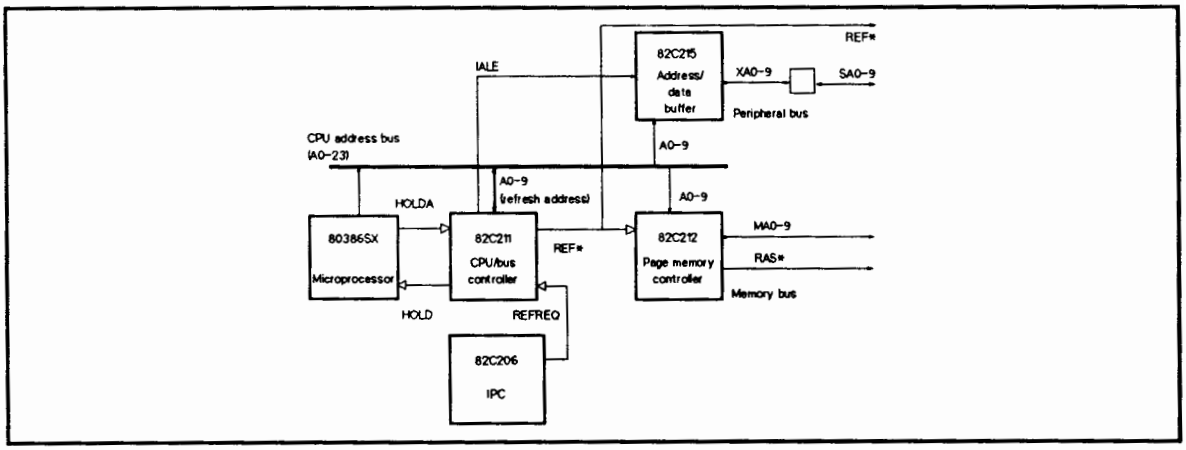

Figure 3-6. Memory Refresh

The REF* signal goes to the backplane I/O and indicates to I/O accessory cards that a refresh operation is taking place.

In addition, an I/O accessory card can issue a REF* signal to initiate a refresh request to the bus controller, the page memory controller, and the address buffers, independent of the IPC's periodic refresh requests (REFREQ).

2. Access Time

   The main memory for the HP Vectra QS/16S uses DRAM with the following access and cycle time:

Access Time:	Cycle Time:
100 nanoseconds	190 nanoseconds

   (Hewlett-Packard assumes no responsibility for the access time of memory modules not supplied by an HP-approved vendor.)

3. Parity

   DRAM uses eight data bits and one parity bit. The 82C215 address/data buffer controls the parity generation and checking.

   The address/data buffer generates parity for each byte of DRAM during write operations, and checks it during read operations.

   If a parity error occurs, a parity check signal PARERR# is generated and sent to the 82C211 CPU/bus controller.

   If parity error detection is enabled, the 82C21 CPU/bus controller generates a non-maskable interrupt (NMI), which is sent to the 80386SX microprocessor via the 8042 port expander. (For details, refer to the "Interrupt Controller" section in the "System Interface PCA" chapter.)

4. Self-tests

   Upon power-up, the main memory goes through a self-test, as discussed in the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

3.5.2 Read-Only Memory

The System Interface PCA provides two 32-Kbyte ROM chips (containing the BIOS firmware) and sockets for two 32-Kbyte option ROM chips. (See the "System Interface PCA" chapter for more information on ROM.)

(*)Active low.

3.6 PAGE MEMORY CONTROLLER

The 82C212 page memory controller:

- Controls all main memory accesses from the 80386SX microprocessor, direct memory access refresh requests
- and organizes the main memory DRAM into paged and interleaved DRAM to decrease the number of accesses incurring a wait state penalty.

OSC4 provides 14.318 MHz to the page memory controller, which is used to generate clock signals 1.19381 MHz OSC12 (to the Intergrated Peripheral Controller on the System Interface PCA) and 14.318 MHz OSC (to the keyboard and HP-HIL controllers on the System Interface PCA), see Figure 3-3.

OSC12 is also used internally to generate the memory row address strobes (RAS#) timeout.

Internal clocking for the page memory controller comes from the signal PROCCLK, which originates from the 82C211 CPU/bus controller.

DRAM chips are physically organized onto single in-line memory modules, which can make up to four 2-byte wide banks: banks "0", "1", "2" and "3". If two 256-Kbyte modules are used, a bank has 512 KB of DRAM; if two 1-MB modules are used, a bank has 2 MB of DRAM. (Refer to the "Main Memory" section and the "Main Memory Expansion" table in this chapter for more information on the physical organization of the DRAM.)

The page memory controller logically organizes DRAM as *pages*. For each 256-Kbyte module, there are 512 pages (rows), with each page having 512 bytes (1 byte for each 512 columns). Since a bank has two single in-line memory modules, a banked page has 1 KB of dynamic RAM (i.e. 512 bytes x 2 modules = 1 KB). This paged memory can be accessed as 8-bit bytes or 16-bit words.

To access memory, the page memory controller issues to each accessed module a row address and then a column address. The row address indicates the page, while the column address indicates which of the 512 bytes on that page (row) are to be accessed.

The row and column addresses are multiplexed over MA0-MA9 from the page memory controller and are latched into a memory module by the appropriate row address strobe (RAS) and column address strobe (CAS) signals. The RAS line drives each 256 x 18-bit bank (16-bit word) and the CAS line drives each individual byte within the bank.

If the next access is within the current page (row), a new row address does not need to be issued, just a new column address and CAS signal, resulting in fewer wait states.

If more than one bank of sockets are filled with DRAM modules, the page memory controller *interleaves* the pages between banks, with even pages on one bank, and odd pages on the next bank. Interleaving requires that two or four (but never three) banks of sockets be filled with DRAM modules. If more than one bank of sockets is to be filled, the two banks making up a pair of banks must each use the same type of modules, but two pairs can use different types of modules.

Interleaving pages on different banks can minimize the number of row addresses and RAS signals required, as the page memory controller has a separate page register for each bank. If bank "0" has an even page number as its current page, and bank "1" has the next (odd) page number as its current page, no new row addresses or RAS signals are needed as long as accesses are within these two pages.

Once the 80386SX microprocessor generates a local address, the page memory controller decodes the type of access according to its various configuration registers. These registers determine if a ROM access, an access of the backplane I/O, or a DRAM access is required. If a DRAM access is required, the page memory controller accesses the DRAM according to configuration registers that state what type of DRAMs are used and how many wait states are desired.

In direct-memory accesses (DMA), only 8-bit and 16-bit operations are supported. The address on the local address bus comes from the System Interface PCA's 82C206 Integrated Peripheral Controller via the peripheral address bus and the address buffers. The page memory controller decodes the address as it would an access from the 80386SX microprocessor.

A refresh access is initiated when the page memory controller receives a REF* input from the 82C211 CPU/bus controller. The refresh row address is strobed into each bank. (For more information on the 82C212 page/interleave memory controller, consult the Chips and Technologies data sheet, *CS8221: New Enhanced AT (Neat™) Data Book.*)

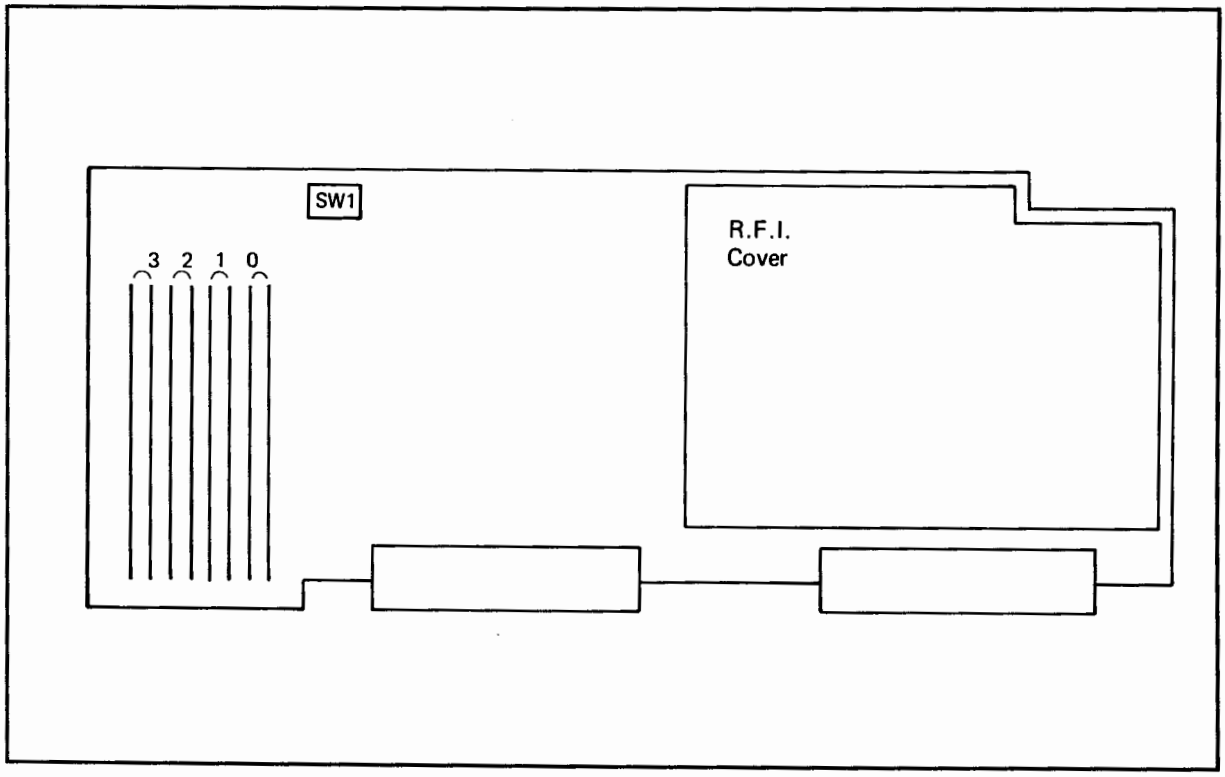

Figure 3-7. QS/16S Physical Organization of DRAM (Board/Memory Modules View)

* Active low

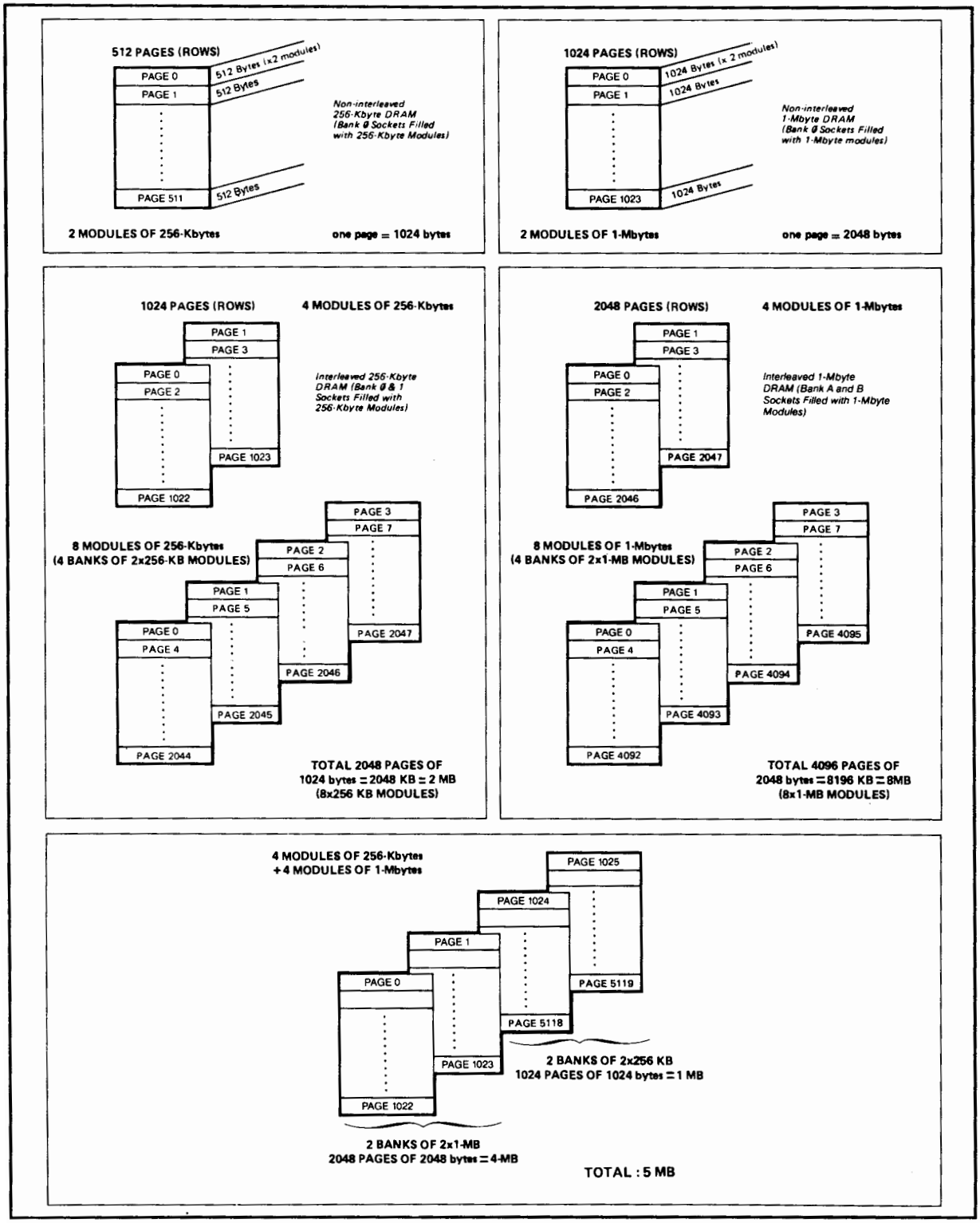

Figure 3-8. Logical Organization of DRAM

3.7 BUS CONTROLLER

The 82C211 CPU/bus controller generates clocking for the 80386SX microprocessor, the coprocessor, and the page memory controller.

The bus controller also provides the generation and synchronization of control signals for all buses. In addition, it offers an industry-standard Port B status register, and optional speeds for timing-dependent software. (For more information, refer to Chips and Technologies Reference Manuals.)

Bus Controller Clocking

Figure 3-3 depicts the bus controller clocking.

The clock input to the CPU/bus controller is provided by ATCLK1 (OSC1, 16 MHz) and CLK2IN (OSC2, 32 MHz).

The CPU/bus controller's PROCCLK output signal is normally derived from OSC2 (32 MHz). Pressing Ctrl Alt \ causes CLK2 to be derived from OSC2 ÷2, for a 16-MHz signal.

PROCCLK is buffered to provide the clock SXCLK2 to the microprocessor and coprocessor. PROCCLK is also used by the 82C212 page memory controller for internal clocking.

In addition, PROCCLK is divided by two to provide signals SCLK and SCLK# that are used in various timing circuits on the Processor/Memory PCA.

The CPU/bus controller's 211SCLK output signal is derived from OSC2 div;4.

211SCLK is buffered to drive the clock signal SYSCLK, the signal for the industry-standard backplane I/O bus. In addition, 211SCLK is buffered to provide the signal ATSCLK which is sent to the 82C306 Integrated Peripheral Controller (on the System Interface PCA).

For more information, refer to Chips and Technologies Reference Manuals.

Bus Arbitration

The 82C211 CPU/bus controller synchronizes control of all bus activities. For direct memory accesses (DMA), the bus controller accesses memory as described in the "DMA Controller" section of Chapter 4. The bus controller has the following two state machines that control access to devices by the 80386SX microprocessor:

1. The *local bus state machine,* controls accesses by the 80386SX to devices on the local bus. It also supports 16-bit transfers between the 80386SX and system memory (or memory-mapped I/O), but does no data size conversions.
2. The *AT (industry-standard) bus state machine,* controls the 80386SX microprocessor accesses to devices on non-local buses. It provides sequencing and timing controls (including wait state generation) for status and command phases of the different bus cycles. In addition, it generates action control code signals that go to the data buffers for data size conversions.

IF AF16# is asserted low, the local bus machine state is initiated by the 82C211. If AF16# is asserted high, the AT bus machine state is initiated.

CPU/Bus Controller Control Buffer

The 82C211 CPU/bus controller buffers control signals from the microprocessor for use by the local peripherals and the backplane I/O.

CPU/Bus Controller NMI Control

The 82C211 CPU/bus controller controls the generation of a non-maskable interrupt (NMI) when a parity error is detected by the 82C215 address/data buffer. Refer to "Main Memory (RAM)" in this chapter.

CPU/Bus Controller Reset Control

When the power supply's PFAIL* signal goes low (detected at the CPU/bus controller's RESET1* pin, see Chapter 5 for details), it activates the bus controller's RESET3 and RESET4.

RESET3 — Resets the 80386SX microprocessor, the 80387SX coprocessor and various Processor/Memory PCA timing circuits.

RESET4 — Provides the backplane I/O connector slots with a reset for input devices and resets the following:

- 82C212 page memory controller
- 82C206 IPC (integrated peripheral controller)
- 8042 keyboard controller
- 8042 keyboard controller port expander
- HP-HIL master controller (IRD2)

For more details on the PFAIL signal, refer to the chapter *Power Supply.*

Note that simultaneously pressing Ctrl Alt Del causes a soft reset - no reset lines are activated.

However, it is possible to reset the microprocessor by writing FEh to I/O address 64 (within the 8042 keyboard controller on the System Interface PCA). This activates RESET2*, which in turn activates RESET3. This is provided for compatibility with the AT 286 computers, as it is the only way to return from protected mode to real mode.

* Active low

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3.9 ADDRESS/DATA BUFFERS

Address buffer. The 82C215 address/data buffer supports transfers on the following address buses (see Figure 3-9):

- A, the local address bus to the 80386SX microprocessor and the coprocessor.
- XA, the peripheral address bus for the keyboard controller 8042 keyboard controller port expander, HP-HIL Controller (IRD2), and 82C206 IPC (integrated peripheral controller).

  The XA bus is buffered to provide the SA bus - the system address bus for the backplane I/O.

The 82C215 acts as a buffer for local address bits A1 through A16, and peripheral address bits XA1 through XA16.

Data buffer. The 82C215 address/data buffer supports transfers on the following data buses (see Figure 3-10):

- D, the local data bus to the 80386 microprocessor and the coprocessor
- MD, the system memory data bus to the dynamic RAM and the ROM data bus connected to the BIOS ROMs
- SD, the system data bus to the backplane I/O, connected to the MD by a transceiver
- XD, the peripheral data bus to the keyboard controller 8042 keyboard controller port expander, HP-HIL controller (IRD2) and the 82C206 IPC (on the System Interface PCA), connected to SD by a transceiver

Via D and MD, the 82C215 supports data transfers between the 80386SX microprocessor and the system RAM and ROM.

Via D and SD, the 82C215 also supports data transfers between the 80386SX and the industry-standard backplane connector slots.

During direct-memory accesses, the data buffers provide data bus connections that convert data words to a size compatible with backplane I/O operations.

Control of Data Bus Buffers

According to signals received from the bus controller and the page memory controller, the 82C215 determines (1)which data buses are active (i.e. connected) and (2)the subsequent direction for data bus buffer drivers.

Data Conversion

The 82C215 converts data to a size permitting the 80386SX microprocessor to access the I/O bus. Data is converted via action code control signals from four bus controller lines to the data buffer; these codes control the connection of bus bits between (1)the system data bus for the backplane I/O and (2)either the local data bus or the memory data bus.

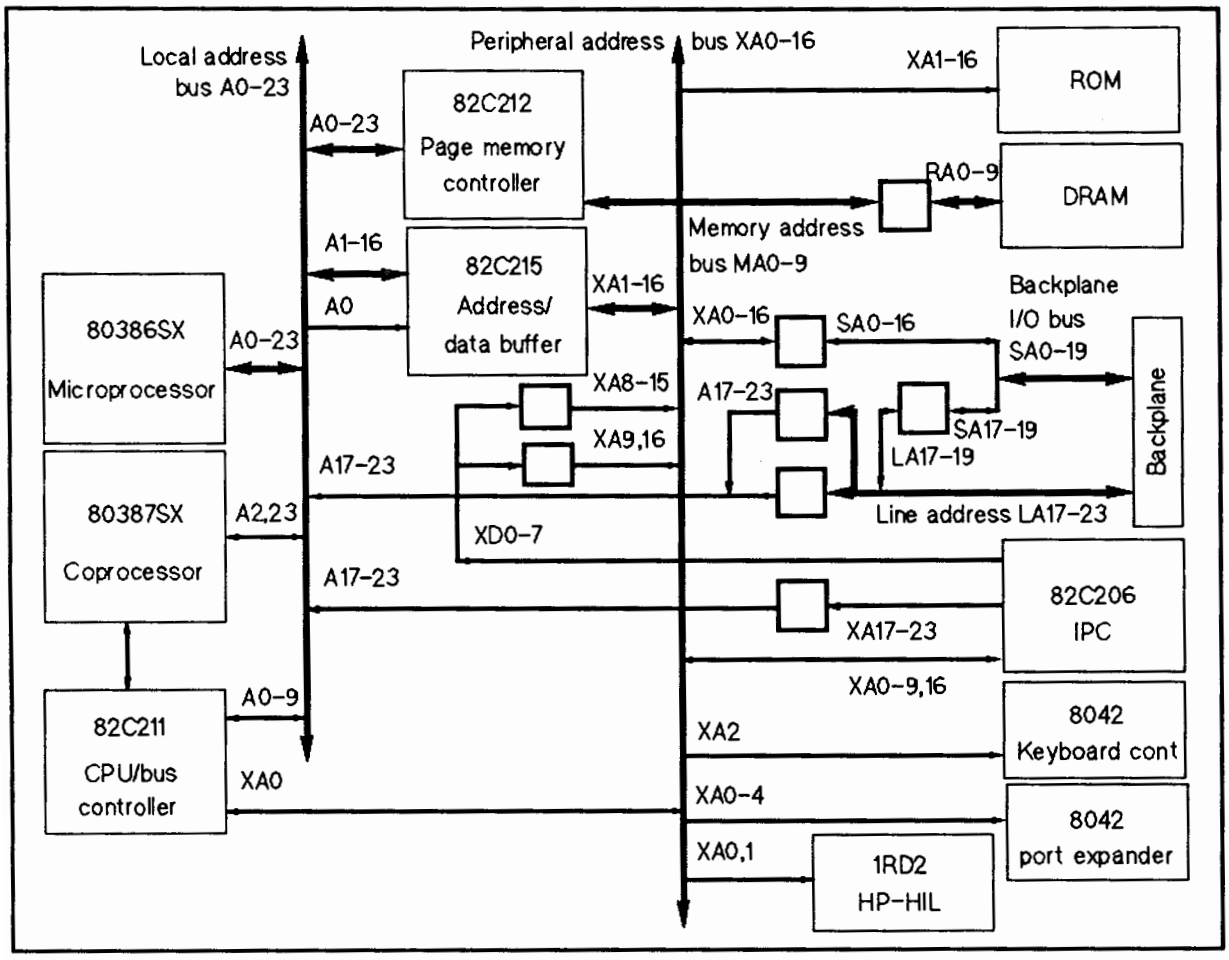

Figure 3-9. Address Control

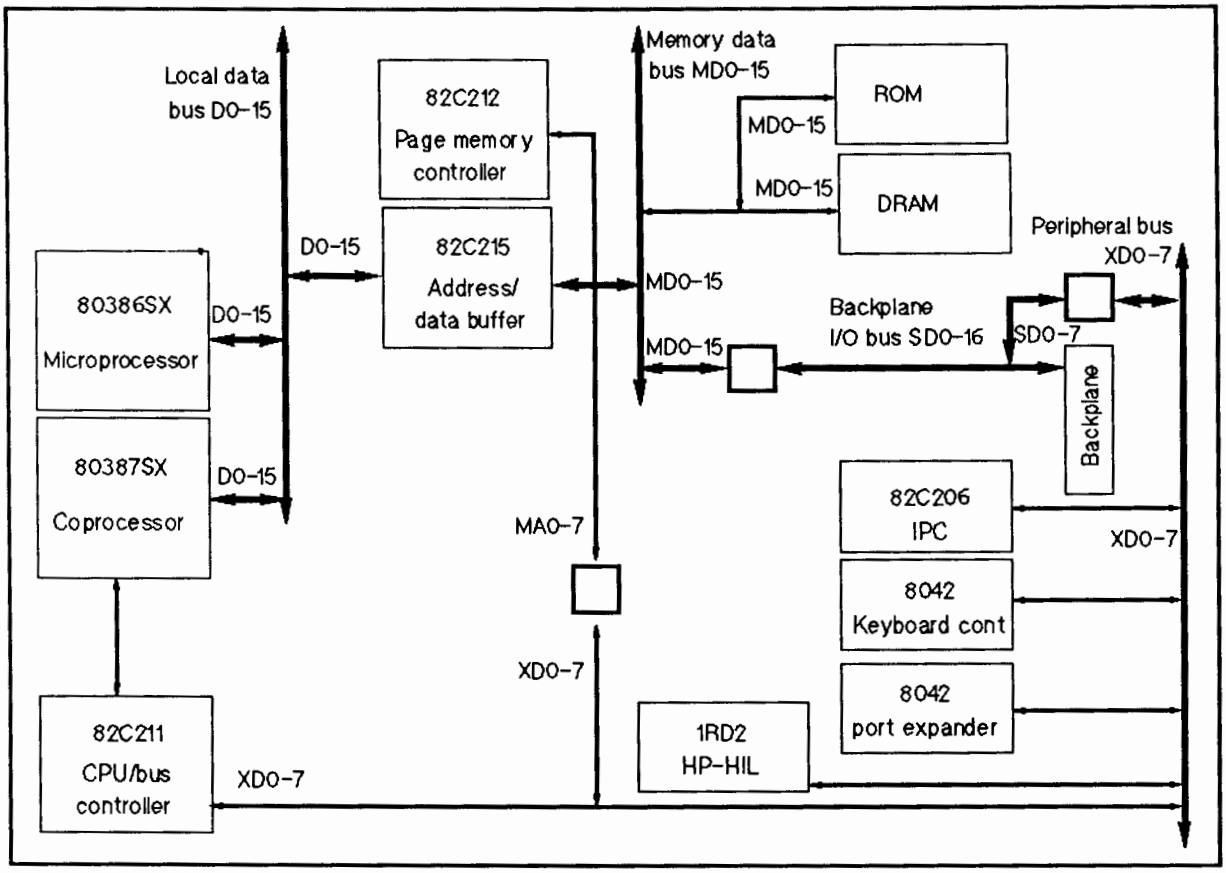

Figure 3-10. Data Control

3.10 LOCAL BUS (LBUS)

The local bus consists of the local address bus (A), the local data bus (D), bus status pins, and bus control pins for the 80386SX microprocessor (and the coprocessor, if installed). The local bus connects the 80386SX microprocessor and the coprocessor to the rest of the system.

Separate from the local data bus, the local address bus generates 24-bit addresses. The 23 address lines (A23 to A1) indicate a 16-bit (2 byte) location, and the two byte-select signals BLE# and BHE# distinguish the lower(L) and higher(H) byte on the 16-bit data bus.

The 16 local data bus lines (D15 to D0) transfer either 8 or 16 bits of data (selected by BLE# and BHE#).

The 82C215 address/data buffer uses the local bus control pins to control the bus cycle on a cycle-by-cycle basis.

At the start of a local bus cycle, the 80386SX microprocessor places valid address signals on the local address bus (A). These signals go to:

1. The 82C215 address/data buffer (and then to other buses)
2. The 82C212 page memory controller, which interfaces with the DRAM
3. The coprocessor.

Status signals corresponding to the bus cycle to take place are then sent to the address/data buffer, page memory controller, and coprocessor. Data to/from the 80386SX microprocessor are sent over the local data bus (D) to/from the data buffers.

3.12 MEMORY BUS

The memory data bus (MD) is 20 bits wide (16 data bits, with 4 parity bits). The system memory data bus interfaces to the local data bus (used for DRAM and ROM), through the 82C215 address/data buffer.

The Memory Address Bus (MA) is an 10-bit bus (MA0-MA9) from the 82C212 page memory controller that accesses a particular DRAM location. (The RAS and CAS strobes complete the memory address scheme.)

3.13 READ-ONLY MEMORY BUS

In addition to the data to/from the DRAM: All data coming from the BIOS ROMs or option ROMs (on the System Interface PCA), or going to or from the peripheral data bus or the backplane I/O data bus, go over the 16-bit memory data bus (MD).

Via the 82C215 address/data buffer, the local data bus interfaces with the MD. Through a transceiver, MD interfaces with the backplane I/O data bus (SD), which in turn, interfaces with the peripheral data bus (XD) through another transceiver.

3.14 BACKPLANE I/O BUS (SBUS)

The HP Vectra QS PC backplane I/O bus, an industry-standard 8-MHz bus (also known as the S-bus, or system bus) is separate from the system memory bus. It connects to the rest of the computer system via one 8-bit and six 16-bit backplane I/O connector slots. Further information is to be found in the chapter "System Interface Printed Circuit Assembly."

The system address bus (SA) is a 24-bit address bus (SA0-19 and LA17-23), connected to other address buses in the system. Backplane I/O connector slots can receive an address from any of the other address buses or generate an address to any of the other buses, depending on the operation involved. (For more information, see the section on "Address/Data Buffers" in this chapter.)

The system data bus (SD) is a 16-bit data bus (D0-D15) over which data to/from the backplane I/O connector slots is sent. This data, in turn, is sent over the memory data bus to the data buffers on the Processor/Memory PCA for connection to the rest of the system.

If a backplane I/O connector slot needs control of the system, it holds MASTER* low. After the appropriate protocol has been completed, an address originating from an I/O accessory card is sent over SA to other address buses in the system.

If the 80386SX microprocessor needs to access a backplane I/O connector slot, an address is sent over the local address bus, through the address buffers, and then to SA.

During direct-memory access (DMA) operations, an address originating from the integrated peripheral controller's DMA controller is sent over the peripheral bus to both the S-bus and the local bus.

3.15 PERIPHERAL BUS

The peripheral bus (also known as the X-bus) connects to the 80386SX microprocessor the following controllers:

- 82C215 address/data buffer on the Processor/Memory PCA
- 82C212 page memory controller on the Processor/Memory PCA
- 82C206 integrated peripheral controller (IPC) on the System Interface PCA
- 8042 keyboard controller on the System Interface PCA
- 8042 port expander on the System Interface PCA
- HP-HIL controller (IRD2) on the System Interface PCA

The 82C215 address/data buffer connects the 16-bit peripheral address bus (XA) to the local address bus (A). Through the local address bus and peripheral address bus, the 80386SX microprocessor can access the various controller's registers.

The 8-bit peripheral data bus (XD) accesses the backplane I/O system data bus via a transceiver and allows the 80386SX to read data from or write data to the control registers. The backplane I/O (system) data bus, in turn, interfaces with the memory data bus via another transceiver.

During DMA cycles, the 82C206 integrated peripheral controller generates a DMA address and sends it over the XA bus, which is connected to the local address bus and the backplane I/O system address bus. The BIOS ROMs are addressed through the XA bus; however, data is read directly over the memory data bus.

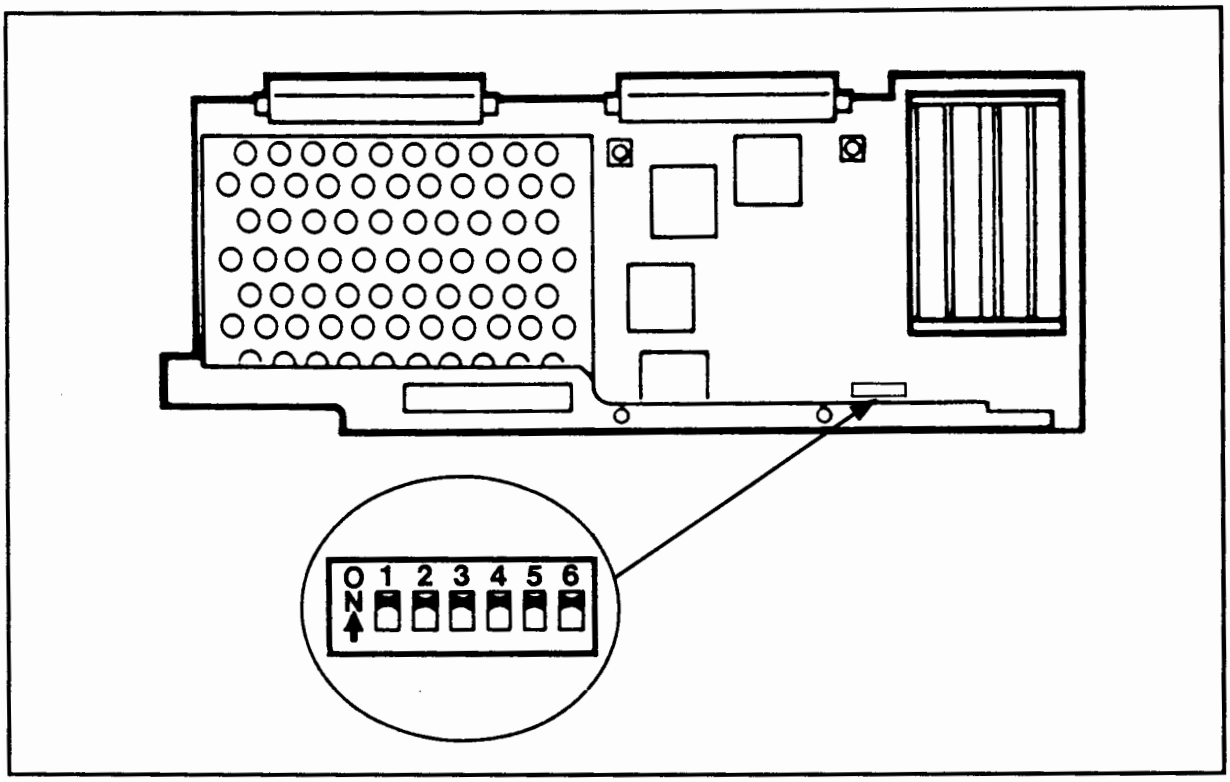

Figure 3-11. QS/16S Processor/Memory PCA Switches

Table 3-2. QS/16S Processor/Memory PCA Default Switch Settings

Switch #	ON	OFF	QS/16S
1	HP Reserved	HP Reserved	Not used
2	HP Reserved	HP Reserved	Not used
3	Base RAM: 640 KB	Base RAM: 512 KB	ON
4	Option ROM enabled	Option ROM disabled	ON
5	HP Reserved	HP Reserved	Not used
6	HP Reserved	HP Reserved	Not used

4

System Interface Printed Circuit Assembly

4.1 INTRODUCTION

This chapter describes the System Interface PCA, which provides I/O support circuitry as well as the interconnection point for all other PCAs used in the system processing unit (SPU). Below is a list of the major System Interface PCA components, the layout for which is given in Figure 4-1. Figure 4-2 is a block diagram of the System Interface PCA. A discussion of the PCA's main components and their operation follows.

The major System Interface PCA components:

Component:	Quantity:
82C206 Integrated Peripheral Controller	1
8042 keyboard controller	1
8042 Keyboard Controller Port Expander	1
1RD2 HP-Human Interface Link controller	1
32-Kbyte BIOS ROMs	2
Sockets for option ROMs	2
Backplane I/O connector slots	7
2-connector slot to Processor/Memory PCA	1
Power connector	1

Note

In this chapter, both the 80386 microprocessor and the 80386SX microprocessor are referred to by the generic name 80386.

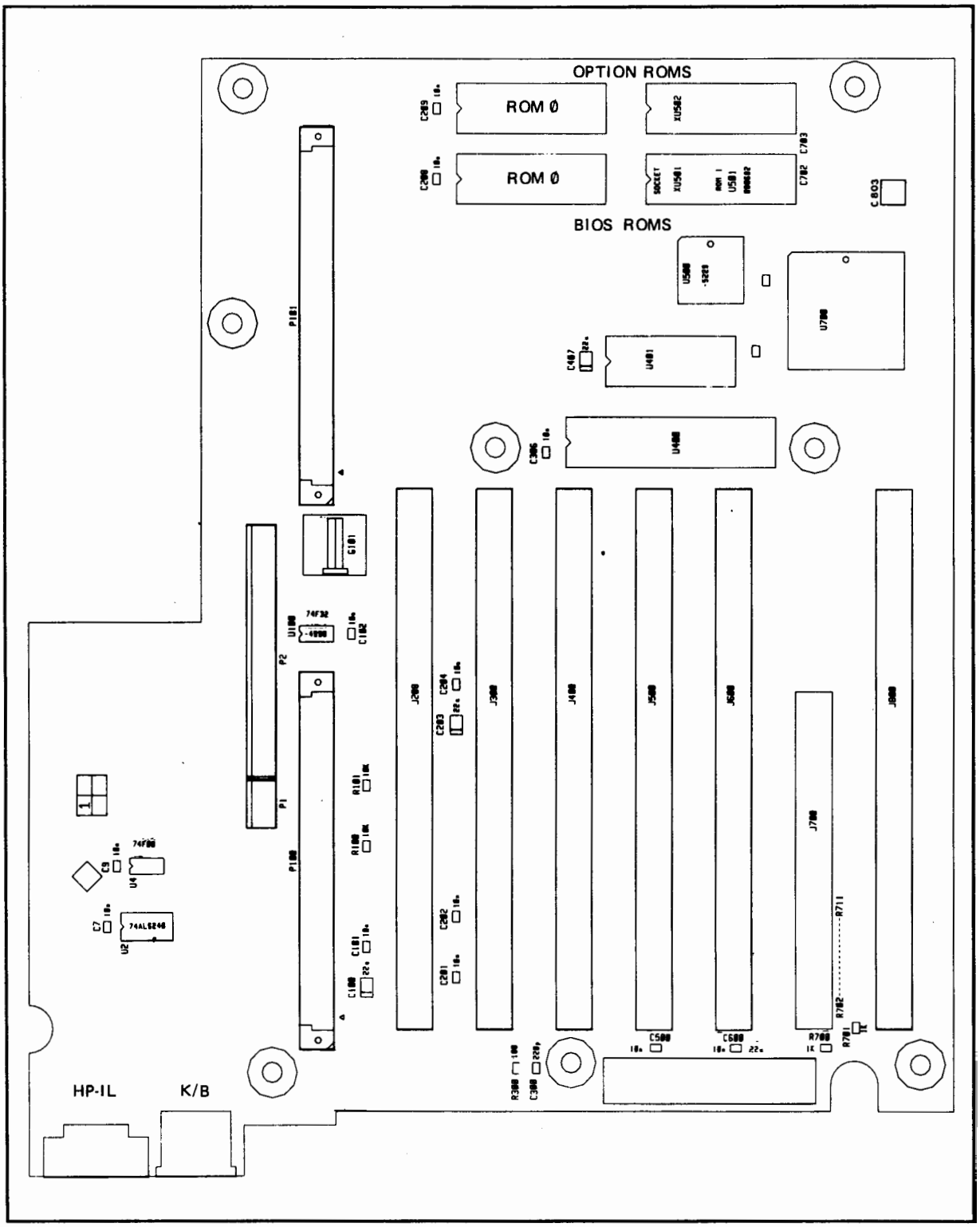

Figure 4-1. System Interface PCA Component Layout

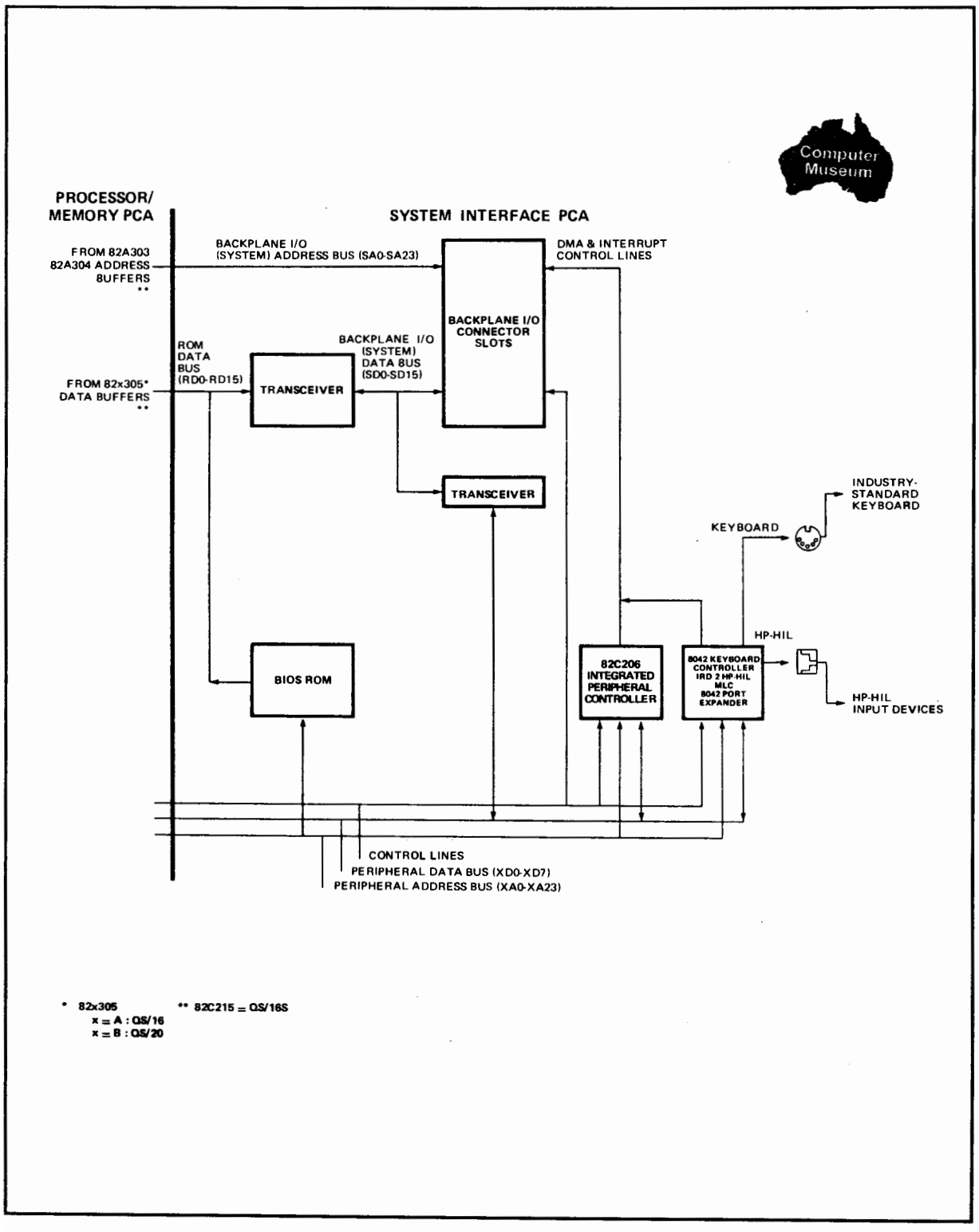

Figure 4-2. System Interface PCA Block Diagram

4.1.1 PC Type Selection

The System Interface PCA used on the Vectra QS/16S has a "PC type" circuitry that allows it to be used with the Vectra QS/16 and QS/20. (The current QS/16 and QS/20 System Interface PCA cannot be used with the QS/16S.)

The "PC type" circuitry uses the state of the CPUTYPE signal to switch certain other signals.

- When a QS/16 or QS/20 Processor/Memory PCA is fitted, pin 31 on the CPU connector is grounded, and signal CPUTYPE is set low.
- When a QS/16S Processor/Memory PCA is fitted, pin 31 on the CPU connector is open circuit, and signal CPUTYPE is pulled up to +5V (high).

The CPUTYPE signal is decoded in the buffer, such that when CPUTYPE is low (QS/16 and QS/20), signals LA17, LA18, LA19, XMEMR# and SDIRO drive signals SA17, SA18, SA19, ROMRD# and SDIR1.

When CPUTYPE is high (QS/16S), signals LA17, LA18, LA19, XMEMR# and SDIRO do NOT drive signals SA17, SA18, SA19, ROMRD# and SDIR1. Instead, signals SA17, SA18, SA19, ROMRD# and SDIR1 are driven normally.

Line address signals LA17 to LA19 are faster than SA17 to SA19 for I/O cards that must generate signals IOCS16# and MEMCS16#.

The ROMRD# signal controls the BIOS and option ROMs.

The SDIR1 signal controls system data bus lines SD8 to SD15.

4.2 INTEGRATED PERIPHERAL CONTROLLER

The 82C206 Integrated Peripheral Controller (IPC) is made up of an internal decode system and a clock and wait-state control system. It interconnects and controls four main IPC subsystems: DMA controller, interrupt controller, counter/timer, and real-time clock/CMOS RAM.

Table 4-1 gives the I/O address map for the IPC components. (For more information on the IPC, consult the Chips and Technologies data book, *82C206 Integrated Peripherals Controller,* and the 82C series of technical reference documents.)

The major IPC components are:

2 x 8237A DMA controller (DMA channels: 4 for 8-bit transfers, 3 for 16-bit transfers).
2 x 8259A interrupt controllers (13 interrupt request channels)
1 x 8254 counter/timer (3 counter/timer channels)
1 x 146818 real-time clock with CMOS RAM
1 x 74LS612 DMA page register

Table 4-1. I/O Addresses for IPC Components

IPC Block	Hex Addr	Register Function
DMA Controller	0000	Channel 0 Address (8 bit - DREQ0)
No. 1*	0001	Channel 0 Count
	0002	Channel 1 Address (8 bit - DREQ1)
	0003	Channel 1 Count
	0004	Channel 2 Address (8 bit - DREQ2)
	0005	Channel 2 Count
	0006	Channel 3 Address (8 bit - DREQ3)
	0007	Channel 3 Count
	0008	Read Status/Write Command
	0009	DMA Request
	000A	Read Command/Write Single Mask Register Bit
	000B	Mode Register
	000C	Byte Pointer Flip-Flop
	000D	Read Temporary Register/Write Master Clear
	000E	Clear Mode/Clear Mask Register
	000F	Read/Write All Mask Register Bits
Interrupt Controller	0020	Master Interrupt Controller Register 0
No. 1 (INTC1)	0021	Master Interrupt Controller Register 1
DMA Configuration	0022	Index Register
Register	0023	Data Register

Table 4-1. I/O Addresses for IPC Components (continued)

IPC Block	Hex Addr	Register Function
Counter/Timer	0040	Channel 0 timer
	0041	Channel 1 counter
	0042	Channel 2 counter
	0043	Command mode register
Real-Time Clock/CMOS RAM	0070	Real-Time Clock Address (D0-D6) NMI enable (D7) (Write)
	0071	Real-Time Clock/CMOS RAM Data (Read/Write)
DMA Page Register	0081	8-bit DMA Channel 2 A16-A23
	0082	8-bit DMA Channel 3 A16-A23
	0083	8-bit DMA Channel 1 A16-A23
	0087	8-bit DMA Channel 0 A16-A23
	0089	16-bit DMA Channel 6 A17-A23
	008A	16-bit DMA Channel 7 A17-A23
	008B	16-bit DMA Channel 5 A17-A23
	008F	Refresh
Interrupt Controller No. 2 (INTC2)	00A0	Slave Interrupt Controller Register 0
	00A1	Slave Interrupt Controller Register 1
DMA Controller No. 2*	00C0	Channel 4 Address (16 bit - cascade)
	00C2	Channel 4 Count
	00C4	Channel 5 Address (16 bit - DREQ5)
	00C6	Channel 5 Count
	00C8	Channel 6 Address (16 bit - DREQ6)
	00CA	Channel 6 Count
	00CC	Channel 7 Address (16 bit - DREQ7)
	00CE	Channel 7 Count
	00D0	Read Status/Write command
	00D2	DMA Request
	00D4	Read Command/Write Single Mask Register Bit
	00D6	Mode Register
	00D8	Byte Pointer Flip-Flop
	00DA	Read Temporary Register/Master Clear
	00DC	Clear Mode/Clear Mask Register
	00DE	Read/Write All Mask Register Bits

*Note: I/O registers for DMA controller 1 (for 8-bit transfers) are located on consecutive addresses, while I/O registers for controller 2 are on even-byte addresses. All DMA registers should be loaded with valid parameters after power-up or reset, even if some channels are unused.

4.2.1 DMA Controller

Direct memory access (DMA) is provided by the 82C206 IPC's DMA controller, which consists of two four-channel DMA controllers (equivalent to two 8237As), the DMA address map, DMA address map selects, and the DMA page register (equivalent to a 74LS612 page register). (See the "I/O Addresses for IPC Components" in this chapter for a breakdown of DMA register assignments.)

DMA Controller Operation

1. Clock Cycle

   Depending on the configuration of Switch 1 setting 2, the QS/16 and QS/16S can operate from a 4-MHz clock, and the QS/20 from a 4-MHz or 5-MHz clock.

   This clock is derived by dividing the backplane I/O clock by two, and all DMA data transfers use five DMA clock cycles.

2. Operating Conditions

   The IPC's DMA controller has three types of operating conditions: program, idle, or active. Once the program condition has been entered to program the DMA controller registers, the DMA controller operates in either the idle or the active condition. In the idle condition, the DMA controller waits for an I/O device to request direct-memory access through one of the 7 DMA channels. When the DMA controller receives a DMA request from an I/O device, it enters the active condition, resolves priority for the channel requesting DMA, and issues HRQ1 (a hold request) to the 82C301 bus controller.

   The bus controller, in turn, generates a hold request to the 80386 microprocessor, which issues a hold acknowledge (HLDA) after finishing its current operation. By sending out HLDA1 to the IPC, the data buffer and the address buffer, the bus controller signals to the data and the address buffers that the IPC controls the buffers.

3. Controller Channels

   The DMA controllers (DMA1 and DMA2) generate memory addresses and control signals for transferring data from an I/O device to memory, or from memory to an I/O device, with little intervention from the 80386.

   DMA1 (I/O address 0000h to 000Fh) provides four DMA channels, 0 to 3, and supports 8-bit data transfers between 8-bit I/O devices and 8-bit or 16-bit memory. During 8-bit to 16-bit transfers, the bus controller and the data buffers provides the required multiplexing. Throughout the system's 16-Mbyte addresses, each channel can transfer data 8 bits or 16 bits at a time, in block as large as 64 Kbyte. (Flexible disc transfers take place with DMA1 channel 2.)

   DMA2 (I/O address 00C0h to 00DEh), provides three DMA channels, 5 to 7, and supports 16-bit data transfers between 16-bit I/O devices and 16-bit memory. (DMA2's Channel 4 cascades DMA1 to DMA2, and is unavailable.) Throughout the system's 16-Mbyte addresses, these 16-bit DMA channels can transfer data 16 bits at a time, in blocks as large as 128 Kbytes, where 128 Kbytes equal one "page". All DMA memory transfers through channels 5 through 7 must occur on even-byte boundaries.

4. Address Generation

   Addresses from DMA channels are not incremented or decremented across page boundaries. The DMA page register (0081h to 008Fh) supplements direct-memory access, driving upper address lines when required, while the lower address bits are provided by the IPC, which accesses system RAM via the bus controller.

4.2.2 Interrupt Controller

System (Maskable) Interrupts

Interrupts to the system's 80386 microprocessor are provided by the 82C206 IPC's interrupt controller (equivalent to two 8259s) consists of two cascaded 8-input interrupt controllers, INTC1 (I/O address 0020h to 0021h) and INTC2 (I/O address 00A0h to 00A1h), see Table 4-1.

The interrupt controllers provide 16 interrupt channels, 3 of which are used internally by the IPC, and 13 of which are used for interrupt requests. (Refer to this chapter "I/O Address Map for IPC Components" for a breakdown of the interrupt controller register assignments.)

Interrupt Controller Operation

The IPC's interrupt controller acts as a system-wide interrupt manager. It accepts requests from I/O devices, resolves priority on pending interrupts, issues interrupt requests to the 80386, and provides an interrupt vector which the 80386 uses as an index to determine which interrupt routine (ISR) to execute.

For proper operation of the 16 interrupt channels, the interrupt controllers must be programmed for the cascade mode. When cascaded, INTC1 is the master interrupt controller, and INTC2 is the slave. The interrupt request output signal, INT, is internally run from INTC2 to INTC1's interrupt request input (IRQ2). For additional information on system interrupts, refer to the *HP Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

Non-Maskable Interrupts

Besides the system interrupts provided by the IPC's 8259 interrupt controllers, the 80386 microprocessor has a non-maskable interrupt (NMI) input bit that can be set and reset with system programs.

The non-maskable interrupt processes the system response to either memory parity errors (refer to "Main Memory Operations" in the "Processor/Memory PCA" chapter) or errors signaled by an accessory card through the backplane I/O signal, I/OCHCK*. Hewlett-Packard has added a feature to allow NMI to be generated by an HP-HIL interrupt.

The NMI generated by the parity error or backplane I/O are ORed with the interrupt from the 1RD2 HP-HIL controller in the 8042 port expander, which generates the HPNMI interrupt to the 80386 microprocessor.

The NMI signal is masked from the 80386 microprocessor at system reset. It must be enabled via system software which is done by setting to a 0, bit 7 of the I/O address register 70h. (The same bit 7 can be masked by setting it to a 1.) The 80386 NMI generates interrupt vector number 02, which has an interrupt vector address of 008h to 00Bh.

The I/O address registers are listed in "I/O Address Map" in the "Processor/Memory PCA" chapter. The interrupt vectors are listed in Table 4-2.

Table 4-2 provides a complete map of all hardware and software interrupts in the HP Vectra QS PC.

Table 4-2. Interrupt Map

Intrpt.	Hex Addr	Function	Type	Routine
00	000-003	Divide by Zero	CPU (1)	STD-BIOS
01	004-007	Single Step	CPU (1)	STD-BIOS
02	008-00B	Non-maskable Interrupt	CPU	STD-BIOS
03	00C-00F	Software Breakpoint	CPU (1)	STD-BIOS
04	010-013	Arithmetic Overflow	CPU (1)	STD-BIOS
05	014-017	Print Screen	SW (2)	STD-BIOS
06	018-01B	Invalid Opcode (option code)	CPU (1)	STD-BIOS
07	01C-01F	Reserved	CPU (1)	STD-BIOS
08	020-023	IRQ0 (Timer Interrupt)	HW	STD-BIOS
09	024-027	IRQ1 (Keyboard ISR)	HW	STD-BIOS
0A	028-02B	IRQ2 (from Interpt Contr 2)	HW	STD-BIOS
0B	02C-02F	IRQ3 (Serial Port 2 ISR)	HW (1)	STD-BIOS
0C	030-033	IRQ4 (Serial Port 1 ISR)	HW (1)	STD-BIOS
0D	034-037	IRQ5 (Parallel Port 2 ISR)	HW (1)	STD-BIOS
0E	038-03B	IRQ6 (Flex Disc Contr ISR)	HW	STD-BIOS
0F	03C-03F	IRQ7 (Parallel Port 1 ISR)	HW (1)	STD-BIOS
10	040-043	Video I/O	SW (2)	STD-BIOS
11	044-047	Equipment Config check	SW (2)	STD-BIOS
12	048-04B	Base Memory Size	SW (2)	STD-BIOS
13	04C-04F	Flex/Hard Disc Contr I/O	SW (2)	STD-BIOS
14	050-053	Serial Port Drive	SW (2)	STD-BIOS
15	054-057	System Functions	SW (2)	STD-BIOS
16	058-05B	Keyboard I/O	SW (2)	STD-BIOS
17	05C-05F	Parallel Port Drive	SW (2)	STD-BIOS
18	060-063	Reserved	SW (3)	N/A
19	064-067	Boot	SW (2)	STD-BIOS
1A	068-06B	Time and Date	SW (2)	STD-BIOS
1B	06C-06F	Keyboard Break	SW (3)	STD-BIOS
1C	070-073	Timer Tick	SW (3)	STD-BIOS
1D	074-077	Video Parameter Table	PT	STD-BIOS
1E	078-07B	Flex Disc Parameter Table	PT	STD-BIOS
1F	07C-07F	Video Graphics Char Table	PT	STD-BIOS

Table 4-2. Interrupt Map (continued)

Intrpt.	Hex Addr	Function	Type	Routine
20	080-083	DOS Program Terminate	SW	DOS
21	084-087	DOS Function Calls	SW	DOS
22	088-08B	DOS Terminate Address	PT	DOS
23	08C-08F	DOS Ctrl Break Address	SW	DOS
24	090-093	DOS Critical Error	SW	DOS
25	094-097	DOS Absolute Disc Read	SW	DOS
26	098-09B	DOS Absolute Disc Write	SW	DOS
27	09C-09F	DOS Terminate, Stay Resident	SW	DOS
28-32	0A0-0CB	Reserved for DOS	SW	DOS
33	0CC-0CF	HP-HIL Mouse	SW (2)	EX-BIOS
34-3F	0D0-0FF	Reserved for DOS	SW	DOS
40	100-103	Alternate Flex Disc Contr	SW	STD-BIOS
41	104-107	Hard Disc Parameter Table (0)	PT	STD-BIOS
42-45	108-117	Reserved	SW	STD-BIOS
46	118-11B	Hard Disc Parameter Table (1)	PT	STD-BIOS
47-5F	11C-17F	Reserved	SW	STD-BIOS
60-6E	180-1BB	Reserved for User Programs	SW	N/A
6F	1BC-1BF	Default EX-BIOS Entry Point	SW (2)	EX-BIOS
70	1C0-1C3	IRQ8 (Real-time Clock ISR)	HW	STD-BIOS
71	1C4-1C7	IRQ9 (SW Redirected)	HW	STD-BIOS
72	1C8-1CB	IRQ10 (Serial Port 3 ISR)	HW (1)	STD-BIOS
73	1CC-1CF	IRQ11 (Serial Port 4 ISR)	HW (1)	STD-BIOS
74	1D0-1D3	IRQ12 (Reserved)	HW (1)	STD-BIOS
75	1D4-1D7	IRQ13 (Coprocessor)	HW	STD-BIOS
76	1D8-1DB	IRQ14 (Hard Disc Contr ISR)	HW (1)	STD-BIOS
77	1DC-1DF	IRQ15 (Reserved)	HW (1)	STD-BIOS
78-7F	1E0-1FF	Not Used	SW	N/A
80-F0	200-3C3	Reserved	SW	N/A
F1-FF	3C4-3FF	Not Used	SW	N/A

See this chapter's "Read-Only Memory" section for a discussion of STD-BIOS and EX-BIOS.
CPU = Interrupt of 80386 microprocessor
HW = Hardware Interrupt
ISR = Interrupt Service Routine
N/A = Not Applicable
PT = Interrupt vector used as pointer to data
SW = Software Interrupt
(1) = Unused interrupt
(2) = Application-callable entry point
(3) = Interrupt returned

4.2.3 Real-Time Clock(RTC)/CMOS RAM

The 82C206 IPC provides the system with real-time clock (RTC) and CMOS RAM functions equivalent to the MC146818. It consists of 128 bytes of memory, which include 10 time-of-day clock bytes for real-time clocking, calendar, and alarm functions, 4 bytes for control and status lines, and 114 bytes of CMOS RAM. (See Table 4-3 for the real-time clock/CMOS RAM memory map.)

The 10 bytes for the RTC time-of-day clock provide the time of day, and count seconds, minutes, hours, days, and years. They also provide calendar functions, keeping track of the day of the week and providing automatic leap year compensation. In addition, these bytes provide for programmable interrupt requests (IRQ8) at either a fixed interval (for example, every second), or when a certain time has arrived (in the alarm clock mode).

The 4 bytes for control and status lines control the RTC/CMOS RAM operation and monitor its status.

The 114 bytes of CMOS RAM provide non-volatile memory to store HP Vectra QS PC system configuration and calibration parameters when power is removed from the system. All the 114 CMOS RAM bytes are either currently used or reserved, with no user-definable bytes. However, applications may read these bytes to determine system configuration, or write to them, providing the byte definitions are adhered to. The CMOS RAM bytes are not affected by the RTC and are accessible during the update cycle.

Real-Time Clock/CMOS RAM Operation

When the system power is on, the RTC/CMOS RAM operates from a 32.768 KHz crystal oscillator (pin OSCI). During power-on reset, the system software reads the current time and date from the RTC and converts it into the appropriate number of system clock "ticks." From this point on, system time is kept via system clock ticks generated by counter/timer 0.

The RTC/CMOS RAM's 128 locations are accessed by the 80386 microprocessor placing the proper address (or "index") ranging from 00h to 7Fh on data lines XD0 through XD6 and then writing these seven bits to I/O address 0070h. (Bit 7 is the non-maskable interrupt bit.) When a strobe is applied to the IPC's Address Strobe input pin, on the falling edge of the Address Strobe, the address on the data input lines is latched into the Real-Time Clock's internal Index Address Register. At this point, the 80386 microprocessor can access the desired location by reading from or writing to I/O address 0071h.

(Note that the I/O address registers are listed in "I/O Address Map" in the "Processor/Memory PCA" chapter.)

When the system power is off, the RTC/CMOS RAM's 32.788 oscillator gets power from the system's battery, keeping track of the time and day and maintaining RAM. The battery, located on the power unit, is a 6-Volt lithium battery pack with an average life between 2 and 5 years.

Table 4-3. Real-Time Clock/CMOS RAM Memory Map

Hex Address	Byte Type	Application
00	Real-Time Clock (RTC) Register *	Seconds
01	RTC Register *	Seconds alarm
02	RTC Register *	Minutes
03	RTC Register *	Minutes alarm
04	RTC Register *	Hours
05	RTC Register *	Hours alarm
06	RTC Register *	Day of Week
07	RTC Register *	Date of Month
08	RTC Register *	Month
09	RTC Register *	Year
0A	RTC Register *	Status Register A
0B	RTC Register *	Status Register B
0C	RTC Register *	Status Register C
0D	RTC Register *	Status Register D
0E	CMOS RAM Byte *	Diagnostic status byte
0F	CMOS RAM Byte *	Shutdown status byte
10	CMOS RAM Byte	Flexible disc drive type (A and B)
11	CMOS RAM Byte	Reserved
12	CMOS RAM Byte	Hard disc drive type (C and D)
13	CMOS RAM Byte	Reserved
14	CMOS RAM Byte	Equipment byte
15	CMOS RAM Byte	Low base memory byte
16	CMOS RAM Byte	High base memory byte
17	CMOS RAM Byte	Low expansion memory byte
18	CMOS RAM Byte	High expansion memory byte
19-20	CMOS RAM Bytes	Reserved
21-2D	CMOS RAM Bytes	Reserved
2E-2F	CMOS RAM Byte	2-byte CMOS checksum
30	CMOS RAM Byte *	Low expansion memory byte
31	CMOS RAM Byte *	High expansion memory byte
32	CMOS RAM Byte *	Date century byte
33	CMOS RAM Byte *	Information flags
34-3F	CMOS RAM Bytes *	Reserved
40-7F	CMOS RAM Bytes *	HP-Reserved

* Indicate bytes which are not included in the CMOS checksum calculation.

4.2.4 Counter/Timers

Counter/timers are provided to the system by the 82C206 IPC's three 16-bit counters, equivalent to 8254 counter/timers.

Counter/Timer Operation

The counter/timers each operate independently, but are driven by a common clock, TMRCLK (1.19 MHz, derived from the 14.318 MHz system timing clock, OSC4, divided by 12). The minimum time resolvable is approximately 838 nanoseconds (1 input clock cycle), and the maximum time resolvable is 55 milliseconds (65,536 clock cycles).

All counter/timers have the same control logic, which decodes information written to them. The control logic also provides the controls to load, read, and configure the counter/timers, all of which are dedicated to system functions.

Timer 0 (I/O address 0040h) generates the MS-DOS real-time clock interrupt.

Counter 1 (0041h) is dedicated to RAM refresh, and no attempt should be made to reprogram it.

Counter 2 (0042h) drives the speaker. Under program control, this counter has a gate input, bit 0 of the industry-standard Port B (0061h). Setting this bit to 0 inhibits counting action, turning the speaker off. (Because bit 1 is ANDed with this counter's output, writing a 0 to this bit also disables the speaker.)

A control/status register (0043h) holds the mode and command information and monitors counter conditions.

4.3 KEYBOARD AND HP-HIL CIRCUITS

The keyboard and HP-HIL (Hewlett-Packard Human Interface Link) circuits consist of the components listed below. Together, the 8042 keyboard controller, the 8042 keyboard controller port expander (an HP-proprietary gate array), and the IRD2 HP-Human Interface Link controller (also known as "the Master Link Controller" or MLC) control the interface to the keyboard and other I/O devices.

Figure 4-3 gives a block diagram of the keyboard and HP-HIL circuits. If an industry-standard keyboard is used, data from it is latched into the keyboard controller, which instructs the 80386 microprocessor to read the data. On the other hand, if HP-HIL input devices are used, data are latched into the HP-HIL controller, after which 8042 keyboard controller port expander instructs the 80386 to read the data.

The major keyboard and HP-HIL components are:

8042 keyboard controller port expander gate array
8042 keyboard controller, for industry-standard keyboards
Industry-standard keyboard
1RD2 HP-HIL master link controller for HP-HIL input devices
HP-HIL interface link connector for HP-HIL input devices

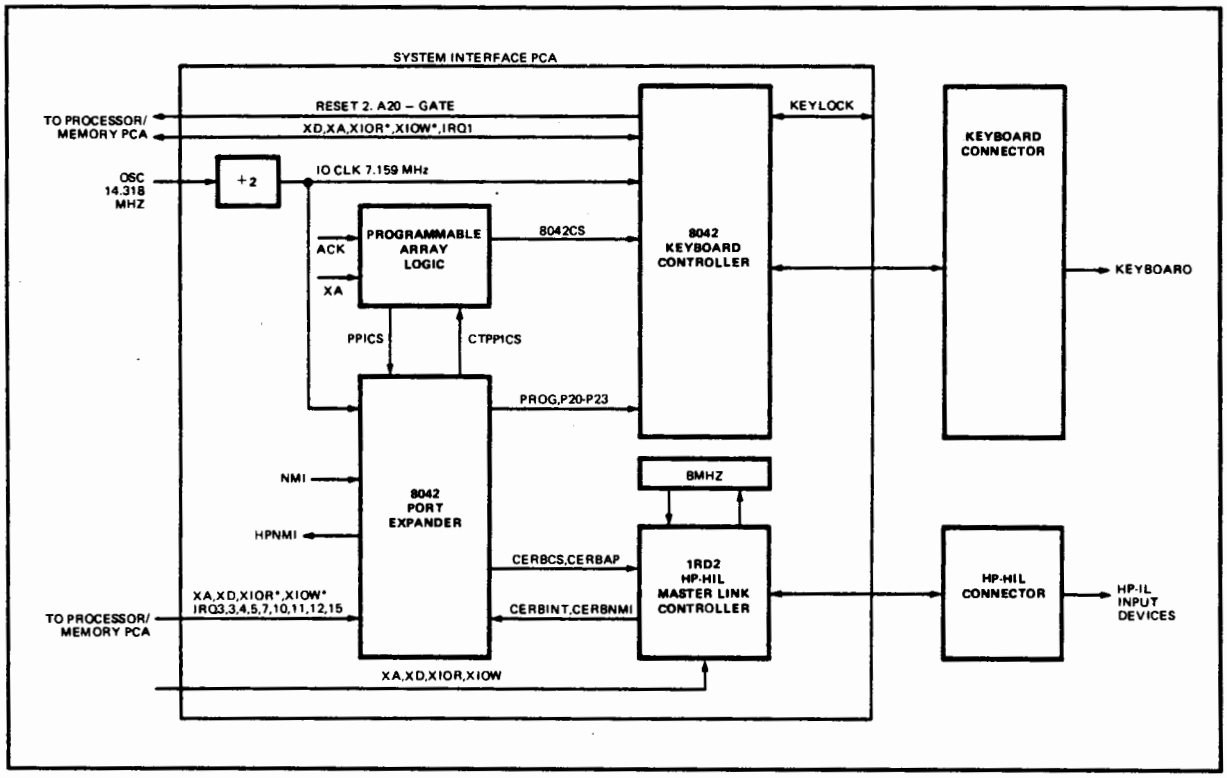

Figure 4-3. Block Diagram of Keyboard and HP-HIL Circuits

4.3.1 Keyboard

Figures 4-4 to 4-6 show the HP Vectra QS PC keyboard and identify the reference numbers.

Depending on which of the keyboard keys are pressed, data from the keyboard to the system is sent via a series of hex scan codes that correspond to the values shown in Tables 4-5 to 4-8. Commands sent from the system to the keyboard are listed and defined in Table 4-9.

Note that Tables 4-4 to 4-8 show the codes sent from the keyboard to the 8042 keyboard controller. The 8042 then generates one of three sets of scan code. The available scan code sets are described in the *Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*

For more information on the keyboard operation and on data and commands sent by the keyboard to the system, refer to the "Keyboard" chapter of the *HP Vectra Accessories Technical Reference Manual.*

The Vectra QS PC supports industry-standard keyboards. It does NOT support the "Vectra PC keyboard" used by earlier versions of the HP Vectra PC.

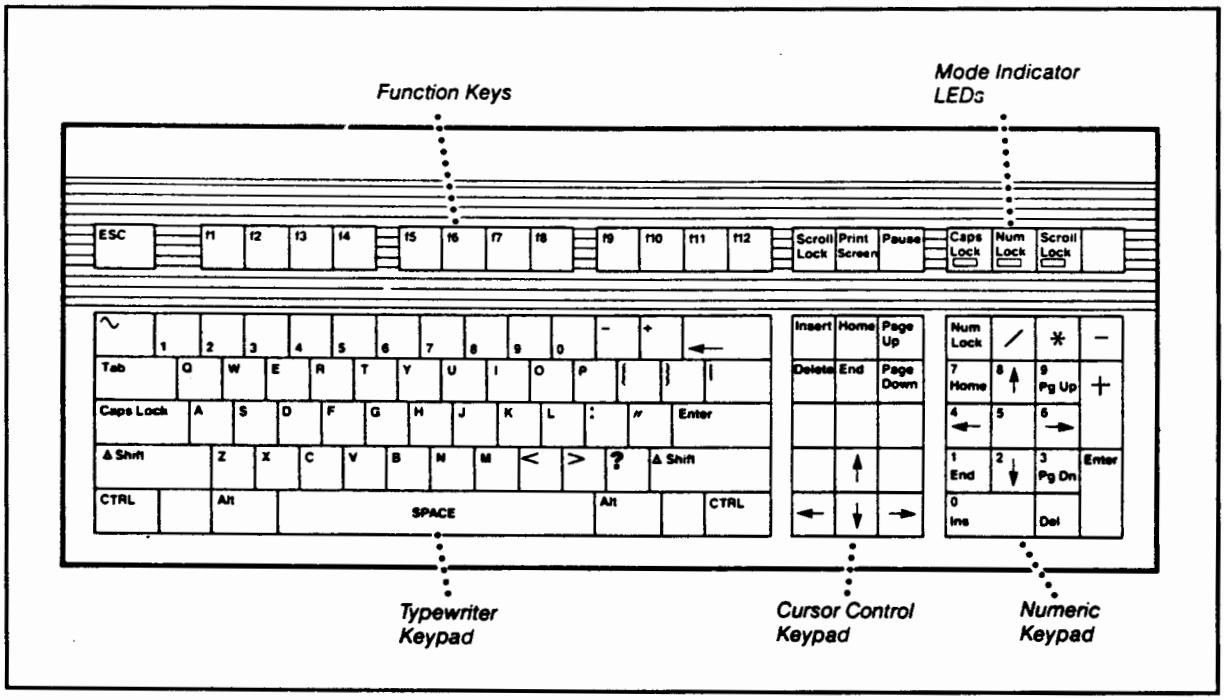

Figure 4-4. HP Vectra QS PC Keyboard (USASCII)

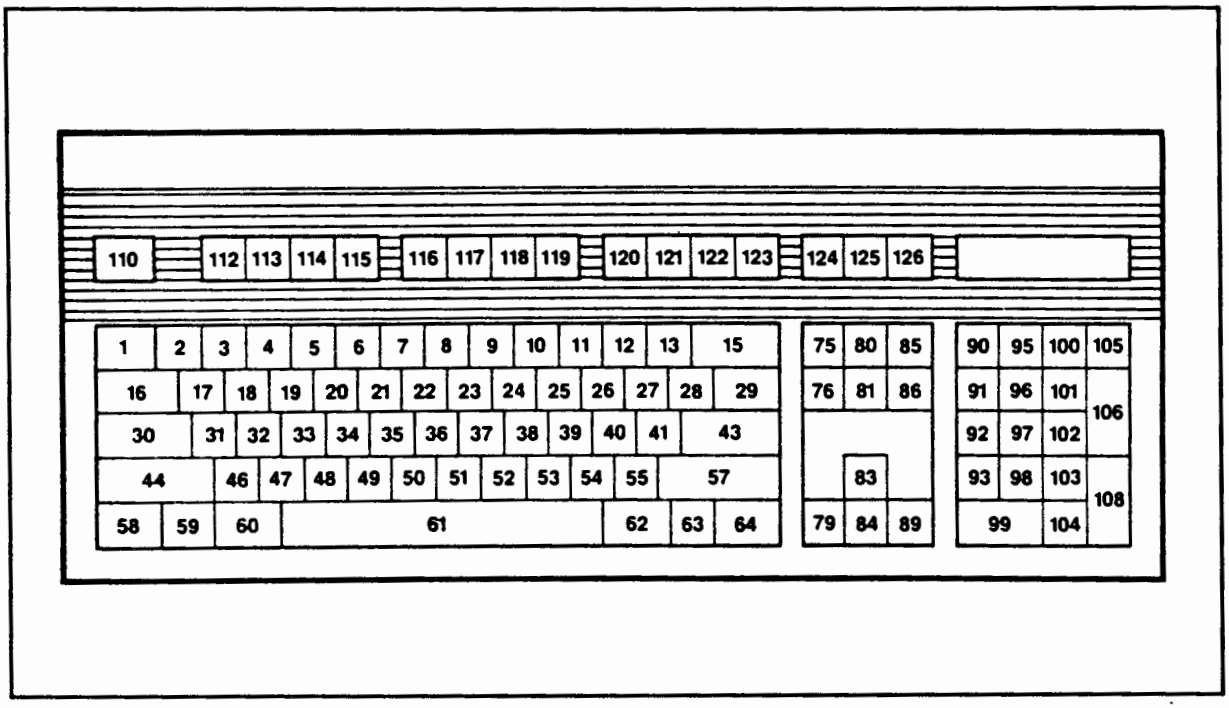

Figure 4-5. Keyboard Reference Numbers (USASCII)

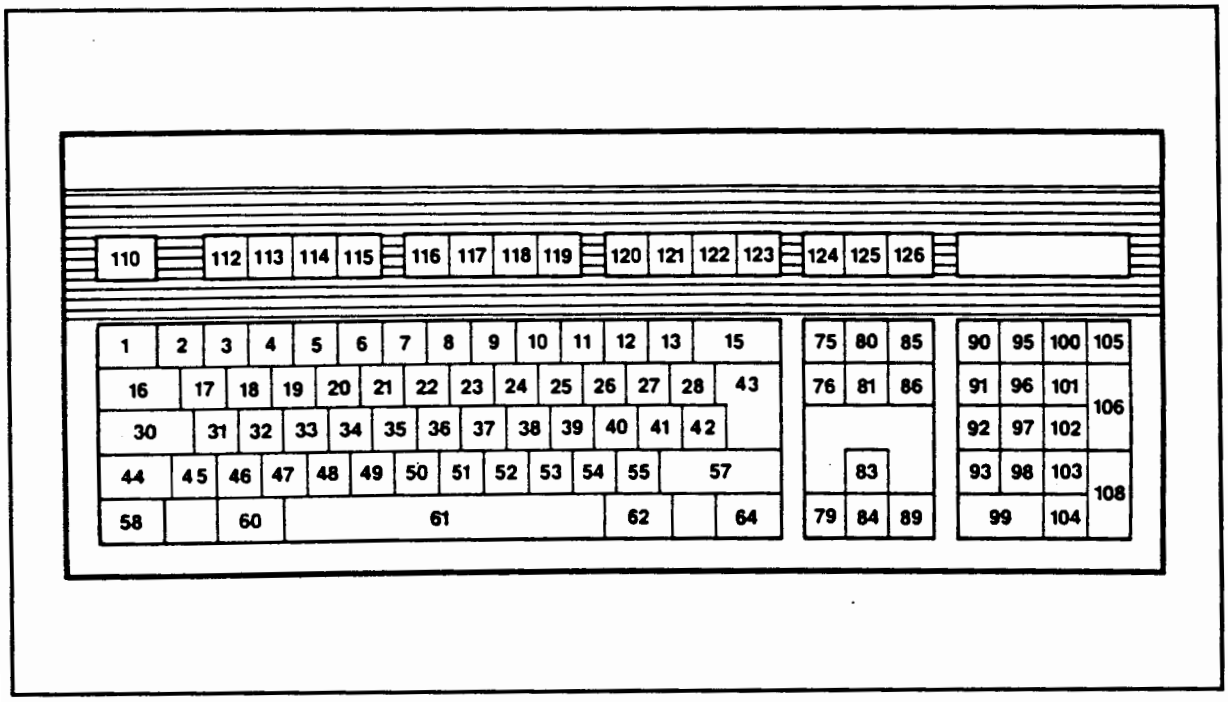

Figure 4-6. Keyboard Reference Numbers (National Keyboard)

Table 4-4. Keyboard Hex Scan Codes

Key #	Make Code	Break Code	Key #	Make Cde	Break Cde
1	0E	F0 0E	41	52	F0 52
2	16	F0 16	42 **	5D	F0 5D
3	1E	F0 1E	43	5A	F0 5A
4	26	F0 26	44	12	F0 12
5	25	F0 25	45 **	61	F0 61
6	2E	F0 2E	46	1A	F0 1A
7	36	F0 36	47	22	F0 22
8	3D	F0 3D	48	21	F0 21
9	3E	F0 3E	49	2A	F0 2A
10	46	F0 46	50	32	F0 32
11	45	F0 45	51	31	F0 31
12	4E	F0 4E	52	3A	F0 3A
13	55	F0 55	53	41	F0 41
14 #	—	——	54	49	F0 49
15	66	F0 66	55	4A	F0 4A
16	0D	F0 0D	56 #	—	——
17	15	F0 15	57	59	F0 59
18	1D	F0 1D	58	14	F0 14
19	24	F0 24	59 ***	5E	F0 5E
20	2D	F0 2D	60	11	F0 11
21	2C	F0 2C	61	29	F0 29
22	35	F0 35	62	E0 11	F0 11
23	3C	F0 3C	63 ***	5F	F0 5E
24	43	F0 43	64	E0 14	E0 F0 14
25	44	F0 44	65 #	——	——
26	4D	F0 4D	66 #	——	——
27	54	F0 54	67-74 #	——	——
28	5B	F0 5B	75	Note (1)	Note (1)
29 *	5D	F0 5D	76-89 #	Note (1)	Note (1)
30	58	F0 58	90	77	F0 77

Table 4-4. Keyboard Hex Scan Codes (continued)

Key #	Make Code	Break Code	Key #	Make Cde	Break Cde
31	1C	F0 1C	91	6C	F0 6C
32	1B	F0 1B	92	6B	F0 6B
33	23	F0 23	93	69	F0 69
34	2B	F0 2B	94 #	—	——
35	34	F0 34	95	Note (2)	Note (2)
36	33	F0 33	96	75	F0 75
37	3B	F0 3B	97	73	F0 73
38	42	F0 42	98	72	F0 72
39	4B	F0 4B	99	70	F0 70
40	4C	F0 4C	100	7C	F0 7C
101	7D	F0 7D	114	04	F0 04
102	74	F0 74	115	0C	F0 0C
103	7A	F0 7A	116	03	F0 03
104	71	F0 71	117	0B	F0 0B
105	7B	F0 7B	118	83	F0 83
106	79	F0 79	119	0A	F0 0A
107 #	—	——	120	01	F0 01
108	E0 5A	E0 F0 5A	121	09	F0 09
109 #	—	——	122	78	F0 78
110	76	F0 76	123	07	F0 07
111 #	—	——	124	Note (3)	Note (3)
112	05	F0 05	125	7E	F0 7E
113	06	F0 06	126	Note (4)	Note (4)

* 101-key keyboard only (U.S.).
** 102-key keyboard only (national).
*** Asian keyboard only.
# Not a referenced key number.
(1) See Table 4-5.
(2) See Table 4-6.
(3) See Table 4-7.
(4) See Table 4-8.

Table 4-5. Keyboard Scan Codes

Key No./Code	Base case *	Shift Case*	Num Lock On
75/Make Code	E0 70	E0 F0 12 E0 70	E0 12 E0 70
/Break Code	E0 F0 70	E0 F0 70 E0 12	E0 F0 70 E0 F0 12
76/Make Code	E0 71	E0 F0 12 E0 71	E0 12 E0 71
/Break Code	E0 F0 71	E0 F0 71 E0 12	E0 F0 71 E0 F0 12
77, 78 #			
79/Make Code	E0 6B	E0 F0 12 E0 6B	E0 12 E0 6B
/Break Code	E0 F0 6B	E0 F0 6B E0 12	E0 F0 6B E0 F0 12
80/Make Code	E0 6C	E0 F0 12 E0 6C	E0 12 E0 6C
/Break Code	E0 F0 6C	E0 F0 6C E0 12	E0 F0 6C E0 F0 12
81/Make Code	E0 69	E0 F0 12 E0 69	E0 12 E0 69
/Break Code	E0 F0 69	E0 F0 69 E0 12	E0 F0 69 E0 F0 12
82 #			
83/Make Code	E0 75	E0 F0 12 E0 75	E0 12 E0 75
/Break Code	E0 F0 75	E0 F0 75 E0 12	E0 F0 75 E0 F0 12
84/Make Code	E0 72	E0 F0 12 E0 72	E0 12 E0 72
/Break Code	E0 F0 72	E0 F0 72 E0 12	E0 F0 72 E0 F0 12
85/Make Code	E0 7D	E0 F0 12 E0 7D	E0 12 E0 7D
/Break Code	E0 F0 7D	E0 F0 7D E0 12	E0 F0 7D E0 F0 12
86/Make Code	E0 7A	E0 F0 12 E0 7A	E0 12 E0 7A
/Break Code	E0 F0 7A	E0 F0 7A E0 12	E0 F0 7A E0 F0 12
87, 88 #			
89/Make Code	E0 74	E0 F0 12 E0 74	E0 12 E0 74
/Break Code	E0 F0 74	E0 F0 74 E0 12	E0 F0 74 E0 F0 12

Not a referenced key number.
* Also applies when (Shift) and (Num lock) are held down.
** The F0 12/12 shift make and break codes are sent with the other scan codes if the left (Shift) key is held down. If the right (Shift) key is held down, then the F0 59/59 shift make and break codes are sent. Both sets of make and break codes are sent with the other scan codes if both (Shift) keys are held down.

Computer Museum

Table 4-6. Keyboard Scan Codes

Key No./Code	Scan Code	Shift Case*
95/Make Code	E0 4A	E0 F0 12 4A
/Break Code	E0 F0 4A	E0 12 F0 4A

* The F0 12/12 shift make and break code is sent with the other scan codes if the left (Shift) key is held down. If the right (Shift) key is held down, then the F0 59/59 shift make and break codes are sent. Both sets of make and break codes are sent with the other scan codes if both (Shift) keys are held down.

Table 4-7. Keyboard Scan Codes

Key No./Code	Scan Code	Ctrl, Shift Case	Alt Case
124/Make Code	E0 12 E0 7C	E0 7C	84
/Break Code	E0 F0 7C E0 F0 12	E0 F0 7C	F0 84

Table 4-8. Keyboard Scan Codes

Key No./Code	Make Code	Control Key Pressed
126 **	E1 14 77 E1 F0 14 F0 77	E0 7E E0 F0 7E

* Not a typematic key. All associated scan codes occur on the key's make code.

Table 4-9. Commands Sent Between the System and the Keyboard

Command	Definition
EDh - Set/Reset Mode Indicators	This command, in conjunction with an option byte that immediately follows it, toggles the keyboard's three mode-indicator LEDs, turning them on and off. Bits 7 through 3 of this option byte are not used, and should be set to 0. Bit 2 controls the (Caps lock) mode indicator, bit 1 controls the (Num lock) mode indicator, and bit 0 controls the (Scroll lock) mode indicator. Setting the respective bits to 1 turns a mode indicator on, while a 0 turns it off.
EEh - Echo	This command is a diagnostic aid. When the system issues this command to the keyboard, the keyboard responds by sending to the system its own Echo command (EEh).
EFh - No operation	This command is reserved. The system sends this command to the keyboard, which acknowledges receiving the command, but takes no action.

Table 4-9.
Commands Sent Between the System and the Keyboard (continued)

Command	Definition
F0h - Select Alternative Scan Codes	This command, in conjunction with an option byte that immediately follows it, instructs the keyboard to select one of three sets of scan codes. When the keyboard receives this command, it clears its output buffer and the typematic key (if one is active). The system then sends an option byte to select the appropriate scan code set: 01h selects set 1, 02h selects set 2, and 03h selects **set 3**.
F1h - No Operation	This command is reserved. The system sends this command to the keyboard, which acknowledges receiving the command, but takes no action.
F2h - Request Keyboard Identification Information	This command instructs the keyboard to discontinue sending scan codes and to send two keyboard identification bytes. After the first identification byte, the second byte must follow by 500 microseconds or less, after which the keyboard resumes sending scan codes.
F3h - Set Typematic Delay/Rate	This command, in conjunction with a parameter byte that immediately follows it, alters the keyboard's typematic delay and rate. Bit 7 of this parameter byte is always zero. Bits 6 and 5 alter the delay parameters, and bits 4, 3, 2, 1 and 0 alter the rate parameters.
F4h - Enable	This command enables the keyboard to send scan codes if the transmission of scan codes had been halted.
F5h - Default Disable	This command resets all keyboard parameters to the power-on default state and stops the keyboard from sending scan codes.
F6h - Set Default	This command resets all keyboard parameters to the power-on default state, after which the keyboard sends scan codes.
F7h - Set All Keys Typematic	This command clears the keyboard's output buffers. The keyboard then sets all keys to typematic, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.
F8h - Set All Keys Make/Break	This command clears the keyboard's output buffers. The keyboard sets all keys to make/break, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.
F9h - Set All Keys Make	This command clears the keyboard's output buffers. The keyboard sets all keys to make, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.
FAh - Set All Keys Type-matic/Make/Break	This command clears the keyboard's output buffers. The keyboard sets all keys to typematic/make/break, and continues to send scan codes. This command can be sent using any scan code set, but only set 3 is affected.

Table 4-9.
Commands Sent Between the System and the Keyboard (continued)

Command	Definition
FBh - Set Key Typematic	This command clears the keyboard's output buffers so the keyboard may receive the key identification. The system identifies each key by its scan code set 3 value. Each identified key is set to typematic.
FCh - Set Key Make/Break	This command clears the keyboard's output buffers so the keyboard may receive the key identification. The system identifies each key by its scan code set 3 value. Each identified key is set to make/break.
FDh - Set Key Make	This command clears the keyboard's output buffers so the keyboard may receive the key identification. The system identifies each key by its scan code set 3 value. Each identified key is set to make.
FEh - Resend	This command, sent by the system's 8042 keyboard controller when it detects an error in data coming from the keyboard, tells the keyboard to resend the last data.
FFh - Reset	This command performs the keyboard's Power-On Reset function. This step takes at least 300 milliseconds, during which time the keyboard is disabled.
00h - Overrun	This character code is placed in position 17 of the keyboard buffer, overlaying the last of the code when the keyboard buffer is full.
AAh - Completion Code	This code is sent after the keyboard has passed its self-test. Any other code tells the system that the keyboard has failed its self-test.
EEh - Echo	This command is a diagnostic aid. After the system has issued its Echo command to the keyboard, the keyboard responds by sending to the system its own Echo command (EEh) and scan codes, if the keyboard has been previously enabled.
F0h - Break Code Prefix	This code is sent when a key is released. The code consists of a two-byte hex prefix, F0, followed by the make code for the released key.
FAh - Acknowledge	This command is sent to the system by the keyboard to acknowledge it has received valid input from the system. The keyboard does not send this command when it receives from the system either an Echo command (EEh) or a Resend command (FEh). If, while the keyboard is sending the acknowledge command, the system interrupts the keyboard with a command, the keyboard discards the acknowledge command. If the new command is recognized, the keyboard accepts the system's new command and processes it. If the command is not recognized, the keyboard sends a Resend command (FEh) to the system.
FCh - Diagnostic Failure	This command is sent if the keyboard detects a malfunction. If the malfunction occurs during the keyboard self-test, the keyboard will stop and wait for a system command or a power-down.
FEh - Resend	This command is sent when the keyboard receives from the system either invalid input, or input with incorrect parity.

4.3.2 Keyboard Controller

The keyboard controller, a 8042 microprocessor, is programmed to provide a serial interface between the 80386 microprocessor and an industry-standard keyboard, HP-HIL devices, and the computer's speaker. More specifically, the keyboard controller provides the following:

- interfaces to the 80386 microprocessor, including logical paths to 80386 microprocessor and system reboot
- a communication path between HP-HIL input devices and the computer's BIOS and/or the computer's application programs
- three output lines and one input line for hardware system purposes

Keyboard Controller Operation

1. Interface to 80386 Microprocessor

   a. Logical paths from Keyboard Controller to CPU

      The application path, a direct logic path from the 8042 keyboard controller to the 80386 microprocessor, consists of two 80386 read/write registers and an interrupt line. The first 80386 read/write register, at I/O address 60h, is used for keyboard commands and data, and for keyboard controller data. The second 80386 read/write register, at I/O address 64h, is used to write commands to, and read the status of, the keyboard controller. The output buffer interrupt line (OBFINT) is set to interrupt the 80386 when the keyboard controller places data in the 80386's read register at I/O address 60h.

      (Note that the I/O address registers are listed in "I/O Address Map" in the "Processor/Memory PCA" chapter.)

   b. System Reboot

      By writing FEh to I/O port 64, RESET2* goes low, activating the bus controller's RESET3 (on the Processor/Memory PCA), which resets the 80386 microprocessor and coprocessor, if the coprocessor is installed.

      Through its A20_GATE signal, the keyboard controller can also be used to extend the 80386 microprocessor's real-address mode, which is limited to 1 Mbyte. When high, A20_GATE enables 80386 address line A20, extending the 80386's real-address mode. When low, A20_GATE forces the 80386 address line A20 to a logical 0.

   c. Industry-Standard Keyboard Interface (clock and data signals)

      Via the signals KBDCLKOUT (keyboard clock out) and KBDATOUT (keyboard data out), the 8042 keyboard controller sends clock reference signals and data (commands or status) to the industry-standard keyboard. In return, the keyboard sends the keyboard controller a clock reference signal, KBDCLKIN (keyboard clock in) and KBDATIN (keyboard data in).

Each time the user presses or releases a key, the keyboard sends a corresponding 11-bit scan code to the 8042 keyboard controller (in the format shown in Table 4-10). By writing the scan code to its output buffer, the keyboard controller sends the scan code to the 80386 microprocessor, which causes an interrupt of the 80386 (IRQ1). The 80386 then reads the scan code from I/O address 60h.

Table 4-10. Keyboard Scan Codes Data Transmission Format

Bit	Definition
1	Start bit (always 1
2	Data bit 0 (least-significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most-significant bit)
10	Parity bit * (0 or 1)
11	Stop bit (always 1)

* The eight data bits, plus the parity always equal an odd number.

2. HP-HIL Input Device Interface

   When an HP-HIL input device sends an input to the IRD2 HP-HIL MLC, the controller sends an interrupt (CERBINT*) to 8042 port expander. The 8042 keyboard controller reads this and in turn, generates an interrupt (HPINT) to the 80386 microprocessor. (HPINT uses IRQ12 by default. This can be changed under software control.) When the 80386 checks the source of the interrupt by reading I/O address 65h, and if bits 5 and 4 are zero, then the 80386 reads data from the IRD2 HP-HIL MLC. (For more information on the HP-HIL interface, refer to the section "HP-HIL" in this chapter.)

3. Speaker Interface

   Each time the keyboard controller receives a keyboard character from either the industry-standard keyboard or an HP-HIL input device, the keyboard controller sends a keyboard click signal (KBCLICK) to the computer's speaker.

   The volume of the keyboard click is increased by pressing CTRL Alt +. The volume of the keyboard click is decreased by pressing CTRL Alt -.

4. Keyboard Inhibit Switch Interface

   The keyboard controller monitors the keyboard inhibit (KBINH) input line, which comes from the optional keyboard inhibit switch. When the user turns this front-panel switch to the lock position, the KBINH signal is set to 0. In this case, keyboard data is still returned to the keyboard controller, but not read by the 80386 microprocessor.

4.3.3 8042 Keyboard Controller Port Expander

The 8042 keyboard controller port expander, a Hewlett-Packard proprietary CMOS standard cell chip packaged in a 44-pin plastic-leaded chip carrier, can select one of eight general-purpose I/O interrupts.

8042 keyboard controller port expander also provides HP-specific keyboard controller functions, as well as extensions for the keyboard controller's ports. In addition, in conjunction 8042 keyboard controller, the port expander provides the auto-polling frequency and address decoding for the IRD2 HP-HIL MLC. Pin assignments for the 8042 port expander are described in Table 4-11.

Table 4-11. 8042 Keyboard Controller Port Expander Pin Assignments

Pin No.	I/O/Power	Pin Name	Pin Definition
1	Ground	GND	Ground
2	Out	CERBAP	Auto-poll frequency for the HP-HIL MLC
3	In	PROG	Program code (keyboard controller address/data strobe)
4-7	I/O Tri-State	P23-P20	Register address and data pins for the keyboard controller
8-11	Out Tri-State	IRQ A,C,E,G	Interrupt request pins for channels 3, 5, 10, 12
12	In with pull-up	CERBINT*	Interrupt pin for 1RD2 HP-HIL MLC
13	In with pull-up	CERBNMI*	Non-maskable interrupt pin 1RD2 HP-HIL MLC
14-18	In	XA0 to XA4	Peripheral address bus bits 0 to 4
19-22	I/O Tri-State	XD0 to XD3	Peripheral data bus bits 0 to 3
23	Ground	GND	Ground
24-27	I/O	XD7 to XD4	Peripheral data bus bits 7 to 4
28-29	Out	Reserved	Reserved
30	In	PPICS*	Programmable Peripheral Interface Chip Select
31	Out	CTPPICS*	Custom Task Programmable Peripheral Interface Chip Select
32	In with pull-up	Reserved	Reserved
33	In	IOCLK	Clock input pin
34	In	RESET*	Reset signal
35	Power	VDD	Power pin
36-39	Out Tri-State	IRQ B,D,F,H	Interrupt request pins for channels 4, 7, 11, 15
40	In	XIOW*	I/O write
41	In	XIOR*	I/O read
42	Out	CERBCS*	1RD2 HP-HIL MLC Chip Select
43	Out	HPNMI	HP non-maskable interrupt
44	In	NMI	Non-maskable interrupt

* Indicates active low.

4.3.4 HP-HIL

The HP-HIL (Hewlett-Packard Human Interface Link) is a Hewlett-Packard proprietary four-wire asynchronous serial interface comprised of:

1. the HP-HIL controller (also known as the Hewlett-Packard 1RD2 HP-HIL MLC), an n-channel metal-oxide semiconductor integrated circuit in a 24-pin dual in-line package
2. the HP-HIL connector, a shielded 4-pin connector

The HP-HIL acts as the HP standard interface between the SPU (system processor unit) and up to seven Hewlett-Packard HIL input devices. An overview of the HP-HIL operation is given below. (For more information, consult the *HP-HIL Technical Reference Manual.*)

HP-HIL Operation

The HP-HIL enables the user to connect input devices to the SPU by "daisy-chaining" them; i.e., the first input device is plugged into the SPU, the second input device is plugged into the first input device, etc.

Note that the HP Vectra keyboard is NOT an HP-HIL device.

Refer to the figure in this chapter, "Block Diagram of Keyboard and HP-HIL Circuits" for a block diagram of how the HP-HIL circuit interfaces with the 8042 keyboard controller port expander, and the HP-HIL input devices.

Each of the HP-HIL input devices contain a Hewlett-Packard custom chip (the IRC8 Slave Link Controller, or SLC) and a microprocessor. The IRC8 handles all HP-HIL communication between the 1RD2 HP-HIL MLC and a microprocessor, which is programmed to handle the hardware for that particular input device.

Approximately 60 times per second, the 1RD2 HP-HIL MLC polls the HP-HIL input devices to collect data from them. If device data is returned, the HP-HIL controller generates an interrupt (CERBINT*) and sends it to 8042 port expander, which sends the interrupt to the 8042 keyboard controller. The keyboard controller recognizes this interrupt and in turn, makes 8042 port expander generate an interrupt to the 80386 microprocessor (HPINT). (HPINT uses IRQ12 by default. This can be changed under software control.) The keyboard controller also writes data into 8042 port expander, stating that the interrupt is from the 1RD2 HP-HIL MLC. The 80386 is interrupted, recognizes the source of the interrupt, and reads the data from the HP-HIL MLC.

The SPU power supply provides +12 Vdc for the HP-HIL input devices. Each HP-HIL device typically regulates the +12 Vdc to +5Vdc, and requires 100 mA.

1. HP-HIL Master Link Controller (IRD2)

   The 1RD2 HP-HIL Master Link Controller (MLC) interfaces the computer's 80386 microprocessor to HP-HIL input devices, via the HP-HIL connector. The 1RD2 HP-HIL MLC accepts commands from the 80386 and transmits them to the HP-HIL input devices in a fixed format called a "frame." Each frame consists of 15 bits of information, including start, stop, command, parity, address, and data bits.

Using this same format, the 1RD2 HP-HIL MLC also receives serial data from input devices and relays the data to the 80386 microprocessor. The 1RD2C HP-HIL MLC pin assignments are given in Table 4-12.

Table 4-12. HP-HIL Controller Pin Assignments

Pin No.	I/O/Power	Pin Name	Pin Definition
1	Out	NMI	Non-Maskable Interrupt
2	Out	INT	Interrupt
3	Power	VDD	+5 V power pin
4	I/O	D0	Data I/O <0>
5	I/O	D1	Data I/O <1>
6	I/O	D2	Data I/O <2>
7	I/O	D3	Data I/O <3>
8	I/O	D4	Data I/O <4>
9	I/O	D5	Data I/O <5>
10	I/O	D6	Data I/O <6>
11	I/O	D7	Data I/O <7>
12	Ground	MOT	Reserved
13	In	A1	Address <1>
14	In	A0	Address <0>
15	In	NRD	Not Read Enable
16	In	NCS	Not Chip Select
17	In	NWR	Not Write Enable
18	Out	SO	Serial data output, HP-HIL
19	In	SI	Serial data input, HP-HIL
20	Ground	GND	Ground
21	In	PON	Power On reset input (active low)
22	In	AP	Auto Poll input (rising edge)
23	Out	CLK0	Oscillator Clock Output
24	In	CLKI	Oscillator Clock Input

2. HP-HIL Connector

The HP-HIL connector pin assignments are given in Table 4-13.

Table 4-13. HP-HIL Connector Pin Assignments

Pin No.	I/O/Power	Pin Name	Pin Definition
1	Power	VDD	+12 Vdc power pin
2	Input	SI	Serial data HP-HIL input signal
3	Output	SO	Serial data HP-HIL output signal
4	Ground	GND	Ground
9,10	Shield	SHLD	Path to system for electro-static discharge

4.4 READ-ONLY MEMORY

4.4.1 BIOS ROM

BIOS, the basic input/output system, is a collection of standardized programs that control the transfer of characters between the 80386 microprocessor, memory, and such I/O devices as the disc drives, keyboard, monitor, and printer. The BIOS ROM components, which contain the firmware comprising the BIOS memory, increase the BIOS's utilization of I/O devices and optimize the I/O devices' response time.

The BIOS ROM components, located on the System Interface PCA, include two 32-Kbyte 27256 EPROMs, for 64 Kbytes of ROM. The EPROM (ROM0) is for low-byte data, and the EPROM (ROM1) is for high-byte data. The BIOS ROMs, addressable from hex 0F0000 to 0FFFFF, are also addressable from hex FF0000 to FFFFFF. On the QS/16 and QS/20, the BIOS ROMs are also addressable at FFFFF0000 to FFFFFFFF

The BIOS ROM components which make up the ROM BIOS contain both Standard BIOS (STD-BIOS) and Extended BIOS (EX-BIOS) firmware. STD-BIOS supports the industry-standard BIOS, while EX-BIOS supports a BIOS unique to Hewlett-Packard computers.

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ROM BIOS = STD-BIOS + EX-BIOS
```

BIOS ROM Operation

The HP Vectra QS PC system memory has locations for the following:

1. ROM BIOS. ROM BIOS memory locations consist of the the STD-BIOS and EX-BIOS interrupt vectors, and data areas loaded into system RAM upon power-up.
2. STD-BIOS. Memory locations for the STD-BIOS data area, the STD-BIOS data expansion area, and the STD-BIOS temporary MS-DOS buffers, all support the industry-standard set of BIOS functions.
3. EX-BIOS. Memory locations for the EX-BIOS data area support those functions unique to HP peripherals.

   (For details on the BIOS contents, refer to the *HP Vectra System BIOS Technical Reference Manual for the Vectra Series of Personal Computers.*)

Upon power-up, the 80386 microprocessor addresses the system memory at hex address 0FFFF0, the location of part of the BIOS ROM components's software, and executes a series of instructions at this address. These instructions load from the BIOS ROM components, into the system RAM: (1)the ROM BIOS interrupt vectors, (2)ROM BIOS data areas, (3)certain ROM BIOS functions.

ROM BIOS software components

ROM BIOS software components include interrupt vectors, drivers, and data areas.

1. Interrupt vectors

   An interrupt occurs when the 80386 microprocessor disrupts a routine's normal operation. As defined by the 80386's interrupt structure, each interrupt has an associated interrupt vector. The 80386's interrupt structure supports 256 interrupt vectors, which occupy the first 1024 bytes of system memory from hex address 00000 to 003FF. (For the interrupt vector assignments, refer to the table in this chapter "Interrupt Map".)

Each interrupt vector consists of two words (four bytes). Each interrupt vector contains the code segment and instruction pointer for the interrupt's service routine. Unused interrupt vectors point to a null routine in the ROM BIOS, which, when required, issues an end-of-interrupt signal to the 82C206 IPC and returns.

The following interface interrupts require interrupt vectors:

- Hardware interrupts that indicate a system hardware component or an I/O device requires service.
- Interrupts of the 80386 microprocessor that indicate (1)the system software requires recovery from an error condition and (2)other hardware exceptions.
- Software interrupts (generated by programming and mapped to the same interrupt vectors used for hardware and 80386 microprocessor), that simulate these interrupts.

2. ROM BIOS drivers

   The ROM BIOS drivers consist of STD-BIOS drivers (which support industry-standard BIOS functions) and EX-BIOS drivers (which support BIOS functions and subfunctions unique to Hewlett-Packard computers). Drivers require system RAM data to support one more application program functions (and, in some cases, subfunctions) for performing specific tasks. (For more information on drivers, consult the *The Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*)

3. Data areas

   To perform their functions, ROM BIOS drivers require data from either STD-BIOS data areas or EX-BIOS data areas. The data areas provide the means for the ROM BIOS drivers to maintain driver variables, data buffers, etc. The drivers differ in the way they handle data. (For more information on drivers, consult the *The Vectra System BIOS Technical Reference Manual for the HP Vectra Series of Personal Computers.*)

4.4.2 Option ROM

The System Interface PCA has two sockets which accept 32-Kbyte option ROM chips. If installed, the option ROMs are automatically enabled (by default). The option ROMs are addressable from hex 0E0000 to 0EFFFF, as well as from from hex FE0000 to FEFFFF and, on the QS/16 and QS/20, hex FFFE0000 to FFFEFFFF. (Via optional I/O accessory cards added on the backplane I/O, up to 128 Kbytes of ROM can also be added, addressable from hex 0C0000 to 0DFFFF.) Option ROMs can be disabled by the Processor Card Switch 1, setting 4 to the OFF position.

4.5 BACKPLANE I/O CONNECTOR SLOTS

The backplane I/O connector slots connect optional industry-standard accessory cards to the Vectra system. The figure "System Interface PCA Component Layout" in the introduction to this chapter shows the location of the seven backplane I/O connector slots. (See the "Processor/Memory PCA" chapter for a discussion of the backplane I/O bus.)

Of the seven backplane I/O connector slots, one is an 8-bit slot, and six are 16-bit slots. The slots allow for:

- 7 DMA channels—four 8-bit and three 16-bit, at 4 MHz
- 11 interrupt request channels
- lines for refresh of dynamic RAM
- generation of wait states

  Default wait states*:

  - 4 wait states during 8 bit I/O or memory access on an accessory card
  - 1 wait state during 16 bit I/O or memory access on an accessory card
- control lines for I/O and memory
- 8-bit or 16-bit data bus
- 20-bit or 24-bit address bus
- industry-standard 8-MHz timing
- QS/20: 10 MHz timing if all accessory cards run at 10 MHz.

(*) For slower accessory cards, additional wait states can be inserted as long as signal I/O CHRDY is pulled low.

Faster accessory cards can shorten I/O or memory accesses by pulling the signal 0WS* low. Refer to Table 4-15 for further details.

4.5.1 Pinout Diagrams and Signal Assignments for Backplane I/O Connector Slots

Figure 4-7 gives the pinout for the backplane I/O connector slots. The 8-bit I/O connector slot (slot 2) has a 62-pin I/O connector. The 16-bit I/O connector slots have a 98-pin I/O connector.

Table 4-14 gives the signal assignments for the backplane I/O connector slots. An 8-bit accessory card inserted in I/O connector slot 2 use the "A" and "B" signal assignments shown in Figure 4-7, while 16-bit accessory cards inserted in the remaining I/O connector slots use all the assigned signals. Table 4-15 describes the signal assignments. (An asterisk in the table "*" indicates a signal is defined as active low.)

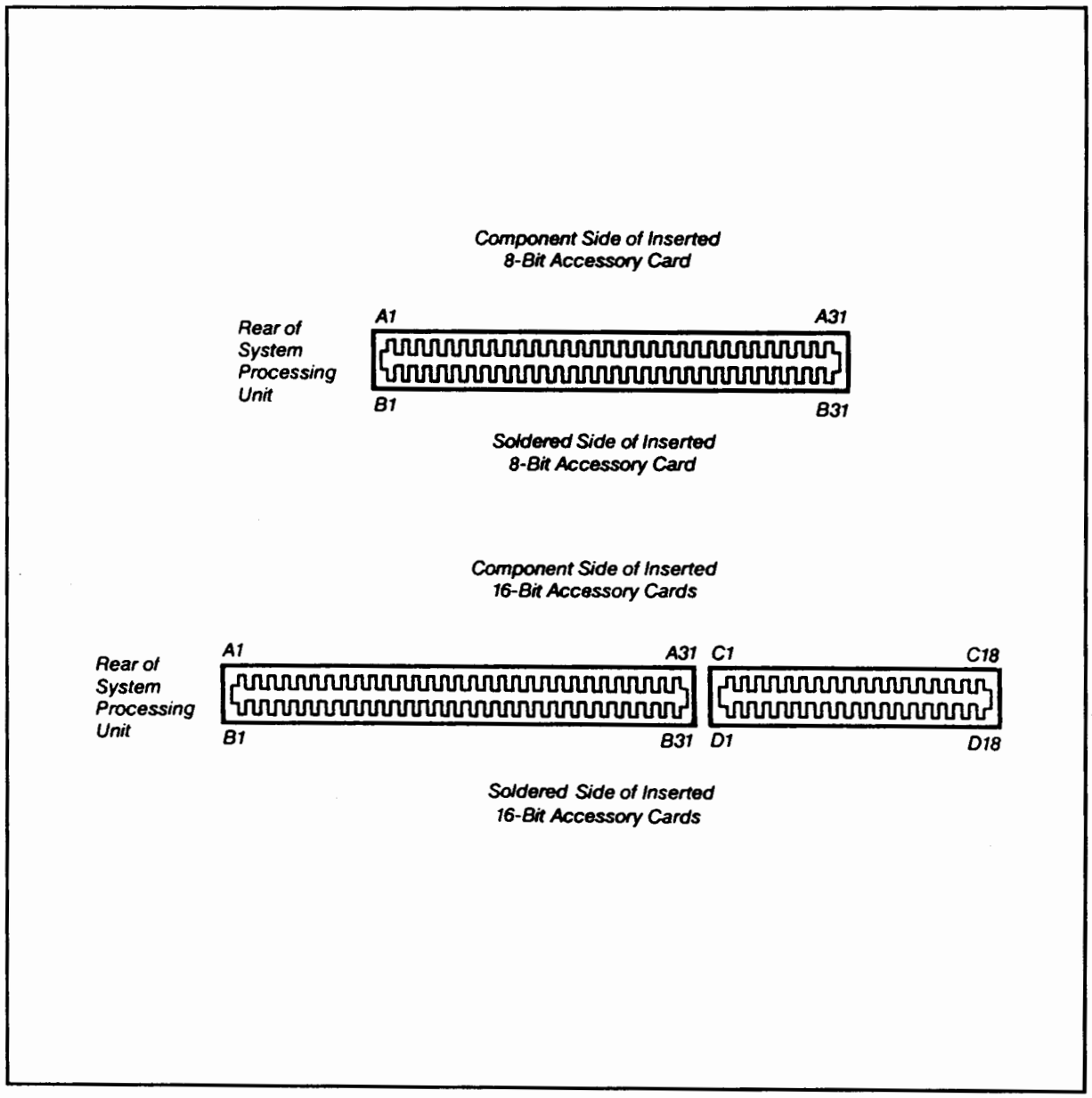


Figure 4-7. Pinout Diagrams for Backplane I/O Connector Slots

Table 4-14. Backplane I/O Connector Slot Signal Assignments

Pin	I/O	Signal Name	Pin	I/O	Signal Name
B1	Ground	GND	A1	In	I/O CHCK*
B2	Out	RESET DRV	A2	I/O	SD7
B3	Power	+5 Vdc	A3	I/O	SD6
B4	In	IRQ9	A4	I/O	SD5
B5	Power	-5 Vdc	A5	I/O	SD4
B6	In	DRQ2 (see 1)	A6	I/O	SD3
B7	Power	-12 Vdc	A7	I/O	SD2
B8	In	0WS*	A8	I/O	SD1
B9	Power	+12 Vdc	A9	I/O	SD0
B10	Ground	GND	A10	In	I/O CHRDY
B11	Out	SMEMW*	A11	Out	AEN
B12	Out	SMEMR*	A12	I/O	SA19
B13	I/O	IOW*	A13	I/O	SA18
B14	I/O	IOR*	A14	I/O	SA17
B15	Out	DACK3*	A15	I/O	SA16
B16	In	DRQ3	A16	I/O	SA15
B17	Out	DACK1*	A17	I/O	SA14
B18	In	DRQ1	A18	I/O	SA13
B19	I/O	REFRESH*	A19	I/O	SA12
B20	Out	SYSCLK	A20	I/O	SA11
B21	In	IRQ7	A21	I/O	SA10
B22	In	IRQ6	A22	I/O	SA9
B23	In	IRQ5	A23	I/O	SA8
B24	In	IRQ4	A24	I/O	SA7
B25	In	IRQ3	A25	I/O	SA6
B26	Out	DACK2* (see 1)	A26	I/O	SA5
B27	Out	T/C	A27	I/O	SA4

Table 4-14. Backplane I/O Connector Slot Signal Assignments (continued)

Pin	I/O	Signal Name	Pin	I/O	Signal Name
B28	Out	BALE	A28	I/O	SA3
B29	Power	+5 Vdc	A29	I/O	SA2
B30	Out	OSC	A30	I/O	SA1
B31	Ground	GND	A31	I/O	SA0
D1	I	MEM CS16*	C1	I/O	SBHE
D2	I	I/O CS16*	C2	I/O	SA23 (see note 2)
D3	I	IRQ10	C3	I/O	SA22
D4	I	IRQ11	C4	I/O	SA21
D5	I	IRQ12	C5	I/O	SA20
D6	I	IRQ15	C6	I/O	SA19
D7	I	IRQ14	C7	I/O	SA18
D8	O	DACK0*	C8	I/O	SA17
D9	I	DREQ0	C9	I/O	MEMR*
D10	O	DACK5*	C10	I/O	MEMW*
D11	I	DRQ5	C11	I/O	SD8
D12	O	DACK6*	C12	I/O	SD9
D13	I	DRQ6	C13	I/O	SD10
D14	O	DACK7*	C14	I/O	SD11
D15	I	DRQ7	C15	I/O	SD12
D16	Power	+5 Vdc	C16	I/O	SD13
D17	I	MASTER*	C17	I/O	SD14
D18	Ground	GND	C18	I/O	SD15

Notes:

1. DRQ2 and DACK2* are used by the flexible disc controller on the Four-Function Controller Card.
2. SA17 to SA23 are called LA17 to LA23 on the standard AT bus.

   I/O and memory cards must use SA17 to SA19 on pins C6, C7 and C8 instead of SA17 to SA10 on pins A12, A13 and A14 to generate I/OCS16* or MEMCS16*. This is because these address signals are different on a QS/16S. SA17-19 pins C6-8 are generated earlier than SA17-19 pins A12-14.
3. An asterisk (*) indicates active low signals.
4. "A" pins are on the component side; "B" pins are on the circuit side.
5. "C" pins are on the component side; "D" pins are on the circuit side.

Table 4-15. Backplane I/O Connector Slot Signal Descriptions

Signal Name	Signal Description
AEN	ADDRESS ENABLE informs the system that the DMA controller has control of address and control buses. Active during DMA transfers.
BALE	BUFFERED ADDRESS LATCH ENABLE is from the 82A306 control buffer. Its falling edge indicates valid address and control signals. Forced high during DMA cycles.
DACK0,1,2,3*, DACK5,6,7*	DMA ACKNOWLEDGE* signals are used by the Processor/Memory PCA to acknowledge direct-memory access requests.
DREQ0,1,2,3, DREQ5,6,7	DMA REQUEST signals are used by accessory cards to request direct-memory access service or to gain system control. The DMA channels are prioritized, with Channel 0 having the highest priority and channel 7 having the lowest. A DMA request signal must be held high until its corresponding acknowledge signal is asserted.
I/O CHCK*	I/O CHANNEL CHECK* is used by an accessory card to indicate to the system that an error has been detected on the card.
I/O CHRDY	I/O CHANNEL READY synchronizes slow memory or I/O devices during read and write operations. If an accessory card is to extend a read or write operation, it should pull this line low as soon as a valid address and a read or write command is detected. A read or write operation should not be extended to more than 15 SYSCLK cycles. Clock cycles added via this signal are in addition to any added by the system.
I/O CS16*	I/O CHIP SELECT (16 bits)* indicates to the system that an accessory card can perform 16-bit I/O operations. The driver should be an open collector or a tri-state device capable of sinking 20 mA.
IOR*	I/O READ* indicates an I/O read cycle is in progress. IOR* may be driven by a DMA controller or by an external microprocessor (if MASTER is asserted).
IOW*	I/O WRITE* indicates an I/O write cycle is in progress. IOW* may be driven by a DMA controller or by an external microprocessor (if MASTER is asserted).
IRQ3,4,5,6,7, IRQ9,10,11,12, IRQ14,15	INTERRUPT REQUEST signals are used by accessory cards to signal request for interrupt service. These edge-sensitive signals are asserted by a low-to-high transition. The signal must be held high until the interrupt is acknowledged. The IRQ signals are prioritized as follows, starting with the highest prioritization: IRQ9, 10, 11, 12, 14, 15, 3, 4, 5, 6, 7. Table 4-2 lists the IRQ allocation.

Table 4-15. Backplane I/O Connector Slot Signal Descriptions (continued)

Signal Name	Signal Description
SA17 to SA23	LINE ADDRESS signals are upper system address lines. When combined with system address lines SA0 to SA19 they produce 16 Mbytes of memory address space. These signals are latched by the accessory card on BALE's trailing edge. SA17 to SA23 may be driven by a DMA controller or 80386 microprocessor on the I/O channel.
MASTER*	MASTER* signal used by an accessory card to disable the 80386 and gain control of the system buses. To gain control, one of the DMA channels must be placed in the cascade mode, and the accessory card must issue a DMA request (DREQ) and receive an acknowledge (DACK). The accessory card may then assert MASTER* and gain control of the system. It must wait one clock cycle before attempting to drive the address or data lines, and two clock cycles before issuing a read or write command. Holding this signal low for 15 microseconds or more may cause a memory loss because of the absence of refresh.
MEMCS16*	MEMORY CHIP SELECT (16 bits)* indicates to the system that the accessory card can perform 16-bit memory operations. The driver should be an open collector or a tri-state device capable of sinking 20 mA, and this signal should be derived from LA17 to LA23.
MEMR*	MEMORY READ* indicates a memory read cycle is in progress. MEMR may be driven by a DMA controller or by an external microprocessor (if MASTER* is asserted).
MEMW*	MEMORY WRITE* indicates a memory write cycle is in progress. MEMW* may be driven by a DMA controller or by an external microprocessor (if MASTER* is asserted).
OSC	OSCILLATOR, a 14.318 MHz timing reference signal with a 50% duty cycle and a period of approximately 70 nanoseconds, is asynchronous with the SYSCLK signal.
REFRESH*	REFRESH*, which indicates a memory refresh operation is in progress, may be driven by a microprocessor on the I/O channel.
RESET DRV	RESET DRIVE resets all system devices during power-on resets and indicates low line voltage conditions.

Table 4-15. Backplane I/O Connector Slot Signal Descriptions (continued)

Signal Name	Signal Description
SA0 to SA19	SYSTEM ADDRESS lines, when combined with SA17 to SA23, produce 16 Mbytes of memory address space. SA0 to SA19 begin to change on BALE's rising edge and are latched for the cycle's duration by BALE's falling edge. SA0 to SA19 may be driven by a DMA controller or processor on the I/O channel. The system refresh controller places the refresh address on SA0 to SA7 during refresh cycles.
SBHE*	SYSTEM BUS HIGH ENABLE indicates that data are to be transferred on SD8 to SD15. SBHE* indicates a 16-bit transfer or an 8-bit transfer to an odd address (A0=1) is in progress.
SD0 to SD15	SYSTEM DATA bus signals transfer data to and from the system. Sixteen-bit transfers occur on SD0 to SD15. Eight-bit transfers occur on SD0 to SD7, unless SBHE* is asserted, in which case, data are transferred on SD8 to SD15. Sixteen-bit to 8-bit transfers are multiplexed by the backplane state machine into two 8-bit transfers on SD0 to SD7.
SMEMR*	SYSTEM MEMORY READ* indicates a system memory read cycle is in progress. SMEMR* is active if MEMR* is active and the address decode circuit indicates a valid address in the bottom 1 Mbyte of memory space.
SMEMW*	SYSTEM MEMORY WRITE* indicates a memory write cycle is in progress. SMEMW* is active if MEMW* is active and the address decode circuit indicates a valid address in the bottom 1 Mbyte of memory space.
SYSCLK	SYSTEM CLOCK, the 8 MHz system clock for the 80386, has a 50% duty cycle and a period of approximately 125 nanoseconds, and can be used to synchronize activities to the 80386 microprocessor.
T/C	TERMINAL COUNT informs the system that the terminal count for one of the DMA channels has been reached.
0WS*	ZERO WAIT STATE* indicates to the system that a read or write operation can take place without additional system generated wait states. To perform a 16-bit memory cycle with zero wait states, this signal should be asserted as soon as a valid address decode and a read or write command is detected. To shorten cycles for 8-bit devices, 0WS* should be asserted on the falling edge of SYSCLK after detecting a valid address and a read or write command for two wait states. If asserted on the second falling edge of SYSCLK after detecting a valid address and a read or write command, three wait states will be generated for 8-bit devices. The driver should be an open collector or a tri-state device capable of sinking 20 mA.

*Active low

4.5.2 Backplane I/O Timing Diagrams

Figures 4-8 to 4-13 contain timing information.

This information is included as a guide to general system characteristics. If the following information is to be used by hardware developers or vendors, full qualification of all equipment should be performed to ensure that worst-case timing requirements and parameters are met.

All the values are in nanoseconds, except for the values given in note 45 which are in microseconds.

Table 4-16. Notes for Timing Diagrams

Figure	Note	Function	Minimum (1)	Maximum (2)
4-8	1	SYSCLK period (8 MHz)	-	125
4-8	2	BALE high from SYSCLK	-	9
4-8	3	BALE low from SYSCLK	-	14
4-8	4	SBHE* low from SYSCLK	-	21
4-8	5	SBHE* invalid from SYSCLK	-	16
4-8	6	SBHE* high from SYSCLK	-	19
4-8	7	SA/LA valid to SYSCLK	5	-
4-8	8	SA/LA tri-state from SYSCLK	-11	23
4-8	9	SMEMR*/SMEMW* low from SYSCLK	-	25
4-8	10	SMEMR*/SMEMW* high from SYSCLK	-	21
4-8	11	MEMR*/MEMW* low from SYSCLK	-	21
4-8	12	MEMR*/MEMW* high from SYSCLK	-	16
4-8	13	IOCHRDY setup to SYSCLK	30	-
4-8	14	IOCHRDY hold from SYSCLK	-2	-
4-8	15	MEMCS16*/IOCS16* setup to SYSCLK	48	-
4-8	16	MEMCS16*/IOCS16* hold from SYSCLK	25 **	-
4-8	17	0WS* setup to SYSCLK	34	-
4-8	18	0WS* hold from SYSCLK	-1	-
4-8	19	Number of idle states between immediate cycles	2 **	-
4-9	20	SD setup to SYSCLK, read cycle	23	-
4-9	21	SD hold from SYSCLK, read cycle	11	-
4-9	22	SD valid from SYSCLK, write cycle	-	47
4-9	23	SD hold from SYSCLK, write cycle	-	31

Table 4-16. Notes for Timing Diagrams (continued)

Figure	Note	Function	Minimum (1)	Maximum (2)
4-10	24	IOR*/IOW* low from SYSCLK	-	31
4-10	25	IOR*/IOW* high from SYSCLK	-	28
4-11	26	SA0 low to high from SYSCLK	-	48
4-12	27	DREQn hold from DACKn* valid	0	-
4-12	28	DREQn low setup to SYSCLK	0	-
4-12	29	AEN high to SYSCLK	3	-
4-12	30	AEN low from SYSCLK	310 **	-
4-12	31	SA/LA valid from SYSCLK	-	90
4-12	32	SA/LA tri-state from SYSCLK	-	85
4-12	33	DACKn* low from SYSCLK	-	105
4-12	34	DACKn* high from SYSCLK	-	105
4-12	35	IOR* low from SYSCLK	-	138
4-12	36	IOR* high from SYSCLK	-	119
4-12	37	CMD *** driven high from SYSCLK	-	109
4-12	38	T/C delay from SYSCLK	-	60
4-12	39	IOCHRDY setup to SYSCLK	35	-
4-12	40	IOCHRDY hold from SYSCLK	20	-
4-13	41	MEMR* low from SYSCLK	-	33
4-13	42	MEMR* high from SYSCLK	-	28
4-13	43	SA valid after REF* valid	-	64
4-13	44	SA invalid after REF* invalid	-	33
4-13	45	Refresh cycle	15 ms**	-

Note: Except for the value given for Note 45, all values are in nanoseconds.
* Active low.
** Typical value.
*** CMD = IOR*, IOW*, SMEMR*, or SMEMW*

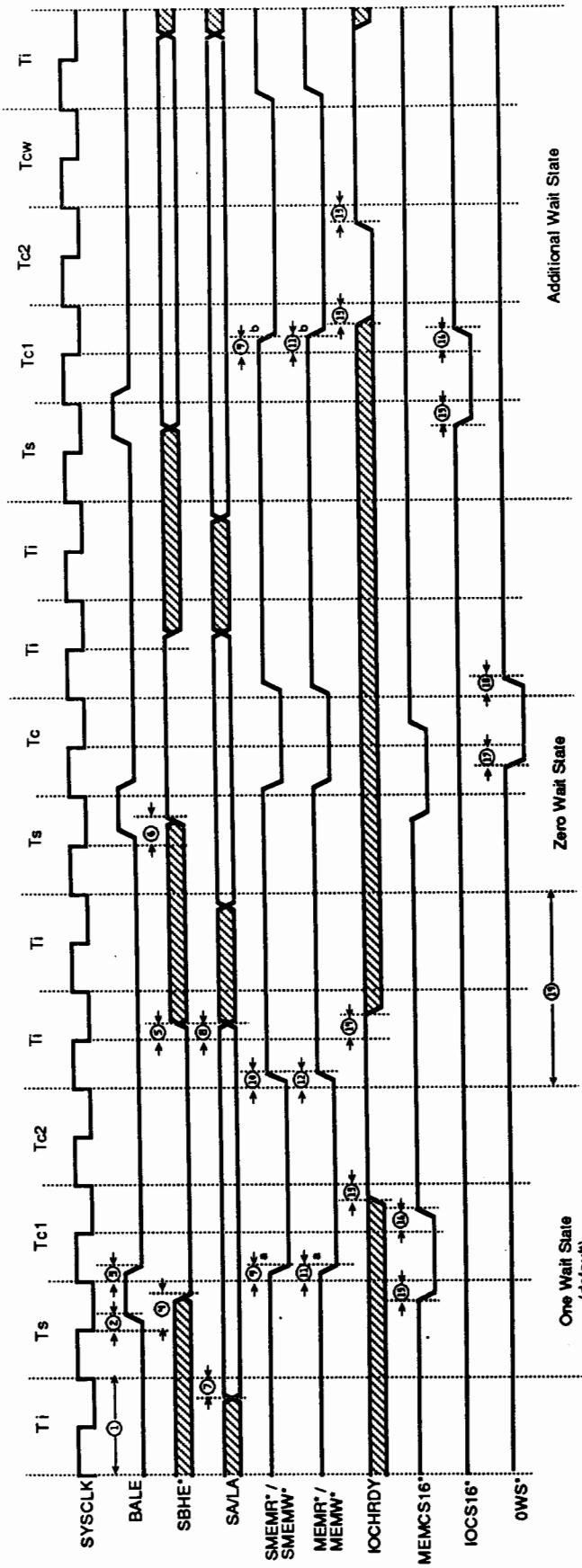


Figure 4-8. Backplane I/O Timing diagram : Common timing

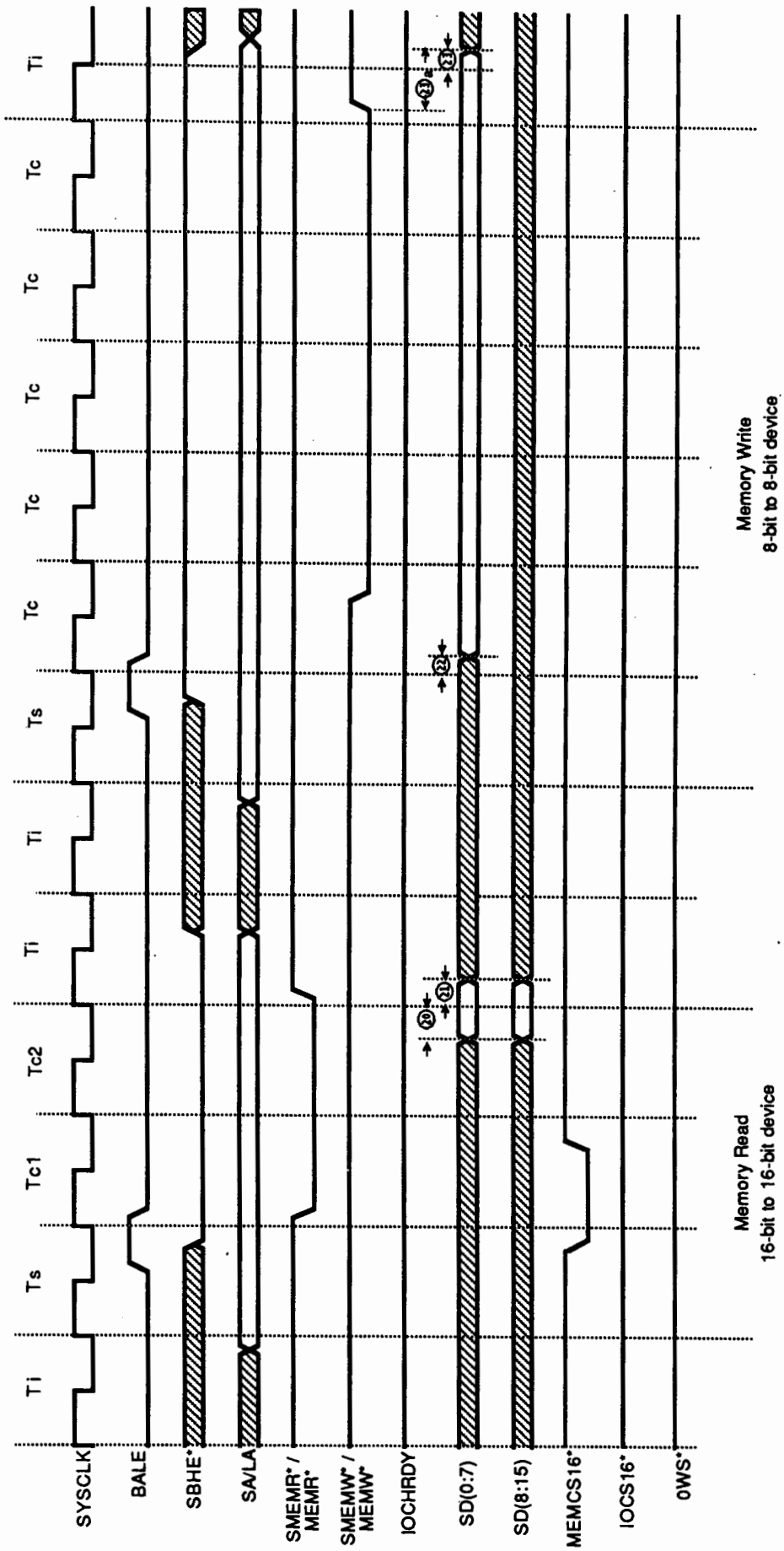


Figure 4-9. Backplane I/O Timing diagram : Memory cycle

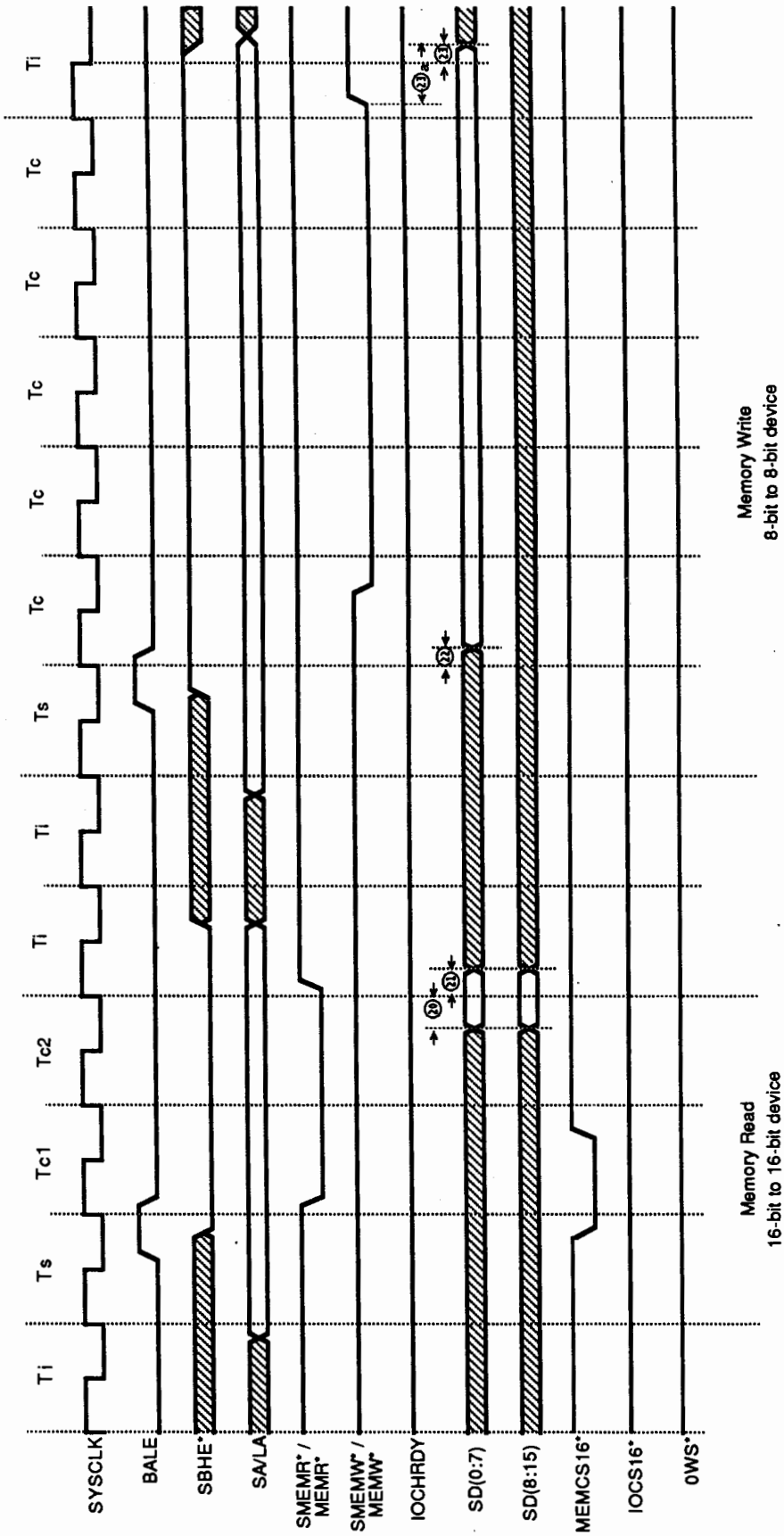


Figure 4-10. Backplane I/O Timing diagram : I/O cycle

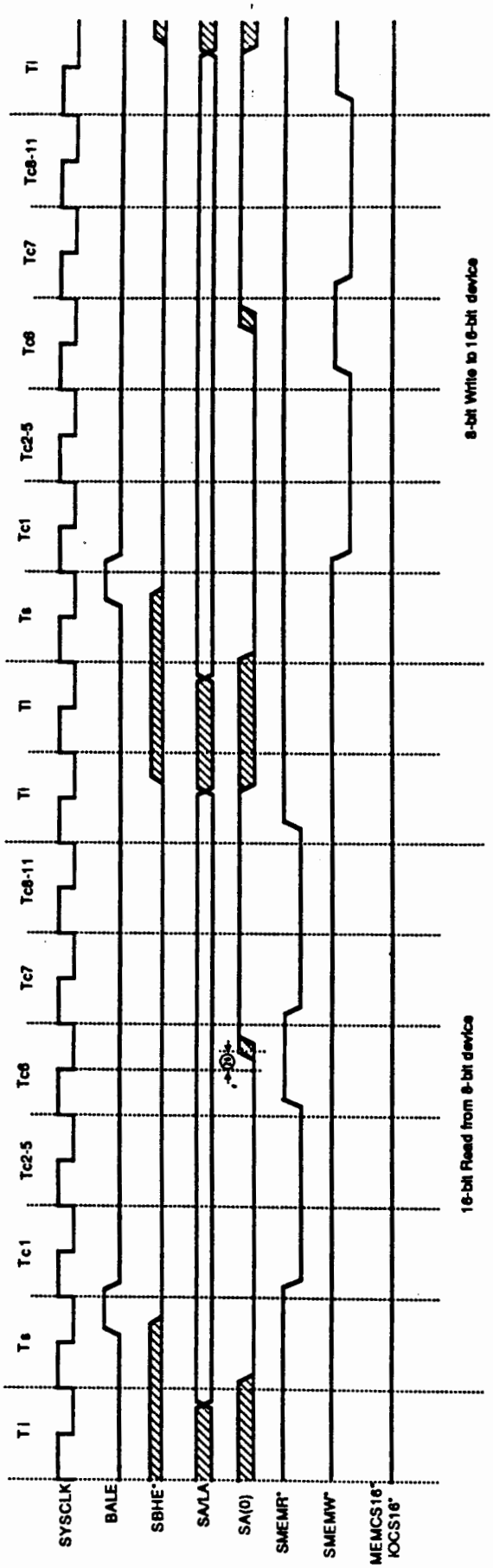


Figure 4-11. Backplane I/O Timing diagram : 16 bit to 8 bit cycles

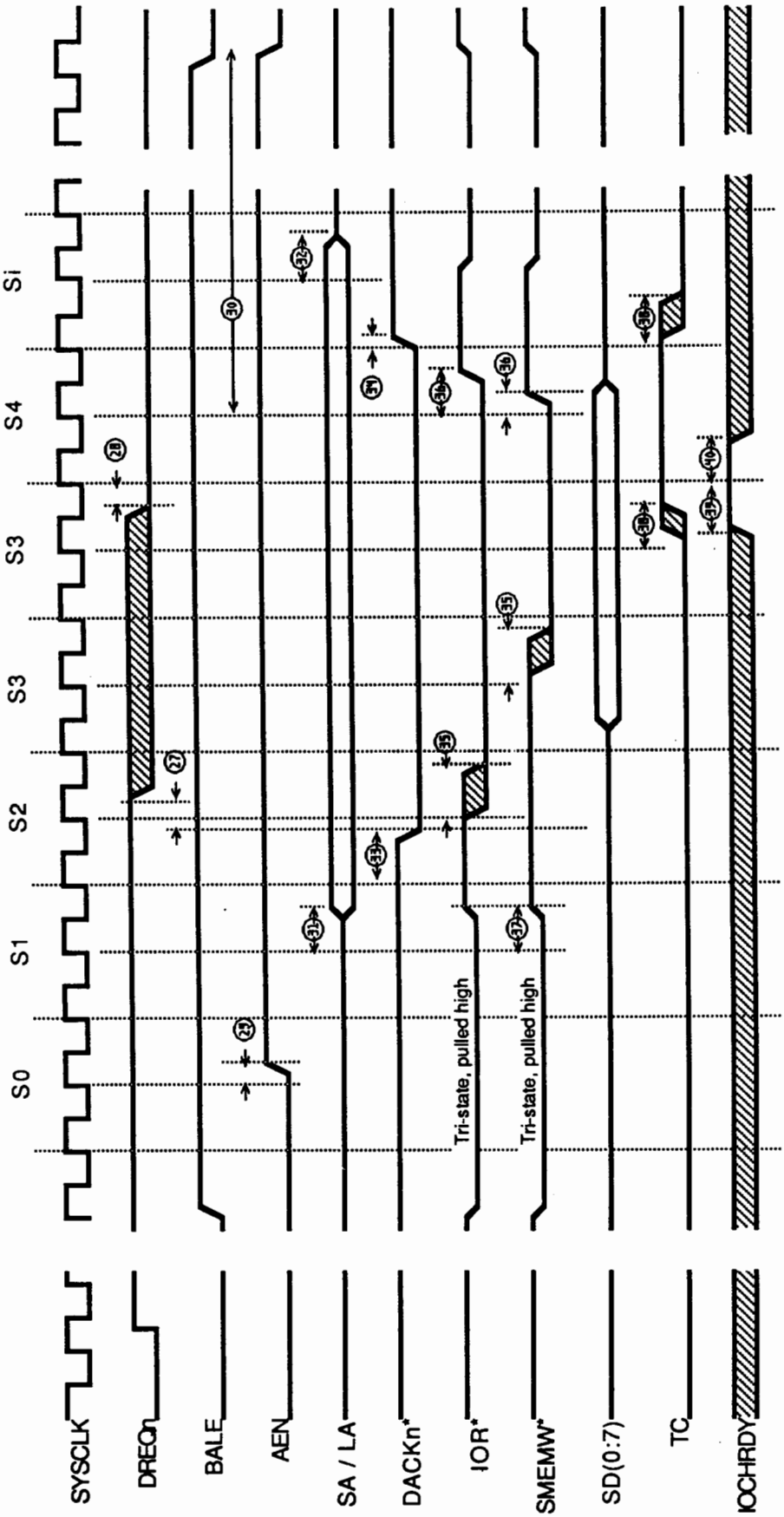


Figure 4-12. Backplane I/O Timing diagram : Single byte/word DMA transfer from I/O to memory

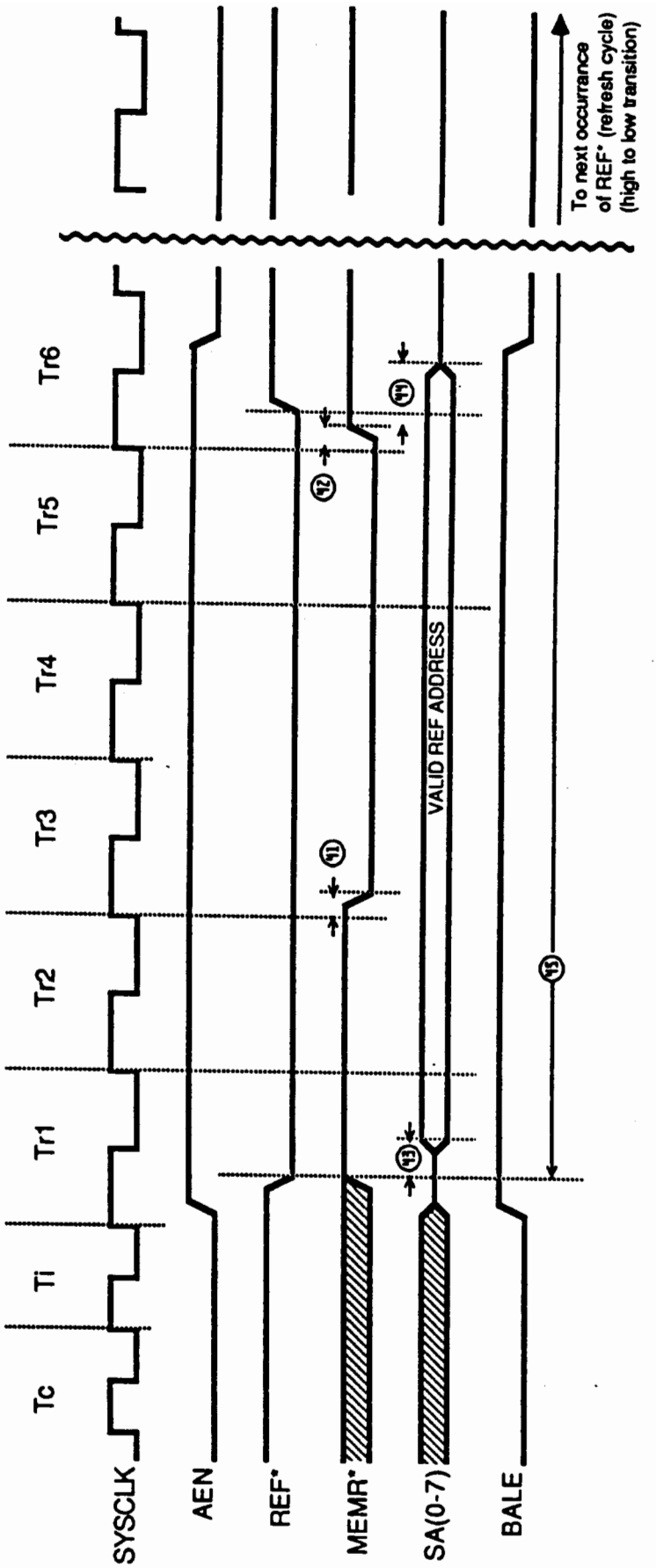


Figure 4-13. Backplane I/O Timing diagram : Refresh

5

Power Supply

5.1 INTRODUCTION

This chapter describes the HP Vectra QS PC power supply, the major components of which are listed below.

Major Power Supply Components

- AC input receptacle
- AC output outlet
- fan
- fuse and fuse holder
- on/off switch
- power cables to disc drives
- power connector to System Interface PCA

The power supply is installed in a zinc-plated steel enclosure, located inside the HP Vectra QS PC System Processing Unit (SPU). The power supply provides power to the components given below. Through the convenience outlet (also known as the AC output outlet), the power supply can provide AC power to the monitor. (Note that a VGA monitor plugs into the wall socket only.)

Components Receiving Power from Power Supply

- Backplane I/O
- Flexible disc drives
- Hard disc drives
- Keyboard and other input devices
- Processor/Memory PCA (power supplied via the System Interface PCA)
- Printed circuit assemblies

5.2 POWER SUPPLY LINE INPUT

The auto-ranging worldwide power supply senses the line voltage and frequency and automatically configures itself to operate with one of the two configuration voltages given in Table 5-1.

Table 5-1. Power Supply Voltages

Line Voltage	Line Frequency	Configuration Voltage
90 to 132 VAC	47 to 63 Hz	115 VAC
198 to 264 VAC	47 to 63 Hz	230 VAC

5.3 POWER SUPPLY OUTPUT

Via the System Interface PCA connector J1, the power supply provides ±5Vdc and ±12Vdc outputs to the System Interface PCA and to the Processor/Memory PCA (via System Interface PCA card edge connectors). Through connector J1, the power supply also provides the PFAIL signal discussed in this chapter's section, "Power Supply Operating Status Indicator."

Through the three identical power cables shown in Figure 5-1 (J2 through J4), the power supply provides +5 Vdc and +12 Vdc outputs to disc drives, according to their power needs. In addition, on the rear of the SPU, the convenience outlet can supply power of up to 150 watts.

Figure 5-1 gives the pinouts for the power supply connectors, and Table 5-2 gives the pin assignments to power supply connector J1. Table 5-3 gives the pin assignments to power supply connectors J2-J4. Table 5-4 gives the power supply's output at start-up and 30 seconds after start-up.

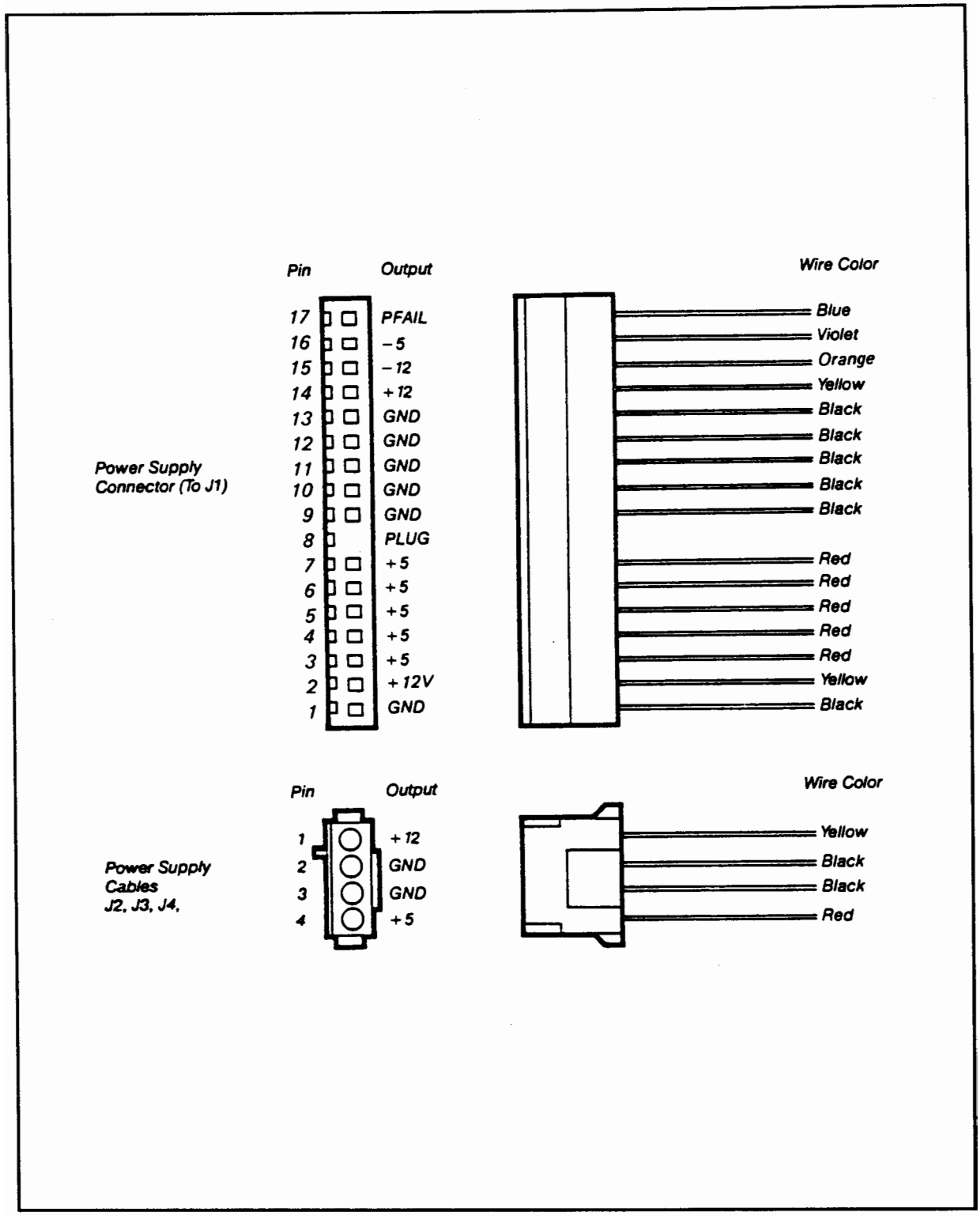


Figure 5-1. Power Supply Connector Pinouts

Table 5-2.
Pin Assignments for Power Supply Connector J1 (To System Interface PCA)

J1 Pins	Vdc Output	Maximum Current Drawn per Pin
17 (Gold Pin)	PFAIL*	*
16	−5 Vdc	−0.3 Amps
15	−12 Vdc	−0.3 Amps
14	+12 Vdc	1.7 Amps
9-13	Ground	—
8	Not used	
3-7	+5 Vdc	3.3 Amps
2	+ 12 Vdc (Not used)	
1	Ground	—

See section in this chapter, "Power Supply Operating Status Indicator."

Table 5-3.
Pin Assignments for Power Supply Connectors J2 to J4 (Cables To Disc Drives)

J2 to J4 Pins	Vdc Output	Maximum Current Drawn (per Pin)
1	+12 Vdc	5 Amps
2,3	Ground	—
4	+5 Vdc	2 Amps

Table 5-4. Power Supply Output at Start-up and After Start-up

Startup voltage	Voltage range	Minimum	Maximum	Ripple(p-p)
+5	+4.75 to +5.25V	5.0A	18.3A	50mV
+12	+11.4 to +12.6V	0.0A	1.0A	120mV
−5	−5.25 to −4.75	0.0A	0.25A	50mV
−12	−12.6 to −11.4	0.0A	0.25A	120mV
Total Power: 176 watts maximum				
30 seconds after startup				
+5	+4.75 to +5.25V	5.0A	17.5A	50mV
+12	+11.4 to +12.6V	0.0A	1.0A	120mV
−5	−5.25 to −4.75	0.0A	0.25A	50mV
−12	−12.6 to −11.4	0.0A	0.25A	120mV
Total Power: 135 watts maximum				

5.3.1 Power to Backplane I/O

Each of the +5 Vdc backplane I/O connector slots can support an average of eight watts per channel. Table 5-5 gives the voltage and maximum total current for the backplane I/O connector slots, and the average current per backplane I/O connector slot.

For the backplane I/O connector pin assignments, refer to the chapter, *System Interface PCA*.

Table 5-5. Power to Backplane I/O Connector Slots

Backplane I/O Voltage	Maximum Total Current for Slots	Average Current/Slot
+ 5 Vdc	7.5 Amps	1.3 Amps
+12 Vdc	0.5 Amps	0.06 Amps
− 5 Vdc	0.3 Amps	0.03 Amps
−12 Vdc	0.3 Amps	0.03 Amps

5.4 POWER SUPPLY PROTECTION

5.4.1 Line Dropout Protection

Under any condition, including low line power at rated load, the power supply will continue to deliver regulated outputs when a 20 millisecond power line dropout occurs at the input to the power supply.

5.4.2 AC Inrush Current Protection

Under any condition, AC inrush current for the power supply is limited to 40 Amps and shall not "blow" the power supply's fuse. (Under any conditions, the AC inrush current for the convenience outlet, an AC output outlet on the rear of the SPU, is 30 Amps.)

5.4.3 Undercurrent Protection

Any or all power supply outputs may be open without damage to the power supply. (For the +5 Vdc power supply to operate normally, the minimum load is 2 Amps.)

5.4.4 Overcurrent Protection

When there exists an overcurrent situation (i.e., a short circuit occurs on the +5 or +12 Vdc outputs), the power supply turns off. To start the power supply again, depress the power supply's ON/OFF switch to the off position, remove the fault, and then turn on the power supply. (The −5 and −12 Vdc outputs are internally protected against a maximum short circuit current of 0.5 Amps, and if a short circuit does occur, the power supply does not turn off.)

5.4.5 Overvoltage Protection

If overvoltage occurs on the +5 or +12 Vdc line, within 500 microseconds, the power supply's switch controller turns off all the power supply outputs. To start the power supply again, depress the power supply's ON/OFF switch to the off position, remove the fault, and then turn on the power supply.

If overvoltage occurs on the −5 or −12 Vdc line, the +5 and +12 Vdc outputs will not turn off, as the −5 and −12 Vdc outputs are internally protected to a maximum short circuit current of approximately 0.5 Amps. (When the cause of the overvoltage situation is removed, the −5 or − 12 Vdc outputs return to normal operation.)

Table 5-6 gives the voltage levels which cause a power supply overvoltage situation.

Table 5-6. Voltage Levels Which Cause Power Supply Overvoltage

Nominal Power Supply Voltage	Maximum Over-Voltage Level
+ 5 Vdc	+ 7 Vdc
+12 Vdc	+17 Vdc
− 5 Vdc	*
−12 Vdc	*

*Inherent overvoltage protection at any voltage level.

5.4.6 Fuse and Fuse Holder

To protect the HP Vectra QS PC from overvoltage and overcurrent, the power supply has a fuse, rated at eight Amps. (The fuse holder is next to the AC output outlet, and inside the power supply, which must be removed from the SPU to replace the fuse. The fuse is not a user-replaceable item.)

5.4.7 Fan

The power supply fan provides at least 52 cubic feet of air per minute to cool the power supply and disc drives.

5.5 POWER SUPPLY OPERATING STATUS INDICATOR

The PFAIL signal (pin 1 of the System Interface PCA's J1 power connector) indicates the power supply's operating status. If the power supply is operating properly, within 100 milliseconds after the +5 Vdc output has reached its minimum sense level, the PFAIL signal goes low to indicate proper power supply operation. If the power supply is not operating properly, the PFAIL signal goes high.

When the AC input voltage either has been removed or has dropped to an insufficient level, the rising edge of the PFAIL signal indicates to the real-time clock and CMOS RAM to go into a power-down mode and operate from the system's battery. When the AC input voltage is replaced or is once again at a sufficient level, PFAIL generates a system reset signal via an interrupt control.

Figure 5-2 gives the PFAIL timing diagram. Figures 5-3 and 5-4 give the PFAIL functional block diagram. (For a description, refer to "Bus Controller Reset Control" in Chapters 2 and 3.)

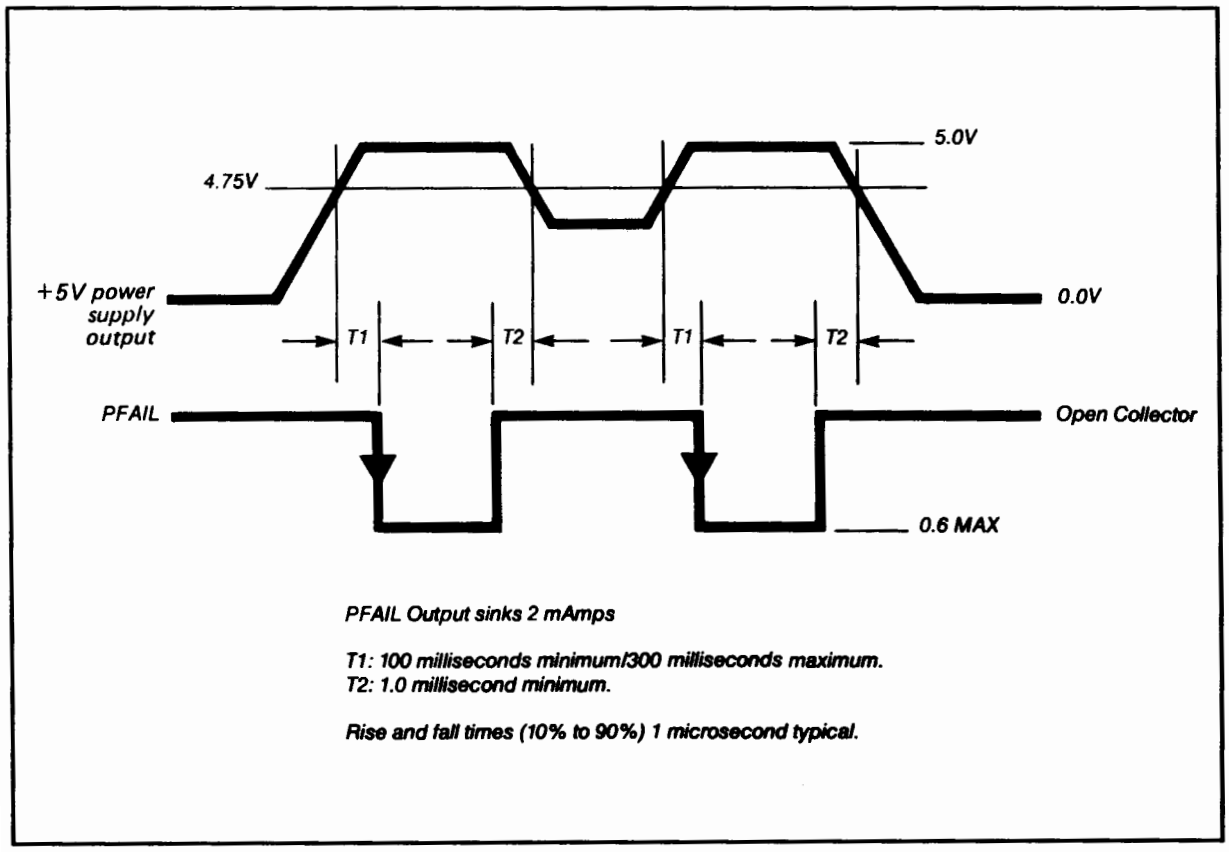


Figure 5-2. PFAIL Timing Diagram

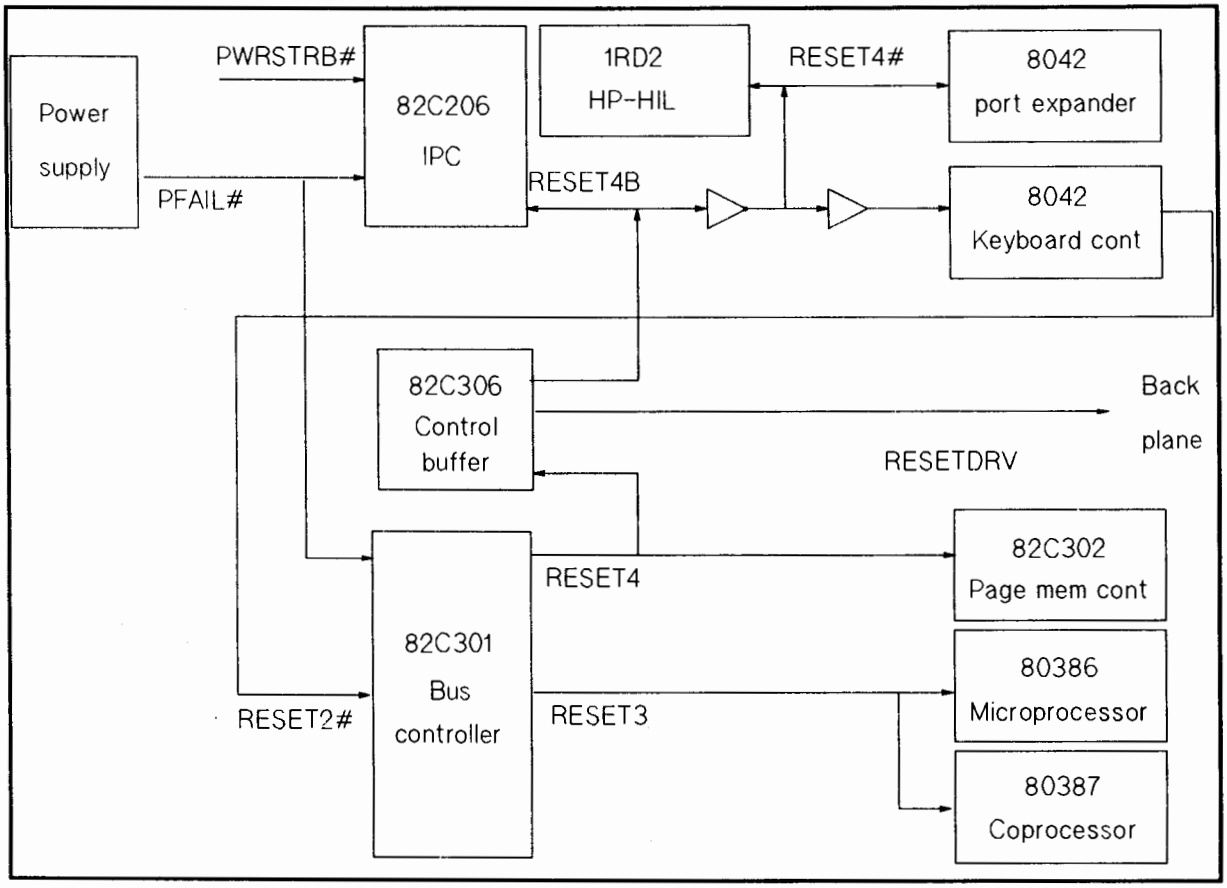


Figure 5-3. QS/16 & QS/20 PFAIL Block Diagram

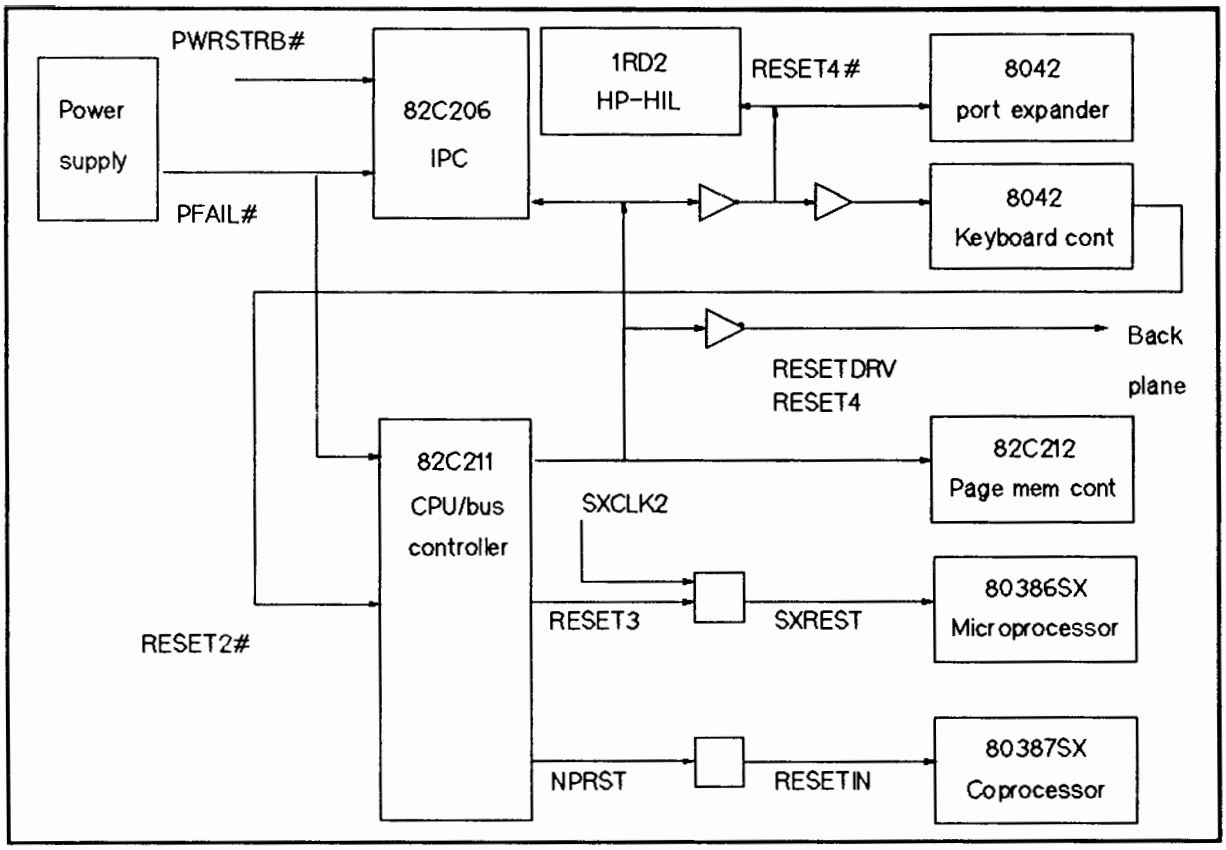


Figure 5-4. QS/16S PFAIL Block Diagram

5.6 BATTERY POWER

A 6-Volt lithium system backup battery, located on the power supply, provides power to the real-time clock and CMOS RAM during power-down and power system failure. The battery has an average life of 2.3 years.

A

I/O Address Map

Table A-1 gives the I/O address map for the central processing unit. The HP Vectra QS PC uses the first 1024 I/O hex addresses, 0000 through 03FF.

Table A-1. I/O Address Map for CPU Components

Hex Address	I/O Address Description
0000-000F	IPC* DMA Controller No. 1 Registers
0010-001F	Reserved
0020-0021	IPC* Interrupt Controller No. 1 Registers
0022	82Cxxx Index Register
0023	82Cxxx Data Register
0024-002F	Reserved
0040-0043	IPC* Counter/Timer Registers
0044-005F	Reserved
0060	8042 Keyboard Controller, Data Buffer
0061	82C301 Bus Controller Port B Status Register (Read/Write)
0062	8042 Keyboard Controller, Data Buffer
0063	82C301 Bus Controller Port B Status Register (Read/Write)
0064	8042 Keyboard Controller, Status/Command Buffer
0065	8042 Port Expander (Read/Write)
0066	8042 Keyboard Controller, Status/Command Buffer
0067	8042 Port Expander (Read/Write)
0068	8042 Keyboard Controller Command Register
0069	8042 Port Expander (Read/Write)
006A	8042 Keyboard Controller Command Register
006B	Reserved
006C	IRD2 HP-HIL Master Link Controller Register 0
006D	IRD2 HP-HIL Master Link Controller Register 1
006E	IRD2 HP-HIL Master Link Controller Register 2
006F	IRD2 HP-HIL Master Link Controller Register 3
0070	Real-Time Clock/CMOS RAM Address (D0 to D6), NMI Enable (D7) (Write)
0071	Real-Time Clock/CMOS RAM Data (Read/Write)
0072-0077	Reserved
0078	Hard Reset Enable/Disable (D7) (Write)
0079-007F	Reserved

* Refer to I/O Address Map for IPC components in the "System Interface PCA" chapter.

Table A-1. I/O Address Map for CPU Components (continued)

Hex Address	I/O Address Description
0080-008F	IPC* DMA Page Register
0090-009A	Reserved
009B	Mode switch
009C-009F	Reserved
00A0-00A1	IPC* Interrupt Controller No. 2 Register
00A2-00BF	Reserved
00C0-00DF	IPC* DMA Controller No. 2 Register
00E0-00EF	Reserved
00F0	Clear 80387 Coprocessor Busy
00F1	Reset 80387 Coprocessor
00F2-00F7	Reserved
00F8-00FF	80387 Coprocessor Command Registers
0100-016F	Undefined
0170-0178	Secondary Hard Disc Controller Registers
0179-017F	Reserved
0180-01EF	Undefined
01F0-01F8	Primary Hard Disc Controller Registers
01F9-01FF	Reserved
0200-0207	Game Controllers Registers
0208-0277	Undefined
0278-027F	Parallel Port 2
0280-02E7	Undefined
02E8-02EF	Serial Port 4
02F0-02F7	Undefined
02F8-02FF	Serial Port 2
0300-0307	Prototype Card
0308-0367	Undefined
0370-0377	Secondary Flexible Disc Drive Controller Registers
0378-037F	Parallel Port 1
0380-038F	Synchronous Data Link Controller (SDLC), Bisynchronous 2
0390-039F	Undefined
03A0-03AF	Bisynchronous 1
03B0-03BF	Monochrome Display/Video Graphics Array Adapter
03C0-03CF	Enhanced Graphics Adapter/Video Graphics Array Adapter
03D0-03DF	Color/Graphics Video Accessory Card/Video Graphics Array Adapter
03E0-03E7	Undefined
03E8-03EF	Serial Port 3
03F0-03F7	Primary Flexible Disc Drive Controller Registers
03F8-03FF	Serial Port 1

* Refer to I/O Address Map for IPC components in the "System Interface PCA" chapter.

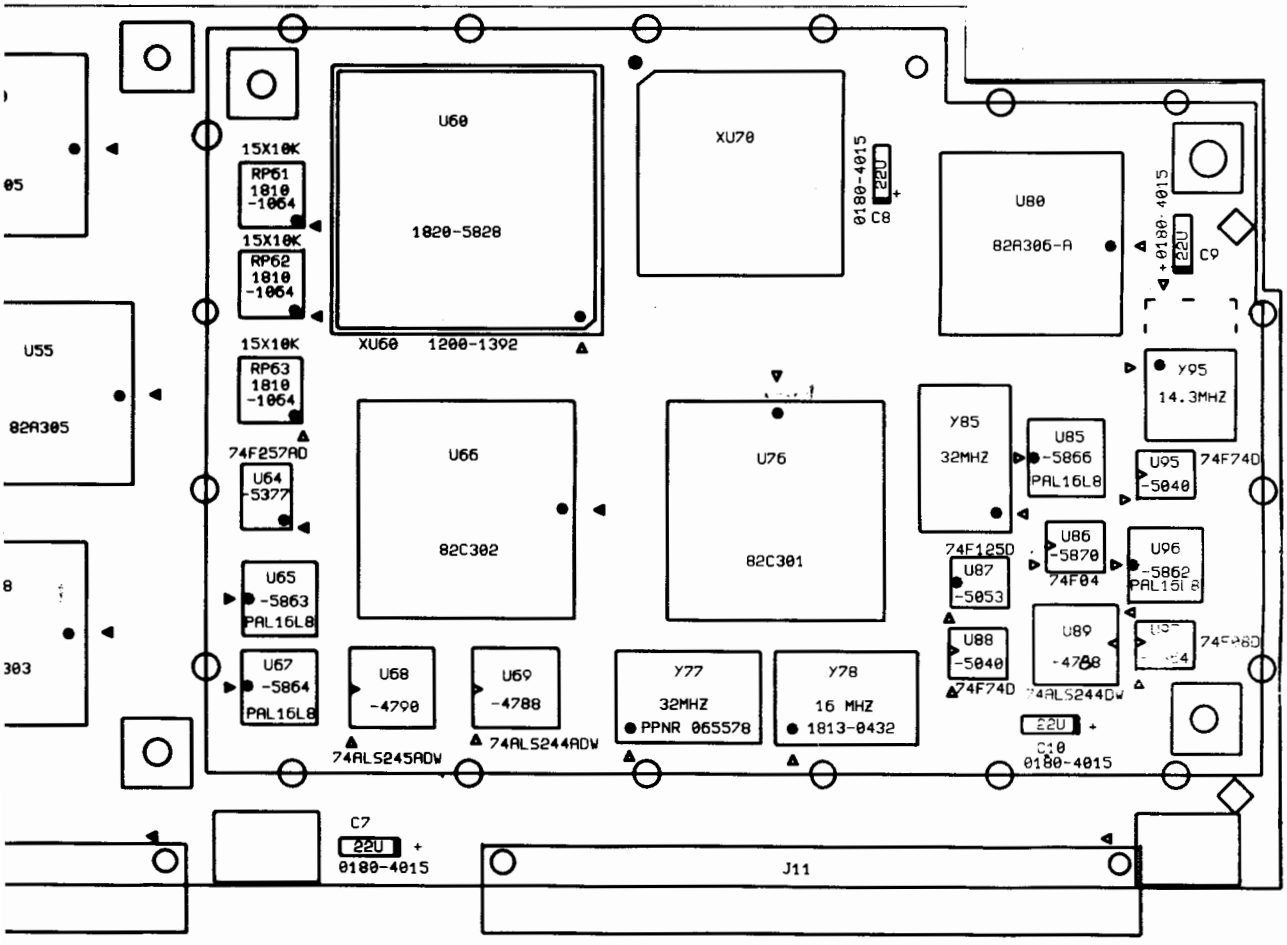
B

Drawings

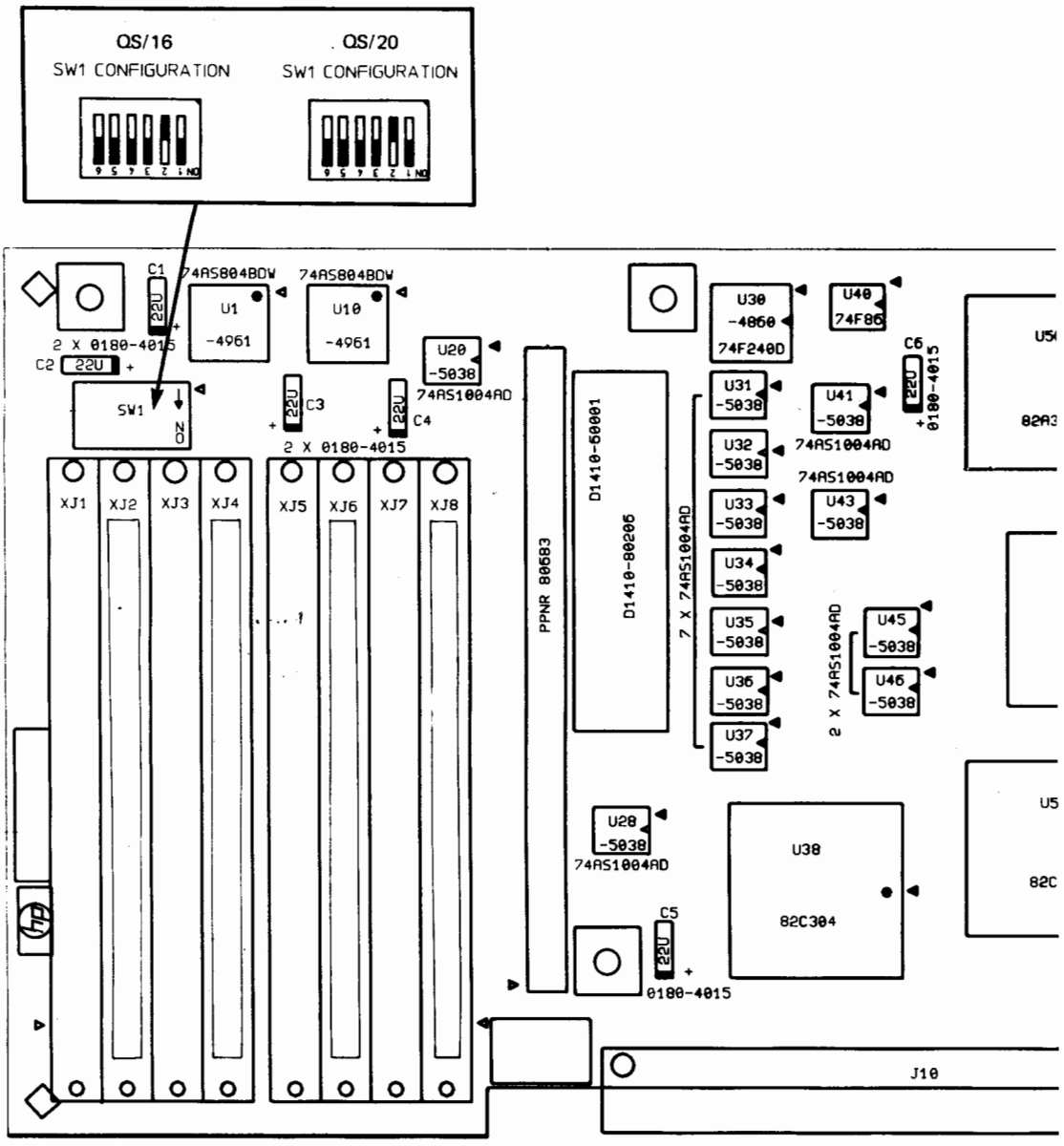
This appendix contains the following drawings:

1. Vectra QS/16, QS/20 Processor/Memory PCA component layout (2 sheets)
2. Vectra QS/16, QS/20 Processor/Memory PCA electrical schematics (11 sheets)
3. Vectra QS/16, QS/20 Memory Extension PCA component layout (1 sheets)
4. Vectra QS/16, QS/20 Memory Extension PCA electrical schematic (1 sheets)
5. Vectra QS/16S Processor/Memory PCA component layout (2 sheets)
6. Vectra QS/16S Processor/Memory PCA electrical schematics (9 sheets)
7. Vectra QS System Interface PCA component layout (1 sheet)
8. Vectra QS System Interface PCA electrical schematics (8 sheet)

Computer Museum

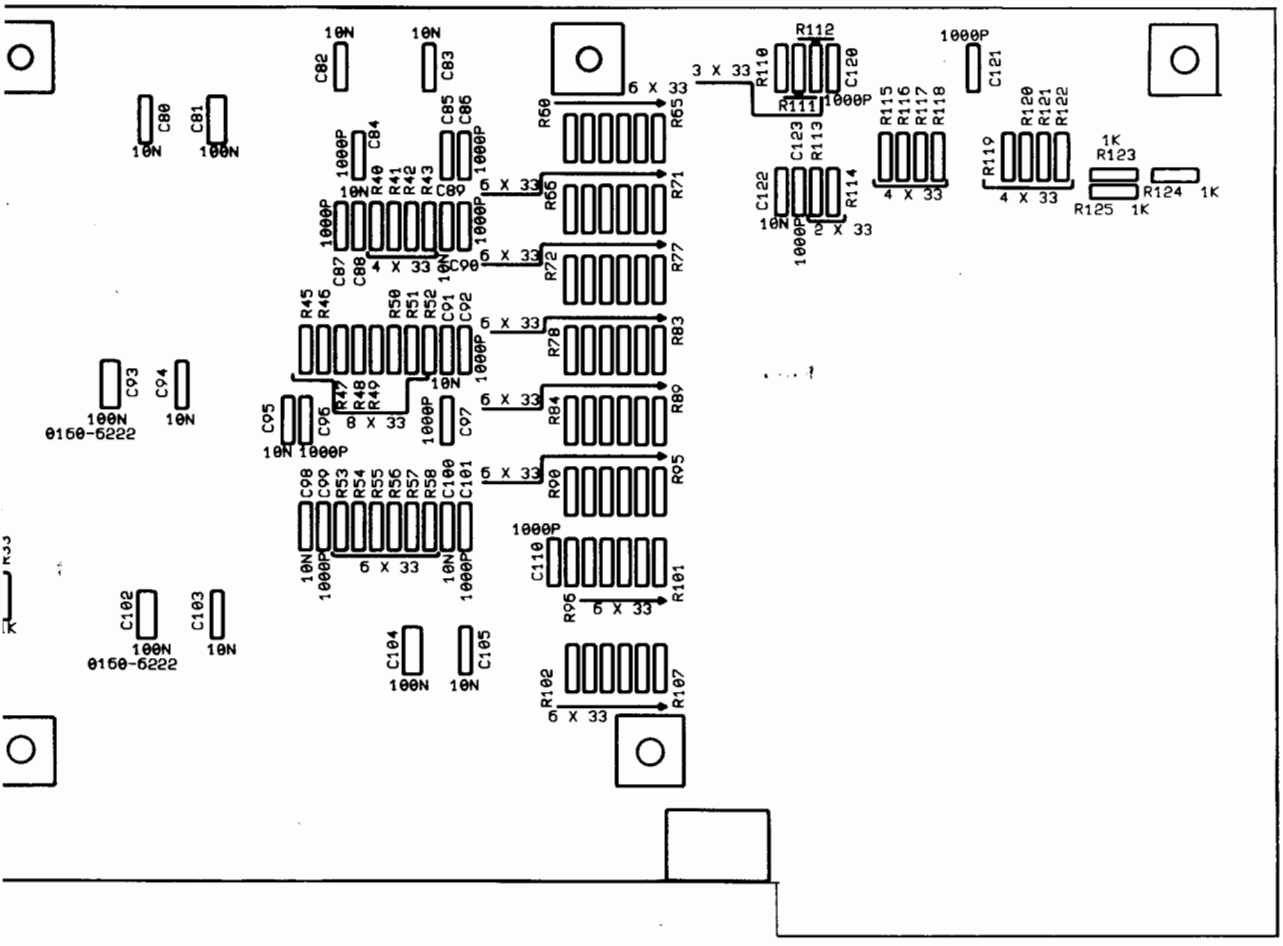


QS/16 QS/20 Processor/Memory PCA
Component Layout
(Component Side)

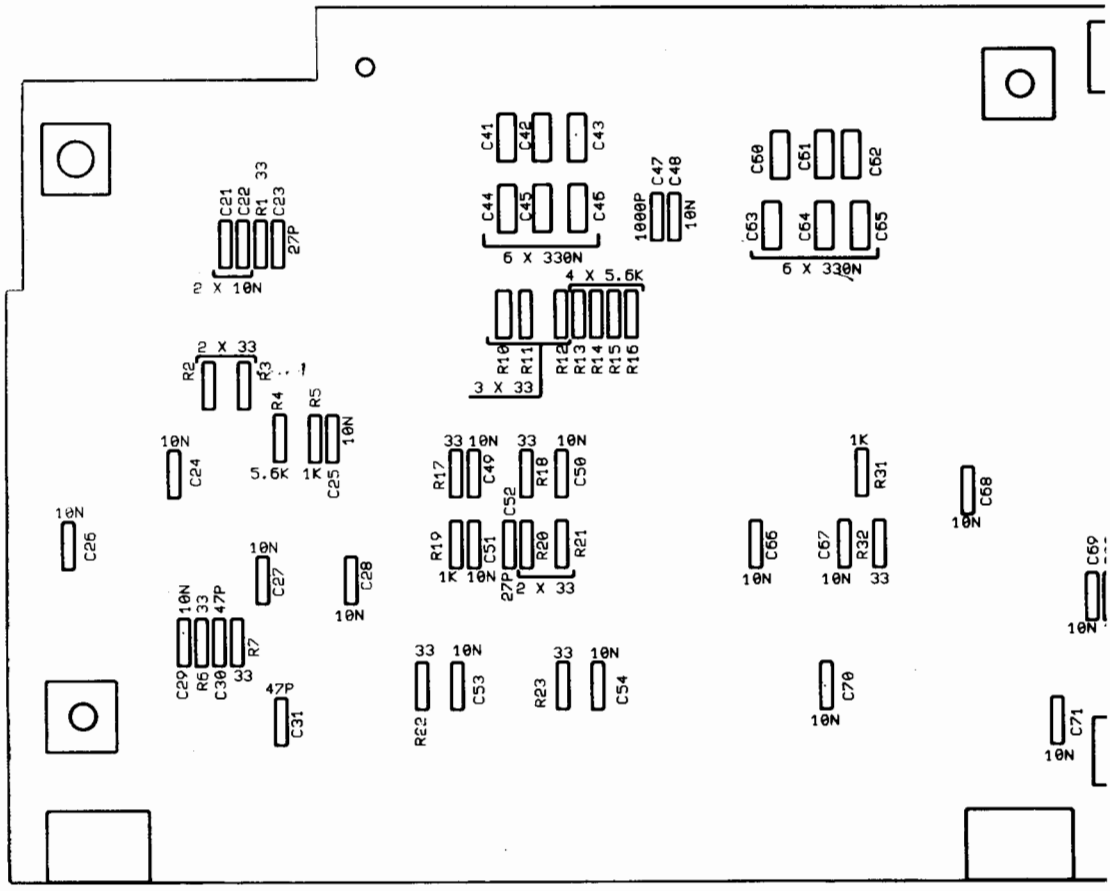


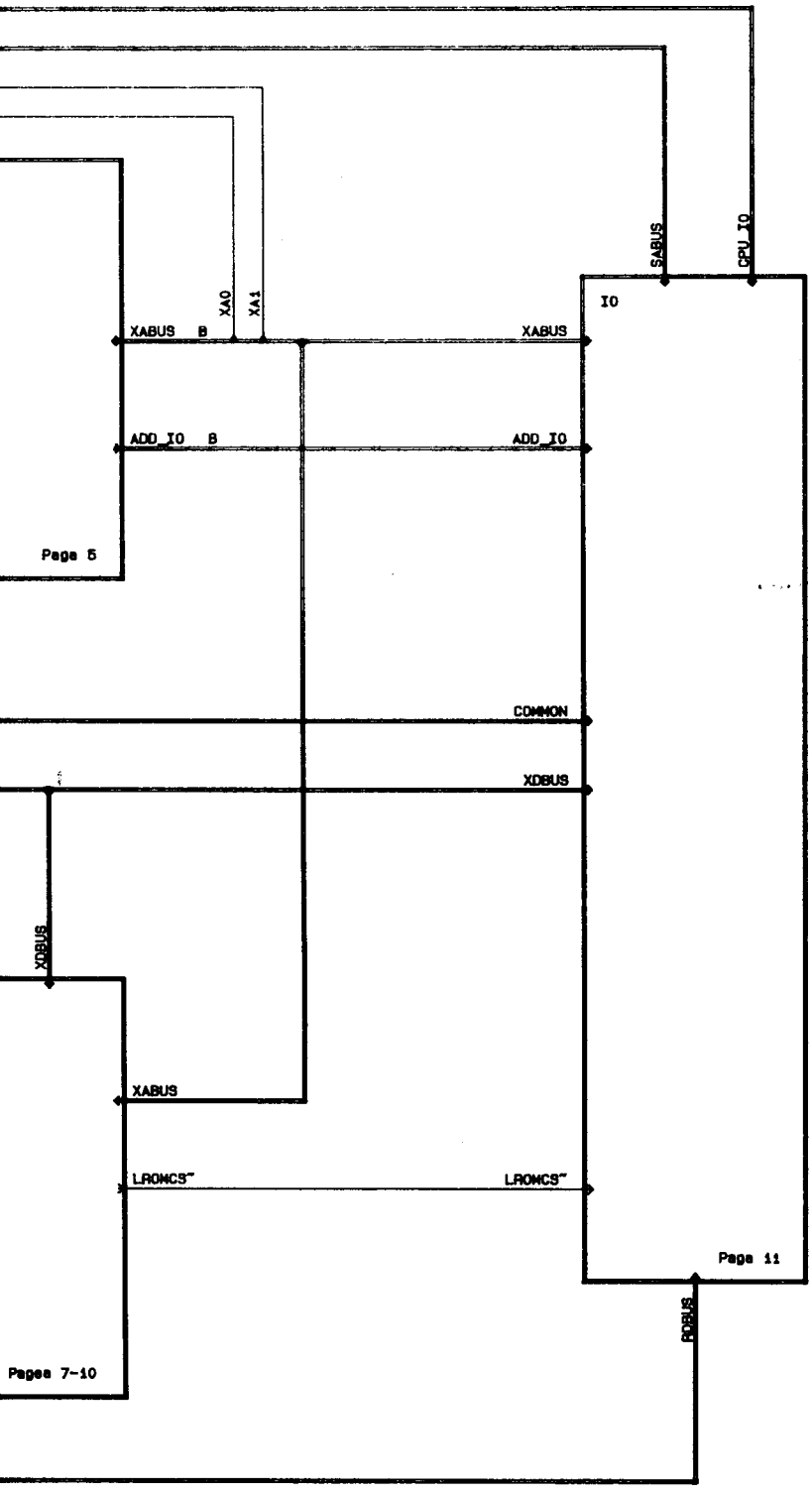
COMPONENT SIDE VIEW

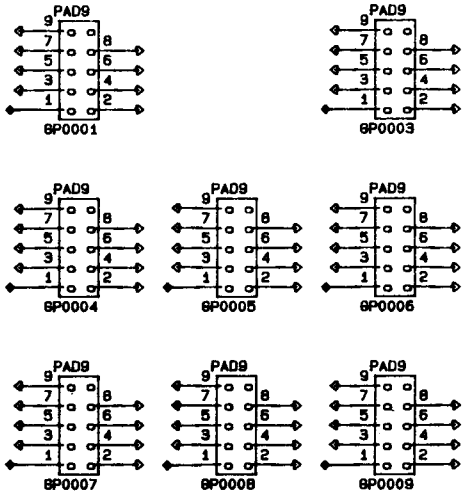
Computer Museum



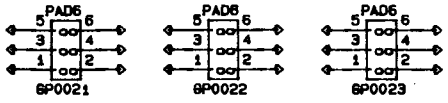
QS/16 QS/20
Processor/Memory PCA
Component Layout
(Solder Side) **SHEET 2 OF 2**


C41
C42
C43
C44
C45
C46
6 X 330N
C47
C48
1000P
10N
C60
C61
C62
C63
C64
C65
6 X 330N
C21
C22
R1
33
C23
27P
2 X 10N
4 X 5.6K
R10
R11
R12
R13
R14
R15
R16
3 X 33
2 X 33
R2
R3
R4
5.6K
R5
1K
10N
C24
C25
10N
10N
C26
10N
C27
C28
10N
10N
33
47P
C29
R6
C30
33
R7
47P
C31
R17
33
10N
C49
R18
33
10N
C50
C52
R19
1K
10N
C51
27P
R20
R21
2 X 33
1K
R31
10N
C66
C67
10N
R32
33
10N
C68
10N
C69
10N
R22
33
10N
C53
R23
33
10N
C54
10N
C70
10N
C71

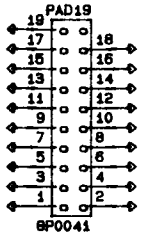




RFI SHIELD FIXATION HOLES



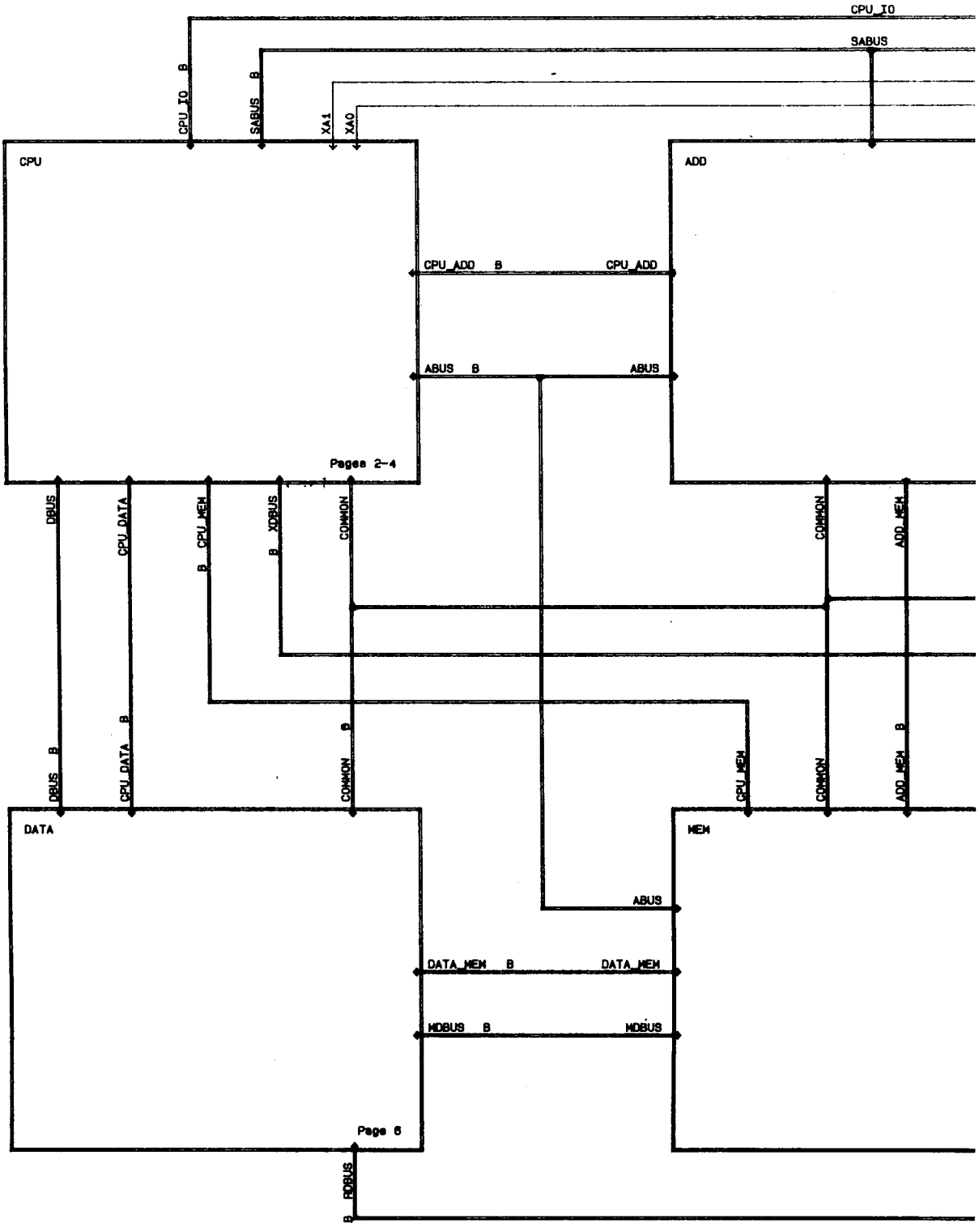
GROUND PADS

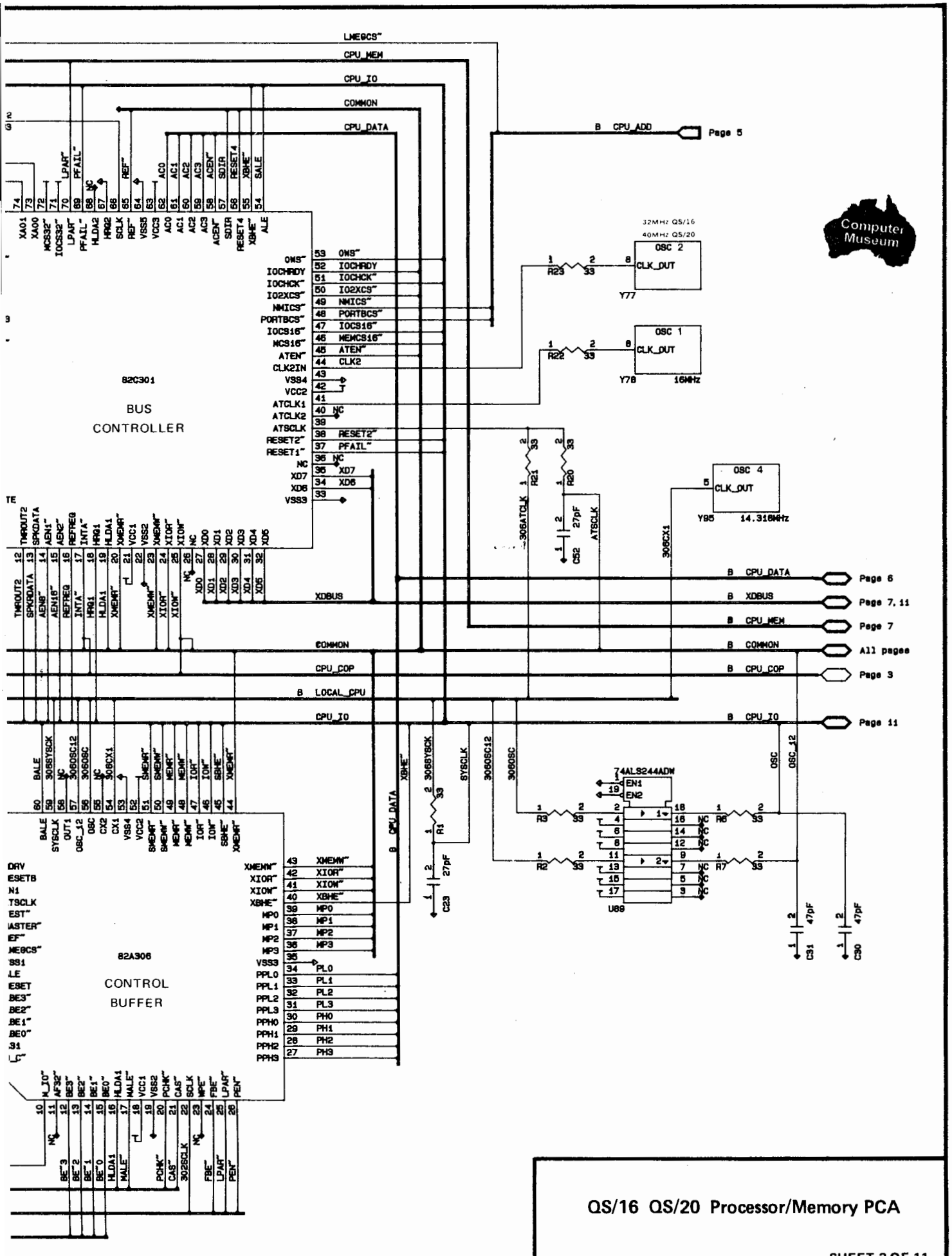


RFI FENCE

QS/16 QS/20 Processor/Memory PCA
Electrical Schematic

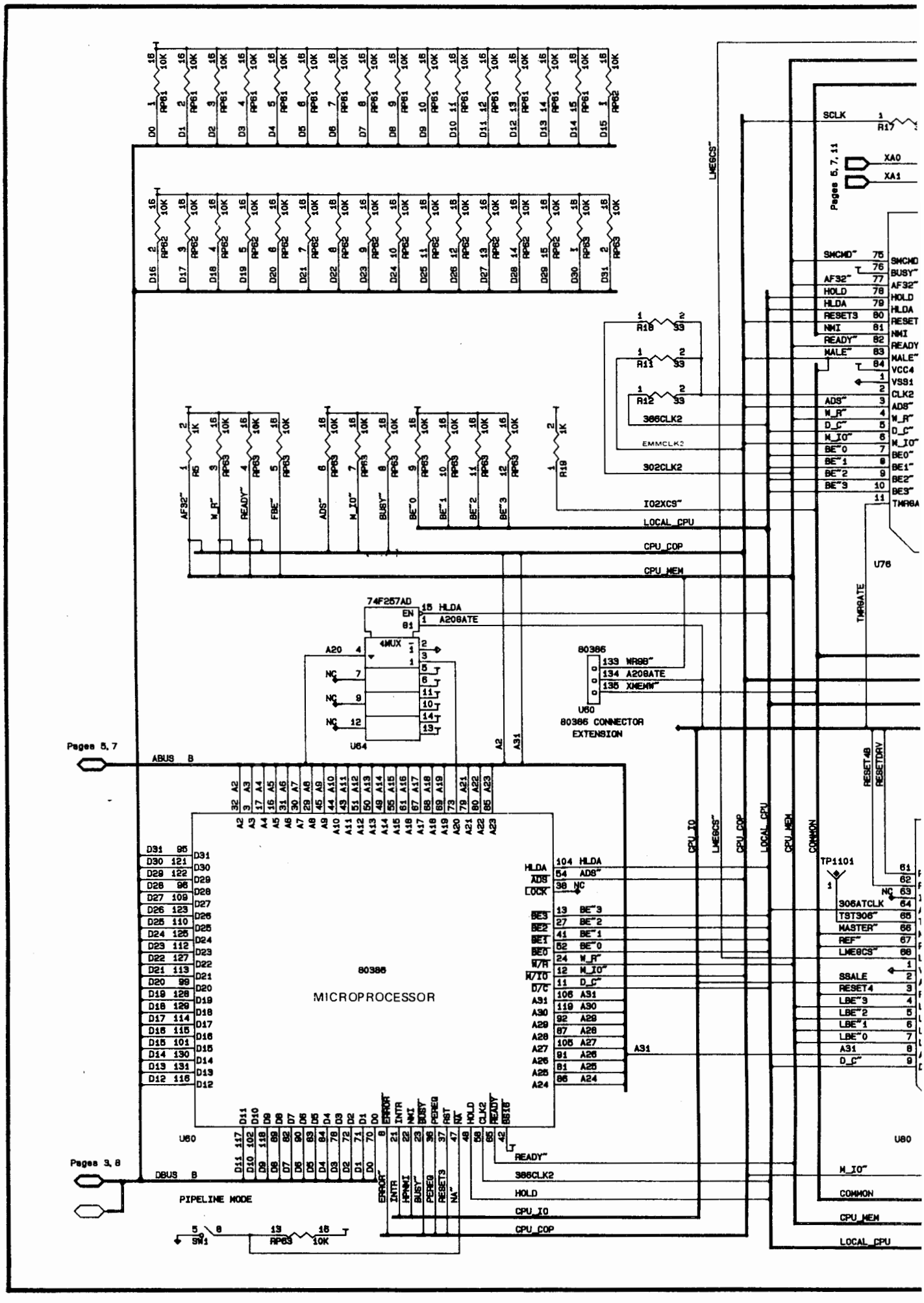
SHEET 1 OF 11

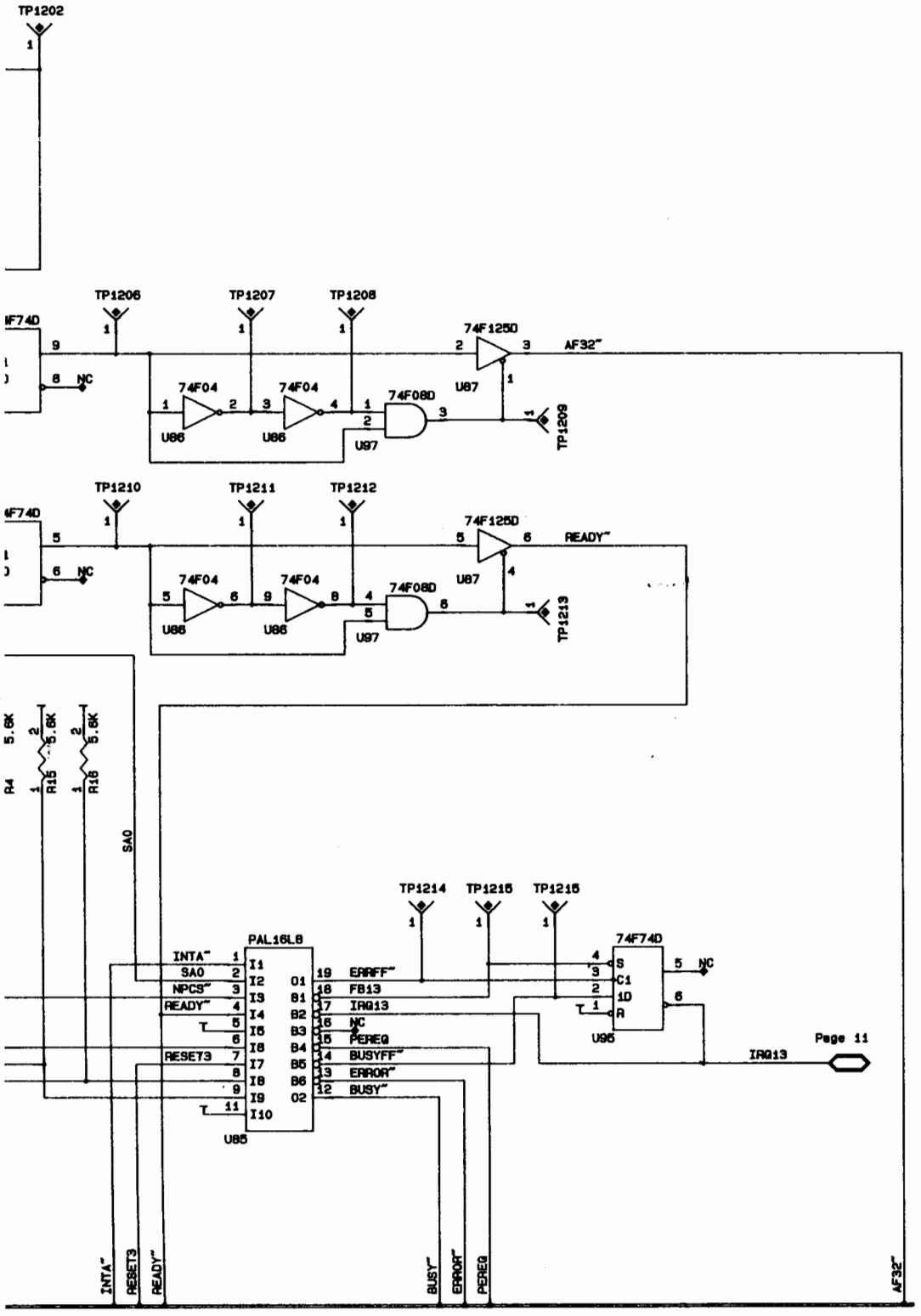

CPU_IO
SABUS
CPU_IO B
SABUS B
XA1
XA0
CPU
ADD
CPU_ADD B
CPU_ADD
ABUS B
ABUS
Pages 2-4
DBUS
CPU_DATA
B CPU_MEM
B XDBUS
COMMON
COMMON
ADD_MEM
DBUS B
CPU_DATA B
COMMON B
CPU_MEM
COMMON
ADD_MEM B
DATA
MEM
ABUS
DATA_MEM B
DATA_MEM
MDBUS B
MDBUS
Page 6
B RDBUS

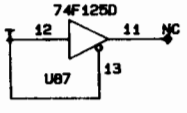


QS/16 QS/20 Processor/Memory PCA

SHEET 2 OF 11

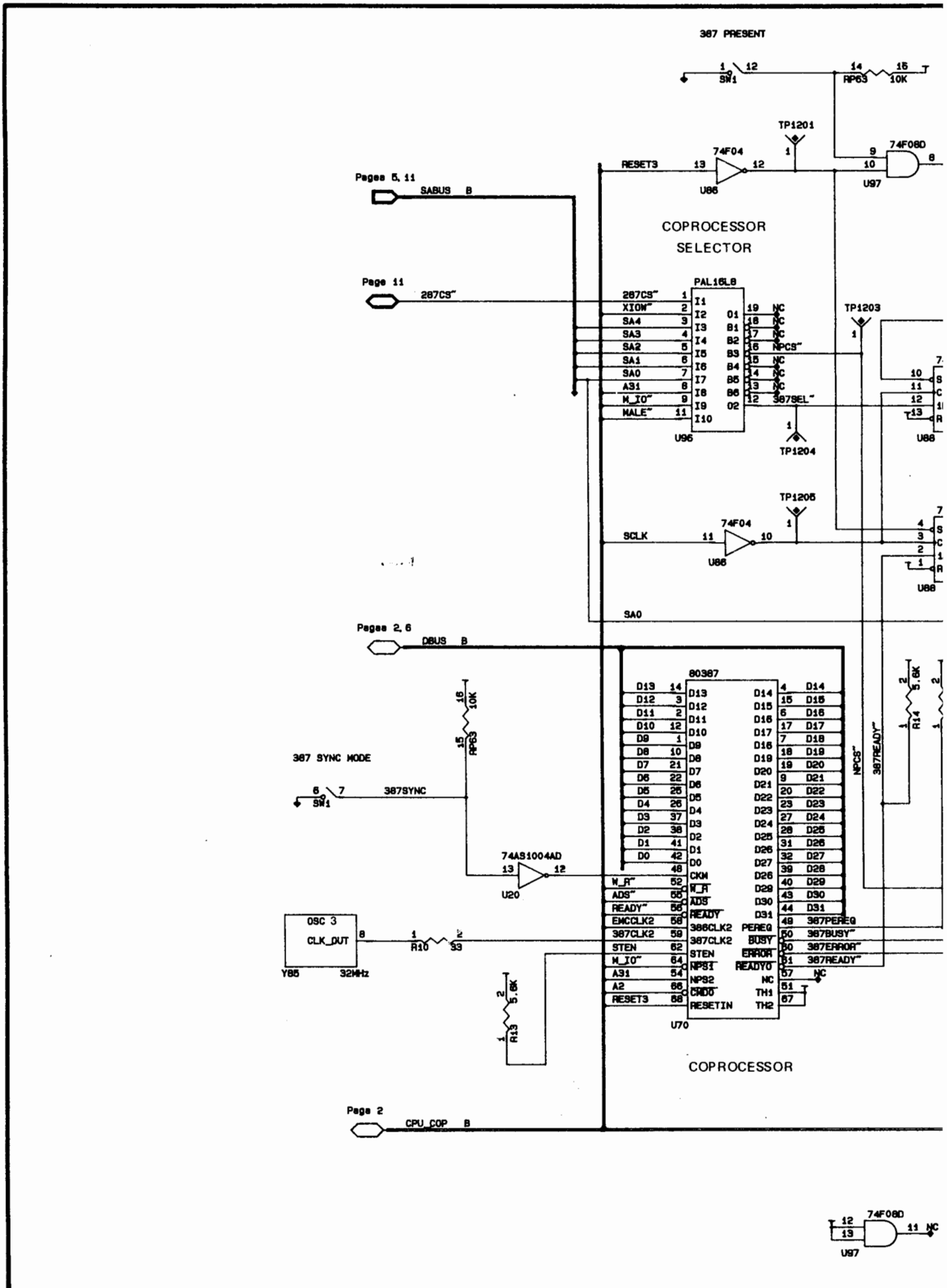

80386
MICROPROCESSOR
PIPELINE MODE
80386 CONNECTOR EXTENSION
74F257AD
4MUX
U60
U64
U76
U80
ABUS B
DBUS B
Pages 5, 7
Pages 3, 8
Pages 5, 7, 11
SCLK
XA0
XA1
LME8CS"
386CLK2
EMMCLK2
302CLK2
IO2XCS"
LOCAL_CPU
CPU_COP
CPU_MEM
COMMON
HLDA
A20GATE
XMEMW"
WR8B"
TMR8A
TMR8GATE
RESET4B
RESETDRV
TP1101
306ATCLK
TST306"
MASTER"
REF"
SSALE
RESET4
LBE"3
LBE"2
LBE"1
LBE"0
A31
D_C"
M_IO"
READY"
HOLD
SW1

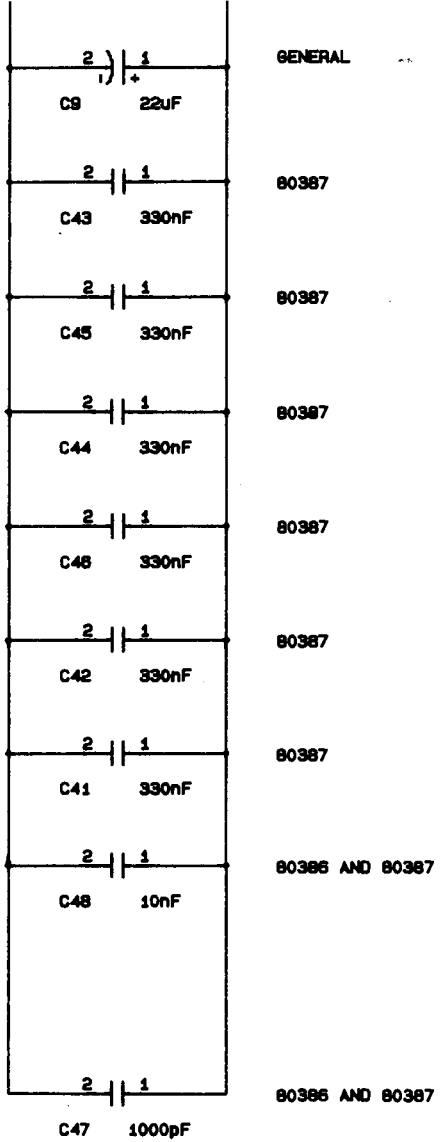


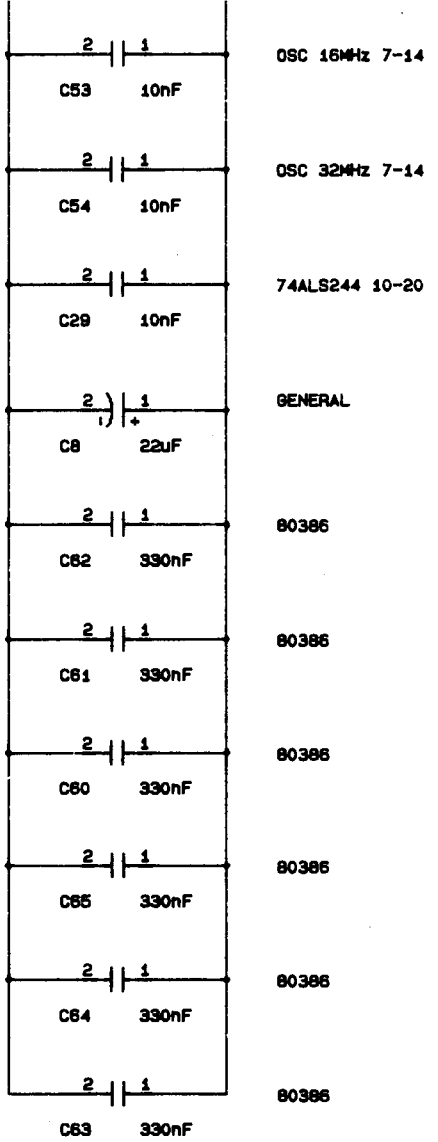


QS/16 QS/20 Processor/Memory PCA

SHEET 3 OF 11


387 PRESENT
SW1
RP63
10K
TP1201
74F04
74F08D
RESET3
U86
U97
Pages 5, 11
SABUS B
COPROCESSOR
SELECTOR
Page 11
287CS"
PAL16L8
XIOW"
SA4
SA3
SA2
SA1
SA0
A31
M_IO"
MALE"
NPCS"
387SEL"
U96
TP1203
TP1204
U88
TP1205
SCLK
SA0
Pages 2, 6
DBUS B
80387
387 SYNC MODE
387SYNC
74AS1004AD
U20
OSC 3
CLK_OUT
Y85
32MHz
R10
33
R13
5.6K
R14
W_R"
ADS"
READY"
EMCCLK2
387CLK2
STEN
RESET3
RESETIN
NPS1
NPS2
CMD0
READY0
PEREQ
BUSY"
ERROR"
387READY"
387PEREQ
387BUSY"
387ERROR"
U70
COPROCESSOR
Page 2
CPU_COP B

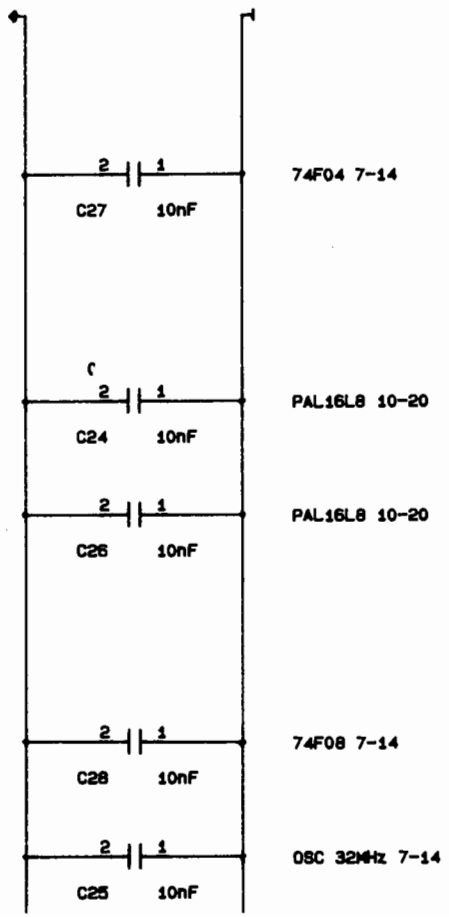




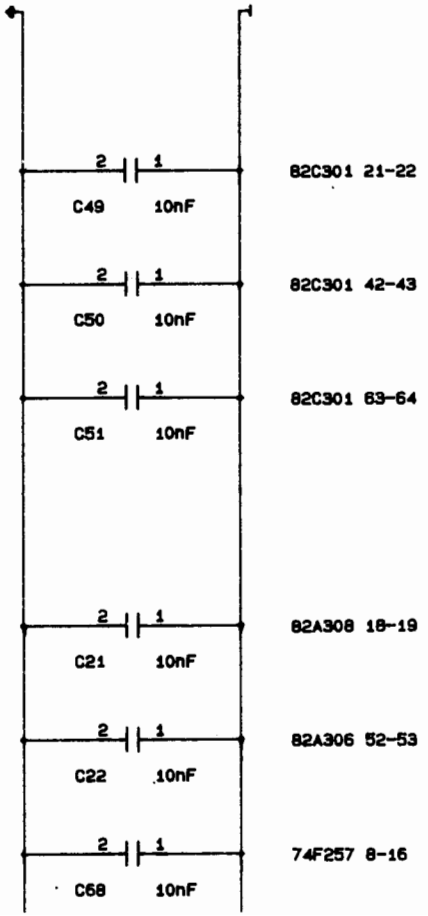
QS/16 QS/20 Processor/Memory PCA

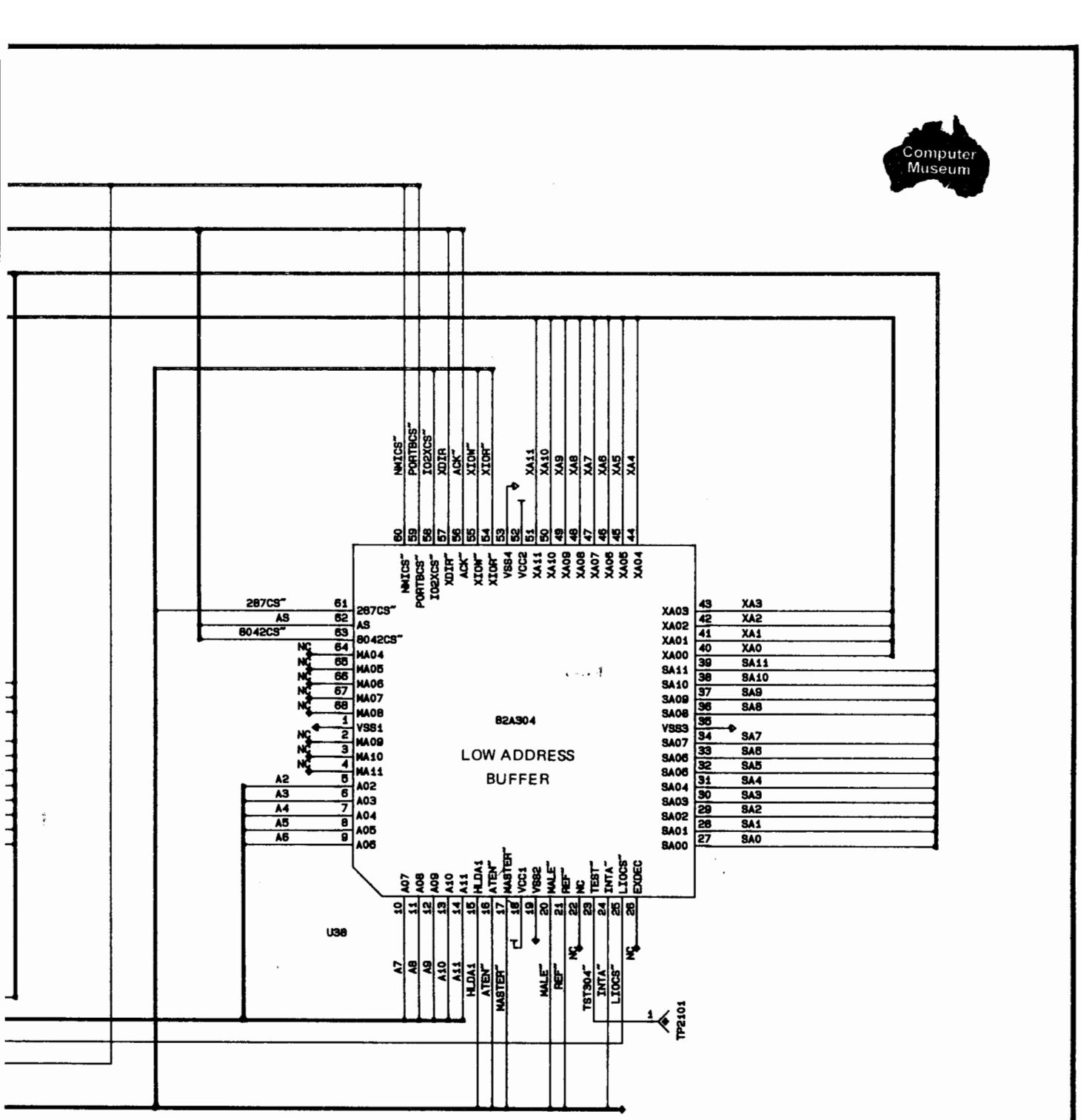
SHEET 4 OF 11

Page 3


2
1
C27
10nF
74F04 7-14
2
1
C24
10nF
PAL16L8 10-20
2
1
C26
10nF
PAL16L8 10-20
2
1
C28
10nF
74F08 7-14
2
1
C25
10nF
OSC 32MHz 7-14

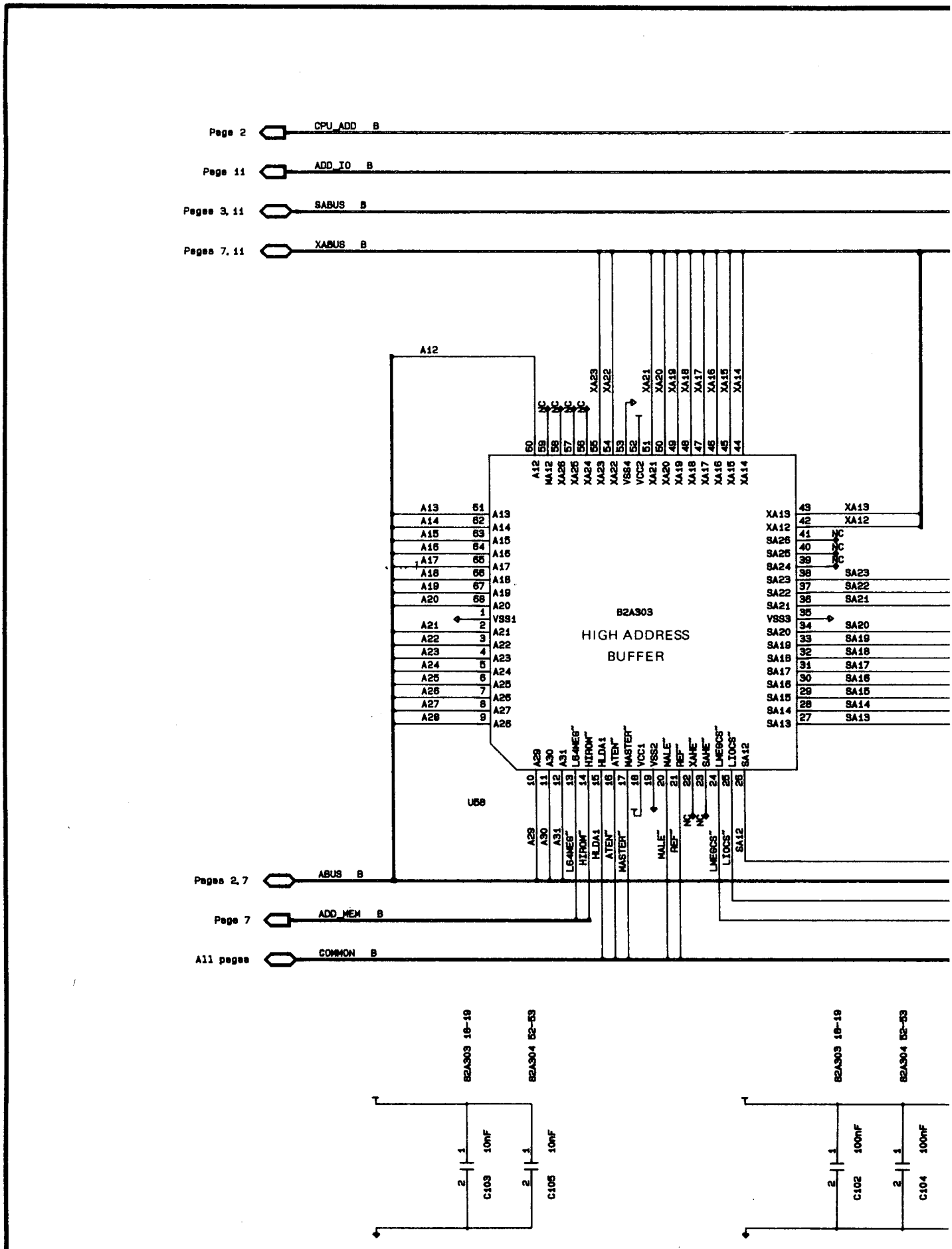
Page 2

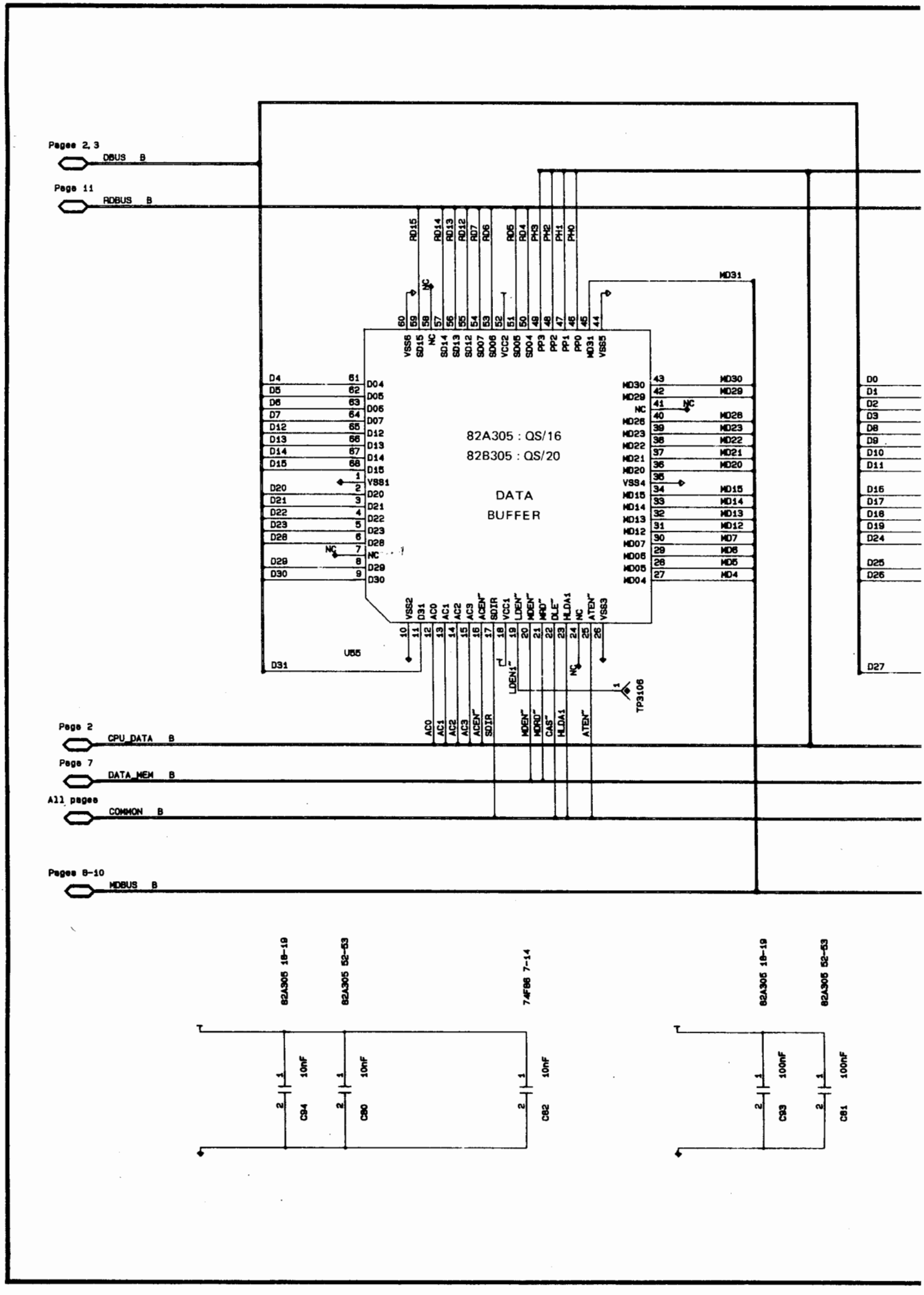

2
1
C49
10nF
82C301 21-22
2
1
C50
10nF
82C301 42-43
2
1
C51
10nF
82C301 63-64
2
1
C21
10nF
82A308 18-19
2
1
C22
10nF
82A306 52-53
2
1
C68
10nF
74F257 8-16

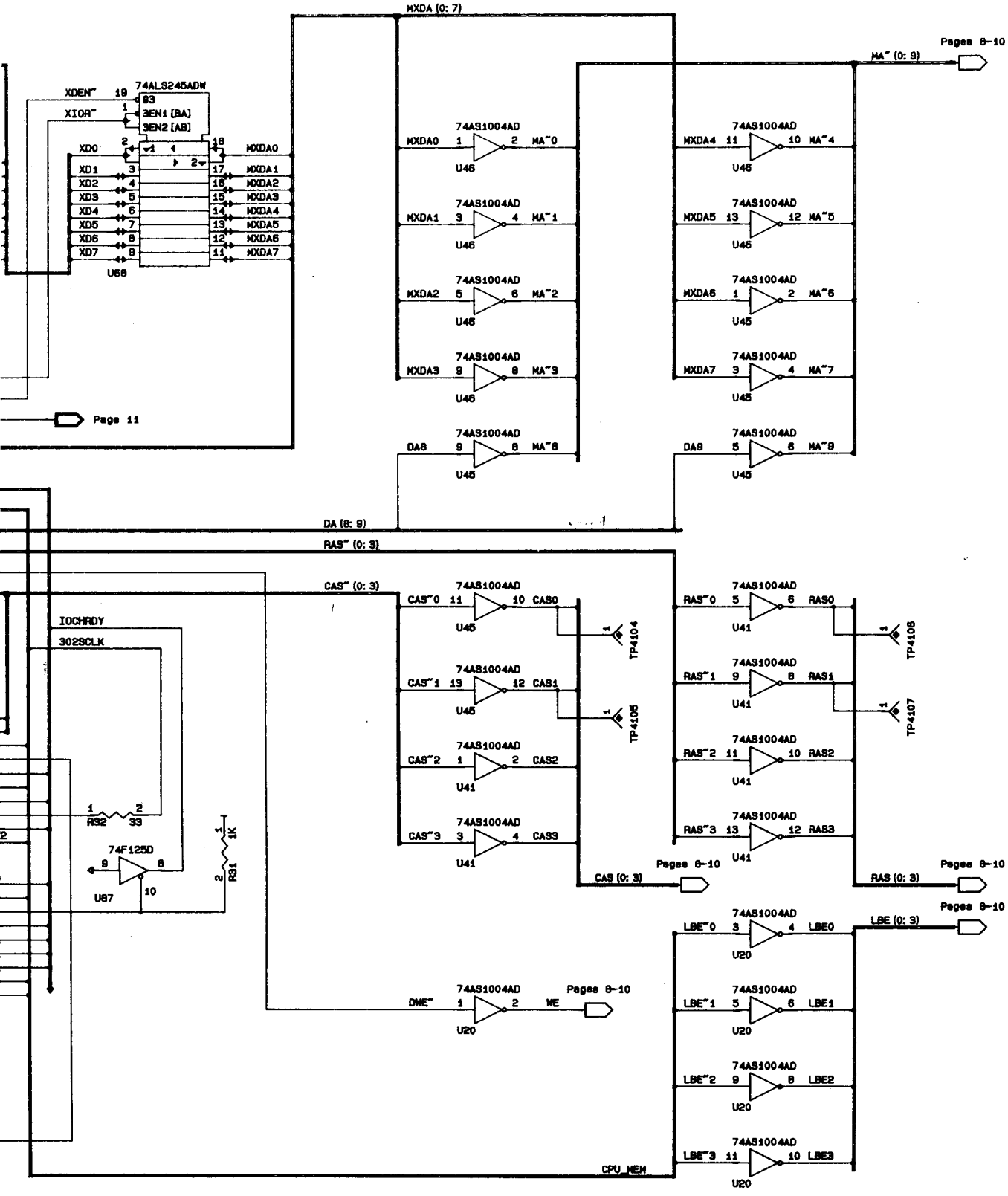


QS/16 QS/20 Processor/Memory PCA

SHEET 5 OF 11

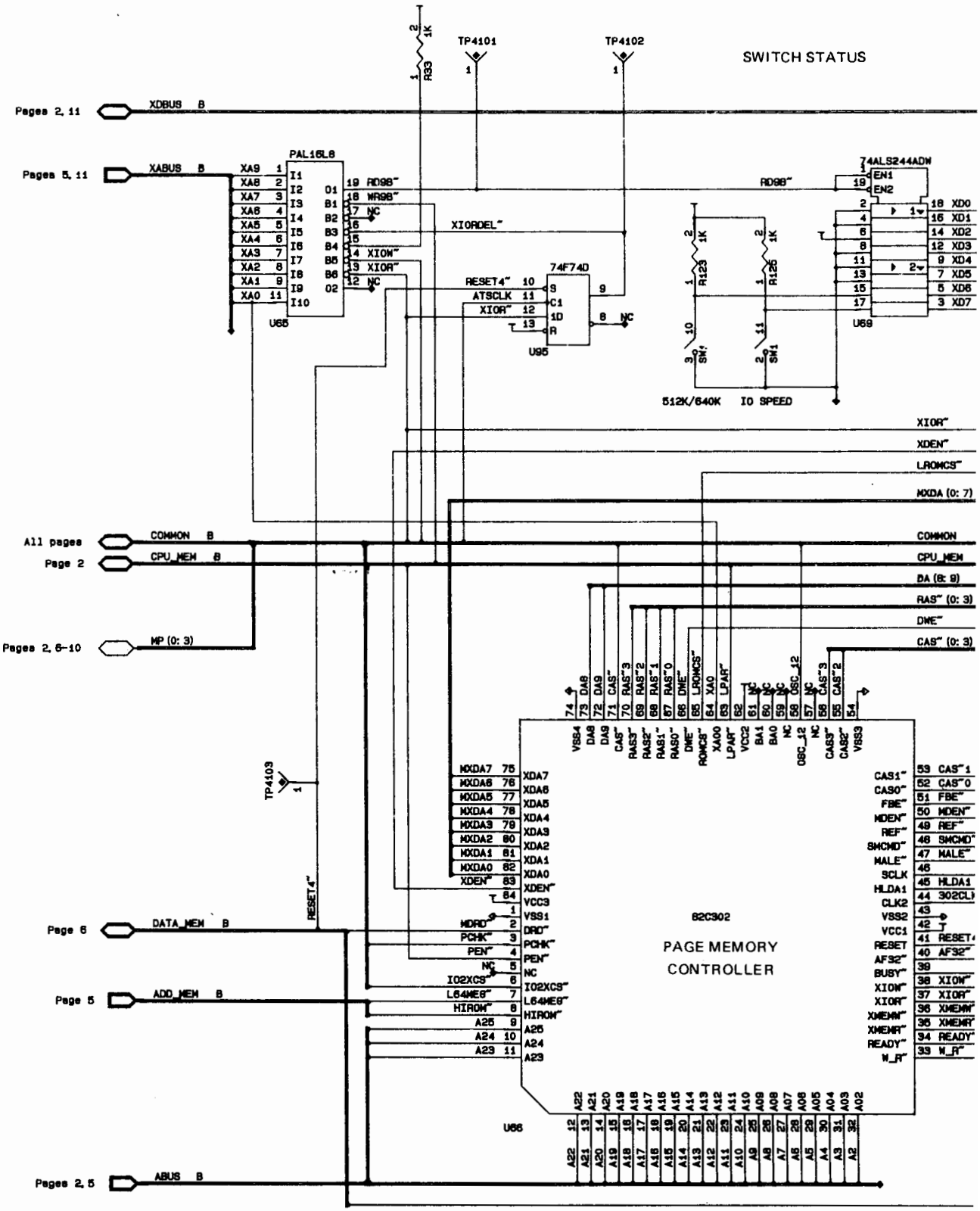

Page 2
CPU_ADD B
Page 11
ADD_IO B
Pages 3, 11
SABUS B
Pages 7, 11
XABUS B
B2A303
HIGH ADDRESS
BUFFER
U58
Pages 2, 7
ABUS B
Page 7
ADD_MEM B
All pages
COMMON B
B2A303 18-19
B2A304 52-53
C103 10nF
C105 10nF
C102 100nF
C104 100nF

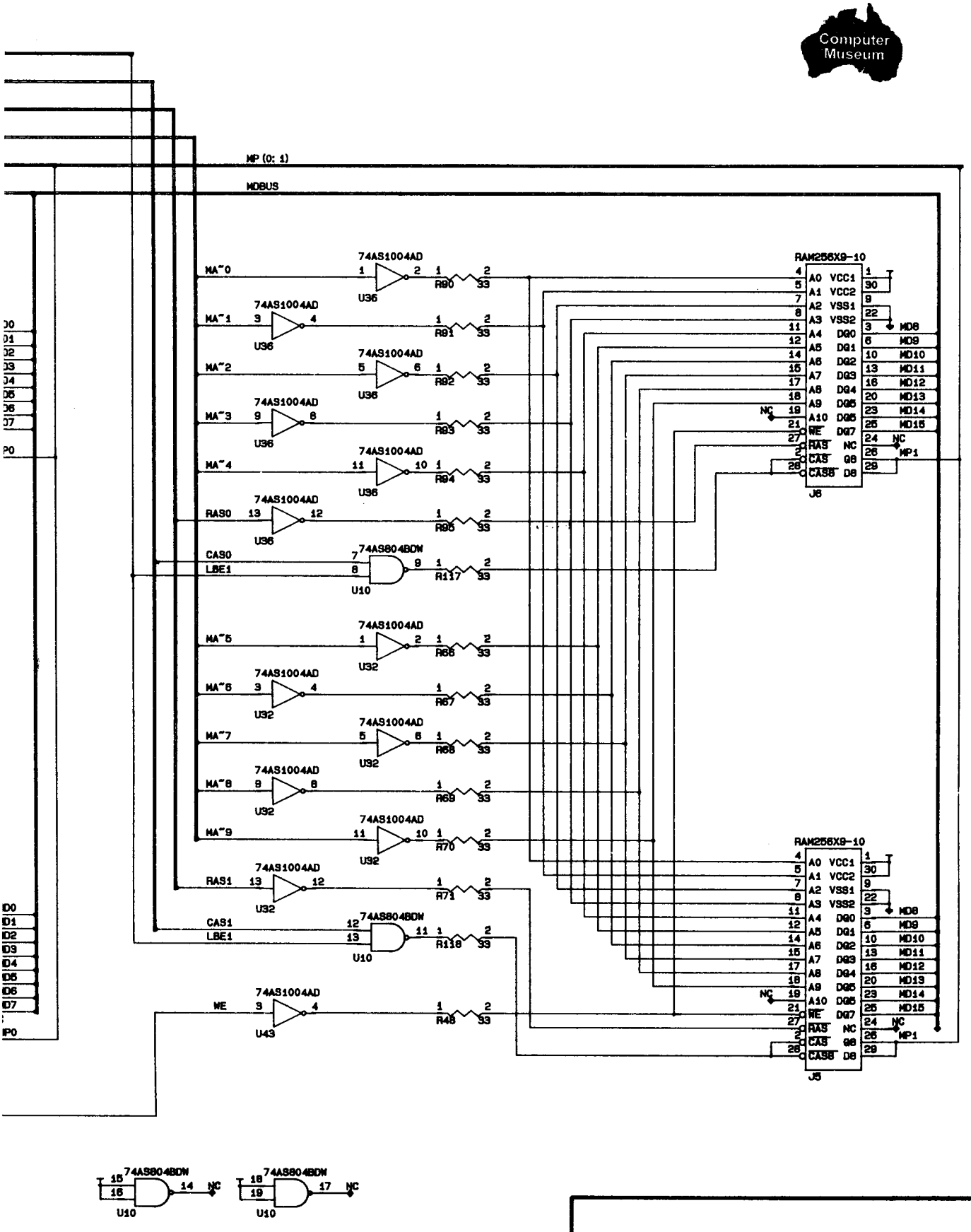

Pages 2, 3
DBUS B
Page 11
RDBUS B
82A305 : QS/16
82B305 : QS/20
DATA
BUFFER
U55
TP3106
Page 2
CPU_DATA B
Page 7
DATA_MEM B
All pages
COMMON B
Pages 8-10
MDBUS B
82A305 18-19
82A305 52-53
74F86 7-14
C84 10nF
C80 10nF
C82 10nF
82A305 18-19
82A305 52-53
C83 100nF
C81 100nF



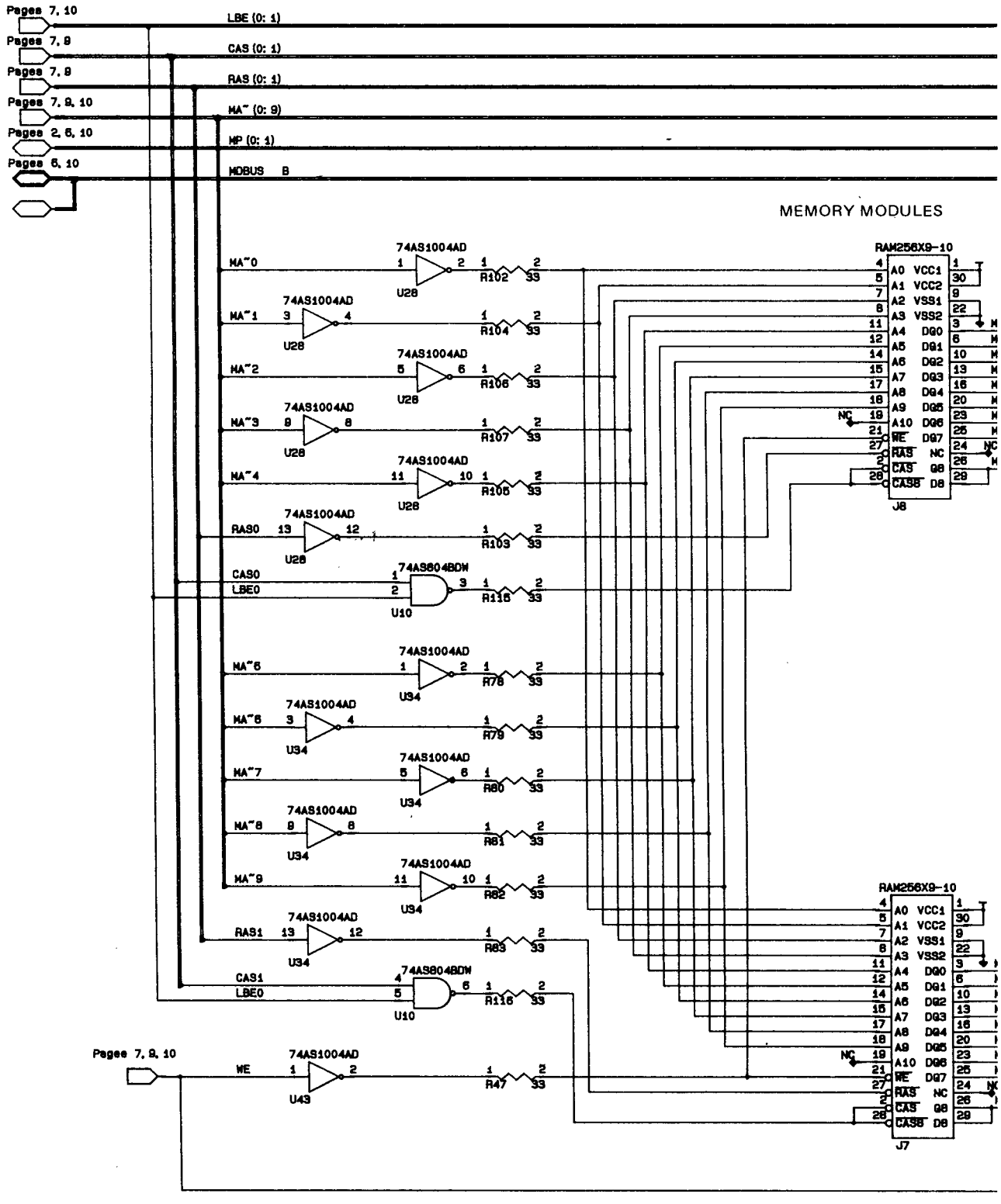
QS/16 QS/20 Processor/Memory PCA

SHEET 7 OF 11

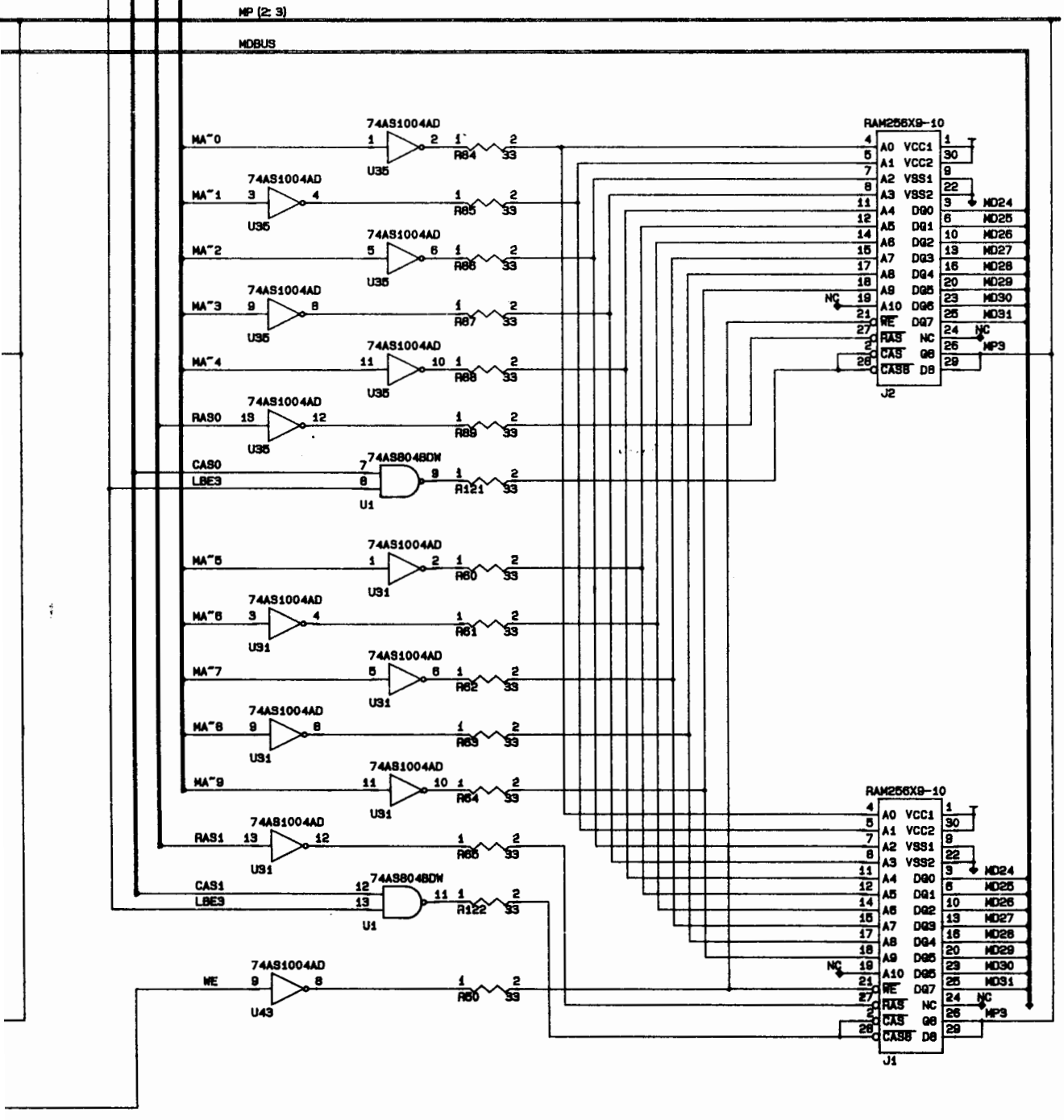

SWITCH STATUS
TP4101
TP4102
R33 1K
Pages 2, 11
XDBUS B
Pages 5, 11
XABUS B
PAL16L8
U65
RD98"
WR98"
XIOW"
XIOR"
XIORDEL"
74F74D
U95
RESET4"
ATSCLK
74ALS244ADW
U69
R123 1K
R125 1K
SW1
512K/640K IO SPEED
XIOR"
XDEN"
LROMCS"
MXDA (0: 7)
All pages
COMMON B
Page 2
CPU_MEM B
BA (8: 9)
RAS" (0: 3)
DWE"
CAS" (0: 3)
Pages 2, 6-10
MP (0: 3)
TP4103
Page 6
DATA_MEM B
Page 5
ADD_MEM B
82C302
PAGE MEMORY
CONTROLLER
U66
Pages 2, 5
ABUS B

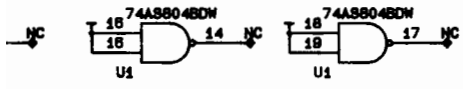


QS/16 QS/20 Processor/Memory PCA

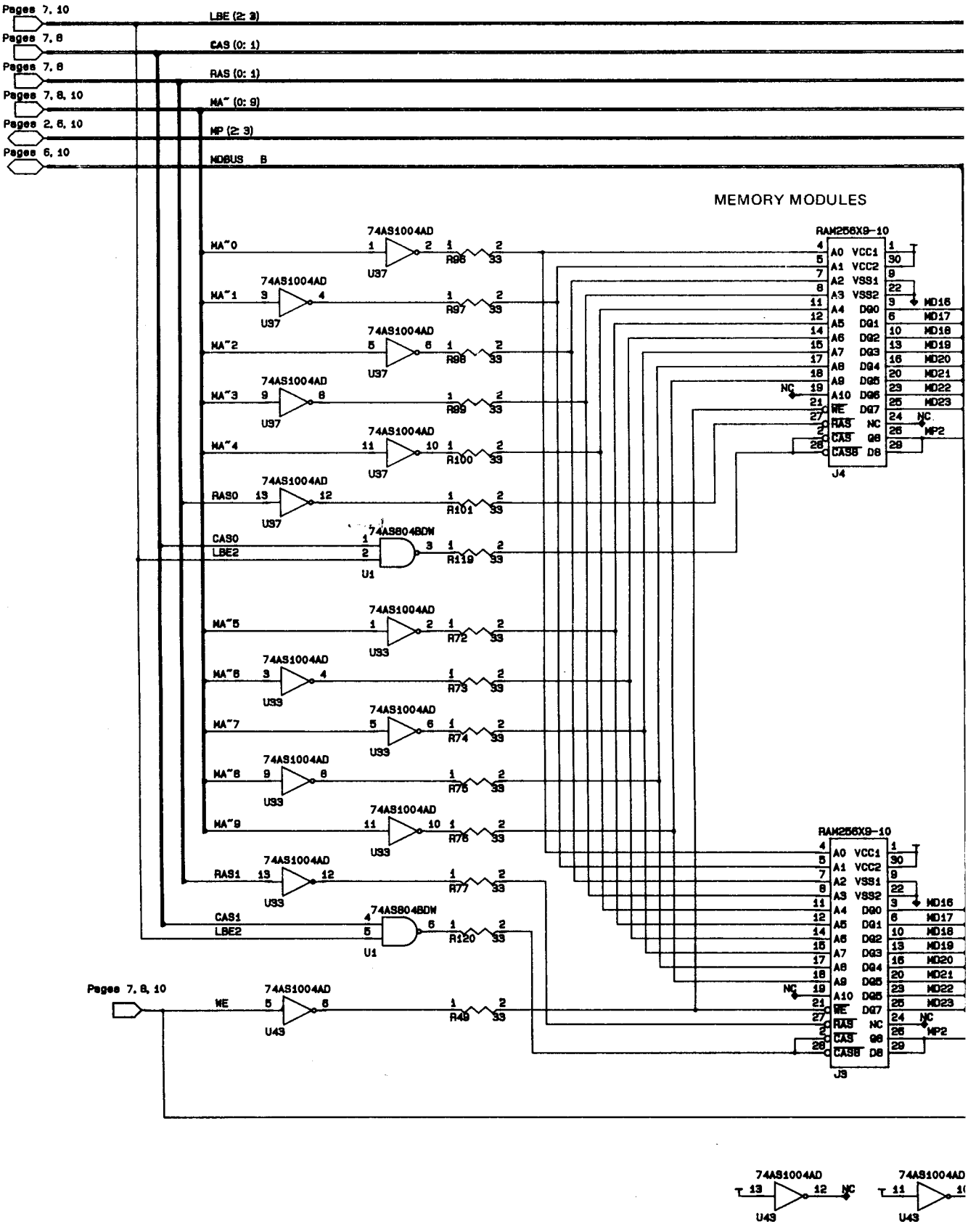

MEMORY MODULES
Pages 7, 10
Pages 7, 9
Pages 7, 9
Pages 7, 9, 10
Pages 2, 6, 10
Pages 6, 10
LBE (0: 1)
CAS (0: 1)
RAS (0: 1)
MA~ (0: 9)
MP (0: 1)
MDBUS B
74AS1004AD
74AS804BDW
RAM256X9-10
MA~0
MA~1
MA~2
MA~3
MA~4
RAS0
CAS0
LBE0
MA~5
MA~6
MA~7
MA~8
MA~9
RAS1
CAS1
WE
R102
R104
R106
R107
R105
R103
R116
R78
R79
R80
R81
R82
R83
R47
U28
U10
U34
U43
J8
J7
Pages 7, 9, 10

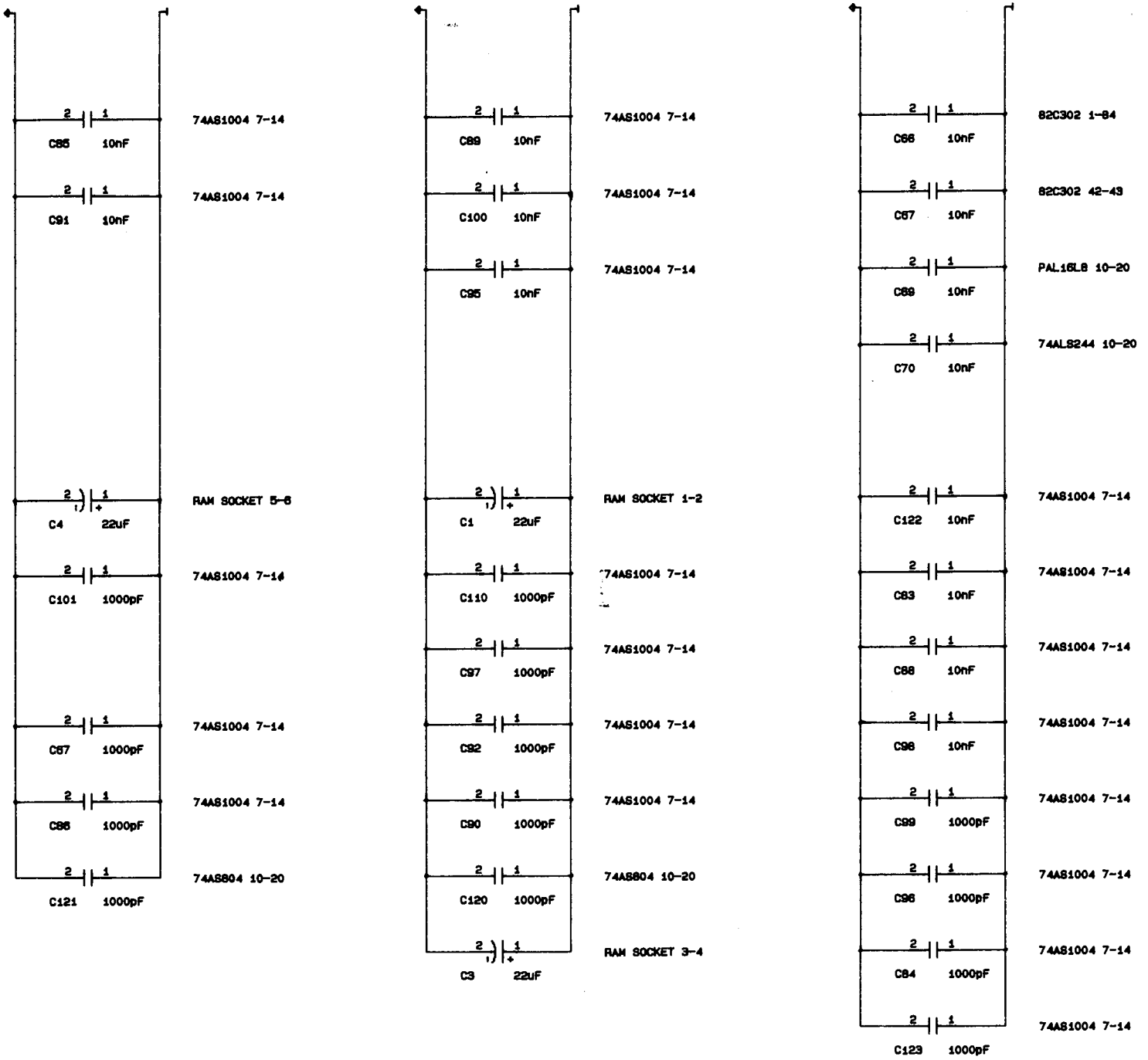
Computer Museum





QS/16 QS/20 Processor/Memory PCA

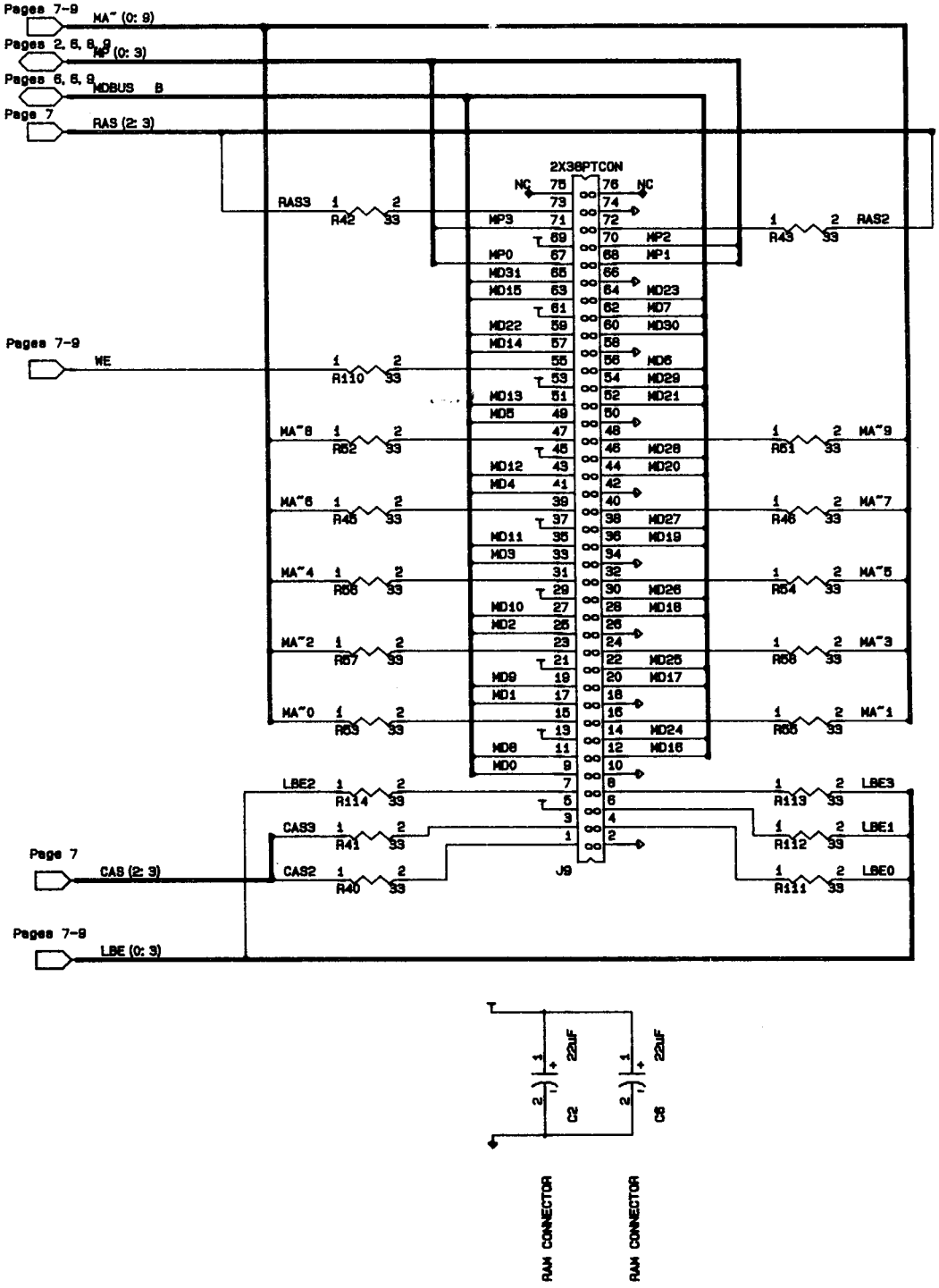

Pages 7, 10
LBE (2: 3)
Pages 7, 8
CAS (0: 1)
Pages 7, 8
RAS (0: 1)
Pages 7, 8, 10
MA~ (0: 9)
Pages 2, 6, 10
MP (2: 3)
Pages 6, 10
MDBUS B
MEMORY MODULES
74AS1004AD
74AS804BDW
RAM256X9-10
MA~0
MA~1
MA~2
MA~3
MA~4
MA~5
MA~6
MA~7
MA~8
MA~9
RAS0
RAS1
CAS0
CAS1
LBE2
WE
R96
R97
R98
R99
R100
R101
R119
R72
R73
R74
R75
R76
R77
R120
R49
U37
U33
U1
U43
J4
J5
MD16
MD17
MD18
MD19
MD20
MD21
MD22
MD23
MP2
Pages 7, 8, 10

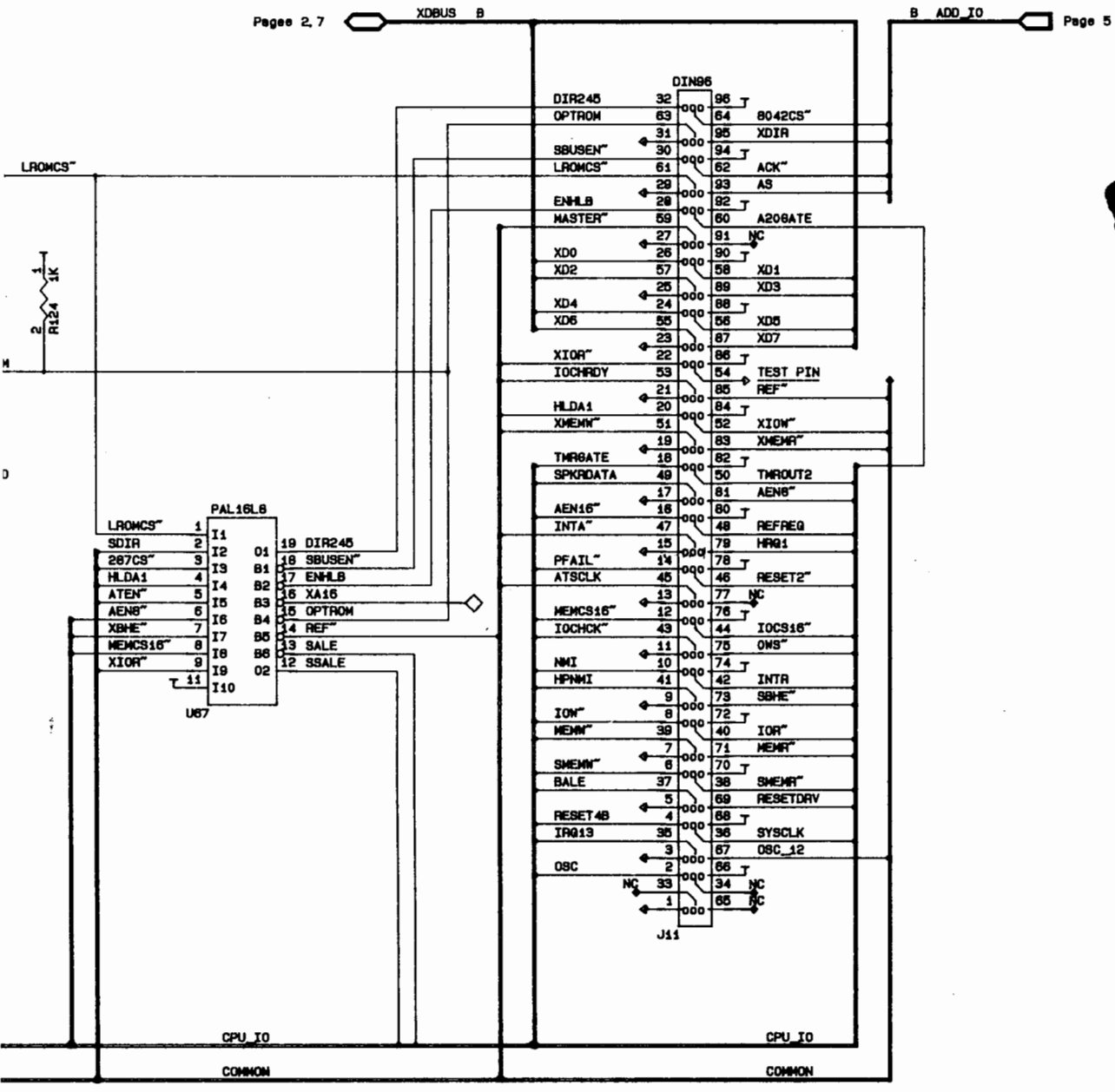


QS/16, QS/20 Processor/Memory PCA

SHEET 10 OF 11

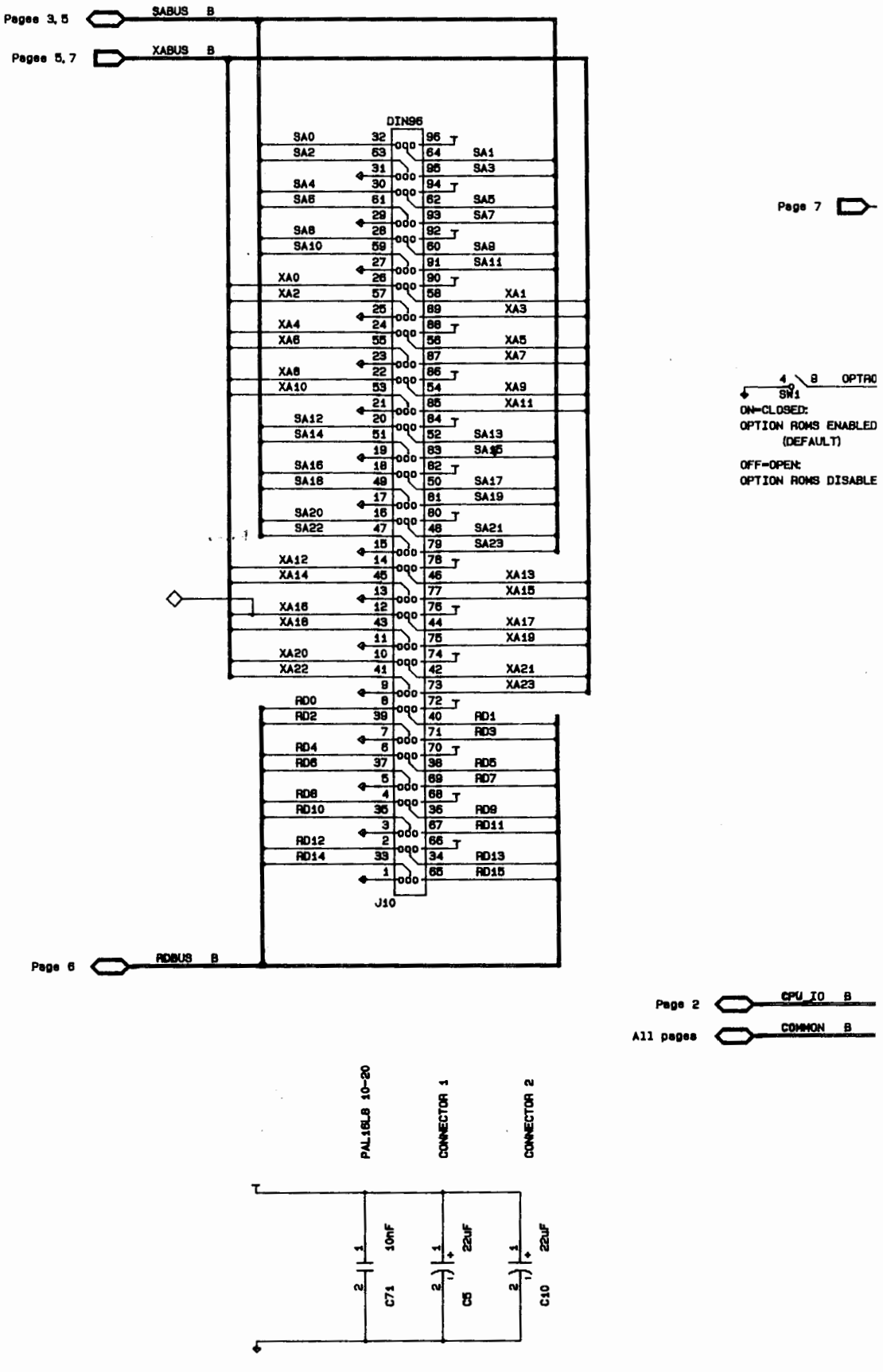
MEMORY EXTENSION
CONNECTOR

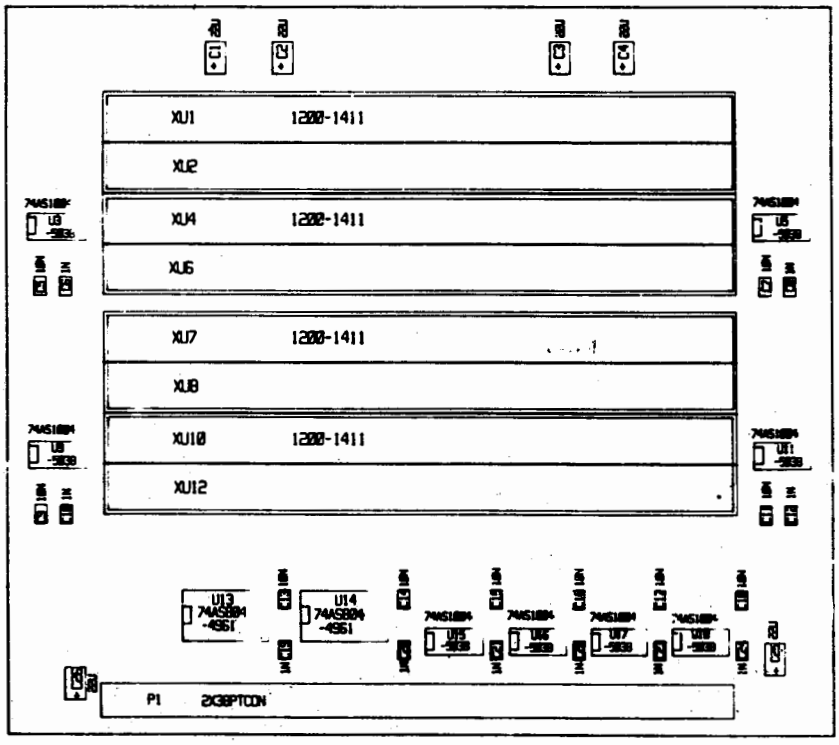




Computer Museum

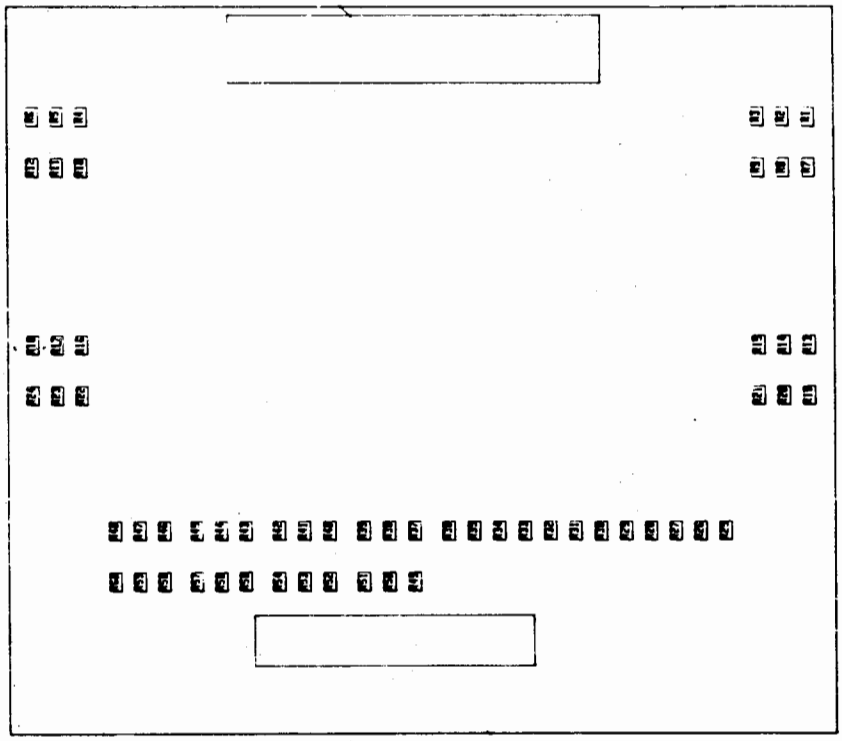
QS/16 QS/20 Processor/Memory PCA


Pages 3, 5
SABUS B
Pages 5, 7
XABUS B
DIN96
SA0 32 96
SA2 63 64 SA1
31 95 SA3
SA4 30 94
SA6 61 62 SA5
29 93 SA7
SA8 28 92
SA10 59 60 SA9
27 91 SA11
XA0 26 90
XA2 57 58 XA1
25 89 XA3
XA4 24 88
XA6 55 56 XA5
23 87 XA7
XA8 22 86
XA10 53 54 XA9
21 85 XA11
SA12 20 84
SA14 51 52 SA13
19 83 SA15
SA16 18 82
SA18 49 50 SA17
17 81 SA19
SA20 16 80
SA22 47 48 SA21
15 79 SA23
XA12 14 78
XA14 45 46 XA13
13 77 XA15
XA16 12 76
XA18 43 44 XA17
11 75 XA19
XA20 10 74
XA22 41 42 XA21
9 73 XA23
RD0 8 72
RD2 39 40 RD1
7 71 RD3
RD4 6 70
RD6 37 38 RD5
5 69 RD7
RD8 4 68
RD10 35 36 RD9
3 67 RD11
RD12 2 66
RD14 33 34 RD13
1 65 RD15
J10
Page 6
RDBUS B
Page 7
4 8 OPTR0
SW1
ON=CLOSED:
OPTION ROMS ENABLED
(DEFAULT)
OFF=OPEN:
OPTION ROMS DISABLE
Page 2
CPU_IO B
All pages
COMMON B
PAL16L8 10-20
CONNECTOR 1
CONNECTOR 2
1
2
10nF
C71
22uF
C5
22uF
C10

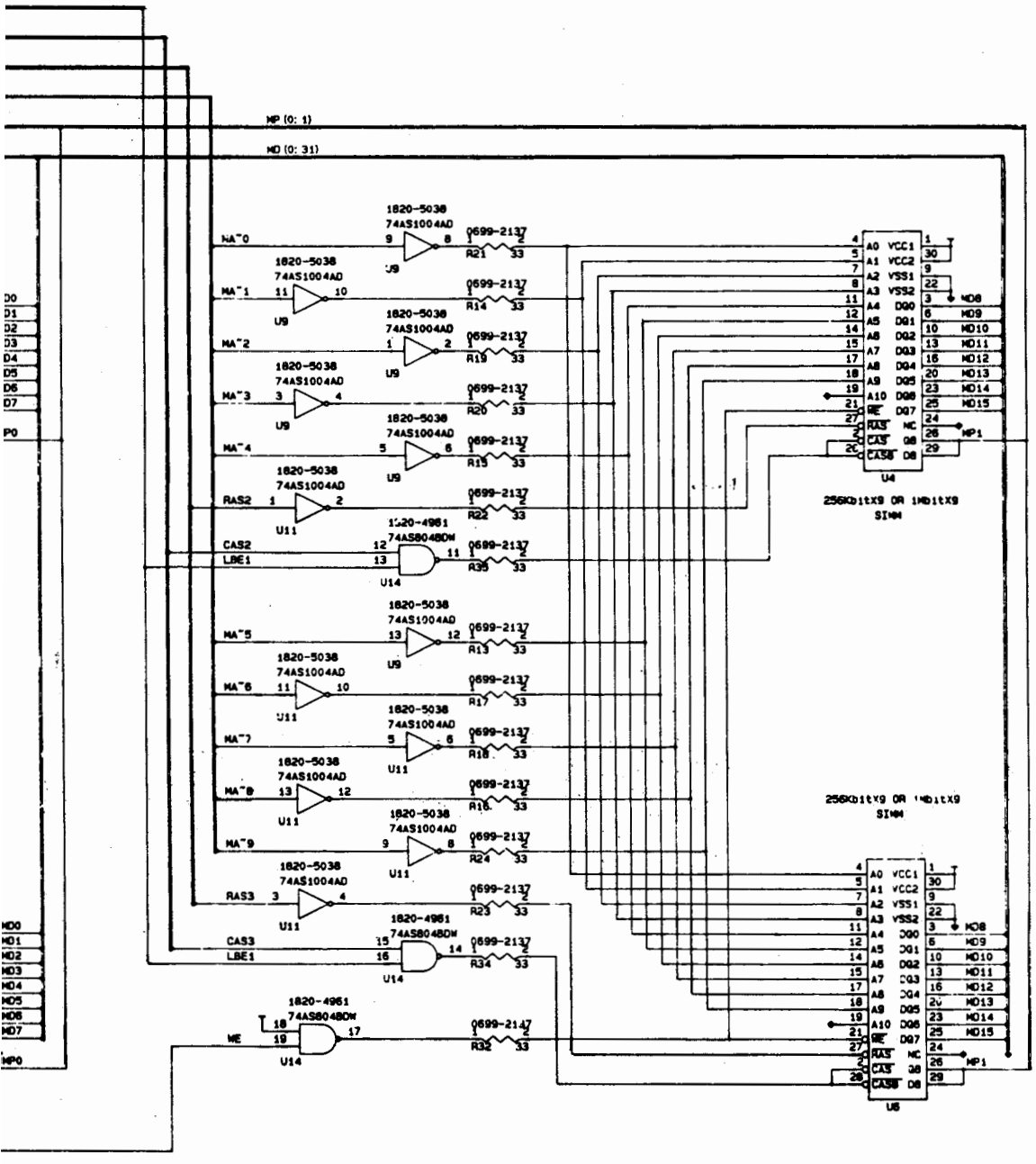


COMPONENT SIDE

QS/16 QS/20 Memory Extension PCA
Component Layout

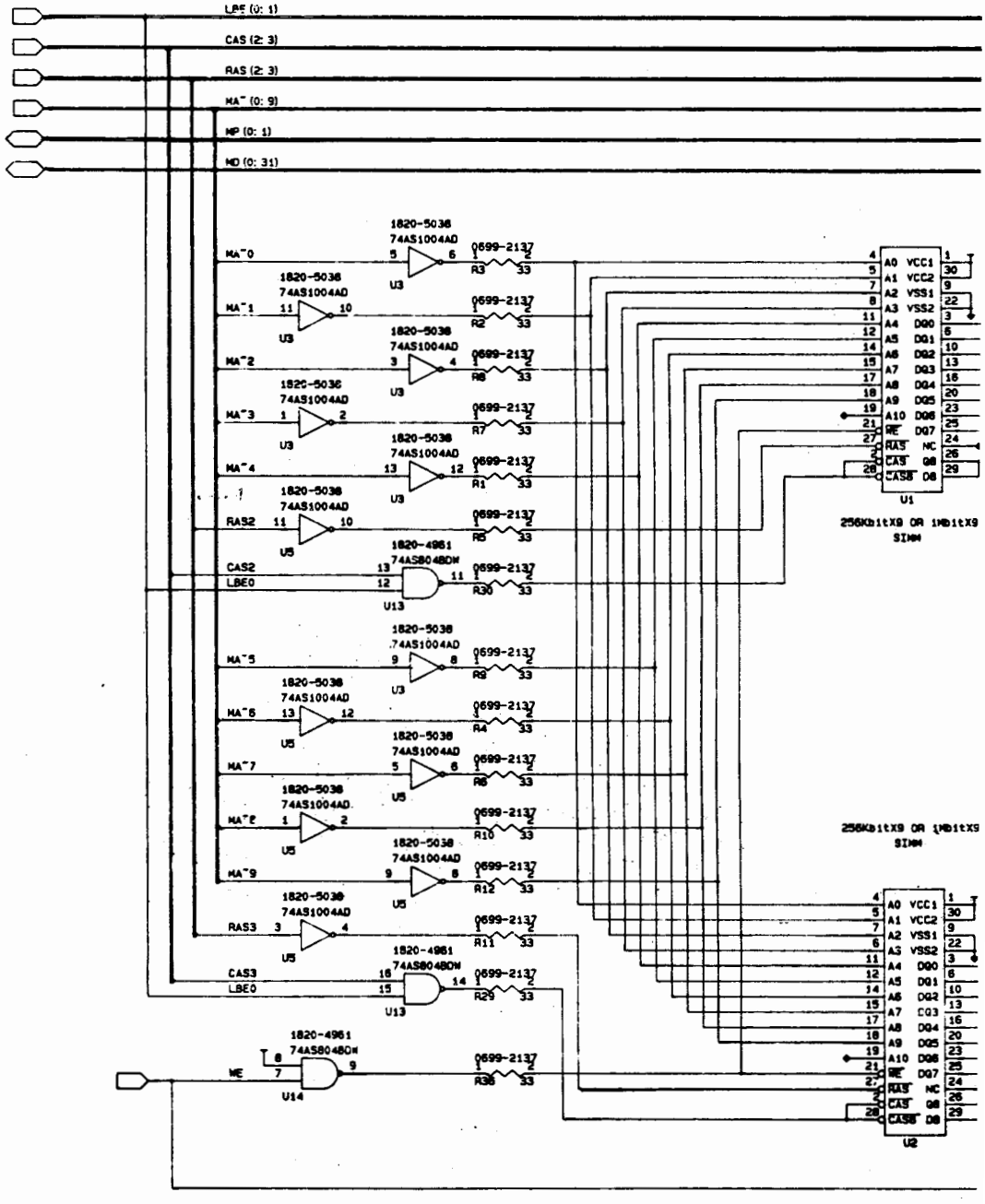


VIEWED FROM SOLDER SIDE

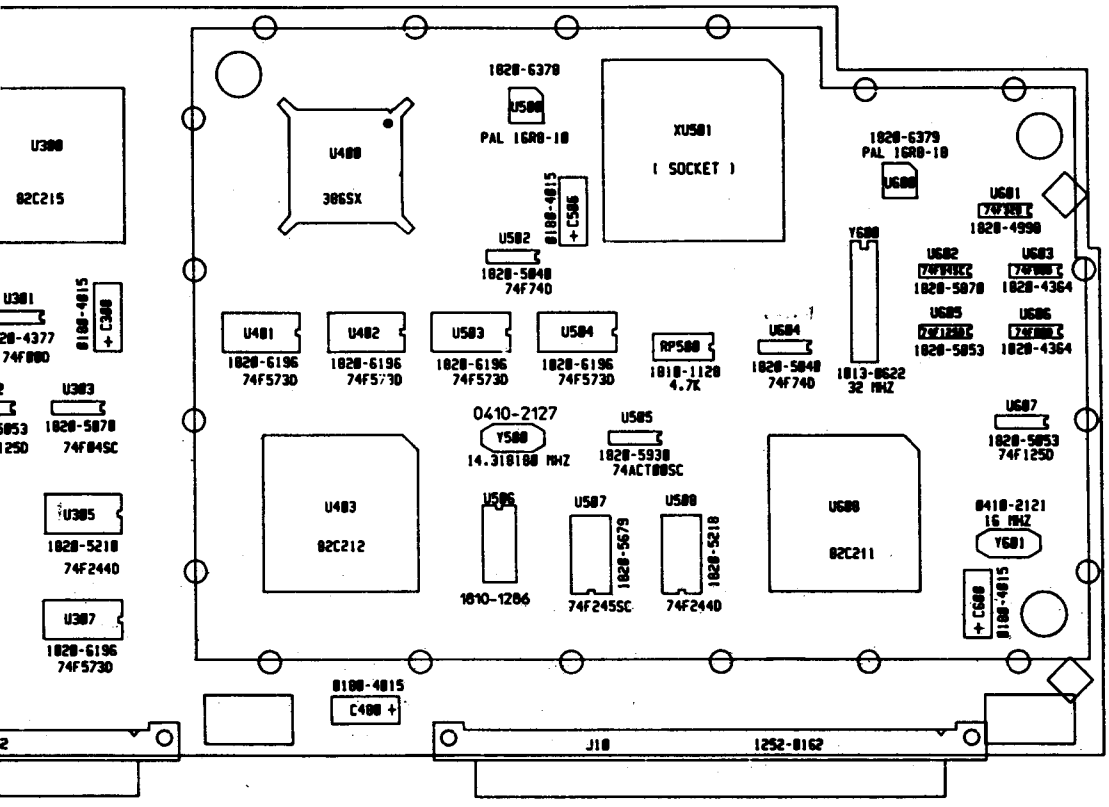


QS/16 QS/20 Memory Extension PCA
Electrical Schematic

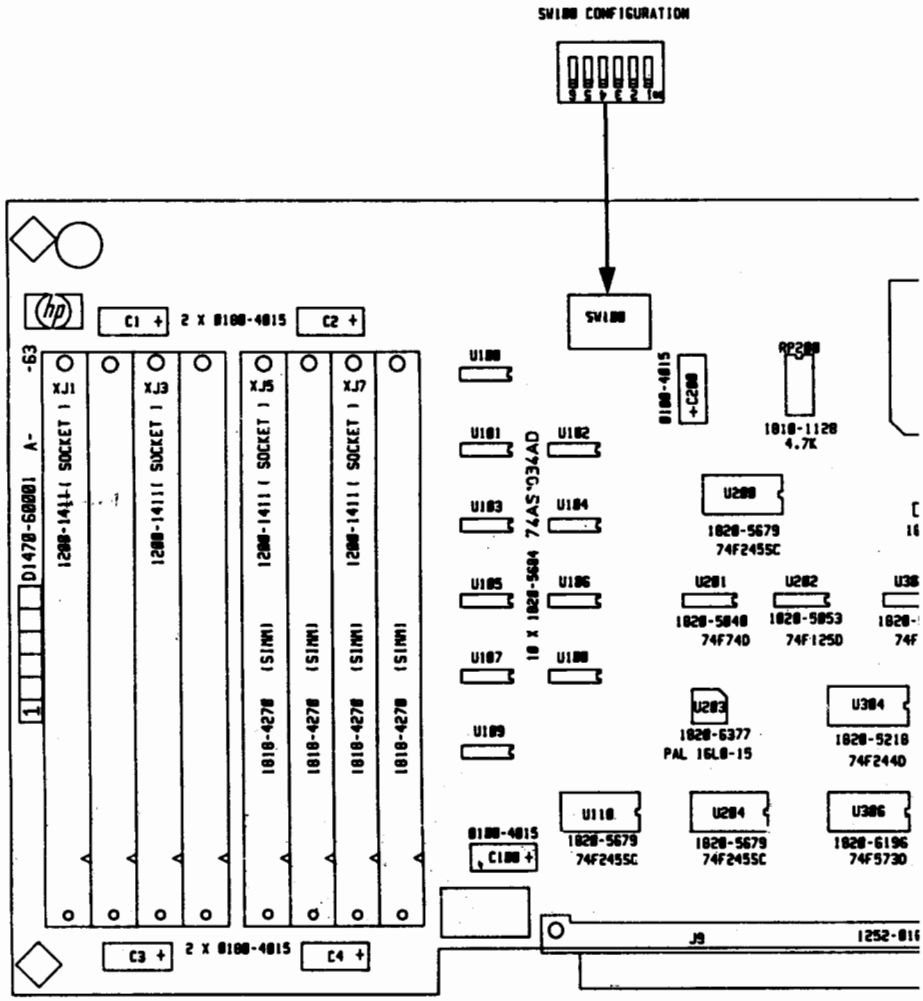
SHEET 1 OF 1


LBE (0: 1)
CAS (2: 3)
RAS (2: 3)
MA (0: 9)
MP (0: 1)
MD (0: 31)
MA0
MA1
MA2
MA3
MA4
RAS2
CAS2
LBE0
MA5
MA6
MA7
MA8
MA9
RAS3
CAS3
LBE0
WE
1820-5036
74AS1004AD
U3
U5
1820-4961
74AS8048DW
U13
U14
0699-2137
R3
R2
R8
R7
R1
R5
R30
R9
R4
R6
R10
R12
R11
R29
R36
33
A0 VCC1
A1 VCC2
A2 VSS1
A3 VSS2
A4 DQ0
A5 DQ1
A6 DQ2
A7 DQ3
A8 DQ4
A9 DQ5
A10 DQ6
WE DQ7
RAS NC
CAS Q8
CASB D8
U1
U2
256KbitX9 OR 1MbitX9
SIMM

Computer Museum

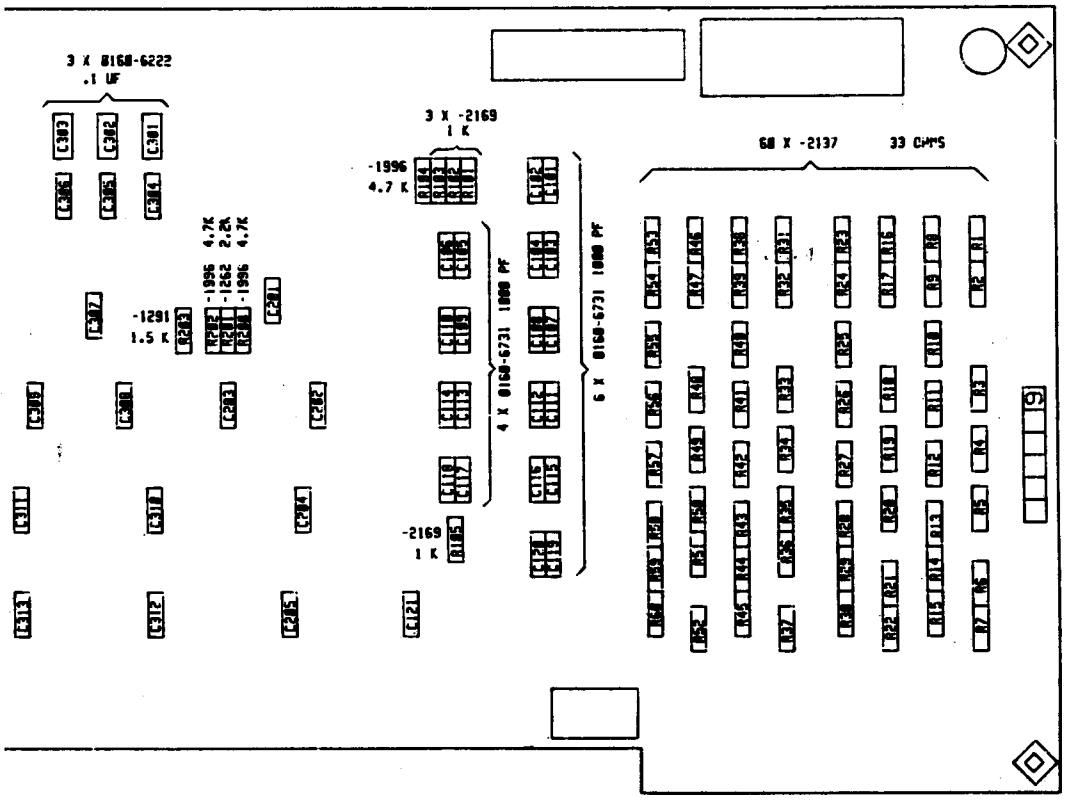


QS/16S Processor/Memory PCA
Component Layout
(Component Side)



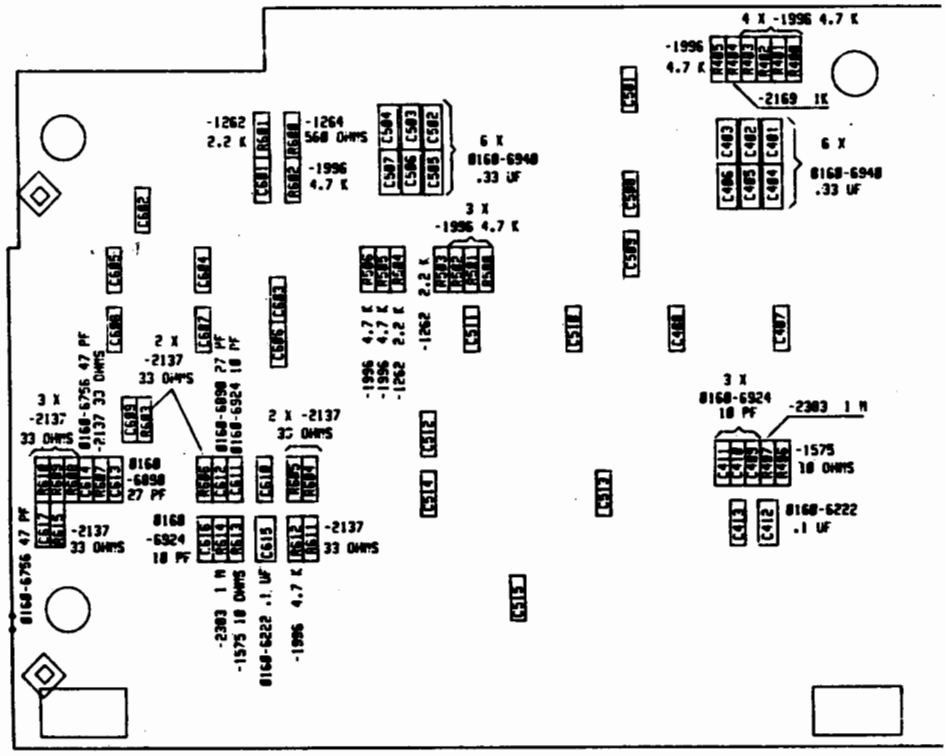
COMPONENT SIDE VIEW

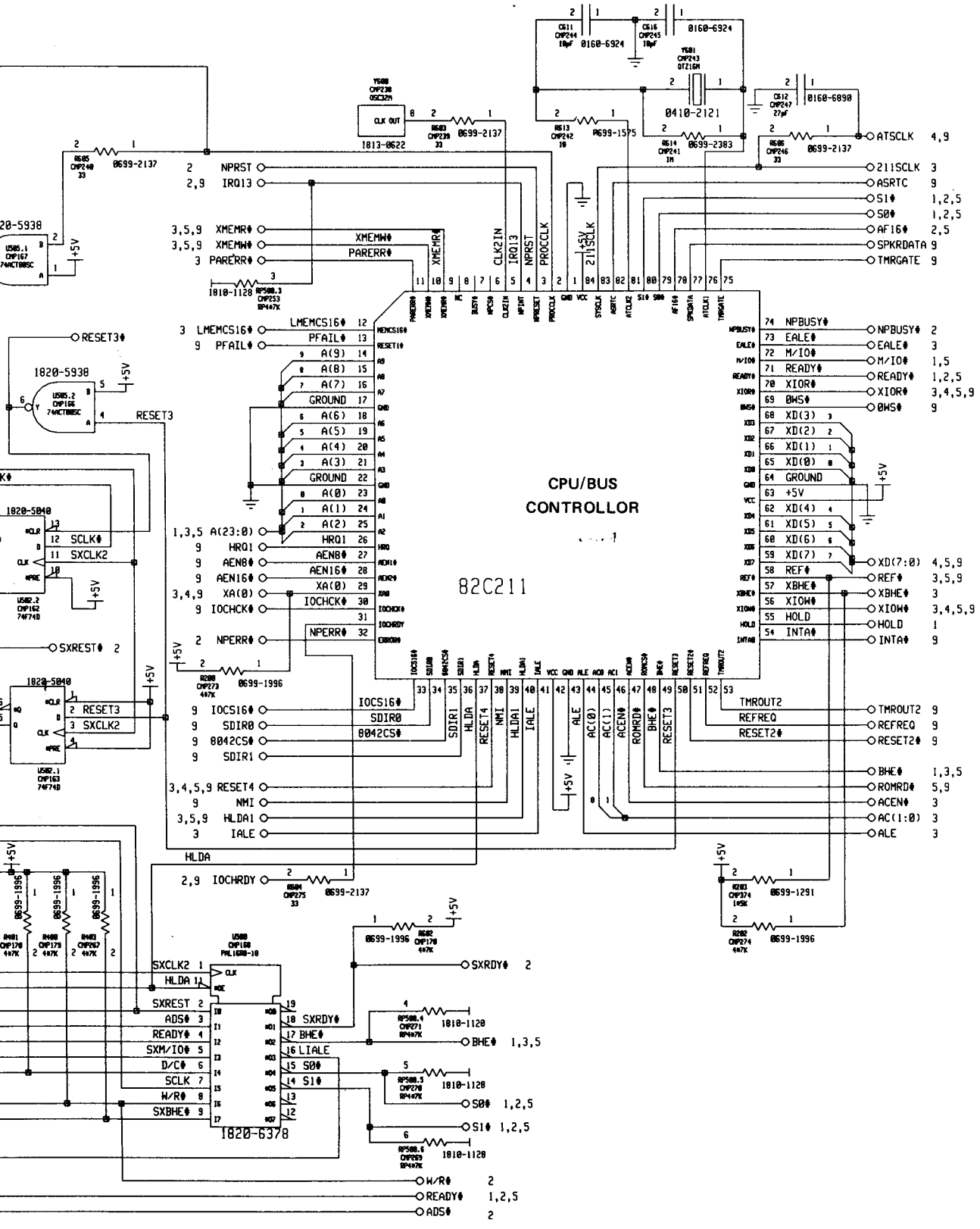
DER SIDE VIEW



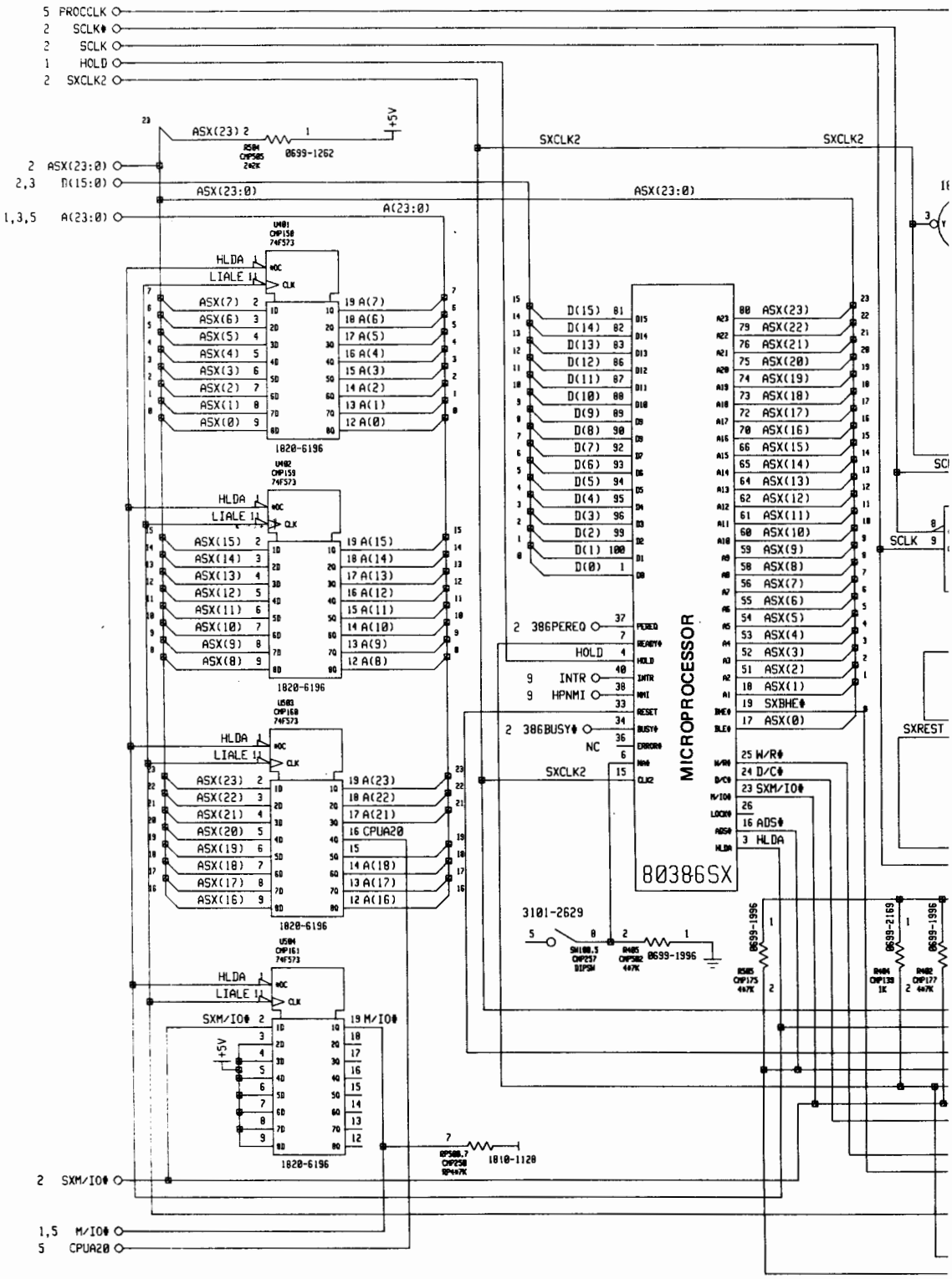
QS/16S Processor/Memory PCA
Component Layout
(Solder Side)

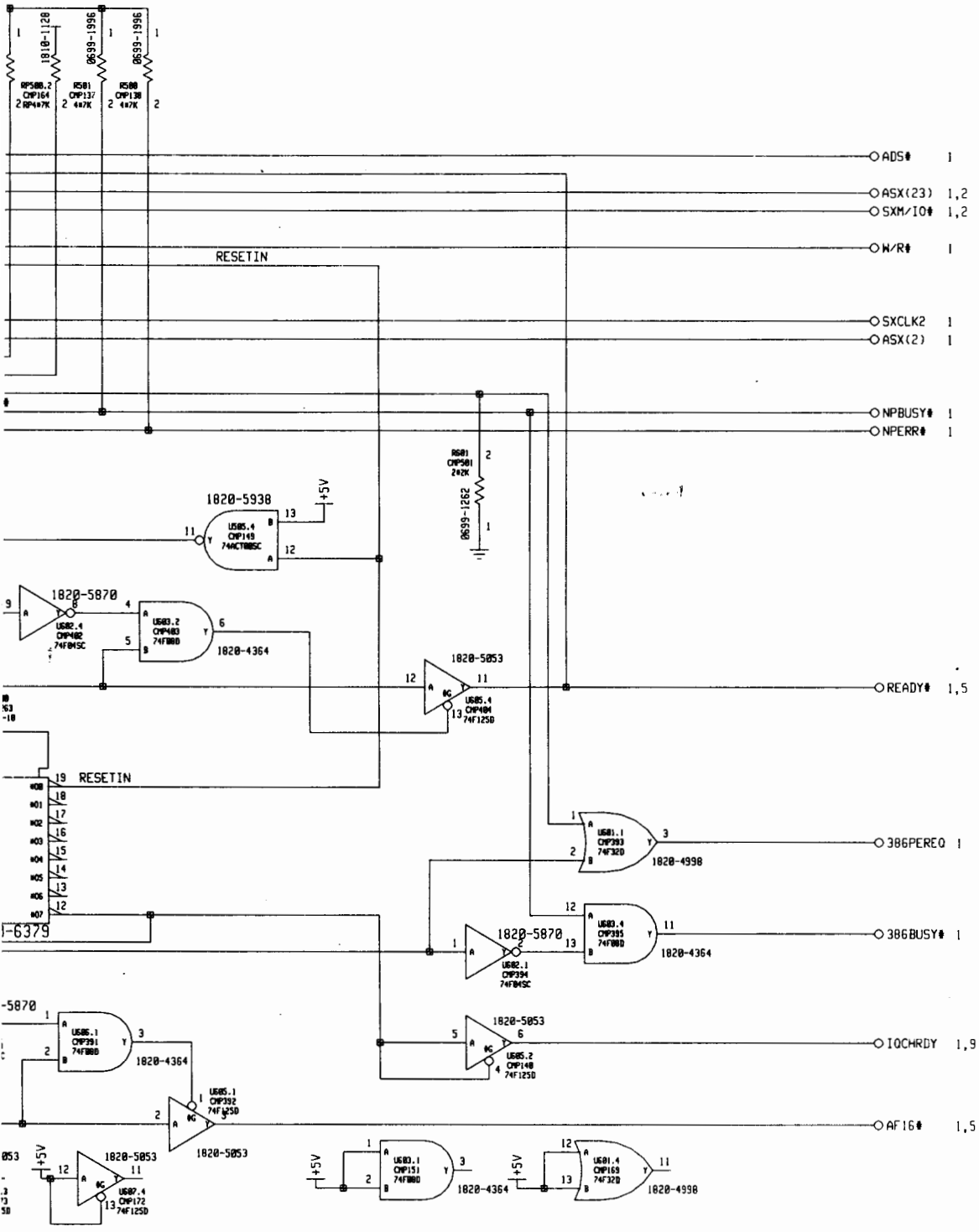
SOL


4 X -1996 4.7 K
-1996
4.7 K
-2169 1K
6 X
8160-6948
.33 UF
-1262
2.2 K
-1264
560 OHMS
-1996
4.7 K
3 X
-1996 4.7 K
2 X
-2137
33 OHMS
3 X
-2137
33 OHMS
8160-6756 47 PF
-2137 33 OHMS
8160
-6050
27 PF
8160-6050 27 PF
8160-6924 18 PF
2 X -2137
33 OHMS
8160
-6924
18 PF
-2137
33 OHMS
-2303 1 M
-1575 10 OHMS
8160-6222 .1 UF
-1996 4.7 K
3 X
8160-6924
18 PF
-2303 1 M
-1575
10 OHMS
8160-6222
.1 UF

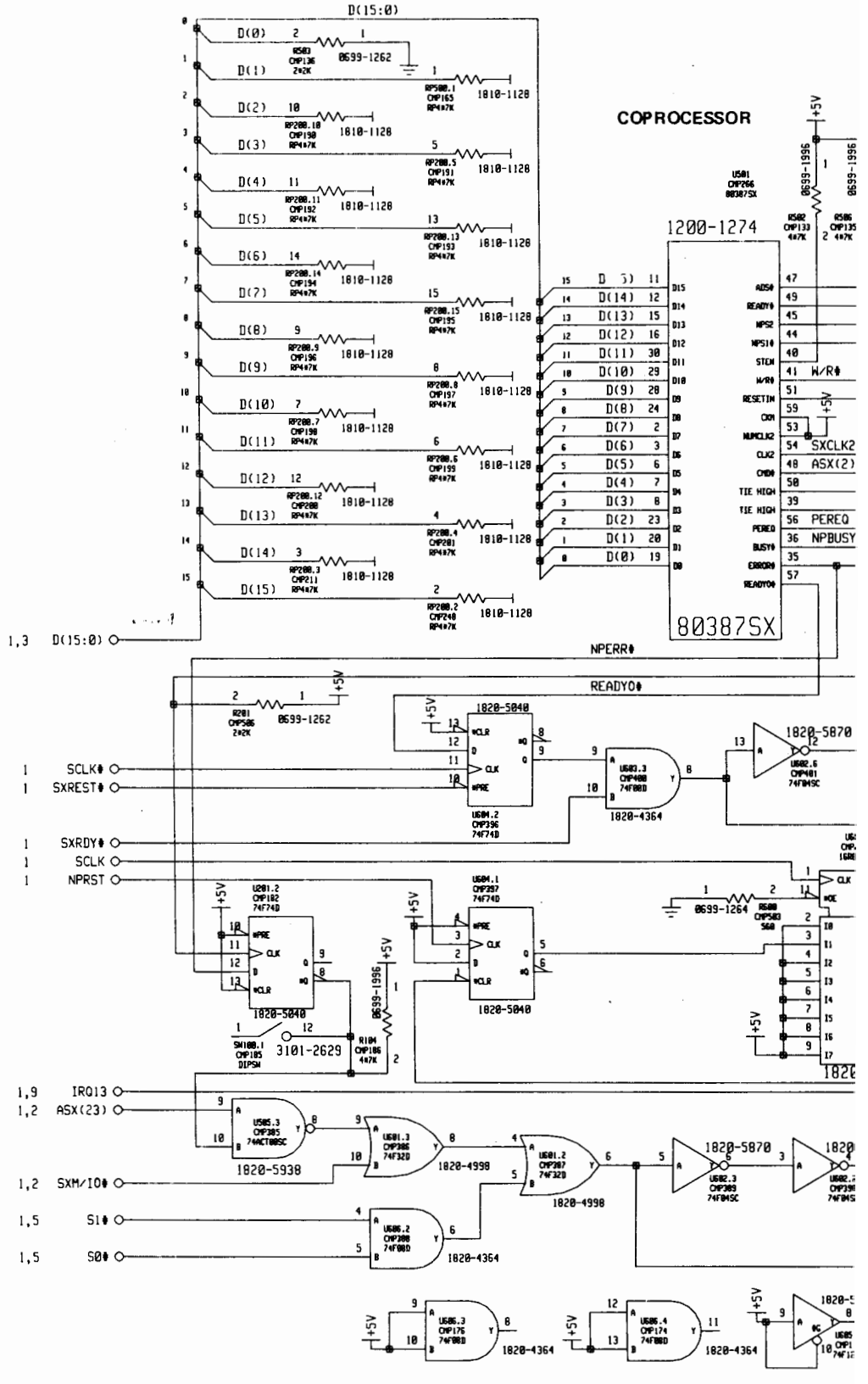


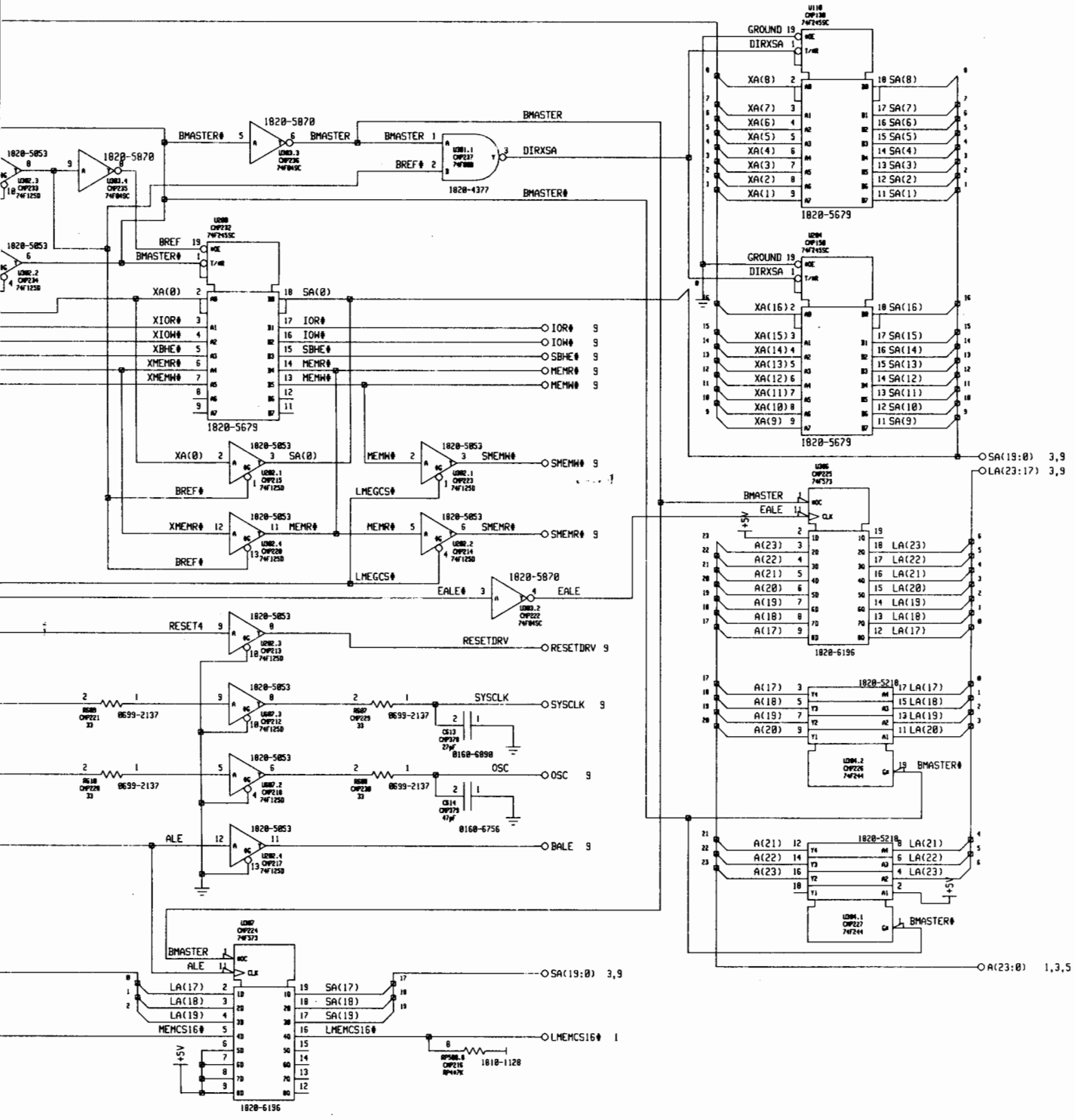
QS/16S Processor/Memory PCA
Electrical Schematic


5 PROCCLK
2 SCLK♦
2 SCLK
1 HOLD
2 SXCLK2
2 ASX(23:0)
2,3 D(15:0)
1,3,5 A(23:0)
ASX(23:0)
A(23:0)
SXCLK2
+5V
HLDA
LIALE
1820-6196
MICROPROCESSOR
80386SX
2 386PEREQ
HOLD
9 INTR
9 HPNMI
2 386BUSY♦
NC
SXCLK2
3101-2629
2 SXM/IO♦
1,5 M/IO♦
5 CPUA20

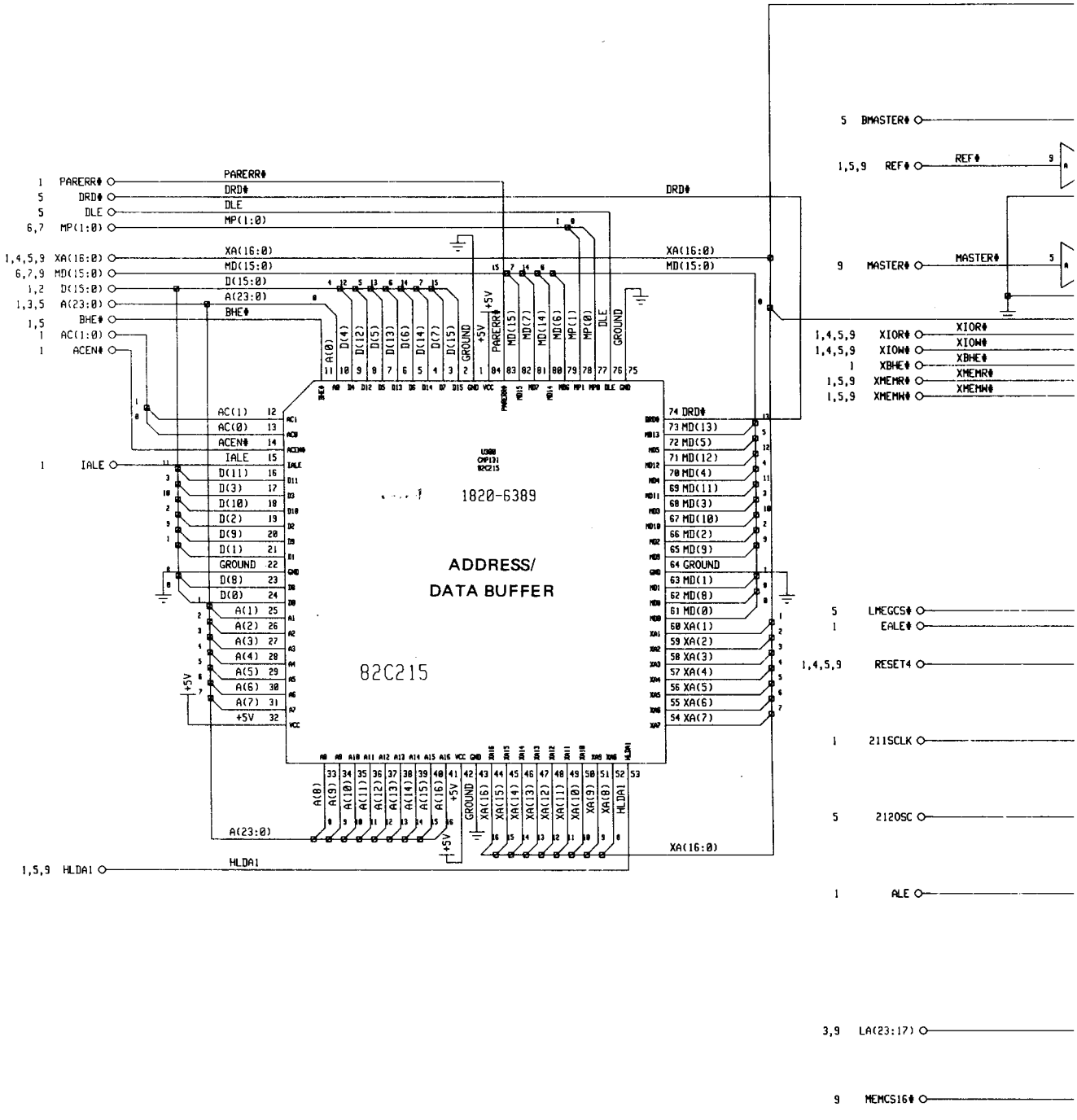


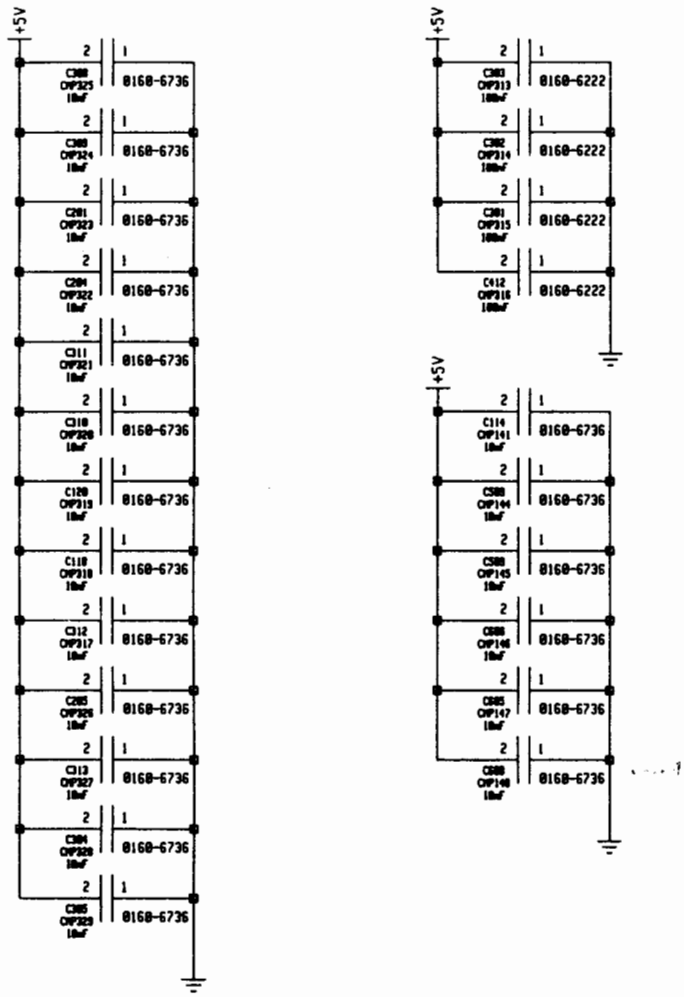
QS/16S Processor/Memory PCA

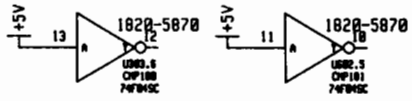

COPROCESSOR
D(15:0)
1200-1274
80387SX
1,3 D(15:0)
NPERR#
READY0#
SCLK#
SXREST#
SXRDY#
SCLK
NPRST
IRQ13
ASX(23)
SXM/IO#
S1#
S0#
SXCLK2
ASX(2)
W/R#
PEREQ
NPBUSY
1820-5040
1820-5870
1820-4364
1820-4998
1820-5938
3101-2629

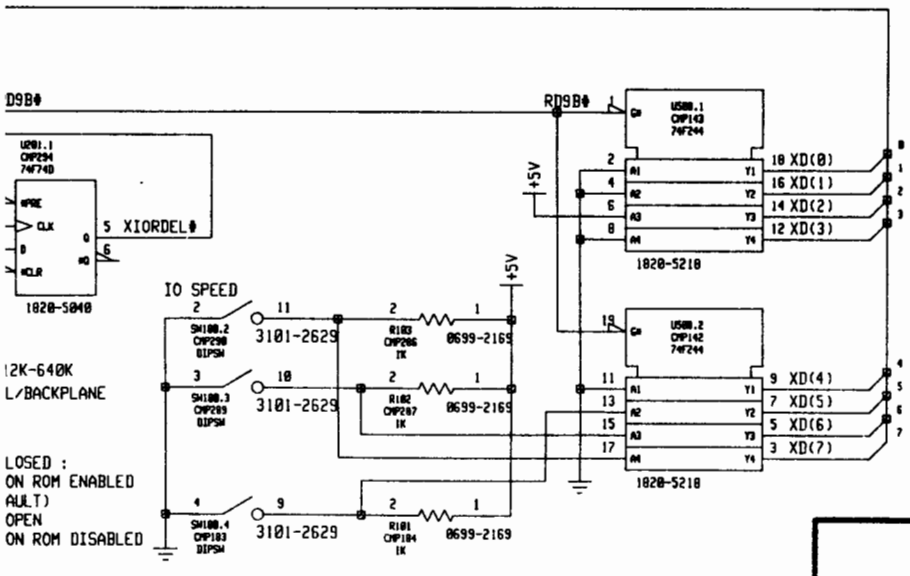


QS/16S Processor/Memory PCA


1820-6389
ADDRESS/
DATA BUFFER
82C215
PARERR#
DRD#
DLE
MP(1:0)
XA(16:0)
MD(15:0)
D(15:0)
A(23:0)
BHE#
AC(1:0)
ACEN#
IALE
HLDA1
+5V
GROUND
1 PARERR#
5 DRD#
5 DLE
6,7 MP(1:0)
1,4,5,9 XA(16:0)
6,7,9 MD(15:0)
1,2 D(15:0)
1,3,5 A(23:0)
1,5 BHE#
1 AC(1:0)
1 ACEN#
1 IALE
1,5,9 HLDA1
5 BMASTER#
1,5,9 REF#
9 MASTER#
1,4,5,9 XIOR#
1,4,5,9 XIOW#
1 XBHE#
1,5,9 XMEMR#
1,5,9 XMEMW#
5 LMEGCS#
1 EALE#
1,4,5,9 RESET4
1 211SCLK
5 2120SC
1 ALE
3,9 LA(23:17)
9 MEMCS16#



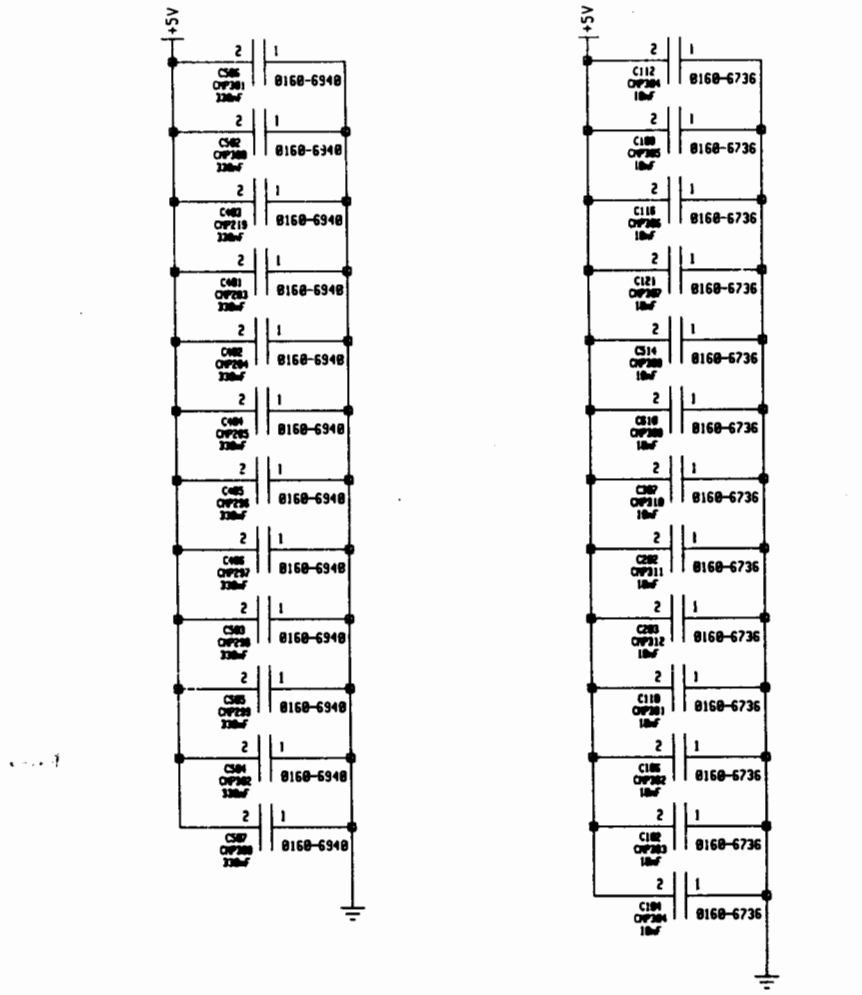


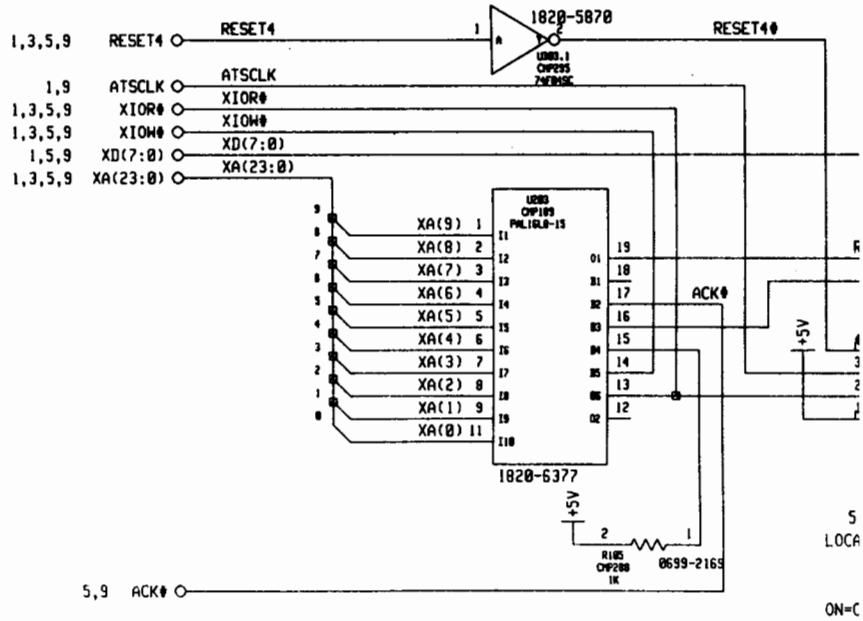


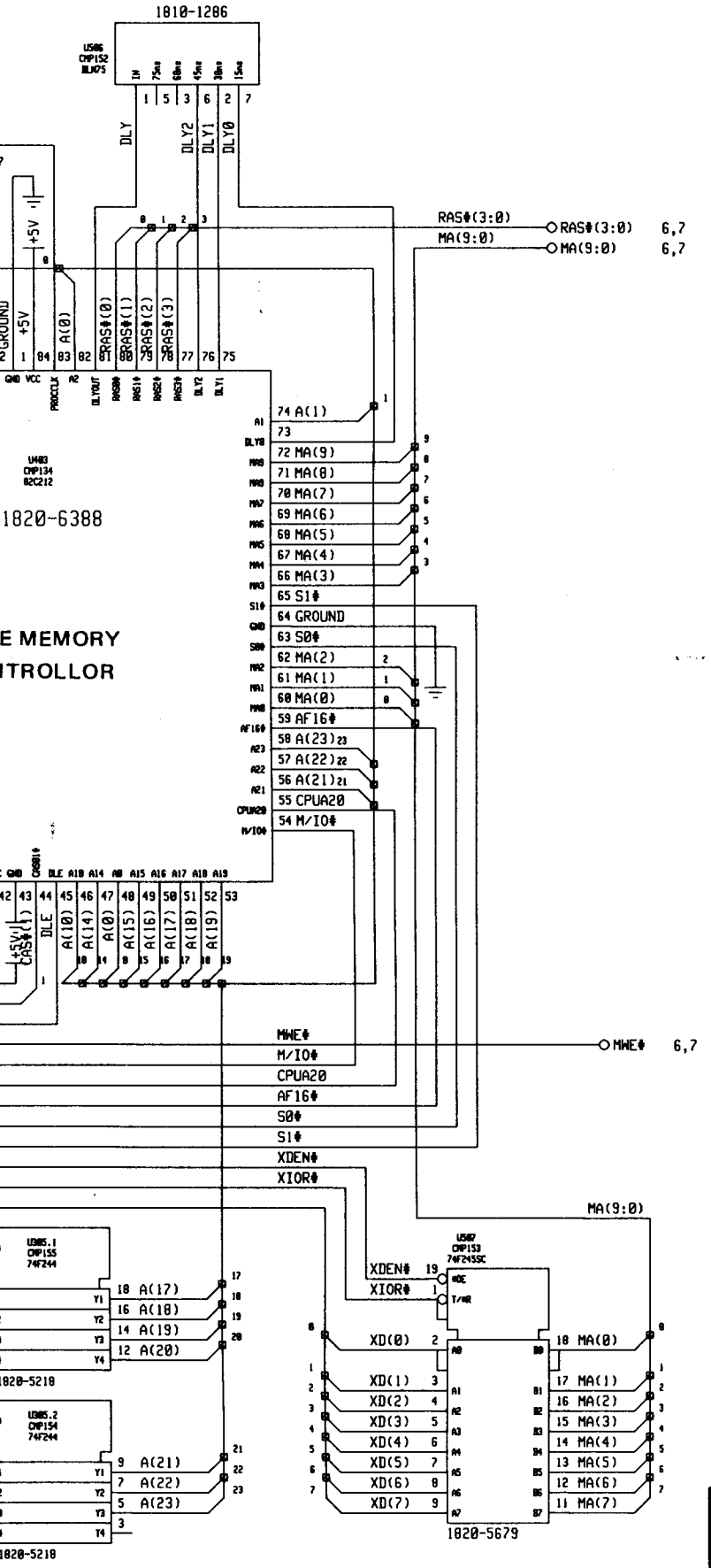
Computer Museum

QS/16S Processor/Memory PCA

SHEET 4 OF 9

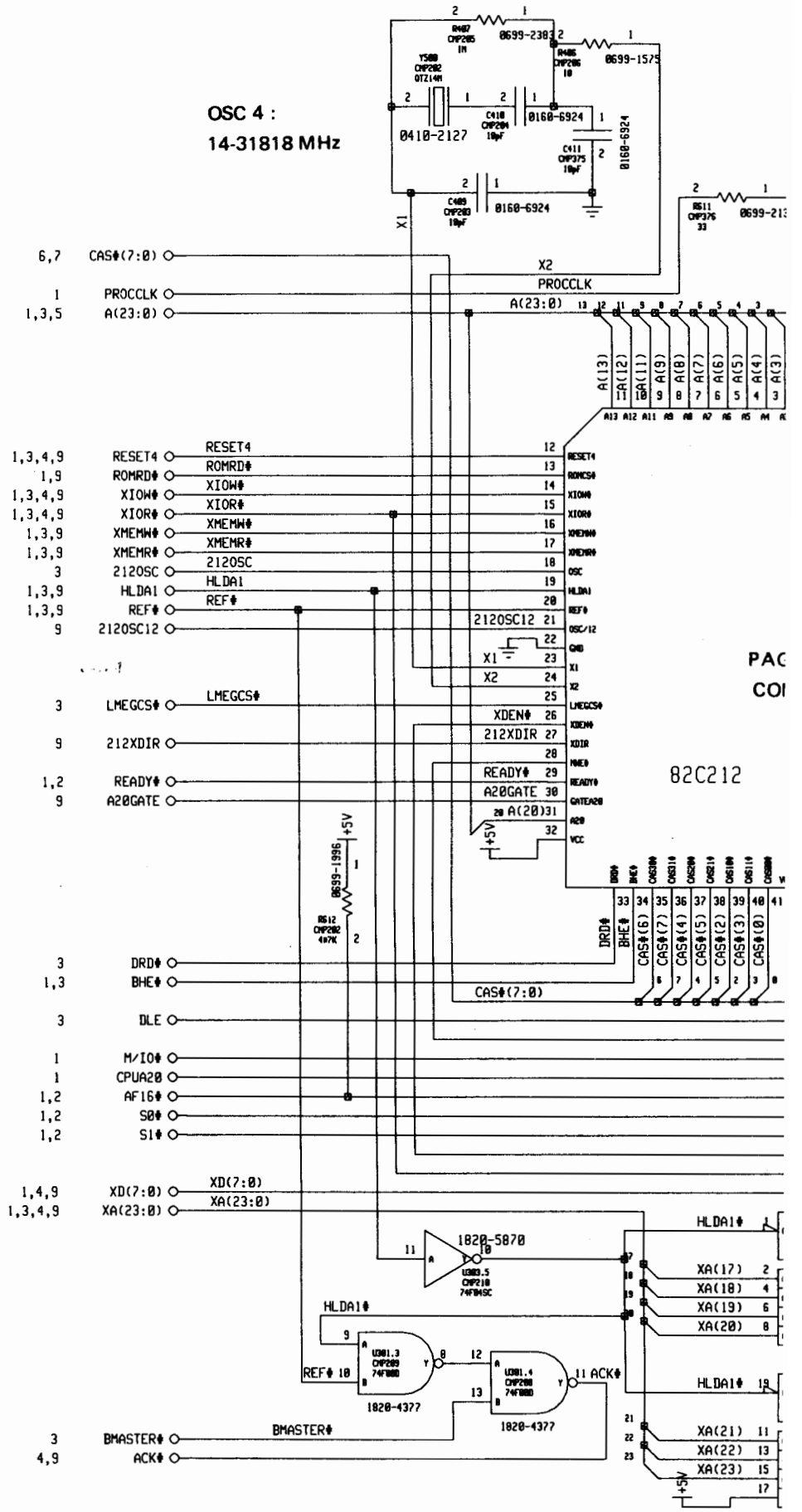

+5V
0160-6940
0160-6736

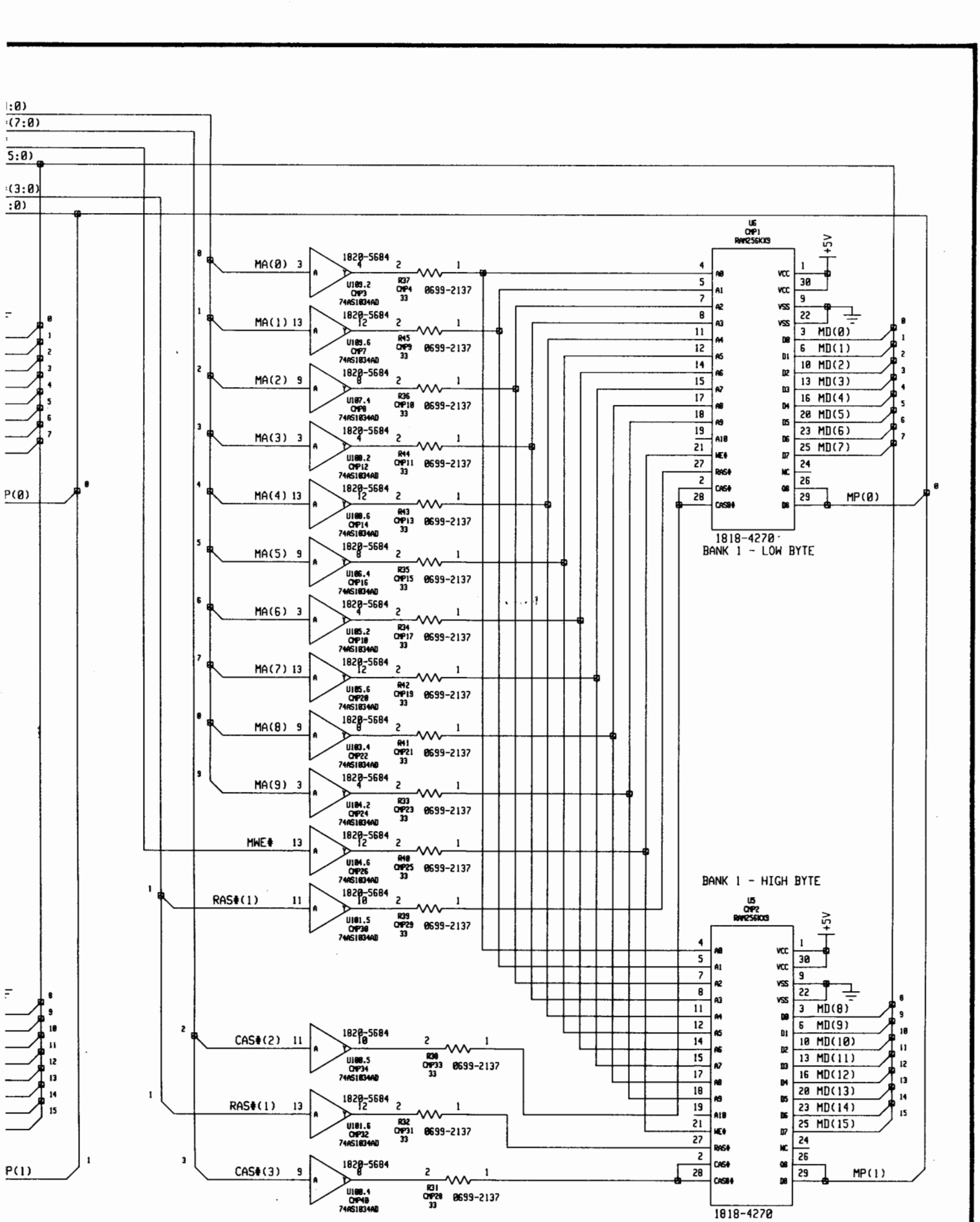

1820-5870
RESET4
RESET4Ø
ATSCLK
XIORØ
XIOWØ
XD(7:0)
XA(23:0)
XA(9)
XA(8)
XA(7)
XA(6)
XA(5)
XA(4)
XA(3)
XA(2)
XA(1)
XA(0)
ACKØ
1820-6377
+5V
0699-2165
1,3,5,9
1,9
5,9



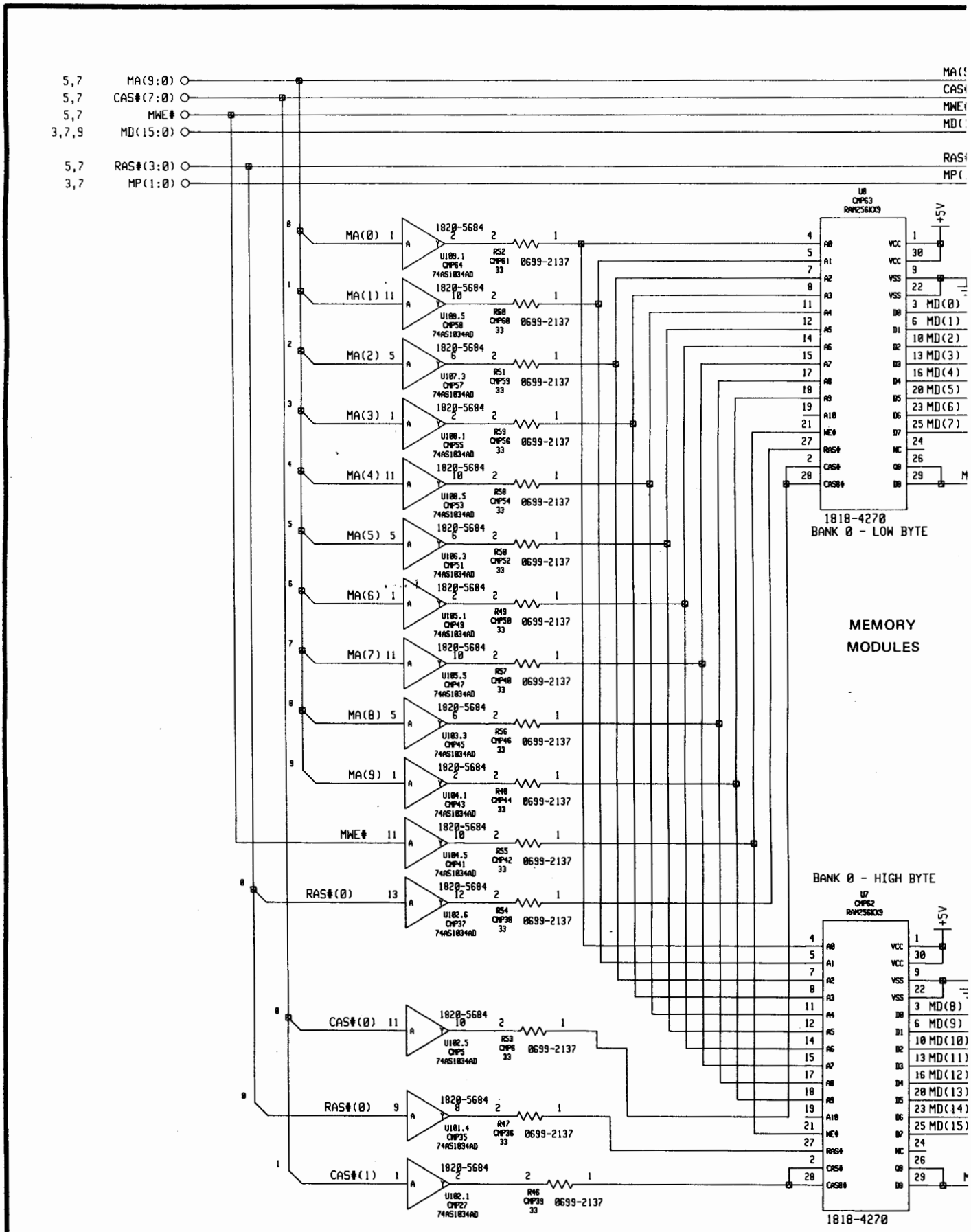
Computer Museum

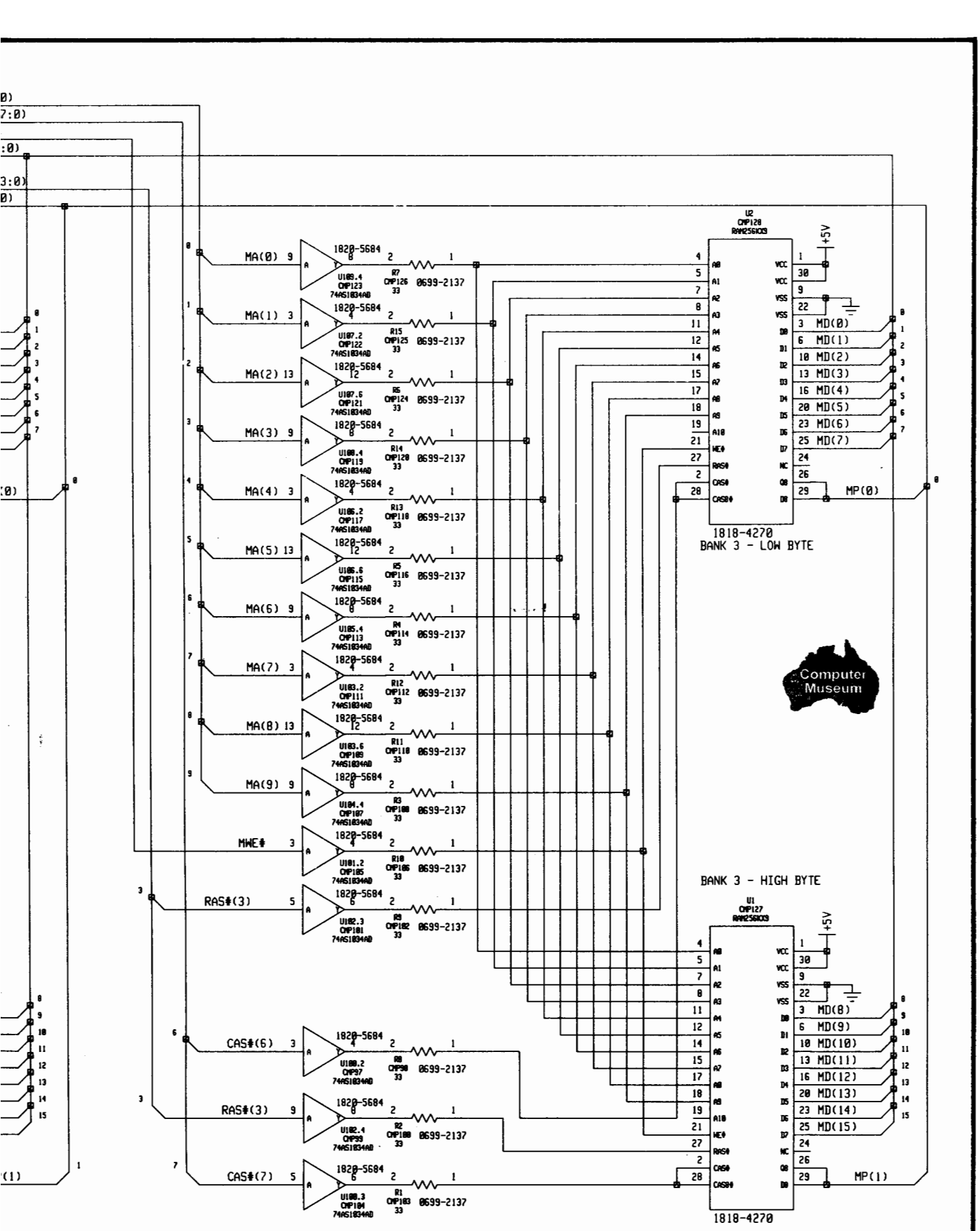
QS/16S Processor/Memory PCA


OSC 4 :
14-31818 MHz
0410-2127
0160-6924
0699-2383
0699-1575
X1
X2
PROCCLK
A(23:0)
CAS#(7:0)
RESET4
ROMRD#
XIOW#
XIOR#
XMEMW#
XMEMR#
2120SC
HLDA1
REF#
2120SC12
LMEGCS#
XDEN#
212XDIR
READY#
A20GATE
A(20)
+5V
82C212
DRD#
BHE#
DLE
M/IO#
CPUA20
AF16#
S0#
S1#
XD(7:0)
XA(23:0)
1820-5870
HLDA1#
REF# 10
1820-4377
BMASTER#
ACK#
XA(17)
XA(18)
XA(19)
XA(20)
XA(21)
XA(22)
XA(23)

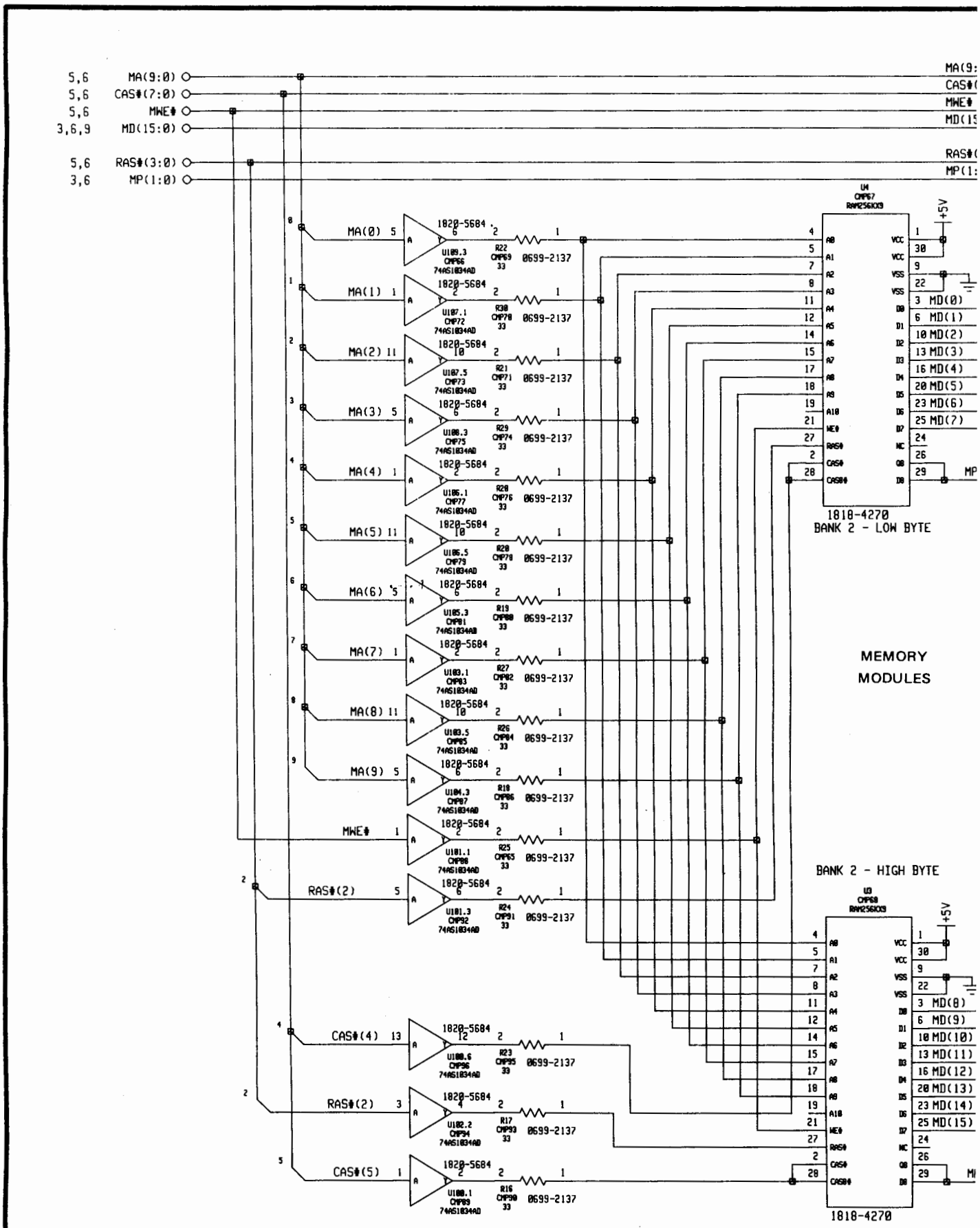


QS/16S Processor/Memory PCA

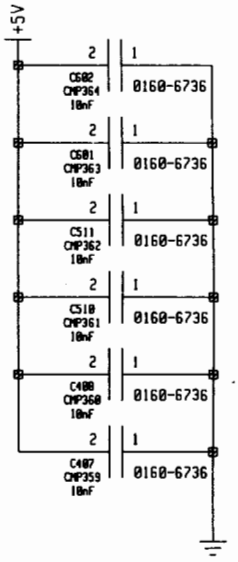

5,7 MA(9:0)
5,7 CAS#(7:0)
5,7 MWE#
3,7,9 MD(15:0)
5,7 RAS#(3:0)
3,7 MP(1:0)
MA(0)
MA(1)
MA(2)
MA(3)
MA(4)
MA(5)
MA(6)
MA(7)
MA(8)
MA(9)
MWE#
RAS#(0)
CAS#(0)
RAS#(0)
CAS#(1)
1820-5684
0699-2137
74AS1034AD
U8
CMP63
RAM256X09
1818-4270
BANK 0 - LOW BYTE
MEMORY
MODULES
BANK 0 - HIGH BYTE
U7
CMP62
RAM256X09
1818-4270
+5V

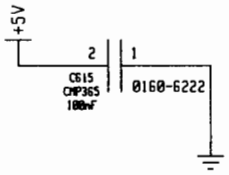


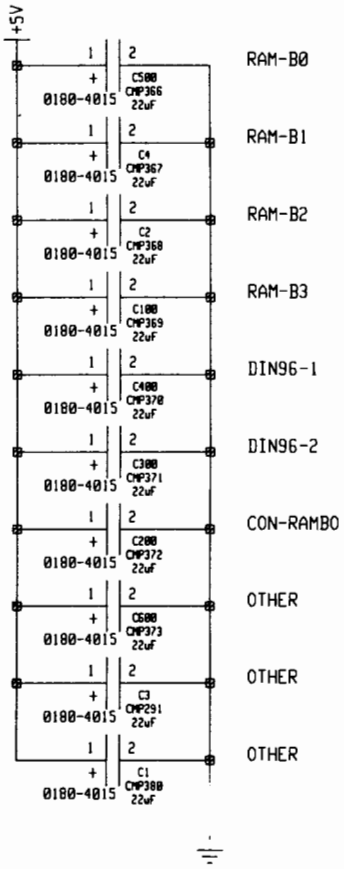
QS/16S Processor/Memory PCA


5,6 MA(9:0)
5,6 CAS#(7:0)
5,6 MWE#
3,6,9 MD(15:0)
5,6 RAS#(3:0)
3,6 MP(1:0)
MA(0) 5
MA(1) 1
MA(2) 11
MA(3) 5
MA(4) 1
MA(5) 11
MA(6) 5
MA(7) 1
MA(8) 11
MA(9) 5
MWE# 1
RAS#(2) 5
CAS#(4) 13
RAS#(2) 3
CAS#(5) 1
1820-5684
0699-2137
74AS1034AD
+5V
1818-4270
BANK 2 - LOW BYTE
BANK 2 - HIGH BYTE
MEMORY
MODULES
MD(0)
MD(1)
MD(2)
MD(3)
MD(4)
MD(5)
MD(6)
MD(7)
MD(8)
MD(9)
MD(10)
MD(11)
MD(12)
MD(13)
MD(14)
MD(15)

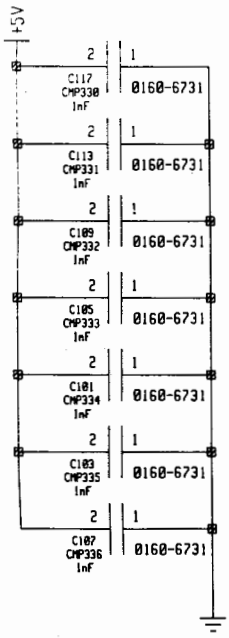
Computer Museum

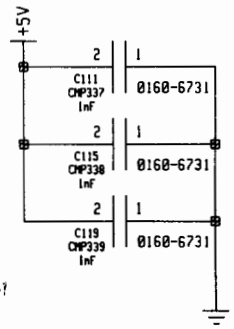


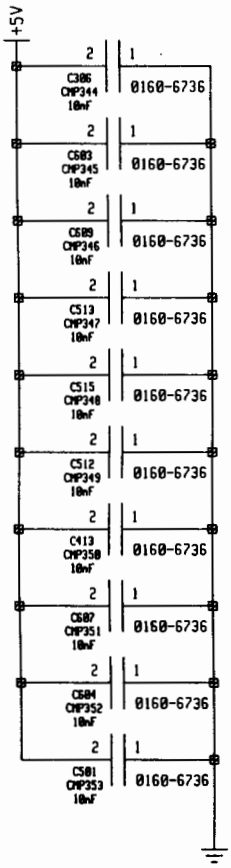


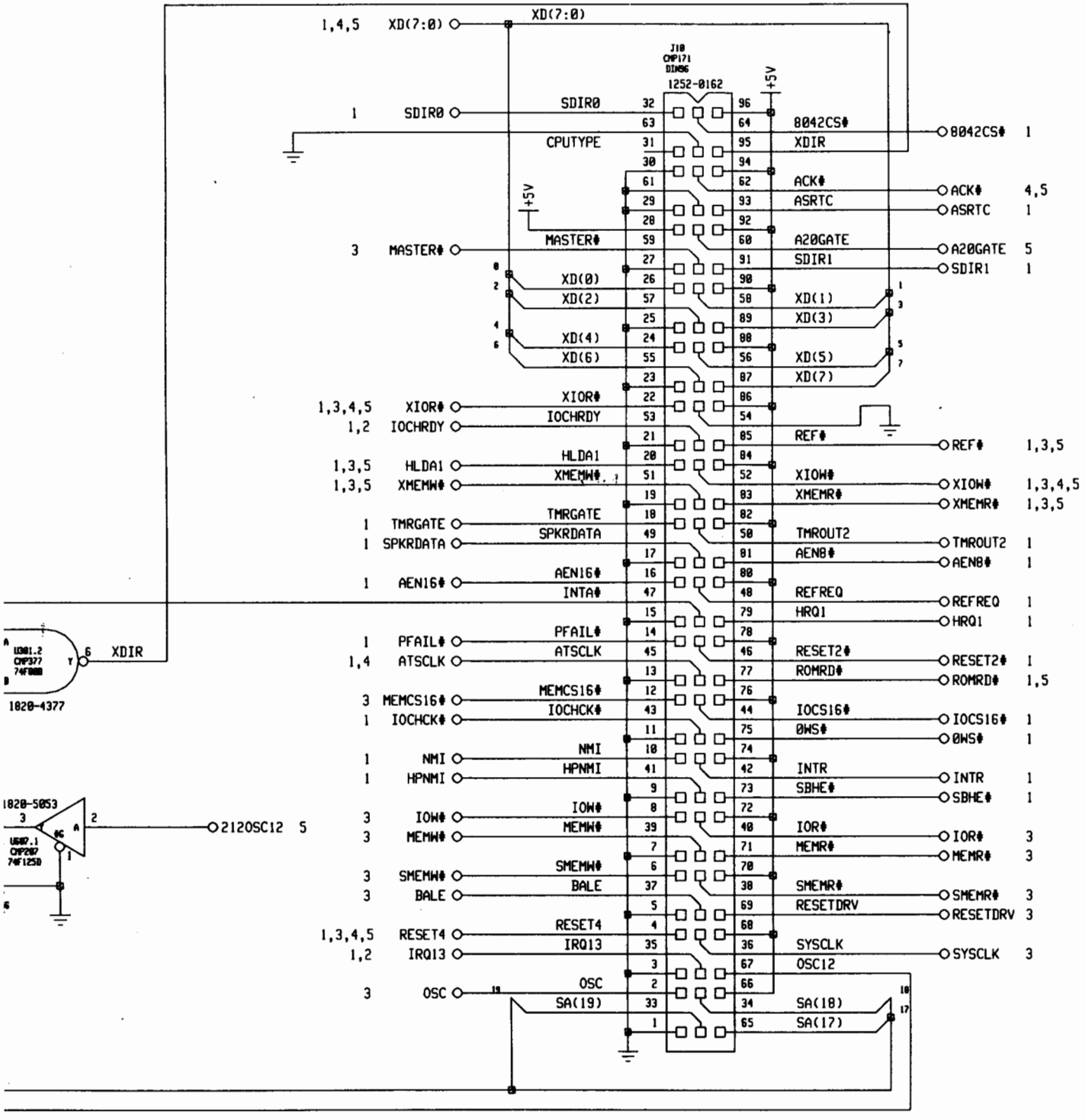


QS/16S Processor/Memory PCA

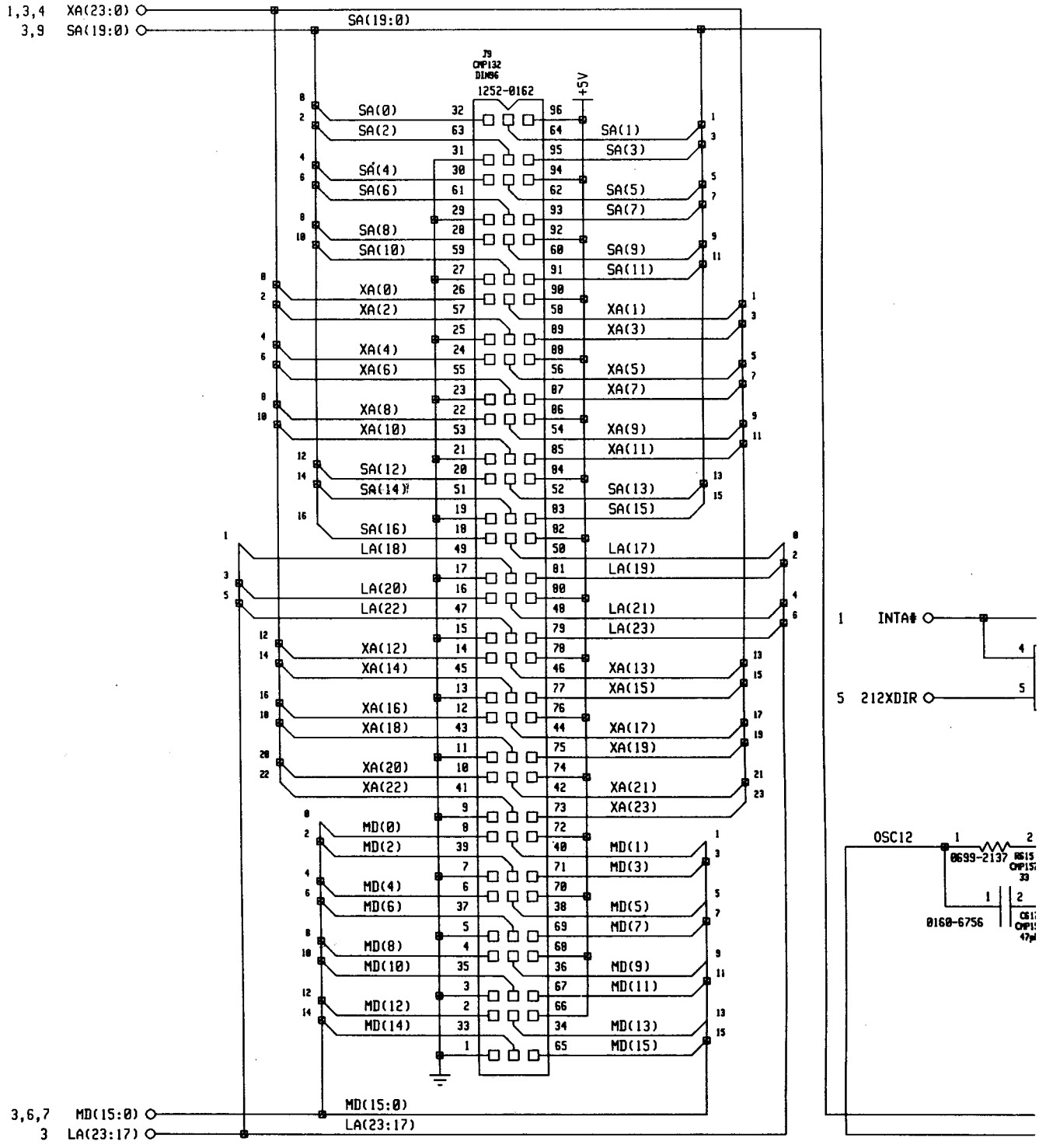

+5V
C117 CMP330 1nF
C113 CMP331 1nF
C109 CMP332 1nF
C105 CMP333 1nF
C101 CMP334 1nF
C103 CMP335 1nF
C107 CMP336 1nF
0160-6731

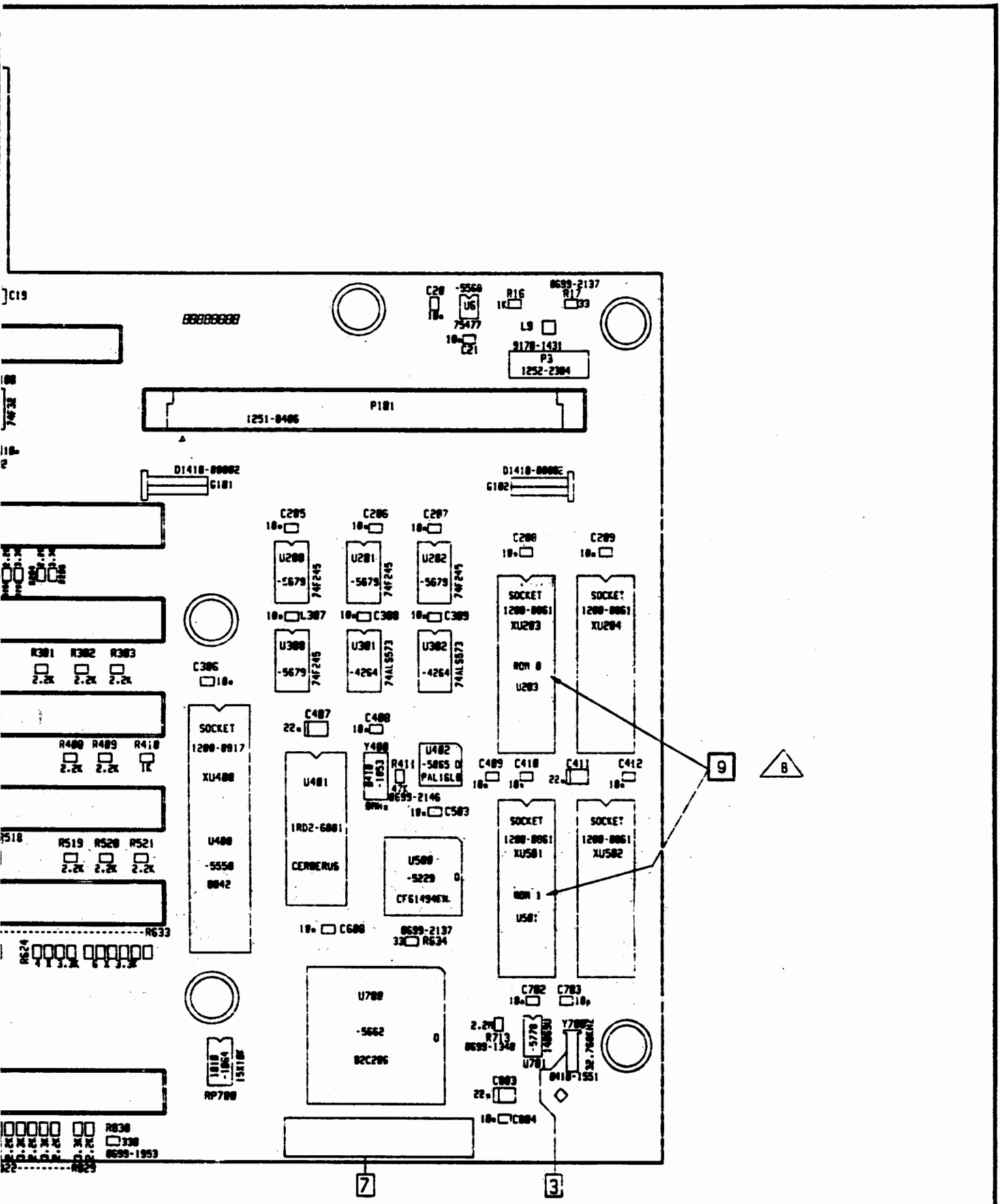

+5V
C111 CMP337 1nF
C115 CMP338 1nF
C119 CMP339 1nF
0160-6731


+5V
C306 CMP344 10nF
C503 CMP345 10nF
C509 CMP346 10nF
C513 CMP347 10nF
C515 CMP348 10nF
C512 CMP349 10nF
C413 CMP350 10nF
C507 CMP351 10nF
C504 CMP352 10nF
C501 CMP353 10nF
0160-6736



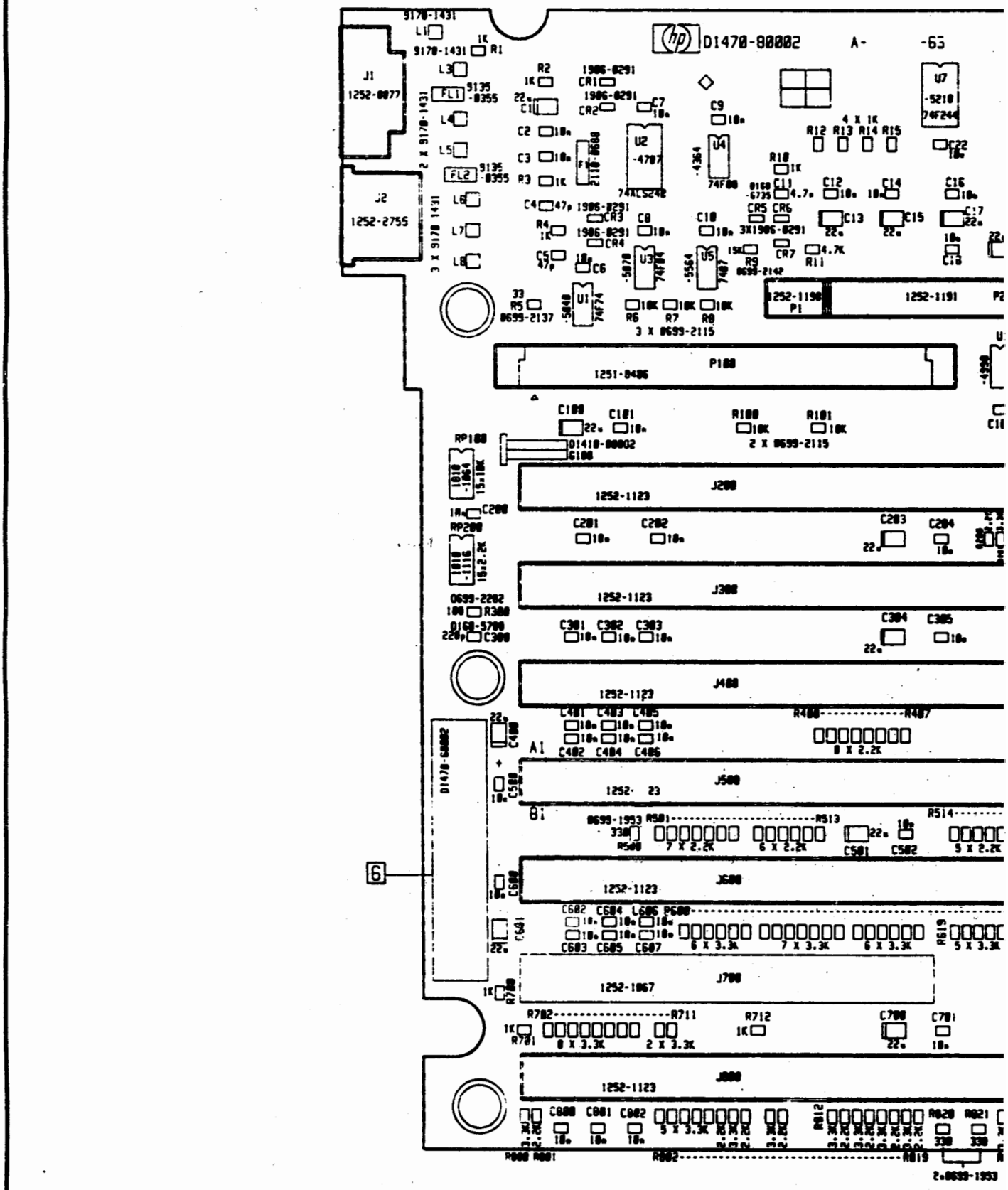
QS/16S Processor/Memory PCA

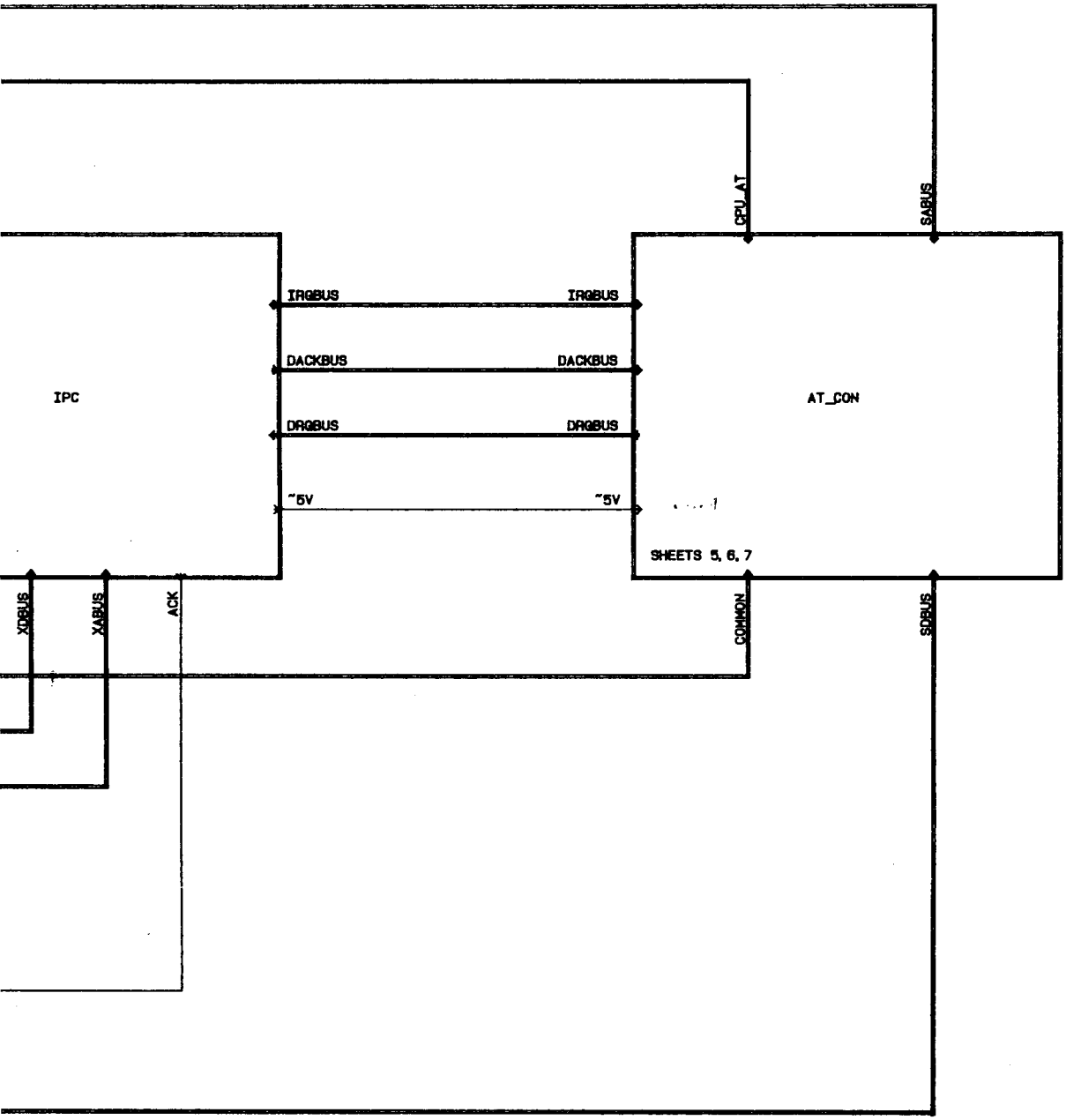

1,3,4 XA(23:0)
3,9 SA(19:0)
SA(19:0)
J9
CMP132
DIN96
1252-0162
+5V
SA(0)
SA(2)
SA(1)
SA(3)
SA(4)
SA(6)
SA(5)
SA(7)
SA(8)
SA(10)
SA(9)
SA(11)
XA(0)
XA(2)
XA(1)
XA(3)
XA(4)
XA(6)
XA(5)
XA(7)
XA(8)
XA(10)
XA(9)
XA(11)
SA(12)
SA(14)
SA(13)
SA(15)
SA(16)
LA(18)
LA(17)
LA(19)
LA(20)
LA(22)
LA(21)
LA(23)
XA(12)
XA(14)
XA(13)
XA(15)
XA(16)
XA(18)
XA(17)
XA(19)
XA(20)
XA(22)
XA(21)
XA(23)
MD(0)
MD(2)
MD(1)
MD(3)
MD(4)
MD(6)
MD(5)
MD(7)
MD(8)
MD(10)
MD(9)
MD(11)
MD(12)
MD(14)
MD(13)
MD(15)
3,6,7 MD(15:0)
3 LA(23:17)
MD(15:0)
LA(23:17)
1 INTA#
5 212XDIR
OSC12
0699-2137
0160-6756



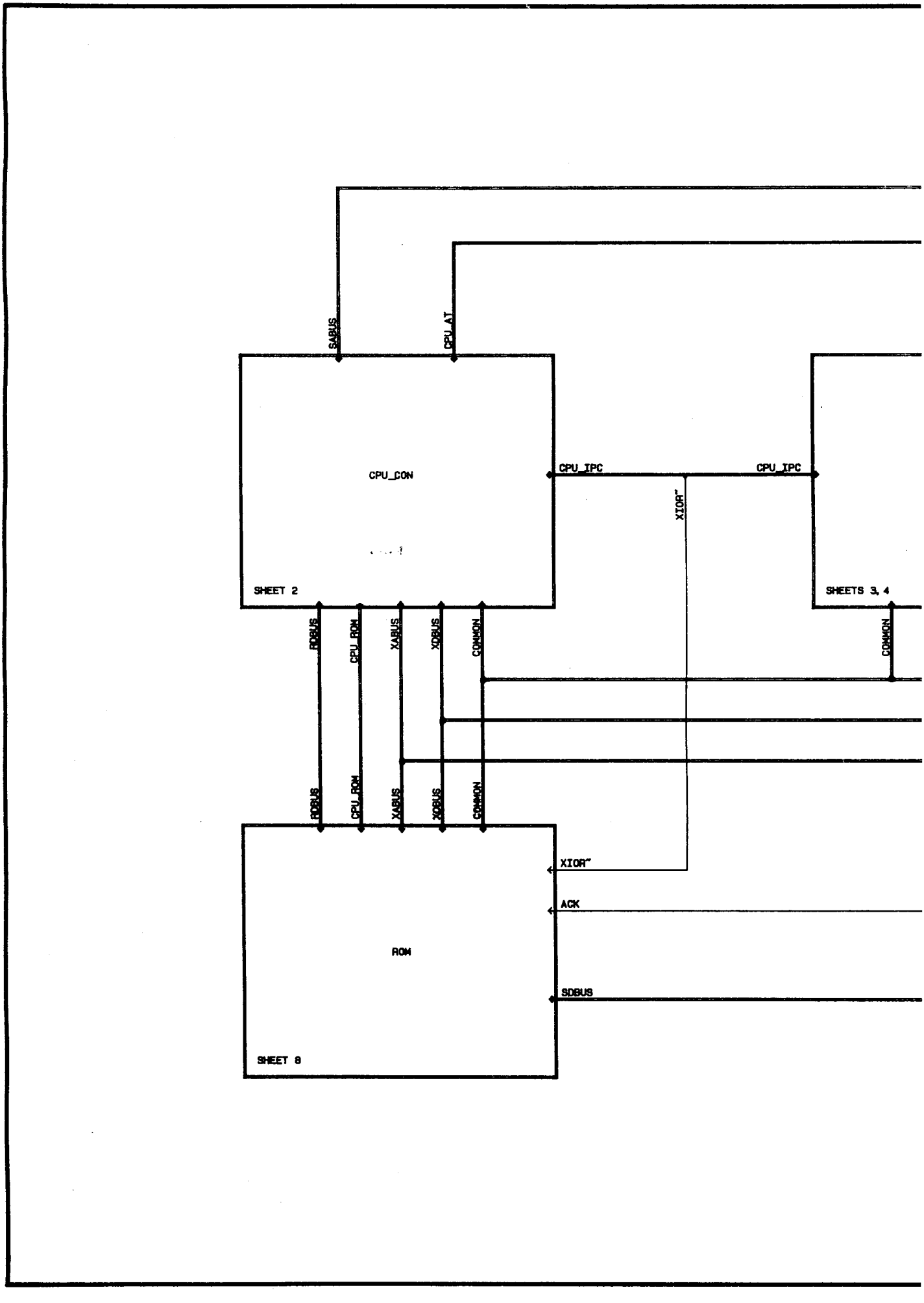
Vectra QS
System Interface PCA
Component Layout

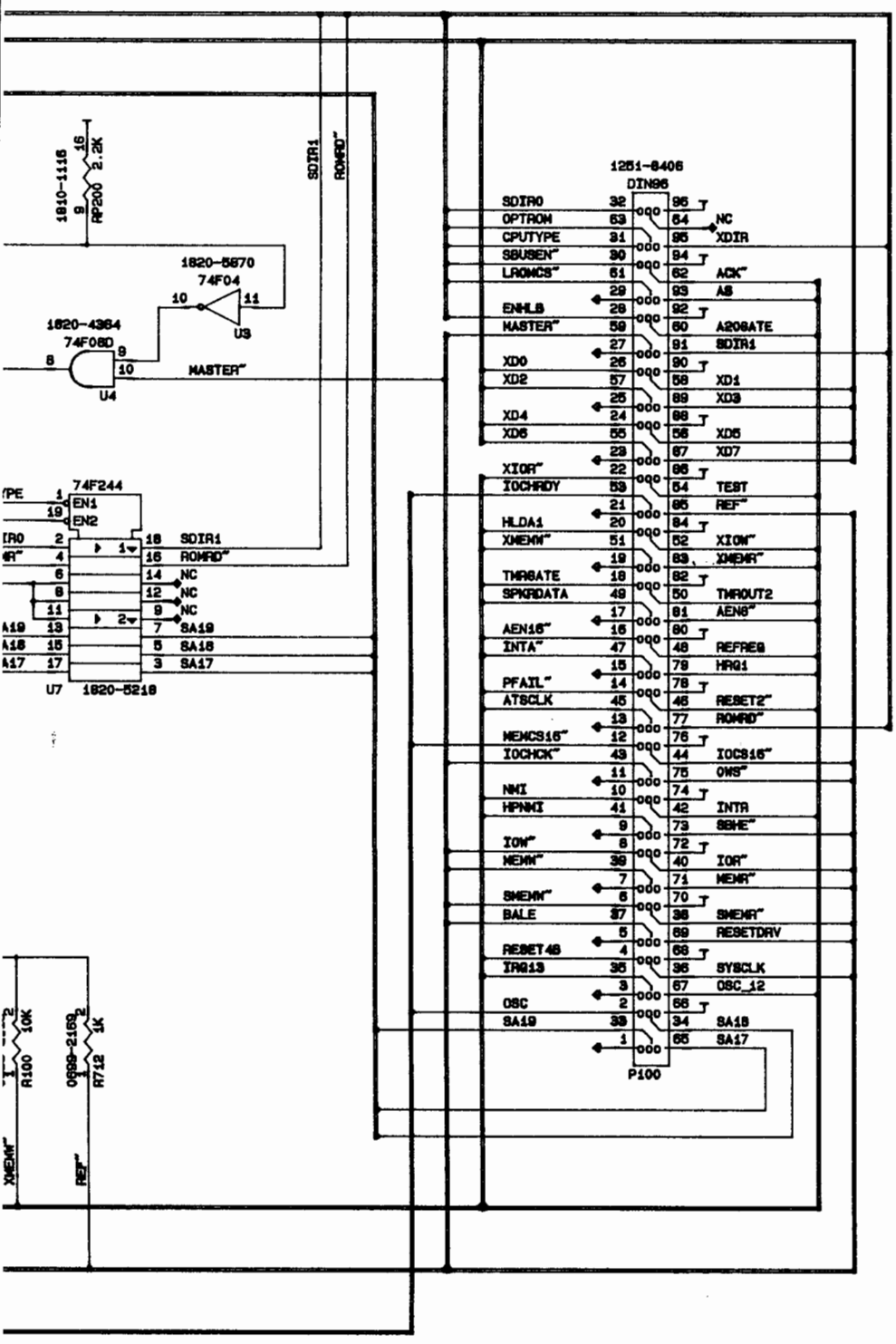
SHEET 1 OF 1


D1470-80002
A-
-63
J1
1252-0077
J2
1252-2755
P100
1251-8486
P1
1252-1190
1252-1191
J200
1252-1123
J300
1252-1123
J400
1252-1123
J500
1252-
23
J600
1252-1123
J700
1252-1867
J800
1252-1123
U1
74F74
U2
-4707
74ALS242
U3
74F04
U4
74F00
U5
7407
U7
-5210
74F244
FL1
9135
-0355
FL2
9135
-0355
D1470-80002
A1
B1
6
2 x 9170-1431
3 x 9170-1431
3 X 0699-2115
2 X 0699-2115
4 X 1K
8 X 2.2K
7 X 2.2K
6 X 2.2K
5 X 2.2K
6 X 3.3K
7 X 3.3K
8 X 3.3K
2 X 3.3K
5 X 3.3K
2 x 0699-1953



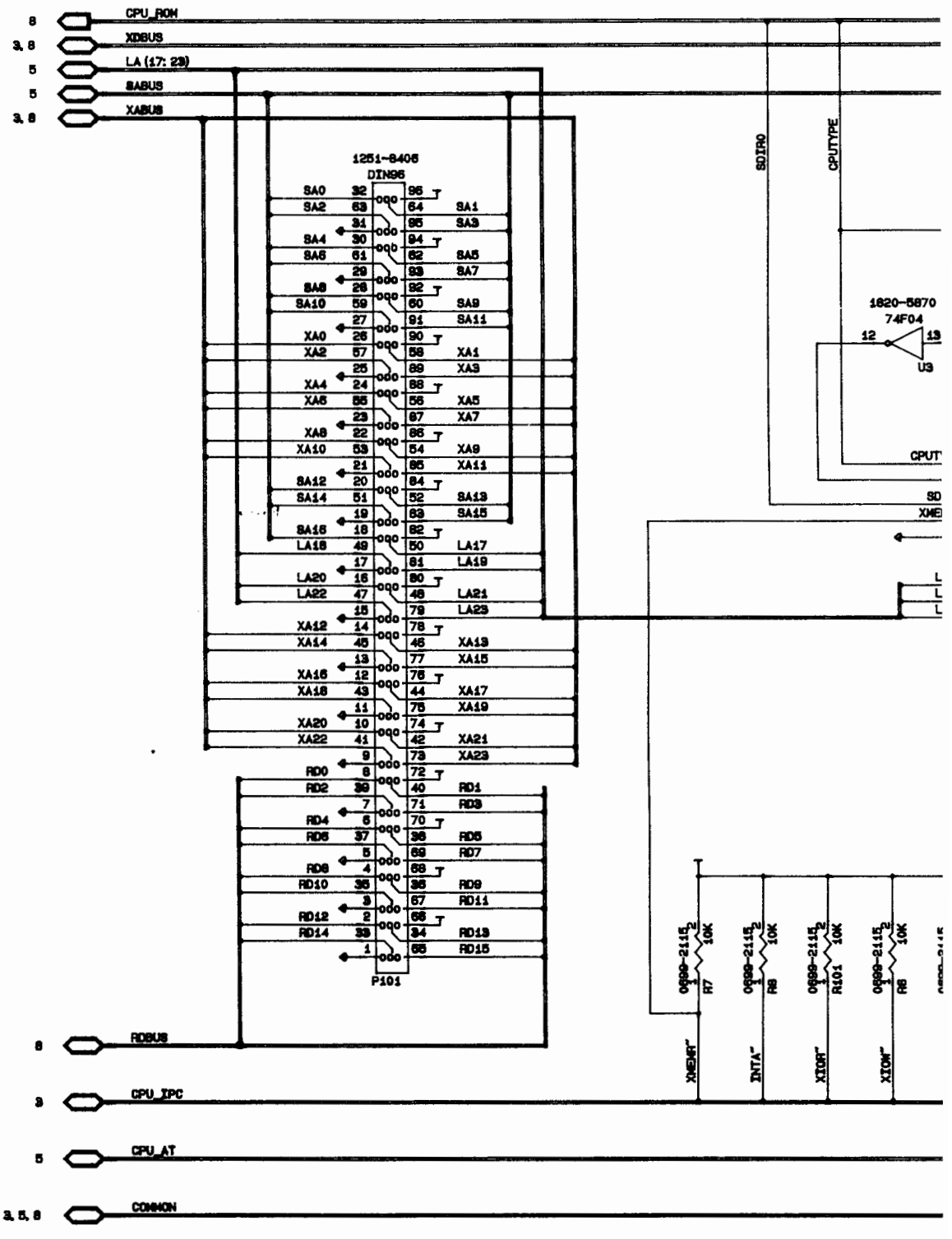
Vectra QS
System Interface PCA
Electrical Schematic

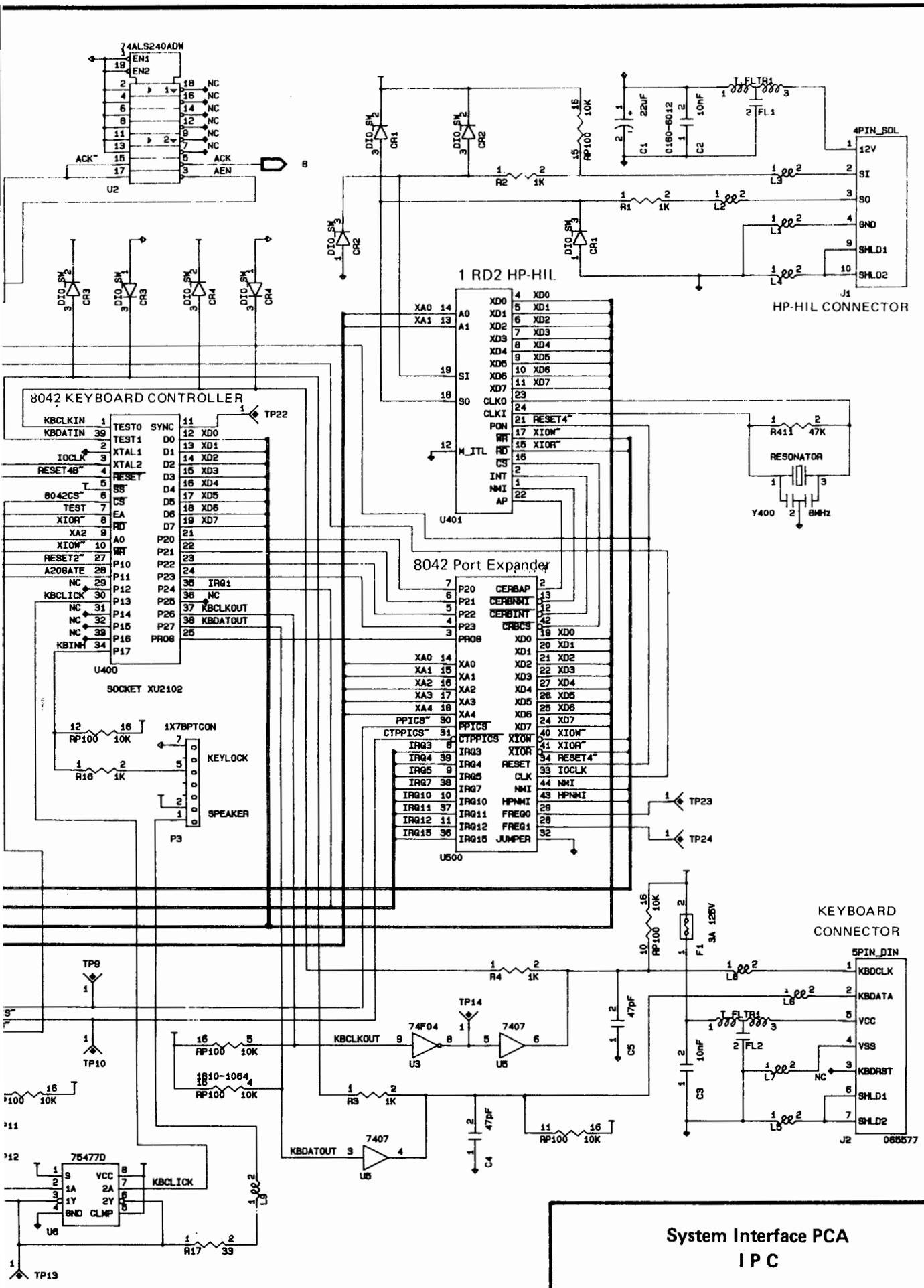

SABUS
CPU_AT
CPU_CON
CPU_IPC
CPU_IPC
XIOR"
SHEET 2
SHEETS 3, 4
RDBUS
CPU_ROM
XABUS
XDBUS
COMMON
COMMON
RDBUS
CPU_ROM
XABUS
XDBUS
COMMON
XIOR"
ACK
ROM
SDBUS
SHEET 8



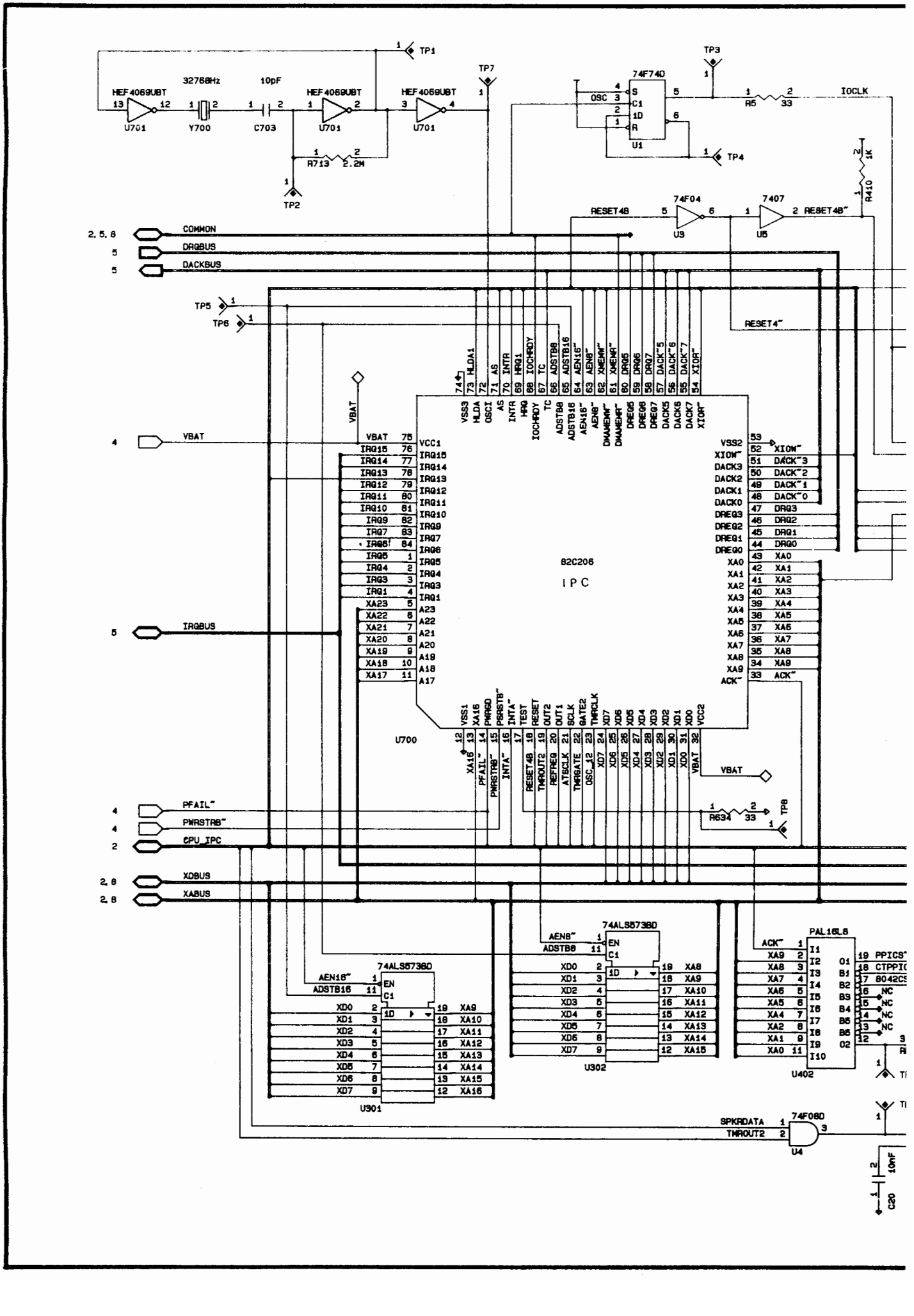
Computer Museum

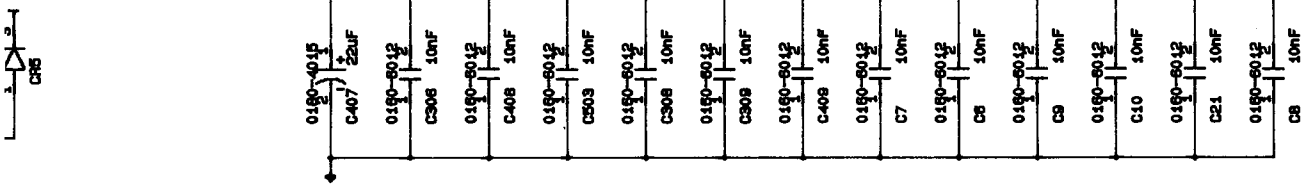
System Interface PCA
CPU Connector

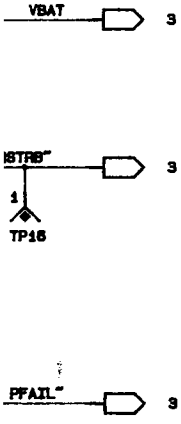

8 CPU_ROM
3, 8 XDBUS
5 LA (17: 23)
5 SABUS
3, 8 XABUS
1251-8406
DIN96
P101
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16
LA17 LA18 LA19 LA20 LA21 LA22 LA23
XA0 XA1 XA2 XA3 XA4 XA5 XA6 XA7 XA8 XA9 XA10 XA11 XA12 XA13 XA14 XA15 XA16
XA17 XA18 XA19 XA20 XA21 XA22 XA23
RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8 RD9 RD10 RD11 RD12 RD13 RD14 RD15
SDIR0
CPUTYPE
1820-5870
74F04
U3
0699-2115
R7
R8
R101
R6
10K
XMEMR"
INTA"
XIOR"
XIOW"
8 RDBUS
3 CPU_IPC
5 CPU_AT
3, 5, 8 COMMON

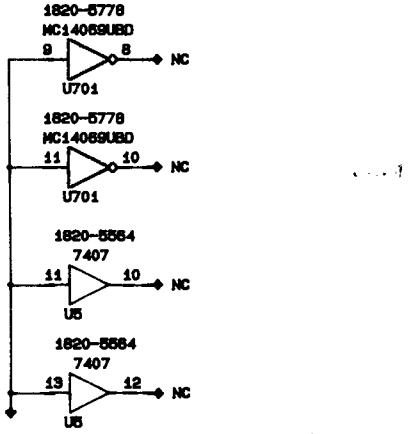


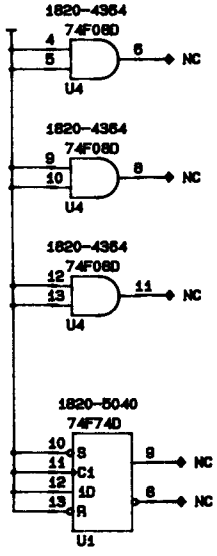
System Interface PCA
I P C


TP1
TP7
TP3
TP2
TP4
TP5
TP6
TP8
32768Hz
10pF
HEF4069UBT
U701
Y700
C703
R713 2.2M
74F74D
U1
OSC
IOCLK
R5 33
74F04
U9
7407
U5
RESET4B
RESET4"
R410 1K
COMMON
DRQBUS
DACKBUS
IRQBUS
VBAT
PFAIL"
PWRSTRB"
CPU_IPC
XDBUS
XABUS
82C206
IPC
U700
R634 33
74ALS573BD
U301
U302
U402
PAL16L8
SPKRDATA
TMROUT2
U4
10nF
C20







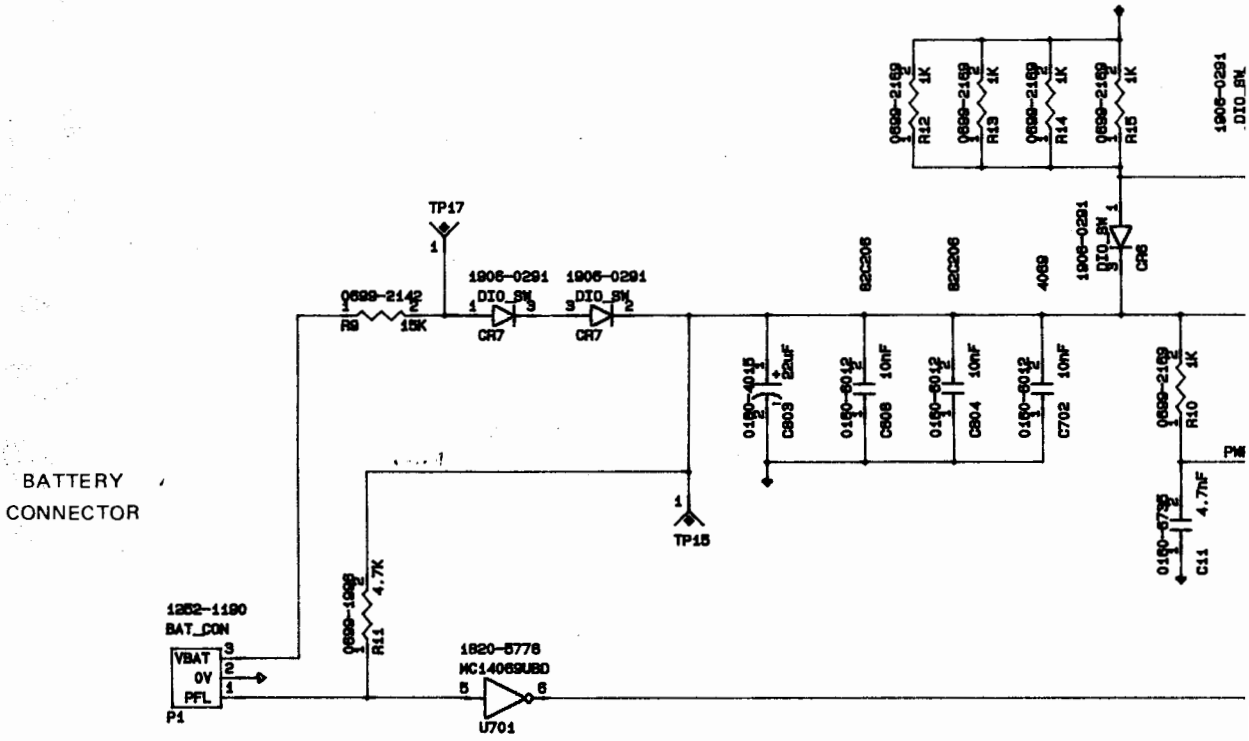


System Interface PCA

I P C

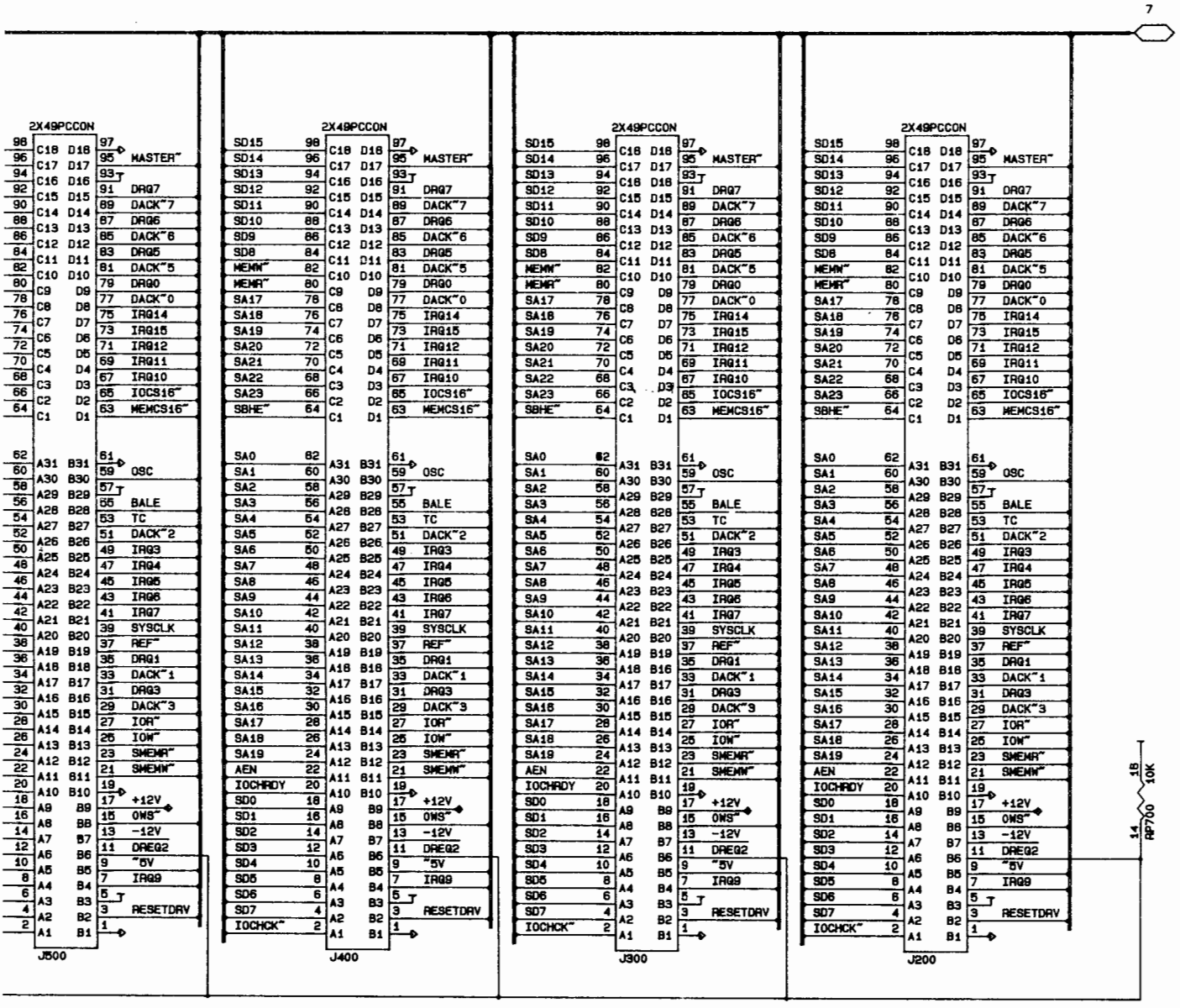
Supply - Decoupling

SHEET 4 OF 8

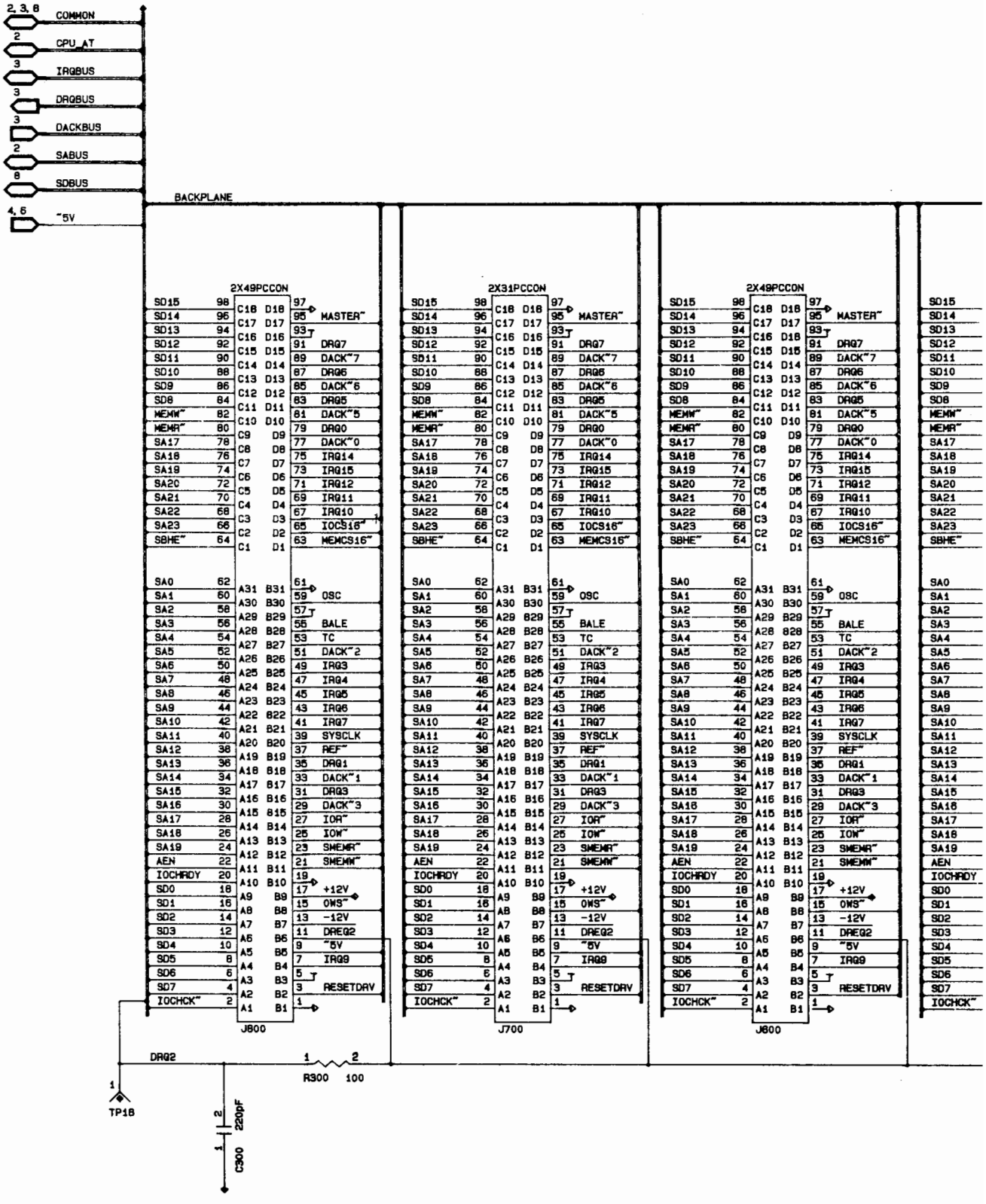


BATTERY
CONNECTOR

POWER CONNECTOR

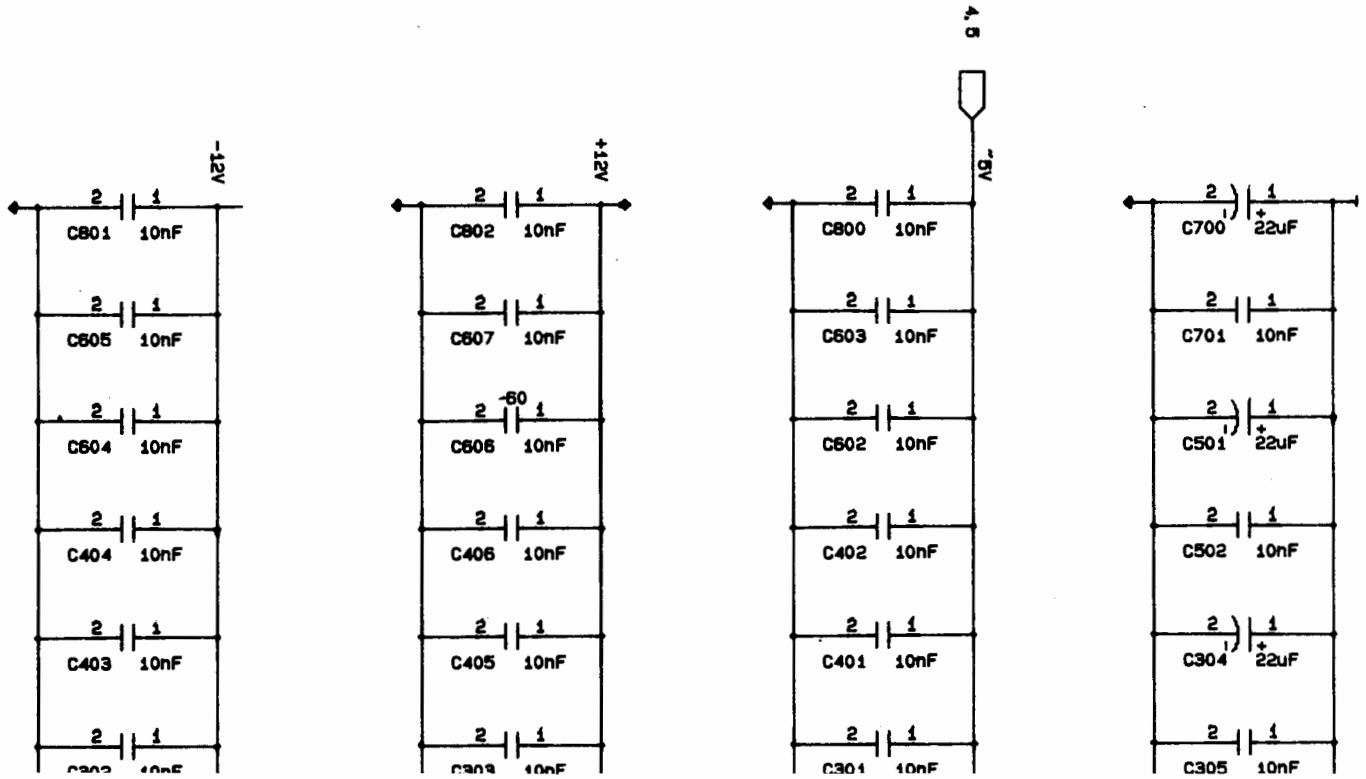


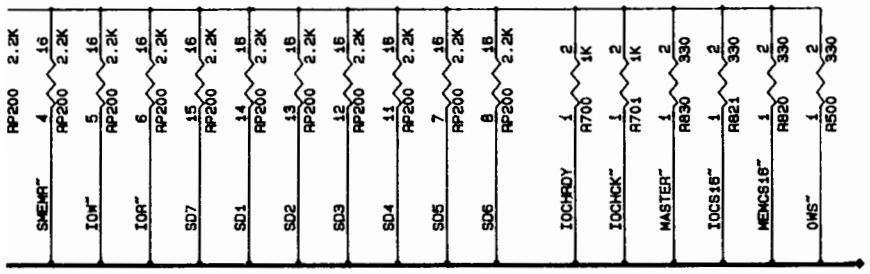
System Interface PCA
AT Connectors

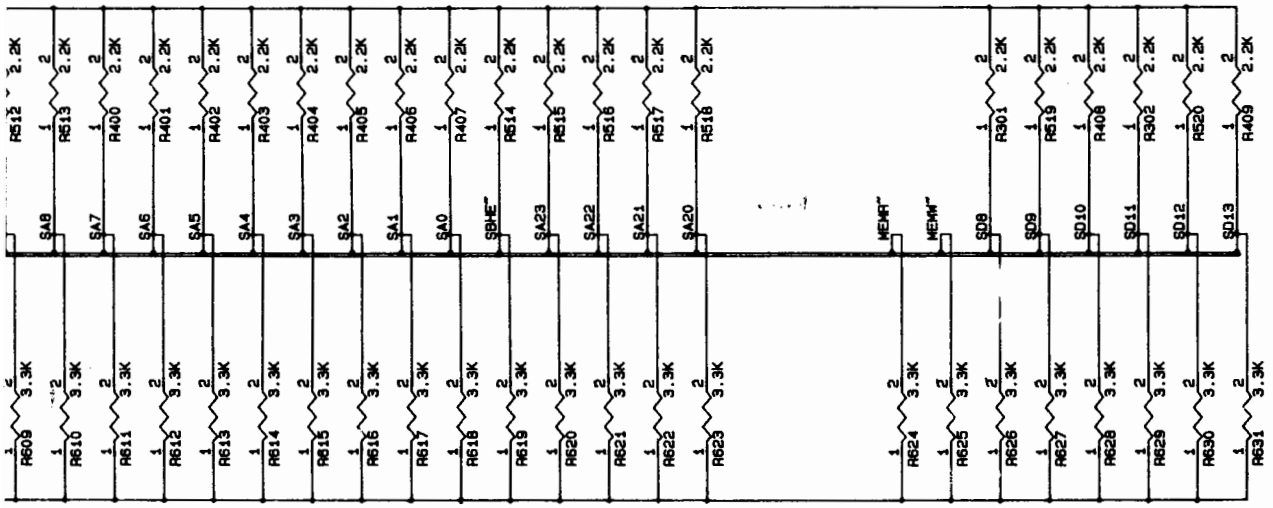

2, 3, 8 COMMON
2 CPU_AT
3 IRQBUS
3 DRQBUS
3 DACKBUS
2 SABUS
8 SDBUS
4, 6 "5V
BACKPLANE
2X49PCCON
2X31PCCON
2X49PCCON
SD15 98 C18 D18 97
SD14 96 C17 D17 95 MASTER"
SD13 94 C16 D16 93
SD12 92 C15 D15 91 DRQ7
SD11 90 C14 D14 89 DACK"7
SD10 88 C13 D13 87 DRQ6
SD9 86 C12 D12 85 DACK"6
SD8 84 C11 D11 83 DRQ5
MEMW" 82 C10 D10 81 DACK"5
MEMR" 80 C9 D9 79 DRQ0
SA17 78 C8 D8 77 DACK"0
SA18 76 C7 D7 75 IRQ14
SA19 74 C6 D6 73 IRQ15
SA20 72 C5 D5 71 IRQ12
SA21 70 C4 D4 69 IRQ11
SA22 68 C3 D3 67 IRQ10
SA23 66 C2 D2 65 IOCS16"
SBHE" 64 C1 D1 63 MEMCS16"
SA0 62 61
SA1 60 A31 B31 59 OSC
SA2 58 A30 B30 57
SA3 56 A29 B29 55 BALE
SA4 54 A28 B28 53 TC
SA5 52 A27 B27 51 DACK"2
SA6 50 A26 B26 49 IRQ3
SA7 48 A25 B25 47 IRQ4
SA8 46 A24 B24 45 IRQ5
SA9 44 A23 B23 43 IRQ6
SA10 42 A22 B22 41 IRQ7
SA11 40 A21 B21 39 SYSCLK
SA12 38 A20 B20 37 REF"
SA13 36 A19 B19 35 DRQ1
SA14 34 A18 B18 33 DACK"1
SA15 32 A17 B17 31 DRQ3
SA16 30 A16 B16 29 DACK"3
SA17 28 A15 B15 27 IOR"
SA18 26 A14 B14 25 IOW"
SA19 24 A13 B13 23 SMEMR"
AEN 22 A12 B12 21 SMEMW"
IOCHRDY 20 A11 B11 19
SD0 18 A10 B10 17 +12V
SD1 16 A9 B9 15 OWS"
SD2 14 A8 B8 13 -12V
SD3 12 A7 B7 11 DREQ2
SD4 10 A6 B6 9 "5V
SD5 8 A5 B5 7 IRQ9
SD6 6 A4 B4 5
SD7 4 A3 B3 3 RESETDRV
IOCHCK" 2 A2 B2 1
A1 B1
J800
J700
J800
DRQ2
1
2
R300 100
1
TP18
2
220pF
1
C300

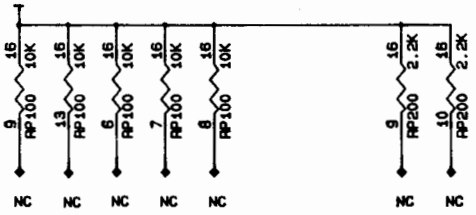
Computer Museum

System Interface PCA
AT Connectors Decoupling

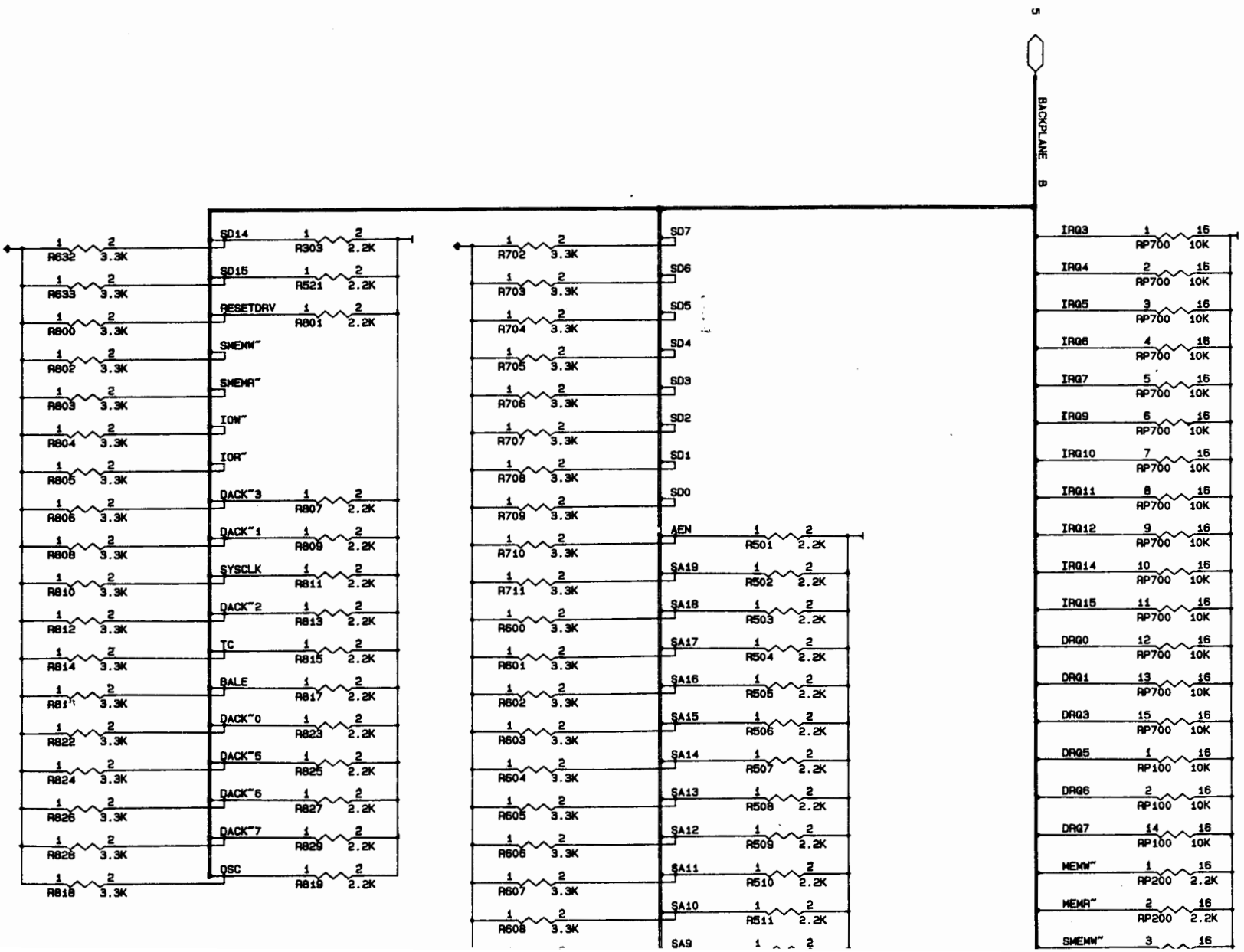

-12V
C801 10nF
C805 10nF
C804 10nF
C404 10nF
C403 10nF
+12V
C802 10nF
C807 10nF
C806 10nF
C406 10nF
C405 10nF
-5V
C800 10nF
C803 10nF
C802 10nF
C402 10nF
C401 10nF
C301 10nF
C700 22uF
C701 10nF
C501 22uF
C502 10nF
C304 22uF
C305 10nF







System Interface PCA
AT Connectors Resistor Networks


BACKPLANE B
SD14
SD15
RESETDRV
SMEMW"
SMEMR"
IOW"
IOR"
DACK"3
DACK"1
SYSCLK
DACK"2
TC
BALE
DACK"0
DACK"5
DACK"6
DACK"7
OSC
SD7
SD6
SD5
SD4
SD3
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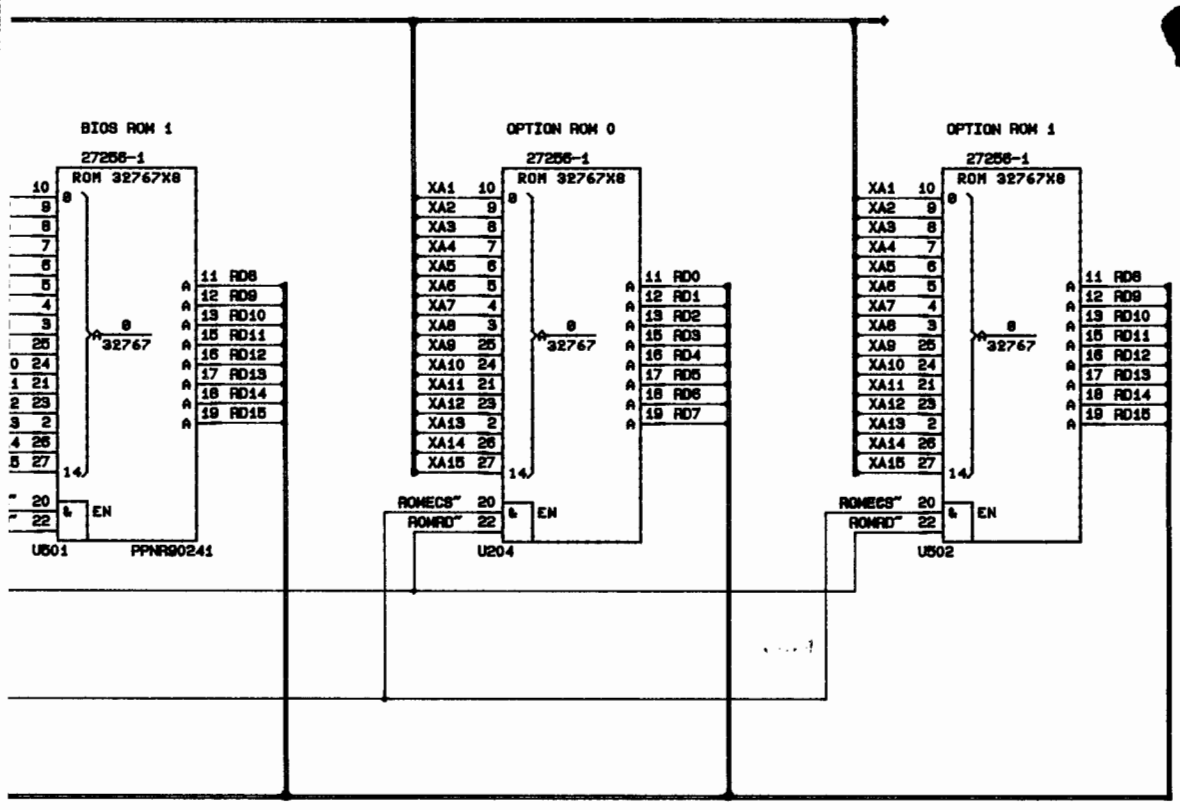

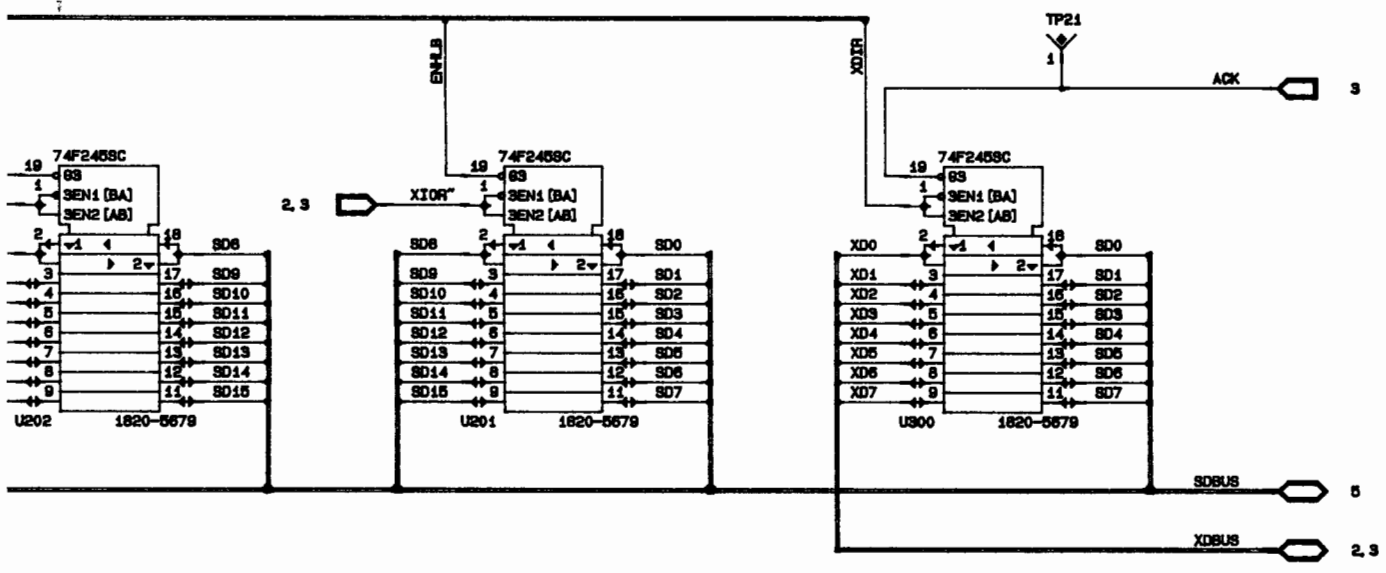

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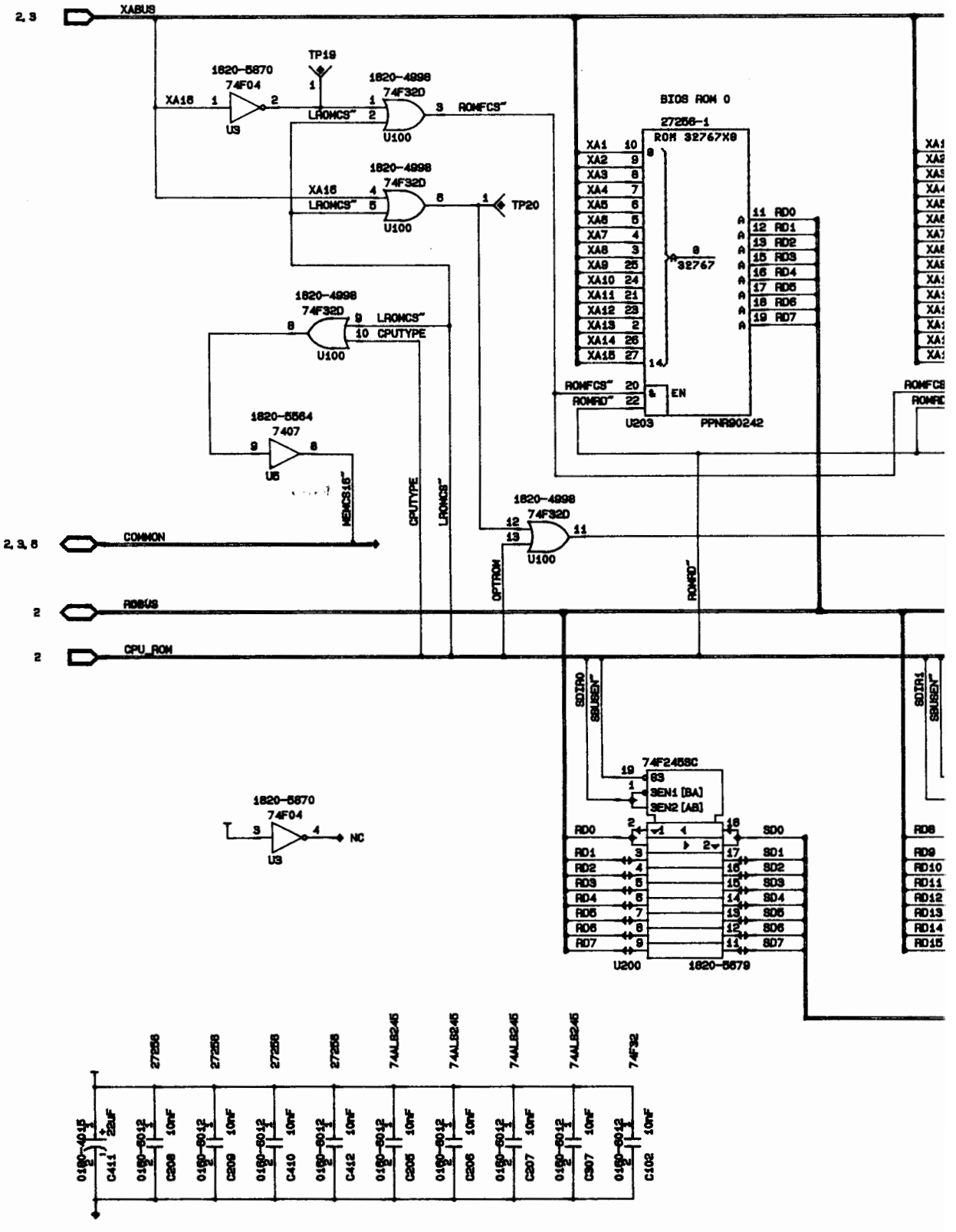
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Glossary

Accessory Card
A circuit board containing electronic circuitry that interfaces a peripheral to the system processor board.

Active Low
Signal that must go low to produce an effect. (Same as negative true.)

Adapter
See Accessory Card.

Address Bus
A circuit that carries a binary-coded address from the 80386 microprocessor to other parts of the system.

Application Software
Software that performs application-specific tasks; examples include word processing packages, spreadsheets, and data bases.

Asynchronous Transmission
A mode of transmitting signals, the start time for which is arbitrary, but the time relationship between signals is fixed.

Barcode Reader
An input device that is used to scan surfaces having barcodes. The barcode reader converts barcodes into scan code data format, and transmits the scan code to an input interface.

Base RAM
The first 640 Kbytes or 512 Kbytes of main memory (depending on the HP Vectra QS PC configuration). Used for MS-DOS applications.

BIOS
Basic Input/Output System. The BIOS is the code module that contains the drivers that constitute the software interface between the hardware, and the system software and application software.

Bisynchronous
Binary Synchronous. A mode of transmission in which binary characters are synchronized via control signals.

Bits Per Second
A unit of measure; the rate at which a device transmits characters serially.

Block
A group of characters or words treated as a unit.

Boot
The process of initializing the system and loading system software after a reset.

Break Code
The code that is sent by the keyboard to the keyboard controller when a key is released, after having been pressed. For most, but not all keys, the break code consists of hex F0, followed by the key's make code.

BTU
British Thermal Units. A measure of heat.

Buffer
(1) A unit that serves as an interface between dissimilar elements, or (2) a register that temporarily holds input or output data, or (3) a memory area that temporarily holds a block of data waiting to be processed.

Bus
A circuit that transmits data or power.

CAS
Column Address Strobe. A signal that latches a column address into dynamic memory.

Central Processing Unit (CPU)
As used in this manual, the 80386 microprocessor.

Channel
A path for sending signals and data.

Character
A word returned by the keyboard driver indicating a key stroke. The code for a character consists of a keyboard scan code, and either an Extended character (00h) or a character in ASCII (the American Standard Code for Information Interchange).

Checksum
An error-checking protocol used to verify the integrity of a block of data or code. Each byte or word in the block is summed, and then added to a Checksum Byte. The block of data or code is presumed valid if this sum equals a predefined value, usually 0.

Checksum Byte
A byte added to the sum of a block of code or data to produce a valid sum.

CMOS
Complementary metal-oxide semiconductor, a type of technology that uses integrated field-effect transistors in a complementary, symmetrical arrangement and needs a relatively low supply current.

CMOS RAM
Random-access memory that is powered by either the system power supply or a battery. When the system power is turned off, the contents of the CMOS RAM are preserved by the battery.

Code Segment
The segment address of the code module currently being executed.

Coprocessor
An add-on processor that works with the 80386 microprocessor, providing the hardware to perform numeric functions otherwise performed in software.

CPU
Central Processing Unit (the 80386 microprocessor).

Cursor Control Keypad
The keypad in between the typewriter keypad and the numeric keypad, which controls the position of the cursor.

Daisy Chain
A method of linking devices together in a serial configuration. If more than one HP-Human Interface Link (HP-HIL) input device is used, they are connected in a daisy chain.

Device
A physical piece of hardware, for example a mouse, keyboard, or printer.

DIN
Acronym for Deutsche Industrie Normenausschuss, a West German association that determines electrical standards. A DIN connector meets the DIN specifications.

Direct-Memory Access
A method for I/O devices to obtain direct access to the main memory, in order to transfer data, without involving the central processing unit.

Divide-By-Zero Interrupt
The 80386 microprocessor executes this interrupt any time a divide-by-zero operation is attempted.

DMA
See Direct-Memory Access.

DOS
Disc Operating System. The software that provides an interface between the hardware, the applications programs, and user-issued commands.

DRAM
See Dynamic RAM.

DREQ
Direct-memory access request.

Driver
(1) A physical device used to control other circuits or simultaneously drive several circuits (usually has a high output current). (2) A program, accessed by interrupt vectors, that executes other programs to perform specific functions, which may be divided into subfunctions.

Dynamic RAM
Dynamic Random-Access Memory. (Also known as Main Memory, Memory, RAM, System Memory, or System RAM. Not to be confused with CMOS RAM.) Dynamic RAM uses transistors and capacitors, the latter which must be recharged (refreshed).

EPROM
Erasable Programmable Read-Only Memory. The devices used to store (and erase, if necessary) the industry-standard BIOS code and the HP extensions to the BIOS code.

EX-BIOS
Extended BIOS. A set of proprietary HP drivers that provide support for various system features.

Fixed Disc Drive
See Hard Disc Drive.

Flexible Disc Drive
Synonymous with floppy disc drive. A unit with a removable magnetic disc for storing and retrieving data.

Function Keys
The twelve industry-standard keys labeled F1 through F12 on the keyboard.

Functions
Code modules within a driver that perform specific tasks. Individual driver functions are selected when a driver is called.

Gate
A combination logic circuit with one or more input channels and one output channel. The output is determined by the state of the input channels.

Gigabyte
One thousand megabytes, or one million kilobytes (10^9).

Graphic Input Device
An input device that generates positional and/or button state data. A mouse, and tablet, are examples of graphic input devices.

Graphics Tablet
A graphic input device that includes a electronic tablet and pen that feed figures or text into the computer. When the graphics pen touches the graphics tablet, a detector registers the coordinates of that point. These coordinates, encoded into binary, generate pulses that are sent to the computer.

Hard Disc Drive
Synonymous with fixed disc drive. A unit with a non-removable magnetic disc for storing and retrieving data.

Hardware Interrupts
Requests for interrupt service, generated by the hardware components.

Hex
Hexadecimal numbers. Hex numbers represent binary data; they are expressed in base 16 and are represented with numbers 0 to 9 and letters A to F. Throughout this manual, hex numbers are indicated with an lower-case "h" as their last character (i.e., 17h).

HP-Human Interface Link (HP-HIL)
The electrical interface and communication protocol utilized to connect HP-HIL input devices.

HP-Human Interface Link Master Link Controller
The hardware that provides the electrical interface to the HP-HIL link and which supervises the communication protocol.

HP-IB
Hewlett-Packard Interface Bus

Hz
Hertz. A unit of frequency equal to one cycle per second.

Industry-Standard
Compatible with IBM AT personal computers.

Instruction Pointer
The offset from the base of the code segment of the next instruction to be executed.

Instruction Set
A structured set of instructions that concern characters and program definitions, transferred to the computer as operations are executed.

Interrupt of 80386 Microprocessor
A signal which temporarily suspends the 80386 microprocessor's normal execution of a routine, in response to error conditions or processor exceptions.

Interrupt Service Routine (ISR)
Consists of a code module (a group of related instructions for the 80386 microprocessor) and the code module's associated data structure(s), (a related group of data fields) that respond to a hardware interrupt.

Interrupt Vector
A data structure (related group of data fields) used by the 80386 microprocessor to branch to a service routine or an interrupt. Interrupt vectors are located in the first 1024 bytes of system memory. Each interrupt vector occupies two words of memory and includes the interrupt service routine's instruction pointer and code segment.

IPC
The 82C206 Integrated Peripheral Controller.

Kbyte
A Kilobyte, a measurement of the physical storage capacity. One Kilobyte equals 1,024 bytes.

Keyboard
The physical keyboard.

Keyboard Controller
The 8042 keyboard controller. The 8042 provides industry-standard keyboard compatibility, and serves as a buffer between the STD-BIOS keyboard drivers and the Input System.

Keylock
The lock on the front of the HP Vectra QS PC's System Processing Unit, which when locked, inhibits inputs from the keyboard or other input devices also locks on the SPU's back, which prevents the SPU unit cover from being removed.

LED
Light-emitting diode. A semiconductor device that is lit when activated.

MA
Memory Address bus.

Main Memory
See Dynamic RAM.

Make Code
The code that is sent by the keyboard to the system's keyboard controller when a key is pressed.

Mask
A mask consists of characters that retain or eliminate bits comprising a string (i.e., a set of records) that is stored in memory.

Mbyte
A measurement of the physical storage capacity. One Megabyte equals 1,048,576 bytes, or 1,024 kilobytes. (See Kbyte).

MD
Memory Data bus.

Memory
Main Memory. (See Dynamic RAM.)

Microprocessor
A control unit that accepts a defined set of instructions for execution.

MLC
Master Link Controller.

Mode-Indicator LEDs
The LEDs located on the keyboard that indicate the state of the Caps lock, Num lock, and Scroll lock keyboard modifiers.

Mouse
A graphic input device that reports relative motion coordinates based on its motion. A mouse will also report the state of its buttons.

MS-DOS
See DOS.

Multiplex
The simultaneous transmission of two of more information streams over the same channel.

Multi-Tasking
The ability of a system microprocessor (such as the 80386) to perform multiple tasks nearly simultaneously. By task-switching (quickly dividing the microprocessor's execution time between different tasks), the illusion of simultaneous execution occurs.

NMI
Non-maskable interrupt, an 80386 interrupt line used to report system error conditions. This interrupt is mapped by the 80386 microprocessor to interrupt vector 02h.

Numeric Keypad
The keypad on the far right of the keyboard, that has keys with numbers and symbols. The numeric keypad can be used for numeric entries only when the Num Lock key has been pressed and the <Num Lock> mode-indicator LED is lit. (Otherwise, this keypad functions the same as the cursor control keypad.)

Operating System
The system software that provides access to system resources for application programs. The operating system manages input and output, data and program files, and system memory.

Page
A block of consecutive-byte memory.

Parallel Port
A system I/O port that transmits and receives data a byte at a time. Parallel ports are typically used to interface to printers.

Parity Bit
In the odd parity system used for the HP Vectra QS PC, a bit added to a group of bits, to make an even number of ones sum up to an odd number.

Parity Check
A method for checking if the total number of ones or zeros in a byte or word is even or odd.

PCA
Printed Circuit Assembly.

Polling
The process of periodically determining the status of a device. Polling is used to determine if peripheral devices have data or are ready to accept data in non-interrupt driven systems.

Port
A point at which an input or output contacts with the central processing unit.

Power-On Self-Test
A self-test process that is executed each time the system is powered on when a hard reset occurs.

Processor
See Central Processing Unit and Microprocessor.

RAM
Random Access Memory. See Dynamic RAM.

RAS
Row Address Strobe. A signal that latches a row address into dynamic memory.

RD
Read-only memory Data bus.

Read-Only Memory (ROM)
Read-only memory is memory the contents of which can not be altered. When power is removed from the system, this memory retains its contents.

Real-Time Clock
A clock circuit that maintains the correct time whether the system is on or off. The real-time clock is powered by either the system power supply or the battery. When the system power is turned off, the clock continues to operate from the battery.

ROM
See Read-Only Memory.

ROM BIOS
The set of EX-BIOS and STD-BIOS drivers. These code modules are contained in ROM on the System Interface PCA.

SA
System Address bus.

SBUS
Backplane I/O Bus.

Scan Codes
Codes returned by the keyboard to the 80386 microprocessor to indicate key presses (makes) and releases (breaks).

SD
System Data bus.

SDLC
See Synchronous Data Link Controller.

Serial Port
A system I/O port that transmits data *serially;* i.e., one bit at a time.

Single Step Interrupt
An interrupt of the 80386 microprocessor, generated after each instruction if the Single Step flag is set. This interrupt is mapped by the 80386 to interrupt vector 01h.

Software Interrupt
An interrupt generated by an 80386 INT n instruction, where "n" is the interrupt number.

SPU
System Processing Unit. The physical container for the system's power supply, disc drives, printed circuit assemblies, etc.

STD-BIOS
The set of drivers that execute the industry-standard BIOS functions.

Synchronous Data Link Controller
An industry-standard card/protocol used for linking minicomputers with industry-standard mainframes.

Synchronous Transmission
(1) A mode of transmitting signals, in which each signal has a fixed time frame. (2) The sending of signals at the same frequency and phase relationship.

System Memory
See Dynamic RAM.

System RAM
See Dynamic RAM.

System Software
See Operating System.

Timer Tick
An interrupt generated by the system timer.

Typematic
Except for the Pause key, all keys are *typematic.* That is, when a key is pressed and held down, the keyboard continues sending the key's make code to the keyboard controller, repeating the key's function until the key is released.

Typematic Delay

The amount of time a key must be held down, before the keyboard enters the typematic or repeat mode. The typematic delay equals:

```
[(1 + binary value of bits 6 and 5 of the parameter byte)  X
(250 milliseconds)] +/- 20%
```

Typematic Rate

The rate (1/period) at which make scan codes are sent by the keyboard when the keyboard is in the typematic, or repeat, mode. The period, the interval from one typematic output to the next, equals:

```
[8 + (the binary value of bits 2, 1, and 0 of the
parameter byte)]  X

[2 raised to the power of the binary value of bits 4 and
3 of the parameter byte]  X

0.00417 seconds
```

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