HEWLETT-PACKARD

HP Vectra Accessories Technical Reference Manual

NOTE

The information contained in this document is subject to change without notice.

Hewlett-Packard makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Hewlett-Packard assumes no responsibility for the use or reliability of its software on equipment that is not furnished by Hewlett-Packard.

Vectra is a U.S. registered trademark of Hewlett-Packard Company
MS-DOS is a U.S. registered trademark of Microsoft, Incorporated
IBM is a U.S. registered trademark of International Business Machine Corporation.
Intel is a U.S. registered trademark of Intel Corporation.

Personal Office Computer Division
974 East Arques Avenue
P.O. Box 486
Sunnyvale, CA 94086, U.S.A.

Part number: 5959-6759

First Edition - May 1988

Printed in U.S.A.

HP Computer Museum
www.hpmuseum.net

For research and education purposes only.

HP Vectra Accessories Technical Reference Manual

WARNING

Electrical Safety. For the user's safety, the power cords supplied with this product have grounded plugs. The power cords should be used with properly grounded (3-hole) wall outlets to avoid electrical shock. (You can also use multiple-outlet strips that have their own circuit breakers.)

FCC Statement

WARNING

This equipment has been certified to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception.

More About Radio and Television Interference

Because the HP Vectra PC generates and uses radio frequency energy, it may cause interference with radio and television reception in a residential installation.

Hewlett-Packard's system certification tests were conducted with HP-supported peripheral devices and HP shielded cables, such as those you receive with your system. The HP Vectra PC meets the requirements for a Class B computing device in accordance with the specifications of Part 15, Subpart J, of protection against interference with radio and television reception in a residential installation.

Hewlett-Packard provides instructions for using this computer in manuals covering setup, connection of peripheral devices, operation, service, and technical reference.

Installing and using the computer in strict accordance with Hewlett-Packard's instructions will minimize the chances that the HP Vectra PC will cause radio or television interference. However, Hewlett-Packard does not guarantee that the computer will not interfere with radio and television reception. If you think your computer is causing interference, turn it off to see if the radio or television reception improves. If the reception:

- Does not improve, your computer is not causing the problem.
- Does improve, your computer is causing the problem.

To correct interference, take one or more of the following steps:

- Relocate the radio or television antenna.
- Move the computer away from the radio or television.
- Plug the computer into a different electrical outlet, so that the computer and the radio or television are on separate electrical circuits.
- Make sure that all of your peripheral devices are certified Class B by the FCC.
- Make sure you use only shielded cables to connect peripheral devices to your computer.
- Consult your computer dealer, Hewlett-Packard, or an experienced radio/television technician for other suggestions.
- Order the FCC booklet called How to Identify and Resolve Radio-TV Interference Problems for the U.S. Government Printing Office, Washington, D.C. 20402.

Contents

Contents

Chapter 4
Disc and DataComm Controller Card

Chapter 5
Four-Function Controller PCAs

Contents

Chapter 6
Dual RS232/422 Interface Card

Chapter 7
Serial/Parallel I/O Card (24540A)

Chapter 8
Multimode Video Adapter Card

Chapter 9
Accessory Cables

1

INTRODUCTION

This manual covers accessories for the Hewlett-Packard Vectra line of computers. Each of the accessories is covered in a separate chapter, and includes tables of all registers including bit definitions.

I/O Channel Connectors

Figure 1-1 shows the pinout of the standard I/O channel connector. Most of the accessories in this manual use a subset of these pins, as required, for their particular application. For detailed information on these connectors in each specific system, refer to the appropriate technical reference manual.

Figure 1-2 shows the dimensions of the industry standard backplane I/O expansion cards.

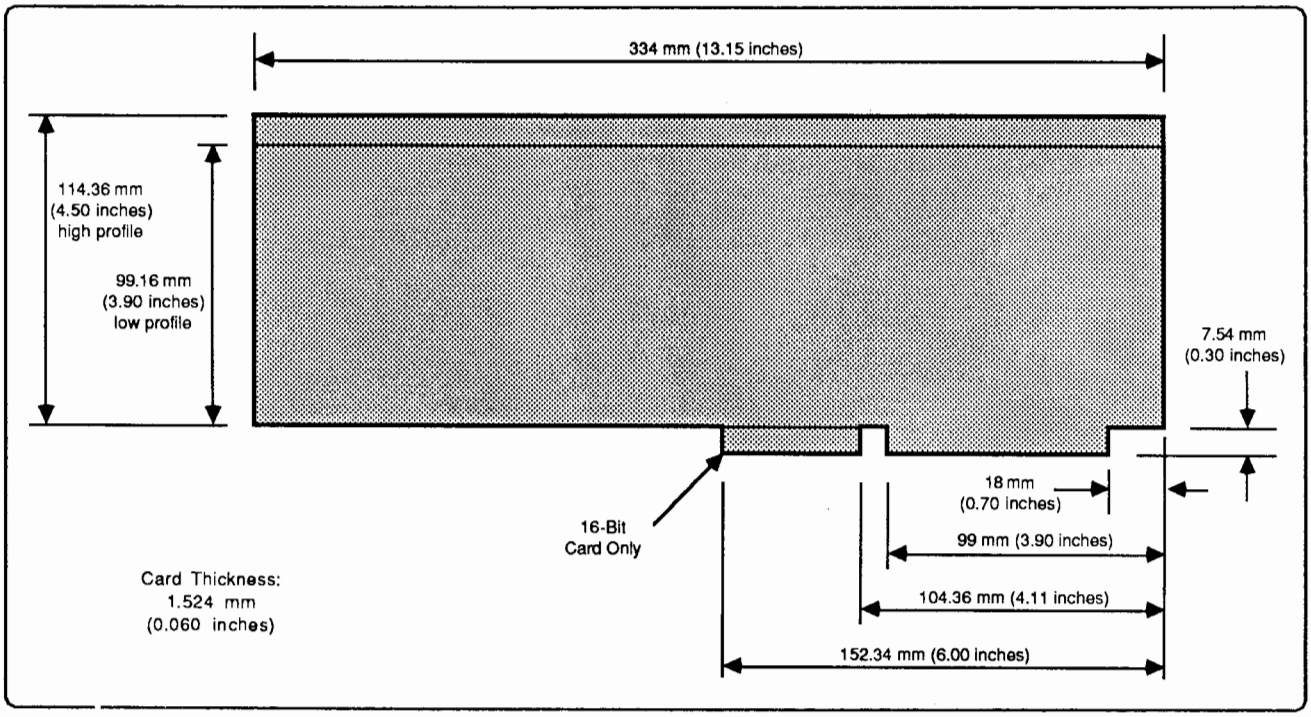


Figure 1-2. I/O Card Dimensions

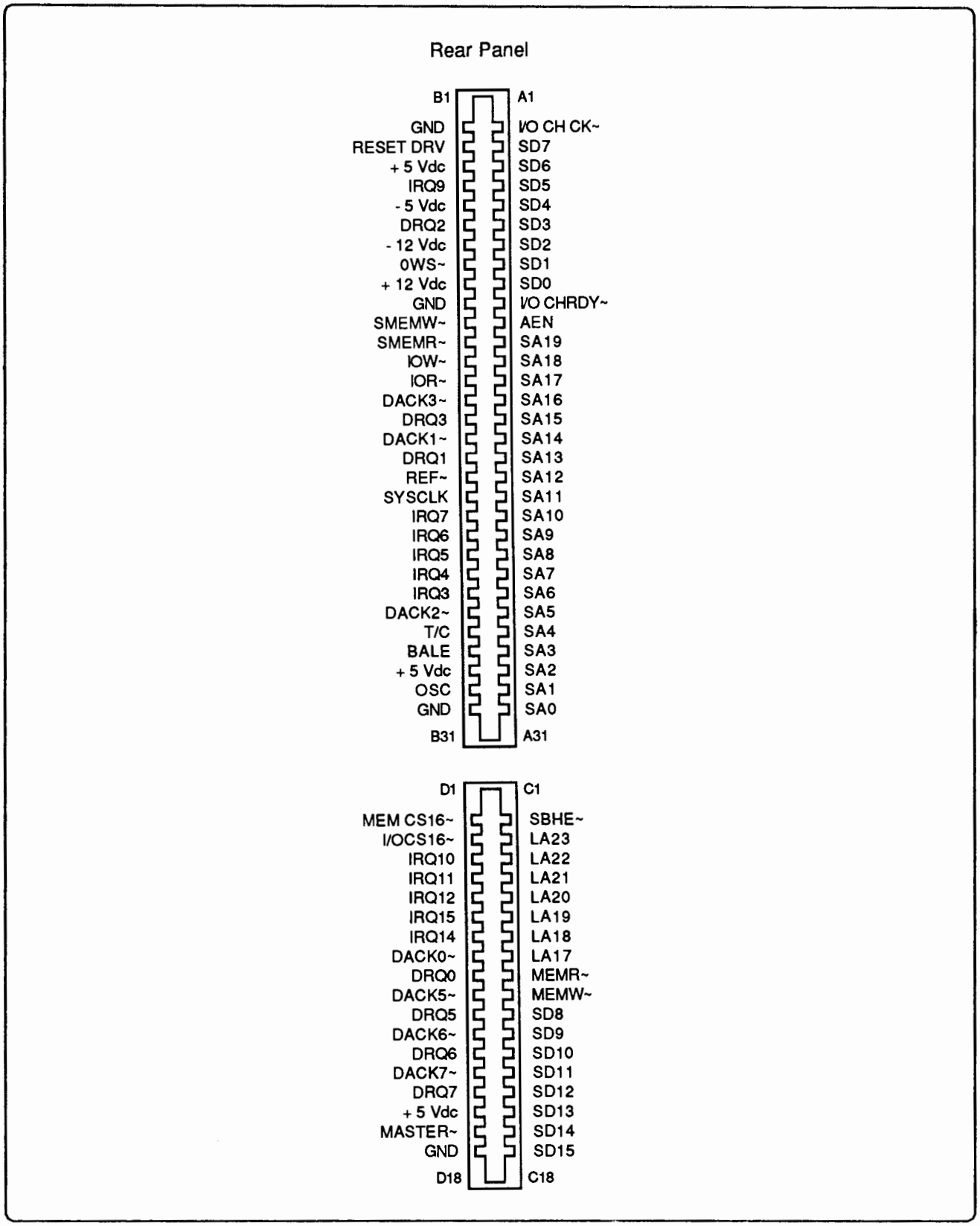


Figure 1-1. I/O Channel Connectors

Table 1-1 gives the pin assignments for the backplane I/O connectors. The "~" (tilde) symbol is used after the signals that are defined as active low.

Table 1-1. I/O Channel Connector Assignments

Signal Name	Description
AEN	This signal is used to inform the system that the DMA controller has control of the address and control buses. This signal is active during DMA transfers.
BALE	This is the buffered ALE signal. Its falling edge indicates valid address and control signals. BALE is forced high during DMA cycles.
DACK0-3~, DACK5-7~	These signals are used by the processor board to acknowledge DMA requests. They are active low.
DRQ0-DRQ3, DRQ5-DRQ7	These lines are used by accessory cards to request DMA service or to gain control of the system. The DMA channels are prioritized with Channel 0 having the highest priority and channel 7 having the lowest. The signal must be held high until its corresponding acknowledge signal is asserted.
I/O CHCK~	This signal is used by an accessory card to indicate to the system that an error has been detected on the card. This signal is active low.
I/O CHRDY	This signal is used to synchronize slow memory or I/O devices during read and write operations. If an accessory card needs to extend a read or write operation, it should pull this line low as soon as a valid address and a read or write command is detected. A read or write operation should not be extended to more than 15 SYSCLK cycles. Clock cycles added via this signal are in addition to any added by the system.
I/O CS16~	This signal is used to indicate to the system that the accessory card can perform 16-bit I/O operations. The driver should be an open collector or a tri-state device capable of sinking 20ma.
IOR~	This signal indicates an I/O read cycle is in progress. IOR~ may be driven by a DMA controller or by an external microprocessor (if MASTER~ is asserted). This signal is active low.
IOW~	This signal indicates an I/O write cycle is in progress. IOW~ may be driven by a DMA controller or by an external microprocessor (if MASTER~ is asserted). This signal is active low.
IRQ3-IRQ7, IRQ9-IRQ12, IRQ14,IRQ15	These signals are used by accessory cards to signal request for interrupt service. The signals are edge sensitive, and are asserted by a low-to-high transition. The signal must be held high until the interrupt is acknowledged. The signals are prioritized; the following list gives their relative priorities starting with the highest: IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7

Table 1-1. I/O Channel Connector Assignments (Cont.)

Signal Name	Description
LA17-LA23	These are the upper system address lines. When combined with SA0-SA19 they produce 16 Mbytes of memory address space. These signals are latched by the adapter card on the trailing edge of BALE. LA17-LA23 may be driven by a DMA controller on the I/O channel (if MASTER is asserted).
MASTER~	This signal is used by an accessory card to disable the 80286 and gain control of the system buses. In order to gain control, one of the DMA channels must be placed in the cascade mode, and the accessory card must issue a DRQ request and receive a DACK acknowledge. The accessory card may then assert MASTER and gain control of the system. It must wait one clock cycle before attempting to drive the address or data lines, and two clock cycles before issuing a read or write command. Holding this signal low for 15 us or more may cause a loss of memory due to the absence of refresh (unless master card asserts REF).
MEM CS16~	This signal is used to indicate to the system that the accessory card can perform 16-bit memory operations. The driver should be an open collector or a tri-state device capable of sinking 20ma. This signal should be derived from LA17-LA23.
OSC	This is a 14.318 MHz timing reference signal. It has a 50% duty cycle and a period of approximately 70 ns. This signal is asynchronous to the system clock SYSCLK.
REFRESH~	This signal indicates a memory refresh operation is in progress. This signal may be driven by a processor on the I/O channel (if MASTER is asserted). This signal is active low.
RESET DRV	This signal is used to reset all system devices during power-on resets and indicates low line voltage conditions. The signal is active high.
SA0-SA19	These are the system address lines. When combined with LA17-LA23 they produce 16 Mbytes of memory address space. SA0-SA19 begin to change on the rising edge of BALE, and are latched for the duration of the cycle by the falling edge of BALE. SA0-SA19 may be driven by a DMA controller or processor on the I/O channel (if MASTER is asserted). The system refresh controller places the refresh address on SA0-SA7 during refresh cycles.
SBHE~	This signal indicates that data will be transferred on SD8-SD15. SBHE~ indicates a 16-bit transfer or an 8-bit transfer to an odd address (A0 = 1) is in progress.
SD0-SD15	This is the system data bus. Data is transferred to and from the system on these lines. Sixteen-bit transfers occur on SD0-SD15. Eight-bit transfers occur on SD0-SD7, unless SBHE~ is asserted. In which case, data is transferred on SD8-SD15. Sixteen-bit to 8-bit transfers are multiplexed by the backplane state machine into two 8-bit transfers on SD0-SD7.

Table 1-1. I/O Channel Connector Assignments (Cont.)

Signal Name	Description
SMEMR~, MEMR~	These signals indicate a memory read cycle is progress. MEMR~ may be driven by a DMA controller or by an external microprocessor (if MASTER~ is asserted). SMEMR~ is active if MEMR~ is active and the address decode circuit indicates a valid address in the bottom 1 Mbyte of memory space. Both of these signals are active low.
SMEMW~, MEMW~	These signals indicate a memory write cycle is in progress. MEMW~ may be driven by a DMA controller or by an external microprocessor (if MASTER is asserted). SMEMW~ is active if MEMW~ is active and the address decode circuit indicates a valid address in the bottom 1 Mbyte of memory space. Both of these signals are active low.
SYSCLK	This is the processor system clock. It has a period of approximately 125 ns for 8 MHz cycles and 83 ns for 12 MHz cycles. This signal can be used to synchronize activities to the 80286.
T/C	This signal informs the system that the terminal count for one of the DMA channels has been reached. The signal is active high.
0WS~	This signal indicates to the system that a read or write operation can take place without additional system generated wait states. To perform a 16 bit memory cycle with zero wait states, this signal should be asserted as soon as a valid address decode and a read or write command is detected. To shorten cycles for 8-bit devices, 0WS~ should be asserted on the falling edge of SYSCLK after detecting a valid address and a read or write command for one wait-state. If asserted on the second falling edge of SYSCLK after detecting a valid address and a read or write command, two wait-states will be generated for 8-bit devices. The driver should be an open collector or a tri-state device capable of sinking 20ma.

References

The following documents should be used for detailed information about components and functions discussed in this manual.

Chips and Technologies 82A and 82C-series technical reference documents
--Discusses the I/O devices (8237A, 82284, 8254, 8259, MC146818)
--Discusses the overall architecture

HP-HIL Technical Reference Manual
--Discusses the HP-HIL interface

HP Vectra Accessories Technical Reference Manual
--Discusses the BIOS ROM

HP Vectra MS-DOS Macro Assembler
--Reference for the assembler.

HP Vectra MS-DOS Programmer's Reference Manual
--Discusses programming of the CPU using MS-DOS.

HP Vectra MS-DOS User's Reference Manual

HP Vectra System BIOS Technical Reference Manual
--Discusses the BIOS ROM

INTEL iAPX286 Hardware Reference Manual
--Discusses the 80286 processor.

INTEL iAPX286 Programmer's Reference Manual
--Reference for the 80286 instruction set and architecture.
--Reference for the 80287 numeric processor.

INTEL Microcontroller Handbook

INTEL Microprocessor and Peripheral Handbook, Volume I
--Discusses the 80286.
--Discusses the 80287.

INTEL Microsystem Components Handbook, Volume II
--Discusses the 8042 keyboard controller chip.

INTEL 8086 Family User's Manual

Motorola Single Chip Microcomputer Data, Section C
--Discusses the MC146818 real-time clock/ CMOS chip.

The Peter Norton Guide to the IBM PC by Peter Norton, Microsoft Press.

Writing MS-DOS Device Drivers by Robert S. Lai, Addison-Wesley Publishing Co.

2

Keyboard

There are two versions of the keyboard provided for the Vectra line of computers. The interface to the keyboards is either through the HP-HIL interface or through the industry standard DIN connection.

HP-HIL is the Hewlett-Packard proprietary standard for interfacing one or more input devices to the system. HP-HIL provides an asynchronous serial communication protocol that enables the user to select a set of input devices (up to seven), and connect them to the HP Vectra without purchasing additional I/O cards or using additional I/O slots. Cable management is simplified because the various input devices are "daisy-chained" from the HP Vectra.

The DIN connector interface conforms to the industry standard and allows other keyboards to be plugged into the system. Note that this is not recommended since HP does not support other keyboards, and cannot assure that the key codes and timing conform to the codes of the HP keyboards. Coverage of the HP-HIL and DIN interface inside the HP Vectra computers is provided in their respective SPU Technical Reference Manuals.

DIN Keyboard Interface

The DIN keyboard interface is provided with an industry-standard DIN connector as shown in Figure 2-1. Data are sent over the serial data line from the keyboard to the system in a serial data stream, the format conforming to the industry-standards. Table 2-1 provides a listing of the scan codes output by the DIN keyboard when the keys are pressed or released.

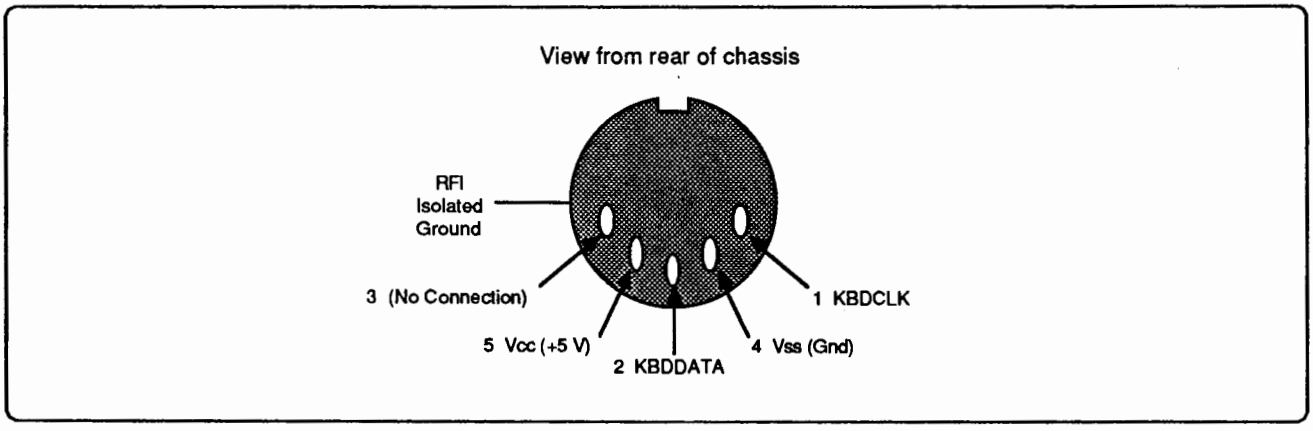


Figure 2-1. Keyboard Connector Pin Assignments

Data received from the keyboard contains a series of hex scan codes, depending on which of the keyboard keys is pressed. The data corresponds to the values shown in Table 2-1. The Vectra ES is designed to be compatible with either of the keyboards shown in Figure 2-2. Figure 2-3 shows the key numbers which are referenced in Table 2-1.

For a detailed description of the keyboard software interface refer to the *Vectra System BIOS Technical Reference Manual*. For a detailed description of the HP-HIL interface refer to the *HP-HIL Technical Reference Manual*.

Commands are sent from the system to the keyboard. These are listed and defined in Table 2-2. Responding commands, sent by the keyboard to the system, are listed and defined in Table 2-3.

Table 2-1. Keyboard Scan Codes

Key Number	Make Code	Break Code	Key Number	Make Code	Break Code
1	0E	F0 0E	48	21	F0 21
2	16	F0 16	49	2A	F0 2A
3	1E	F0 1E	50	32	F0 32
4	26	F0 26	51	31	F0 31
5	25	F0 25	52	3A	F0 3A
6	2E	F0 2E	53	41	F0 41
7	36	F0 36	54	49	F0 49
8	3D	F0 3D	55	4A	F0 4A
9	3E	F0 3E	57	59	F0 59
10	46	F0 46	58	14	F0 14
11	45	F0 45	59 ***	5E	F0 5E
12	4E	F0 4E	60	11	F0 11
13	55	F0 55	61	29	F0 29
15	66	F0 66	62	E0 11	E0 F0 11
16	0D	F0 0D	63 ***	5F	F0 5F
17	15	F0 15	64	E0 14	E0 F0 14
18	1D	F0 1D	90	77	F0 77
19	24	F0 24	91	6C	F0 6C
20	2D	F0 2D	92	6B	F0 6B
21	2C	F0 2C	93	69	F0 69
22	35	F0 35	96	75	F0 75
23	3C	F0 3C	97	73	F0 73
24	43	F0 43	98	72	F0 72
25	44	F0 44	99	70	F0 70
26	4D	F0 4D	100	7C	F0 7C
27	54	F0 54	101	7D	F0 7D
28	5B	F0 5B	102	74	F0 74
29 *	5D	F0 5D	103	7A	F0 7A
30	58	F0 58	104	71	F0 71
31	1C	F0 1C	105	7B	F0 7B
32	1B	F0 1B	106	79	F0 79
33	23	F0 23	108	E0 5A	E0 F0 5A
34	2B	F0 2B	110	76	F0 76
35	34	F0 34	112	05	F0 05
36	33	F0 33	113	06	F0 06
37	3B	F0 3B	114	04	F0 04
38	42	F0 42	115	0C	F0 0C
39	4B	F0 4B	116	03	F0 03
40	4C	F0 4C	117	0B	F0 0B
41	52	F0 52	118	83	F0 83
42 **	5D	F0 5D	119	0A	F0 0A
43	5A	F0 5A	120	01	F0 01
44	12	F0 12	121	09	F0 09
45 **	61	F0 61	122	78	F0 78
46	1A	F0 1A	123	07	F0 07
47	22	F0 22	125	7E	F0 7E

* 101-key keyboard only.
** 102-key keyboard only (non-US).
*** Asian keyboard only.

Table 2-1. Keyboard Scan Codes (cont.)

Key Number	Base Case, or Shift + Num Lock Make / Break	Shift Case Make / Break *	Num Lock on Make / Break
75	E0 70 / E0 F0 70	E0 F0 12 E0 70 / E0 F0 70 E0 12	E0 12 E0 70 / E0 F0 70 E0 F0 12
76	E0 71 / E0 F0 71	E0 F0 12 E0 71 / E0 F0 71 E0 12	E0 12 E0 71 / E0 F0 71 E0 F0 12
79	E0 6B / E0 F0 6B	E0 F0 12 E0 6B / E0 F0 6B E0 12	E0 12 E0 6B / E0 F0 6B E0 F0 12
80	E0 6C / E0 F0 6C	E0 F0 12 E0 6C / E0 F0 6C E0 12	E0 12 E0 6C / E0 F0 6C E0 F0 12
81	E0 69 / E0 F0 69	E0 F0 12 E0 69 / E0 F0 69 E0 12	E0 12 E0 69 / E0 F0 69 E0 F0 12
83	E0 75 / E0 F0 75	E0 F0 12 E0 75 / E0 F0 75 E0 12	E0 12 E0 75 / E0 F0 75 E0 F0 12
84	E0 72 / E0 F0 72	E0 F0 12 E0 72 / E0 F0 72 E0 12	E0 12 E0 72 / E0 F0 72 E0 F0 12
85	E0 7D / E0 F0 7D	E0 F0 12 E0 7D / E0 F0 7D E0 12	E0 12 E0 7D / E0 F0 7D E0 F0 12
86	E0 7A / E0 F0 7A	E0 F0 12 E0 7A / E0 F0 7A E0 12	E0 12 E0 7A / E0 F0 7A E0 F0 12
89	E0 74 / E0 F0 74	E0 F0 12 E0 74 / E0 F0 74 E0 12	E0 12 E0 74 / E0 F0 74 E0 F0 12

* The F0 12/12 shift make and break is sent with the other scan codes if the left Shift key is held down. If the right Shift key is held down, then F0 59/59 is sent. Both sets of codes are sent with the other scan code if both Shift keys are held down.

Key Number	Scan code Make / Break	Shift Case Make / Break *
95	E0 4A / E0 F0 4A	E0 F0 12 4A / E0 12 F0 4A

* The F0 12/12 shift make and break is sent with the other scancodes if the left Shift key is held down. If the right Shift key is held down, then F0 59/59 is sent. Both sets of codes are sent with the other scancode if both Shift keys are held down.

Key Number	Scan code Make / Break	Ctrl Case, Shift Case Make / Break	Alt Case Make / Break
124	E0 12 E0 7C / E0 F0 7C E0 F0 12	E0 7C / E0 F0 7C	84 / F0 84

Key Number	Make Code	Ctrl Key Pressed
126 *	E1 14 77 E1 F0 14 F0 77	E0 7E E0 F0 7E

* Not a Typematic key. All associated scan codes occur on the make of the key.

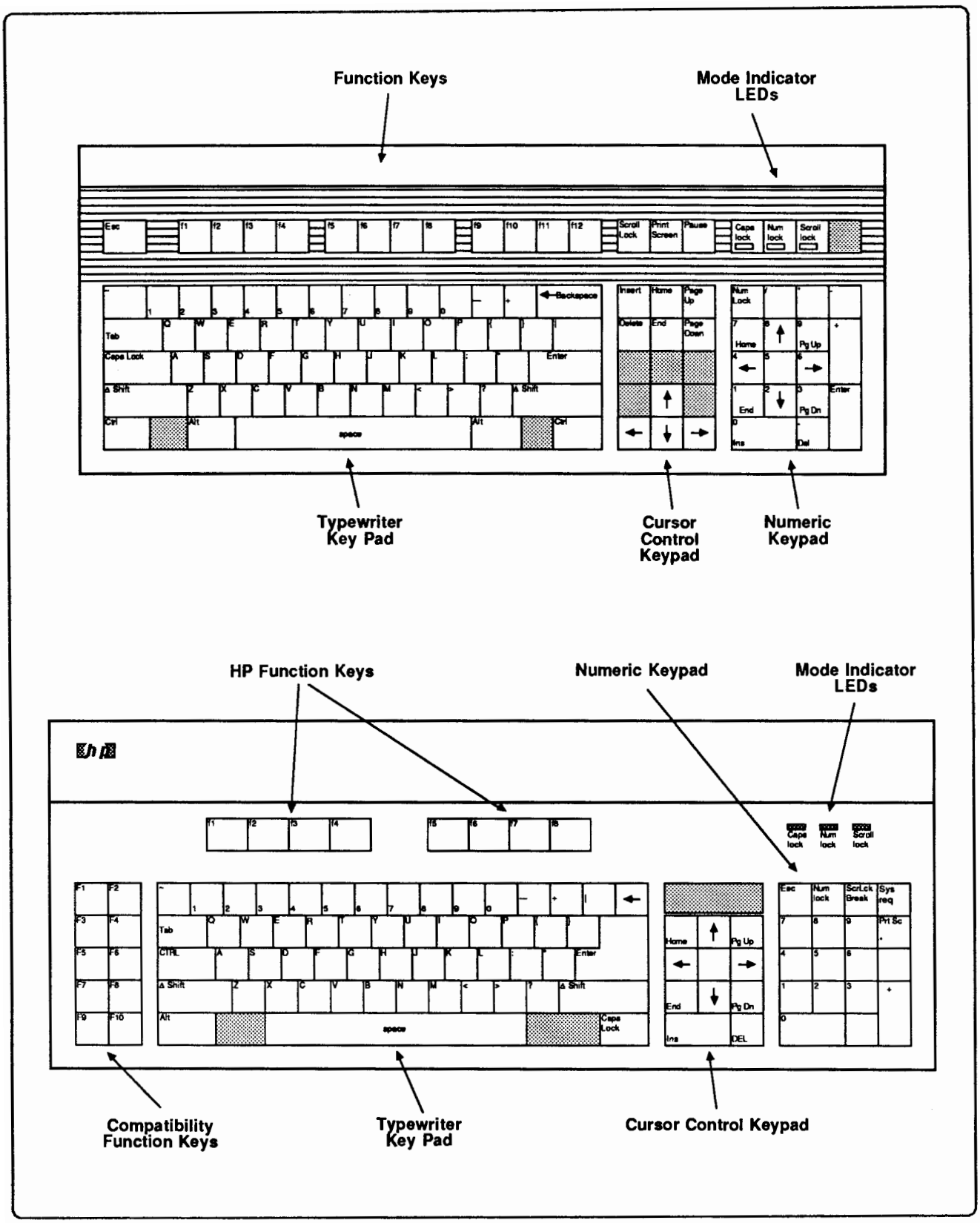


Figure 2-2. Keyboard Configurations

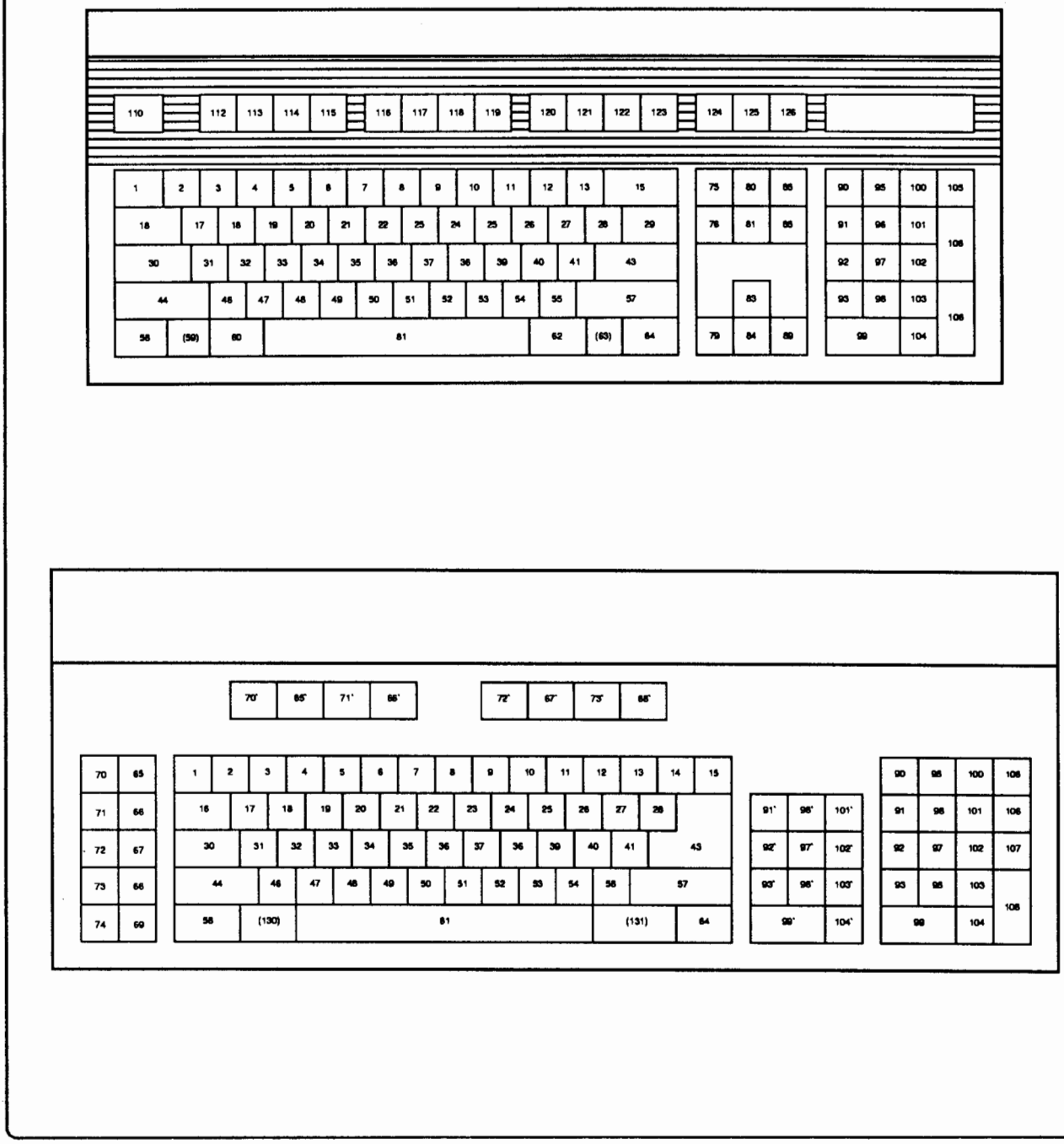


Figure 2-3. Keyboard Reference Numbers

Table 2-2. Keyboard Commands Sent to Keyboard

Command	Definition
Reset (FFh)	This command resets the keyboard and starts a self-test routine. The routine begins with an acknowledge signal sent to the system. The system responds by halting the clock and data for a minimum of 500 microseconds. The keyboard then begins the reset operation.
Resend (FEh)	This command is sent by the 8042, when it detects an error in the data coming from the keyboard, to tell the keyboard to resend the last data.
No Operation (FDh to F7h)	These commands are reserved. The keyboard will acknowledge receiving these commands, however no action will be taken.
Set Default (F6h)	This command resets all keyboard functions to the default (power-on) state.
Default Disable (F5h)	This command halts the keyboard scanning.
Enable (F4h)	This command resumes the keyboard scanning if halted from an F5h command.
Set Typematic Rate/Delay (F3h)	This command alters the typematic rate and delay. This command (F3h) is followed immediately by a byte which is sent immediately after the Set command. Bits 6 (msb) and 5 (lsb) are the delay parameter, and bits 4 (msb) through 0 (lsb) are the rate parameters. Bit 7 is always 0.
No Operation (F2h to EFh)	These commands are reserved. The keyboard will acknowledge receiving these commands, however no action will be taken.
Echo (EEh)	This command causes the keyboard to return (echo) an EEh response as a diagnostic aid.
Mode Indicators (EDh)	This command controls the three mode indicator LEDs on the keyboard. The command (EDh) is followed immediately by a byte which contains the state in which the keyboard is to set the LEDs. Bits 7 (msb) through 3 are not used. Bit 2 controls the Caps Lock indicator, Bit 1 controls the Numeric Lock indicator, and Bit 0 controls the Scroll Lock indicator. The bits do not determine the state of the LEDs, but rather toggle them. If a default condition needs to be determined, the keyboard should first be reset to a known condition (F6h) and then the LEDs toggled as required.

Table 2-3. Keyboard Commands Sent by Keyboard

Command	Definition
Resend (FEh)	This command is sent by the keyboard if it receives an invalid input or an input with incorrect parity.
Ack (FAh)	This command is sent by the keyboard to acknowledge it has received valid input from the system. The keyboard does not send this command when it receives from the system either an Echo command (EEh) or a Resend command (FEh). If the system interrupts the keyboard with a command while the keyboard is sending ACK, the keyboard discards the ACK command. If the new command is recognized, the keyboard accepts the system's new command and processes it. If the command is not recognized, the keyboard sends a Resend command (FEh) to the system.
Overrun (00h)	This character is placed in position 17 of the keyboard buffer, overlaying the last of the code when the buffer is full.
Diagnostic Failure (FDh)	This command is sent if the keyboard detects a malfunction. If it occurs during the keyboard self-test the keyboard will stop and wait for a system command or a power-down.
Break Code Prefix (F0h)	This code is sent to the system by the keyboard when a key is released. The code consists of a two-byte hex prefix, F0, followed by the make code for the released key.
Completion Code (AAh)	After the keyboard has successfully passed the keyboard self-test. Any other code tells the computer that the keyboard test failed.
Echo (EEh)	This command is sent to respond to an ECHO command from the computer, acknowledging the receipt of the Echo command.

HP-HIL Interface

The HP-HIL (Hewlett-Packard Human Interface Link) is a Hewlett-Packard proprietary four-wire asynchronous serial interface. HP-HIL provides an interface between the SPU and up to seven Hewlett-Packard HIL input devices. An overview of the HP-HIL operation is given below. (For more information, consult the *HP-HIL Technical Reference Manual.*)

HP-HIL Operation

The HP-HIL enables the user to connect input devices to the SPU by "daisy-chaining" them; i.e., the first input device is plugged into the SPU, the second input device is plugged into the first input device, etc.

Approximately 60 times per second, the HP-HIL Master Link Controller polls the HP-HIL input devices: (1) to read inputs from the user and (2) to send commands and data to the HP-HIL input devices. When the HP-HIL input devices are ready to send inputs, they send serial data to the HP-HIL controller, which converts the data to parallel data.

Through the SPU power supply, the HP-HIL provides +12 Vdc at 750 mA (maximum) for the HP-HIL input devices.

HP-HIL Controller

The HP-HIL controller interfaces the computer to HP-HIL input devices through the built-in HP-HIL connector. The HP-HIL controller accepts commands from the computer's microprocessor and transmits them to the input devices in a fixed format called a "frame." Each frame consists of 15 bits of information, including start, stop, command, parity, address, and data bits.

Using this format, the HP-HIL controller also automatically configures, identifies, and polls the input devices, collects data entered by the user, and relays the data to the 80286. In addition, using the parity bit, the HP-HIL controller detects errors.

HP-HIL Connector

The pinout for the HP-HIL connector is shown in Figure 2-4. The HP-HIL connector pin assignments are shown in Table 2-4.

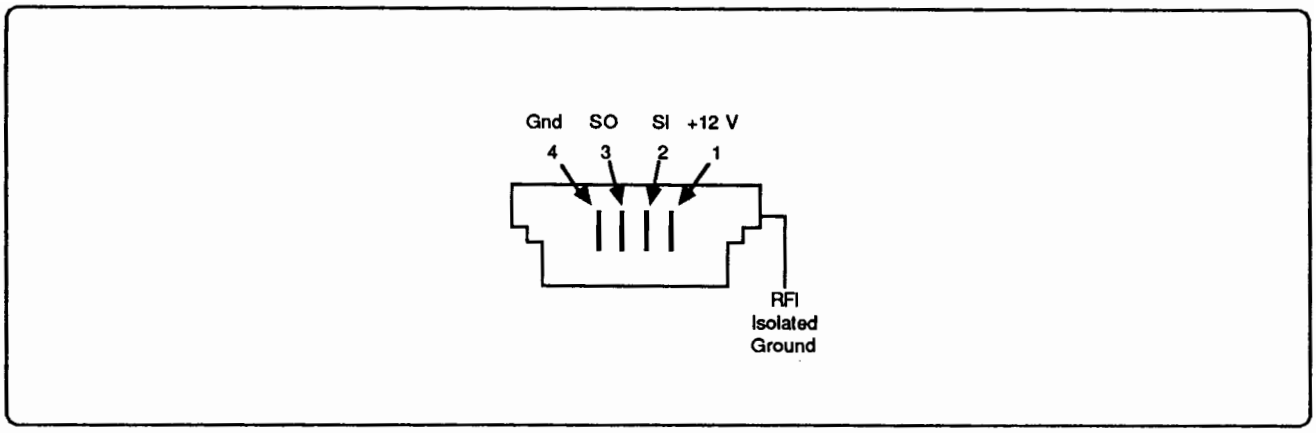


Figure 2-4. HP-HIL Connector Pin Numbering

Table 2-4. HP-HIL Connector Pin Assignments

Pin No.	Function	Pin Name	Pin Definition
1	Power	VDD	+12 Vdc power pin
2	Input	SI	Serial data HP-HIL input signal
3	Output	SO	Serial data HP-HIL output signal
4	Ground	GND	Ground
9,10	Shield	SHLD	Path to system for electro-static discharge

3

Disc and Tape Drives

This chapter covers the following disc drives:

- HP45811A 360Kb Internal Flexible Disc Drive
- HP45812A 1.2Mb Internal Flexible Disc Drive
- HP45813A 1.44Mb 3.5" Internal Flexible Disc Drive
- D1296A/HP45816A 20Mb disc drive
- D1297A/HP45817A 40Mb 5 1/4 inch disc drive

HP45811A 360Kb Internal Flexible Disc Drive

The 360Kb Internal Flexible Disc Drive can be purchased as an accessory to the HP Vectra (product number HP45811A). It stores data on double-sided 5/14 inch flexible discs and can be identified by an asterisk molded into the faceplate just below the activity light.

The drive can read and write on Double-Sided Discs (HP92190A or equivalent). Also, it can read and write to single sided discs, however, excessive head wear results when single sided discs are used.

The 360Kb Internal Flexible Disc Drive chassis is 171mm wide x 41mm high x 207mm deep. It weighs 1.6kg and fits in either of the half- height disc drive cages. It draws a maximum of 19.8 watts from the power supply. Table 3-1 describes the performance of the 360Kb Internal Flexible Disc Drive when properly installed in the HP Vectra PC.

Table 3-1. 360Kb Internal Disc Drive Performance

Formatted Capacity(MFM)	360Kb
Media type	HP92190 or equivalent
Track density	48 tpi
Tracks/surface	40
Sectors/track	8 and 9 valid
Bytes/sector	512
Track-to-track seek time	6msec
Average access time	93msec
Motor start time	500msec
Rotation speed	300 rpm
Data transfer rate	250kHz

Hardware Interface

The 360Kb Internal Flexible Disc Drive interfaces with the flexible disc controller (FDC) through the control interface cable. The signals for this interface are defined in the Disc and DataComm Controller Card chapter of this manual. Table 3-2 defines the pins used in the DC power interface.

Table 3-2. DC Power Interface Pin Assignments

Pin	Signal Name
1	+12 Vdc
2	+12 Vdc return
3	+5 Vdc return
4	+5 Vdc

Jumper Settings

The following jumpers should be installed: DS2, +WP, HS, MM, DS (in the DS/MX group).

The following jumpers should NOT be installed: DS1, DS3, DS4, MX, HL, IU, MS, HM, -WP.

HP45812A 1.2Mb Internal Flexible Disc Drive

The 1.2Mb Internal Flexible Disc Drive can be purchased as an accessory (HP product number 45812A). It stores formatted data on 5 1/4 inch flexible discs.

The 1.2Mb drive differs from the 360Kb disc drive in three major ways:

- The media on the 1.2Mb drive rotates at 360 rpm
- The read/write gap is half the width of the 360Kb disc drive
- It has two distinct read/write channels.

One of the read/write channels is optimized to transfer data to and from the media at 500kHz, the other channel is optimized to transfer data to and from the media at 300kHz. The 500kHz channel is designed to be used with HP92190X High-Capacity 96 tpi Discs. HP92190X is a high coercivity (approximately 650 Oersteds) media.

The 300kHz channel is used with HP92190A Double Sided Double-Density Discs. Because the bit storage density of the HP92190A disc is not as high as HP92190X discs, when this media is used in the 1.2Mb drive, the flexible disc controller enables the 300kHz channel and issues double STEP pulses to the drive. As a result, the 1.2Mb Internal Flexible Disc Drive can format and write a Double-Sided Double-Density Disc similar to the 360Kb Internal Flexible Disc Drive. However, since the read/write gap is half as wide as the gap in the 360Kb Internal Flexible Disc Drive head, the 360Kb Internal Flexible Disc Drive and other similar drives cannot read the signal on these smaller tracks.

Media

Note the following when using the 1.2Mb Internal Flexible Disc Drive:

- Use of HP92190X High-Capacity Discs will result in maximum storage capacity.
- HP92190X High-Capacity Discs are designed to be used only with the 1.2Mb Internal Flexible Disc Drive. They will not work in the 360Kb Internal Flexible Disc Drive.
- The 1.2Mb Internal Flexible Disc Drive can read and write data with HP92190A Double-Sided Discs. After being used in the 1.2 drive, the discs will not be able to be read or written on the 360Kb Internal Flexible Disc Drive because of the narrower track.

NOTE

A HP92190A Double-Sided Disc that has been formatted with the 1.2Mb Internal Flexible Disc Drive will only be able to be read and written on by a 1.2Mb Internal Flexible Disc Drive after the update. Label the discs that have been updated by the 1.2 drive, so that they will only be used in the 1.2Mb Internal Flexible Disc Drive.

Drive Performance

During a read command, the disc drive mode is automatically selected by the flexible disc controller after a formatted disc is inserted.

The chassis of the 1.2Mb Internal Flexible Disc Drive is 171mm wide x 41mm high x 207mm deep. It fits into either of the two half-height disc drive cages. It draws a maximum of 19.8 watts from the power supply. Table 3-3 describes the performance of the 1.2Mb Internal Flexible Disc Drive when it is properly installed in the HP Vectra.

Table 3-3. 1.2Mb Internal Flexible Disc Drive Performance

	360Kb Mode	1.2Mb Mode
Formatted Capacity	360Kb	1.2Mb
Recommended Media	HP 92190A	HP 92190X
Track density	48 tpi	96 tpi
Tracks/surface	40	80
Sectors/track	8 or 9	15
Bytes/sector	512	512
Track-to-track seek time	6 msec	3 msec
Average access time	93msec	93msec
Data transfer rate	250kHz	500kHz
Motor Start time	500 ms	500 ms
Rotation speed	300 rpm	360 rpm

Hardware Interface

The 1.2 Mb Internal Flexible Disc Drive interfaces with the flexible disc controller (FDC) through the control interface cable. The signals for this interface are defined in the Disc and DataComm Controller Card chapter of this manual. Table 3-4 defines the pins used in the DC power interface.

Table 3-4. DC Power Interface Pin Assignments

Pin	Signal Name	Current
1	+12 Vdc	1.2 A (maximum)
2	+12 Vdc return	
3	+5 Vdc return	
4	+5 Vdc	0.9 A (maximum)

Jumper Settings

The following jumpers should be installed: DC, AT, CX, DA, MM, DS2, DS, SP.

The following jumpers should NOT be installed: LR, DO, DD, IX, AX, BX, HA, UA, MS, DS1, DS3, DS4, MX, IRD, OA.

HP45813A 1.44Mb 3.5" Internal Flexible Disc Drive

The 1.44Mb Internal Flexible Disc Drive can be purchased as an accessory (HP product number 45813A). It stores data on 3.5" discs.

Media

Note the following when using the 1.44Mb Internal Flexible Disc Drive:

- Use of HP92192X High-Capacity Discs will result in maximum storage capacity.
- The 1.44Mb Internal Flexible Disc Drive can read and write data with HP92192A Double-Sided Discs, but will only have a capacity of 720 Kbytes.

Drive Performance

During a read command, the disc drive mode is automatically selected by the flexible disc controller after a formatted disc is inserted.

The chassis of the 1.44Mb Internal Flexible Disc Drive is 171mm wide x 41mm high x 207mm deep. It fits into any of the half-height disc drive cages. It draws a maximum of 1.89 watts from the power supply. Table 3-5 describes the performance of the 1.44Mb Internal Flexible Disc Drive when it is installed in the HP Vectra.

Table 3-5. 1.44Mb Internal Flexible Disc Drive Performance

	720Kb Mode	1.44Mb Mode
Formatted Capacity	720Kb	1.44Mb
Recommended Media	HP92192A	HP 92192X
Track density	135 tpi	135 tpi
Tracks/surface	80	80
Sectors/track	9	18
Track-to-track seek time	3 msec	3 msec
Average access time	175msec	175msec
Data transfer rate	250kHz	500kHz
Motor Start time	750 ms	750 ms
Rotation speed	300 rpm	300 rpm

Hardware Interface

The 1.44 Mb Internal Flexible Disc Drive interfaces with the flexible disc controller (FDC) through the control interface cable. The signals for this interface are defined in the Disc and DataComm Controller Card chapter of this manual. Table 3-6 defines the pins used in the DC power interface.

Table 3-6. DC Power Interface Pin Assignments

Pin	Signal Name	Current
1	+12 Vdc	1.2 A (maximum)
2	+12 Vdc return	
3	+5 Vdc return	
4	+5 Vdc	0.9 A (maximum)

Jumper Settings

This disc drive contains no user-changeable jumpers. The interface card may contain jumpers for drive selection (usually set to drive 2) and and H/L jumper (usually set to H).

D1296A/HP45816A 20Mb Hard Disc Subsystem

The 20Mb hard disc subsystem (Seagate ST-225, drive type 2) provides 20 Mb. of storage. The drive chassis fits in any of the half height drive slots, however, the cabling is best managed when the hard disc drive is installed in the lower slot. Table 3-7 describes the performance of the drive when installed in the HP Vectra PC.

Table 3-7. 20Mb Drive Performance

Formatted Capacity/Drive	21.09 Mbyte
Formatted Capacity/Sector	512 bytes
Sector/Track	17
Data Transfer Rate	5.0 Mbit/sec
Track-to-Track Seek Time	20 msec
Average Access Time	85 msec
Maximum Seek	190 msec
Latency	8.33 msec
Rotational Speed	3,600 RPM +/-1%
Cylinders	606
Read/Write Heads	4
Discs	2
Dissipation	15 watts typical

Drive to Controller Interface

The drive interfaces with the controller in two areas: the control interface and the data interface. The disc drive receives control signals and transmits status signals over the J1/P1 connectors. Data signals are received and transmitted over the J2/P2 connectors. The signals for these interfaces are defined in the Disc and DataComm Controller Card chapter of this manual. The DC power connector, J3, is a 4-pin AMP "Mate-n-Lock" connector as defined in Table 3-8.

Table 3-8. DC Power Interface Pin Assignments

Pin	Signal Name	Current
1	+12 Vdc	1.2 A (maximum)
2	+12 Vdc return	
3	+5 Vdc return	
4	+5 Vdc	0.9 A (maximum)

Jumper Settings

The 20 Mb hard disc drive should be jumpered as shown in Figure 3-1.

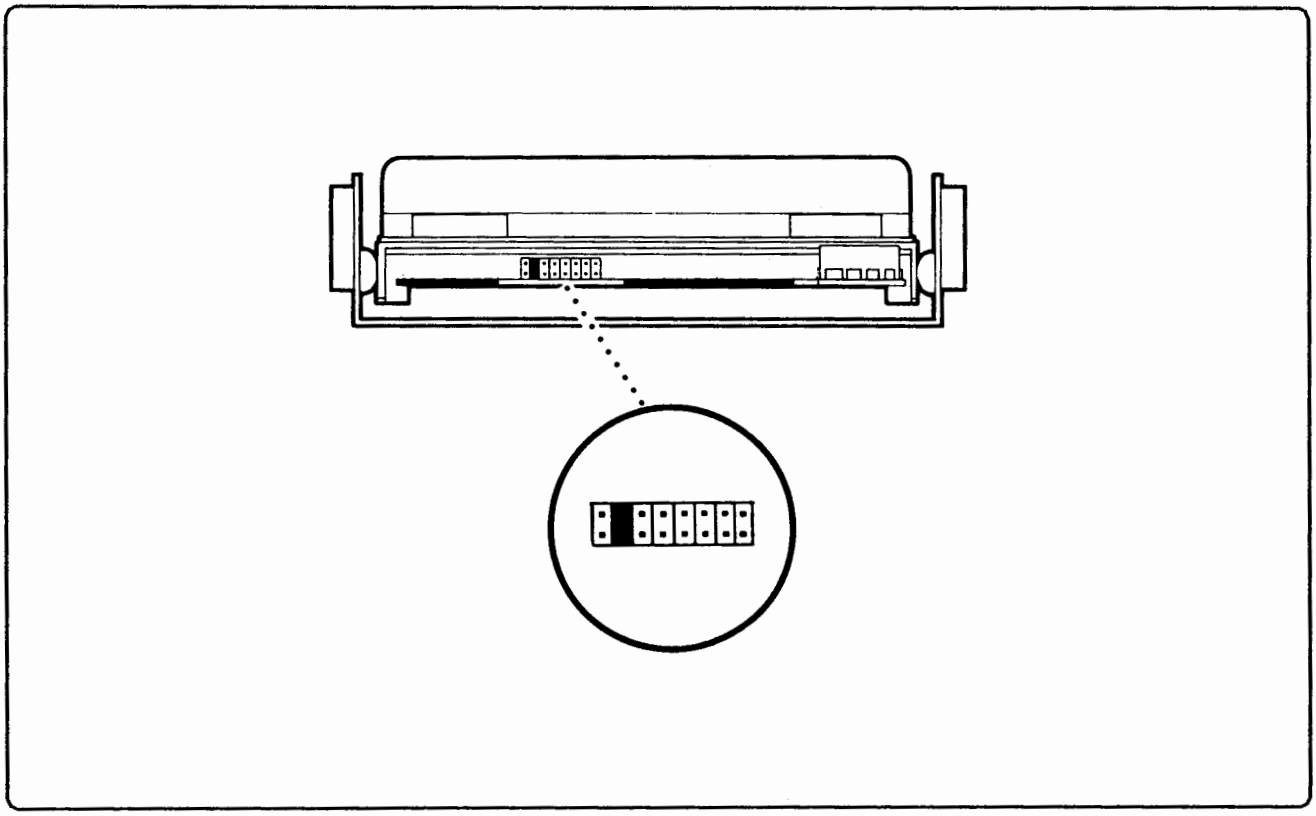


Figure 3-1. 20 Mb Hard Disc Drive Jumper Setting.

D1297A/HP45817A 40Mb Hard Disc Subsystem

The 40Mb hard disc subsystem (Seagate ST-251, drive type 44) provides fast access and high-capacity storage. The drive automatically retracts the read and write heads to a parking zone when powered off. This protects the disc against damage during handling or moving. Table 3-9 defines the performance of the 40 Mb drive when installed in the HP Vectra PC.

Table 3-9. 40 Mb Drive Performance

Formatted capacity/drive	42.7 Mbyte (normally accessed as 2-20Mbyte units)
Formatted capacity/sector	512 bytes
Sector/Track	17
Data Transfer Rate	5.0 Mbit/sec
Track-to-Track Seek Time	10msec
Average Access Time	40msec
Maximum Seek	80msec
Latency	8.33msec
Rotational Speed	3,600 RPM +/-1%
Cylinders	971
Read/Write Heads	5
Discs	3
Heat Dissipation	24 watts typical

Drive to Controller Interface

The drive interfaces with the controller in three areas: the control interface, the data interface and the DC power interface. The disc drive receives control signals and transmits status signals over the J1/P1 connectors. Data signals are received and transmitted over the J2/P2 connectors. The DC power connector is J3 and is a 4-pin AMP "Mate-n-Lock" connector. The DC power connector, J3, is a 4-pin AMP "Mate-n-Lock" connector as defined in Table 3-10.

Table 3-10. DC Power Interface Pin Assignments

Pin	Signal Name	Current
1	+12 Vdc	1.2 A (maximum)
2	+12 Vdc return	
3	+5 Vdc return	
4	+5 Vdc	0.9 A (maximum)

Jumper Settings

The 40 Mb hard disc drive should be jumpered as shown in Figure 3-2.

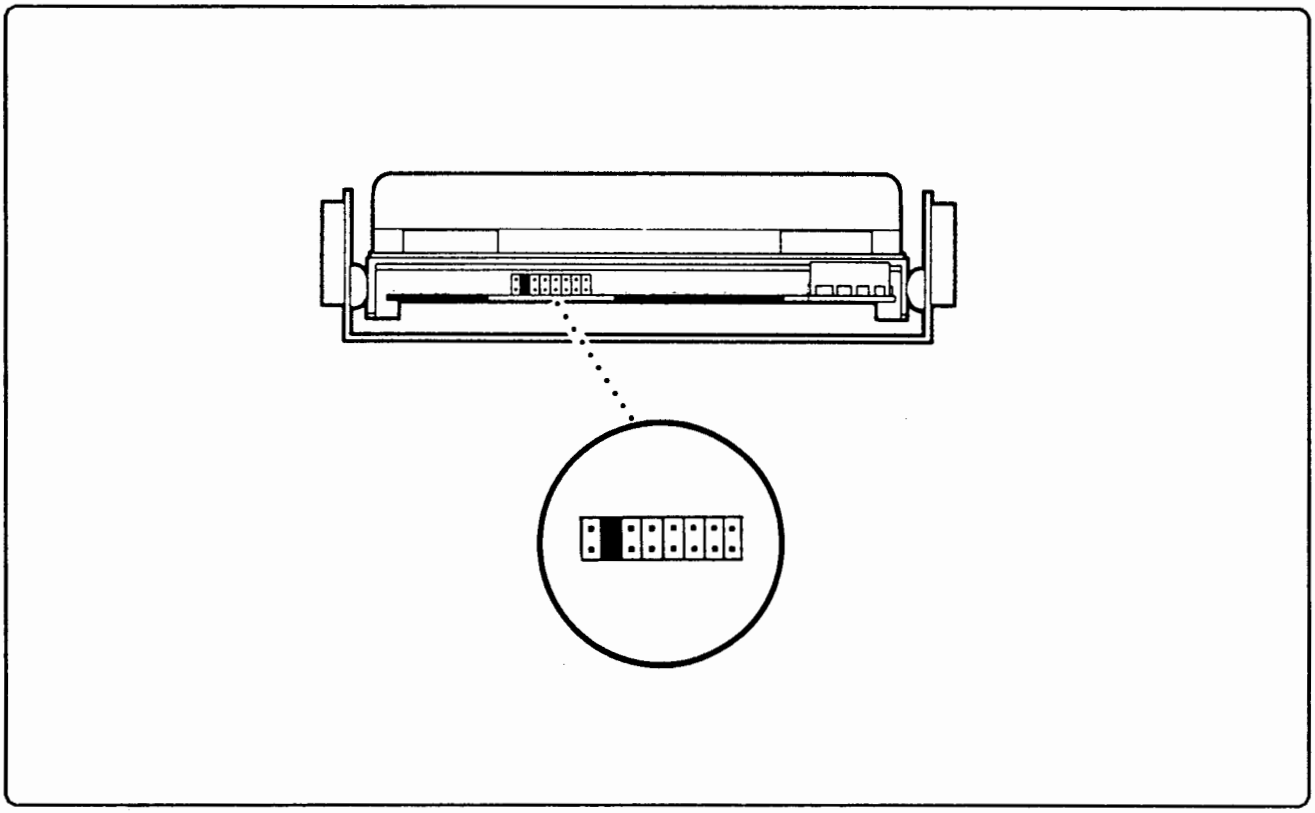


Figure 3-2. 40 Mb Hard Disc Drive Jumper Setting.

D1674A 103Mb Full-Height Hard Disc Subsystem

The D1674A 103Mb hard disc subsystem (Hewlett-Packard 97961R, drive type 42 or 45) provides fast access and high-capacity storage. The drive automatically retracts the read and write heads to a parking zone when powered off, which protects the disc against damage during handling or moving. Table 3-11 defines the performance of the D1674A when installed in the HP Vectra RS PC.

Table 3-11. D1674A Drive Performance

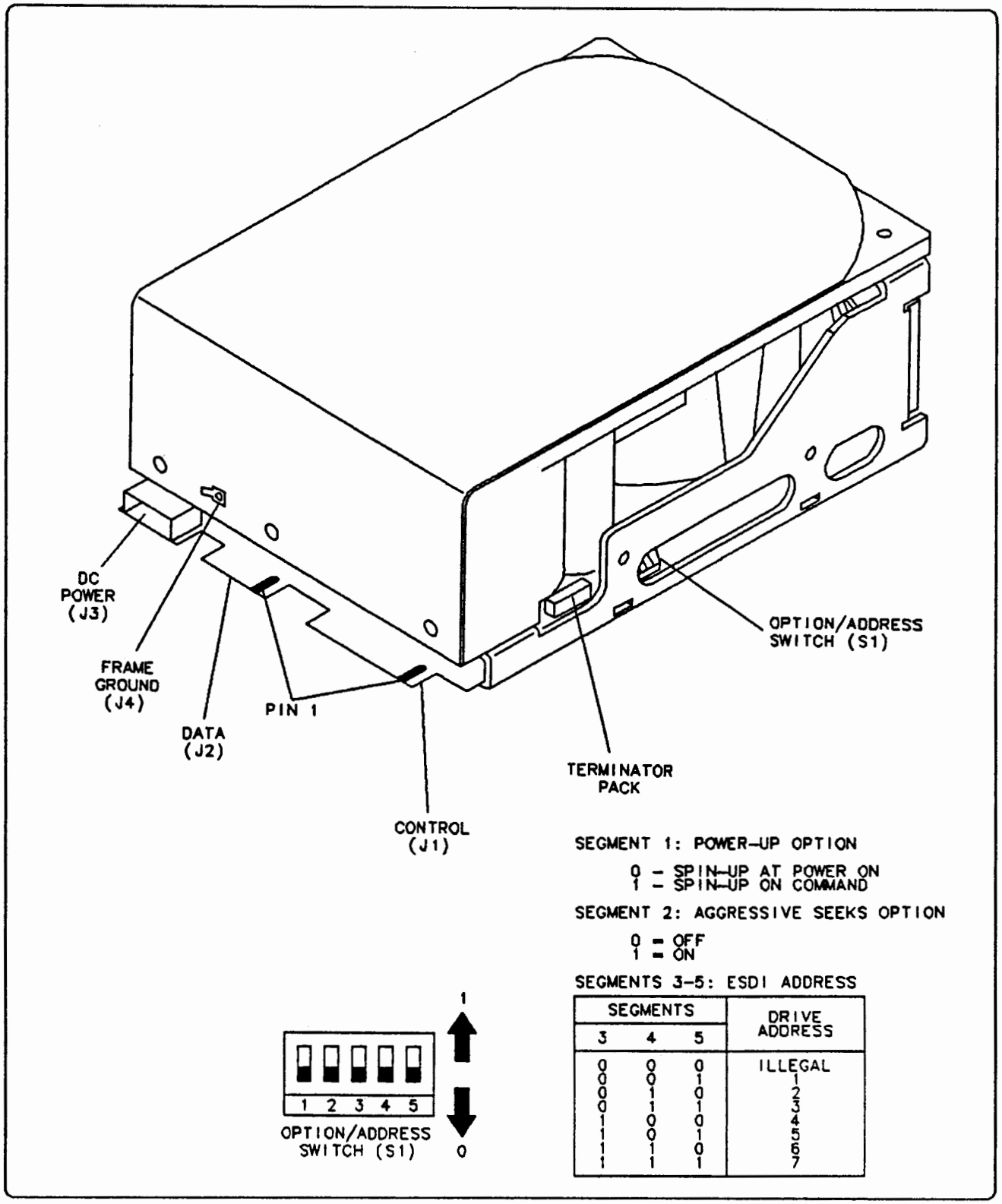
Formatted capacity/drive	103 Mbytes
Formatted capacity/sector	256 bytes
Sector/Track	64
Data Transfer Rate	10.0 Mbit/sec
Track-to-Track Seek Time	3.5msec
Average Access Time	17 msec
Maximum Seek	32msec
Latency	8.96msec
Rotational Speed	3,348.2 RPM +/-1%
Cylinders	1583
Read/Write Heads	4
Discs	2
Power Dissipation	21 watts typical

Drive to Controller Interface

The drive interfaces with the controller in three areas: the control interface, the data interface, and the DC power interface. The disc drive receives control signals and transmits status signals over the J1/P1 connectors. Data signals are received and transmitted over the J2/P2 connectors. The DC power connector, J3, is a 4-pin AMP "Mate-n-Lock" connector. Table 3-12 gives the DC power connector's pin assignments. The D1674A hard disc drive (as well as the D1675A and D1676A hard disc drives) should be jumpered as shown in Figure 3-3.

Table 3-12. DC Power Connector Pin Assignments

Pin	Signal Name	Current
1	+12 Vdc	1.2 A (maximum)
2	+12 Vdc return	1.2 A
3	+5 Vdc return	1.4 A
4	+5 Vdc	1.4 A (maximum)



SEGMENTS			DRIVE ADDRESS
3	4	5	
0	0	0	ILLEGAL
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 3-3. D1674A, D1675A, D1676A Hard Disc Drive Jumper Settings

D1675A 155Mb Full-Height Hard Disc Subsystem

The D1675A 155Mb hard disc subsystem (Hewlett-Packard 97962R, drive type 43 or 46) provides fast access and high-capacity storage. The drive automatically retracts the read and write heads to a parking zone when powered off, which protects the disc against damage during handling or moving. Table 3-13 defines the performance of the D1675A when installed in the HP Vectra RS PC.

Table 3-13. D1675A Drive Performance

Formatted capacity/drive	155 Mbytes
Formatted capacity/sector	256 bytes
Sector/Track	64
Data Transfer Rate	10.0 Mbit/sec
Track-to-Track Seek Time	3.5msec
Average Access Time	17 msec
Maximum Seek	32msec
Latency	8.96msec
Rotational Speed	3,348.2 RPM +/-1%
Cylinders	1583
Read/Write Heads	6
Discs	3
Power Dissipation	21 watts typical

Drive to Controller Interface

The drive interfaces with the controller in three areas: the control interface, the data interface, and the DC power interface. The disc drive receives control signals and transmits status signals over the J1/P1 connectors. Data signals are received and transmitted over the J2/P2 connectors. The DC power connector, J3, is a 4-pin AMP "Mate-n-Lock" connector. Table 3-14 gives the DC power connector's pin assignments. The D1675A hard disc drive should be jumpered as shown in Figure 3-3.

Table 3-14. DC Power Connector Pin Assignments

Pin	Signal Name	Current
1	+12 Vdc	1.2 A (maximum)
2	+12 Vdc return	1.2 A
3	+5 Vdc return	1.4 A
4	+5 Vdc	1.4 A (maximum)

D1676A 310Mb Full-Height Hard Disc Subsystem

The D1676A 310Mb hard disc subsystem (Hewlett-Packard 97963R, drive type 47) provides fast access and high-capacity storage. The drive automatically retracts the read and write heads to a parking zone when powered off, which protects the disc against damage during handling or moving. Table 3-15 defines the performance of the D1676A when installed in the HP Vectra RS PC.

Table 3-15. D1676A Drive Performance

Formatted capacity/drive	310 Mbytes
Formatted capacity/sector	256 bytes
Sector/Track	64
Data Transfer Rate	10.0 Mbit/sec
Track-to-Track Seek Time	3.5msec
Average Access Time	17 msec
Maximum Seek	32msec
Latency	8.96msec
Rotational Speed	3,348.2 RPM +/-1%
Cylinders	1583
Read/Write Heads	12
Discs	6
Power Dissipation	21 watts typical

Drive to Controller Interface

The drive interfaces with the controller in three areas: the control interface, the data interface, and the DC power interface. The disc drive receives control signals and transmits status signals over the J1/P1 connectors. Data signals are received and transmitted over the J2/P2 connectors. The DC power connector, J3, is a 4-pin AMP "Mate-n-Lock" connector. Table 3-16 gives the DC power connector's pin assignments. The D1676A hard disc drive should be jumpered as shown in Figure 3-3.

Table 3-16. DC Power Connector Pin Assignments

Pin	Signal Name	Current
1	+12 Vdc	1.2 A (maximum)
2	+12 Vdc return	1.2 A
3	+5 Vdc return	1.4 A
4	+5 Vdc	1.4 A (maximum)

4

Disc and DataComm Controller Card

The Hewlett-Packard Disc and DataComm Controller card consists of four subsystems: the Hard Disc Controller (HDC) subsystem, the Flexible Disc Controller (FDC) subsystem, the Serial DataComm Interface subsystem and the Parallel DataComm Interface subsystem.

Compatibility

The Hewlett-Packard Disc and DataComm Controller card is compatible with the HP Hard Disc Controller (P/N HP 1150-1767), the flexible disc controller in the early Vectras, and the HP Serial/parallel card (P/N HP?4540A) in the following areas:

- BIOS entry point
- Firmware
- Registers
- Disc Drive Support
- Serial and Parallel Port Connectors

The Hewlett-Packard Disc and DataComm Controller card uses the following hardware interrupt request levels:

IRQ14 Hard Disc Controller
IRQ6 Flexible Disc Controller
IRQ7 Parallel Port 1
IRQ5 Parallel Port 2
IRQ4 Serial Port 1
IRQ3 Serial Port 2

The layout of the card is shown in Figure 4-1.

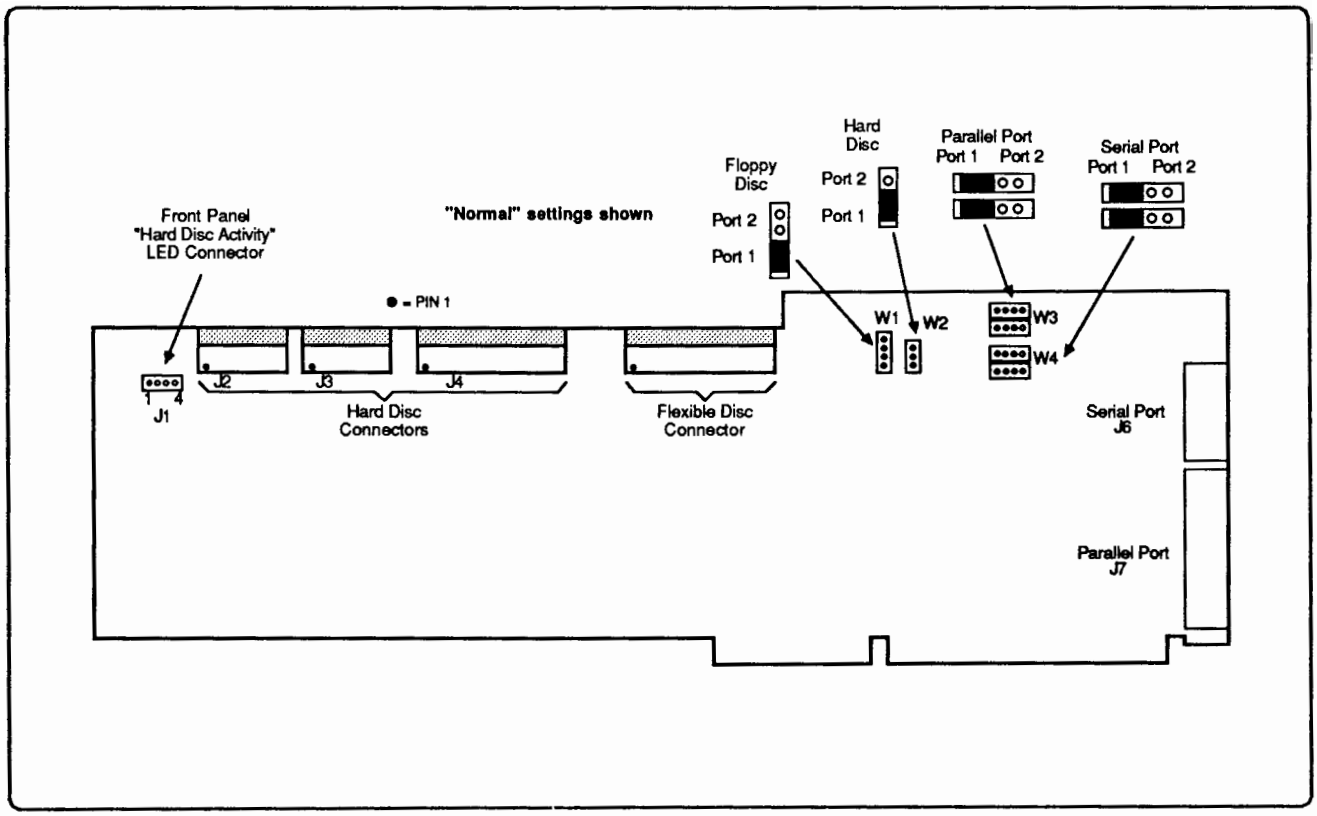


Figure 4-1. Disc and DataComm Card.

Hard Disc Controller (HDC) Subsystem

Jumper Configurations

Jumper block W2 selects or deselects the hard disc controller subsystem, or selects the location of the interface registers in the system I/O map. The I/O address can be either the primary addressing, 1F0H through 1F7H and 3F6H, 3F7H or the secondary addressing, 170H through 177H and 376H, 377H. The location of the jumpers is shown in Figure 4-1. The jumpers are set according to Figure 4-2.

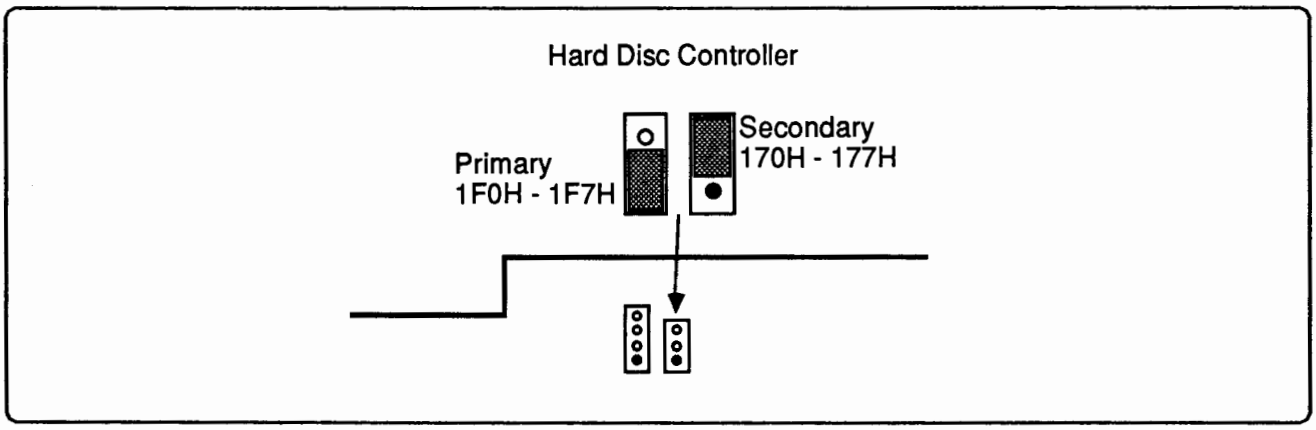


Figure 4-2. HDC Jumpers

Basic Function

The hard disc controller subsystem generates the signals which control the electromechanical parts of the drive, interpret the status signals received from the drive, and convert between parallel and serial data formats.

The hard disc controller features 512-byte sectors; high-speed, PIO data transfers; ECC correction of up to five bits on data fields multiple sector operations across track and cylinder boundaries; and on-board diagnostic tests.

System to HDC Subsystem Interface

The hard disc controller subsystem interfaces to the system bus through the address, data and programmed I/O control signals. All data transfers are 16 bits wide and occur between the bus and the data buffer memory. Control, status and ECC check byte transfers are 8 bits wide and use lower data byte lines SD07-SD00 only. The bus interrupt request level is fixed at IRQ14.

The hard disc controller subsystem contains 19 registers for control and data transfer. Table 4-1 lists the registers and their primary and secondary I/O addresses.

Table 4-1. Accessible Registers

Register	R/W	I/O Address	
		Primary	Secondary
Hard Disc Data Reg. (16 bits)	R/W	1F0H	170H
Write Pre-compensation Cylinder	W	1F1H	171H
Error Register	R	1F1H	171H
Sector Count	R/W	1F2H	172H
Sector Number	R/W	1F3H	173H
Cylinder Number - Low Byte	R/W	1F4H	174H
Cylinder Number - High Byte	R/W	1F5H	175H
Sector Size, Drive/Head Select	R/W	1F6H	176H
Command Register	W	1F7H	177H
Status Register	R	1F7H	177H
Hard Disc Register	W	3F6H	376H
Alternate Status Register	R	3F6H	376H
Digital Input Register	R	3F7H	377H

Hard Disc Data Register (Read/Write, 1F0H or 170H)

The data register provides access to the sector buffer for read and write operations in the PIO mode. This register must not be accessed unless a Read or Write command is being executed. The register provides a 16-bit path into the sector buffer for normal Read and Write commands. When a R/W Long is issued, the 4 ECC bytes are transferred by byte with at least 2 microseconds between transfers. "Data Request" (DRQ) must be active before the transferring of the ECC bytes.

Write Pre-compensation Register (Write only, 1F1H or 171H)

This is a Write only register. The value in this register is the starting cylinder divided by 4. The "Reduced Write Current" (RWC) signal to the drive is activated and the HDC subsystem Write Precompensation logic is turned on.

Error Register (Read only, 1F1H or 171H)

This is a read-only register that contains specific information related to the previous command. The data is valid only when the error bit in the status register is set in the operating mode or unless the HDC subsystem is in diagnostic mode.

The following are bit definitions of the error register in the operational mode.

Bit	Data	Definition
0	1	Data Address Mark Not Found within 16 bytes of the ID field.
1	1	Track 000 error.
2	1	Aborted command.
3	-	Not used.
4	1	ID field not found.
5	-	Not used.
6	1	Data ECC error.
7	1	Bad block detected.

Diagnostic mode is the state immediately after power is switched on or after a diagnostic command is issued. In both cases, the register must be checked regardless of the status register error bit.

The following are error definitions for the diagnostic mode.

Mode	Definition
01	No error
02	Winchester Controller error
03	Sector RAM buffer data error
04	Host bus manager or pipeline register error
05	Control processor ROM or RAM data error
00, 06-FF	Not used.

Sector Count Register (Read/Write, 1F2H or 172H)

This register defines the number of sectors to be transferred during a Verify, Read, Write, or Format command. The value written into this register is decremented by one after each sector is transferred to or from the sector buffer. Note: A 0 represents a 256 sector transfer, a 1 = one sector, etc. This register is disregarded when a single sector command is specified.

Sector Number Register (Read/Write, 1F3H or 173H)

This register holds the number of the desired sector for Read, Write, Verify commands. The starting sector number is loaded into this register for multi-sector operation. It is incremented by one after each sector has been transferred to or from the sector buffer.

Cylinder Number Registers - Low Byte (Read/Write, 1F4H or 174H)

This register holds the least signification 8 bits of the desired cylinder number.

Cylinder Number Register - High Byte (Read/Write, 1F5H or 175H)

The least three signification bits of this register contains the three most signification bits of the desired cylinder number. The cylinder number register determines where the Read/Write heads are to be positioned.

Sector Size, Drive/Head Select Register (Read/Write, 1F6H or 176H)

This register contains the following information:

Bit	Data	Definition
0-3		Head select, bit 0 is least signification bit. The hard disc controller supports 16 read/write heads.
4	0	First hard disc drive selected.
	1	Second hard disc drive selected.
5	1	Set to 1 to select for 512 byte per sector.
6	0	Set to 0 together with bit 5 to select 512 bytes per sector.
7	1	Set to 1 to select ECC mode for the data field.

Command Register (Write only, 1F7H or 177H)

The Command Register accepts eight commands and command attributes to perform hard disc operations. Any code not defined in the following causes an Aborted Command error. Interrupt 14 is reset when any command is written. The following are acceptable commands to the command register.

Command	Bit							
	7	6	5	4	3	2	1	0
Restore	0	0	0	0	RT3	RT2	RT1	RT0
Seek	0	0	1	1	RT3	RTY	RT1	RT0
Read Sector	0	0	1	0	0	0	LNG	RTY
Write Sector	0	0	1	1	0	0	LNG	RTY
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	RTY
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1

RT3-RT0: Drive stepping rate (see below).
LNG = 0: Normal mode, normal ECC functions.
LNG = 1: Long mode.
RTY = 0: Error retries are enabled.
RTY = 1: Retries are disabled.

RT3-0 DECODE (H)	RATE (ms)	RT3-0 DECODE(H)	RATE (ms)
0	35.0us	8	4.00
1	0.50	9	4.50
2	1.00	A	5.00
3	1.50	B	5.50
4	2.00	C	6.00
5	2.50	D	6.50
6	3.00	E	3.2us
7	3.50	F	16.0us

NOTE

After Diagnose command or a reset, the stepping rate defaults to 16 us.

Command Description

Command	Definition
RESTORE:	This command is used to move the R/W heads to the Track 000 position. The controller issues step pulses to the drive unit the Track 000 indicator from the drive is true. If Track 000 is not true within 2048 steps the Error bit in the Status Register is set and a Track 000 error is posted in the Error Register. The implied seek step rate may be set up according to the table in section above by the this command. The step rate is established by the seek complete signal from the drive, i.e., each step pulse is issued only after seek complete is asserted by the drive from the previous step. If the ~DRIVE READY signal is de-asserted or ~WRITE FAULT is asserted. This command terminates with the error bit set in the Status Register and the Error Register reports an aborted command.
SEEK:	This command moves the R/W heads to the cylinder specified in the task file cylinder high and low registers. The implied seek step rate is also set by this command. An interrupt is generated at the completion of the command. If the ~DRIVE READY signal is de-asserted or ~WRITE FAULT is asserted, this command is terminated with the error bit set in the Status Register and the Error Register reports an aborted command.
READ SECTOR:	A number of sector (1-256) can be read from the selected drive with this command. The sector count register in the task file determine the number of sector to be transferred. Multi- sector reads may cross head and cylinder boundaries. If the Read command is issued prior to initializing a step rate the default value of 16 usec is selected and a Recalibrate is performed prior to the Read. If the R/W heads are not positioned over the target track, the controller performs an implied seek to the proper cylinder. The stepping rate used during the implied seek is the value specified during the previous Seek or Restore command. The optional long bit (L set to 1 enables Read Long) informs the disc controller whether of not to include the four ECC bytes. These four ECC bytes are transferred as individual bytes, not words, as is the data field information. The data request bit in the data register must be valid before each byte transferred and at least 2 usec will pass between each byte transferred. Data errors up to 11 bits in length will be automatically corrected on normal Read commands. If an uncorrectable error occurs, the data transfer will still take place, a multi- sector read, however, will terminate after the sector in error is read by the system.

Command	Definition
	The optional retry bit (T set to 1 disables retries) disables or enables retries. The Winchester disc controller performs up to 10 automatic retries when the retry bit is enabled. The Winchester disc controller properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two automatic retries before the Winchester disc controller sets the error and status registers. For ECC errors, eight retries are made at reading before a soft uncorrectable error is reported. A retry results in the reissuing of the Winchester disc controller Read Sector command. The Winchester disc controller Read Sector command attempts to verify the sector eight times before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the Winchester disc controller, the command terminates. Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command, if the ~DRIVE READY signal is de-asserted or ~WRITE FAULT asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.
WRITE SECTOR:	A number of sectors (1-256) can be written to the selected drive. The sector count register in the task file determines the number of sectors to be transferred. Multi- sector write may cross head and cylinder boundaries. If the Write command is issued prior to initializing a step rate, the default value of 16 usec is selected and Recalibrate is performed prior to the Write. If the heads are not positioned at the cylinder specified in the cylinder high and low registers, the controller performs an implied seek. The step rate used is determined by the step rate field of the most recently executed Restore or Seek command. The optional long bit (L set to 1 enables Write Long) informs the controller whether or not to append the host supplied ECC bytes. These four bytes are transferred as individual bytes, not words, as is data field information. The data request bit in the data register must be valid before each byte transferred and at least 2 usec will pass between each byte transferred. The optional retry bit (T set to 1 disables retries) disables or enables retries. The Winchester disc controller performs up to 10 automatic retries when the retry bit is enabled. The Winchester disc controller properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two automatic retries before the Winchester disc controller sets the error and status registers.

Command	Definition
	The controller interrupt is generated as the data for each sector is required to be transferred into the sector buffer (except the first sector) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and the data request status is set. If the ~DRIVE READY signal is de-asserted or ~WRITE FAULT is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.
FORMAT TRACK:	The track specified by the task file is formatted with ID and Data fields according to the interleave table transferred to the buffer. The interleave table consists of two bytes per sector, the 1st byte is to indicate a bad block with a 80H (otherwise is 00H) and the second byte is for the logical sector address. The data transfer must be 512 bytes even though the table may be only 34 bytes (17 sectors per track). The sector count register must be loaded with the number of sectors per track before each Format Track command. The Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80H. When switching between drives, a Restore command must be executed prior to attempting a format. Command completion will leave all data fields initialized to zeros. The completion interrupt is generated after each track has been formatted.
READ VERIFY:	This command functions similarly to a normal Read command except that data is not output to the host. One to 256 sectors may be verified at on time. The generated ECC bytes are compared with the recorded ECC bytes for data verification. A signal interrupt is generated upon completion of the command or in the even of an error. For ECC errors, eight retries are made at reading before a soft uncorrectable error is reported. A retry results in the reissuing of the Winchester disc drive controller Read Sector command. The Read Sector command attempts to verify the sector eight times before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the Winchester disc drive controller, the command terminates. The ~WRITE FAULT and ~DRIVE READY inputs are checked throughout the command's execution.

Command	Definition
DIAGNOSE:	This command causes the controller to perform an onboard diagnostic and to report the result in the Error Register. An interrupt is generated upon completion of the command. The Diagnose command performs tests on the onboard micro- processor's internal ROM and RAM, host bus interface circuit, Winchester disc controller and the Sector buffer. If nay component fails, the appropriate error code is loaded into the error register. Error code — Definition 01 — No error 02 — Winchester disc controller register error. 03 — Sector RAM buffer data error. 04 — Host bus manager RMAC error or RMAC byte 0 pipeline register error. 05 — Control processor ROM checksum or RAM data error. 00,06-FF — Not used, undefined In addition, the diagnose command sets the write pre-comp task file register to 32. This causes write pre-compensation to begin at cylinder 128 since the write pre-comp register holds the desired value divided by four. (Write pre-comp and Reduce Write Current begin on the same cylinder.) The sector count register is reset to one while the cylinder high and cylinder low and SDH register are all set to zero.
SET PARAMETERS:	This command sets up the drive parameters regarding the maximum number of heads and sectors per tracks. The hard disc controller uses these two parameters when performing multiple sector operations. The SDH task file register specifies the drive affected. The sector count and SDH registers must be set up before this command is issued. An interrupt is set at the completion of the command. This command must be issued before any multiple sector operations are undertaken. By setting the SDH register for each of the two possible drives, this command allows the controller to support two drives with different characteristics.

Status Register (Read only, 1F7H or 177H)

The hard disc controller sets up the status register with the command status after execution. A read of the status register clears interrupt request 14. The following defines the bits of the status register.

Bit	Definition
0	Error. A 1 on this bit indicates that the command ended in an error, Error Register bits are set. The next command resets the error bit.
1	Index. Set to 1 at each revolution of the disc.
2	Corrected Data. Each time the error data read from disc is corrected by the ECC algorithm, this bit is set to 1.
3	Data Request. This bits indicates that the sector buffer requests servicing during a read of write command.
4	Seek Completed. It is set to 1 when the read/write heads have completed a seek operation.
5	Fault. A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.
6	Ready. When both this bit and Seek Complete bit (bit 4) are set to 1, the hard disc drive is ready to read, write or seek.
7	Busy. It is set when the hard disc controller is executing a command and no other status register bit is valid.

Hard Disk Register (Write only, 3F6h or 376H)

This register allows programmed hard disc subsystem reset and provides enable/disable control of the hard disc interrupt.

Bit	Data	Definition
0		Reserved
1	0	Enable interrupt (IRQ14).
	1	Interrupt disabled.
2		Reset when it is set to 1.
3	0	Enable RWC
	1	Enable head select 3.
4		Reserved.
5		Reserved.
6		Reserved.
7		Reserved.

Hard Disk Register (Read only, 3F6h or 376H)

This register is a support register and provides status to either the WD1015 or host microprocessor. This register is an exact duplicate of the Status Register at location 1F7 (or 177).

Digital Input Register (Read only, 3F7H or 377H)

This register is shared with the flexible disc controller subsystem. It contains the current state of the hard disc drive select, head select and drive write gate signals. The bit definition is shown below.

Bit	Definition
0	Drive select 0
1	Drive select 1
2	Head select 0
3	Head select 1
4	Head select 2
5	Head select 3/Reduce Write Current
6	Write Gate On
7	Reserved for the Flexible Disc Controller subsystem

Command Control Flow

The host processor starts a disc operation by writing task information into the register task file. The hard disc subsystem task file is nine, 8-bit registers used to hold status information indicating the success or failure of an operation, as well as the parameters under which the drive is to operate. The parameter includes the disc cylinder, head and sector numbers, drive number, track number for start of write precompensation, sector size, and number of sectors to be transferred. After the parameters have been written to the task file, the host writes the command into the command register. The operation cycle starts when the command is received. A typical command sequence is given below to illustrate this relationship.

- In the idle state, the WD2010B drive control signals are off, the controller status indicates ready, drive status is valid, the HDC interrupt is enabled (but not asserted) and the WD1015 is in idle, monitoring it's wakeup signal input.

- The host processor outputs the command parameters to the WD2010B task file and outputs the operation command (seek, read, write, etc.) and the command attributes (long mode, retry control, etc.). For write operations the host processor also outputs the sector of format data.

- The Command byte is intercepted by the WD11C00 command support register and is held for later interpretation by the WD1015 processor.

- All commands, except write and format, set the wakeup latch in the WD11C00 which causes the controller status to indicate BUSY and a wakeup signal to the WD1015 to be asserted. Write and Format commands first set the data request status signal DRQ to initiate the host data transfer; completion of the data transfer then sets the WD1015 wakeup latch and BUSY status.

- The WD1015 examines the command, verifies command parameters, and passes the command to the WD2010B for execution.

- The WD2010B executes the command providing drive positioning, data transfer control, error monitoring and completion status. Drive read/write data control is provided by the data separation and write pre-compensation circuitry for commands that require data transfers.

- On command completion, the WD2010B interrupt the WD1015 which examines the command, status, etc. for any additional requirements. If completed, busy is reset, status indicates ready and DRQ if read data is available. If enabled, an interrupt to the host is set.

- The controller returns to idle and the host may examine drive and controller status, read input data, etc. as required to complete the operation.

Disc Drive Interface

The hard disc subsystem interfaces to the disc drive(s) through one 34-pin daisy-chain control cable and two 20-pin data cables. These connectors are in conformance with ST-506 signal definitions. To terminate the control signals properly, the last drive on the daisy chain must have a 220/300 ohm termination resistor installed.

Figure 4-3 shows the Control Interface Cable. Table 4-2 shows the pin assignments for the connectors. The input or output of the signals are referenced to the hard disc controller subsystem.

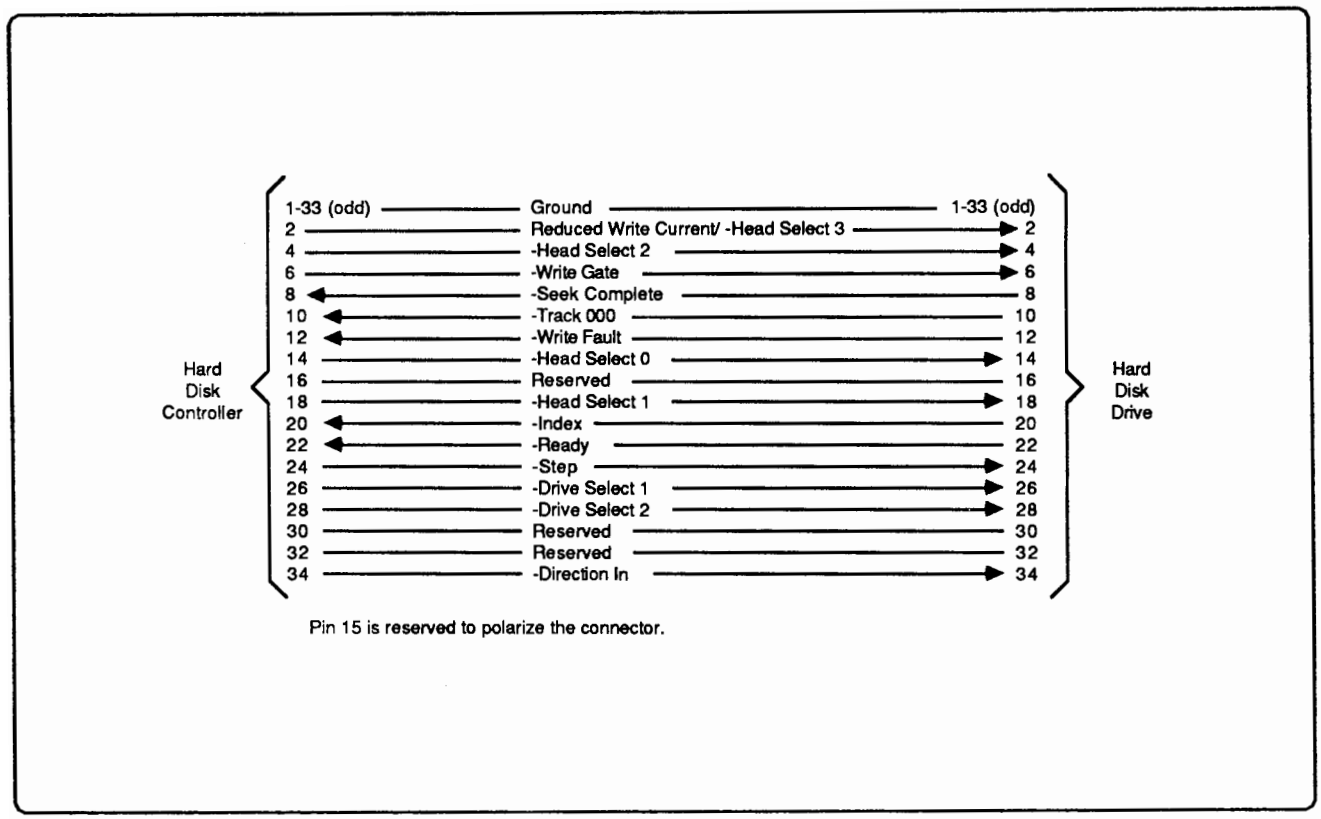


Figure 4-3. Control Interface Cable

Table 4-2. Control Cable Signal Definitions

Pin	I/O	Signal	Description
2	O	HS3~/RWC~	The hard disc controller uses HS3~ to select one of 16 R/W heads. RWC~ is not used with 16 head drives. RWC~ reduces the write current on the inner cylinders.
26,28	O	DS1~ or DS2~	Drive select lines 1 or 2 are used to select drive 1 and drive 2 respectively.
4,18,14	O	HEAD SELECT 2~, HEAD SELECT 1~, HEAD SELECT 0~	These three signals together with HS3~ are decoded by the drive to select one of eight or 16 R/W heads.
6	O	WRITE GATE~	This signal is asserted when valid data is to be written on a disc. It is deasserted when WRITE FAULT~ signal from the selected drive is detected.
24	O	STEP~	This signal with the DIRECTION IN~ signal position the R/W heads to the desired cylinder. STEP~ pulses once for each step.
34	O	DIRECTION IN~	This signal determine the direction in which the R/W heads move when the STEP~ line is pulsed. DIRECTION IN~ = 0 move toward the spindle DIRECTION IN~ = 1 move away from spindle

Table 4-2. Control Cable Signal Definitions (Cont.)

Pin	I/O	Signal	Description
8	I	SEEK COMPLETE~	This signal informs the disc controller that the head of a selected drive has reached desired cylinder and has stabilized.
10	I	TRACK 000~	The selected drive asserts this signal line if the R/W head is over track 0.
12	I	WRITE FAULT~	It is asserted by the selected drive when a write error occurred. While this signal is being asserted, the command in progress aborts and no other disc command can be executed.
20	I	INDEX~	It indicates the start of a track. It pulses once at each disc revolution.
22	I	READY~	It is asserted by the selected drive to inform the controller that the drive motor is up to speed.

Data Interface Pin Assignments and Description

The data lines between the hard disc controller and the two disc drives are connected to J2 and J3 at board upper edge (see board blank drawing for the exact location). The data lines are defined in Figure 4-4.

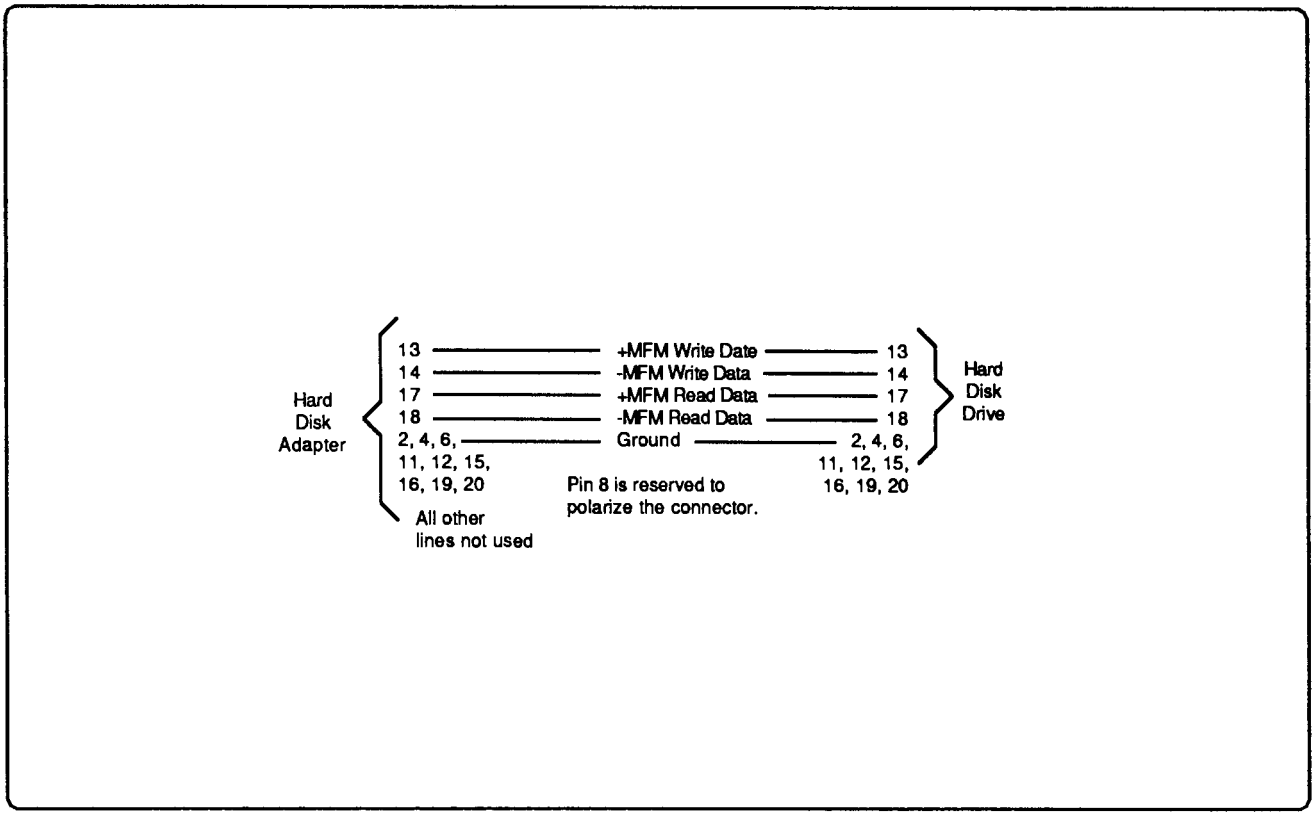


Figure 4-4. Data Interface Cable

Hard Disc Drive Activity LED Connector

The LED connector is a 4-pin header that connects with a reversible cable to the Vectra front panel. The hard disc controller lights the LED when the hard disc drive is busy or the host asserts RESET. The following shows the connector pin assignments and functions.

Pin	Signal Name
1,4	+LED; connects to LED anode.
2,3	-LED; connects to LED cathode.

Disc Drive Support

The card provides a standard ST506/412 interface for compatible drives with two flat ribbon cables for control and data signals. Drives supported include:

- D1296A (HP45896M) 20 MB Internal Hard Disc Drive.
- D1297A (HP45897M) 40 MB Internal Hard Disc Drive.

Recording Specifications

Encoding method:	MFM
Data rate	5.0 MBit per Sec
Sector format:	512 bytes/sector, 17 sectors/track soft sectored formatted, 256 bytes/sector, read only.
Interleave:	2:1
Drives supported:	2 maximum
Heads supported:	16 maximum
Tracks supported:	2048 maximum
Hard error rate:	less than 1 per 10(E12) bits read
Soft error rate:	less than 1 per 10(E10) bits read
Seek error rate:	less than 1 per 10(E06) seeks

Read/Write Control Specifications

Max. acquisition time:	12.8 us @5.0 MBS
Read margin:	+/- 16 nanoseconds
Asymmetry tolerance:	30 nanoseconds measured 5MHz RAW MFM periods of 185ns, 215ns, 185ns.
Write precompensation:	12 ns

Error Correction Specifications

Method:	Polynomial division
Degree:	32
Forward polynomial:	X(E32)+X(E28)+X(E26)+X(E19)+X(E17)+ X(E10)+X(E06)+X(E02)+1
Reciprocal polynomial:	X(E32)+X(E30)+X(E26)+X(E22)+X(E15)+ X(E13)+X(E06)+X(E04)+1
Record length (r):	516 X 8 bits maximum
Correction span (b):	5 bits
Single burst detection:	r=516X8
Width b=0	32 bits
Width b=5	19 bits
Double burst detection span:	r=512X8
Width b=0	3 bits
Width b=5	3 bits
Non-detection probability:	2.3(E-10), r=516X8, b=5
Miscorrection Probability:	1.57(E-5), r=516X8, b=5

Flexible Disc Controller (FDC) Subsystem

Jumper Configurations

Jumper block W1 selects the location of the interface registers in the system I/O map. The I/O address can be either the primary addressing, 3F0H through 3F7H (operational state-default) or the secondary addressing, 370H through 377H. The jumper can also be used to select or deselect the flexible disc controller subsystem by putting it in the middle (deselected) position. Figure 4-1 shows the jumper locations. The jumpers are set according to Figure 4-5.

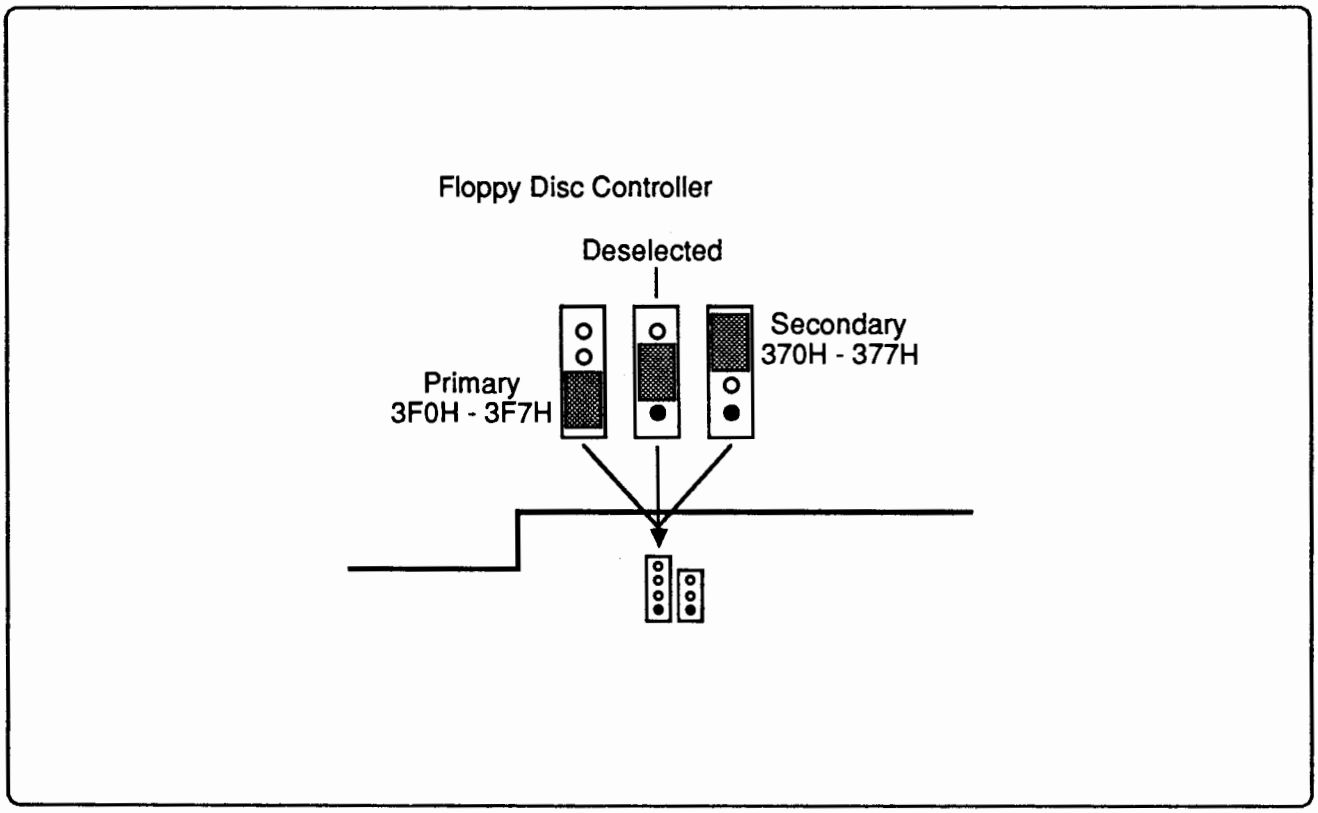


Figure 4-5. FDC Jumpers

Basic Function

The flexible disc controller subsystem generates the signals which control the electromechanical parts of the drive, interprets the status signals received from the drive, and converts between parallel and serial data formats.

The FDC chip transfers parallel data to and from the system memory space through DMA (Channel 2). Commands to the FDC chip and status information from it are transferred by programmed I/O. Command termination and error conditions are signaled through interrupts (IRQ6). The FDC phase locked loop (PLL) supports 250kHz, 300kHz, or 500kHz data rates. The data rates are selected by the digital control port.

Operations and Commands

The FDC subsystem is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the host. The results after execution of the command may also be a multibyte transfer back to the host. The commands consists of three phases: Command Phase, Execution Phase, and the Result Phase.

- Command Phase - The FDC receives all information required to perform a particular operation from the host
- Execution Phase - The FDC performs the operation is was instructed to do.
- Result Phase - After completion of the operation, status and other housekeeping information are made available to the host.

The commands and required parameter and their results are in the following tables. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written. An "R" indicates a result byte to be read by host.

The bytes of data which are sent to the FDC to form the command phase and are read out of the FDC in the result phase must occur in the order shown in the following command tables. This is the command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phases is allowed After the last by of data in the command phase is sent to the FDC, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the FDC is ready for a new command.

It is important to note that during the result phase all bytes shown in the following tables must be read. The READ DATA command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the READ DATA command. The FDC chip will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								4 bytes are compared
	W	<---------- N ---------->								against header on disc
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- DTL---------->								
EXECUTION										Data transfer between FDD and host.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								4 bytes are compared
	W	<---------- N ---------->								against header on disc
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- DTL---------->								
EXECUTION										Data transfer between FDD and host.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								4 bytes are compared
	W	<---------- N ---------->								against header on disc
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- DTL---------->								
EXECUTION										Data transfer between FDD and host.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								4 bytes are compared
	W	<---------- N ---------->								against header on disc
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- DTL---------->								
EXECUTION										Data transfer between FDD and host.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								
	W	<---------- N ---------->								
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- DTL---------->								
EXECUTION										Data transfer bet. FDD and host. FDD reads all data fields from index hole to EOT
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Read a Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	MF	0	0	1	0	1	0	Command Code
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The 1st correct ID info. on the cylinder is stored in data reg.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								read during execution
	R	<---------- R ---------->								phase from disc.
	R	<---------- N ---------->								

Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	MF	0	0	1	1	0	1	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- N ---------->								Bytes/Sector
	W	<---------- SC ---------->								Sectors/Track
	W	<---------- GPL ---------->								Gap 3
	W	<---------- D ---------->								Filler Byte
EXECUTION										FDC formats an entire track.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								In this case, the ID
	R	<---------- H ---------->								info has no meaning.
	R	<---------- R ---------->								
	R	<---------- N ---------->								

Format a Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								
	W	<---------- N ---------->								
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- STP---------->								
EXECUTION										Data compared between FDD and host.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Scan Equal

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								
	W	<---------- N ---------->								
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- STP---------->								
EXECUTION										Data compared between FDD and host.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Scan Low or Equal

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- C ---------->								Sector ID info. prior
	W	<---------- H ---------->								to command execution.
	W	<---------- R ---------->								
	W	<---------- N ---------->								
	W	<---------- EOT ---------->								
	W	<---------- GPL ---------->								
	W	<---------- STP---------->								
EXECUTION										Data compared between FDD and host.
RESULTS	R	<---------- ST0 ---------->								Status information
	R	<---------- ST1 ---------->								after the command
	R	<---------- ST2 ---------->								execution.
	R	<---------- C ---------->								Sector ID information
	R	<---------- H ---------->								after the command
	R	<---------- R ---------->								execution.
	R	<---------- N ---------->								

Scan High or Equal

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	0	0	0	0	1	1	1	Command Code
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retrack to Track 0.

Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	0	0	0	1	0	0	0	Command Code
RESULTS	R	<---------- ST0 ---------->								Status info. about the
	R	<---------- PCN ---------->								FDC at the end of seek operation.

Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	0	0	0	0	0	1	1	Command Code
	W	<--- SRT ---->					<--- HUT ---->			
	W	<---------- HLT ---------->							ND	

Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	0	0	0	0	1	0	0	Command Code
	W	X	X	X	X	X	HS	US1	US0	
RESULTS	R	<---------- ST3 ---------->								Status info about the FDC.

Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
COMMAND	W	0	0	0	0	1	1	1	1	Command Code
	W	X	X	X	X	X	HS	US1	US0	
	W	<---------- NCN ---------->								
EXECUTION										Head is positioned over proper cylinder on the disc.

Seek

Command Symbol Descriptions

Symbol	Description
C	Cylinder number; the current/selected cylinder (track) numbers, 0 through 255 of the medium.
D	Data pattern which is going to be written into a sector.
D7-D0	8 bit data bus, D7 is the MSB and D0 is the LSB.
DTL	Data Length; when N is defined as 00, DTL is which users are going to read out or write into the sector.
EOT	End of Track (the final sector number on a cylinder). During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	Length of Gap 3. During the FORMAT Command it determines the size of Gap 3.
H	Head number 0 or 1, as specified in the ID field.
HLT	Head Load Time in FDD (2 to 254ms in 2ms increments).
HS	Head Select, either 0 or 1.
HUT	Head Unload Time after a Read or Write operations has occurred (16 to 240ms in 16ms increments).
MF	If MF is low ("0") FM mode is selected, and if it is high, MFM mode is selected.
MT	If MT is high ("1"), a multitrack operation is performed. If MT=1 after finishing Read/Write operation on disc side 0, FDC will automatically start searching for sector 1 on disc side 1.
N	Number of data bytes written in a sector.
NCN	New Cylinder Number which is going to be reached as a result of the SEEK operation. Desired position of head.
ND	It is the Non-DMA mode operation.
PCN	The cylinder number at he completion of the SENSE INTERRUPT STATUS command. Position of head at present time.
R	The sector number which will be read or written.

Command Symbol Descriptions (Cont.)

Symbol	Description
R/W	Read or Write signal.
SC	The number of sectors per cylinder.
SK	Skip deleted data address mark.
SRT	Stepping rate of the FDD (1 to 16ms in 1ms increments). It applies to all drives. In 2's complement format, i.e. F(Hex)=1ms, E(Hex)=2ms, etc.
STP	During the SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data send from the host via DMA operation, if STP=2, then alternate sectors are read and compared.
US0-US1	Selected drive; binary encoded, 1 of 4.
ST0-ST3	The four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These register should not be confused with the main status register These registers may be read only after a command has been executed and contains information relevant to that particular command. The followings are the bit definitions for these 4 command status registers.

ST0:

Bit	Name	Definition
0-1	US0, US1	UNIT SELECT 0, UNIT SELECT 1 - Binary encoded to indicate the drive's unit number at interrupt. Bit 1 Bit 0 Drive Selected --- 0 0 A 0 1 B 1 0 Unused 1 1 Unused
2	HS	HEAD SELECT - Indicate the state of the head at interrupt.
3	NR	NOT READY - This bit is set, when the disc drive is in the not ready state and a READ or WRITE command is issued.
4	EC	EQUIPMENT CHECK - This bit is set, if a fault signal is received from the FDD or if the track 0 signal fails to occur after 255 step pulses (Recalibrate command).
5	SE	SEEK END - This bit is set when the FDC completes the SEEK command.
6-7	IC	INTERRUPT CODE - Encoded in binary for the interrupt code: Bit 7 Bit 6 Definition --- 0 0 Normal termination of command. Command was completed and properly executed. 0 1 Abnormal termination of command. Execution of command was started but was not successfully completed. 1 0 Invalid command issued. Command which was issued was never started. 1 1 Abnormal termination because during command execution the ready signal from disc drive changed state.

ST1:

Bit	Name	Definition
0	MA	MISSING ADDRESS MARK - This bit is set if: * the FDC cannot detect the address mark after encountering the index hole twice. OR * the FDC cannot detect the data address mark or deleted data address mark. Also at the same time status register bit 2 will be set to 1.
1	NW	NOT WRITABLE - During execution of Write Data, Write Deleted Data or Format A Cylinder command, if the FDC detects a write protect signal from the FDD, this bit is set to 1.
2	ND	NO DATA - This bit is set, if: * The FDC cannot find the sector specified in the internal data register, during execution of Read Data, Write Deleted Data or Scan command. * The FDC cannot read the ID field without an error, during execution of Read ID command. * The starting sector cannot be found during execution of the Read A Cylinder command.
3	-	Not used, this bit is always set to 0
4	OR	OVERRUN - This bit is set to 1 if the FDC is not serviced by the host system during the data transfers within a certain time interval.
5	DE	DATA ERROR - This bit is set when the FDC detects a CRC error in either the ID field or the data field.
6	-	Not used, this bit is always set to 0.
7	EN	END OF CYLINDER - This bit is set to 1 when the FDC tries to access a sector beyond the final sector of a cylinder.

ST2:

Bit	Name	Definition
0	MD	MISSING ADDRESS MARK IN DATA FIELD - This bit is set if the FDC cannot find a Data Address mark or Deleted Data Address Mark when data is read from the medium.
1	BC	BAD CYLINDER - This bit is related to the ND bit. This bit is set when the contents of C on the medium is different from that stored in the internal data register and the contents of C is FF(hex).
2	SN	SCAN NOT SATISFIED - This bit is set to 1 if the FDC cannot find a sector on the cylinder which meets the condition during execution of the SCAN command.
3	SH	SCAN EQUAL HIT - This bit is set to 1 if the condition of "equal" is satisfied, during execution of the SCAN command.
4	WC	WRONG CYLINDER - This bit is related to the ND bit. This bit is set to 1 when the contents of C on the medium are differnt from that stored in the internal data register.
5	DD	DATA ERROR IN DATA FIELD - This bit is set to 1 if FDC detects a CRC error in the data field.
6	CM	CONTROL MARK - This bit is set to 1 if the FDC encounters a sector which contain a Delected Data Address Mark during execution of the READ DATA or SCAN command.
7	-	Not used, this bit is always set to 0.

ST3:

Bit	Name	Definition
0	US0	UNIT SELECT 0 - This bit is used to indicate the status of the Unit Select 0 signal to the FDD.
1	US1	UNIT SELECT 1 - This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
2	HD	HEAD ADDRESS/SELECT - This bit is used to indicate the status of the Side Select signal of the FDD.
3	WP	WRITE PROTECTED - This bit is used to indicate the status of the WRITE PROTECT signal from the FDD.
4	T0	TRACK 0 - This bit is used to indicate the status of the Track 0 signal from the FDD.
5	RY	READY - This bit is always be a logic 1. The drive is presumed to be ready.
6	WP	WRITE PROTECTED - This bit is used to indicate the status of the WRITE PROTECT signal from the FDD.
7	0	Not used, this bit is always set to 0.

System to FDC Subsystem Interface

This subsystem is designed for compatibility with the industry standard disc formats, both single and double density. It is designed around compatibility with the NEC uPD765A flexible disc controller.

The flexible disc controller subsystem interfaces with the microprocessor through six registers. There are three write registers and three read registers. Table 4-3 lists the registers and their primary and secondary I/O addresses.

Table 4-3. Accessible Registers

Register	R/W	Pri/Sec.
Digital Output Register	W	3F2H/372H
FDC Status Register	R	3F4H/374H
FDC Data Register	R/W	3F5H/375H
Digital Control Register	W	3F7H/377H
Digital Input Register	R	3F7H/377H

Digital Output Register (Write only, 3F2H or 372H)

This register controls the disc drive spindle motors and selects the desired disc drive.

Bit	Data	Definition
0	0	Drive select, Drive A
0	1	Drive select, Drive B
1		Reserved
2	0	FDC reset, active low will reset
3	1	Interrupt and DMA enable, active high
4	1	Drive A motor enable, active high turns on motor 5 1/4 " drive
5	1	Drive B motor enable, active high turns on motor 5 1/4 " drive
6		Reserved
7		Reserved

Digital Control Register (Write only, 3F7H or 377H)

The two LSBs of the digital control register select the desired data rate. Clock switchover is "deglitched", allowing continuous operation after changing the data rate.

Bit	Definition
0, 1	Least significant bit in rate select code of PLL Bit Data Rate 1 0 (kHz) 0 0 500 0 1 300 1 0 250 1 1 Unused
2-7	Reserved

FDC Status Register (Read only, 3F4H or 374H)

This is an 8-bit main status register. This register contains the status information to facilitate the transfer of data between the host and the FDC, and may be accessed at any time.

Bit	Data	Definition
0		Disc drive A Busy (DBA) in seek mode.
1		Disc drive B busy (DBB) in seek mode.
2-3		Reserved
4		Disc controller is busy (CB) read/write being executed.
5		Disc controller is in non-DMA mode (NDM).
6	1	Data Input/Output (DIO). Data transfer from the data register of the FDC to the host.
	0	Data transfer from the host to the data register of the FDC.
7	1	Request for master(RQM) indicates data register is ready to send or receive data to or from the host.
	0	Data register is not ready for data transfer to and from host.

Note that the FDC contains five status registers. The main status register mentioned above (3F4H or 374H) may be read by the host at any time. The other four status registers (ST0, ST1, ST2 and ST3) are available only during the result phase and may be read only after completing a command. The particular command that has been executed determines how many of the status registers will be read.

The 8 bit data register (which actually consists of several register in a stack with only one register presented to the data bus at a time) stores data, command, parameters and flexible disc drive status information. Data bytes are read out of, or written into, the data register in order to program or obtain the results after a particular command.

FDC Data Register (Read/write, 3F5H or 375H)

This is a bi-directional register. Write Function: 8-bit data is written to FDC chip as commands via programmed I/O and write data during disc transfers via DMA.

Read Function: 8-bit data is read from FDC chip as result of commands via programmed I/O and read data during disc transfers via DMA.

Digital Input Register (3F7H or 377H)

This register is shared with the hard disc controller - bits 0-6 are used in the hard disc controller subsystem. The flexible disc controller uses the following information.

Bit	Definition
0-6	Used by the hard disc subsystem
7	State of the disc change line. Becomes active when the drive door is opened and at power-on. It will remain active until reset when a step pulse is issued. It is active high.

FDC to Disc Drive Interface

The 5 1/4 inch disc drive interface with the controller is through control signals, status signals and data signals. The 5 1/4 inch drives are daisy-chained on one connector and cable. Figure 4-6 shows the pin assignments for the 34-pin connector. The input or output direction of the signals are referenced from the card.

In the HP Vectra system the HP45812A 1.2 MB Internal Flexible Disc Drive provides a DISC CHG~ signal on the drive interface pin 34. This signal indicates the detection of the drive door being opened. The HP45811A 360 KB Internal Flexible Disc Drive does not provide a DISC CHG~ signal on pin 34. Thus, this signal will always be inactive and the system cannot detect a possible media change via hardware. (Refer to HP Vectra Technical Reference Manual Volume 2: System BIOS for the appropriate techniques to accomplished this detection.)

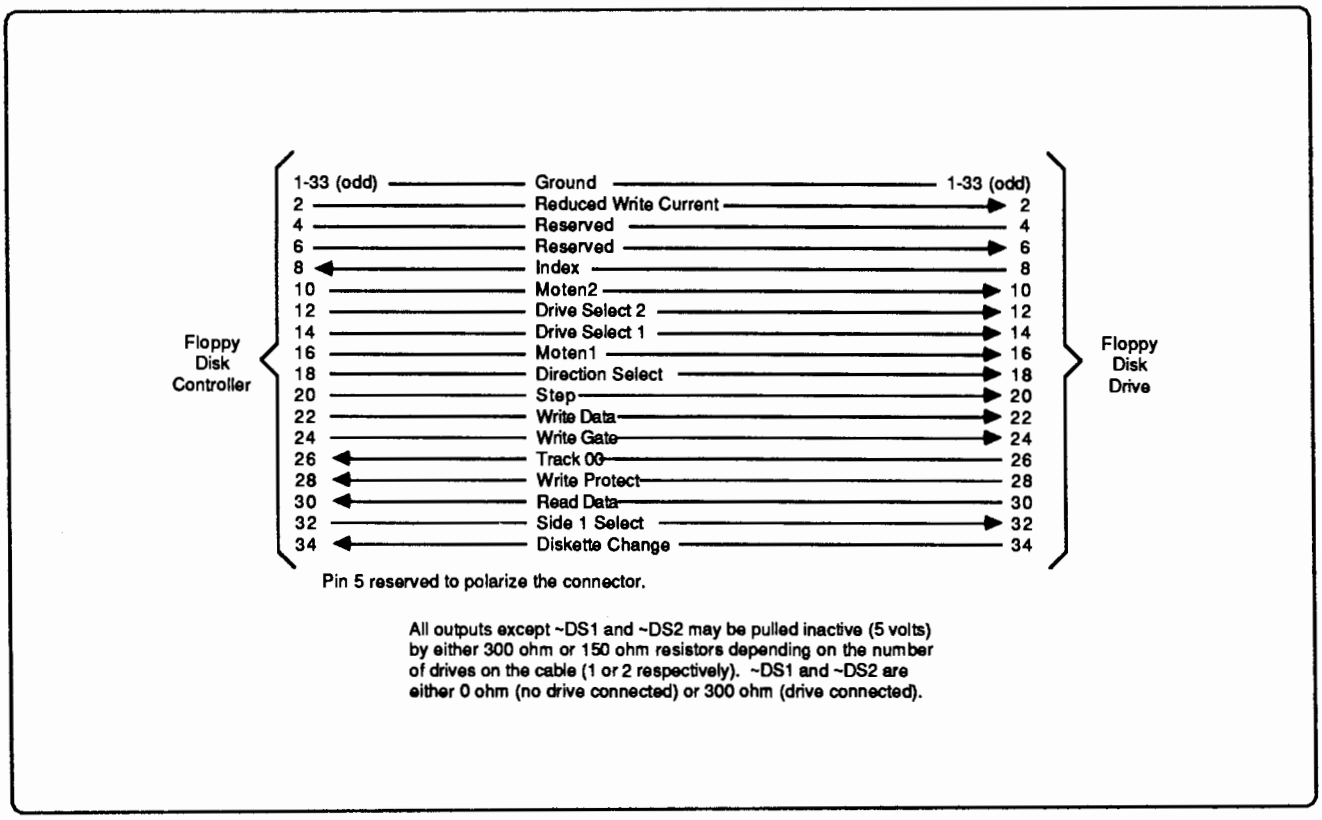


Figure 4-6. Control Interface Cable

Table 4-4 shows signal descriptions for the interface between the controller and the 5 1/4 inch flexible disc drives.

Table 4-4. Interface Cable Signal Definitions

Pin	I/O	Signal	Description
18	O	DIRECTION~	Active level indicates the read/write head to move toward the spindle. Inactive level instructs the heads to move away from the spindle.
14,12	O	DS1~ or DS2~	Drive select lines 1 or 2 are used by drives 1 and 2 to degate all adapter and receiver drivers from the attachment, except MOTEN~, when the line associated with a drive is inactive.
32	O	HEAD SELECT~	Head 1 will be selected when this line is active. An inactive level will select the head on side 0.
10,16	O	MOTEN1~ or MOTEN2~	MOTEN~ controls the spindle motor of the drive (1 or 2) associated with each line. The line controls the spindle motor such that it starts when the line becomes active and stops when the line becomes inactive.
2	O	REDWRCUR~	Selects read channel filters and write current on the 1.2 MB drive. It is active only when the PLL is in 300kHz mode and inactive for the 500kHz and 250kHz modes.
20	O	STEP~	The selected drive moves the read/write head one cylinder in or out per the direction line for each pulse present on this line. Motion is started each time the signal changes from an active to inactive level.
24	O	WRITE ENABLE~	Disables write current in the drive head unless this line is active.
30	I	READ DATA~	The selected drive supplies a pulse on the line for each flux change encountered on the disc.

Table 4-4. Interface Cable Signal Definitions (Cont.)

Pin	I/O	Signal	Description
22	O	WRITE DATA~	For each inactive to active transition of this line while write enable is active, the selected drive causes a flux change to be stored on the disc.
34	I	DISC CHG~	Indicates that the drive door has been opened.
8	I	INDEX~	The selected drive supplies one pulse per disc revolution on this line.
26	I	TRACK 00~	The selected drive makes this line active if the read/write head is over track 0.
28	I	WRITE PROTECT~	The selected drive makes this line active if a write-protected disc is mounted in the drive.

Disc Drive support

The card provides a standard ST506/412 interface for compatible drives including the current HP internal flexible disc drives such as:

- HP45811A 360 KB 5" Internal Flexible Disc Drive.
- HP45812A 1.2 MB 5" Internal Flexible Disc Drive
- HP45813A 1.44 MB 3.5" Internal Flexible Disc Drive.

Recording Specifications

Encoding method:	MFM
Data rate:	500, 300, 250 KBPS - synchronously switched.
Sector format:	Soft sector 360KB = 8(or 9) sectors/track 1.2MB = 15 sectors/track
Interleave:	2:1
Drives supported:	2
Heads supported:	2
Tracks supported:	256
Hard error rate:	less than 1 per 10(E12) bits
Soft error rate:	less than 1 per 10(E10) bits
Seek error rate:	less than 1 per 10(E06) seeks
Precompensation:	125 ns all tracks all data rates.

Read/Write Control Specifications

Read margin:	600 ns @360K drive 300 ns @1.2M drive 400 ns @1.2M drive with 360K media
Asymmetry tolerance:	700 ns @360K drive 350 ns @1.2M drive 700 ns @1.2M drive with 360K media and Reduce Write Current = active
MSV:	+/- 2%
ISV:	+/- 2%

NOTE

When No Index is returned by the drive, the FDC subsystem MUST NOT generate an ABORT command, i.e. DO NOT generate an interrupt.

Serial DataComm Interface Subsystem

The serial data communication subsystem provides asynchronous communications at RS-232C levels. Other features include: a programmable baud rate of 75 to 19200 bps, character length of 5, 6, 7, or 8 bits, a stop bit of 1, 1 1/2, or 2, a parity bit, modem control signals, full double buffering, and automatic adding or deletion of start, stop, and parity bits.

Jumper Configurations

The serial output port can be addressed as either communications Port 1 or communications Port 2 by jumper block W4. These two ports are mapped to different I/O address and have different interrupt level. Port 1 has I/O address 3F8H through 3FFH and interrupt level 4. Port 2 has the I/O address 2F8H through 2FFH and interrupt level 3. The selection of ports/interrupts, as well as inhibiting the serial port, is performed by a jumper. The location of the jumpers are shown in Figure 4-1. jumpers are set according to Figure 4-7.

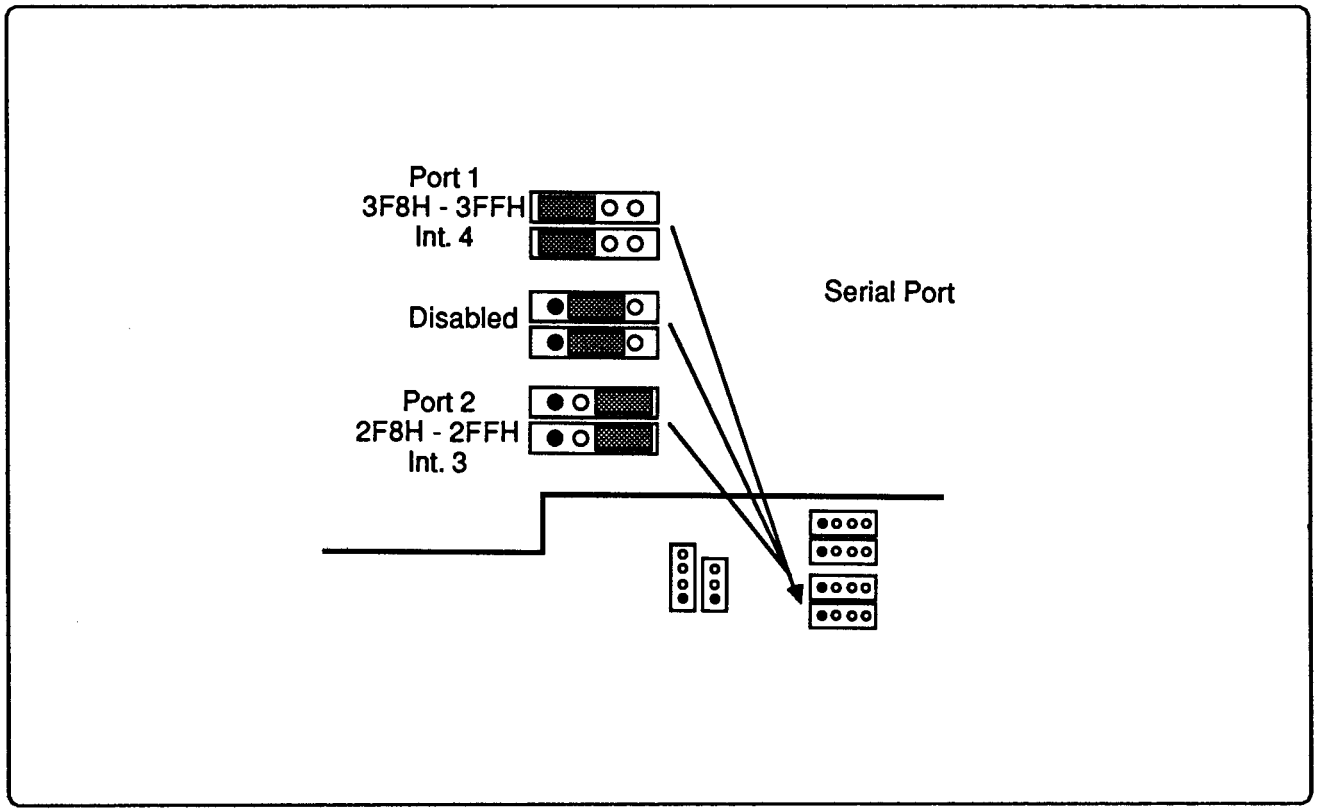


Figure 4-7. Serial Port Jumpers

Serial Port Interface

The serial port uses an RS-232C connector type D 9-pin male Table 4-5 defines the pin assignments and signal descriptions for this connector.

Table 4-5. Serial Port Pin Assignments

Pin	I/O	Signal	Description
1	I	CF (CD)	When active, it indicates the device has detected the data carrier.
2	I	BB (RX)	Rx data
3	O	BA (TX)	Tx data
4	O	CD (DTR)	When active, it informs the device that the card is available to communicate.
5		AB (Gnd)	GND, ground
6	I	CC (DSR)	When active, it indicates the device is ready to establish the communications link in order to transfer data.
7	O	CA (RTS)	When active, it informs the device that the card is ready to transmit data.
8	I	CB (CTS)	When active, it indicates the device is available to receive data.
9	I	CE (RI)	When active, it indicates the device has a telephone ringing signal.

Registers

The serial datacomm subsystem has 11 programmable registers. The system programmer may gain access or control any of the registers through the system CPU (microprocessor). Table 4-6 defines the registers and their addresses.

Table 4-6. Serial Datacomm Subsystem Registers

Register	R/W	Port 1 Port 2
Transmit Buffer	W	3F8H 2FH8*
Receive Buffer	R	3F8H 2F8H*
Divisor Latch LSB	R/W	3F8H 2F8H*
Divisor Latch MSB	R/W	3F9H 2F9H*
Interrupt Enable Register	R/W	3F9H 2F9H*
Interrupt ID Register	R	3FAH 2FAH
Line Control Register	R/W	3FBH 2FBH
Modem Control Register	R/W	3FCH 2FCH
Line Status Register	R/W	3FDH 2FDH
Modem Status Register	R/W	3FEH 2FEH
Reserved		3FFH 2FFH

* Access to these registers is determined by the state of the Line Control Register (3FBH or 2FBH).

Transmit Buffer Register (Write only, 3F8H or 2F8H)

This register contains the characters to be transmitted via the serial connector. Data bit 0, the least significant bit (LSB), is transmitted first and data bit 7, the most significant bit (MSB), is the last bit transmitted.

Receive Buffer Register (Read only, 3F8H or 2F8)

This register contains the characters received via the serial connector. Data bit 0, the least significant bit (LSB), is received first and data bit 7, the most significant bit (MSB), is the last bit received.

Bit 7 of the Line Control Register (3FBH or 2FBH) determines whether the Transmit Buffer Register or the Divisor Latch Register LSB is accessed and whether the Interrupt Enable Register or the Divisor Latch Register (MSB) is accessed.

Divisor Latch Registers LSB and MSB (Read/Write, 3F8H or 2F8H, 3F9H or 2F9H)

The divisor latch LSB (3F8H or 2F8H) and the divisor latch MSB (3F9H or 2F9H) registers are used to control the baud-rate of the transmitted and received data.

This subsystem has a clock of 1.8432MHz. This frequency is divided by any divisor from 1 to 65,525 as set on the two divisor latches. The output frequency is 16 times the baud-rate.

The two divisor latches must be loaded to define the baud-rate before attempting to transmit or receive data. When either of the latches is loaded, a 16-bit baud-rate counter is immediately loaded to prevent long counts on the first load.

Table 4-7 gives examples of loading the divisor latch registers to determine the baud-rate.

Table 4-7. Divider Latch Values

Baud Rate	Divisor	MSB (XF9H) Bits	(XF8H) Bits LSB
		7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
75	1536	0 0 0 0 0 1 1 0	0 0 0 0 0 0 0 0
110	1047	0 0 0 0 0 1 0 0	0 0 0 1 0 1 1 1
300	384	0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0
600	192	0 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0
1200	96	0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0
2400	48	0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0
4800	24	0 0 0 0 0 0 0 0	0 0 0 1 1 0 0 0
9600	12	0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0
19200	6	0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 0

Interrupt Enable Register (Read/Write, 3F9H or 2F9H)

This register enables and disables the four types of interrupt from the serial datacomm subsystem.

Bit	Data	Interrupt
0	1	Enable the received data available interrupt.
	0	Disable interrupt.
1	1	Enable transmitter holding register empty interrupt.
	0	Disable interrupt.
2	1	Enable the receiver line status interrupt.
	0	Disable interrupt.
3	1	Enable the modem status interrupt.
	0	Disable interrupt.
4-7	0	Not Used.

When the enabled interrupt signal is received it activates the chip interrupt (INTRPT) output signal which is sent to the system. When all interrupts are disabled, the Interrupt Enable Register and the INTRPT output signal are disabled. The other registers are not affected.

Bit 7 of the Line Control Register (3FBH or 2FBH) determines whether the divisor latch MSB or the Interrupt Enable Register is accessed.

Interrupt Identification Register (Read only, 3FAH or 2FAH)

This register identifies the highest priority pending interrupt signal. When this register is addressed it inhibits the highest priority interrupt. No other interrupts are acknowledged until this inhibited interrupt is cleared.

Bit	Data	Definition
0	0	Interrupt pending.
1-2		Identifies the pending interrupt with the highest priority as in the following: Bit 1 2 Interrupt Condition 1 1 Receiver line status 1 0 Received data avail. 0 1 Trans. buffer empty 0 0 Modem status
3-7	0	Not Used.

The following defines the interrupt priorities.

Interrupt	Priority	Interrupt Source	Clear Interrupt
Receiver line status	1 (Highest)	Overrun error or parity error or framing error or break (200mS space on receive data line).	Reading the line status register.
Received data available	2 (Second)	Data available in receive buffer.	Reading the receive buffer register.
Transmitter buffer register empty	3 (Third)	Data transmitted from transmit buffer.	Reading the interrupt identification register (if source), or writing to the transmit buffer register.
Modem status	4 (Fourth)	CB, CC, CE or CF signal received.	Reading the modem status register.

Line Control Register (Read/Write, 3FBH or 2FBH)

This register controls the format of the data communications.

Bit	Data	Definition
0-1		Specifies the number of bits in each transmitted or received character as in the following: Bit 0 1 — Character Length in bits 1 1 — 8 1 0 — 7 0 1 — 6 0 0 — 5
2	0 1	One stop bit is generated or deleted in the data sent or received. 1 1/2 stop bit is generated or deleted for 5-bit words. For a 6, 7, or 8-bit word, 2 stop bits are generated or deleted.
3	0 1	Disable parity bit. A parity bit is generated (transmit data) or deleted (receive data).
4	0 1	When bit 3 is 1, parity bits sent or checked odd. When bit 3 is 1, parity bits sent or checked even.
5	1 0	When bit 3 is 1, the parity bit is set 0 for even parity and 1 for odd parity. Stuck parity disabled.
6	1 0	Break bit. The transmit data line is set to the space state (0) and remains at that state regardless of the state of the output buffer register. Set-breaking is disabled.
7	1 0	Address selection bit. Set to gain access of the divisor latches of the baud-rate generator during a read/write operation. Reset to gain access of the receiver buffer register, the transmit buffer register, or the interrupt enable register.

Modem Control Register (Read/Write, 3FCH or 2FCH)

This register controls the modem signals It also allows the serial DataComm subsystem to be set into diagnostic mode. In the diagnostic mode, transmitted data is received immediately. The receiver and transmitter interrupts and the modem control interrupts are fully operational, allowing the interrupts to be tested.

Bit	Data	Definition
0	1	Data terminal ready (CD) signal active.
	0	CD signal inactive.
1	1	Request to sent (CA) signal active.
	0	CA signal inactive.
2		Controls the OUT1~ signal from the controller chip. Can be 0 or 1.
3	1	Controls OUT2~ signal from the controller chip. Enables INTRPT generated by the interrupt enable register.
	0	The OUT2~ output is forced inactive.
4	1	Enables the modem loopback feature (diagnostic test) as follows: Receiver serial input is disabled. Transmitter serial output is set to the active state. The output from the transmitter shift register is looped back to the receiver shift register. The four modem control inputs to the modem status register are disabled. The four modem control outputs from the modem control register are internally connected to the four modem control inputs
5-7	0	Not Used.

Line Status Register (Read/Write, 3FDH or 2FDH)

This register provides information on the data transfer. Bits 1 through 4 are error conditions that generate a receiver line status interrupt. This register is not to be written to.

Bit	Data	Definition
0	1	Set when a complete incoming character has been received and transferred into the receiver buffer register.
	0	Reset by reading the data in the receiver buffer register or writing 0 in it.
1	1	Indicates that data in the receive buffer register was not read by the processor before the next character was transferred into the register, thereby erasing the previous character.
	0	Reset when the host reads the Line Status Register.
2	1	Detection of a parity error.
	0	Reset when the host reads the Line Status Register.
3	1	Framing error has occurred, character does not have a valid stop bit.
	0	Reset when the host reads the Line Status Register.
4	1	The received data line was at a space state (0) for longer than a transmission time of a complete data character. (Including start, data, parity, and stop bits.)
	0	Reset when the host reads the Line Status Register.
5	1	Set when a character is transferred from the transmit buffer register to the transmit shift register indicating the card is available to transmit another character.
	0	Reset when the next character is written into the transmit buffer register.
6	1	Transmit buffer register and transmit shift register are empty.
	0	Reset when either register contains a character.
7	0	Not Used.

Modem Status Register (Read/Write, 3FEH or 2FEH)

This register provides information on the current state of the control lines from the modem or device.

Bit	Data	Definition
0	1	Set if clear to send signal (CB) input changes state.
	0	Reset when the Modem Status Register is read.
1	1	Set if data set ready (CC) input changes state.
	0	Reset when the Modem Status Register is read.
2	1	Set when the ring indicator (CE) input changes from low to a high state.
	0	Reset when the modem status register is read.
3	1	Set if the received line signal detector (CF) input changes state.
	0	Reset when the Modem Status Register is read.
4	1	Set when the CB input is active. However, if the modem loopback is enabled, this bit is equivalent to CA of XFCH (bit 1).
	0	Reset when the CB input is inactive.
5	1	Set when the CC input is active. However, if the modem loopback is enabled, this bit is equivalent to CD of XFCH (bit 0).
	0	Reset when the CC input is inactive.
6	1	Set when the CE input is active. However, if the modem loopback is enabled, this bit is equivalent to OUT1~ of XFCH (bit 2).
	0	Reset when the CE input is inactive.
7	1	Set when the CF input is active. However, if the modem loopback is enabled, this bit is equivalent to OUT2 of XFCH (bit 3).
	0	Reset when the CF input is inactive.

Parallel DataComm Interface Subsystem

The Parallel DataComm Subsystem provides a parallel port to attach devices that accept eight bits of parallel data at standard TTL levels. It includes programmable printer control such as automatic initialization, printer select, auto linefeed, and data strobe.

Jumper Configurations

The parallel output port can be addressed as either parallel Port 1 or 2 by jumper block W3. These two ports are mapped to different I/O addresses and have different interrupt levels. Port 1 is mapped to I/O address 378H through 37FH and interrupt level 7. Port 2 is mapped to I/O address 278H through 27FH and interrupt level 5. The selection of ports/interrupts, as well as inhibiting the serial port, is performed by a jumper. The location of the jumpers are shown in Figure 4-1. The jumpers are set according to Figure 4-8.

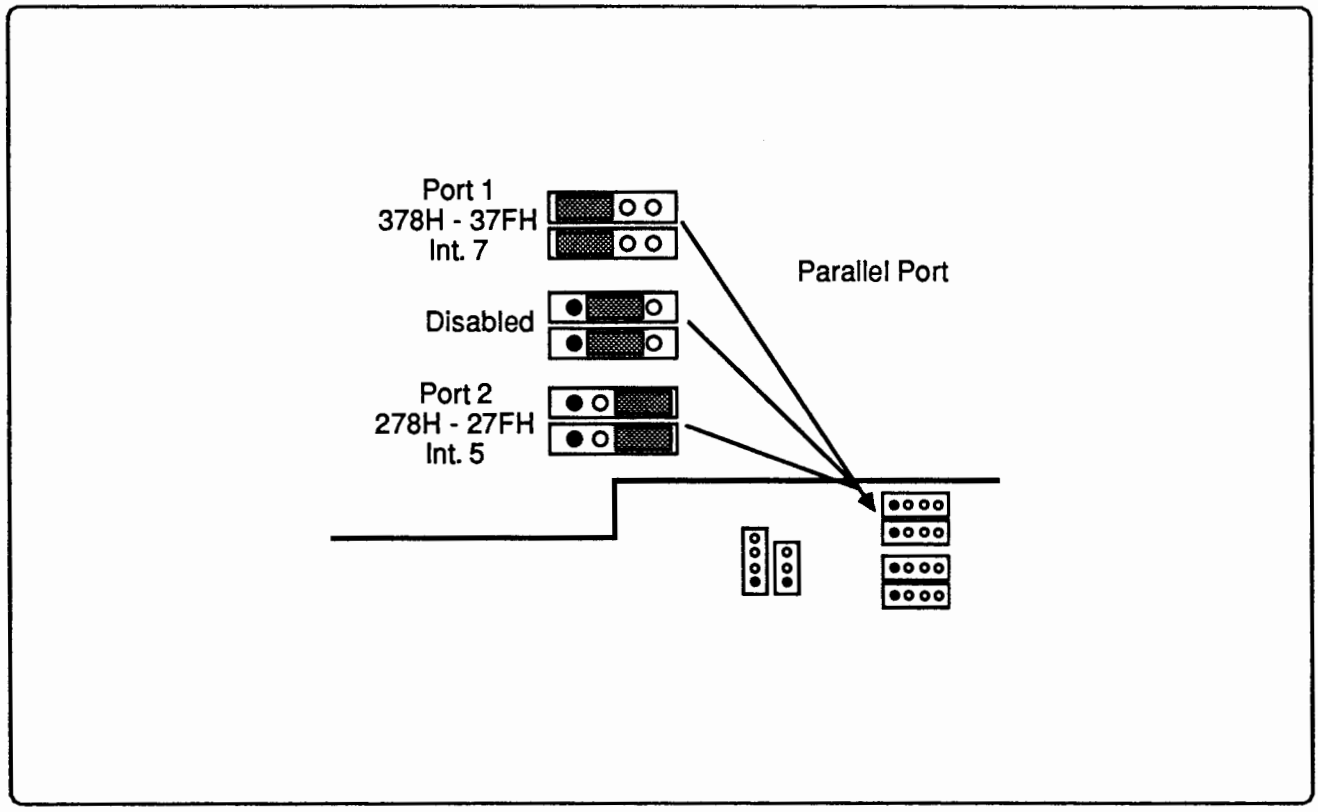


Figure 4-8. Parallel Port Jumpers

Parallel Port Interface to the System

The parallel port uses a D-type 25-pin female connector. Table 4-8 defines the pin assignments and signal descriptions for this connector.

Table 4-8. Parallel Port Pin Assignments

Pin	I/O	Signal	Definition
1	O	STROBE~	Data strobe
2	O	Data 0	Data bit 0
3	O	Data 1	Data bit 1
4	O	Data 2	Data bit 2
5	O	Data 3	Data bit 3
6	O	Data 4	Data bit 4
7	O	Data 5	Data bit 5
8	O	Data 6	Data bit 6
9	O	Data 7	Data bit 7
10	I	ACK~	Printer has processed the received character.
11	I	BUSY	Printer is busy and will not accept more data.
12	I	PE	Printer detects end of paper.
13	I	SLCT~	Printer select.
14	O	AUTO FD~	Printer to perform a linefeed after a line is printed.
15	I	ERROR~	Printer has encountered an error.
16	O	INIT~	Initialize printer.
17	O	SLCT IN~	Set low to enable the printer to accept data.
18		GND	Ground
19		GND	Ground
20		GND	Ground
21		GND	Ground
22		GND	Ground
23		GND	Ground
24		GND	Ground
25		GND	Ground

Registers

The parallel subsystem has three programmable registers. The system programmer may gain access or control any of the registers in the parallel subsystem through the 80286. Table 4-9 defines the registers and their addresses.

Table 4-9. Accessible Registers

Register	R/W	Port 1 Port 2
Data Buffer Register	R/W	378H/37CH 278H/27CH
Printer Control Register	R/W	37AH/3F8H 27AH/2F8H
Printer Status Register	R	379H/37DH 279H/27DH

Data Buffer Register (Read/Write, 378H/37CH or 278/27CH)

This register contains the data character. Reading from this address causes the character to be transferred from the port buffer to the host microprocessor. Writing to this address causes the character to be transmitted from the host microprocessor data bus to this port buffer and the parallel connector data line (DATA0-DATA7).

This register is cleared at power-up by the reset input signal.

Printer Control Register (Read/Write, 37AH/37EH or 27AH/27EH)

This register controls the printer signals. It is cleared at power-up by the reset input signal.

During a Write operation, bit 0 through 3 are output to parallel port ~STROBE (pin 1), ~AUTOFD (pin 14), ~INIT (pin 16) and ~SLCTIN (pin 17) respectively. During a Read operation, the levels on signals ~STROBE, ~AUTOFD and ~SLCTIN are inverted and read as bits 0, 1 and 3. The level on signal INIT and IRQ are read as bit 2 and bit 4, respectively, directly with no inversion.

Bit	Data	Definition
0	1	Generates an active low STROBE signal for a minimum of 500nS. The STROBE signal clocks the data from the parallel port into the printer. The valid data must be present a minimum of 0.5uS before and after the STROBE signal.
	0	STROBE inactive.
1	1	Generates the low AUTO FD signal.
	0	AUTO FD inactive.
2	0	Generates the low INIT~ signal for a minimum of 50uS.
	1	INIT~ inactive.
3	1	Generates the low SLCT IN~ signal.
	0	SLCT IN inactive.
4	1	Enables the IRQ when the ACK~ input signal changes from true to false.
	0	Disable IRQ.
5-7	0	Not Used.

Printer Status Register (Read Only, 379H/37DH or 279H/27DH)

This register provides information on the control lines from the printer. This register is cleared at power-up by the reset input signal.

Bit	Data	Definition
0-2		Not Used.
3	0	The ERROR~ input is active. The printer is either at the paper end, at an off-line state, or an error state.
4	1	The SLCT input is active. The printer is selected.
5	1	The PE input is active. The printer is out of paper.
6	0	The ACK~ input is active. The printer has received the character and is ready to accept another character.
7	0	The BUSY input is active. The printer is busy and not ready to accept data.

5

Four-Function Controller PCAs

Two types of Four-Function Controller PCAs are supported on the HP Vectra RS PC: the ST-506 Four-Function Controller PCA, identical to the Disc and Datacomm Controller Card, P/N 45945-60013 (see the section "Disc and Datacomm Controller Card") and the ESDI Four-Function Controller PCA P/N D1677A (discussed here).

As with the ST-506 Four-Function Controller PCA/Disc and Datacomm Controller Card, the ESDI Four-Function Controller PCA consists of four subsystems: the Hard Disc Controller subsystem, the Flexible Disc Controller subsystem, the Serial DataComm Interface subsystem and the Parallel DataComm Interface subsystem.

All subsystems on the ESDI Four-Function Controller PCA are identical to those on the ST-506 Four-Function Controller PCA, except for the Hard Disc Controller subsystem. That subsystem, discussed here, has a different physical drive interface hardware. However, because it is logically similar to the ST-506's hard disc controller subsystem, to the host, the ESDI hard disc controller appears identical to the ST-506.

The ESDI Four-Function Controller PCA Hard Disc Controller subsystem supports 103-, 155-, and 310-Mbyte hard disc drives. Its layout is shown in Figure 5-1.

Compatibility

The HP Vectra RS PC will not support two hard disc controllers in the unit at the same time. That is, if the ST-506 Four-Function Controller PCA is used, only another ST-506 40-Mbyte hard disc drive may be added to the system. If the ESDI Four-Function Controller PCA is used, only another ESDI 103-, 155-, or 310-Mbyte hard disc drive may be added to the system.

The ESDI Four-Function Controller PCA is compatible with: the HP Hard Disc and Datacomm Controller (P/N HP 45945-60013), the flexible disc controller in the early Vectras, and the HP serial/parallel card (P/N HP24540A) in the following areas:

- BIOS entry point
- Disc drive support
- DMA transfer for flexible disc controller
- Firmware
- Hardware interrupt request Levels
- Jumpers
- Registers
- Serial and parallel port connectors

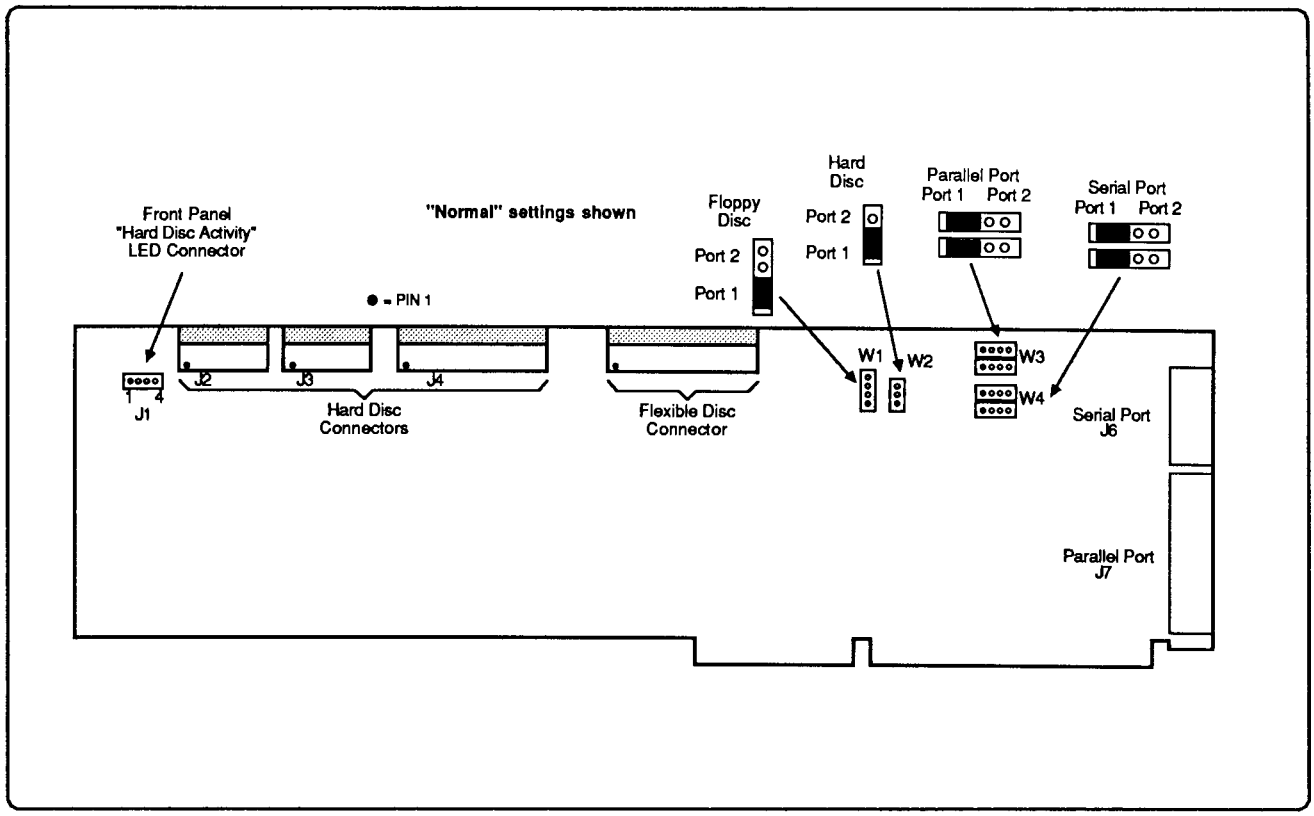


Figure 5-1. ESDI Four-Function Controller PCA

Hard Disc Controller Subsystem

Hard Disc Controller Jumper Configurations

Jumper block W2 selects the hard disc controller's interface registers in the system I/O map. The I/O address can be used to address a primary hard disc drive (1F0h through 1F7h, 3F6h, and 3F7h) or a secondary hard disc drive (170h through 177h, 376h, and 377h). The jumpers for block W2, located as shown in Figure 5-1, are set according to Figure 5-2.

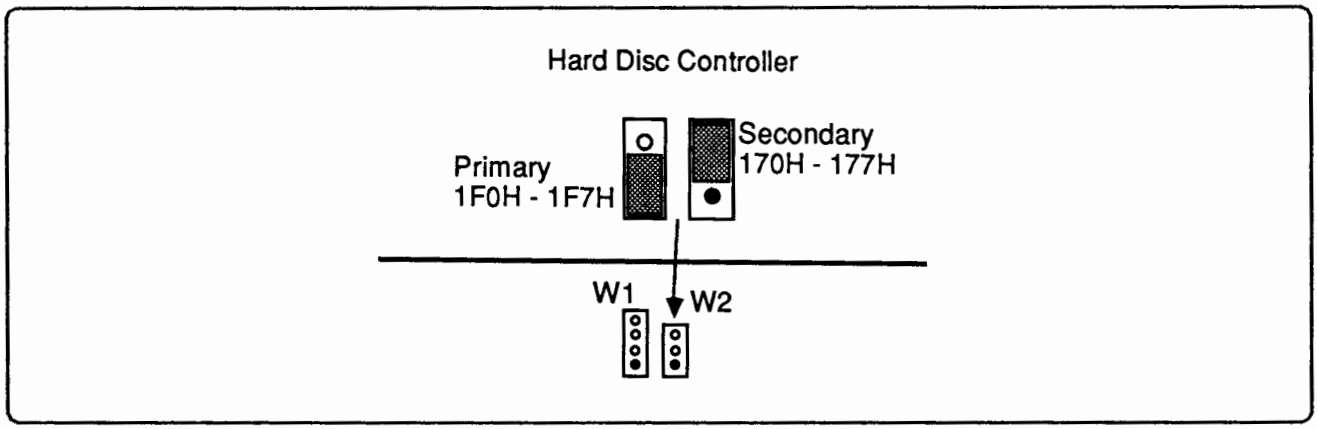


Figure 5-2. ESDI Hard Disc Controller Jumpers

Hard Disc Controller Basic Function

The hard disc controller subsystem generates the signals which control the electromechanical parts of the drive, interpret the status signals received from the drive, and convert between parallel and serial data formats.

The ESDI hard disc controller supports 256- and 512-byte sectors; high-speed, programmable I/O data transfers; error checking and correction (ECC) of up to 22 bits on data fields multiple sector operations across track and cylinder boundaries; and on-board diagnostic tests. The subsystem will support two hard disc drives with up to 16 read/write heads and 2048 cylinders.

System to Hard Disc Controller Subsystem Interface

The hard disc controller subsystem interfaces to the system bus through the address, data and programmed I/O control signals. All data transfers are 16 bits wide and occur between the bus and the data buffer memory. Control, status and ECC byte transfers are 8 bits wide and use lower data byte lines SD07-SD00 only. The bus interrupt request level is fixed at IRQ14.

The hard disc controller subsystem contains 19 registers for control and data transfer. Table 5-1 lists the registers and their primary and secondary I/O addresses.

Table 5-1. Accessible Registers

Register	R/W	I/O Address*	
		Primary	Secondary
Hard Disc Data Register (16 bits)	R/W	1F0	170
Cache Control	W	1F1	171
Error Register	R	1F1	171
Sector Count	R/W	1F2	172
Sector Number	R/W	1F3	173
Cylinder Number - Low Byte	R/W	1F4	174
Cylinder Number - High Byte	R/W	1F5	175
Sector Size, Drive/Head Select	R/W	1F6	176
Command Register	W	1F7	177
Status Register	R	1F7	177
Hard Disc Register	W	3F6	376
Alternate Status Register	R	3F6	376
Digital Input Register	R	3F7	377

* Addresses are in hex.

Hard Disc Data Register (Read/Write, 1F0h or 170h)

The data register provides access to the sector buffer for read and write operations in the programmed I/O mode. This register must not be accessed unless a Read or Write command is being executed. The register provides a 16-bit path into the sector buffer for normal Read and Write commands. When a R/W Long is issued, 4 ECC bytes are transferred in low order byte with at least 2 microseconds between transfers. "Data Request" (DRQ) must be active before the transferring of the ECC bytes.

Error Register (Read only, 1F1h or 171h)

This is a read-only register that contains specific information related to the previous command. The data are valid only when the error bit in the Status Register (1F7h or 177h) is set in the operating mode or the hard disc controller subsystem is in diagnostic mode (the state immediately after power is switched on, or after a Diagnose command). In diagnostic mode the register must be checked regardless of the status register indicator. The following are error code bit values in the error register definitions for the diagnostic mode.

Code	Definition
00	Not used, undefined
01	No error
02	Winchester Disc Controller register error
03	Sector RAM buffer data error
04	Host bus manager or pipeline register error
05	Control processor ROM checksum or RAM data error
06-FF	Not used, undefined

The following are bit definitions for the operational mode.

Bit	Data	Definition
0	1	Data Address Mark Not Found within 16 bytes of the ID field
1	1	Track 000 error
2	1	Aborted command
3	-	Not used
4	1	ID field not found
5	-	Not used
6	1	Data ECC error
7	1	Bad block detected

Cache Control Register (Write Only, 1F1h or 171h)

According to this register's state, it enables or disables the track buffer's cache option. Upon power-up and caching is enabled. By writing 55h into the Cache Control Register, and issuing the cache enable/disable command caching will be disabled. Writing AAh into Cache Control Register and issuing cache enable/disable command enables caching.

Sector Count Register (Read/Write, 1F2h or 172h)

This register defines the number of sectors to be transferred during a Verify, Read, Write, or Format command. The value written into this register is decremented by one after each sector is transferred to or from the sector buffer. Note: A 0 represents a 256 sector transfer, a 1 = one sector, etc. This register is disregarded when a single sector command is specified.

Sector Number Register (Read/Write, 1F3h or 173h)

This register holds the number of the desired sector for Read, Write, and Verify commands. The starting sector number is loaded into this register for multi-sector operation. It is incremented by one after each sector has been transferred to or from the sector buffer.

Cylinder Number Registers - Low Byte (Read/Write, 1F4h or 174h)

This register holds the least signification 8 bits of the desired cylinder number.

Cylinder Number Register - High Byte (Read/Write, 1F5h or 175h)

The least three signification bits of this register contains the three most signification bits of the desired cylinder number.

Sector Size, Drive/Head Select Register (Read/Write, 1F6h or 176h)

This register contains the following information:

Bit	Data	Definition
0-3		Head select, bit 0 is least signification bit. The hard disc controller supports 16 read/write heads.
4	0	First hard disc drive selected.
	1	Second hard disc drive selected.
5	1	Set to 1 to select 512 bytes per sector. (See also bit 6.)
6	0	Set to 0 to select 512 bytes per sector. (See also bit 5.)
7	1	Set to 1 to select ECC mode for the data field.

Status Register (Read only, 1F7h or 177h)

The hard disc controller sets up the status register with the command status after execution. A read of the status register clears interrupt request 14. The following defines the bits of the status register.

Bit	Definition
0	Error. A 1 on this bit indicates that the command ended in an error, and Error Register bits are set. The next command resets the error bit.
1	Index. This bit is set to 1 at each revolution of the disc.
2	Corrected Data. Each time the error data read from disc is corrected by the ECC algorithm, this bit is set to 1.
3	Data Request. This bit indicates that the sector buffer requests servicing during a read of write command.
4	Seek Completed. This bit is set to 1 when the read/write heads have completed a seek operation.
5	Write Fault. A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.
6	Drive Ready. When both this bit and the Seek Completed bit (bit 4) are set to 1, the hard disc drive is ready to read, write, or seek.
7	Busy. This bit is set to 1 when the hard disc controller is executing a command and no other status register bit is valid.

Command Register (Write only, 1F7h or 177h)

The Command Register accepts eight commands and command attributes to perform hard disc operations. Any code not defined in the following causes an Aborted Command error. Interrupt 14 is reset when any command is written. The following are acceptable commands to the command register. (The last five commands in the table below are extensions to the compatibility model, providing drive mechanism diagnostic capability and drive identification.) See Table 5-2 for descriptions of the commands.

Command	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Restore	0	0	0	0	X	X	X	X
Seek	0	1	1	1	0	0	0	0
Read Sector	0	0	1	0	0	0	LNG	RTY
Write Sector	0	0	1	1	0	0	LNG	RTY
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	RTY
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1
Read Drive Parameters	1	1	1	0	1	1	0	0
Initiate ESDI	1	1	1	0	0	0	0	0
Read Data Stack	1	1	1	0	0	1	0	0
Write Data Stack	1	1	1	0	1	0	0	0
Cache Enable/Disable	1	1	1	0	1	1	1	1

LNG = 0: Normal mode, normal ECC functions.
LNG = 1: Long mode.
RTY = 0: Error retries are enabled.
RTY = 1: Retries are disabled.
X = Don't care.

Table 5-2 Command Description

Command	Definition
RESTORE:	This command is used to move the R/W heads to the Track 000 position. If Track 000 is not true, within 2048 steps the Error bit in the Status Register is set and a Track 000 error is posted in the Error Register. If the ~DRIVE READY signal is de-asserted or ~ATTENTION is asserted, this command terminates with the error bit set in the Status Register, and the Error Register reports an aborted command.
SEEK:	This command moves the R/W heads to the cylinder specified in the task file cylinder high and low registers. An interrupt is generated at the completion of the command. If the ~DRIVE READY signal is de-asserted or ~ATTENTION is asserted, this command is terminated with the error bit set in the Status Register, and the Error Register reports an aborted command.
READ SECTOR:	A number of sector (1-256) can be read from the selected drive with this command. The sector count register in the task file determines the number of sector to be transferred. Multi-sector reads may cross head and cylinder boundaries. If the R/W heads are not positioned over the target track, the controller performs an implied seek to the proper cylinder. The optional long bit (L set to 1 enables Read Long) informs the disc controller whether of not to include the four ECC bytes. These four ECC bytes are transferred as individual bytes, not words, as is the data field information. The data request bit in the data register must be valid before each byte transferred and at least 2 usec will pass between each byte transferred. Data errors up to 22 bits in length will be automatically corrected on normal Read commands. If an uncorrectable error occurs, the data transfer will still take place. A multi-sector read, however, will terminate after the sector in error is read by the system. The optional retry bit (T set to 1 disables retries) disables or enables retries. The Winchester disc controller performs up to 10 automatic retries when the retry bit is enabled. The Winchester disc controller properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two automatic retries before the Winchester disc controller sets the error and status registers.

Table 5-2 Command Description (Cont.)

Command	Definition
READ SECTOR: (continued)	For ECC errors, eight retries are made at reading before a soft uncorrectable error is reported. A retry results in the reissuing of the Winchester disc controller Read Sector command. The Winchester disc controller Read Sector command attempts to verify the sector eight times before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the Winchester disc controller, the command terminates. Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command. If the ~DRIVE READY signal is de-asserted or ~WRITE FAULT asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.
WRITE SECTOR:	A number of sectors (1-256) can be written to the selected drive. The sector count register in the task file determines the number of sectors to be transferred. A Multi-sector write may cross head and cylinder boundaries. The optional long bit (L set to 1 enables Write Long) informs the controller whether or not to append the host supplied ECC bytes. These four bytes are transferred as individual bytes, not words, as is data field information. The data request bit in the data register must be valid before each byte transferred and at least 2 usec will pass between each byte transferred. The optional retry bit (T set to 1 disables retries) disables or enables retries. The Winchester disc controller performs up to 10 automatic retries when the retry bit is enabled. The Winchester disc controller properly sets the error and status registers if the retries are unsuccessful. Disabling retries allows only two automatic retries before the Winchester disc controller sets the error and status registers. The controller interrupt is generated as the data for each sector is required to be transferred into the sector buffer (except the first sector) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and the data request status is set. If the ~DRIVE READY signal is de-asserted or ~WRITE FAULT is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

Table 5-2 Command Description (Cont.)

Command	Definition
FORMAT TRACK:	The track specified by the task file is formatted with ID and Data fields according to the interleave table transferred to the buffer. The interleave table consists of two bytes per sector, the 1st byte is to indicate a bad block with a 80h (otherwise is 00h) and the second byte is for the logical sector address. The data transfer must be 512 bytes even though the table contains fewer bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. The Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80H. When switching between drives, a Restore command must be executed prior to attempting a format. Command completion will leave all data fields initialized to zeros. The completion interrupt is generated after each track has been formatted.
READ VERIFY:	This command functions similarly to a normal Read command except that data are not output to the host. One to 256 sectors may be verified at on time. The generated ECC bytes are compared with the recorded ECC bytes for data verification. A signal interrupt is generated upon completion of the command or in the even of an error. For ECC errors, eight retries are made at reading before a soft uncorrectable error is reported. A retry results in the reissuing of the Winchester disc drive controller Read Sector command. The Read Sector command attempts to verify the sector eight times before returning an error. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. If the error is an uncorrectable error or an error is reported by the Winchester disc drive controller, the command terminates. The ~WRITE FAULT and ~DRIVE READY inputs are checked throughout the command's execution.

Table 5-2 Command Description (Cont.)

Command	Definition
DIAGNOSE:	This command causes the controller to perform an onboard diagnostic and to report the result in the Error Register. An interrupt is generated upon completion of the command. The Diagnose command performs tests on the onboard micro- processor's internal ROM and RAM, host bus interface circuit, Winchester disc controller and the Sector buffer. If any component fails, the appropriate error code is loaded into the error register. Error code — Definition 00 — Not used, undefined 01 — No error 02 — Winchester disc controller CP/WD50C12 register error. 03 — Sector RAM buffer data error. 04 — Host bus manager 8753/AMAC error or AMAC byte 0 pipeline register error. 05 — Control processor ROM checksum or RAM data error. 06-FF — Not used, undefined The sector count register is reset to one while the cylinder high and cylinder low and SDH register are all set to zero.

Table 5-2 Command Description (Cont.)

Command	Definition
SET PARAMETERS:	This command sets up the drive parameters regarding the maximum number of heads and sectors per tracks. The hard disc controller uses these two parameters when performing multiple sector operations. The SDH task file register specifies the drive affected. The sector count and SDH registers must be set up before this command is issued. An interrupt is set at the completion of the command. This command must be issued before any multiple sector operations are undertaken. By setting the SDH register for each of the two possible drives, this command allows the controller to support two drives with different characteristics. If the parameters set with the SET PARAMETERS command are not identical to drive's physical parameters, the controller enters translation mode, where logical host sector addresses are translated into physical drive sector addresses. Translation is conceptualized as follows: Variables Used: LC: Logical Cylinder PC: Physical Cylinder LH: Logical Head PH: Physical Head LS: Logical Sector PS: Physical Sector Constants Used: SH: Set Parameters Heads/Cylinder SS: Set Parameters Sectors/Track DH: Actual Drive heads/cylinder DS: Actual Drive sectors/track Intermediate Variable: AS : Absolute Sector AS:= (LC * SH + LH) * SS + LS PC:= AS DIV (DH * DS) PH:= (AS - PC * DH * DS) DIV DS PS:= AS - PC * DH * DS - DH * DS This logical-to-physical translation enables drives whose physical parameters exceed BIOS limits to be supported if the capacity of the physical drive is greater than or equal to the capacity of the drive specified in the Drive Type. The logical parameters of number of drive heads and number of sectors per track defined in the drive type are those used in SET PARAMETERS.

Table 5-2 Command Description (Cont.)

Command	Definition
INITIATE ESDI:	This command privides a way for the system software to issue ESDI specific commands directly to the ESDI interface. The contents of the cylinder high and cylinder low are sent to the drive set in the SDH register (1F6/176). Cylinder high (1F5/175) is the high order byte of the command while Cylinder low (1F4/174) is the low order byte. When command complete is asserted by the drive, the return status/data from the drive is placed back into. the cylinder hi and low registers and an IRQ 14 is issued to inform the system that the results are available. See the ESDI specifications for valid commands. These are not intended for normal system useage.
READ DATA STACK:	This diagnostic command is intended for use in conjunction with the WRITE DATA STACK command to verify the system-bus-to-controller data path and control logic. This command allows the system software to transfer one sector worth of data from the controller to the host. If a READ DATA STACK command is issued immediately after a WRITE DATA STACK, the same data buffer is returned to the system. The controller will not issue an IRQ 14h; only DRQ is asserted to synchronize the data transfer. A fixed disk is not required for the execution of this command and if one is connected, no disk activity will take place.
WRITE DATA STACK:	This diagnostic command is intended for use in conjunction with the READ DATA STACK command to verify the system bus to controller data path and control logic. This command allows the system software to transfer one sector worth of data to the controller. The data is held by the controller in its internal cache memory and is available to be read back in a stack like manner where the last sector written is the first read. The controller will not generate an IRQ 14h, only DRQ will be asserted to synchronize the transfer of data. The controller will not alter the data in any way nor will it initiate any drive activity. A fixed disk drive is not needed for the execution of this command.
CACHE ENABLE/ DISABLE:	This command enables or disables the track buffer's cache option according to the state of the Cache Control Register. Upon power-up, the cache is enabled. When the Cache Control Register is set to 55h, caching is disabled. When CLR is set to AAh caching is enabled when command is issued.
READ DRIVE PARAMETERS:	This command returns 49 bytes of the ESDI mass storage subsystem configuration to the host. (See Table 5-3.) The configuration information covers both the controller and the drive specified in the SDH register. When configuration information is ready to send to the host, the controller issues IRQ 14h and sets DRQ. The returned information has the following format. Words 0 through 9 are the drive's actual responses to the referenced ESDI commands.

Table 5-3. ESDI Mass Storage Subsystem Configuration Bytes

Word	ESDI Command	Configuration Information
0	3000h	General configuration
	3100h	Number of fixed cylinders
1		
	3200h	Number of removable cylinders
2		
	3300h	Number of heads:
3		bits 15 - 8 = number of removable heads bits 7 - 0 = number of fixed heads
4	3400h	Minimum number of unformatted bytes/track
	3500h	Minimum number of unformatted bytes/sector (hard sectored drives only)
5		
	3600h	Number of sectors/track bit
6		bits 15 - 8 = reserved bits 7 - 0 = sectors/track
7	3700h	Minimum bytes in Inter Sector Gap (ISG) field, not including inter-sector speed tolerance bits 15 - 8 = ISG bytes after index/sector pulse to write splice bits 7 - 0 = bytes per ISG
8	3800h	Minimum bytes per Phase Lock Oscillator (PLO) sync field bits 15 - 8 = reserved bits 7 - 0 = bytes per PLO sync field required when read gate is asserted.
9	3900h	Number of words in vendor unique status bits 15 - 8 = reserved bits 7 - 0 = number of vendor unique status words

Table 5-3. ESDI Mass Storage Subsystem Configuration Bytes (Cont.)

Word	ESDI Command	Configuration Information
10-19		Board serial number. 20 ASCII characters. All "0" means that the board is unserialized. (Currently not used.)
20		Controller type: 0 : Unspecified 1 : Single ported, single sector buffer 2 : Dual ported, multisector buffer 3 : Dual ported, multisector buffer, cache
21		Number of 512 byte per sector pages of controller buffer
22		Number of ECC bytes transferred on long operations.
23-26		Controller firmware revision, 8 ASCII characters.
27-46		Controller model number, 40 ASCII characters.
47		Number of sectors transferred per read command interrupt.
48		Various controller flag bits: bit 0, double-word capability 0 = none 1 = capability bit 1, Fast command transfer 0 = disabled 1 = enabled bit 2, Caching Disabled 0 = enabled 1 = disabled

Hard Disc Register (Write only, 3F6h or 376h)

This register allows programmed hard disc subsystem reset and provides enable/disable control of the hard disc interrupt.

Bit	Data	Definition
0	-	Reserved
1	0	Enable interrupt (IRQ14).
	1	Interrupt disabled.
2	1	Reset subsystem.
3	-	Reserved
4	-	Reserved
5	-	Reserved
6	-	Reserved
7		Reserved.

Alternate Status Register (Read only, 3F6h or 376h)

The Alternate Status Register is an exact duplicate of the Status Register at location 1F7h (or 177h).

Digital Input Register (Read only, 3F7h or 377h)

The digital input register contains the current state of the hard disc drive select, head select and drive write gate signals. The bit definition is shown below.

Bit	Definition
0	Drive select 0
1	Drive select 1
2	Head select 0
3	Head select 1
4	Head select 2
5	Head select 3
6	Write Gate On
7	Reserved for the Flexible Disc Controller subsystem

Clock Sources

10 MHz

Disc Drive Interface

The hard disc subsystem interfaces to a maximum of two hard disc drives through one 34-pin daisy-chain control cable and two 20-pin radial data cables, in conformance with ESDI signal definitions. The control cable can connect two drives; for each drive a separate data cable is used. To terminate the control signals properly, the last drive on the daisy chain must have a 220/300 ohm termination resistor installed.

Figure 5-3 shows the Control Interface Cable, and Table 5-4 shows the pin assignments for the connectors. Signal descriptions follow in Table 5-5; the input or output of the signals are referenced to the hard disc controller subsystem.

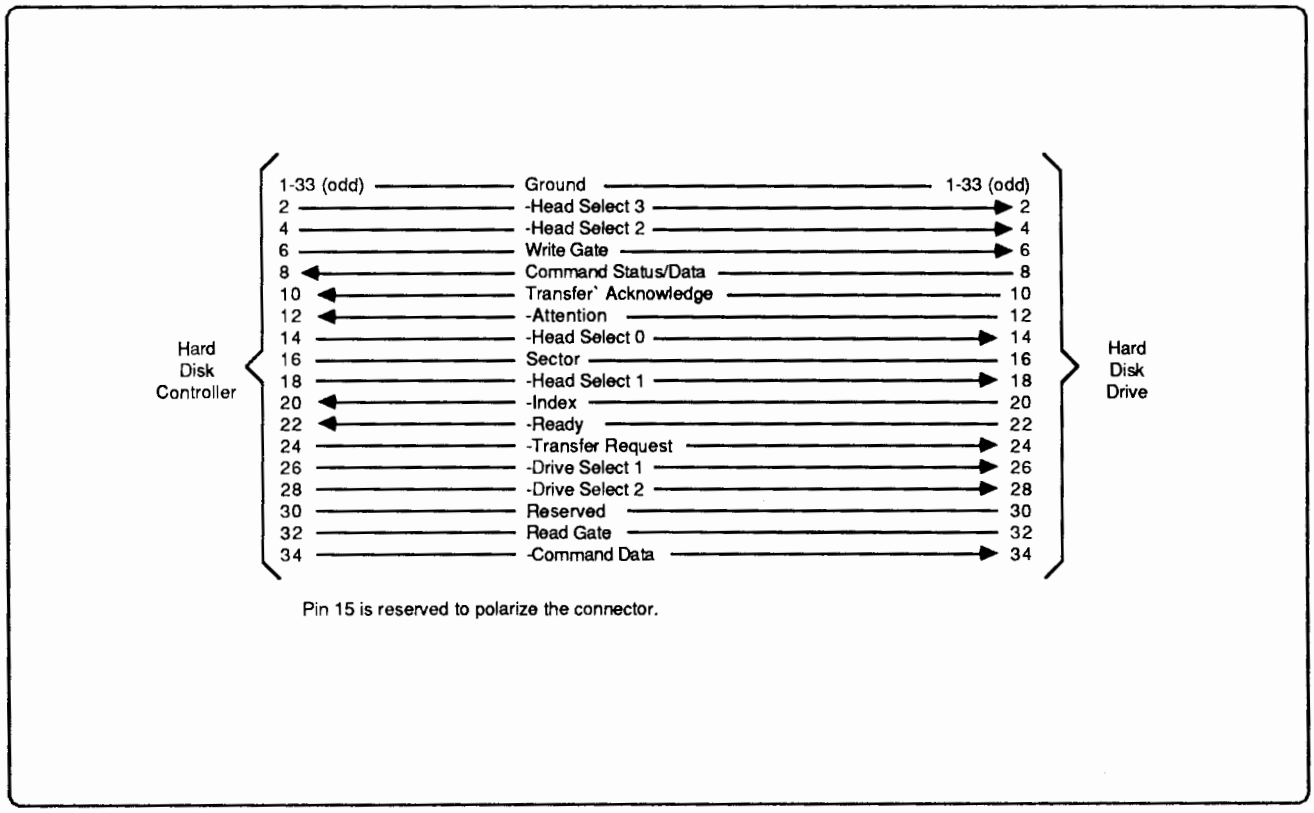


Figure 5-3. Control Interface Cable

Table 5-4. Control Cable Pin Assignments

Pin	I/O	Signal Name
2	O	~Head Select 3
4	O	~Head Select 2
6	O	~Write Gate
8	I	~Command Status/Data
10	I	~Transfer Acknowledge
12	I	~Attention
14	O	~Head Select 0
16	I	~Sector
18	O	~Head Select 1
20	I	~Index
22	I	~Ready
24	O	~Transfer Request
26	O	~Drive Select 1
28	O	~Drive Select 2
30	-	Reserved
32	O	~Read Gate
34	O	~Command Data
1-33	-	Odd pins are ground

Note: Pin 15 reserved to polarize the connector.

Table 5-5. Signal Descriptions

Signal	I/O	Signal Description
~ATTENTION	I	This signal informs the disc controller that some extraordinary event occured in the drive requiring attention or error recovery.
~COMMAND DATA	O	Serial commands sent by the controller.
~CSD	I	Status or data from commands sent from the controller to the drive over the COMMANMD DATA line.
~DS1 or ~DS2	O	Drive select lines 1 or 2 are used to select drive 1 and drive 2 respectively.
~HEAD SELECT3, ~HEAD SELECT2, ~HEAD SELECT1, ~HEAD SELECT0	O	These four signals are decoded to select one of up to sixteen read/write heads.
~INDEX	I	It indicates the start of a track. It pulses once at each disc revolution.
~READ GATE	O	Informs the drive that a series of 0's has been detected as in the case of a sync field.
~READY	I	It is asserted by the selected drive to inform the controller that the drive motor is up to speed.
~SECTOR	I	Asserted by the drive when an address mark is detected.
~TRANSFER ACK	I	Handshake signal for serial command transfer to and status reception from an ESDI drive.
~TRANSER REQ	O	Indicates that the controller wishes to transfer command/status information to/from the drive. This signal is used with TRANSFER ACK to handshake Command Serial Data.
~WRITE GATE	O	This signal is asserted when valid data is to be written on a disc. It is deasserted when ~Write Fault signal from the selected drive is detected.

Data Interface Pin Assignments and Description

The data lines between the hard disc controller and the two disc drives are connected to J2 and J3 at board upper edge. Both J2 and J3 have the same pin assignment and definition. The data lines are defined in Figure 5-4.

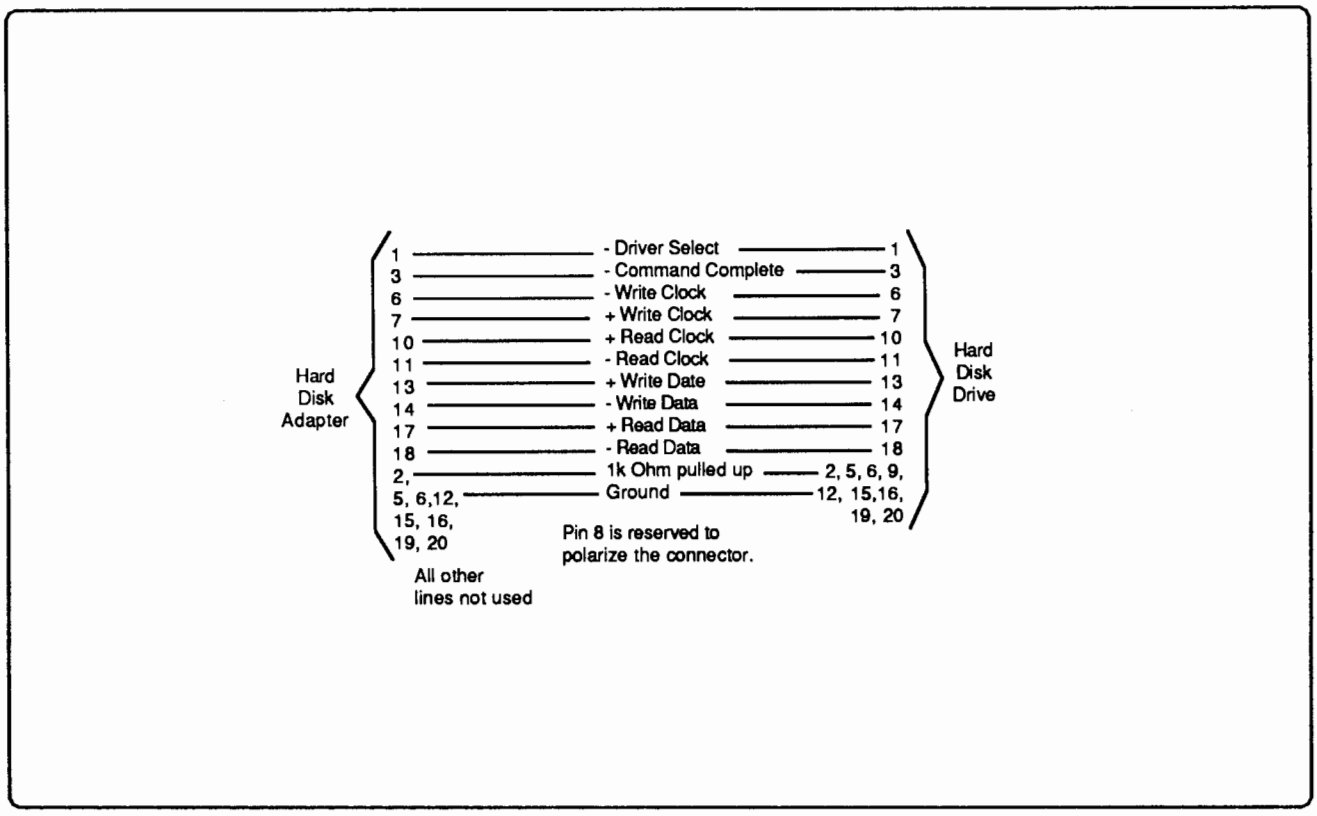


Figure 5-4. Data Interface Cable

Hard Disc Drive Activity LED Connector

The LED connector is a 4-pin header that connects with a reversible cable to the Vectra front panel. The hard disc controller lights the LED when the hard disc drive is busy or the host asserts RESET. The following shows the connector pin assignments and functions.

Pin	Signal Name
1, 4	+LED; connects to LED anode.
2, 3	-LED; connects to LED cathode.

Disc Drive Support

The card supports up to two ESDI hard disc drives. Drives supported include:

- HP 97961R 103-Mbyte Internal Hard Disc Drive
- HP 97962R 155-Mbyte Internal Hard Disc Drive
- HP 97963R 310-Mbyte Internal Hard Disc Drive

Recording Specifications

Data rate:	10.0 Mbit per Sec
Sector format:	512 bytes/sector
Interleave:	1:1
Drives supported:	2 maximum
Heads supported:	16 maximum
Cylinders supported:	2048 maximum
Hard error rate:	less than 1 per 10(E12) bits read
Soft error rate:	less than 1 per 10(E10) bits read
Seek error rate:	less than 1 per 10(E06) seeks

Error Correction Specifications

Method:	Polynomial division
Degree:	56
Forward polynomial:	X(E56)+X(E52)+X(E50)+X(E43)+X(E41)+ X(E34)+X(E30)+X(E26)+X(E24)+X(E8)+1
Reciprocal polynomial:	X(E56)+X(E48)+X(E32)+X(E30)+X(E26)+ X(E22)+X(E15)+X(E13)+X(E6)+X(E4)+1
Record length (r):	263X8 or 519X8 bits maximum
Correction span (b):	11 bits
Single burst detection:	r=519 X 8
Width b=0	56 bits
Width b=5	32 bits
Double burst detection span:	r=519X8
Width b=11	11 bits
Non-detection probability:	1.39(E-17), r=519X8, b=11
Miscorrection Probability:	5.84(E-11), r=519X8, b=11

Flexible Disc Controller Subsystem

The ESDI Four-Function Controller PCA's flexible disc controller subsystem is identical to that of the ST-506 Four-Function Controller PCA (which is identical to the Disc and Datacomm Controller Card). See the section "Disc and Datacomm Controller Card" for a discussion of the Flexible Disc Controller Subsystem.

Serial DataComm Interface Subsystem

The ESDI Four-Function Controller PCA's serial data communication subsystem is identical to that of the ST-506 Four-Function Controller PCA (which is identical to the Disc and Datacomm Controller Card). See the section "Disc and Datacomm Controller Card" for a discussion of the serial datacomm interface subsystem.

Parallel DataComm Interface Subsystem

The ESDI Four-Function Controller PCA's parallel data communication subsystem is identical to that of the ST-506 Four-Function Controller PCA (which is identical to the Disc and Datacomm Controller Card). See the section "Disc and Datacomm Controller Card" for a discussion of the parallel datacomm interface subsystem.

6

Dual RS232/422 Interface Card

The Hewlett-Packard Dual RS232/422 Interface card consists of two serial port interfaces on one card.

The Dual RS232/422 Interface Card provides asynchronous communications at RS-232C and RS-422 levels. Other features include: a programmable baud rate of 75 to 19200 bps, character length of 5, 6, 7, or 8 bits, a stop bit of 1, 1 1/2, or 2, a parity bit, modem control signals, full double buffering, and automatic adding or deletion of start, stop, and parity bits.

Jumper Configurations

The serial output port can be addressed as communications Port 1, 2, 3 or 4 by jumper block W1. These ports are mapped to different I/O address and have different interrupt level. Port 1 has I/O address 3F8H through 3FFH and interrupt level 4. Port 2 has the I/O address 2F8H through 2FFH and interrupt level 3. Port 3 has I/O address 3E8H through 3EFH and interrupt level 10. Port 4 has the I/O address 2E8H through 2EFH and interrupt level 11. The selection of ports/interrupts, as well as inhibiting the serial port, is performed by a jumper.

Serial Port Interface

Serial port A uses an RS-232C connector type DE 9-pin male. Table 6-1 defines the pin assignments and signal descriptions for this connector. Serial Port B uses an RS-232C connector type DB 25-pin male. Table 6-2 defines the pin assignments and signal descriptions for this connector.

Table 6-1. Serial Port Pin Assignments

Pin	I/O	Signal	Description
1	I	CF (CD)	When active, it indicates the device has detected the data carrier.
2	I	BB (RX)	Rx data
3	O	BA (TX)	Tx data
4	O	CD (DTR)	When active, it informs the device that the card is available to communicate.
5		AB (Gnd)	GND, ground
6	I	CC (DSR)	When active, it indicates the device is ready to establish the communications link in order to transfer data.
7	O	CA (RTS)	When active, it informs the device that the card is ready to transmit data.
8	I	CB (CTS)	When active, it indicates the device is available to receive data.
9	I	CE (RI)	When active, it indicates the device has a telephone ringing signal.

Table 6-2. Serial Port Pin Assignments

Pin	I/O	Signal	Description
8	I	CF (CD)	When active, it indicates the device has detected the data carrier.
3	I	BB (RX)	Rx data
2	O	BA (TX)	Tx data
20	O	CD (DTR)	When active, it informs the device that the card is available to communicate.
7		AB (Gnd)	GND, ground
6	I	CC (DSR)	When active, it indicates the device is ready to establish the communications link in order to transfer data.
4	O	CA (RTS)	When active, it informs the device that the card is ready to transmit data.
5	I	CB (CTS)	When active, it indicates the device is available to receive data.
22	I	CE (RI)	When active, it indicates the device has a telephone ringing signal.

Registers

The serial datacomm subsystem has 11 programmable registers. The system programmer may gain access or control any of the registers through the system CPU (microprocessor). Table 6-3 defines the registers and their addresses.

Table 6-3. Serial Datacomm Subsystem Registers

Register	R/W	Port 1 Port 2
Transmit Buffer	W	3F8H 2FH8*
Receive Buffer	R	3F8H 2F8H*
Divisor Latch LSB	R/W	3F8H 2F8H*
Divisor Latch MSB	R/W	3F9H 2F9H*
Interrupt Enable Register	R/W	3F9H 2F9H*
Interrupt ID Register		3FAH 2FAH
Line Control Register		3FBH 2FBH
Modem Control Register		3FCH 2FCH
Line Status Register		3FDH 2FDH
Modem Status Register		3FEH 2FEH
Reserved		3FFH 2FFH

* Access to these registers is determined by the state of the Line Control Register (3FBH or 2FBH).

Transmit Buffer Register (Write only, 3F8H or 2F8H)

This register contains the characters to be transmitted via the serial connector. Data bit 0, the least significant bit (LSB), is transmitted first and data bit 7, the most significant bit (MSB), is the last bit transmitted.

Receive Buffer Register (Read only, 3F8H or 2F8)

This register contains the characters received via the serial connector. Data bit 0, the least significant bit (LSB), is received first and data bit 7, the most significant bit (MSB), is the last bit received.

Bit 7 of the Line Control Register (3FBH or 2FBH) determines whether the Transmit Buffer Register or the Divisor Latch Register LSB is accessed and whether the Interrupt Enable Register or the Divisor Latch Register (MSB) is accessed.

Divisor Latch Registers LSB and MSB (3F8H or 2F8H, 3F9H or 2F9H)

The divisor latch LSB (3F8H or 2F8H) and the divisor latch MSB (3F9H or 2F9H) registers are used to control the baud-rate of the transmitted and received data.

This subsystem has a clock of 1.8432MHz. This frequency is divided by any divisor from 1 to 65,525 as set on the two divisor latches. The output frequency is 16 times the baud-rate.

The two divisor latches must be loaded to define the baud-rate before attempting to transmit or receive data. When either of the latches is loaded, a 16-bit baud-rate counter is immediately loaded to prevent long counts on the first load.

Table 6-4 gives examples of loading the divisor latch registers to determine the baud-rate.

Table 6-4. Divider Latch Values

Baud Rate	Divisor	MSB (XF9H) Bits	(XF8H) Bits LSB
		7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
75	1536	0 0 0 0 0 1 1 0	0 0 0 0 0 0 0 0
110	1047	0 0 0 0 0 1 0 0	0 0 0 1 0 1 1 1
300	384	0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0
600	192	0 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0
1200	96	0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0
2400	48	0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0
4800	24	0 0 0 0 0 0 0 0	0 0 0 1 1 0 0 0
9600	12	0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0
19200	6	0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 0

Interrupt Enable Register (Read/Write, 3F9H or 2F9H)

This register enables and disables the four types of interrupt from the serial datacomm subsystem.

Bit	Data	Interrupt
0	1	Enable the received data available interrupt.
	0	Disable interrupt.
1	1	Enable transmitter holding register empty interrupt.
	0	Disable interrupt.
2	1	Enable the receiver line status interrupt.
	0	Disable interrupt.
3	1	Enable the modem status interrupt.
	0	Disable interrupt.
4-7	0	Always.

When the enabled interrupt signal is received it activates the chip interrupt (INTRPT) output signal which is sent to the system. When all interrupts are disabled, the Interrupt Enable Register and the INTRPT output signal are disabled. The other registers are not affected.

Bit 7 of the Line Control Register (3FBH or 2FBH) determines whether the divisor latch MSB or the Interrupt Enable Register is accessed.

Interrupt Identification Register (3FAH or 2FAH)

This register identifies the highest priority pending interrupt signal. When this register is addressed it inhibits the highest priority interrupt. No other interrupts are acknowledged until this inhibited interrupt is cleared.

Bit	Data	Definition
0	0	Interrupt pending.
1-2		Identifies the pending interrupt with the highest priority as in the following: Bit 1 2 Interrupt 1 1 Receiver line status 1 0 Received data avail. 0 1 Trans. buffer empty 0 0 Modem status
3-7	0	Always.

The following defines the interrupt priorities.

Interrupt	Priority	Interrupt Source	Clear Interrupt
Receiver line status	1	Overrun error or parity error or framing error or break (200mS space on receive data line).	Reading the line status register.
Received data available	2	Data available in receive buffer.	Reading the receive buffer register.
Transmitter buffer register empty	3	Data transmitted from transmit buffer.	Reading the interrupt identification register (if source), or writing to the transmit buffer register.
Modem status	4	CB, CC, CE or CF signal received.	Reading the modem status register.

Line Control Register (3FBH or 2FBH)

This register controls the format of the data communications.

Bit	Data	Definition
0-1		Specifies the number of bits in each transmitted or received character as in the following: Bit Character Length in bits 0 1 1 1 8 1 0 7 0 1 6 0 0 5
2	0 1	One stop bit is generated or deleted in the data sent or received. 1 1/2 stop bit is generated or deleted for 5-bit words. For a 6, 7, or 8-bit word, 2 stop bits are generated or deleted.
3	0 1	Disable parity bit. A parity bit is generated (transmit data) or deleted (receive data).
4	0 1	When bit 3 is 1, parity bits sent or checked odd. When bit 3 is 1, parity bits sent or checked even.
5	1 0	When bit 3 is 1, the parity bit is set 0 for even parity and 1 for odd parity. Stuck parity disabled.
6	1 0	Break bit. The transmit data line is set to the space state (0) and remains at that state regardless of the state of the output buffer register. Set-breaking is disabled.
7	1 0	Address selection bit. Set to gain access of the divisor latches of the baud-rate generator during a read/write operation. Reset to gain access of the receiver buffer register, the transmit buffer register, or the interrupt enable register.

Modem Control Register (3FCH or 2FCH)

This register controls the modem signals. It also allows the serial DataComm subsystem to be set into diagnostic mode. In the diagnostic mode, transmitted data is received immediately. The receiver and transmitter interrupts and the modem control interrupts are fully operational, allowing the interrupts to be tested.

Bit	Data	Definition
0	1	Data terminal ready (CD) signal active.
	0	CD signal inactive.
1	1	Request to sent (CA) signal active.
	0	CA signal inactive.
2		Controls the OUT1~ signal from the controller chip. Can be 0 or 1.
3	1	Controls OUT2~ signal from the controller chip. Enables INTRPT generated by the interrupt enable register.
	0	The OUT2~ output is forced inactive.
4	1	Enables the modem loopback feature (diagnostic test) as follows: Transmitter serial input is disabled. Transmitter serial output is set to the active state. The output from the transmitter shift register is looped back to the receiver shift register. The four modem control inputs to the modem status register are disabled. The four modem control outputs from the modem control register are internally connected to the four modem control inputs
5-7	0	Always.

Line Status Register (3FDH or 2FDH)

This register provides information on the data transfer. Bits 1 through 4 are error conditions that generate a receiver line status interrupt. This register is not to be written to.

Bit	Data	Definition
0	1	Set when a complete incoming character has been received and transferred into the receiver buffer register.
	0	Reset by reading the data in the receiver buffer register or writing 0 in it.
1	1	Indicates that data in the receive buffer register was not read by the processor before the next character was transferred into the register, thereby erasing the previous character.
	0	Reset when the 80286 reads the Line Status Register.
2	1	Detection of a parity error.
	0	Reset when the 80286 reads the Line Status Register.
3	1	Framing error has occurred, character does not have a valid stop bit.
	0	Reset when the 80286 reads the Line Status Register.
4	1	The received data line was at a space state (0) for longer than a transmission time of a complete data character. (Including start, data, parity, and stop bits.)
	0	Reset when the 80286 reads the Line Status Register.
5	1	Set when a character is transferred from the transmit buffer register to the transmit shift register indicating the card is available to transmit another character.
	0	Reset when the next character is written into the transmit buffer register.
6	1	Transmit buffer register and transmit shift register are empty.
	0	Reset when either register contains a character.
7	0	Always.

Modem Status Register (3FEH or 2FEH)

This register provides information on the current state of the control lines from the modem or device.

Bit	Data	Definition
0	1	Set if clear to send signal (CB) input changes state.
	0	Reset when the Modem Status Register is read.
1	1	Set if data set ready (CC) input changes state.
	0	Reset when the Modem Status Register is read.
2	1	Set when the ring indicator (CE) input changes from low to a high state.
	0	Reset when the modem status register is read.
3	1	Set if the received line signal detector (CF) input changes state.
	0	Reset when the Modem Status Register is read.
4	1	Set when the CB input is active. However, if the modem loopback is enabled, this bit is equivalent to CA of XFCH (bit 1).
	0	Reset when the CB input is inactive.
5	1	Set when the CC input is active. However, if the modem loopback is enabled, this bit is equivalent to CD of XFCH (bit 0).
	0	Reset when the CC input is inactive.
6	1	Set when the CE input is active. However, if the modem loopback is enabled, this bit is equivalent to OUT1~ of XFCH (bit 2).
	0	Reset when the CE input is inactive.
7	1	Set when the CF input is active. However, if the modem loopback is enabled, this bit is equivalent to OUT2 of XFCH (bit 3).
	0	Reset when the CF input is inactive.

Clock Source

1.8432 MHz Crystal

7

Serial/Parallel I/O Card (24540A)

The Hewlett-Packard Serial/Parallel I/O card consists of two subsystems: a serial port interface and a parallel port interface. The layout of the card is shown in Figure 7-1.

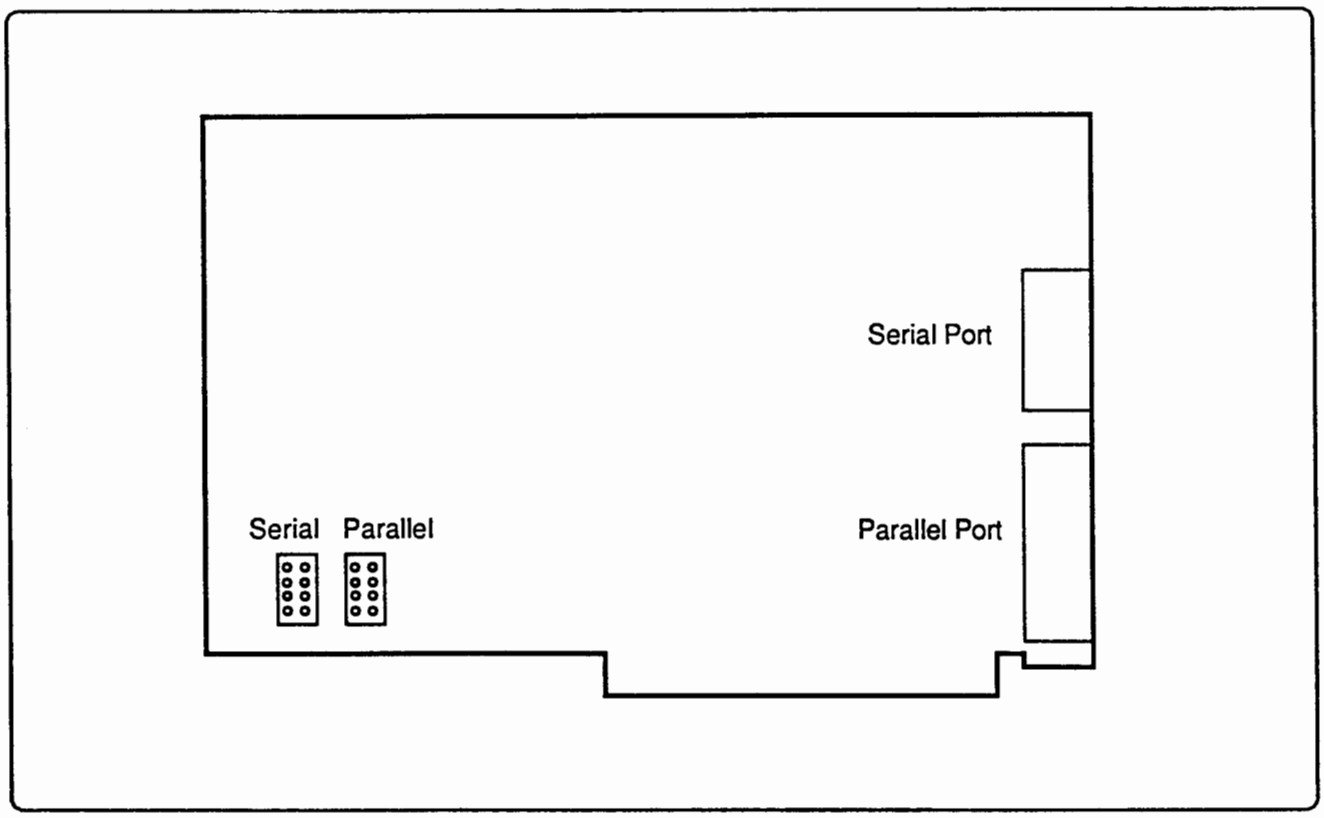


Figure 7-1. Serial/Parallel I/O Card.

Serial Interface

The serial interface provides asynchronous communications at RS-232C levels. Other features include: a programmable baud rate of 75 to 19200 bps, character length of 5, 6, 7, or 8 bits, a stop bit of 1, 1 1/2, or 2, a parity bit, modem control signals, full double buffering, and automatic adding or deletion of start, stop, and parity bits.

Jumper Configurations

The serial output port can be addressed as either communications Port 1 or communications Port 2 by jumper block J1. These two ports are mapped to different I/O address and have different interrupt level. Port 1 has I/O address 3F8H through 3FFH and interrupt level 4. Port 2 has the I/O address 2F8H through 2FFH and interrupt level 3. The selection of ports/interrupts, as well as inhibiting the serial port, is performed by a jumper. The location of the jumpers are shown in Figure 7-1. The jumpers are set according to Figure 7-2.

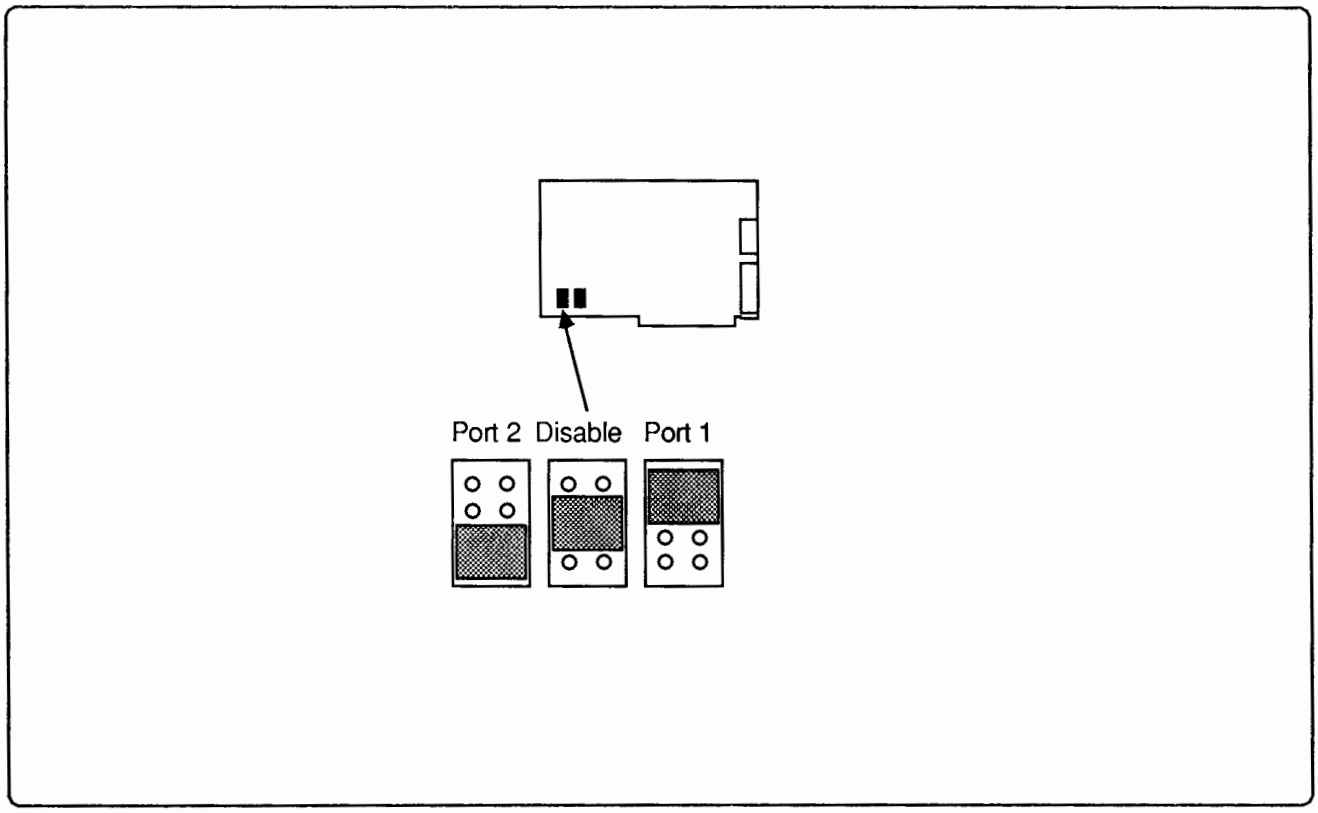


Figure 7-2. Serial Port Jumpers

Serial Port Interface

The serial port uses an RS-232C connector type DE 9-pin male. Table 7-1 defines the pin assignments and signal descriptions for this connector.

Table 7-1. Serial Port Pin Assignments

Pin	I/O	Signal	Description
1	I	CF (CD)	When active, it indicates the device has detected the data carrier.
2	I	BB (RX)	Rx data
3	O	BA (TX)	Tx data
4	O	CD (DTR)	When active, it informs the device that the card is available to communicate.
5		AB (Gnd)	GND, ground
6	I	CC (DSR)	When active, it indicates the device is ready to establish the communications link in order to transfer data.
7	O	CA (RTS)	When active, it informs the device that the card is ready to transmit data.
8	I	CB (CTS)	When active, it indicates the device is available to receive data.
9	I	CE (RI)	When active, it indicates the device has a telephone ringing signal.

Registers

The serial datacomm subsystem has 11 programmable registers. The system programmer may gain access or control any of the registers through the system CPU (microprocessor). Table 7-2 defines the registers and their addresses.

Table 7-2. Serial Datacomm Subsystem Registers

Register	R/W	Port 1	Port 2
Transmit Buffer	W	3F8H	2FH8*
Receive Buffer	R	3F8H	2F8H*
Divisor Latch LSB	R/W	3F8H	2F8H*
Divisor Latch MSB	R/W	3F9H	2F9H*
Interrupt Enable Register	R/W	3F9H	2F9H*
Interrupt ID Register		3FAH	2FAH
Line Control Register		3FBH	2FBH
Modem Control Register		3FCH	2FCH
Line Status Register		3FDH	2FDH
Modem Status Register		3FEH	2FEH
Reserved		3FFH	2FFH

* Access to these registers is determined by the state of the Line Control Register (3FBH or 2FBH).

Transmit Buffer Register (Write only, 3F8H or 2F8H)

This register contains the characters to be transmitted via the serial connector. Data bit 0, the least significant bit (LSB), is transmitted first and data bit 7, the most significant bit (MSB), is the last bit transmitted.

Receive Buffer Register (Read only, 3F8H or 2F8)

This register contains the characters received via the serial connector. Data bit 0, the least significant bit (LSB), is received first and data bit 7, the most significant bit (MSB), is the last bit received.

Bit 7 of the Line Control Register (3FBH or 2FBH) determines whether the Transmit Buffer Register or the Divisor Latch Register LSB is accessed and whether the Interrupt Enable Register or the Divisor Latch Register (MSB) is accessed.

Divisor Latch Registers LSB and MSB (3F8H or 2F8H, 3F9H or 2F9H)

The divisor latch LSB (3F8H or 2F8H) and the divisor latch MSB (3F9H or 2F9H) registers are used to control the baud-rate of the transmitted and received data.

This subsystem has a clock of 1.8432MHz. This frequency is divided by any divisor from 1 to 65,525 as set on the two divisor latches. The output frequency is 16 times the baud-rate.

The two divisor latches must be loaded to define the baud-rate before attempting to transmit or receive data. When either of the latches is loaded, a 16-bit baud-rate counter is immediately loaded to prevent long counts on the first load.

Table 7-3 gives examples of loading the divisor latch registers to determine the baud-rate.

Table 7-3. Divider Latch Values

Baud Rate	Divisor	MSB (XF9H) Bits								(XF8H) Bits LSB							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
75	1536	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
110	1047	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1
300	384	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
600	192	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
1200	96	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
2400	48	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
4800	24	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
9600	12	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
19200	6	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Interrupt Enable Register (Read/Write, 3F9H or 2F9H)

This register enables and disables the four types of interrupt from the serial datacomm subsystem.

Bit	Data	Interrupt
0	1	Enable the received data available interrupt.
	0	Disable interrupt.
1	1	Enable transmitter holding register empty interrupt.
	0	Disable interrupt.
2	1	Enable the receiver line status interrupt.
	0	Disable interrupt.
3	1	Enable the modem status interrupt.
	0	Disable interrupt.
4-7	0	Always.

When the enabled interrupt signal is received it activates the chip interrupt (INTRPT) output signal which is sent to the system. When all interrupts are disabled, the Interrupt Enable Register and the INTRPT output signal are disabled. The other registers are not affected.

Bit 7 of the Line Control Register (3FBH or 2FBH) determines whether the divisor latch MSB or the Interrupt Enable Register is accessed.

Interrupt Identification Register (3FAH or 2FAH)

This register identifies the highest priority pending interrupt signal. When this register is addressed it inhibits the highest priority interrupt. No other interrupts are acknowledged until this inhibited interrupt is cleared.

Bit	Data	Definition
0	0	Interrupt pending.
1-2		Identifies the pending interrupt with the highest priority as in the following: Bit 1 2 Interrupt 1 1 Receiver line status 1 0 Received data avail. 0 1 Trans. buffer empty 0 0 Modem status
3-7	0	Always.

The following defines the interrupt priorities.

Interrupt	Priority	Interrupt Source	Clear Interrupt
Receiver line status	1	Overrun error or parity error or framing error or break (200mS space on receive data line).	Reading the line status register.
Received data available	2	Data available in receive buffer.	Reading the receive buffer register.
Transmitter buffer register empty	3	Data transmitted from transmit buffer.	Reading the interrupt identification register (if source), or writing to the transmit buffer register.
Modem status	4	CB, CC, CE or CF signal received.	Reading the modem status register.

Line Control Register (3FBH or 2FBH)

This register controls the format of the data communications.

Bit	Data	Definition
0-1		Specifies the number of bits in each transmitted or received character as in the following: Bit Character Length in bits 0 1 1 1 8 1 0 7 0 1 6 0 0 5
2	0 1	One stop bit is generated or deleted in the data sent or received. 1 1/2 stop bit is generated or deleted for 5-bit words. For a 6, 7, or 8-bit word, 2 stop bits are generated or deleted.
3	0 1	Disable parity bit. A parity bit is generated (transmit data) or deleted (receive data).
4	0 1	When bit 3 is 1, parity bits sent or checked odd. When bit 3 is 1, parity bits sent or checked even.
5	1 0	When bit 3 is 1, the parity bit is set 0 for even parity and 1 for odd parity. Stuck parity disabled.
6	1 0	Break bit. The transmit data line is set to the space state (0) and remains at that state regardless of the state of the output buffer register. Set-breaking is disabled.
7	1 0	Address selection bit. Set to gain access of the divisor latches of the baud-rate generator during a read/write operation. Reset to gain access of the receiver buffer register, the transmit buffer register, or the interrupt enable register.

Modem Control Register (3FCH or 2FCH)

This register controls the modem signals. It also allows the serial DataComm subsystem to be set into diagnostic mode. In the diagnostic mode, transmitted data is received immediately. The receiver and transmitter interrupts and the modem control interrupts are fully operational, allowing the interrupts to be tested.

Bit	Data	Definition
0	1	Data terminal ready (CD) signal active.
	0	CD signal inactive.
1	1	Request to sent (CA) signal active.
	0	CA signal inactive.
2		Controls the OUT1~ signal from the controller chip. Can be 0 or 1.
3	1	Controls OUT2~ signal from the controller chip. Enables INTRPT generated by the interrupt enable register.
	0	The OUT2~ output is forced inactive.
4	1	Enables the modem loopback feature (diagnostic test) as follows: Transmitter serial input is disabled. Transmitter serial output is set to the active state. The output from the transmitter shift register is looped back to the receiver shift register. The four modem control inputs to the modem status register are disabled. The four modem control outputs from the modem control register are internally connected to the four modem control inputs
5-7	0	Always.

Line Status Register (3FDH or 2FDH)

This register provides information on the data transfer. Bits 1 through 4 are error conditions that generate a receiver line status interrupt. This register is not to be written to.

Bit	Data	Definition
0	1	Set when a complete incoming character has been received and transferred into the receiver buffer register.
	0	Reset by reading the data in the receiver buffer register or writing 0 in it.
1	1	Indicates that data in the receive buffer register was not read by the processor before the next character was transferred into the register, thereby erasing the previous character.
	0	Reset when the 80286 reads the Line Status Register.
2	1	Detection of a parity error.
	0	Reset when the 80286 reads the Line Status Register.
3	1	Framing error has occurred, character does not have a valid stop bit.
	0	Reset when the 80286 reads the Line Status Register.
4	1	The received data line was at a space state (0) for longer than a transmission time of a complete data character. (Including start, data, parity, and stop bits.)
	0	Reset when the 80286 reads the Line Status Register.
5	1	Set when a character is transferred from the transmit buffer register to the transmit shift register indicating the card is available to transmit another character.
	0	Reset when the next character is written into the transmit buffer register.
6	1	Transmit buffer register and transmit shift register are empty.
	0	Reset when either register contains a character.
7	0	Always.

Modem Status Register (3FEH or 2FEH)

This register provides information on the current state of the control lines from the modem or device.

Bit	Data	Definition
0	1	Set if clear to send signal (CB) input changes state.
	0	Reset when the Modem Status Register is read.
1	1	Set if data set ready (CC) input changes state.
	0	Reset when the Modem Status Register is read.
2	1	Set when the ring indicator (CE) input changes from low to a high state.
	0	Reset when the modem status register is read.
3	1	Set if the received line signal detector (CF) input changes state.
	0	Reset when the Modem Status Register is read.
4	1	Set when the CB input is active. However, if the modem loopback is enabled, this bit is equivalent to CA of XFCH (bit 1).
	0	Reset when the CB input is inactive.
5	1	Set when the CC input is active. However, if the modem loopback is enabled, this bit is equivalent to CD of XFCH (bit 0).
	0	Reset when the CC input is inactive.
6	1	Set when the CE input is active. However, if the modem loopback is enabled, this bit is equivalent to OUT1~ of XFCH (bit 2).
	0	Reset when the CE input is inactive.
7	1	Set when the CF input is active. However, if the modem loopback is enabled, this bit is equivalent to OUT2 of XFCH (bit 3).
	0	Reset when the CF input is inactive.

Clock Source

1.8432 MHz Crystal

Parallel Interface

The parallel interface provides a parallel port to attach devices that accept eight bits of parallel data at standard TTL levels. It includes programmable printer control such as automatic initialization, printer select, auto linefeed, and data strobe.

Jumper Configurations

The parallel output port can be addressed as either parallel Port 1 or 2 by jumper block J2. These two ports are mapped to different I/O addresses and have different interrupt levels. Port 1 is mapped to I/O address 378H through 37FH and interrupt level 7. Port 2 is mapped to I/O address 278H through 27FH and interrupt level 5. The selection of ports/interrupts, as well as inhibiting the serial port, is performed by a jumper. The location of the jumpers are shown in Figure 7-1. The jumpers are set according to Figure 7-3.

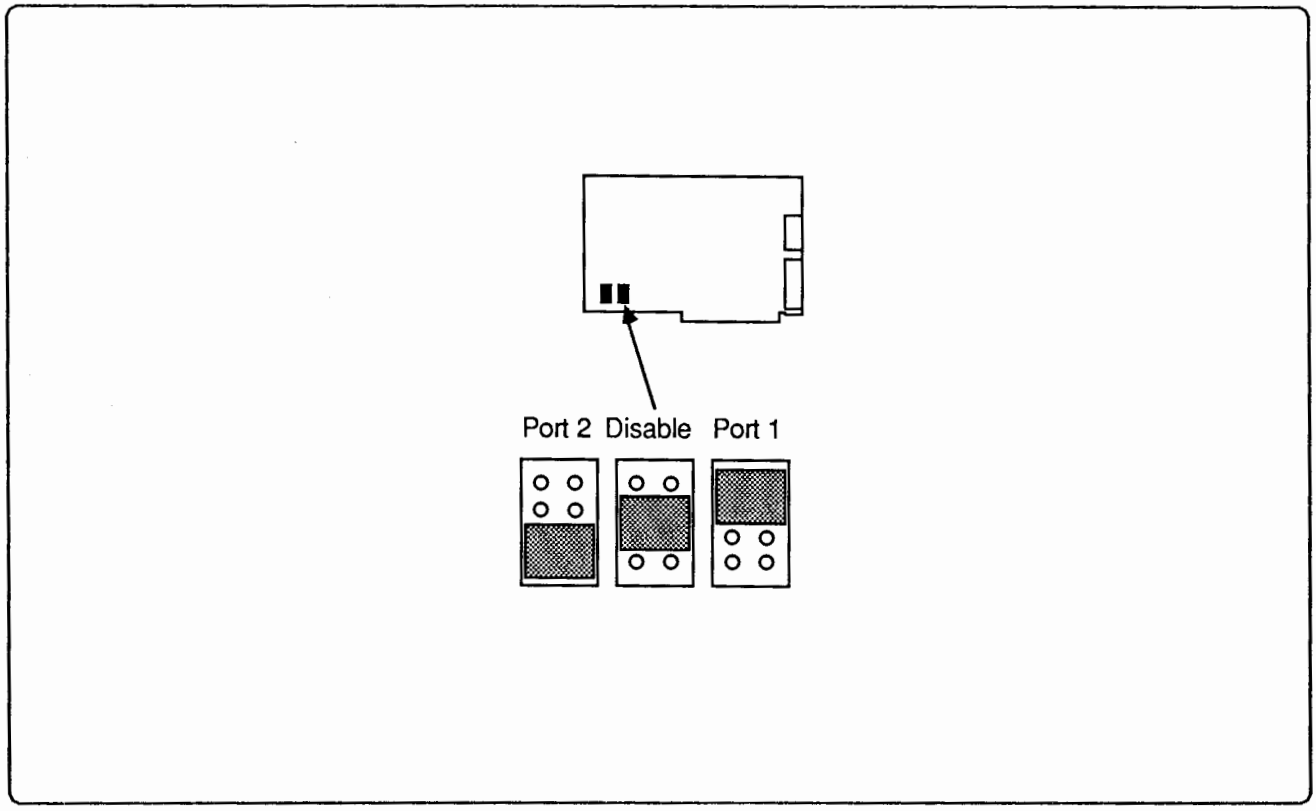


Figure 7-3. Parallel Port Jumpers

Parallel Port Interface to the System

The parallel port uses a DB-type 25-pin female connector. Table 7-4 defines the pin assignments and signal descriptions for this connector.

Table 7-4. Parallel Port Pin Assignments

Pin	I/O	Signal	Definition
1	O	STROBE~	Data strobe
2	O	D0	Data bit 0
3	O	D1	Data bit 1
4	O	D2	Data bit 2
5	O	D3	Data bit 3
6	O	D4	Data bit 4
7	O	D5	Data bit 5
8	O	D6	Data bit 6
9	O	D7	Data bit 7
10	I	ACK~	Printer has processed the received character.
11	I	BUSY	Printer is busy and will not accept more data.
12	I	PE	Printer detects end of paper.
13	I	SLCT IN~	Printer select.
14	O	AUTO FD~	Printer to perform a linefeed after a line is printed.
15	I	ERROR~	Printer has encountered an error.
16	O	INIT~	Initialize printer.
17	O	SLCT IN~	Set low to enable the printer to accept data.
18		GND	Ground
19		GND	Ground
20		GND	Ground
21		GND	Ground
22		GND	Ground
23		GND	Ground
24		GND	Ground
25		GND	Ground

Registers

The parallel subsystem has three programmable registers. The system programmer may gain access or control any of the registers in the parallel subsystem through the 80286. Table 7-5 defines the registers and their addresses.

Table 7-5. Accessible Registers

Address* Hex	Register
X78 or X7C	Data Buffer Register
X7A or X7E	Printer Control Register
X79 or X7D	Printer Status Register

The X is substituted with the appropriate port selection number, a 3 for port 1, a 2 for port 2.

Buffer Register (378H/37CH or 278/27CH)

This register contains the data character. Reading from this address causes the character to be read by the card. Writing to this address causes the character to be transmitted through the parallel connector.

Printer Control Register (37AH/37EH or 27AH/27EH)

This register controls the printer signals

Bit	Data	Definition
0	1	Generates an active low STROBE signal for a minimum of 500nS. The STROBE signal clocks the data from the parallel port into the printer. The valid data must be present a minimum of 0.5uS before and after the STROBE signal.
	0	STROBE inactive.
1	1	Generates the low AUTO FD signal.
	0	AUTO FD inactive.
2	0	Generates the low INIT~ signal for a minimum of 50uS.
	1	INIT~ inactive.
3	1	Generates the low SLCT IN~ signal.
	0	SLCT IN inactive.
4	1	Enables the IRQ when the ACK~ input signal changes from true to false.
	0	Disable IRQ.
5-7	0	Always.

Printer Status Register (379H/37DH or 279H/27DH)

This register provides information on the control lines from the printer.

Bit	Data	Definition
0-2	0	Always.
3	0	The ERROR~ input is active.
4	1	The SLCT input is active.
5	1	The PE input is active.
6	0	The ACK~ input is active.
7	0	The BUSY input is active.

8

Multimode Video Adapter Card

The HP45981A Multimode Video Adapter Card has available memory to support eight pages of alpha and fast memory with full access interleaving. There is no need to wait for retrace to access memory for a clean display. An 8 x 16 dot alpha character cell is supported for improved alpha.

Other features include:

- Underline enhancement support
- Hardware that will support gray-scale for monochrome monitors
- Selectable HP or industry standard character sets
- Support for both 15kHz (200 line) and 25kHz (400 line) monitors, but not simultaneously.

Clock Cycle

The HP45981A operates from the master oscillator at 22.440MHz and the backplane clock at 14.3818MHz.

Adapter to System Hardware Interface

The HP45981A is interfaced to the 80286 microprocessor as an 8-bit memory device and and 8-bit I/O device. All signal lines are buffered onto the card and load to the system bus. Wait states are provided for memory accesses to synchronize the 80286. The RAM on the card is on four 16 Kbyte x 4 RAM chips.

Jumpers and Connectors

Jumper W2 must be installed on pins 1 and 2 of P4 for operation with a 15 kHz monitor. Jumper W2 must be installed on pins 2 and 3 of P4 for operation with a 25 kHz monitor.

Tables 8-1 and 8-2 define the pin assignments and signal definitions for the Light Pen Connector and Direct Connect (RGB) Monitor Connector. Table 8-3 defines the pin assignments and signal definitions for the Color Adapter Connector.

Table 8-1. Light Pen Connector (P5) Pin Assignments

Pin	Signal	I/O	Signal
P2-1	~LPHIT	I	Light Pen Hit (TTL level)
P2-2		n.c.	Missing pin (key)
P2-3	~LPSWITCH	I	Light Pen Switch (TTL level)
P2-4	GND		Ground
P2-5	+5 Vdc	O	+5 Volts DC power
P2-6	+12Vdc	O	+12 Volts DC power

Table 8-2. Direct Connect Monitor Connector (J1) Pin Assignments

Pin	Signal	I/O	Signal
J1-1	GND		Ground
J1-2	GND		Ground
J1-3	RED	O	Red Drive (TTL level)
J1-4	GREEN	O	Green Drive (TTL level)
J1-5	BLUE	O	Blue Drive (TTL level)
J1-6	INTENSIFY	O	Intensify (TTL level)
J1-7	n.c.		
J1-8	HSYNC	O	Synchronization (TTL level)
J1-9	VSYNC	O	Vertical Synchronization (TTL level)

Table 8-3. Color Adapter Connector (P3) Pin Assignments

Pin	Signal	I/O	Signal
1	GND		Ground
2	INTENSITY	O	Intensity dot stream
3	RED	O	Red dot stream
4	GND		Ground
5	GREEN	O	Green dot stream
6	BLUE	O	Blue dot stream
7	GND		Ground
8	COMPSYNC	O	Composite sync
9	HSYNC	O	Horizontal sync
10	GND		Ground
11	VSYNC	O	Vertical sync
12	MCLK	O	Dot rate clock
13	GND		Ground
14	-PRESENT	I	Board present

Character Generator ROM

The character generator ROM for the HP45981A is an 128 Kbyte bit ROM (16 Kbyte x 8) containing four character sets. Each set consists of 256 patterns. Depending on the monitor in use either an 8 or 16 high cell is selected. The font bit (bit 2) of the extension control register and the monitor determines the character set that is selected. A 15kHz monitor selects the eight row version, while a 25kHz monitor selects the 16 row version.

Each character set is stored in contiguous 4 Kbytes in the ROM defined by the following chart.

Set	Font	Size	Location
0	STD	8x8	0000-0FFF
1	STD	16x8	1000-1FFF
2	HP	8x8	2000-2FFF
3	HP	14x8	3000-3FFF

Within each set the top row of each character is the first 256 bytes, the second row in the next 256, etc. Within each byte the high order bit 7 is displayed on the left side of the character. A 1 is stored for a lit dot, a 0 for an unlit dot.

The complete address definition of the ROM is:

A13	A12	A11,10,9,8	A7,6,5,4,3,2,1,0
Font 0=STD 1=HP	Height 0=8x8 1=14x8	Row #	Character Code Row 0 is the top of the cell.

RAM Access

The HP45981A contains 32K of RAM based in a contiguous segment B8000-BFFFF. The memory on the video card is run asynchronously to the 80286. Therefore, any access to the video memory will include at least four wait-states, and as many as six, to complete an instruction. Refresh is generated internally. Data is taken from memory depending on the mode of operation. The two modes of operation are alpha mode and graphics mode.

Memory address wrapping and page selection is controlled by four bits in the extension control register. The 16/32K (bit 4) select and the page select (bit 5) determine the way the SPU has access to memory. The vertical resolution (bit 0) and the font select (bit 2) determine the way the display accesses the memory. The access to memory differs in the alpha and graphics modes. The various access methods are summarized in Table 8-4.

Table 8-4. SPU Access and Display Access

Access		Data	Description
SPU Access			
Alpha	16/32K Select	0	First 16K of memory available. Wraps into the entire 32K address space.
	Page Select		Not used.
	16/32K Select	1	One 16K page of memory available. Wraps into entire 32K address space.
	Page Select		Not used.
Graphics	16/32K Select	0	First 16K of memory available. Wraps into the entire 32K address space.
	Page Select	0/1	Selects which page is active.
	16/32K Select	1	Entire 32K of memory available.
	Page Select		Not used.
Display Access			
Alpha	Vertical Resolution	0	Display first 16K of memory. Wraps into the entire 32K address space.
	Font Select	0/1	Selects character set displayed.
	Vertical Resolution	1	Display from entire 32K of memory. 400 line display.
	Font Select		Not used.
Graphics	Vertical Resolution	0	Display from one 16K page of memory. Wraps into entire 32K address space.
	Font Select	0/1	Selects which page is displayed.
	Vertical Resolution	1	Display from entire 32K of memory. 400 line display.
	Font Select		Not used.

Modes of Operation

The mode control register determines the mode of operation. The following is a list of available RAM access modes.

```
Alphanumeric Mode
   80 x 25
   40 x 25
Graphics Mode
   640 x 1
   320 x 2
```

Alphanumeric Mode

When the HP45981A is set in the alphanumeric mode, words (attribute byte + character byte) are fetched from the memory starting at the offset programmed into the 6845 CRT controller. This address is a word pointer and will always be used to fetch from even byte boundaries. Words are fetched contiguously from memory. For an 80 x 25 display, 2000 words (8 pages) are fetched. For a 40 x 25 display, 1000 words (16 pages) are fetched.

The character code is a byte with the ASCII code for the character. The attribute byte is defined as:

```
D7 D6 D5 D4 D3 D2 D1 D0
:  :  :  :  :  :  :  :
:  ---:---  :  ---:---
:     :     :     Foreground color (R-G-B)
:     :     Foreground Intensity
:     Background color (R-G-B)
Background intensity/Blink
```

If underline enable is set, an underline will be generated for any character with a foreground color of 001, and the color of the character will be forced to 111. If underline enable is not set the character will be displayed as blue or a gray level.

Graphics Mode

In the 200 line graphic modes the memory is mapped with even and odd lines of data in separate banks. Even lines start at offset 0000H and odd lines at offset 2000H. Sufficient memory exists for two pages of graphics to be stored. The second page stores the even lines at offset 4000H and the odd lines at offset 6000H. In this mode 25kHz monitors are supported by displaying each of the 200 lines twice.

In the 400 line graphics mode the memory is mapped into four banks. Lines 0,4,8,... are in the first bank at offset 0000H. Lines 1,5.9,... are in the second bank at offset 2000H. The third bank at offset 4000H contains lines 2,6,10,... while the fourth bank at offset 6000H contain lines 3,7,11,etc..

Data Format for Graphic Mode

In the data format mode the 320 x 2 mode maps two bits to each pixel. Each byte is displayed with the most significant bits to the left. This is shown in the following chart:

D7	D6	D5	D4	D3	D2	D1	D0
:	:	:	:	:	:	:	:
C1	C0	C1	C0	C1	C0	C1	C0

C1 and C0 select the color as defined by the color register.

640 x 1

The data for the 640 x 1 mode is mapped one bit per pixel with the most significant bit displayed to the left.

6845 CRT Controller

The 6845 CRT controller (CRTC) contains 19 internal registers. One of these is the index register. It is accessed at any even I/O address in the range 3D0-3D6. This write-only register functions as a pointer to the other 18 registers in the chip. Reading it will return an undefined value. The 18 internal data registers are accessible at any odd I/O address in the range 3D1 3D7, after first setting the index to point to it. Table 8-5 defines the initial values that should be sent to the CRTC chip.

Table 8-5. Initial 6845 Register Values

Mode		6845 Data Register													
25 KHz	Hz	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	3D8	3DD
80 x 25	60	6D	50	57	0A	19	09	19	19	00	0F	0E	0F	0D	00
80 x 25	60	36	28	2C	0A	19	09	19	19	00	0F	0E	0F	0C	00
80 x 27	60	6D	50	57	0A	1D	05	1B	1C	00	0D	0D	0E	0D	00
80 x 27	60	36	28	2C	0A	1D	05	1B	1C	00	0D	0D	0E	0C	00
320 x 2 x 200	60	36	28	2B	0A	69	01	64	66	00	03	0E	0F	0E	00
640 x 1 x 200	60	36	28	2B	0A	69	01	64	66	00	03	0E	0F	1E	00
320 x 2 x 400	60	36	28	2C	0A	69	01	64	66	00	03	0E	0F	0E	11
640 x 1 x 400	60	36	28	2C	0A	69	01	64	66	00	03	0E	0F	1E	11
80 x 25	50	6D	50	57	0A	1E	0E	19	1C	00	0F	0E	0F	0D	00
40 x 25	50	36	28	2C	0A	1E	0E	19	1C	00	0F	0E	0F	0C	00
80 x 27	50	6D	50	57	0A	23	06	1B	1F	00	0D	0C	0D	0D	00
40 x 27	50	36	28	2C	0A	23	06	1B	1F	00	0D	0C	0D	0C	00
320 x 2 x 200	50	36	28	2B	0A	7E	02	64	70	00	03	0E	0F	0E	00
640 x 1 x 200	50	36	28	2B	0A	7E	02	64	70	00	03	0E	0F	1E	00
320 x 2 x 400	50	36	28	2C	0A	7E	02	64	70	00	03	0E	0F	0E	11
640 x 1 x 400	50	36	28	2C	0A	7E	02	64	70	00	03	0E	0F	1E	11
15 KHz															
80 x 25	60	71	50	5A	0A	1F	06	19	1C	02	07	06	07	0D	00
40 x 25	60	38	28	2D	0A	1F	06	19	1C	02	07	06	07	0C	00
320 x 2 x 200	60	38	28	2D	0A	7F	06	64	70	02	01	06	07	0E	00
640 x 1 x 200	60	38	28	2D	0A	7F	06	64	70	02	01	06	07	1E	00
80 x 25	50	71	50	5A	0A	26	02	19	1F	02	07	06	07	0D	00
40 x 25	50	38	28	2D	0A	26	02	19	1F	02	07	06	07	0C	00
320 x 2 x 200	55	38	28	2D	0A	7F	1F	64	75	02	01	06	07	0E	00
640 x 1 x 200	55	38	28	2D	0A	7F	1F	64	75	02	01	06	07	1E	00

Translation

Data written to the CRTC passes through a translation circuit to allow applications written for a 15kHz monitor to operate without modification when a 25kHz monitor is connected. In this way the actual monitor connected is transparent to the program. The low four bits of any data written to the address index register is also latched external to the CRTC in a phase alternation line (PAL). When a subsequent write is performed to the data register of the CRTC, the latched data and the actual data written are combined and used as an address into the translation ROM. It is the data contained in the ROM that is written into the CRTC.

The translation will occur for any register needing it if the data written to the register is in the range 00H to 7FH. If an application needs to set a register to a specific value without translation, bit 7 must be set to 1. Data in the range 80 to FF will then be written to the chip as 00H to 7FH. The translation occurs only on the data written to the CRTC and only when a 25kHz monitor is connected. Data is read back directly from the chip. Translation will also occur for any monitor if the 50Hz jumper is installed. Again, values greater than 80H will be passed with bit 7 set to 0.

Programming Model

The application must read the status register bit 4 to determine which monitor is connected. No harm will be done setting the 400 line mode bit with a 200 line monitor connected, but the display will not be as expected.

At power-on or reset all bits are cleared in I/O registers except the light pen latch. Table 8-6 lists the I/O registers.

Table 8-6. I/O Registers

Register I/O Adr.	Read	Write
3D0	CRTC undefined	CRTC Register Index
3D1	CRTC Data Register	CRTC Data Register
3D2	CRTC undefined	Duplicate CRTC Register Index
3D3	CRTC Data Register	Duplicate CRTC Data Register
3D4	CRTC undefined	Duplicate CRTC Register Index
3D5	CRTC Data Register	Duplicate CRTC Data Register
3D6	CRTC undefined	Duplicate CRTC Register Index
3D7	CRTC Data Register	Duplicate CRTC Data Register
3D8	Undefined*	Mode Control Register
3D9	Undefined*	Color Select Register
3DA	Status Register	Not allowed***
3DB	Clear LP Flag**	Clear LP Flag**
3DC	Set LP Flag**	Set LP Flag**
3DD	Undefined*	Extended Control Register
3DE	Undefined*	Unused
3DF	Board ID*	Unused

* Reading an undefined register will cause its contents to become undefined.
** Reading or writing will cause function. No data is written and value returned via read is meaningless.
*** Do not write to this register.

Mode Control Register

The mode control register is a 6-bit write-only register.

Bit	Data	Definition
0	0	40 character alpha, 320x2 graphics, 640x1 graphics
	1	80 character alpha, 640x2 graphics
1	0	Alpha mode
	1	Graphics mode
2*	0	Color mode
	1	Black and white mode
3	0	Disable video
	1	Enable video
4	0	Select 320 pixel graphics
	1	Select 640 pixel graphics
5	0	Attribute bit 7 is background intensity
	1	Attribute bit 7 is blink

* Bit 2 provides a secondary function tying the blue and green guns together changing the displayed colors.

Color Register

The color register is a 6-bit write only register.

Bit	Data	Definition
0	0	Off, blue
	1	On, blue
1	0	Off, green
	1	On, green
2	0	Off, red
	1	On, red
3	0	Off, intensify
	1	On, intensify
4	0	Alternate set select
	1	Pallet select

The use of bits 0, 1, 2, and 3 depends on the mode of operation selected. This is defined as follows:

Alphanumeric:	selects the screen border color.*
320x2 graphics:	selects the screen background color.
640x1 graphics:	selects the foreground color, background black.

*Not implemented for 25kHz monitor.

Bit 4, when set to 1, intensifies the 320 x 2 colors to their alternates. Bit 5 determines the pallet of colors used in the 320 x 2 mode. This is defined as:

Pixel C1/C0	Bit 5 = 0 Normal/Alternate	Bit 5 = 1 Normal/Alternate
0 0	Background determined by bits 0-3.	
0 1	Green/Lt. Green	Cyan/Lt. Cyan
1 0	Red/Lt. Red	Magenta/Lt. Magenta
1 1	Brown/Yellow	White/Bright White

Status Register

The status register is an 8-bit read-only register.

Bit	Data	Definition
0	0	Display Enable, retrace
	1	Active area
1	0	Light pen hit, register reset
	1	Register set
2	0	Light Pen Switch, open
	1	Closed
3	0	Vertical Sync,
	1	within vertical sync time
4	0	Monitor type, 25kHz
	1	Monitor type, 15kHz
5	0	Color adapter connected
	1	Color adapter not connected
6		Diagnostic purposes
7		Diagnostic purposes

Light Pen

Any access to I/O address 3DB, read or write, will clear the light pen latch. No data is transferred, if a read is performed the data returned is meaningless.

Any access to I/O address 3DC, read or write, will set the light pen latch. No data is transferred, if a read is performed, the data returned is meaningless.

Extension Control Register

The extension control register is a 6-bit write-only register.

The programmer has control over the font style, but not the height. The type of monitor determines the cell size of the alphanumeric character font.

Bit	Data	Definition
0	0	Vertical Resolution, emulate 200 line display
	1	Enable 400 line display
1	0	Underline Enable, normal
	1	Enable underline if bits 2-0 are 001.
2	0	Font Select, STD on Display Graphics page 1
	1	HP, Roman 8 font on Display Graphics page 2
3	0	Memory Disable, normal
	1	Disable memory from responding to R/W access.
4	0	16/32K select, wrap first 16K into 32K
	1	Use all 32K
5	0	Page, use first 16K
	1	Use second 16K (graphics)

The underline enable bit must be set for underlines to be displayed. If it is not set an underlined character will be displayed as blue or a shade of gray.

Board ID Register

The board ID register is a read-only register. It will return the value 41H when read.

9

Accessory Cables

This chapter provides wiring diagrams for HP peripheral interface cables. In each case the layout of the information is as follows:

CARD SIDE CONNECTOR	SIGNAL	DEVICE SIDE CONNECTOR

PIN#	TITLE	DESCRIPTION	PIN#
1	CF	Data carrier detect	4
2	BB	Receive data	2
3	BA	Transmit Data	3
4	CD	Data Terminal Ready	5----\
			6----/
5	AB	Ground 0 Volts	7
6---\	CC	Data Set Ready	20
7 |	CA	Request To Send	8
8---/	CB	Clear To Send	
9	AA	Cable Shield	1

HP 24542G and HP 24542H Serial Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	CF	Data Carrier Detect	8
2	BB	Receive Data	3
3	BA	Transmit Data	2
4	CD	Data Terminal Ready	20
5	AB	Ground (0 Volts)	7
6	CC	Data Set Ready	6
7	CA	Request To Send	4
8	CB	Clear To Send	5
9	CE	Ring Indicator	22
	AA	Cable Shield	1

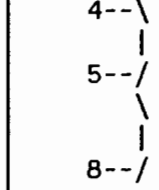
HP 24542M US/European Modem Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	2
3	BB	Receive Data	3
	RD.A	RS-424 Receive Data A	
4	CA	Request to Send	4
5	CB	Clear to Send	5
6	CC	Data Set Ready	6
7	AB	Signal Ground	7
8	CF	Carrier Detect	8
14	SBA	Secondary Transmit Data*	14
15	DB	Transmit Signal Element Timing (DEC Source)*	15
20	CD	Data Terminal Ready	20
23	CH	Data Signal Rate Select (DTE Source)	23
	CI	Data Signal Rate (DTE Source)	
24	DA	Transmit Signal Element Timing (DTE Source)*	24

* These signals are not provided on the Dual RS-232/422 card 25-pin connector.

HP 40242C RS-232 Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
3	RD.A	RS-422 Receive Data A	3
7	AB	Signal Ground	1
9	SD.A	RS-422 Transmit Data A	2
10	SD.B	RS-422 Transmit Data B	4
18	RD.B	RS-422 Receive Data B	5



HP 40242P or 13242P Direct Connect 422 Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
2	BA	Transmit Data	2
3	BB	Receive Data	3
7	AB	Signal Ground	1

HP 40242X or 13242X Direct Connect 232 Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	2
3	BB	Receive Data	3
7	AB	Signal Ground	7

HP 40242Y EMP Protect Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	2
3	BB	Receive Data	3
4	CA	Request to Send	4
5	CB	Clear to Send	5
6	CC	Data Set Ready	6
7	AB	Signal Ground	7
8	CF	Carrier Detect	8
14	SBA	Secondary Transmit Data*	14
15	DB	Transmit Signal Element Timing (DEC Source)*	15
20	CD	Data Terminal Ready	20
23	CH	Data Signal Rate Select (DTE Source)	23
	CI	Data Signal Rate (DTE Source)	
24	DA	Transmit Signal Element Timing (DTE Source)*	24

* These signals are not provided on the Dual RS-232/422 card 25-pin connector.

HP 40242M US/European Modem Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	2
3	BB	Receive Data	3
4	CA	Request to Send	4
	CB	Clear to Send	
5			
6	CC	Data Set Ready	20
7	AB	Signal Ground	7
8	CF	Carrier Detect	4--\
			|
			5--/
20	CD	Data Terminal Ready	6

HP 40242Z Modem Bypass Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	3
3	BB	Receive Data	2
4	CA	Request to Send	8
5--\	CB	Clear to Send	20
|			
6--/	CC	Data Set Ready	
7	AB	Signal Ground	7
8	CF	Carrier Detect	4
12	SCF	Secondary Carrier Detect*	19--\
			|
11--\	SCA	Secondary Request to Send	11--/
|			
19--/	SCA	Secondary Request to Send*	12
20	CD	Data Terminal Ready	5--\
			|
			6--/

* These signals are not provided on the Dual RS-232/422 card 25-pin connector.

HP 40242G (or 13242G) RS-232 Printer Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	3
3	BB	Receive Data	2
7	AB	Signal Ground	7
/--5	CF	Carrier Detect	20
|			
\--6			
20	CD	Data Terminal Ready	5--\
			|
			6--/

HP 17255D Modem Eliminator Type Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	2
3	BB	Receive Data	3
	RD.A	RS-424 Receive Data A	
4	CA	Request to Send	4
5	CB	Clear to Send	5
6	CC	Data Set Ready	6
7	AB	Signal Ground	7
8	CF	Carrier Detect	8
11	SCA	Secondary Request to Send*	19
12	SCF	Secondary Carrier Detect	12
15	DB	Transmit Signal Element Timing (DEC Source)*	15
17	DD	Receive Signal Element Timing*	17
19	SCA	Secondary Request to Send*	11
20	CD	Data Terminal Ready	20
22	CE	Ring Indicator	22
23	CH	Data Signal Rate Select (DTE Source)	23
	CI	Data Signal Rate (DTE Source)	
24	DA	Transmit Signal Element Timing (DTE Source)*	24

* These signals are not provided on the Dual RS-232/422 card 25-pin connector.

HP 13242N US Modem Cable Pinouts

PIN#	TITLE	DESCRIPTION	PIN#
1	AA	Shield	1
2	BA	Transmit Data	2
3	BB	Receive Data	3
	RD.A	RS-424 Receive Data A	
4	CA	Request to Send	4
5	CB	Clear to Send	5
6	CC	Data Set Ready	6
7	AB	Signal Ground	7
8	CF	Carrier Detect	8
12	SCF	Secondary Carrier Detect	12
15	DB	Transmit Signal Element Timing (DEC Source)*	15
17	DD	Receive Signal Element Timing*	17
19	SCA	Secondary Request to Send*	11
20	CD	Data Terminal Ready	20
22	CE	Ring Indicator	22
23	CH	Data Signal Rate Select (DTE Source)	23
	CI	Data Signal Rate (DTE Source)	
24	DA	Transmit Signal Element Timing (DTE Source)*	24

* These signals are not provided on the Dual RS-232/422 card 25-pin connector.

HP 13242M Europe Modem Cable Pinouts

PIN#	DESCRIPTION	PIN#
1	STROBE	1
2	DATA BIT 0	2
3	DATA BIT 1	3
4	DATA BIT 2	4
5	DATA BIT 3	5
6	DATA BIT 4	6
7	DATA BIT 5	7
8	DATA BIT 6	8
9	DATA BIT 7	9
10	ACK	10
11	BUSY	11
12	PE	12
13	SLCT	13
14	AUTO FD	14
15	ERROR	32
16	INIT	31
17	SLCT IN	36
18 TO 25	GROUND, 0 VOLTS	19 TO 30

HP 24542D Parallel Printer Cable Pinouts

HEWLETT PACKARD

Printed in USA 06/88
Part Number 5959-6759