PRINCIPLES OF OPERATION

DPC 1200 SERIES

CHAINTRAIN™ LINE PRINTERS

Models CT-1260, CT-1290, and CT-1210

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PREFACE

The operating principles of three of the four models in the DPC (Data Printer Corp) 1200 CHAINTRAIN™ Line Printer Series (Models CT-1260, CT-1290, and CT-1210) are described in this manual entitled Principles of Operation (DPC Form 1260/90/10-2). Its purpose is to prepare you to perform the maintenance procedures outlined in the companion Maintenance Instructions manual (DPC Form 1260/90/10-3).

The operating principles and maintenance procedures for the fourth model in the DPC 1200 Series (Model CT-1200) are described in a similar set of manuals, entitled Principles of Operation (DPC Form 1200-2) and Maintenance Instructions (DPC Form 1200-3).

Two additional manuals, each of which covers all four models in the DPC 1200 Series, are also included in your printer's documentation package: Operating Instructions (DPC Form 1200-1), and Illustrated Parts Breakdown and Circuit Diagrams (DPC Form 1200-4).

Additional copies of any of these manuals can be obtained from your local DPC representative or by writing directly to Data Printer Corp at the address below. The price of each manual is listed in the current issue of the Customer Services Catalog, a free copy of which can be obtained by writing or phoning the DPC Customer Services Department in Malden, Massachusetts.

The postage-paid "Readers' Comments" card at the end of this manual is provided for your convenience if you wish to suggest improvements to this manual. We welcome your comments.

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CHAPTER 1
INTRODUCTION

1.1 OBJECTIVES

This manual describes the principles of operation of three of the four models in the DPC 1200 CHAINTRAIN™ Line Printer Series: CT-1260, CT-1290, and CT-1210. Its purpose is to prepare you to perform the maintenance and repair operations described in the companion Maintenance Instructions manual (DPC Form 1260/90/10-3).[1]

Written from a Field Service point of view, the chapters that follow present material in a logical, step-by-step way in order to build the kind of understanding that makes it possible to service a printer with confidence and dispatch. Model- and option-related differences are pointed out where appropriate so that careful reading will enable you to understand the operation any CT-1260, CT-1290, or CT-1210 printer, however configured.

1.2 METHOD OF TREATMENT

Although each of the three models dealt with in this manual can be configured in a variety of ways, all consist of two basic subsystems: (1) a electromechanical, back-impact Print System, based on the DPC CHAINTRAIN™ lateral type carrier; and (2) a programmable Control System, based on an 8080A CPU.

For purposes of this discussion, the Print System shall be understood to include all mechanisms and related mechanical adjustments needed to print a line of data and feed ribbon and paper. The Control System shall be under-

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[1]The fourth model in this series, the CT-1200, differs sufficiently in operation from the other three to warrant treatment in a separate Principles of Operation manual (DPC Form 1200-2). Its companion Maintenance Instructions manual is DPC Form 1200-3.

stood to include all drive, control, and interface circuitry, power supplies and power-sequencing circuitry, and all indicators and switches needed to make the Print System perform its printing and paperfeeding tasks. Because the nature of the Control System is determined in large part by the nature of the Print System it must control, a detailed description of the Print System (Chapter 2) precedes a detailed description of the Control System (Chapter 3).

Some familiarity with the operation of back-impact printer mechanisms would be helpful, but this manual is not written in a way that makes such knowledge essential. If you are new to printer mechanisms, you will find the footnotes in Chapter 2 informative.

Because printers in the DPC 1200 Series are microprocessor-controlled, understanding this manual requires some familiarity with the operation of small microcomputer systems. The reference books mentioned at the beginning of Appendix C provide helpful background material if you are unfamiliar with the operation of these devices.

If you have not already done so, read through the Operating Instructions manual (DPC Form 1200-1) before proceeding: this manual was written on the assumption that you have at least an operator's familiarity with DPC 1200 Series printers. Read also the "INTRODUCTION" to the Illustrated Parts Breakdown and Circuit Diagrams manual (DPC Form 1200-4) so that you will be able to locate and understand drawings referred to in this manual.

1.2.1 Appendices

Appendices containing useful reference material have been placed at the back of this manual for your convenience. They are as follows:

Appendix A. Flow charts of a typical operating program used in CT-1260, CT-1290, and CT-1210 CHAINTRAIN™ Line Printers.

Appendix B. Tables that show how to interpret the binary error

codes displayed by the Diagnostic LED's at the rear of the printer whenever "CALL SERV" or "VF ERROR" are illuminated on the right-hand control panel.

Appendix C. Intel data sheets for the following: the 8080A "Eight-bit Microprocessor" (CPU), the 8224 "Clock Generator and Driver," the 8228 "System Controller and Bidirectional Bus Driver," the 8205 "High Speed 1 of 8 Binary Decoder," the 8212 "Parallel 8-bit I/O Port," and the 8214 "Priority Interrupt Control Unit" (PICU).2

Appendix D. List of abbreviations used in this manual and on the Circuit Diagrams (CD's) found in the Illustrated Parts Breakdown and Circuit Diagrams manual (DPC Form 1200-4).

1.2.2 CD and IPB References

CD and IPB references in this manual point to Circuit Diagrams (CD's) and Illustrated Parts Breakdowns (IPB's) contained in the Illustrated Parts Breakdown and Circuit Diagrams manual (DPC Form 1200-4). Such references are liberally scattered throughout this manual to encourage familiarity with that important document.

A reference such as "IPB 26-28" should be understood to mean IPB Figure 26, Index Number -28, which calls out the 1/2" Strobe Sensor in an exploded view drawing of an 8-Channel Vertical Format Unit (VFU).

A reference such as "CD 3.0.0" should be understood to mean one drawing (DWG. NO. C40006, Sheet 1 of 6) in a series of six drawings that show in

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[2]The data sheets in Appendix C have been reprinted by permission of the Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA. 95051.

schematic form the circuitry on the Traffic Control Board. A reference such as "CD 3.X.X" should be understood to mean the entire series of six drawings.

The Illustrated Parts Breakdown and Circuit Diagrams manual (DPC Form 1200-4) contains the following basic set of CD's:

Series	Dwg. No.	Description
0.X.X	C40020-22	Motherhood Connectors J-201, J-202, J-211, J-212, J-213, and J-214.
1.X.X	C40004	DPC Standard I/O Board.
2.X.X	C40002	Controller (CPU) Board.
3.X.X	C40006	Traffic Control Board.
4.0.0	C40012	Paperfeed Stepper Drive Board
5.0.0	40025	LSI Hammer Driver Board.
6.0.0	C40010	Power Control Board.
7.0.0	D40028	Control Panel Switch Wiring.
11.0.1	D40015	CT-1290, CT-1210, and CT-1200 Power Supply manufactured by Power Supplies Incorporated (PSI). This supply carries the number PSI 1196.
11.0.1	D40023	CT-1290, CT-1210, and CT-1200 Power Supply manufactured by North Electric Company (NECO). This supply carries the number NECO 8806A.
11.0.1	D40016	CT-1260 Power Supply manufactured by Power Supplies Incorporated (PSI). This supply carries the number PSI 1207.
12.0.1	40026	Power Distribution Diagram.

Individual copies of the Illustrated Parts Breakdown and Circuit Diagrams manual may contain additional CD drawings to reflect the actual configuration of your particular printer. Any CD reference in this manual should be

understood to refer only to the drawings listed above rather than to any additonal drawings.

1.3 FIELD SERVICE PHILOSOPHY

CT-1260, CT-1290, and CT-1210 printers are complete, self-contained, microprocessor-controlled back-impact line printers that produce hardcopy output one-line-at-a-time from stored digital data sent from an external device. From a Field Service point of view, the use of a programmable microprocessor-based Control System has two important advantages.

First, it simplifies troubleshooting by permitting expanded self-diagnostic capability in the form of five Diagnostic LED's, located on the Controller Board (CD 2.3.0 and IPB 67-16). The LED's, which display a binary error code whenever "CALL SERV" or "VF ERROR" is illuminated on the right-hand control panel, are visible through a clear plastic panel at the rear of the printer. The diagnostic codes (listed in Appendix B) give you a powerful tool for locating the cause of almost any malfunction.

Second, because microprocessor-control permits most individual printer characteristics to be "programmed-in" instead of being "hard-wired," printers in this series have the minimum possible number of model- and option-related differences at an electrical hardware level. This results in circuitry that is more flexible and easier to understand.

Expanded diagnostic capability and consistent, easily understood electrical hardware make Field Service a relatively simple matter of mechanical and electrical adjustment, parts repair and replacement, and board substitution--all of which can be carried out logically and efficiently once the general principles of operation are understood.

Although a familiarity with the operation of the operation of the 8080A CPU and its support devices would be helpful to readers of this manual, an intimate knowledge of these components--or the operating program that "drives"

them--is not needed to perform competent Field Service: testing down to the chip level is not practical when servicing a microprocessor-controlled printer in the field.

For the most part, major differences among CT-1260, CT-1290, and CT-1210 printers are confined to the area of "firmware"--the Read Only Memories (or ROM's) that contain the operating program that tells the CPU what to do. That program--which "particularizes" each printer according to model and equipment selected--is contained in six 512-byte ROM's that are located on the Controller Board (CD 2.2.0 and IPB 67-41). A seventh position for one additional ROM is available for program expansion. If present, that ROM will usually contain a "check load" subroutine that permits the CPU to verify the accuracy of vertical format data loaded from punched tape. Although Field Service does not require an intimate knowledge of a particular printer's operating program, you should have a general idea of what that program does. To that end, the operation of a typical operating program is presented in simplified flow chart form in Appendix A.

1.4 MODEL IDENTIFICATION

The DPC 1200 Series is made up of four standard models, each of which can be reconfigured through the selection of optional equipment. The four basic model numbers are CT-1260, CT-1290, CT-1210, and CT-1200. The last two digits in each of these numbers reflect the rate of throughput that is achieved by that model when it is configured with 64-character "arrays": CT-1260 (600 LPM), CT-1290 (900 LPM), CT-1210 (1000 LPM), and CT-1200 (1200 LPM).[3]

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[3] In all models, however configured, the CHAINTRAIN™ type carrier transports a font containing 384 characters. These are divided into an integral number of identical arrays, each of which contains one each of the characters included in the font.

Other array sizes (48, 96, and 128) are available as an option on each of the four models. Array size is indicated by means of a hyphenated suffix appended to the basic model number stamped on the nameplate: CT-12XX-48 (a DPC 1200 Series printer equipped with eight 48-character arrrays, where XX = 60, 90, 10, or 00), CT-12XX-64 (a DPC 1200 Series printer equipped with six 64-character arrays), CT-12XX-96 (one equipped with four 96-character arrays), and CT-12XX-128 (three 128-character arrays).

The primary reason for the difference in the rate of throughput between different models equipped with arrays of the same size is a difference in the speed of the type carrier: CT-1260 (110 IPS), CT-1290 (185 IPS), CT-1210 (220 IPS), and CT-1200 (256 IPS).[4]

Because the speed of each model's type carrier remains constant regardless of array size, decreasing array size produces a corresponding increase in a model's rate of throughput. Conversely, increasing array size produces a corresponding decrease in a model's rate of througput. The various rate of throughput that can result are illustrated in Table 1-1.

Your printer's model number is stamped on a nameplate mounted on the front yoke cover as shown in Figure 1-1. The nameplate can be seen after lifting the canopy and pulling down the hinged front panel located above the paper bay doors at the front of the machine. Check your model number and keep it in mind as you read.

CAUTION

If your printer is a CT-1200, you are reading the wrong manual. The principles of operation for that model are found in DPC Form 1200-2.

[4] IPS stands for inches per second.

TABLE 1-1

Throughput in Lines per Second (LPS)

Model Number	Array Size -48	-64	-96	-128
CT-1260	760 LP	600 LP	430 LP	330 LP
CT-1290	1100 LP	900 LP	670 LP	530 LP
CT-1210	1200 LP	1000 LP	750 LP	600 LP
CT-1200	1450 LP	1200 LP	900 LP	725 LP

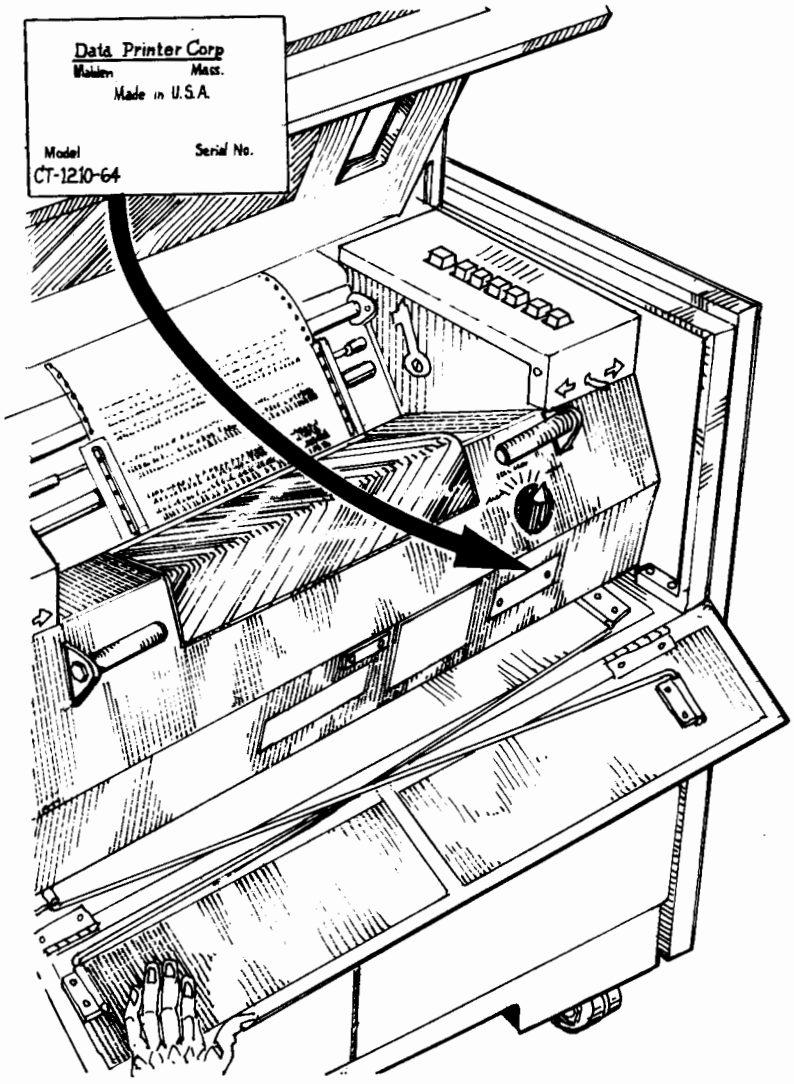

Figure 1-1. Nameplate Location.

CHAPTER 2
PRINT SYSTEM OPERATION

2.1 INTRODUCTION

A thorough understanding of Print System operation is a prerequisite for understanding many of the more complex operations of the Control System. In the subsections that follow, the Print System is treated as three function-related subsystems: (1) the Print Mechanism (2.2), (2) the Ribbonfeed Mechanism (2.3), and (3) the Paperfeed Mechanism (2.4). Each is examined in detail in order to lay the groundwork for an adequate understanding of the Control System.

2.2 PRINT MECHANISM

The Print Mechanism consists of two basic subassemblies: (1) a bank of print hammers and their corresponding actuators, mounted on a stationary frame at the back (non-print) side of the paper path; and (2) the DPC CHAINTRAIN™ lateral type carrier (or "chain") and its associated components, mounted on a movable yoke at the front (print) side of the paper path (Figure 2-1).

The yoke can be "opened"--that is, swung away from the hammer bank on the frame--in order to permit paper loading and facilitate servicing. Closing the yoke brings print hammers, paper, ribbon, and chain into proximity so printing can take place. Operation of the printer in the Run Mode requires the yoke to be locked in the closed position by means of a yoke latch lever, located on the right-hand side of the frame assembly.

Paper is held stationary and ribbon is fed continuously during data printout. Printing is accomplished by firing print hammers at appropriate times into the backside of the paper form. The hammers compress column-sized sections of paper and ribbon against selected characters on the chain, thereby creating solid character print impressions on the paper forms. Back-impact printing such as this takes place "on the fly" as character typefaces on the chain are driven laterally past the hammer bank at constant speed. DPC type-

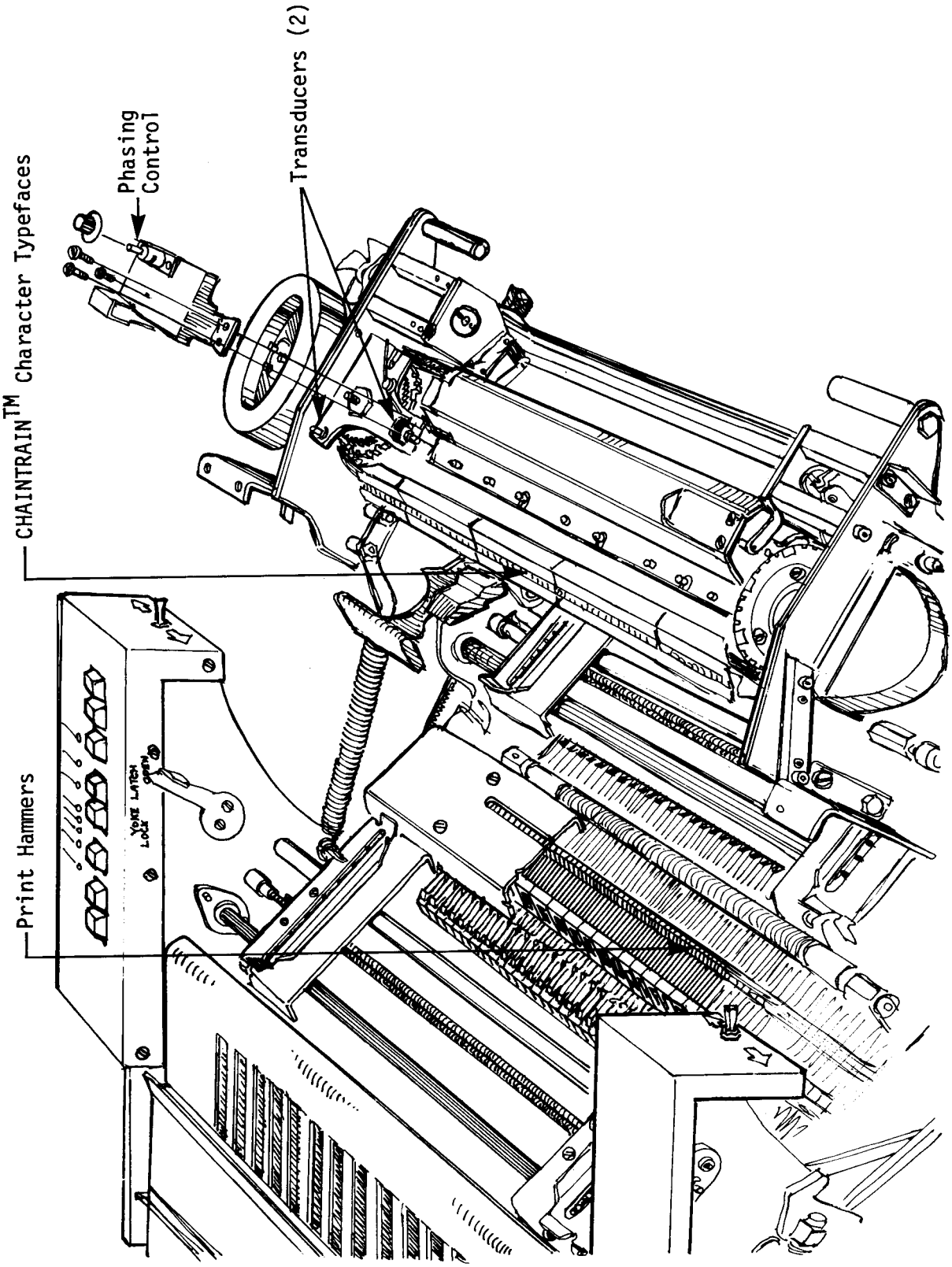

Figure 2-1. Print Mechanism with Yoke Open.

face design precludes the possibility of print quality degradation due to "dynamic growth".[1]

The Control System monitors chain speed, tracks character positions, and determines hammer firing times in response to impulses generated by two variable reluctance transducers that are mounted on an adjustable plate at the right-hand end of the chain assembly. The position of these transducers can be adjusted by means of a PHASING CONTROL, which allows hammer firing time to be advanced or retarded as needed to achieve the best overall print quality. An IMPRESSION CONTROL, also located on the yoke, permits the operator to adjust print hammer striking force in response to ribbon wear or a change in paper form thickness when different forms are loaded.

2.2.1 Yoke Latch and Interlock Switches

Two switches allow the Control System to monitor yoke and latch position (Figure 2-2). Moving the yoke into printing position closes a yoke interlock switch and latching it in that position closes a yoke latch switch. The switches, which are connected in series (CD 7.0.0), interface with the Control System as shown on CD 1.4.1. Operation in the Run Mode will not be initialized or maintained by the Control System if either switch is open.

For maintenance purposes, it is often convenient to operate the printer in the Run Mode with the yoke in the open position. This is easily accomplished by pulling out the plunger on the yoke interlock switch and closing the yoke latch lever. When this is done, both switches will be closed and the Control System will operate normally even though the yoke remains in the open position.

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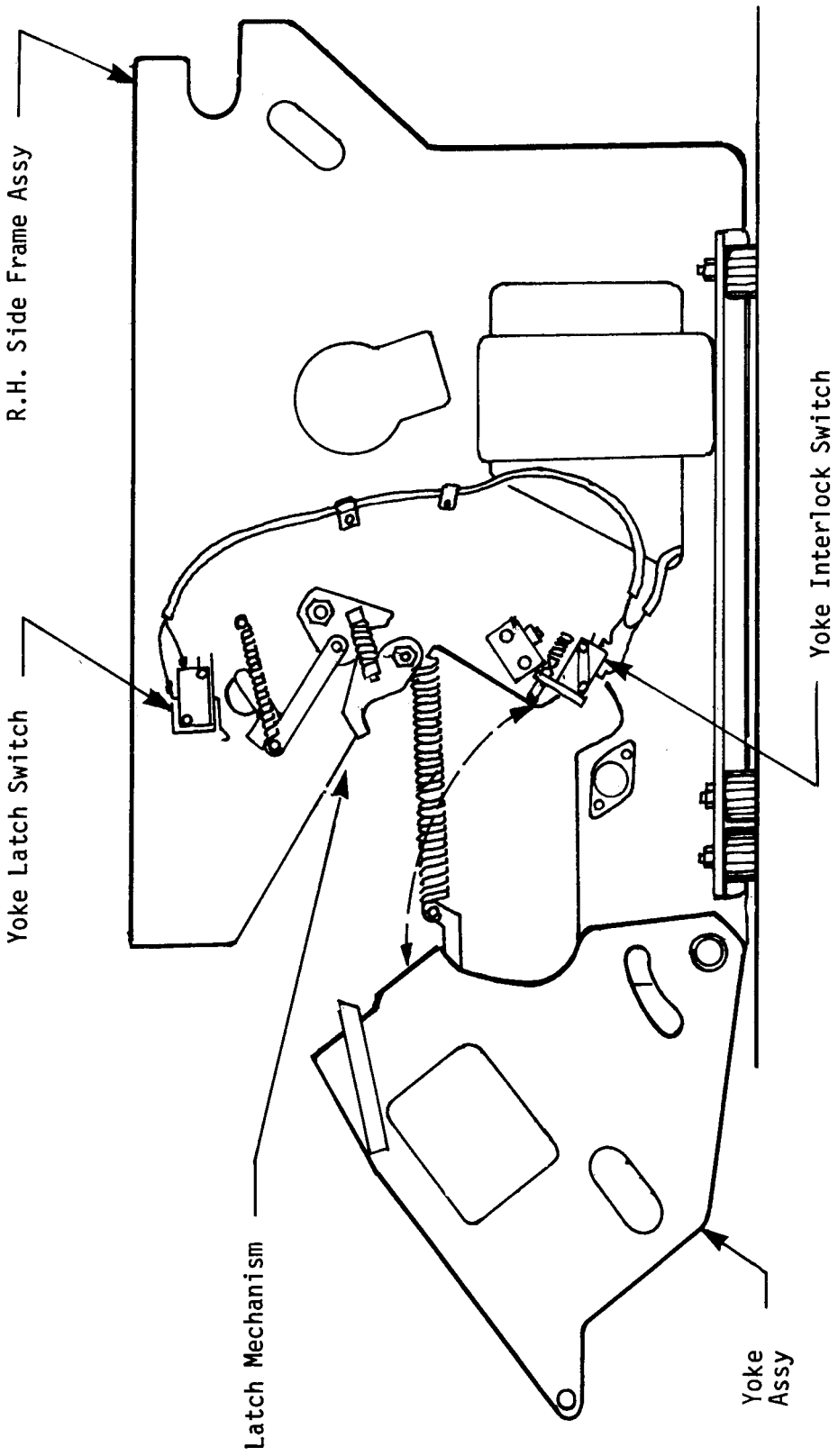
[1]Dynamic growth refers to the broadening of the character imprint that takes place during the brief instant hammer, paper, and ribbon are in contact with a selected character typeface on the moving chain.



RIGHT-HAND SIDE OF PRINTER MECHANISM (CABINET REMOVED)

Figure 2-2. Yoke Latch and Interlock Switches.

CAUTION

When operating the printer open-yoked, always put the PRINT/INHIBIT switch in the INHIBIT position to prevent hammer firing. Hammer firing with the yoke open can result in damage to the print hammers. Note: INHIBIT is ignored when operating in the Remote Mode.

On any printer equipped with the "DPC Standard Interface" that means always put the bottom toggle switch on the test panel in the up position in order to inhibit hammer firing ("SW-1" on IPB 72-18). Regardless of the type of interface, putting the PRINT/INHIBIT switch into the INHIBIT position when operating in the Local Mode will result in the illumination of "PRINT INHIBIT" on the right-hand operator control panel.

2.2.2 Print Hammers and Actuators

All DPC 1200 Series printers come equipped with a hammer bank composed of seventeen 8-up hammer modules, arranged end-to-end on a hammer bar/bumper as shown in IPB 42. Each module consists of eight "single-duty," "free-flight" print hammers and their supporting flexures molded into a plastic base (Figure 2-3).[3] The seventeen modules provide a potential typeline of 136 columns (8 x 17 = 136) spaced ten-columns-to-the-inch. Printers configured for the standard 132 column typeline simply lack actuators corresponding to the last four hammers in the rightmost module (columns 133 through 136). The missing actuators cause those hammers to be recessed--a certain indication that a printer is configured with a 132 column typeline.

Just as one hammer is dedicated to each column position, one electromechanical actuator is dedicated to each of the 132 (136 optional) hammers in-

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[3] Single-duty refers to the fact that each print hammer is dedicated to a single column position. Free-flight means that the hammer flies free of the actuator that drives it before it hits the chain.

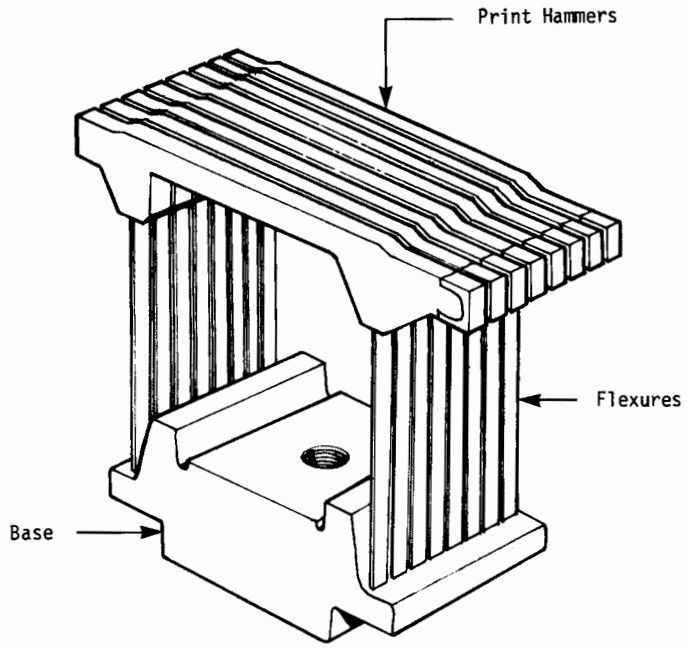


Figure 2-3. Eight-Up Hammer Module.

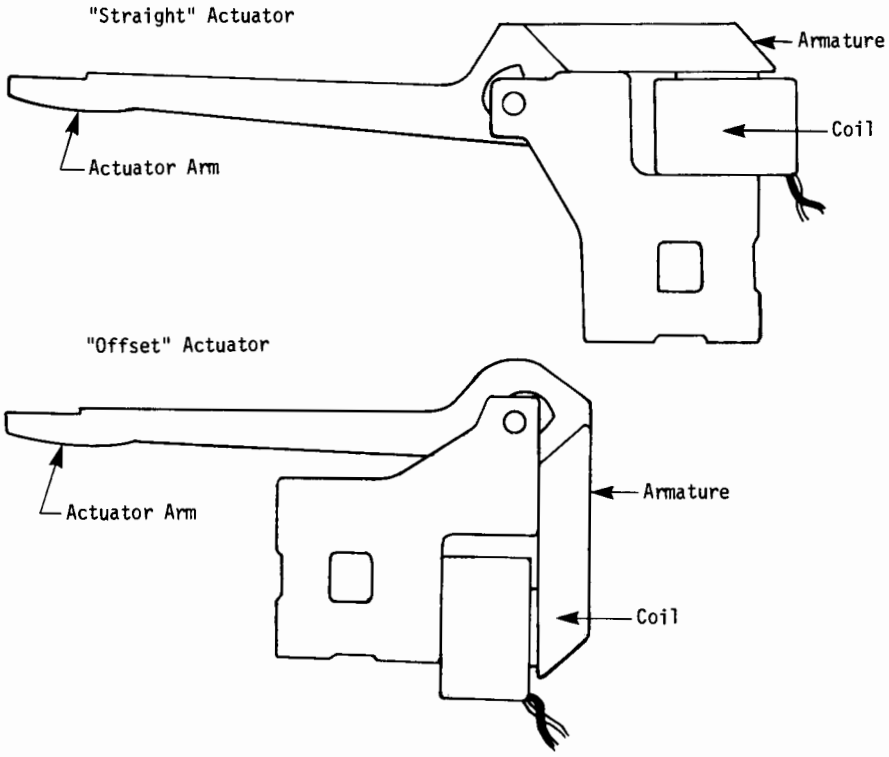


Figure 2-4. Straight and Offset Hammer Actuators.

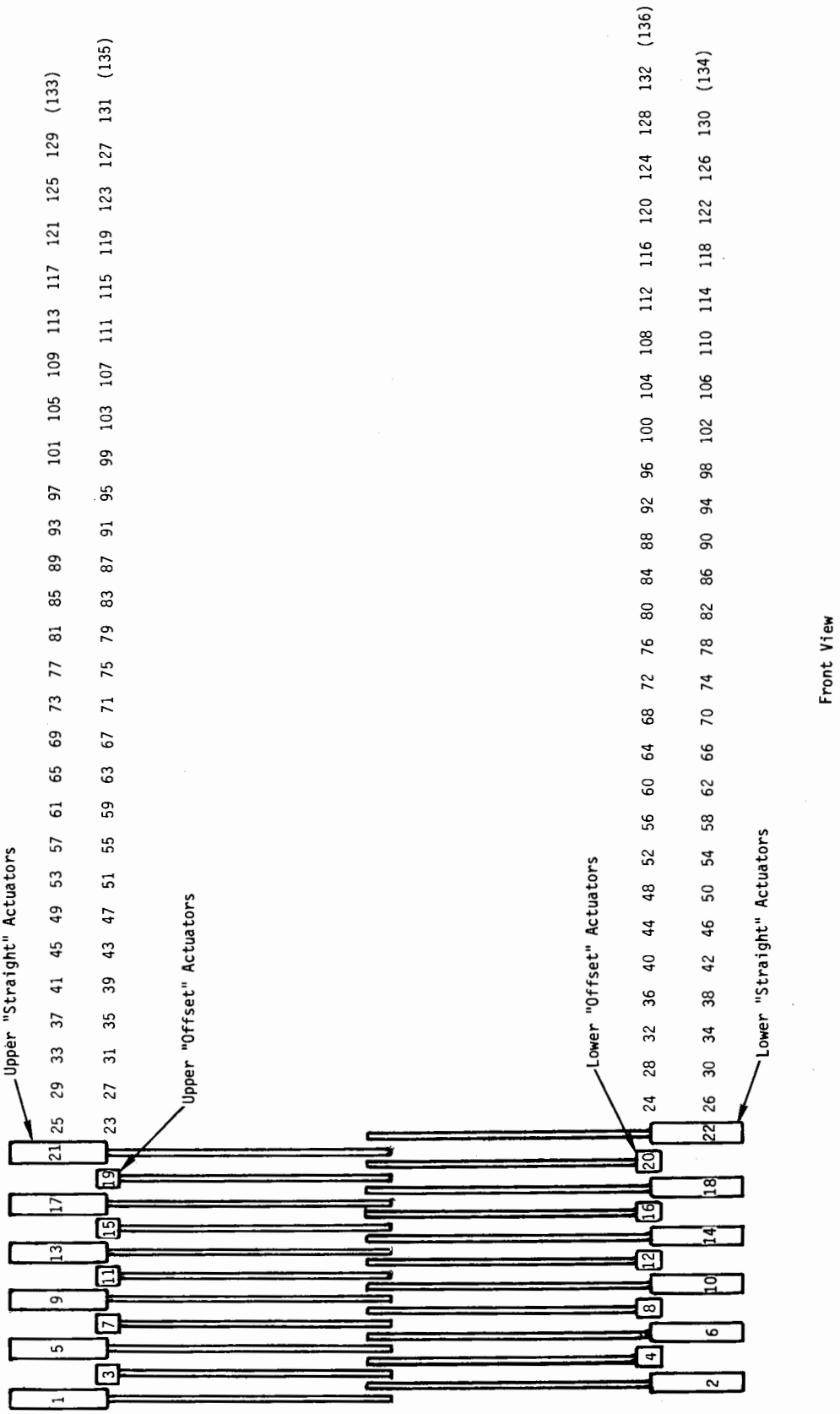


Figure 2-5. Actuator Tip Interlace Pattern.

cluded in the chosen typeline. In order to accommodate the necessary size of the actuator coils, actuators are constructed in both "straight" and "offset" configurations (Figure 2-4) so they can be mounted on the frame in four rows, each of which contains 33 (34 optional) actuators (IPB 39). Figure 2-5 shows the way in which the tips of the actuator arms interlace to accommodate 132 (or 136) hammers in the hammer bank. The hammer bank is wedded to the frame as shown in IPB 38.

Horizontal alignment of the print hammers with the average position of the actuator arm tips is accomplished by adjusting an eccentric located in the right-hand side platen support (IPB 42). Vertical alignment of the hammers with the characters on the chain is accomplished by adjusting set screws in both the right- and left-hand side platen supports (IPB 42).

The resting position of a typical print hammer is shown in Figure 2-6. Under pressure from its supporting flexures, the hammer holds the actuator arm firmly against its corresponding finger on the stop comb bumper. The hammer is fired by briefly energizing the coil in its corresponding actuator. The resulting armature stroke is transferred to the hammer by the actuator arm, which drives the hammer forward toward the chain. Upon completion of the stroke, the accelerated hammer flies free of the actuator tip and pushes paper and ribbon against a selected character on the chain. It then rebounds driving the no-longer-energized actuator back against the stop comb bumper and comes to rest in its original resting position ready to be fired again.

The Control System must fire hammers in advance of actual alignment in order to give the hammers time to travel to the chain. The interval between actuation and impact is called "flight time" and must be equal for all hammers if print quality is to be maintained. When that is the case and the PHASING CONTROL is properly adjusted, no "side clipping" will occur.[4] Any side clip

[4]Side clipping refers to left- or right-hand side cut off of the character imprint.

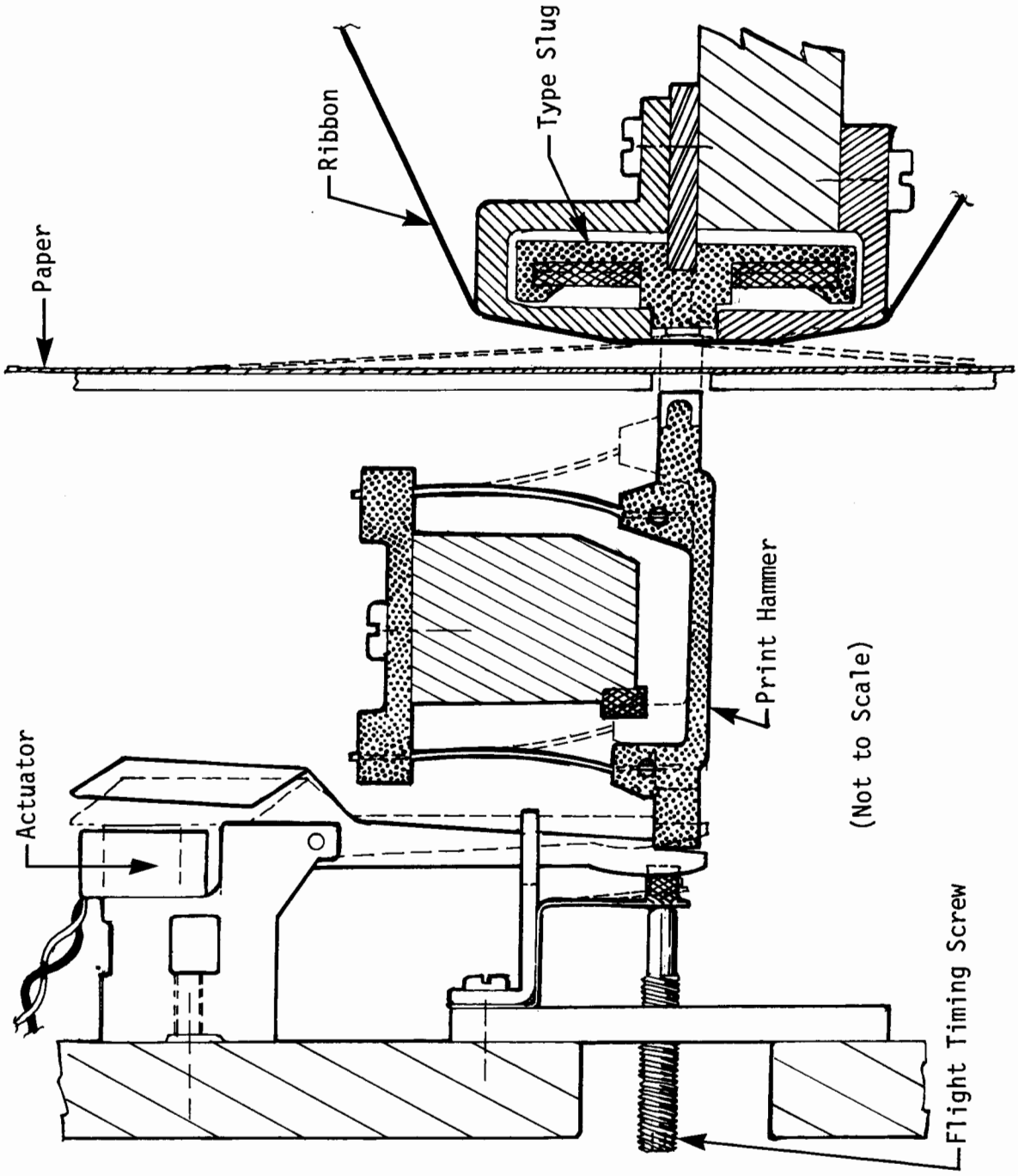


Figure 2-6. Hammer in Resting Position.

ping that cannot be removed by adjusting the PHASING CONTROL is a certain indication that the flight timing of the hammer corresponding to the clipped column position diverges from the overall flight time norm.

Character typefaces move from right (column 132/136) to left (column 1) accross the typeline at constant speed during a print operation. Therefore, right-hand clipping indicates a hammer that prints too soon (flight time too short); and left-hand clipping indicates a hammer that prints too late (flight time too long).

Individual hammer flight time can be adjusted by means of 132 (or 136) flight timing screws, which are accessible from the rear of the printer mechanism. The screws are conveniently arranged on the backside of the frame into two rows divided by a strip label that shows the corresponding hammer/column positions. CT-1290 and CT-1210 printers have a cooling plenum mounted on the backside of the frame assembly that obscures the flight timing screws. The screws may be accessed by removing the rear panel of the plenum as shown in Figure 2-7.

Adjustment of a flight timing screw affects the resting position of its corresponding actuator/hammer pair (Figure 2-6). Lefthand clipping can be removed by turning the appropriate screw clockwise to reduce flight time by moving the resting position closer to the chain. Conversely, right-hand clipping can be removed by turning the screw counter-clockwise to increase flight time by moving the resting position away from the chain. Sufficient tension is preloaded into the hammer flexures at time of manufacture to guarantee return to the same resting position after each firing so that consistency in flight time can be maintained.

All flight timing screws are carefully adjusted at the factory after a thorough run-in period. They will not require frequent attention during the life of the machine. A few may need to be touched up occasionally as part of your quarterly PM routine; and, of course, replacement of actuators or hammer modules will necessitate readjustment of the timing screws affected.

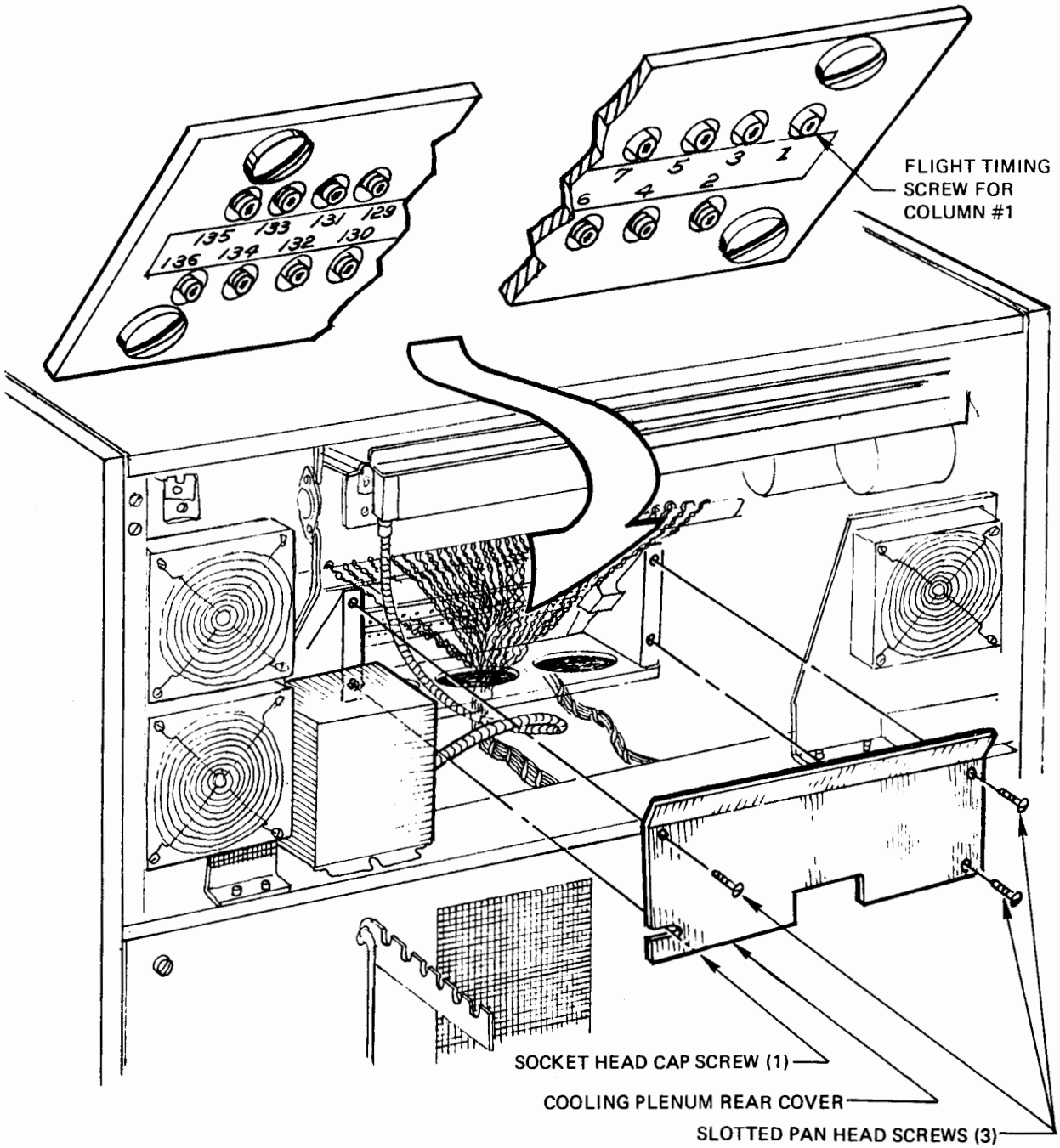


Figure 2-7. Location of Flight Timing Screws.

CAUTION

Excessive adjustment of a flight timing screw can result in parts failure. Follow the instructions in subsection 3.5.1.4.3 of the Maintenance instructions manual (DPC Form 1260/90/10-3) carefully when retiming a hammer.

A good rule of thumb to follow is this. If the clipping problem cannot be improved by turning the flight timing screw less than one full turn, return the flight timing screw to its original position and look for the presence of an electrical or mechanical problem.

2.2.3 DPC CHAINTRAIN™ Type Carrier

The CHAINTRAIN™ lateral type carrier transports forty-eight 8-character type slugs, which are mounted end-to-end on motor-driven double belt loop (Figure 2-8). The resulting 384-character "chain" (48 x 8 = 384) can be divided into an integral number of identical arrays having 48, 64, 96, or 128 characters each. The chain can transport three 128-character arrays (3 x 128 = 384), four 96-character arrays (4 x 96 = 384), six 64-character arrays (6 x 64 = 384), or eight 48-character arrays (8 x 48 = 384). Every array on the chain contains one each of the characters in the chosen font arranged in a fixed sequence "known" to the Control System. Figure 2-9 shows the arrangement of the characters on the eight type slugs that make up one standard 64-character array (8 x 8 = 64).

The chain is driven at constant speed by means of a motor/flywheel drive assembly coupled to a slug drive pulley by a rubber drive belt as shown in Figure 2-10. Chain speed is determined by the size of the motor pulley, which must be appropriate to the motor and model on which it is used (see IPB 43 and 46). Throughput is a function of chain speed and array size.

The Control System activates the run and start windings of the chain drive motor by means of optically-coupled triac circuitry on the "Power Control Board" (CD 6.0.0 and IPB 56-2).

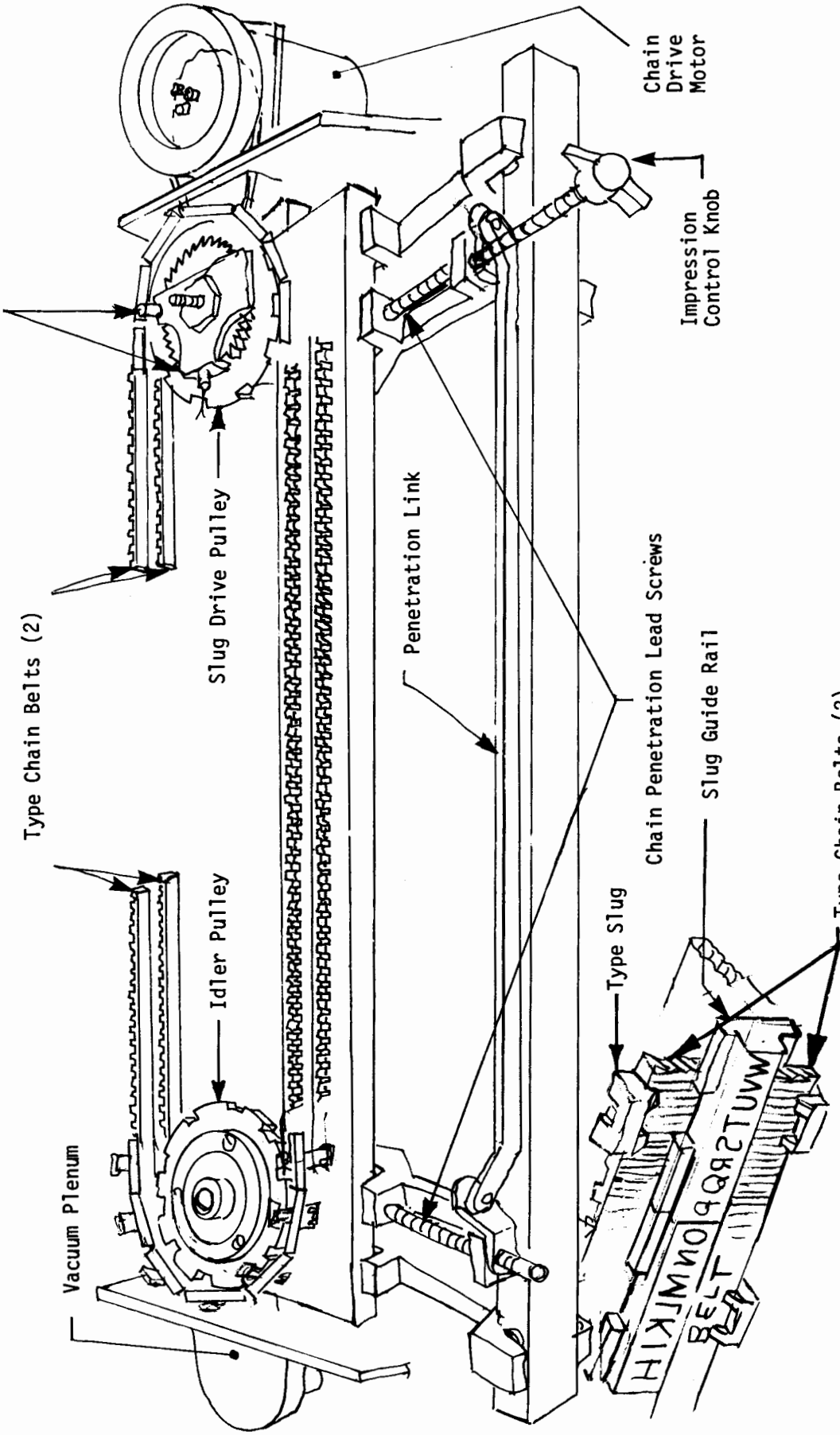


Figure 2-8. DPC CHAINTRAIN™ Lateral Type Carrier.

DPC CHAINTRAIN™ Arrangement
Standard 64-Character Subset of USASCII
(Printout Representation)

Chain Travel Direction

?>=<;:98	76543210	/.-,+*)(	'&%$#"!◊	_^]\[ZYX	WVUTSRQP	ONMLKJIH	GFEDCBA@
8/I	7	6	5	4	3	2	1

Figure 2-9. Typical 64-Character Array.

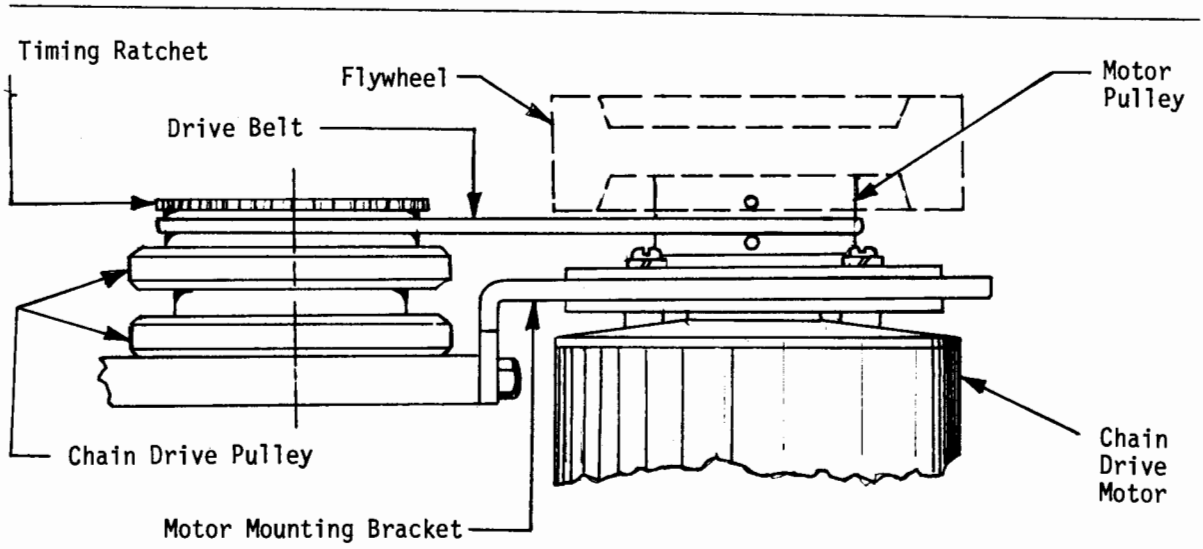


Figure 2-10. Motor/Flywheel Drive Assembly.

Type slugs are pushed from right to left across the typeline in order to prevent alignment problems due to gapping when the chain is run at high speed. The same chain travel direction is maintained on all models in this series for purposes of consistency.

Different chain speeds produce different amounts of dynamic growth in the printout. The faster the chain speed, the greater the dynamic growth. Careful DPC typeface design compensates for this by exercising appropriate amounts of surface area from the vertical lands of the character typefaces. Therefore, type slugs are model-specific: be careful when ordering replacement slugs.

Heavy duty slugs, with character type faces fabricated from specially hardened steel are required equipment on CT-1200 printers. They are available as an option on the other models.

Chain stability and print quality are maintained by two kinds of slug restraints--slug guide rails, and ribbon/slug guides--shown in Figure 2-11.

The front and rear monorail tracks, called slug guide rails, prevent vertical displacement of the type slugs, that would produce destructive instability in the chain. The front guide rail also serves as an anvil when characters on the chain are struck by the hammers. The channels in the backs of the type slugs, which mate with these rails, are oiled by a wick-fed lubricant contained in a bottle at the left front side of the chain assembly (IPB 52-14).

Front upper and lower ribbon/slug guides, the second type of slug restraint shown in Figure 2-11, prevent horizontal displacement of the slugs, which would cause random variations in flight time that would show up as side clipping. They also keep the ribbon from dragging across the chain when it is started or stopped. A mylar ribbon shield is attached to the upper and lower ribbon/slug guides at the right-hand side of the chain to prevent fraying of the right-hand edge of the ribbon.

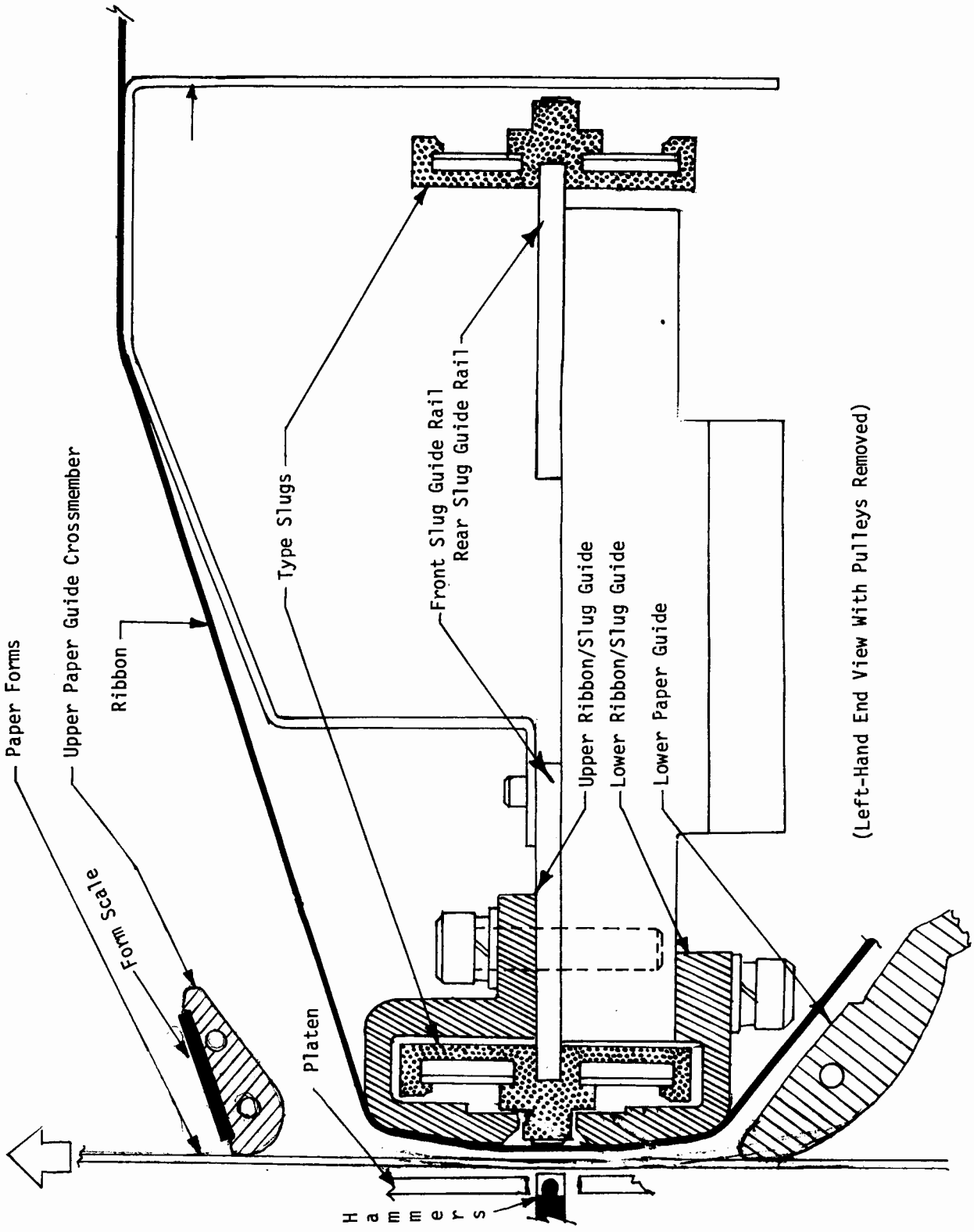


Figure 2-11. Slug Guide Rails and Ribbon/Slug Guides.

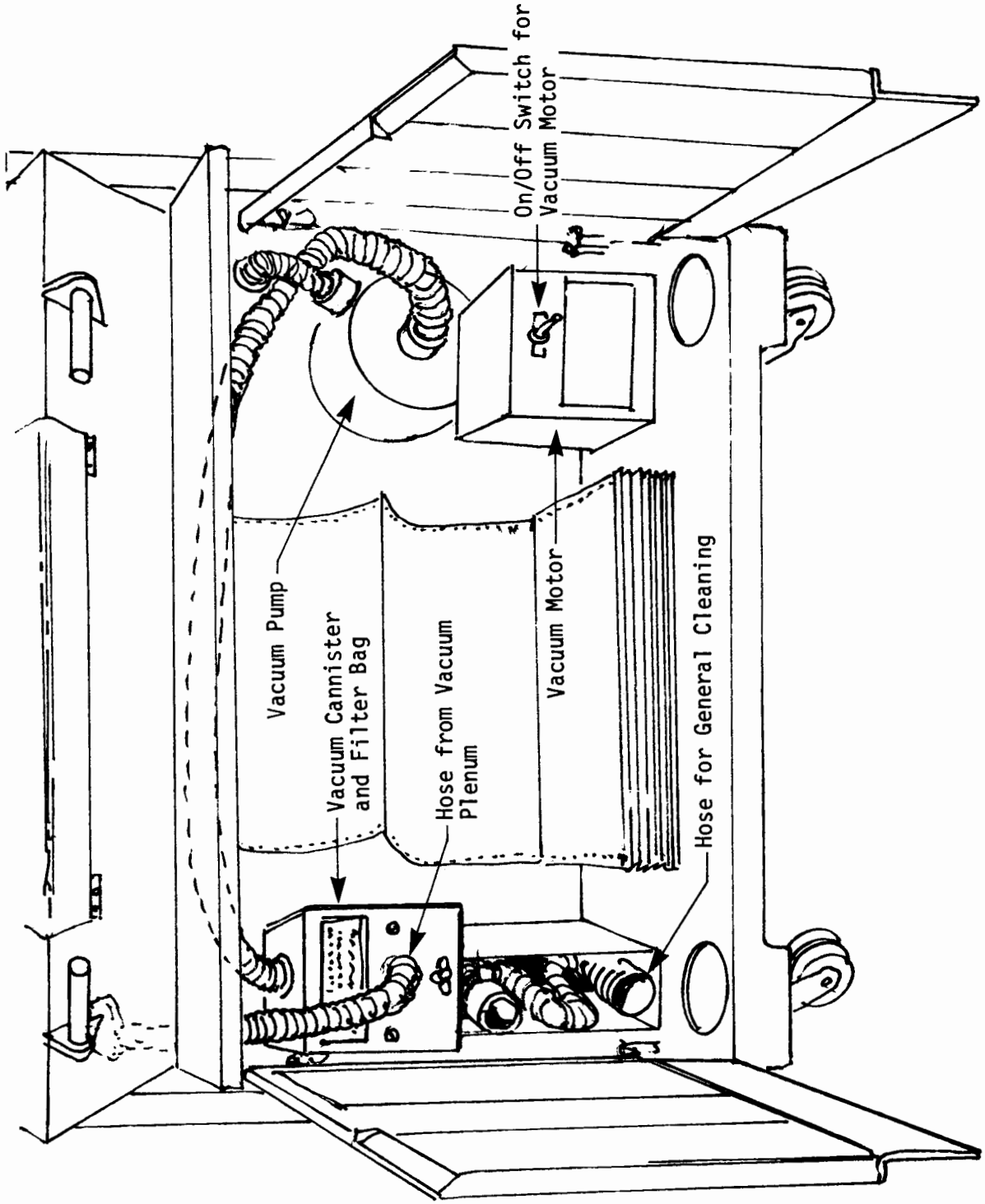


Figure 2-12. Vacuum Cleaning System.

Ribbon particles and paper dust are the unavoidable by-products of any impact printing process. Because they accumulate quickly in printers run at high rate throughput, a vacuum plenum is required equipment on CT-1210 (Figure 2-8). It is optional on the CT-1290 and not available--or necessary--the CT-1260.

The vacuum plenum is connected by means of a hose to a vacuum cleaning system that is located beneath the printer mechanisms, behind the paper bay doors (Figure 2-12). Wired in parallel with the run windings of the chain drive motor, the vacuum motor is turned on and off simultaneously with the chain (regardless of the position of the vacuum cleaning system's ON/OFF switch) in order to guarantee continuous cleaning whenever the machine is printing (CD 12.0.1).

A vacuum cleaning system without the vacuum plenum is available as an option for routine clean up of the printing mechanism on CT-1260 Printers. Its vacuum motor is not wired in parallel with the run windings of the chain drive motor.

2.2.4 Hammer-to-Character Alignment

All print hammers in the hammer bank are uniformly spaced 0.100-inch center-to-center to guarantee a ten-columns-to-the-inch typeline. To avoid "ghosting", characters on the chain must be spaced more widely to produce something other than a 1:1 alignment ratio between hammers and characters.[5] DPC 1200 Series printers have characters spaced at 0.133-inch center-to-center. This results in a 4:3 hammer-to-character alignment ratio, in which

---

[5]Ghosting refers to the unintentional partial printing of the character before and after the selected character on the chain. Because the paper/ribbon sandwich compressed against the selected character by the print hammer is of necessity wider than one single column position, ghosting would be unavoidable on a back impact printer having a 1:1 alignment ratio.

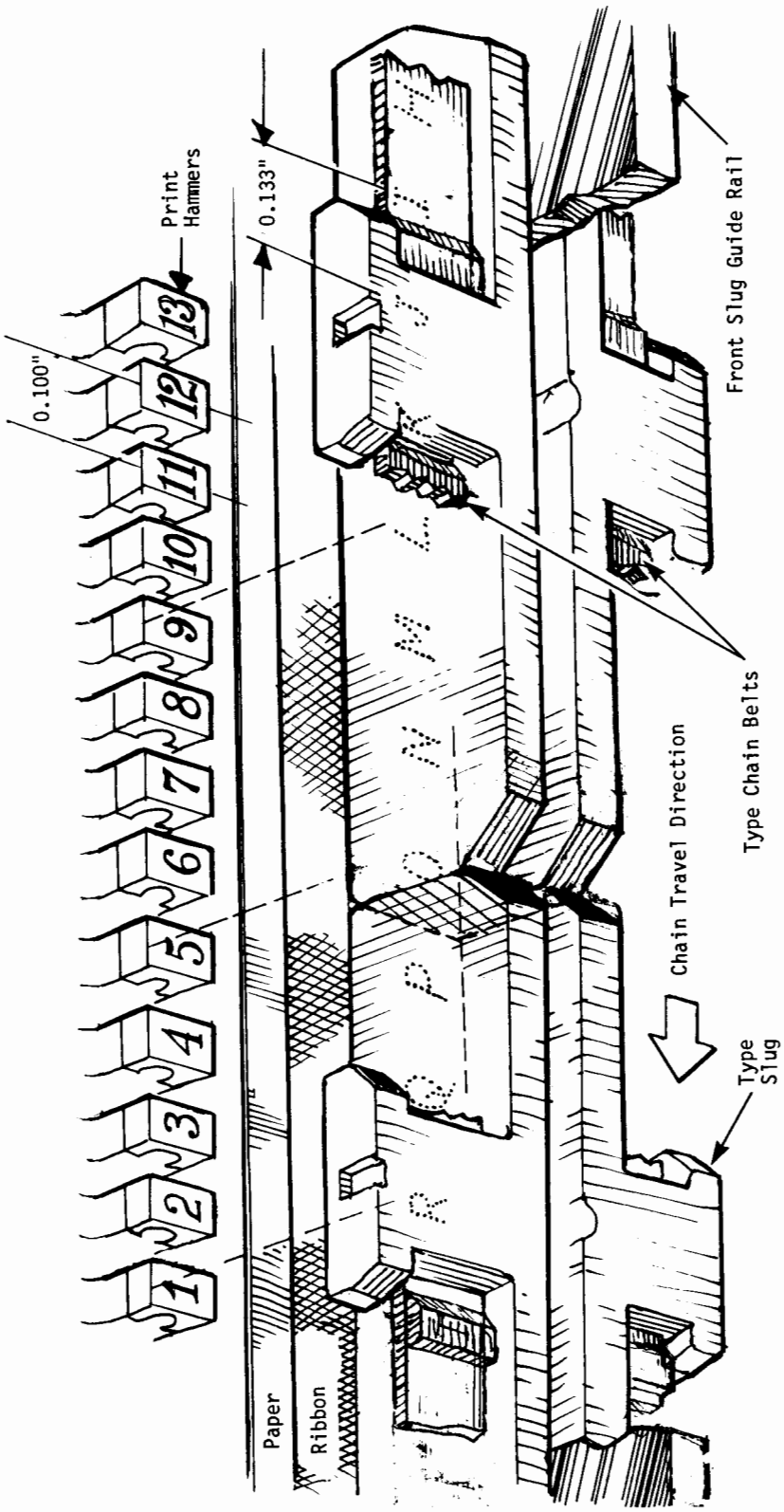


Figure 2-13. Four-to-Three Alignment Ratio.

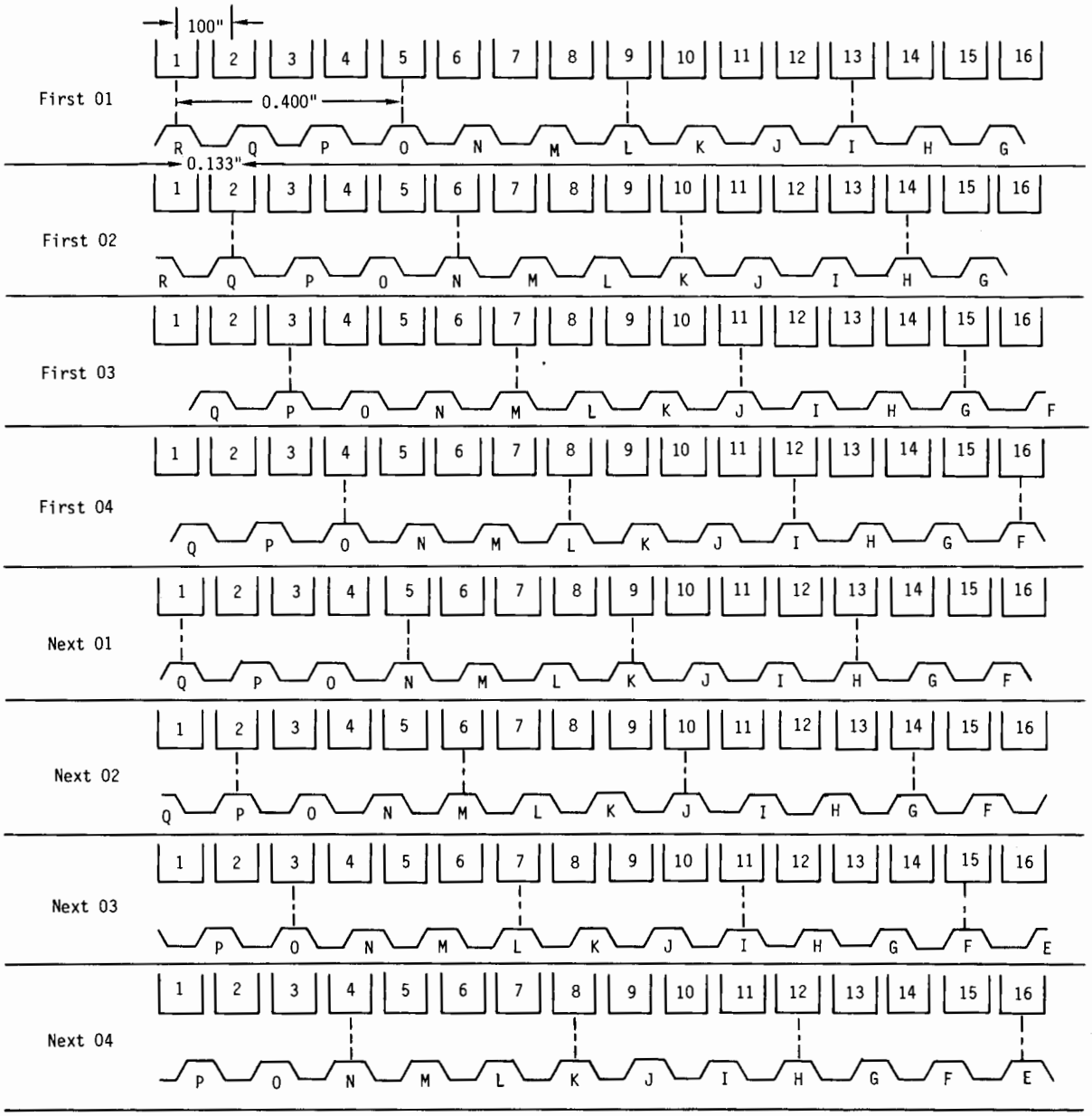


Figure 2-14. Two Consecutive Four Phase Alignment Sequence.

only one-fourth of the print hammers in the hammer bank can be aligned with the characters on the chain at any given instant (Figure 2-13).

The chief consequence of selecting a 4:3 alignment ratio is the fact that alignment of "some character" with every print hammer necessarily takes place in four successive phases as shown in Figure 2-14. As the characters on the chain are pushed at constant speed from right-to-left past the print hammers alignment "streams" repeatedly left-to-right within four-column segments of the typeline in a constant succession of four phase alignment sequences. Figure 2-14 shows two such consecutive four phase alignment sequences covering the first sixteen columns of the typeline.

Each time a new four phase alignment sequence occurs, "some next character" in the font becomes available for printout in each column position (compare "Phase 1" to "Next Phase 1," "Phase 2" to "Next Phase 2," and so forth in Figure 2-14). Thus, every character in an N-character font will be presented for printout to every column position in "N" four phase alignment sequences. For example, every character in a 64-character font will be presented to every column position each time the chain moves through 64 four phase alignment sequences (256 discrete single phase alignments). Clearly, then, the printing of a single line is a serial process.

2.2.5 Character and Index Strobe Transducers

The Control System tracks character positions, monitors chain speed, and determines print hammer firing times by means of two variable reluctance transducers ("RP-101" and "RP-102" on CD 7.0.0) that are mounted in tandem on an adjustable pick-up mounting plate at the right-hand end of the chain assembly (Figure 2-15).

Transducer RP-101 generates an analog Character Strobe (CSTB) pulse each time the chain moves a distance equivalent to one character. It does this by sensing the passage of teeth on a timing ratchet mounted on top of the slug drive pulley. Each CSTB signals onset of the next four phase alignment sequence.

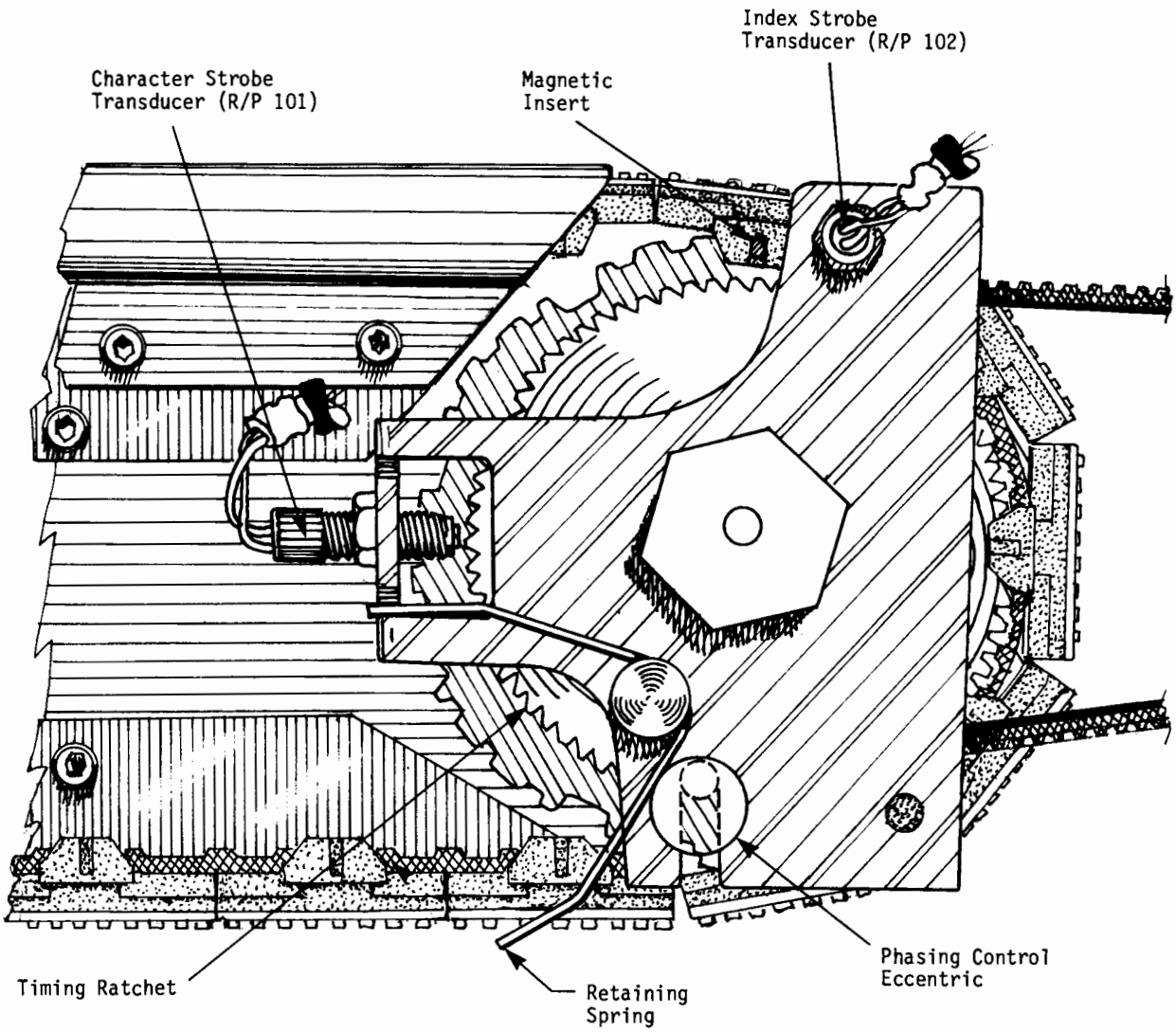


Figure 2-15. CSTB and INDEX Variable Reluctance Transducers.

Transducer RP-102 generates an analog Index Strobe (INDEX) pulse each time the chain moves a distance equivalent to one array. It does this by sensing the passage of magnetic inserts strategically placed in the upper part of one type slug in the same position in each array (For Example slug #8 in Figure 2-9). Each INDEX pulse signals the onset of the next series of "N" four phase alignment sequences, where "N" equals array size. Thus each CSTB pulse is meaningful for purposes of character position tracking only by virtue of its order of occurance after a preceding INDEX pulse.

CAUTION

Careful adjustment of the CSTB (RP-101) and INDEX (RP-102) transducers is essential for proper operation. These adjustments are described in detail in section 3.5.1.2.3 of the Maintenance Instructions (DPC Form 1260/90/10-3).

2.2.6 Impression Control

One purpose of the IMPRESSION CONTROL (IPB 52) is to allow the operator to fine-adjust hammer-to- chain distance (called "penetration") to prevent embossing or punch-through when using single-part forms and to compensate for lightness of impression on the top (visible) form when using multi-part forms.

Another purpose of the IMPRESSION CONTROL is to allow the operator to compensate for improper print impression density due to ribbon wear. Hence, the lables "LIGHT" and "DARK" adjacent to the extreme left- and right-hand positions of the IMPRESSION CONTROL.

Altering penetration by means of the IMPRESSION CONTROL changes print hammer flight time uniformaly across the typeline and therefore, may, produce side clipping. Any clipping that results can be removed by readjusting the PHASING CONTROL, described in the next section.

The IMPRESSION CONTROL and the PHASING CONTROL function interactively although there is no mechanical or electrical linkage between the two. The IMPRESSION CONTROL should always be adjusted first to provide the best print

impression obtainable for the particular forms and ribbon being used. Following that, the PHASING CONTROL should be adjusted to remove any side clipping that may have resulted from adjusting the IMPRESSION CONTROL. When multi-part paper forms are in use, operators should remember to check the back as well as the top form for proper phasing and print density.

2.2.7 Phasing Control

Because adjustment of the IMPRESSION CONTROL introduces changes in flight time, fire pulse lead time must be operator-adustable within certain narrow limits in order to permit removal of any side clipping that results from readjustment of the IMPRESSION CONTROL.

Fine adjustment of hammer firing time is accomplished by means of a PHASING CONTROL that permits movement of the CSTB and INDEX transducers in tandem about a common axis. As shown in Figure 2-16, a phasing bracket subassembly is mounted above the pick-up mount/spring subassembly that carries the CSTB and INDEX transducers. After pushing the retaining spring on the pick-up mount to the left, the eccentric at the bottom of the phasing control shaft is inserted into the slot in the pick-up mount/spring subassembly. Once the phasing control bracket subassembly is bolted in place, rotating the PHASING CONTROL knob will cause the pick-up mount to rotate by means of the eccentric that rides in the pick-up mount slot. The setting of the PHASING CONTROL is held in place by the retaining spring on the pick-up mount.

Figure 2-17 shows the effect of rotating the PHASING CONTROL from left to right. When the knob is rotated to the left, the pick-up mount is rotated to the right, advancing hammer firing time. Conversely, when the knob is rotated to the right, the pick-up mount is rotated to the left retarding hammer firing time.

During factory assembly, the pan head screws (shown in Figure 2-16) are backed off slightly to permit lateral adjustment of the phasing control shaft subassembly. With the PHASING CONTROL knob centered so the eccentric is in its neutral top-of-slot position, the phasing control shaft subassembly is

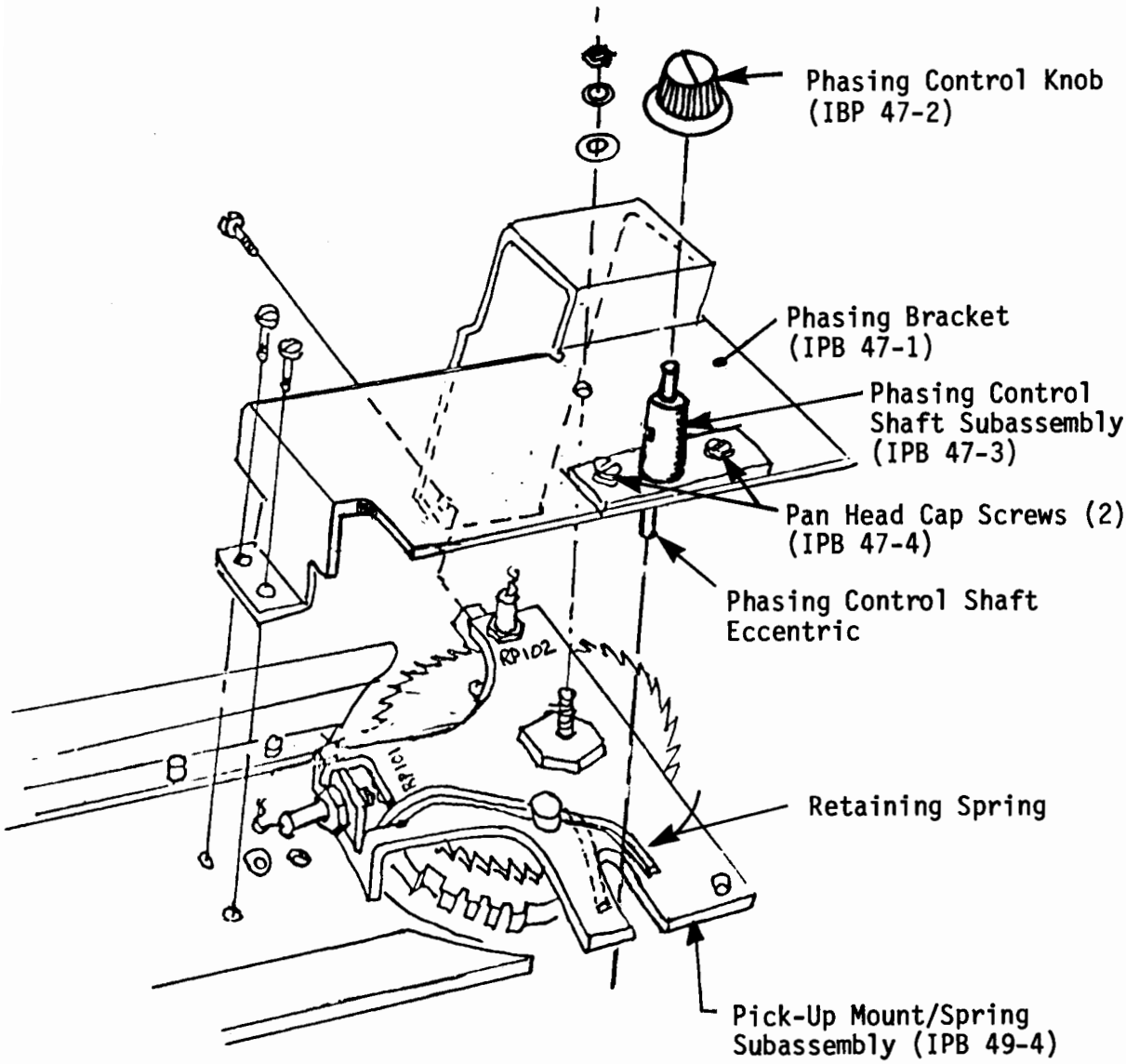


Figure 2-16. Phasing Control Assembly.

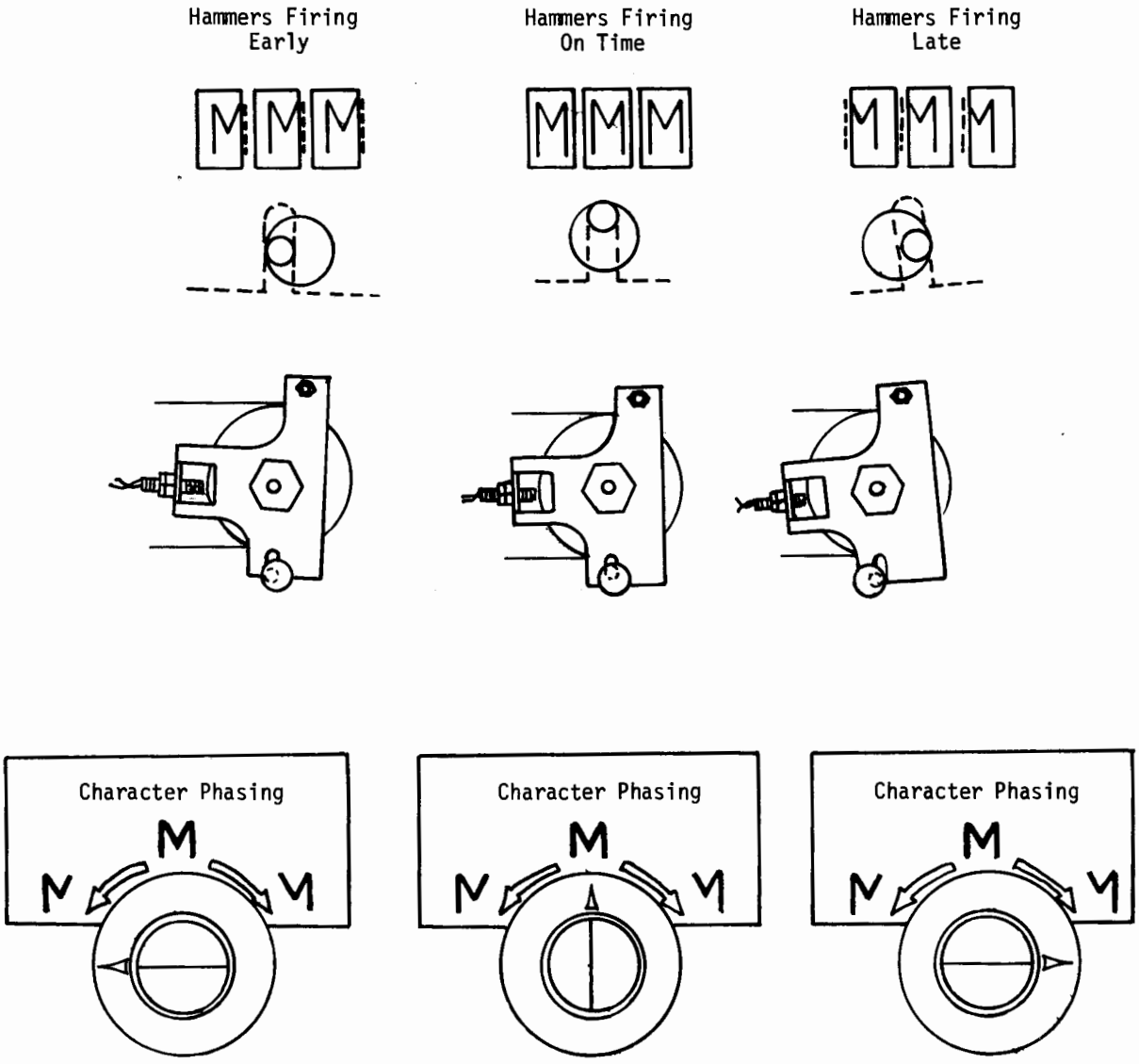


Figure 2-17. Phasing Control Operation.

shifted in the appropriate direction to center characters in their column positions as shown in the drawings down the center of Figure 2-17. The pan head screws are then tightened securely and the PHASING CONTROL knob removed and reinstalled in the same position after the right-hand yoke cover is mounted in place.

Once this is done, turning the PHASING CONTROL knob to the left will produce right-hand side clipping; conversely, turning it to the right will produce left-hand side clipping. That is the meaning of the "CHARACTER PHASING" decals shown in Figure 2-17. If the phasing control shaft is properly centered it will be impossible to phase-in another character when the PHASING CONTROL knob is rotated to its extreme right or left position. The decal is useful when centering the phasing assembly as described in Section 3.5.1.4.2 ("Character Phasing Adjustment") of the Maintenance Instructions (DPC Form 1260/90/10-3). The decal DOES NOT show the direction in which to turn the PHASING CONTROL knob in order to cure side clipping.

CAUTION

When performing this adjustment follow the maintenance instructions carefully: it is not only possible to phase in an entirely different character but also possible to damage print hammers and slugs.

The diamond-shaped character on slug #5 (Figure 2-9) occupies the position of the space code and can never print when the phasing control shaft is properly positioned laterally. If the diamond shows up when printing a RIPPLE pattern, it is a certain indication that the phasing control shaft subassembly is out of adjustment.

Now for a simple rule: keep your eyes on the copy and turn the PHASING CONTROL knob to the right to eliminate right-hand side clipping or to the left to eliminate left-hand side clipping.

Remember: clipping that cannot be removed by means of the PHASING CONTROL is an indication that the flight time of the hammer corresponding to the clipped column position is out of adjustment.

2.2.8 Hammer Driver Cabling

Each hammer actuator is energized by means of a dedicated constant current hammer driver, a typical example of which is shown at the bottom of CD 5.0.0 ("LSI Hammer Driver Board"). Regardless of the length of the typeline (132 or 136 columns), thirty-four discrete constant current hammer drivers are contained on each of the four hammer driver boards used in any DPC 1200 Series printer.

Each board is dedicated exclusively to hammers of a single phase. Because all actuators in any given row on the frame assembly correspond to print hammers of the same phase, actuator cabling is straightforward as illustrated in Table 2-1.

The leads from all actuators in any given row terminate in a single plug that mates with double-sided tabs at the top edge of the hammer driver board dedicated to that phase (row). Plug, bay position, and phase numbering have been made consistent to minimize confusion when servicing these components.

It is impossible to remove a hammer driver board from the logic bay without first removing the actuator cabling plug attached to it at the top. When reinserting a hammer driver board, make sure it is securely seated so that a break in the series of hammer driver interlock connections (CD 5.0.1 "Hammer Driver Interconnection Wiring") will not generate an alarm. Remember, also, to reinsert the proper actuator cabling plug, which is keyed to prevent improper insertion.

TABLE 2-1

HAMMER ACTUATOR CABLING

PHASE	ACTUATOR ROW	COLUMN POSITIONS	PLUG	LOGIC BAY POSITION
Ø1	Upper Straight	1, 5, 9, 13 . . . 129, (133)	P-221	1
Ø2	Lower Straight	2, 6, 10, 14 . . . 130, (134)	P-222	2
Ø3	Upper Offset	3, 7, 11, 15 . . . 131, (135)	P-223	3
Ø4	Lower Offset	4, 8, 12, 16 . . . 132, (136)	P-224	4

2.3 RIBBONFEED MECHANISM

The Ribbonfeed Mechanism can be broken down into two major components: (1) a ribbon drive assembly (IPB 43-37) and its associated motor (IPB 43-34), which are mounted at the right, front side of the yoke; and (2) a ribbon sensing assembly (ipb 43-38), which is mounted at the left, front side of the yoke. These mechanisms automatially control the feeding, reversing, and skewing of mandrel-wound, towel-form ribbon over the faces of the upper and lower ribbon/slug guides.

2.3.1 Ribbonfeeding and Reversing

Ribbon drive direction is determined by upper and lower ribbon reversing dogs on the ribbon drive assembly. When the upper reversing dog is pushed forward by the ribbon reversing bar attached to the end of the ribbon fed from the upper mandrel, drive is supplied to the upper hub, and the lower hub is declutched. Ribbon is then wound on to the upper mandrel until the lower ribbon reversing bar pushes the lower reversing dog forward. When that happens, ribbon is fed in the opposite direction from the upper mandrel to the lower. The upper hub is declutched, and take-up drive is supplied to the lower mandrel. Ribbon drag in both the upper and lower mandrel hubs is adjustable

as explained in Section 3.5.3 of the Maintenance Instruction manual (DPC Form 1260/90/10-3). Two different ribbon drive assemblies are available according to the length of the typeline selected.

2.3.2 Ribbon Skewing

Ribbon is skewed back and forth across the typeline in order to maximize ribbon life. Skewing is controlled automatically by the ribbon sensing assembly. Whenever the left-hand edge of the ribbon trips the mechanical ribbon sensor, the skew position of the upper and lower left-hand mandrel hubs is changed causing ribbon to track in the opposite direction. This mechanism is not adjustable but does require careful, periodic cleaning as described in Section 3.5.3 of the Maintenance Instruction manual (DPC Form 1260/90/10-3).

2.4 PAPERFEED MECHANISM

Printout is recorded on standard fanfold, sprocket-fed, single- or multipart paper forms. Paper enters the printer at the front from an enclosed space directly below the yoke and exits the printer at the rear into a paper receptical (Figure 2-18). Paperfeeding is a microprocessor-controlled process that is accomplished by phase switching a stepper motor, which is coupled to pin-feed paper tractors, through the exact number of steps needed to advance paper to the next desired linespace. A single line advance at 6 LPI takes approximately 15 milliseconds in all models, however configured. Paper slewing occurs at the rate of 20 or 40 IPS depending on the model or option selected.

The Paperfeed Mechanism in all CT-1260, CT-1290, CT-1210 models consists of the following subsystems: (1) two pairs of motor-driven paper tractors (2.4.1); (2) a FORM TENSION Control (2.4.2); (3) a manually-switched, motorized tractor positioning system (2.4.3); (4) a retractable PAPER GUIDE/SCALE

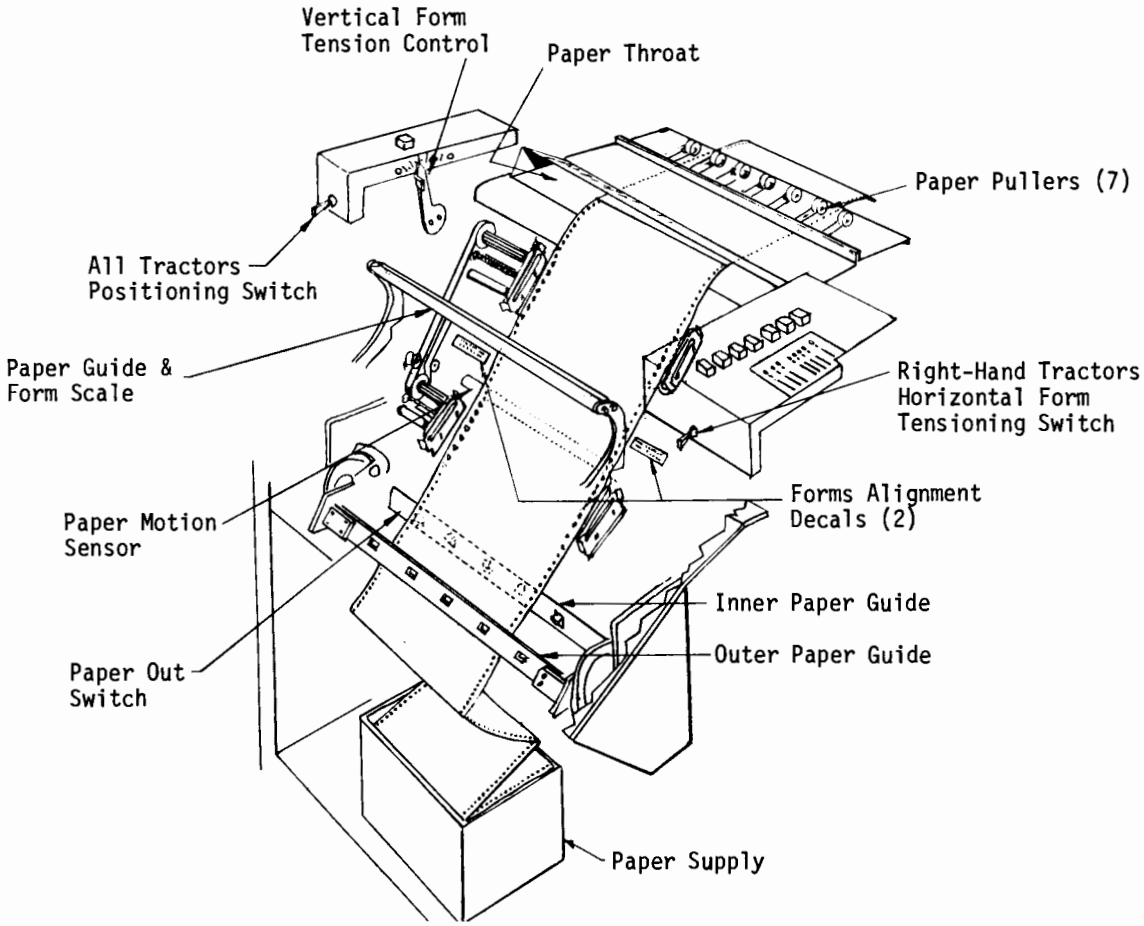


Figure 2-18. Paperfeed Path.

(2.4.4); (5) a DC stepper motor tractor drive system (2.4.5); (6) an INFINITE FORMS POSITION CONTROL (2.4.6); (7) a paper low switch (2.4.7); (8) a paper motion sensor (2.4.8); and (9) a paper receptical (2.4.9).

Individual printers in this series may also have the following: (1) a motor-driven paper puller (2.4.10); (2) a static eliminator (2.4.11); (3) an 8- or 12-channel Vertical Format Unit (VFU) punched tape reader (2.4.12), and (4) a 6/8 LPI switch, which permits operator selection of 6 or 8 LPI spacing (2.4.13).

Each component in the Paperfeed Mechanism will be dealt with in turn in the subsections indicated above.

2.4.1 Paper Tractors

Two pairs of motor-driven, pin-feed paper tractors--one pair of which is mounted above and the other below the hammer bank--hold paper stationary during printout and transport paper vertically during a paperfeed operation (Figure 2-19). Each pair consists of a left-hand (IPB 36 A/B) and a right-hand (IPB 37) tractor, both of which share a common tractor guide shaft and a common splined drive shaft (IPB 28, Dwg. 1 of 2). The upper and lower tractor drive shafts are coupled by means of upper and lower toothed pulleys and a timing belt. The four tractors are driven in tandem by way of an upper tractor drive pulley (IPB 34-7), which is located on the outside of the left-hand side frame assembly.

The upper and lower tractors use different tractor frame bushings (IPB 36-15/16 and 37-15/16) so that the bushing's 1/4-20 "tap thru's" and clearance holes will be properly aligned with the tractor positioning system lead screws. Except for the different bushings, the upper and lower right-hand tractors are identical in all printers in this series. The same is true of the upper and lower left-hand tractors except on CT-1260 printers, which have a paper low switch incorporated as an intergral part of the lower left-hand tractor assembly (IPB 36B).

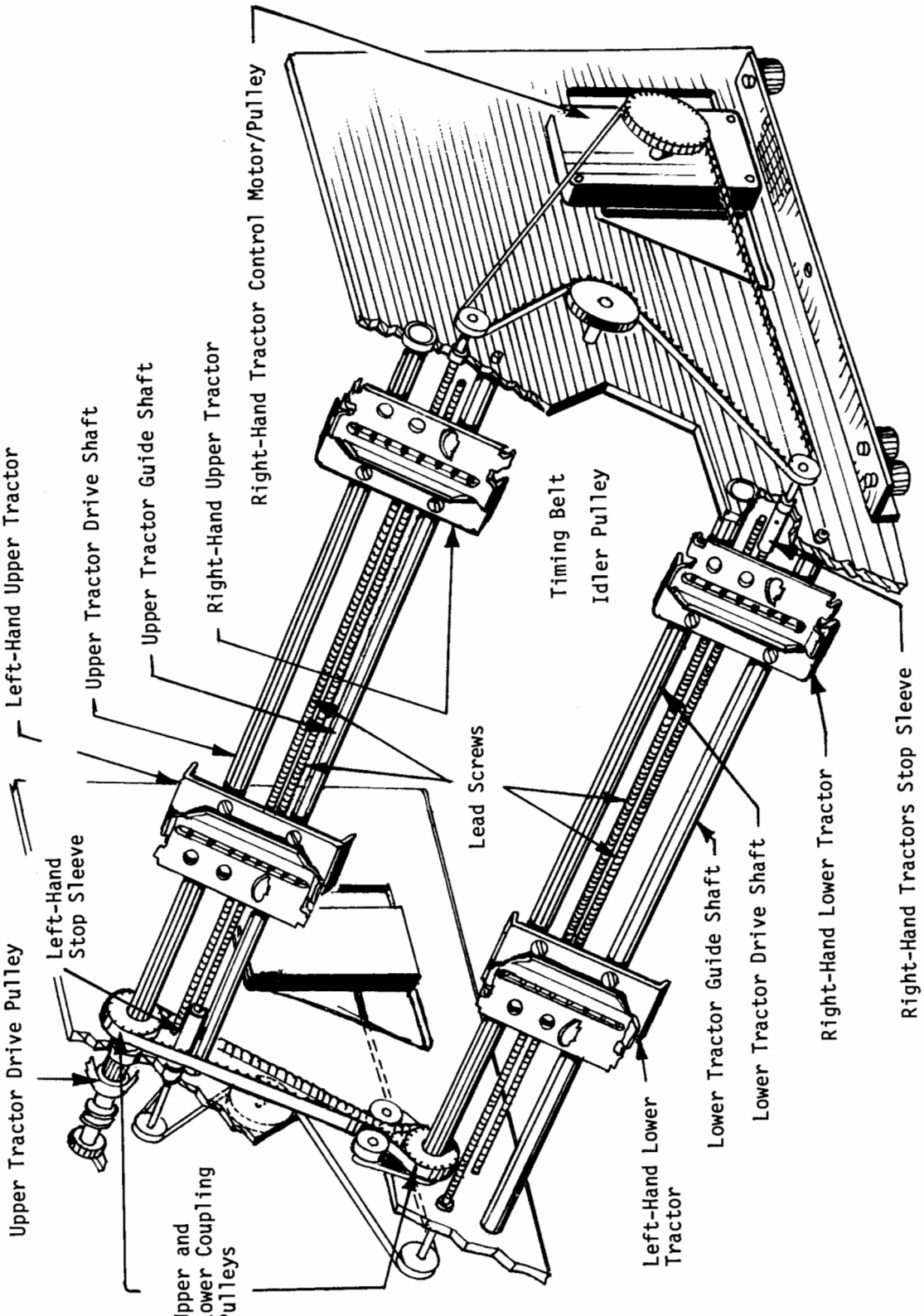


Figure 2-19. Paperfeed Tractors.

2.4.2 Vertical Form Tension Control

Vertical form tensioning is accomplished manually by means of an adjustable idler pulley/lever assembly that affects the position of the lower tractor drive shaft--and, thereby, the position of the lower tractor feed pins--relative to the stationary position of the upper tractor drive shaft and feed pins (Figure 2-20). The setting of the handle/pointer is retained by a detent mechanism located on the outside of the left-hand side frame assembly (IPB 29).

2.4.3 Tractor Positioning System

A manually switched, motor-driven lead screw tractor positioning system permits movement of all tractors in tandem, left or right, for forms positioning (margin set up) and movement of the upper and lower right-hand tractors, left or right, for horizontal forms tensioning (Figure 2-19).

The ALL TRACTORS switch turns on both the left- and right-hand tractor positioning motors simutaneously for forms positioning. The RIGHT-HAND TRACTORS switch turns on only the right-hand tractor motor for horizontal forms tensioning. The ALL TRACTORS switch ("S-111" on CD 12.0.1) is located in front, below the left-hand control panel. The RIGHT-HAND TRACTORS switch ("S-107" on CD 12.0.1) is located in front, below the right-hand control panel. Both are three-position, spring-loaded switches that return to a neutral center position (motors "off") when released. In order to prevent damage to the positioning system through operator error, the switches are wired so that the RIGHT-HAND TRACTORS switch is disabled whenever the ALL TRACTORS switch is toggled out of its neutral ("off") position.

The position of the upper and lower right-hand tractors is controlled by a right-hand tractor control motor ("B-104" on CD 12.0.2), mounted inside the right-hand side frame assembly (IPB 30-3). The motor drives the right-hand tractor positioning lead screws by means of toothed pulleys and a timing belt as shown in Figure 2-19. The position of the left-hand tractors is controlled in a similar way by a left-hand tractor control motor ("B-103" on CD

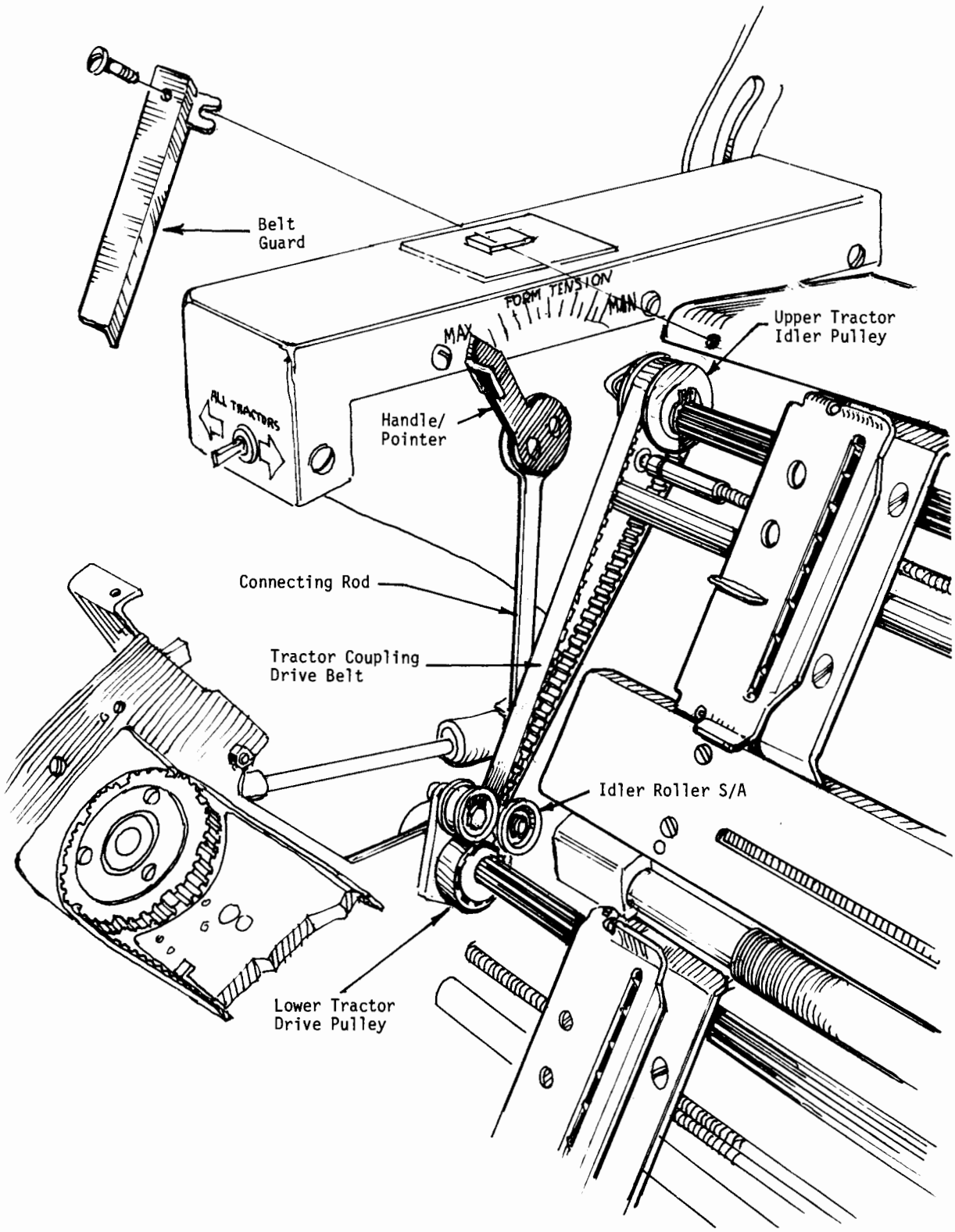


Figure 2-20. Vertical Form Tension Control.

12.0.1), mounted inside the left-hand side frame assembly (IPB 29-4).

Left- and right-hand tractor stop sleeves (Figure 2-19) prevent damage to components mounted inside either side frame assembly if an operator inadvertantly runs the tractors too far to the right or left. Running a tractor up against either stop sleeve produces an audible alarm that is the result of drive belt slippage on the lead screw drive pulleys. It may also cause misalignment of the upper and lower tractors on that side and should, therefore, be avoided. A similar alarm will be produced with similar results if the right- and left-hand tractors are run together.

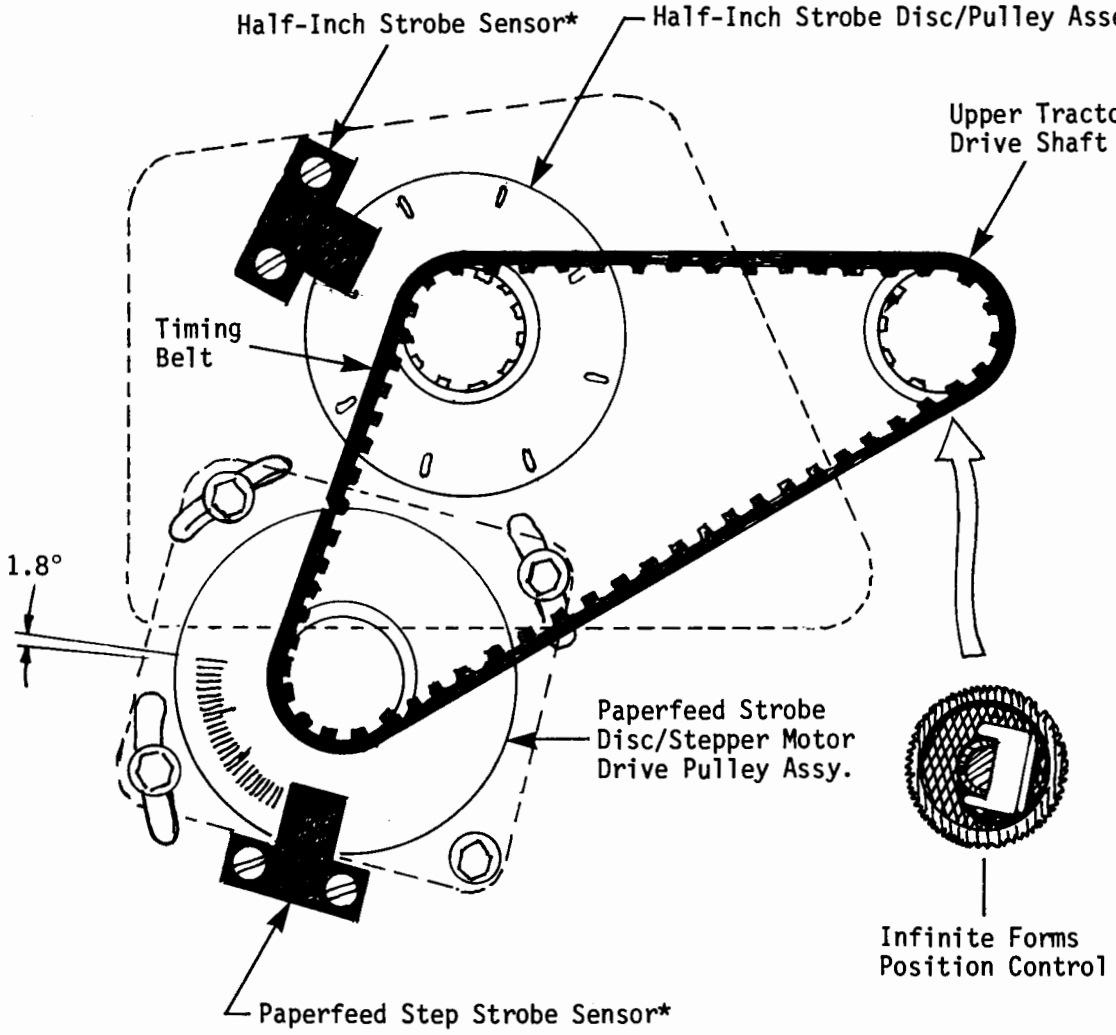
The tractors motors can be operated whenever "ON" is illuminated. After power-up, their operation takes place independently of the Control System.

2.4.4 Paper Guide/Scale

The retractable Paper Guide/Scale (IPB 43 and 48) serves three purposes. First, the forms scale cross members (IPB 48-3 and -4) prevent smudging by keeping paper from contacting the ribbon when the printer is idling or feeding paper. Second, the forms scale (IPB 48-17) that is mounted on the upper paper guide cross member allows the operator to properly position the left- and right-hand margins opposite the print hammers, which are obscured by the paper forms. The third purpose of the paper guide--one which is dealt with more fully in section 2.4.8. below--involves a presser foot (IPB 48-5) that is mounted on the left-hand side of the lower paper guide cross member. When the yoke is closed and latched, the spring fingers on the presser foot assure proper contact between the paper forms and a roller assembly that is part of the paper motion sensing mechanism.

2.4.5 Stepper Motor Tractor Drive System

Paperfeeding is accomplished by phase-switching a DC stepper motor, which is coupled to the tractors by way of the upper tractor drive pulley, through the number of steps required to move paper to the next desired linespace (Figure 2-21). The motor, which is driven by the Control System through com-



*NOTE

Careful adjustment of the Step Strobe and Half-Inch Strobe sensors is essential for proper operation. These adjustments are described in detail in sections 3.5.2.3.3. and 3.5.2.4 of the Maintenance Instructions manual (DPC Form 1260/90/10-2).

Figure 2-21. Stepper Motor Tractor Drive System.

mands sent to the Paperfeed Stepper Drive Board (CD 4.0.0), is moved in discrete steps of 1.8^{0} by progressively switching pairs of its four phase windings. Two hundred steps are needed for one revolution (1.8^{0} x 200 = 360^{0}).

The motor-to-tractor gear ratio is such that 48 steps are required to move paper through a distance of one inch. Thus, when the printer is configured to transport paper at 6 LPI, movement of one line requires 8 steps; conversely, when the printer is configured to transport paper at 8 LPI, movement of one line requires 6 steps.

To make paper slewing possible, the stepper motor is operated in a closed-loop fashion with step strobe pulses ("(-) PF STB" on CD 7.0.0 and 3.2.0) being returned to the Control System by means of a timing disc attached to the stepper motor shaft (Figure 2-21). These pulses force-feed the Control System the positional data needed to accurately control the Paperfeed Mechanism. Thus, the commutation of the pairs of motor windings--which is timed to lead the actual shaft position by variable amounts as the mechanism is accelerated and decelerated during a paper slew operation--can be performed in perfect synchronism with the rotating motor shaft.

High speed slew (40 IPS, rather than 20 IPS) is accomplished by the Control System program forcing the mechanism to take an extra step during acceleration and, then, skipping one step during deceleration.

A half-inch strobe ("(-) 1/2 IN STB" on CD 7.0.0 and 3.3.0) is generated once every 24 steps by means of a half-inch strobe disc and its associated optical sensor as shown in Figure 2-21. Half-inch strobe pulses are used during system initialization to establish a starting Top of Form (TOF) position and, thereafter, to validate positioning of the mechanism.

In addition to transporting paper vertically during a line-feed or slew operation, the paperfeed stepper motor performs a second important tasks: it holds paper stationary while printing takes place and while the machine is idling. The Control System accomplishes this automatically whenever at ther end of a feed operation it removes "INC I (+)" from the Paperfeed Stepper

Drive Board (CD 4.0.0). When "INC I (+)" is removed, a chopper circuit on that board applies a reduced power level to the last pair of windings energized during the preceding paperfeed operation.

2.4.6 Infinite Forms Position Control

Alignment of the actual top line of the paper form with the nominal Top-of-Form (TOF) position set up and held stationary by the Control System is accomplished by means of the INFINITE FORMS POSITION CONTROL (IPB 34). This control makes it possible to declutch the upper tractor drive shaft from the stepper motor drive system so that the vertical position of the paper forms can be adjusted independently of the holding position of the stepper motor. Pulling out the cam lever releases the pressure exerted on the upper tractor drive pulley by the inner and outer cones (IPB 34-3 and -10) making it possible to move paper up or down without disturbing the holding position of the stepper motor. Forms alignment decals on the paper platen (IPB 38-3), which show the position of the typeline relative to the left- and right-hand margins on the paper forms, permit operators to accurately align the actual paper TOF with the nominal TOF position of the printer mechanism.

2.4.7 Paper Low Switch (CD 7.0.0)

As already noted, the paper low switch is an integral part of the lower left-hand tractor on CT-1260 printers (IPB 36B). Normally open, the switch is closed whenever paper is installed in the tractor and the pressure plate is closed. The switch will open again when the bottom of the last remaining form passes through, releasing the switch button. This occurs on CT-1260 printers when 6.5 inches of the last form remains in the printer.

The paper low switch used in CT-1290 and CT-1210 printers operates in a similar way. Located in the paper throat gap (IPB 28), it generates a paper low signal when 3.5 inches of the last form remains in the printer. Normally open, the switch closes whenever paper is installed between the inner and outer paper guides and the yoke is closed and latched. The outer paper guide presses paper against five sensing fingers that protrude through corresponding

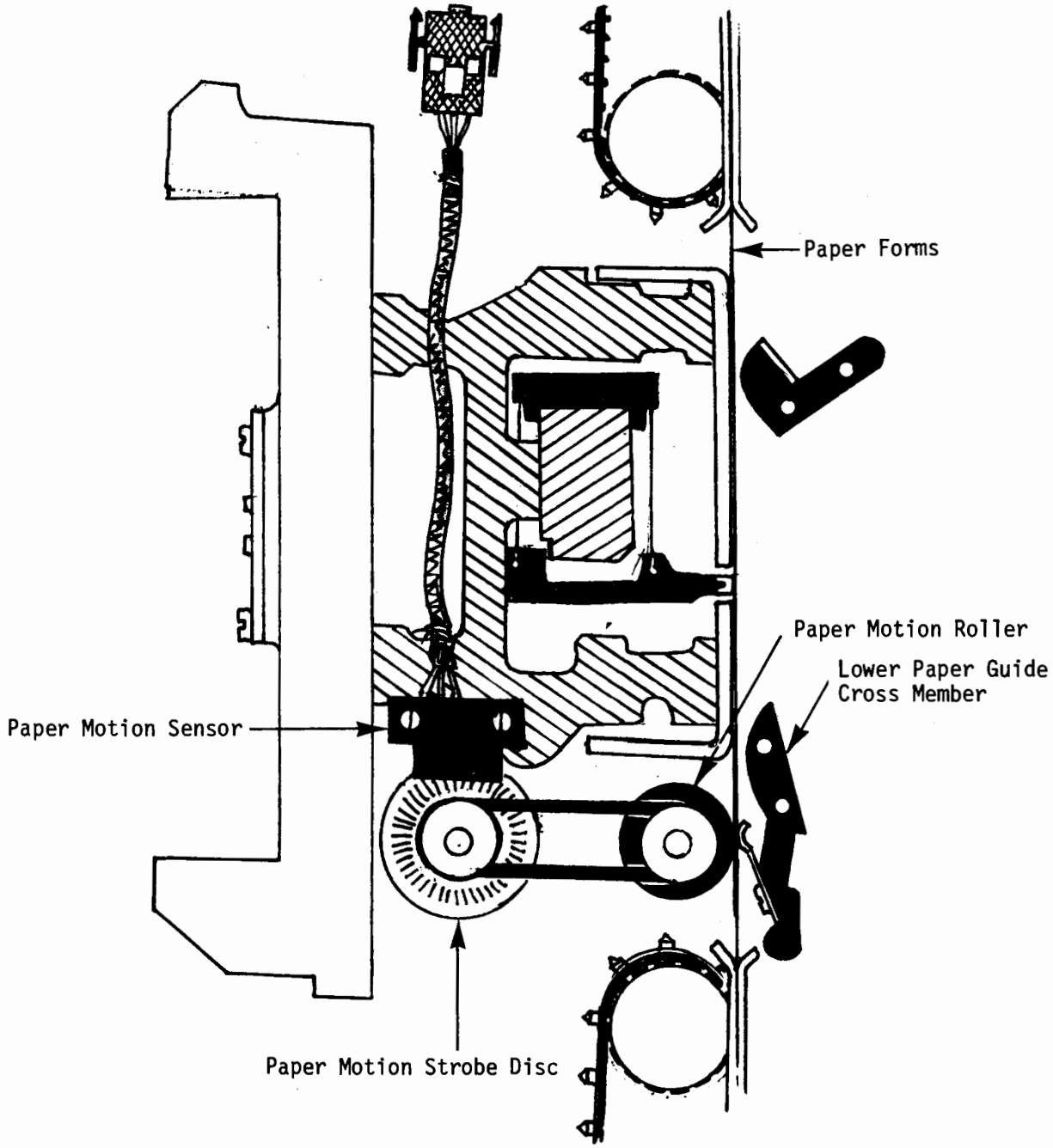
slots in the inner paper guide. The fingers cause the pivot bar on which they are mounted to rotate, which in turn causes the paper low switch set screw in the contact arm at the left-hand end of the pivot bar to close the paper low switch. When the bottom of the last remaining form passes through the throat gap, the sensing fingers pass through the corresponding slots in both the inner and outer paper guides, opening the switch and generating a paper low signal ("(-)PAPER LOW" on CD 1.4.1).

The paper low switch, regardless of model, interfaces with the Control System as shown on CD 7.0.0, 0.1.1, 1.4.1, 1.2.0, and 3.3.0. When the switch opens, IC-12A on CD 1.4.1 generates "(-) PAPER LOW", which turns on "PAPER LOW" on the right-hand control panel. At the same time, IC-11A generates "(-) PAPER LOW", which is sent to "DI-5" of input port 12 to the external device (via IC-6A on CD 1.2.0) as "(+) PAPER LOW". When feeding paper, the Control System polls input port 12 for "(-) PAPER LOW" once every line. When it finds "(-) PAPER LOW", it allows printing and feeding to continue for an additional 5-inches (CT-1260) or 7-inches (CT-1290 and CT-1210) before looking for TOF. When it finds TOF it illuminates "STOP," "ALARM," and "PAPER OUT," and it refuses to permit operation in the RUN Mode until "PAPER LOW" is cleared by loading more paper forms.

2.4.8 Paper Motion Sensor

The paper motion sensor is mounted on the hammer bank as shown in IPB 42. It consists of a roller and associated drive pulley that is coupled to a paper motion disc by means of an O-ring drive belt. When the yoke is closed, paper is pressed against the paper motion roller by means of the presser foot on the lower paper guide cross member, which causes paper motion to be transmitted to the paper motion strobe disc (Figure 2-22).

The disc rotates with paper motion and interrupts the light path in the paper motion optoelectrical sensor (CD 7.0.0). The first slot-to-no-slot transition produces a positive edge that triggers the paper motion latch ("IC-40A") on CD 3.3.0. The latch responds by making a "logical 1" available to "DI-8" of input port 12, thus, indicating that paper motion has occured.



(Left-Hand Side View)

Figure 2-22. Paper Motion Sensor

At the end of every paperfeed operation (be it merely a single line advance of a slew-to-channel feed), the Control System polls input port 12 to verify that paper motion has occured. If a "logical 1" is not present at "DI-8", the Control System will illuminate "PAPER JAM", "STOP," and "ALARM" on the right-hand control panel and take the printer off-line. The jam must be corrected and the reset switch (ALARM) depressed to return the printer to normal operation.

When a paper low occurs it "fakes" a paper motion signal in order to permit the last form to be printed even though no paper motion signal can be generated once the tail end of the last form gets past the paper motion roller. It does this by using "(-) PAPER LOW" to hold the paper motion latch ("IC-40A" on CD 3.3.0) in the set state so that the Control System will think that paper motion has occured.

2.4.9 Paper Receptical

Two types of paper recepticals are used on DPC 1200 Series printers. The first type, a simple paper basket (IPB 1), is standard equipment on CT-1260 and not available on the others. The second, a paper catcher (IPB 2), is standard on CT-1290 and CT-1210 and optional on the CT-1260. Both are equipped with a ground cord, which must be inserted into the jack at the lower left rear of the printer to prevent stacking problems due to static build up

2.4.10 Paper Puller

A motor-driven paper puller is required standard equipment on CT-1210 models and optional on CT-1260 and CT-1290 models unless they are programmed for the optional 40 IPS slew speed, in which case a paper puller is required. The paper puller consists of a pressure roller assembly (IPB 60) and a corresponding drive roller assembly (IPB 61) that are located near the paper exit point on the main platen assembly (IPB 59) at the top, rear of the machine. The drive roller is coupled to a small AC motor (IPB 33) by means of pulleys and a timing belt. The paper puller motor is turned on whenever "ON" is illuminated (CD 12.0.2).

The paper puller will not affect print quality when the printer is holding paper stationary because friction drive is applied to the non-print side of the paper. This mechanism is adjustable and may require periodic service as described in Section 3.5.2.8 of the Maintenance Instructions manual (DPC Form 1260/90/10-3).

2.4.11 Static Eliminator

Available as an option on all models, an air-ioizing static eliminator is recommended whenever the printers are operated in a dry environment (IPB Option). It consists of a lugged static bar and an accompanying HV trans former capable of delivering 7 KV RMS to the bar. The lugs on the bar leak a charge to the paper, which eliminates paper drag due to static build up. The static bar should be cleaned weekly as instructed in Table 3-7 in the Maintenance Instruction manual (DPC 1260/90/10-3).

CAUTION

Before attempting to clean the lugged static eliminator bar, ALWAYS (1) turn off the Primary Circuit Breaker and (2) unscrew and disconnect the HV cable at the static eliminator transformer.

2.4.12 Vertical Format Units

Vertical formatting data can be entered locally by means of an 8-Channel (standard) or 12-Channel (optional) VFU punched tape reader, shown in IPB 26 and 27, respectively. Punched tape is advanced and read one line at a time by means of a sprocket coupled to the Half-Inch Strobe Disc/Pulley (IPB 26-18 and IPB 27-2/3). The holes punched in the tape are sensed by a multi-channel photoelectric sensor (IPB 26-4 and IPB 27-5), which interfaces with the Control System as shown on CD 7.0.0 and 3.3.0.

2.4.13 Optional 6/8 LPI Switch

An option 6/8 LPI Switch is available on all machines not having an 8-Channel VFU. Data from the switch is read at Input Port 12 (CD 3.3.0) whenever the printer enters the Stop Mode. Changing the position when the printer is operating in the Run Mode is of no consequence until STOP is depressed.

CHAPTER 3
CONTROL SYSTEM OPERATION

3.1 INTRODUCTION

The Control System includes all drive, control, and interface circuitry, power supplies and power-sequencing circuitry, and all sensors, switches, and indicators needed to make the Print System perform its printing and paper-feeding tasks in both the Local and Remote Modes of operation. It consists of the components shown on CD 7.0.0, which are distributed throughout the printer, and two major subassemblies mounted in the Main Frame: (1) a Logic Bay Assembly (IPB 15-1), which contains eight circuit boards plugged into a Mother Board; and (2) a Power Supply and Capacitor Bank Assembly (IPB 15-2), which contains two power supplies ("T1" and "T2" on CD 11.0.1) and a Power Control Board (CD 6.0.0).* The operation and interaction of these components is examined in this chapter.

3.2 CONTROL SYSTEM ARCHITECTURE

The basic function of any printer's control circuitry is the maintenance of two-way communication with an operator, an external device, and the various printer mechanisms in such a way that correct hardcopy printout gets produced. The way this goal is reached by the microprocessor-based Control System used in CT-1260, CT-1290, and CT-1210 printers is illustrated by Figure 3-1.

The Control System can be divided into two subsystems that operate in parallel: (1) a Power-Sequencer, which is powered-up by turning on the Primary Circuit Breaker at the rear of the printer; and (2) a Microprocessor-Controller, which is powered-up and allowed to continue operation only if the Power-Sequencer determines that certain basic operating conditions are fulfilled.

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*CT-1260 printers do not use a capacitor bank.

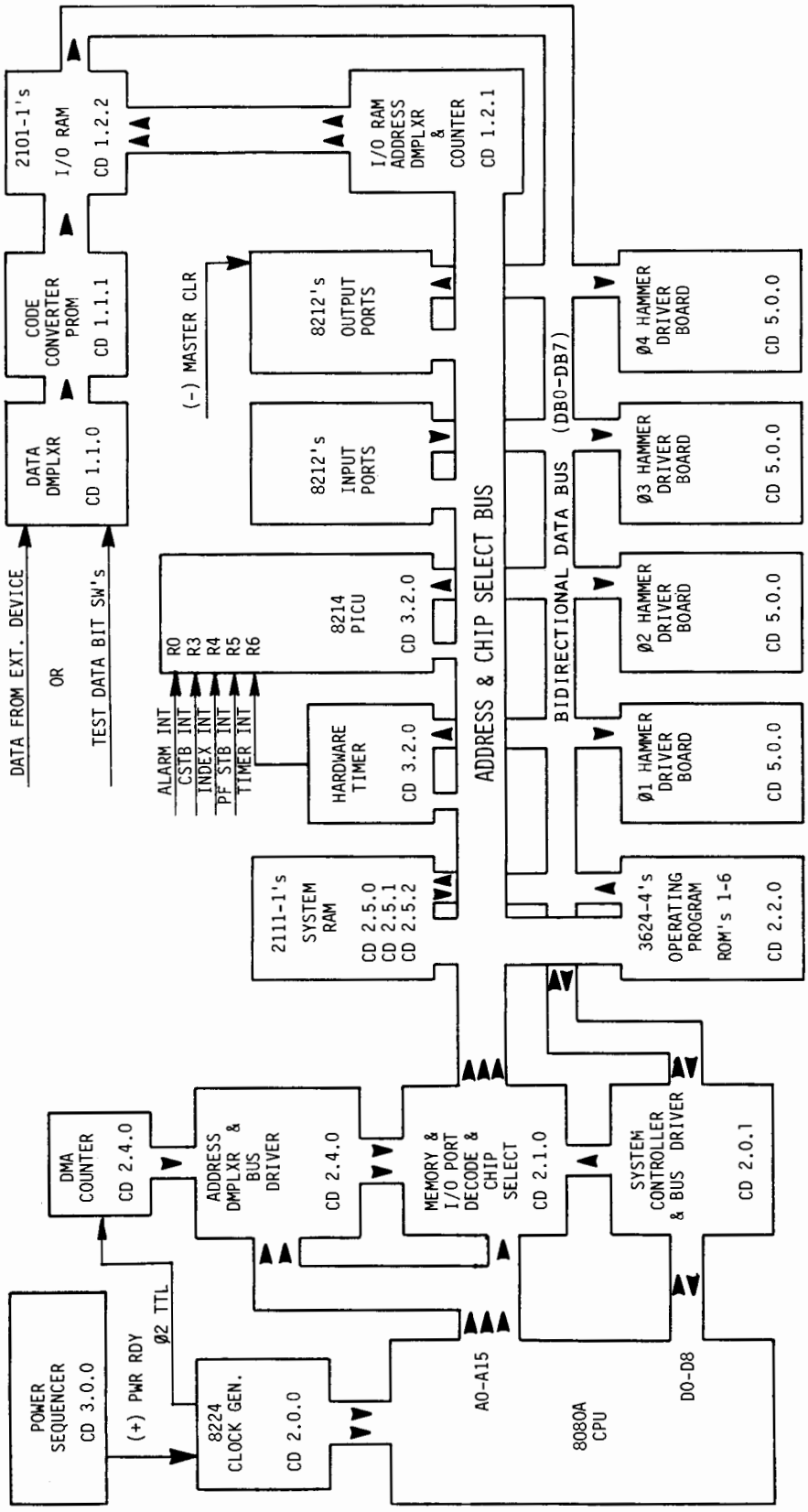


Figure 3-1. System Architecture - DPC Models CT-1260, CT-1290, and CT-1210.

The ability to illuminate and extinguish the "ON" and "OFF" indicators and to monitor the ON and OFF switches on the right-hand control panel resides exclusively with the Power-Sequencer. When ON is depressed, the Power-Sequencer starts a cycle counter; turns on a triac that powers up the transformer that supplies all necessary voltages to run the Microprocessor-Controller and the Print System mechanisms; clears the Output Ports to prevent the generation of erroneous signals; resets the 8080A CPU's Program Counter to 0000_{hex} so program execution will start at the beginning of ROM 1; and, finally, if all necessary voltages come up as expected, generates "POWER READY (+)" when the cycle counter times out, thereby permitting the CPU to begin program execution.

Thereafter, the CPU becomes the focal point of a complex network of two-way communication with the operator, the external device, the various Print System mechanisms, and hardware within the Control System itself. While all this is happening, however, the Power-Sequencer continues to monitor critical supply voltages and the OFF switch. If a voltage is lost or if OFF is depressed, the sequencer will turn off T-2 shutting down the Microprocessor-Controller; extinguish "ON" and illuminate "OFF"; and revert to waiting for the ON switch to be depressed - all quite independently of the Microprocessor-Controller. Although the latter is the more sophisticated of the two subsystems, it is the more primitive Power-Sequencer that takes over when there is trouble. "$\overline{\text{RUN}}$" provides the external device with a foolproof indication that the printer is off-line should a power-down sequence occur (CD 1.4.0).

As Figure 3-1 shows, the Microprocessor-Controller is a fairly typical 8080A microcomputer system with some unique hardware (CD 1.X.X and 5.0.0) hung on the data and address busses. Sustained by timing pulses originating in an 8224 "Clock Generator" and told what to do by an operating program contained in ROM, the 8080A CPU directs its complex network of two-way communication by means of (1) 8212's configured as Input Ports, (2) 8212's configured as Output Ports, (3) an 8214 "Priority Interrupt Control Unit" (or PICU), and (4) DMA counter circuitry. Constantly up-dated data needed for proper printer operation are stored temporarily in RAM on the CPU Board. Ports, PICU, ROM, and RAM are

tied to the CPU by a common unidirectional address buss and a common bidirectional data buss. DMA control of the address buss is provided to make it possible to load data from RAM on the CPU Board into the four Hammer Driver Boards (CD 5.0.0) at a high rate of speed. High speed data load from the external device is conducted independently of CPU operation by means of address demultiplexing and counting hardware on the I/O Board.

3.3 CONTROL SYSTEM OPERATING PROGRAM

The Control System operating program is contained in seven ROM's located on the CPU Board (CD 2.2.0). They are as follows:

3.3.1 ROM #1 - Initialization

This ROM stores the Initialization program, which tests all RAM, the hardware timer, and the stepper motor and checksums the seven ROM's. Any error during initialization will result in an appropriate diagnostic. The ROM also contains hard vectors for the five interrupts impinging on the PICU. Some of these vectors send the CPU to soft vectors in RAM, which can be changed whenever deemed appropriate by the program. Successful execution of the Initialization program leaves all RAM on the CPU Board cleared to 00hex, all RAM on the I/O Board cleared to FFhex, and the stepper motor initialized to a 1/2"-Strobe position. Program execution continues on into ROM 2.

3.3.2 ROM #2 - Control Loop

This ROM stores the Control Loop program, which polls various conditions such as alarms, switch status, I/O load completion, and chain movement. Because it contains loops for operation in the Run and Stop Modes, this ROM is the pivot point of all printer operation. The program contained in this ROM calls the Print Cycle subroutine in ROM 3, the Paperfeed Cycle subroutine in ROM 4, and the VF Sample and External Format Load subroutines in ROM 5. It also initiates data loads into the I/O RAM buffer in both Local and Remote, determines when the load operation is complete and what kind of data was loaded, and behaves accordingly by calling the appropriate subroutine in ROM 3, 4, or 5.

3.3.3 ROM #3 - Print Cycle

This ROM contains the Print Cycle subroutine, which loads a Matrix Memory in RAM on the CPU Board with hammer firing position data and, then, initiates a series of DMA Hammer Driver Board load and fire operations that cause the data loaded into the I/O RAM buffer to be printed out. Successful execution of the subroutine contained in this ROM (no diagnostics) results in a RETURN to the Control Loop at the next instruction following the CALL that initially sent the CPU to ROM 3.

3.3.4 ROM #4 - Paperfeed

This ROM contains the Paperfeed Cycle subroutine, which causes paper to be advanced according to the dictates of a paperfeed code and the setting of the 6/8 LPI switch (if this option is present). All paperfeed, whether the result of a code for linefeed or slew-to-channel or the result of the external device raising Autolinefeed, is by line count. The program determines when to accelerate paper movement, when to level off, and when to decelerate to stop according to the initial line count and data stored in a Lines Left Register in RAM on the CPU Board.

3.3.5 ROM #5 - VF Sample

This ROM contains two subroutines, one of which is called from ROM 2 when the program is looping in the Stop Mode and the other of which is called from ROM 2 (when appropriate) when the program is looping in the Run/Remote Mode. "VF Sample" is called when in Stop to permit VF data to be loaded from tape if no VF data had been loaded previously from the external device. If VF data is already loaded it does some paper low housekeeping and gives the operator a crack at operating the HOME and ONE LINE switches before returning to ROM 2.

3.3.6 ROM #6 - Paperfeed Interrupts

This ROM contains the Paperfeed Interrupt subroutines used by the Paperfeed Cycle subroutine in ROM 4. It contains a table for setting the hardware timer (CD 3.2.0) for paperfeed acceleration, slew, and deceleration to stop. ROM's 4 and 6 work together during paperfeed. ROM 6 controls the time between steps and ROM 4 counts the steps.

3.3.7 ROM #7 - VF Tape Read Check

This ROM contains a Check Load subroutine, which is called by the VF Sample subroutine in ROM 5 to verify the accuracy of a tape load from the VFU. An option, this ROM is called only if present.

Appendix A contains flow charts of a typical seven-ROM operating program that can be used in any of the three models dealt with in this manual.

3.4 INPUT/OUTPUT BOARD

To maintain the 500 kHz input data rate established by earlier designs, the RAM Buffer on the "I/O Board" is configured with separate input and output data lines and multiplexed address lines so that a complete line of print data can be loaded at the necessary speed without interference from the slower parts of the systems. A front end Code Converter ROM, which is addressed by the incoming data, is used to convert print data into printer-compatible "chain code" that is loaded into the RAM Buffer. A modest amount of TTL circuitry is used to control the transfer of data from the external device to the RAM Buffer and to reflect the status of the printer to the external device within the specifications of earlier designs.

While data is being loaded at high speed, the CPU goes about its business doing other things, one of which is to repeatedly check an Input Port that tells the CPU when the load operation is complete. Once it senses load completion, the CPU is free to process data in the RAM Buffer under direction of the Control System program.

3.5 RANDOM ACCESS MEMORY (RAM)

The Random Access Memory (RAM) is divided into several domains. Each domain may be individually addressed for both reading and writing by the 8080A. The domains are as follows: Stack, VF (Vertical Format), Scratch Pad, Matrix, and Matrix Extend.

The Stack is used to temporarily store the address of the next instruction and/or the contents of certain registers when the program is diverted to a special routine such as a CALL or INTERRUPT. When the particular routine is complete, the program address and other information is retrieved from the Stack and the program continues where it previously left off.

The VF Memory stores data read from the VFU tape, or vertical format information transmitted directly from an external source over the signal data lines. This data is used in the Paperfeed Cycle.

The Scratch Pad Memory is used to temporarily store changeable information such as interrupt vectors and chain position data.

The Matrix and Matrix Extend Memories store hammer firing position information. After the line buffer has been loaded with print data, a virtual image of print hammer firing times for a full line of print is constructed in the data memory. This memory takes on the aspects of a matrix, with single bit coordinates for each chaintrain position encountered at each print position during the complete print cycle. The duration of a print cycle is then the amount of time it takes to present each different character in the font to each print position (column), and is independent of the particular data to be printed.

The matrix is constructed by sequentially processing print data in the line buffer memory after a data transmission has been completed. Data for each column is read, and the chaintrain position at which time the associated print hammer is to be fired is determined from the binary encoded data, the known font size, and the column location. This calculated chaintrain position

is used to address a corresponding bit in the matrix memory, which is then set true. When all print data has been processed, matrix construction is complete, and the control system prepares to initiate actual printing. During this time chaintrain velocity and position have been tracked by character strobe and head-of-font interrupts to the control system. The font size was determined by counting character strobes between successive index interrupts, and the resultant value was stored in data memory for reference. If the control system determines that printing is to commence, but the chaintrain and ribbon motors are off, these motors are directed to turn on. A chaintrain initialization sequence determines when the chaintrain has reached operational velocity, and ensures that all font characteristics are valid.

At the onset of actual printing, the chaintrain position is used as an address to the matrix memory, and the 132 bits corresponding to this position are DMA'd into the four hammer driver modules (printed circuit board #42020), each module handling one phase of the print system. Then the control system sequentially generates fire commands to each of the four modules, starting with phase 1. The firing sequence is initiated by a character strobe interrupt, which defines the exact chaintrain position, and timing delays between hammer fire commands are calculated by referencing the previously determined chaintrain velocity. These velocity figures are updated at the onset of each successive character strobe, and the loading of hammer driver modules from the matrix memory and subsequent hammer firing continues for each successive chaintrain position until the entire font has been presented to each print position. Printing continues line after line in this manner, interspersed with the required linefeeding and formatting.

3.6 INPUT PORTS

Data is recovered from an Input Port whenever the CPU encounters an input instruction in the Control System program. The input instruction, which always specifies a particular port, causes the CPU to address that port and get ready to store data from it in the Accumulator. When addressed, the Input

Port latches data coming into it via electrical or optoelectrical Translators (TR's) and sends that data to the Accumulator for use during a subsequent program instruction. (See Table 3-1.)

3.7 PRIORITY INTERRUPT CONTROL UNIT (PICU)

Unlike the Input ports, which mutely wait to be polled, the PICU force-feeds information to the CPU whenever an enabled interrupt becomes active. When this occurs, the PICU causes the CPU to suspend current program execution (as soon as any instruction in progress is processed) and, also, outputs an interrupt-specific address vector via an Input Port, which the CPU fetches in order to branch to an appropriate interrupt service routine located elsewhere in ROM. Thus, interrupts force program execution - and, thereby, printer operation - to conform to the rhythm of real time mechanical and electrical activity. Without the PICU, microprocessor control of a high speed line printer would not be possible.

Chief among the functions of the PICU is that of assigning priority to simultaneous interrupts so the interrupt having the highest priority is serviced first. Another important function is that of allowing all or some of the interrupts to be disabled when directed by the Control System program so they have no effect on the operation of the CPU. Thus, however forceful, interrupts can only operate at the discretion of the Control System program. Once an interrupt is serviced and no other enabled interrupt is pending, normal program execution resumes wherever it left off.

3.8 OUTPUT PORTS

Communicating in the opposite direction, the CPU sends data to an Output Port whenever it encounters an output instruction in the Control System program. The output instruction, which always specifies a particular port, causes the CPU to output data in its Accumulator to the system data bus and then addresses the specified port. When addressed, the Output Port latches the data on the bus and presents it to electrical or optoelectrical Translators (TR's) that actually cause the program directives to be carried out. (See Table 3-2.)

TABLE 3-1
Input Ports

PORT	IN 11	IN 12	IN 13	IN "INTA"
DWG. REF	CD 3.3.0, IC-34	CD 3.3.0, IC-30	CD 3.3.0, IC-25	CD 3.2.0, IC-20
MD	GND	GND	GND	GND
STB	Vg	Vg	Vg	PICU INT (+)
$\overline{INT}$	N/C	N/C	N/C	(-) INTERRUPT
$\overline{CLR}$	Vg	Vg	Vg	Vcc
DB_1	VFU CHANNEL 1 (+)	VFU CHANNEL 9 (+)	(-) HOME SW	Vcc
DB_2	VFU CHANNEL 2 (+)	VFU CHANNEL 10 (+)	(-) ONE LINE SW	Vcc
DB_3	VFU CHANNEL 3 (+)	VFU CHANNEL 11 (+)	(-) LOAD TAPE SW	Vcc
DB_4	VFU CHANNEL 4 (+)	VFU CHANNEL 12 (+)	INC I (+)	(-) PA_0
DB_5	VFU CHANNEL 5 (+)	(-) PAPER LOW	(-) VF PGM MD SW	(-) PA_1
DB_6	VFU CHANNEL 6 (+)	(-) ½" STROBE	(-) RUN	(-) PA_2
DB_7	VFU CHANNEL 7 (+)	(+)6/(-)8 LPI SW	Vcc	Vcc
DB_8	VFU CHANNEL 8 (+)	(-) PAP MOTION STB	INC I DELAY (+)	Vcc

PORT	IN 21	IN 22	IN 23	
DWG. REF	CD 1.2.0, IC-23	CD 1.3.0, IC-20	CD 1.3.0, IC-24	
MD	GND	GND	GND	
STB	Vgb	Vgb	Vgb	
$\overline{INT}$	N/C	N/C	N/C	
$\overline{CLR}$	Vgb	Vgb	Vgb	
DB_1	PRINT LOAD (+)	(-) REM/LOC (+)	Vcc *	
DB_2	FORMAT LOAD (+)	(-) PF/SS (+)	Vcc	
DB_3	PF LOAD (+)	(-)SOLID/RIPPLE(+)	Vcc	
DB_4	LOAD COMPLETE (+)	PRINT INH SW (+)	Vcc	
DB_5	(-) INH FMT CMND	FIRST CHAR SW (+)	Vcc	
DB_6	AUTOLINEFEED (+)	FBP SW (+)	Vcc	
DB_7	DOUBLE SPACE (+)	(-) LS/HS (+)	Vcc	
DB_8	(-) CLEAR	EXTENDED FONT (=)	Vcc	

*DB_1 of Input Port 23 is jumpered to DC RTN to select the optional 192 line VF Memory

TABLE 3-2
Output Ports

PORT	OUT 10	OUT 20	OUT 40	OUT 41
DWG. REF	CD 2.3.0, IC-3	CD 2.4.0, IC-35	CD 2.3.0, IC-2	CD 1.4.0, IC-10
MD	Vg	Vg	Vg	Vg
STB	GND	GND	GND	GND
$\overline{INT}$	N/C	(-) CLR CHAIN INT	N/C	N/C
$\overline{CLR}$	(-) MASTER CLR & (-) COUNT 17	(-) COUNT 17	(-) MASTER CLR	(-) MASTER CLR
DB_1	N/C	AB_0	Ø4 FIRE PULSE (+)	REMOTE RDY (+)
DB_2	HOLD REQUEST (+)	AB_1	Ø3 FIRE PULSE (+)	PRINTER RDY (+)
DB_3	N/C	AB_2	Ø2 FIRE PULSE (+)	1st CHAR LD (+)
DB_4	DIAG. LED #1	AB_3	Ø1 FIRE PULSE (+)	TEST LD (+)
DB_5	DIAG. LED #2	AB_4	N/C	CLR T MEM (+)
DB_6	DIAG. LED #3	AB_5	N/C	N/C
DB_7	DIAG. LED #4	AB_6	N/C	RUN REMOTE (+)
DB_8	DIAG. LED #5	AB_7	N/C	[EN OUT 42, DO_{1-4}]

PORT	OUT 42	OUT 43	OUT 82	
DWG. REF	CD 1.4.0, IC-5	CD 1.3.0, IC-15	CD 3.3.1, IC-14	
MD	Vga	Vga	Vg	
STB	GND	GND	GND	
$\overline{INT}$	N/C	N/C	N/C	
$\overline{CLR}$	(-) MASTER CLR	(-) MASTER CLR	(-) MASTER CLR	
DB_1	[$\overline{LINESTROBE}$]	PF ØA (+)	IND RUN (+)	
DB_2	[$\overline{CHANNEL\ 1}$]	PF ØB (+)	IND STOP (+)	
DB_3	[$\overline{CHANNEL\ 2}$]	INC I (+)	IND ALARM (+)	
DB_4	[$\overline{CHANNEL\ 8/12}$]	N/C	CHAIN MTR ON (+)	
DB_5	IND RUNAWAY (+)	N/C	RIBBON MTR ON (+)	
DB_6	IND JAM (+)	N/C	(-)"CLR HD (+)"	
DB_7	IND PAPER OUT (+)	N/C	(-) PRINT INHIBIT	
DB_8	IND LOAD TAPE (+)	IND CALL SERV (+)	(-) SET STOP LATCH	

3.9 DIRECT MEMORY ACCESS (DMA)

Direct Memory Access (DMA) is the reading or writing of data to or from memory with the 8080A in a HOLD state. The Bidirectional Bus Drivers are put into their high impedance state to isolate the 8080A from the system bus.

DMA is necessary when the 8080A cannot perform a certain memory function fast enough. In printer operation, DMA is used principally to transfer data from the Matrix Memory to the Hammer Driver Boards during a Print Cycle.

A DMA Counter supplies the necessary controls and addresses to transfer the data by means of the system bus. When the transfer is complete, the HOLD is removed from the 8080A and it continues operation with the next instruction.

3.10 PAPERFEED CYCLE

The 8080 addresses Port 43 and changes the outputs of A and B by means of the System Bus, as shown in Figure 3-2.

This change is decoded by the Stepper Motor Drive logic to select the next pair of phase windings to the Stepper Motor.

The Stepper Motor and Line Count Disc turn in unison. When the Stepper Motor turns one increment, a PF STB is generated.

PF STB is directed to the Priority Interrupt Control Unit (PICU) where it generates INT and is encoded to a "vector" (A0, A1, A2).

INT clocks the vector into the latches of the Interrupt Input Port.

INT signals the 8080 that there is an interrupt request.

When the 8080 is free to service the interrupt, it sends an INTA (Interrupt acknowledge) signal to the Interrupt Input Port. INTA selects this port and gates the interrupt vector on the System Bus.

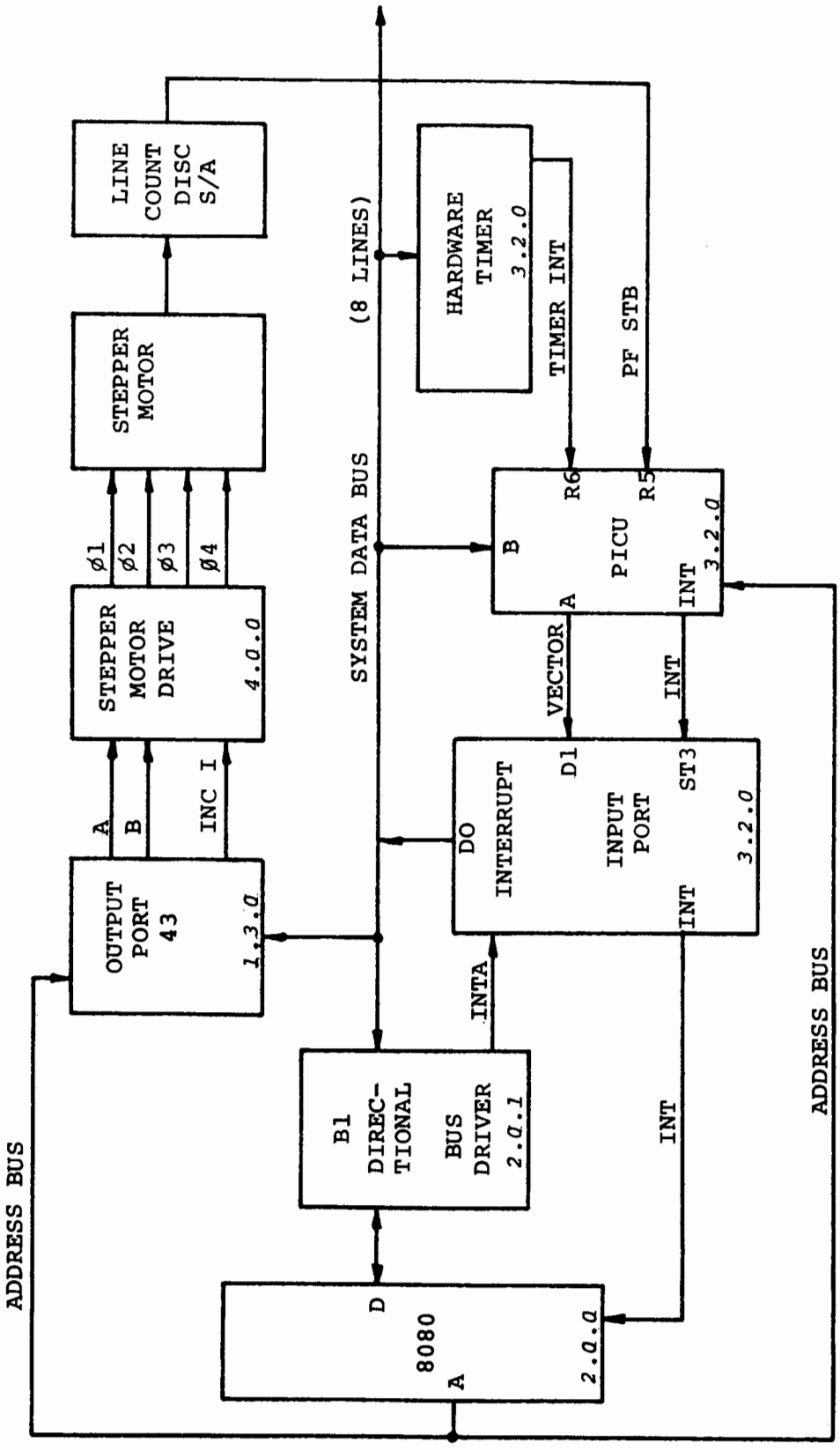


Figure 3-2. Paperfeed Cycle.

The vector directs the 8080 to the PF STB interrupt routine. This routine sets the Hardware Timer. When the timer counts down to zero, it generates a Timer Interrupt.

The timer interrupt routine changes the selection of phases to the stepper motor through Port 43 to continue paper advance.

The count set in the Hardware Timer determines the speed of paper advance. The count is varied for acceleration, slew, and deceleration.

3.11 PRINT CYCLE

The line of data to be printed is stored in the Line Memory in "chain code" during the Load Cycle, as shown in Figure 3-3.

Before actual printing begins, the contents of the Line Memory are used to set up the Chain Image Matrix Memory under 8080 control. It is set up on the basis of the character ":" of the chain over the column 1 hammer. This chain position is represented by row 1 of the Matrix Memory.

Each column of the Line Memory is read in sequence. The combination of the column address and chain code from the Line Memory is used to select the column and row address of the Matrix Memory. A "1" bit is inserted at the intersection of the row and column to indicate the firing of a particular hammer (column) at a particular chain position (row).

Printing begins at the current position of the chain. This is represented by a corresponding row in the Matrix Memory.

The 8080 keeps track of the current row position of the chain by constantly monitoring the INDEX and CHARACTER pulses.

The "zeros" and "ones" of the current row position are transferred from the Matrix Memory to their respective Hammer Driver Shift Register (HDSR). This is accomplished by direct memory access (DMA) in seventeen "8 bit" transfers.

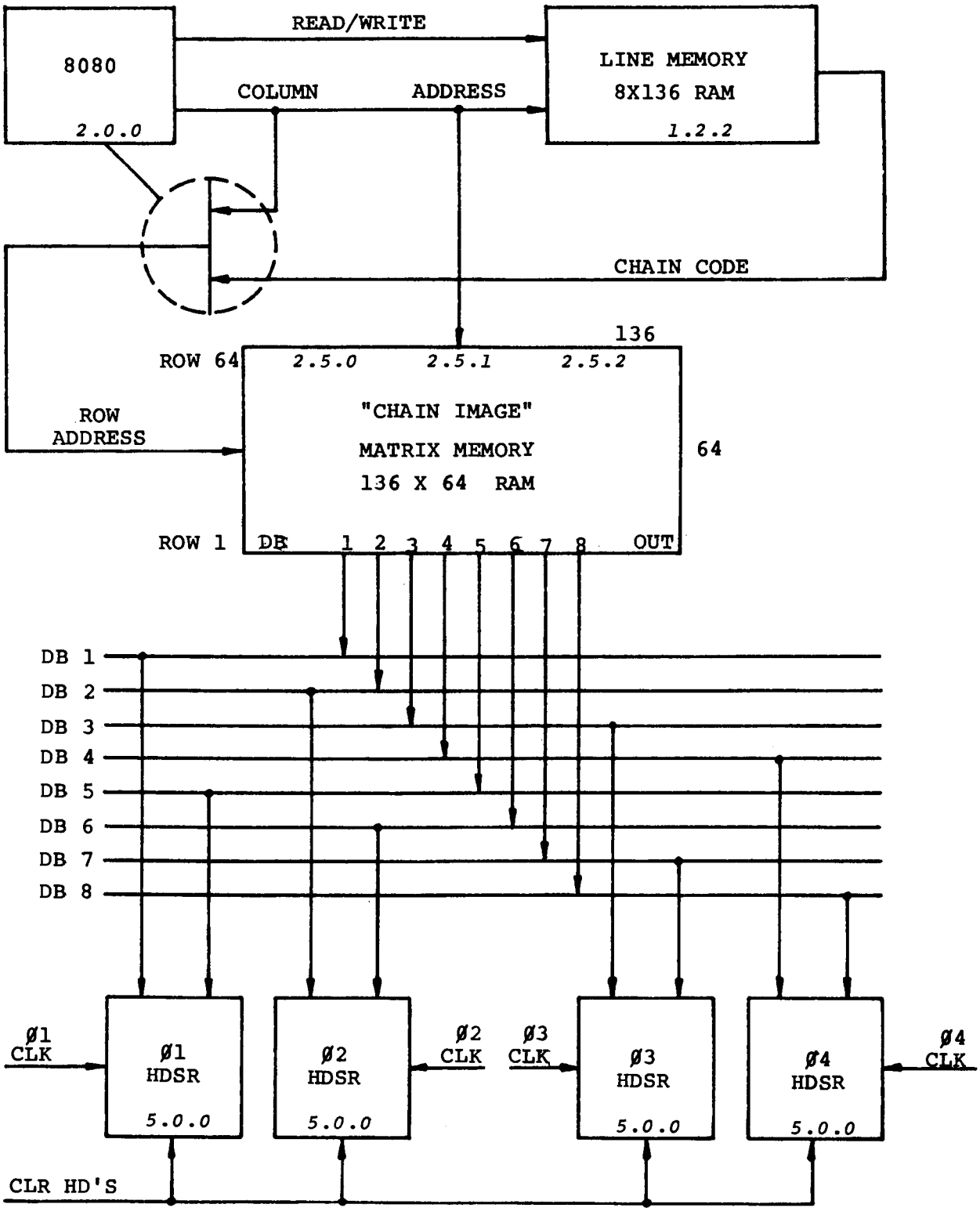


Figure 3-3. Print Cycle.

In each transfer, 2 discrete bits are shifted into each of four HDSR's. Each HDSR controls one phase of hammer actuators.

When transfer is complete, the hammers are fired in sequence. The $\phi 1$ hammers are fired first, followed by $\phi 2$, $\phi 3$, and $\phi 4$ at definite intervals.

The 8080 controls time between phases and determines when each phase of hammers is to be fired.

In the time between phases, the particular row of the Matrix Memory being printed is cleared to all zeros.

After the $\phi 4$ hammers are fired, the next row of the Matrix Memory is transferred to the HDSR's to continue the printing sequence. The Print Cycle is complete after all 64 rows of the Matrix Memory have been transferred and printed.

APPENDIX A

TYPICAL CONTROL SYSTEM OPERATING PROGRAM

ROM #1 - Initialization

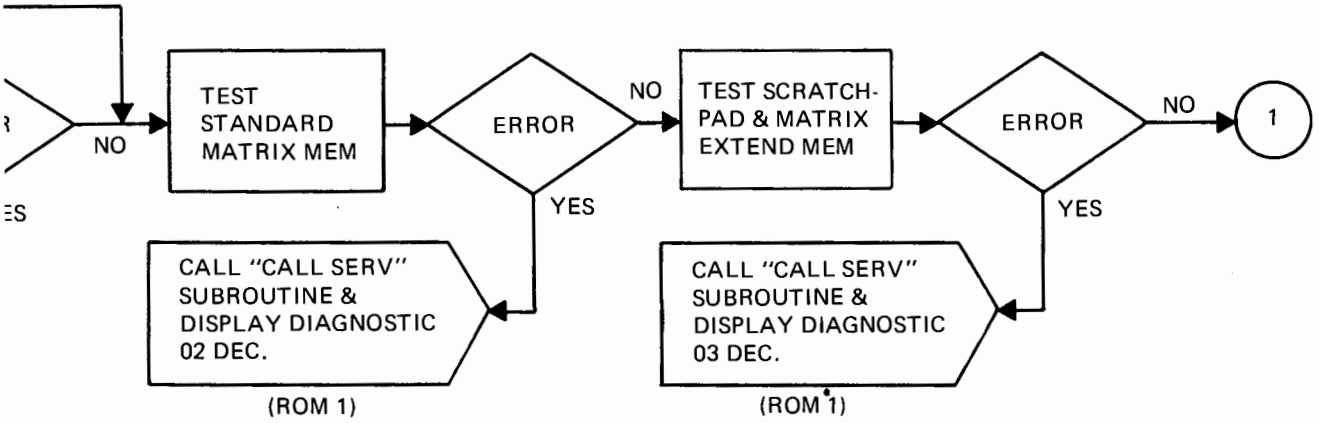
ROM #2 - Control Loop

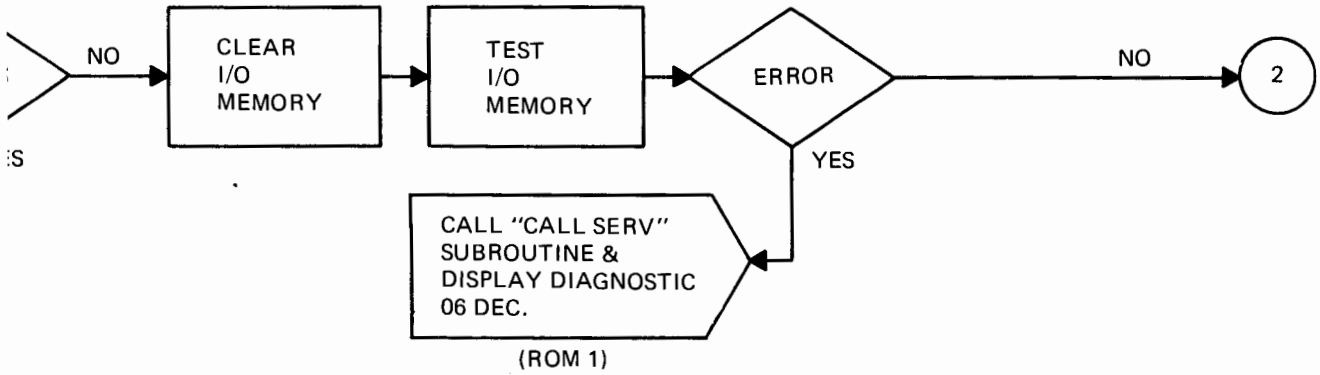
ROM #3 - Print Cycle

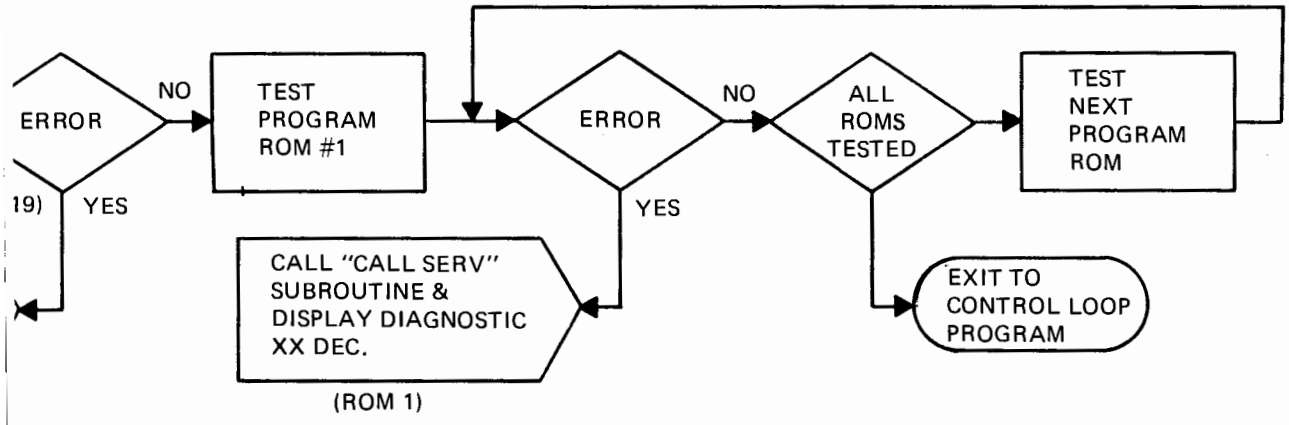
ROM's #4 and 6 - Paper Feed Cycle

ROM #5 - VF Sample

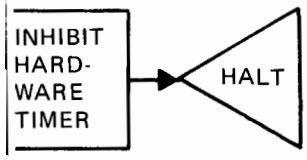
ROM #7 - Check Load





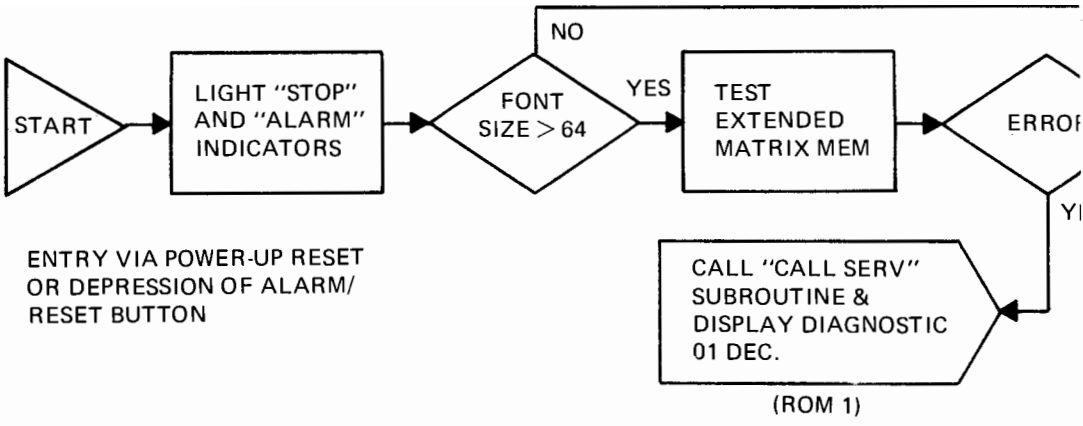


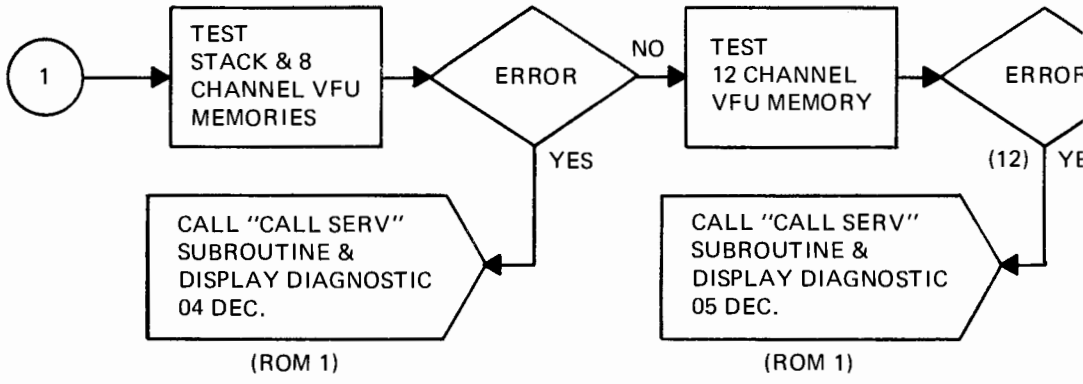
XX = 07 ROM 1
08 ROM 2
09 ROM 3
10 ROM 4
11 ROM 5
12 ROM 6
13 ROM 7 (OPTIONAL)*

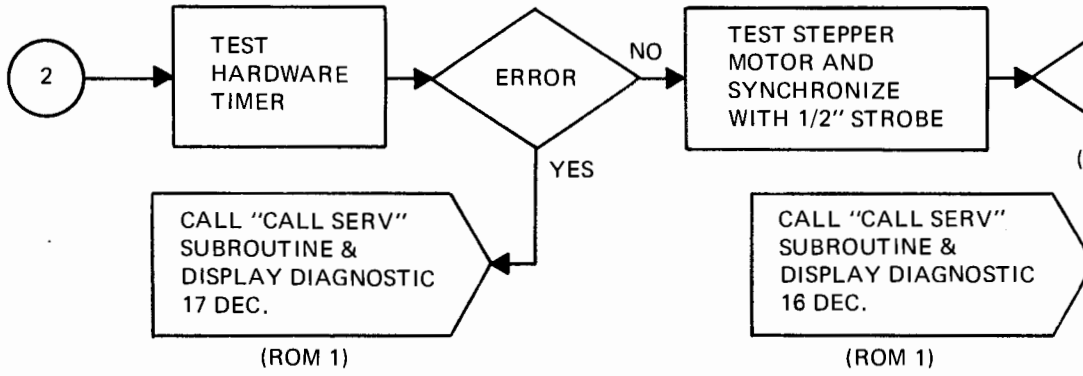


*THIS ROM IS CHECKED ONLY IF PRESENT

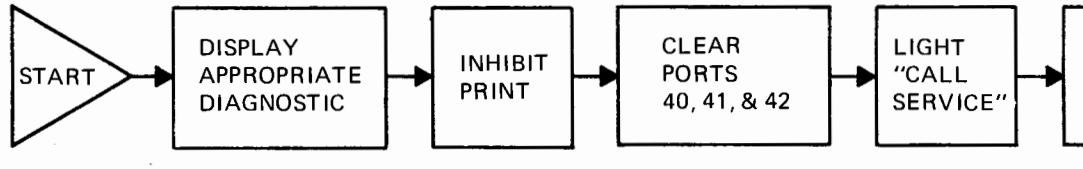
DATA PRINTER CORP.		
TITLE: INITIALIZATION ROM #1		
DWG. NO.	SHEET ___of___	REV.

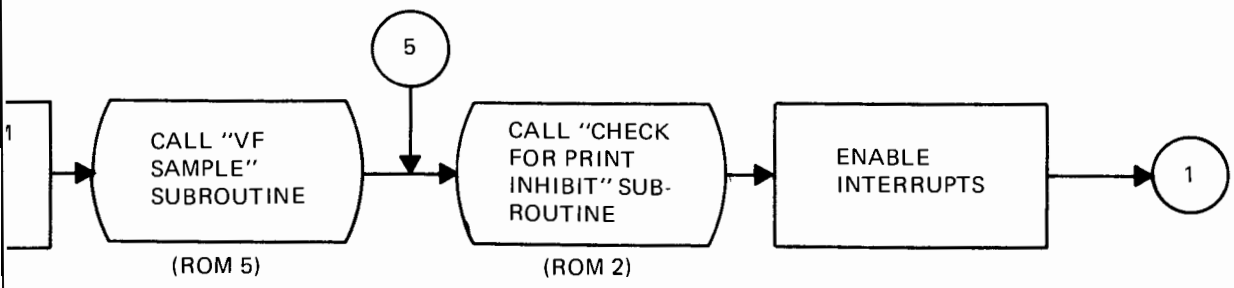


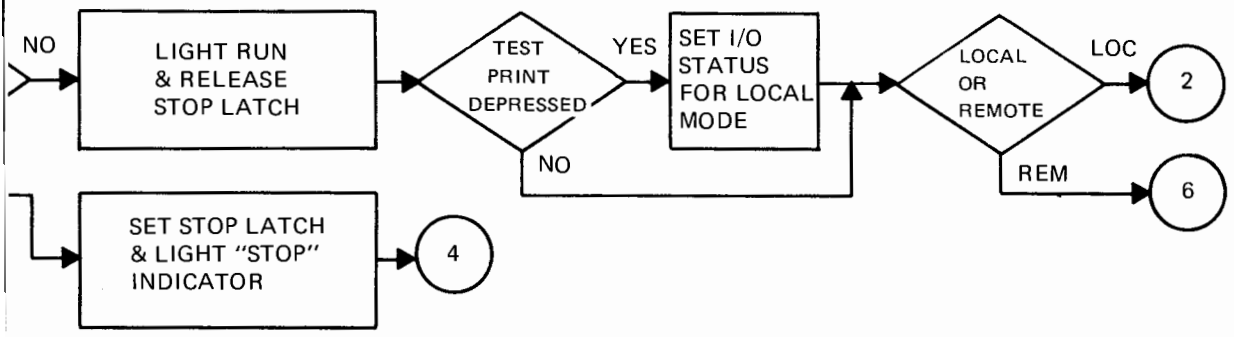


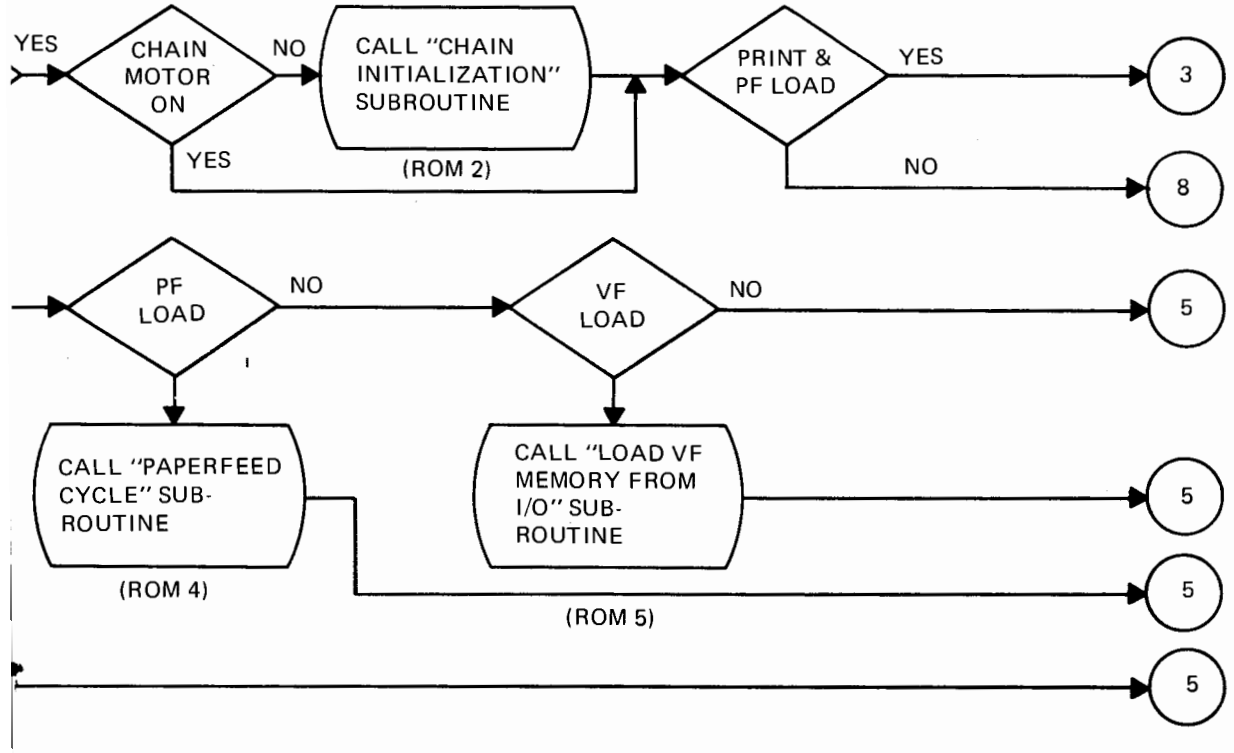


"CALL SERV" DIAGNOSTIC SUBROUTINE

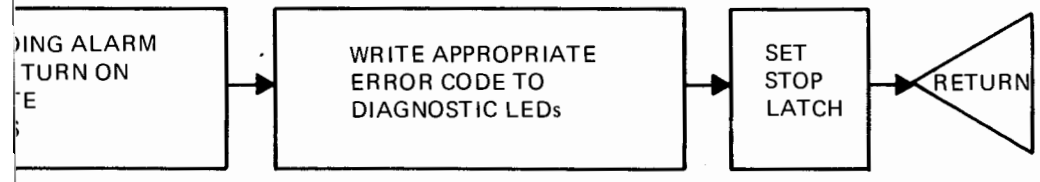




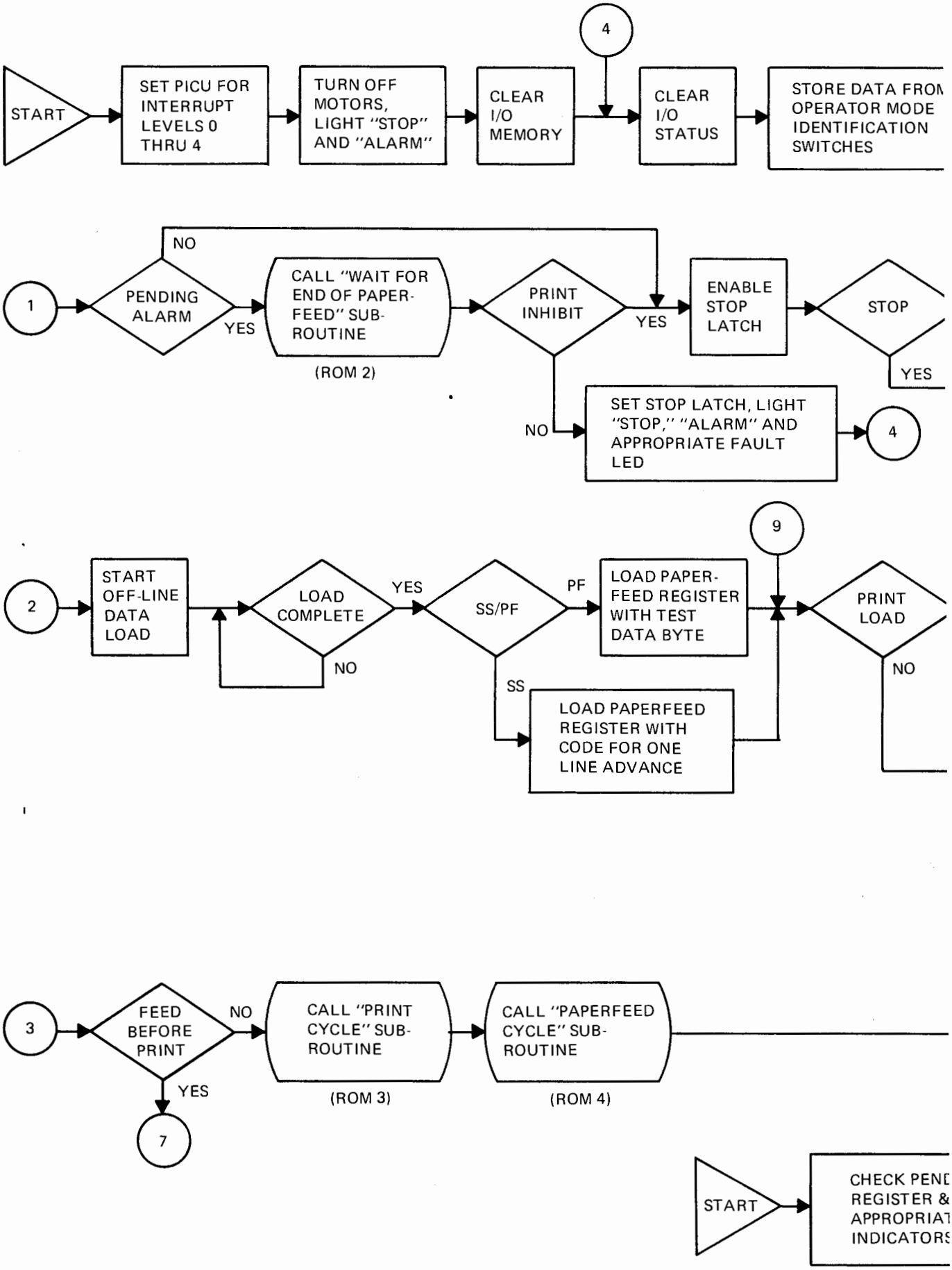


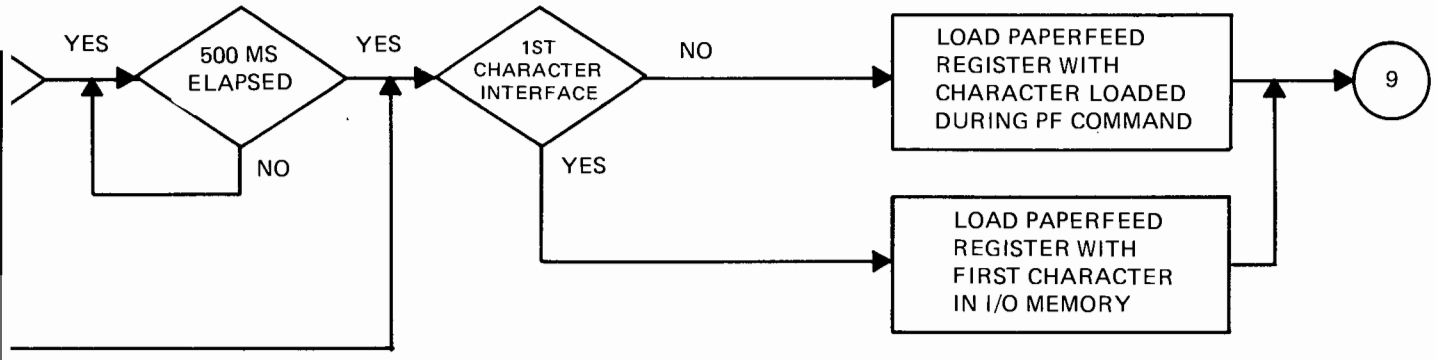


"VF SPACE ERROR" DIAGNOSTIC SUBROUTINE

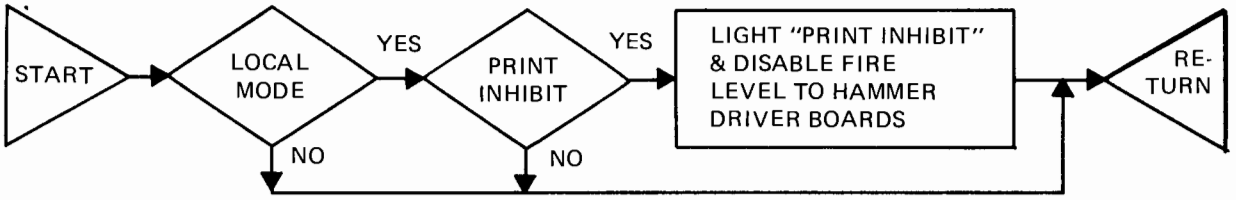


DATA PRINTER CORP.		
TITLE: CONTROL LOOP ROM #2		
DWG. NO.	SHEET ___of___	REV.

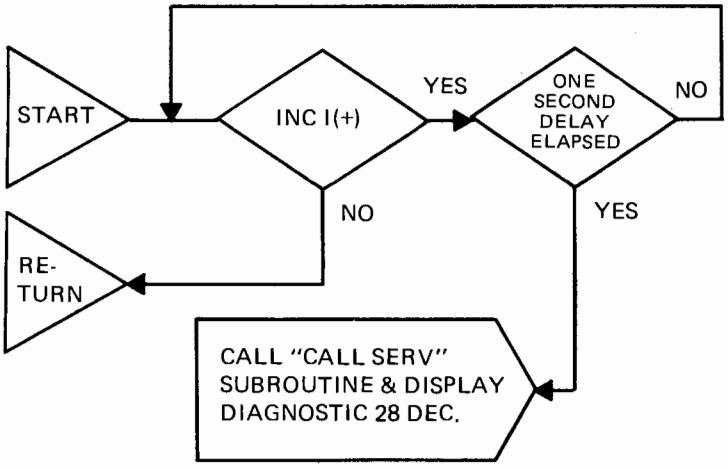

START
SET PICU FOR INTERRUPT LEVELS 0 THRU 4
TURN OFF MOTORS, LIGHT "STOP" AND "ALARM"
CLEAR I/O MEMORY
4
CLEAR I/O STATUS
STORE DATA FROM OPERATOR MODE IDENTIFICATION SWITCHES
1
PENDING ALARM
NO
YES
CALL "WAIT FOR END OF PAPER-FEED" SUB-ROUTINE
(ROM 2)
PRINT INHIBIT
YES
ENABLE STOP LATCH
STOP
YES
NO
SET STOP LATCH, LIGHT "STOP," "ALARM" AND APPROPRIATE FAULT LED
4
2
START OFF-LINE DATA LOAD
LOAD COMPLETE
YES
NO
SS/PF
PF
LOAD PAPER-FEED REGISTER WITH TEST DATA BYTE
SS
LOAD PAPERFEED REGISTER WITH CODE FOR ONE LINE ADVANCE
9
PRINT LOAD
NO
3
FEED BEFORE PRINT
NO
YES
7
CALL "PRINT CYCLE" SUB-ROUTINE
(ROM 3)
CALL "PAPERFEED CYCLE" SUB-ROUTINE
(ROM 4)
START
CHECK PEND
REGISTER &
APPROPRIAT
INDICATORS



"CHECK FOR PRINT INHIBIT" SUBROUTINE

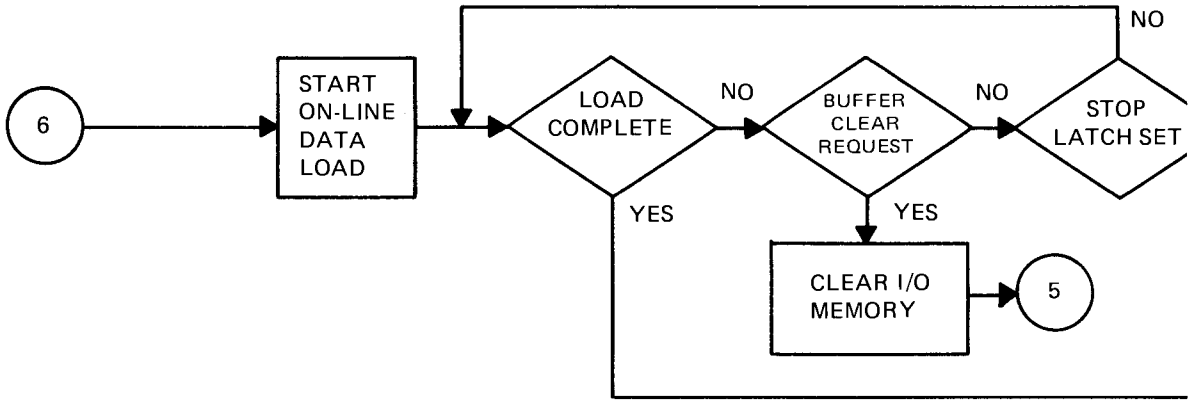


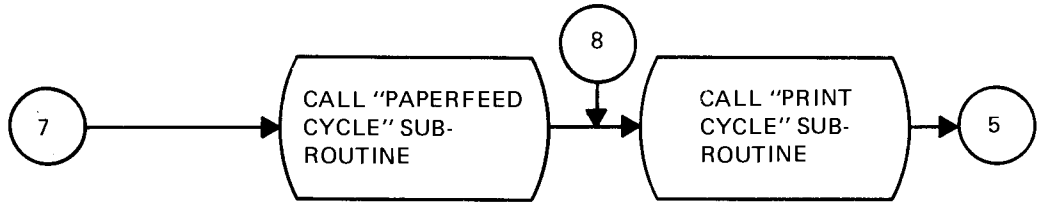
"WAIT FOR END OF PAPER FEED" SUBROUTINE



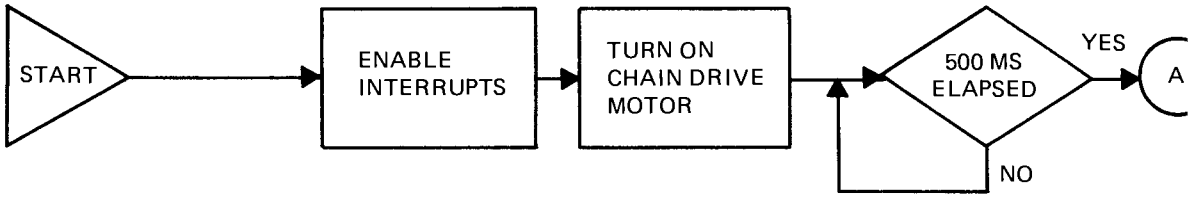
(ROM 1)

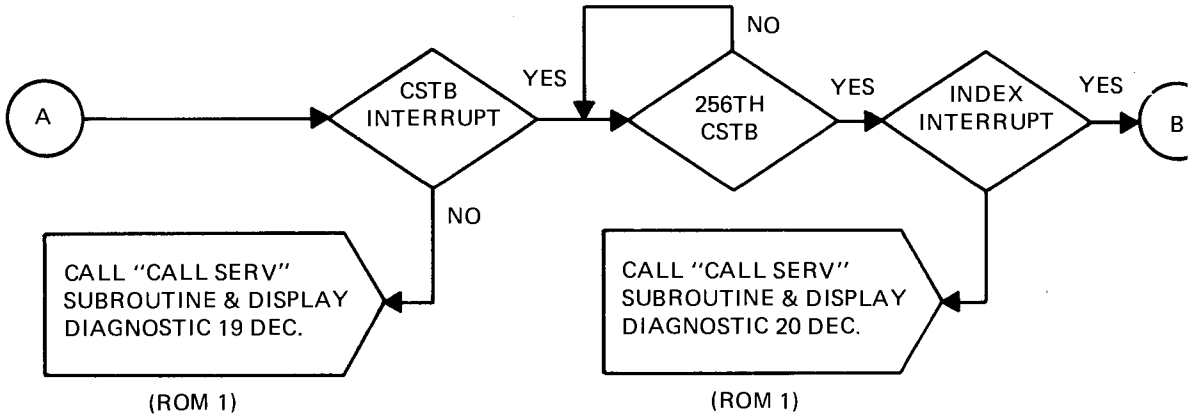
DATA PRINTER CORP.		
TITLE: CONTROL LOOP ROM #2		
DWG. NO.	SHEET ___of___	REV.

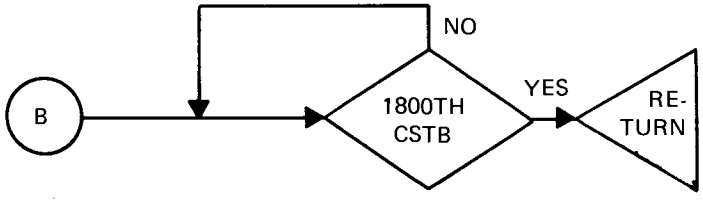


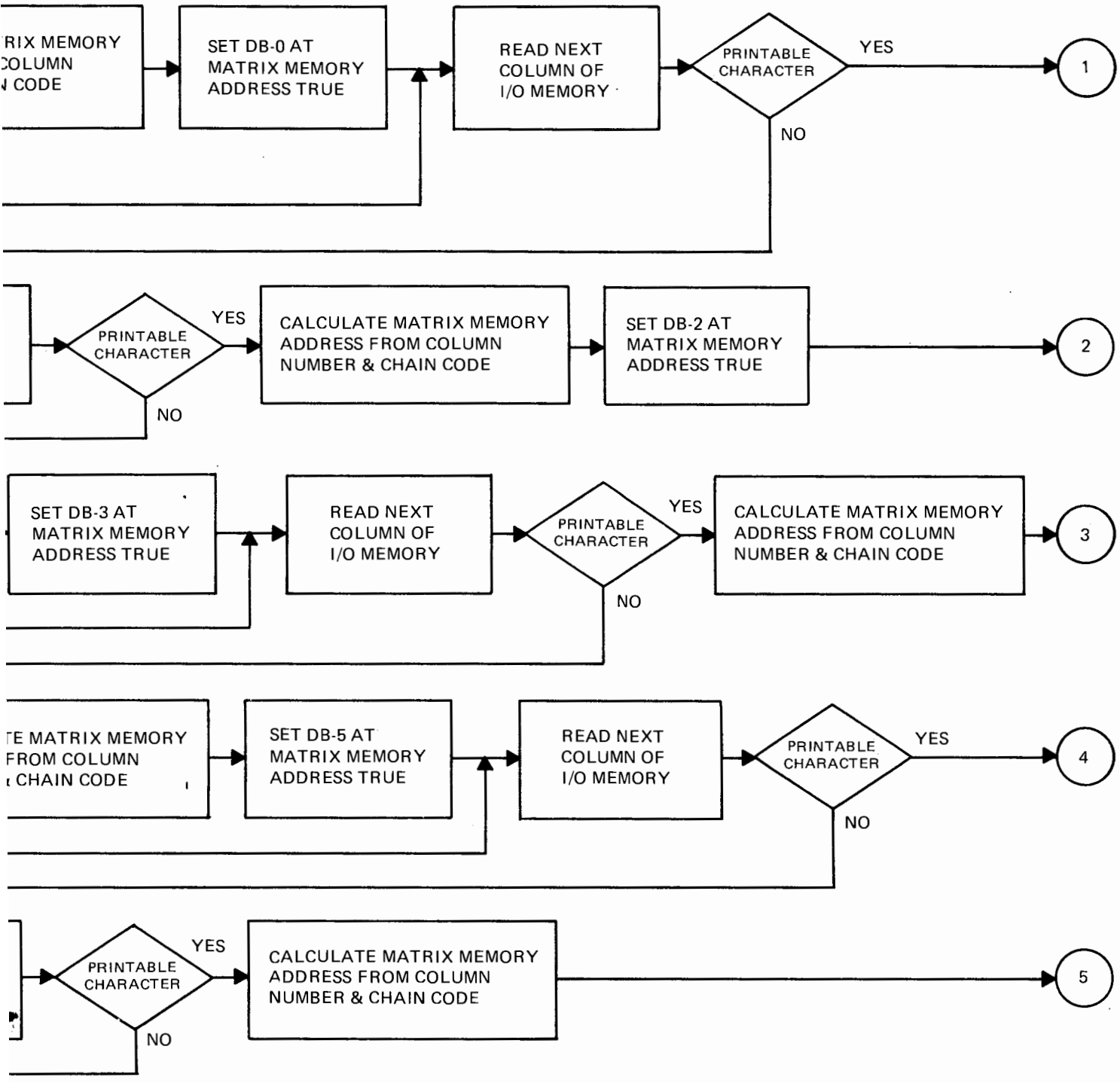


"CHAIN INITIALIZATION" SUBROUTINE

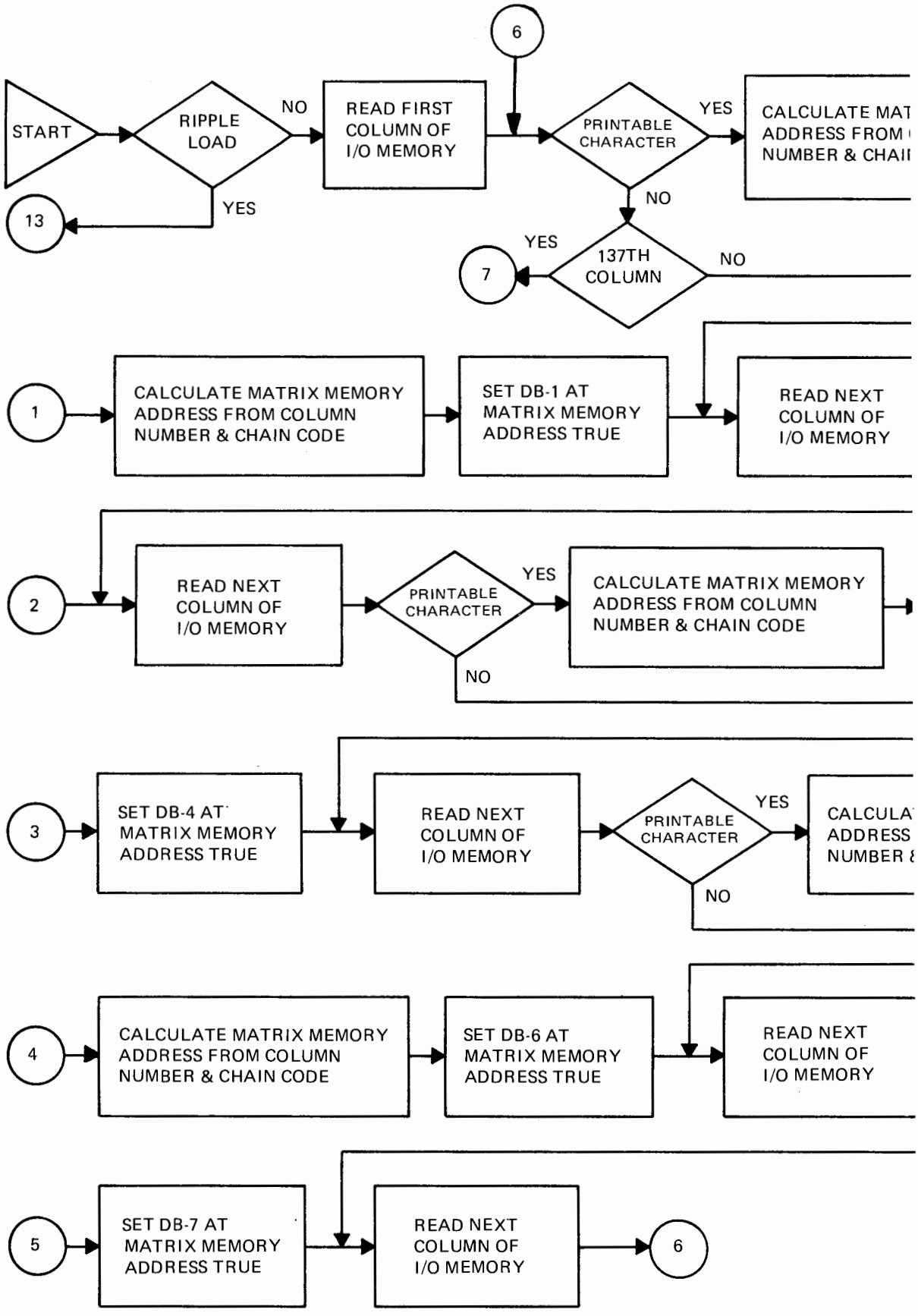


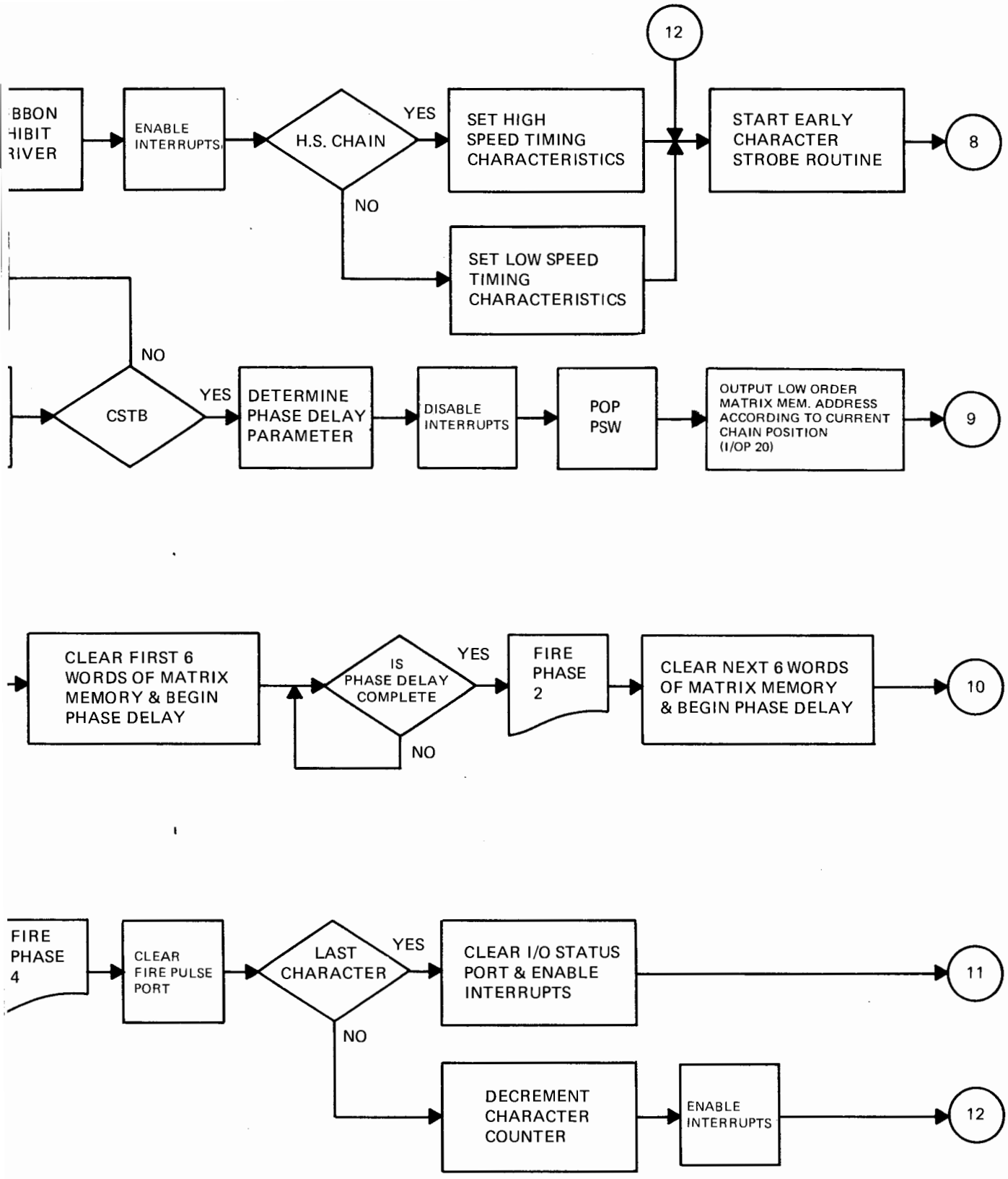




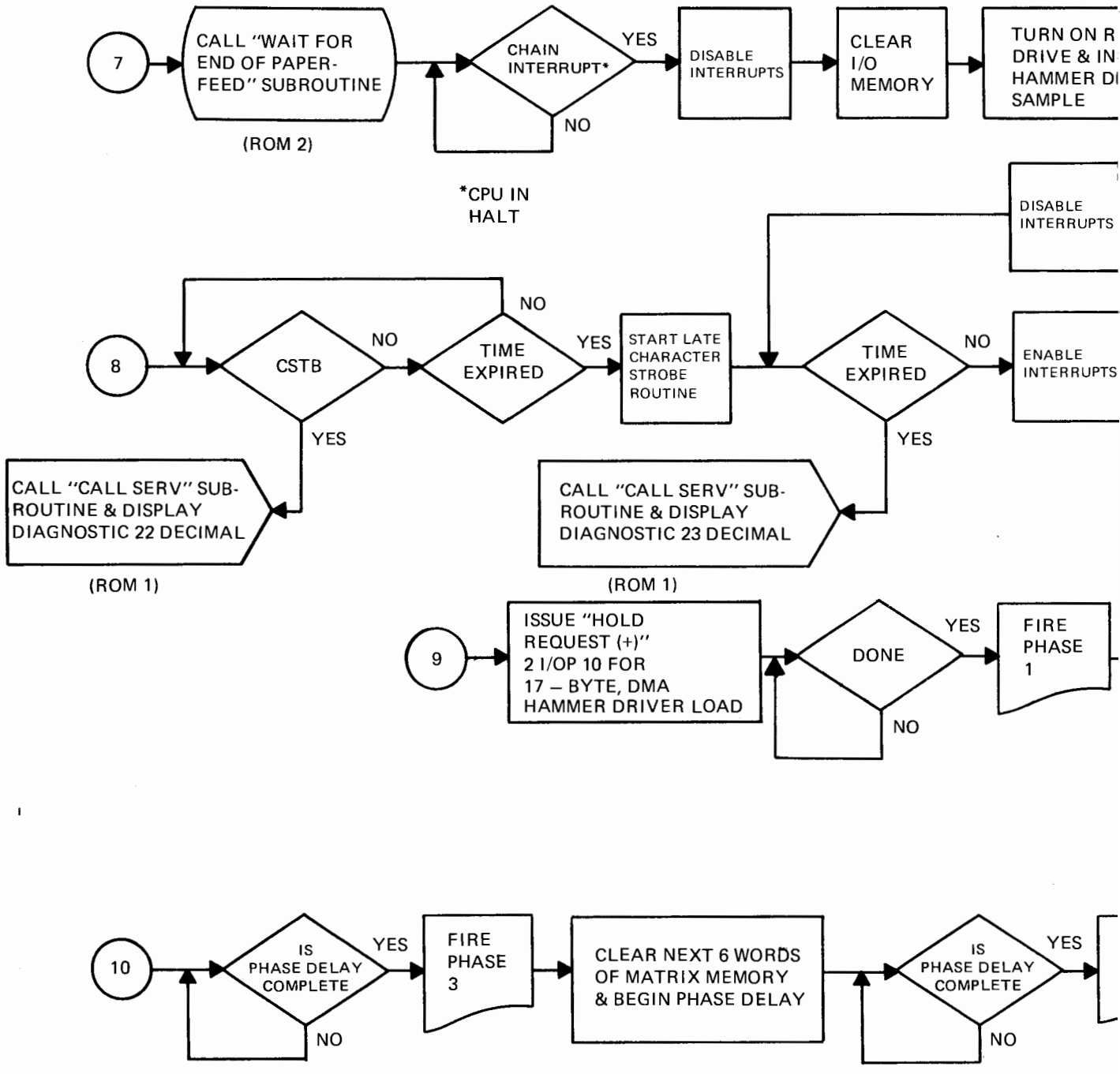


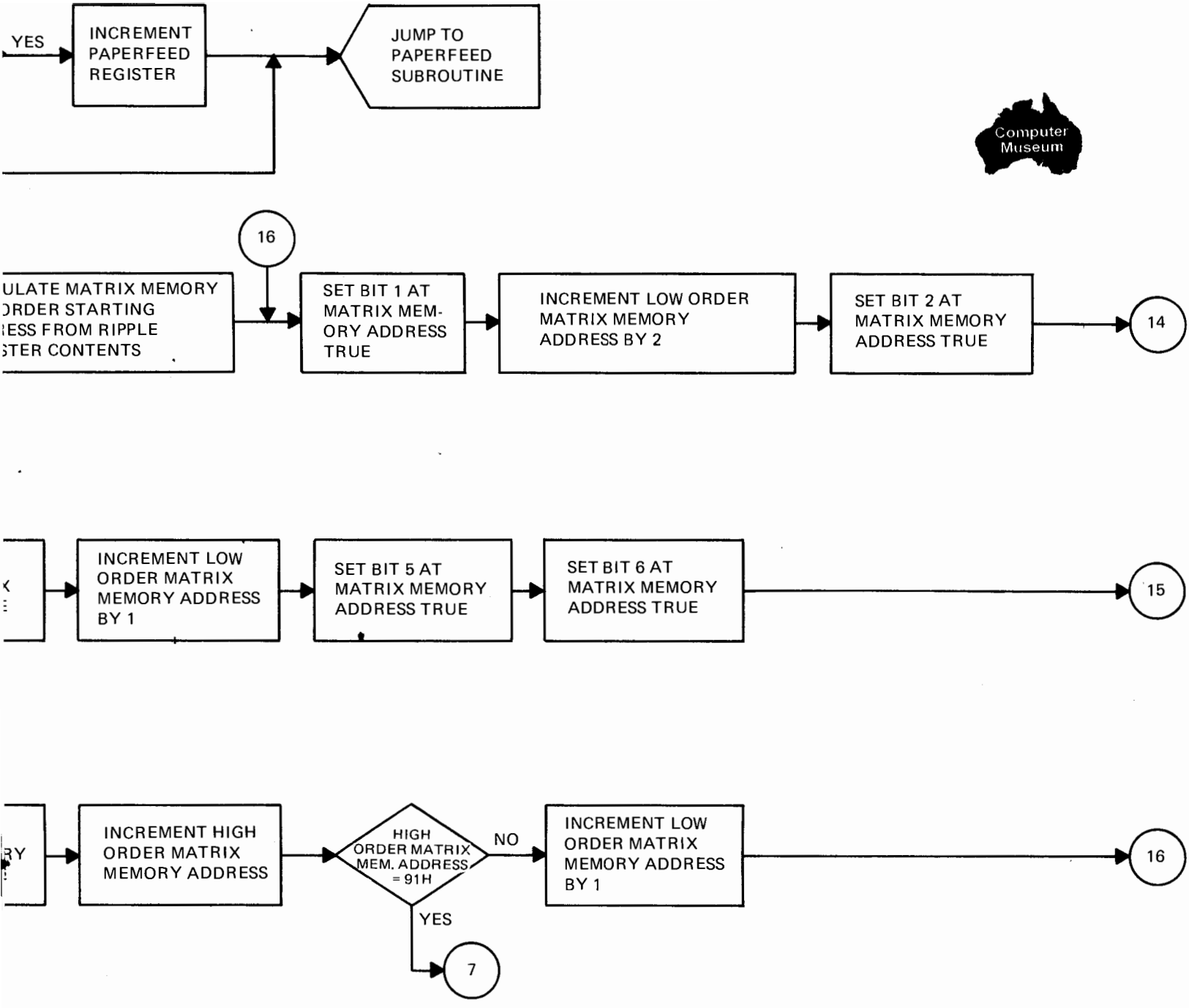
DATA PRINTER CORP.		
TITLE: PRINT CYCLE ROM #3		
DWG. NO.	SHEET ___of___	REV.


START
RIPPLE LOAD
NO
YES
13
READ FIRST COLUMN OF I/O MEMORY
6
PRINTABLE CHARACTER
YES
NO
CALCULATE MAT
ADDRESS FROM
NUMBER & CHAI
YES
137TH COLUMN
NO
7
1
CALCULATE MATRIX MEMORY ADDRESS FROM COLUMN NUMBER & CHAIN CODE
SET DB-1 AT MATRIX MEMORY ADDRESS TRUE
READ NEXT COLUMN OF I/O MEMORY
2
READ NEXT COLUMN OF I/O MEMORY
PRINTABLE CHARACTER
YES
NO
CALCULATE MATRIX MEMORY ADDRESS FROM COLUMN NUMBER & CHAIN CODE
3
SET DB-4 AT MATRIX MEMORY ADDRESS TRUE
READ NEXT COLUMN OF I/O MEMORY
PRINTABLE CHARACTER
YES
NO
CALCULA
ADDRESS
NUMBER &
4
CALCULATE MATRIX MEMORY ADDRESS FROM COLUMN NUMBER & CHAIN CODE
SET DB-6 AT MATRIX MEMORY ADDRESS TRUE
READ NEXT COLUMN OF I/O MEMORY
5
SET DB-7 AT MATRIX MEMORY ADDRESS TRUE
READ NEXT COLUMN OF I/O MEMORY
6

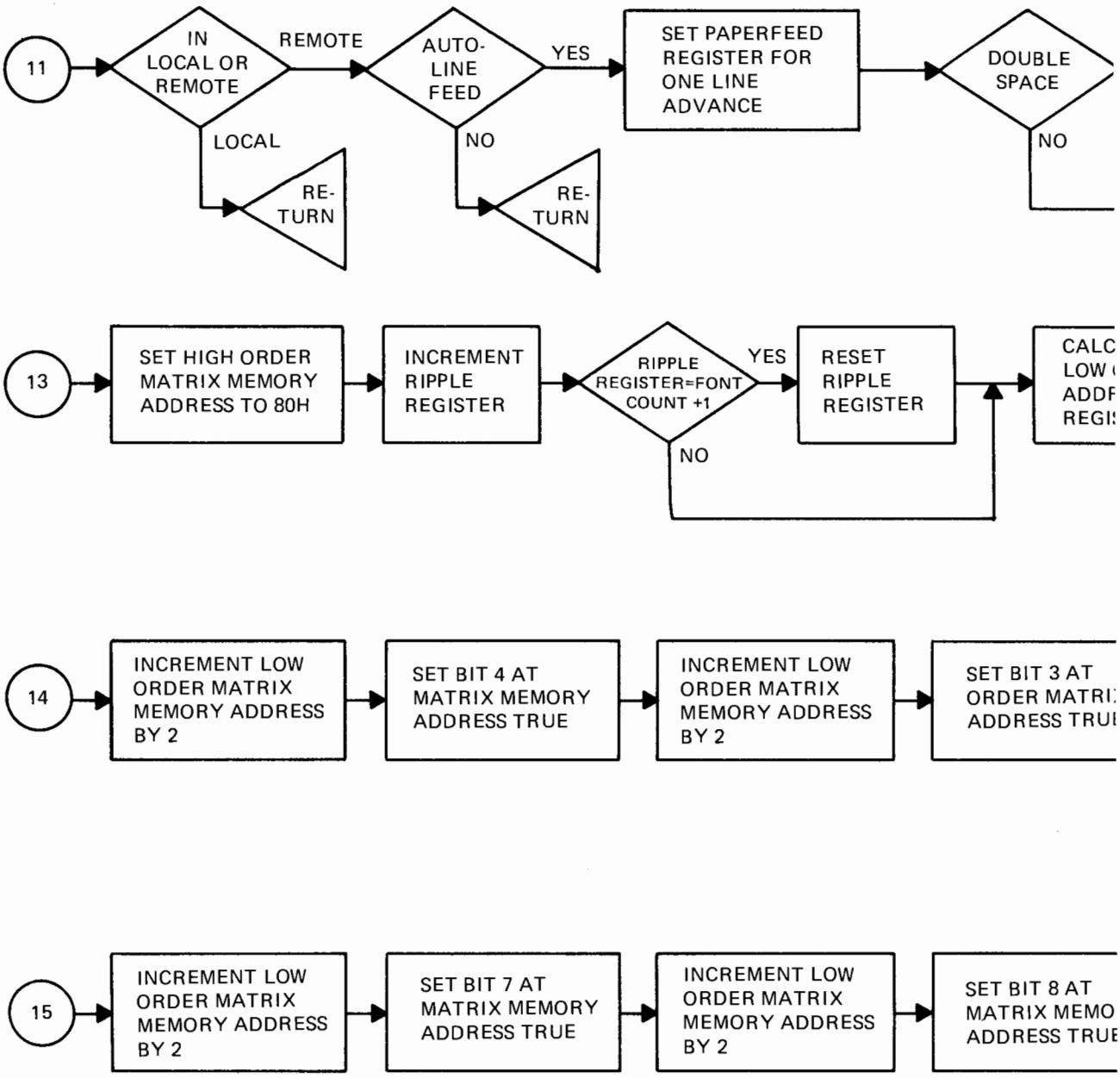


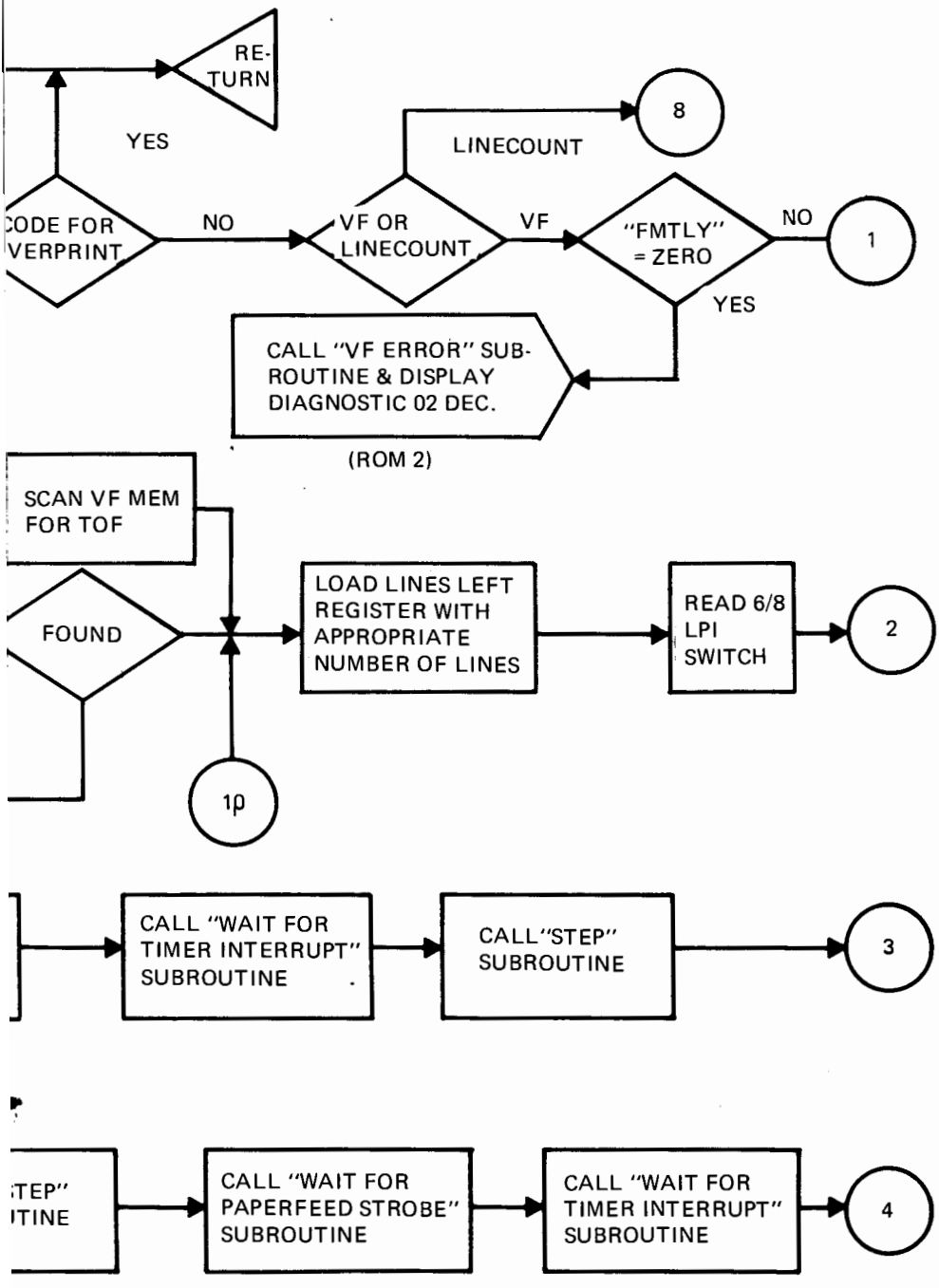
DATA PRINTER CORP.		
TITLE: PRINT CYCLE ROM #3		
DWG. NO.	SHEET ___of___	REV.


7
CALL "WAIT FOR END OF PAPER-FEED" SUBROUTINE
(ROM 2)
CHAIN INTERRUPT*
YES
NO
*CPU IN HALT
DISABLE INTERRUPTS
CLEAR I/O MEMORY
TURN ON R
DRIVE & IN
HAMMER DI
SAMPLE
DISABLE INTERRUPTS
8
CSTB
NO
TIME EXPIRED
NO
YES
START LATE CHARACTER STROBE ROUTINE
TIME EXPIRED
NO
ENABLE INTERRUPTS
YES
YES
CALL "CALL SERV" SUB-ROUTINE & DISPLAY DIAGNOSTIC 22 DECIMAL
(ROM 1)
CALL "CALL SERV" SUB-ROUTINE & DISPLAY DIAGNOSTIC 23 DECIMAL
(ROM 1)
9
ISSUE "HOLD REQUEST (+)" 2 I/OP 10 FOR 17 – BYTE, DMA HAMMER DRIVER LOAD
DONE
YES
NO
FIRE PHASE 1
10
IS PHASE DELAY COMPLETE
YES
NO
FIRE PHASE 3
CLEAR NEXT 6 WORDS OF MATRIX MEMORY & BEGIN PHASE DELAY
IS PHASE DELAY COMPLETE
YES
NO



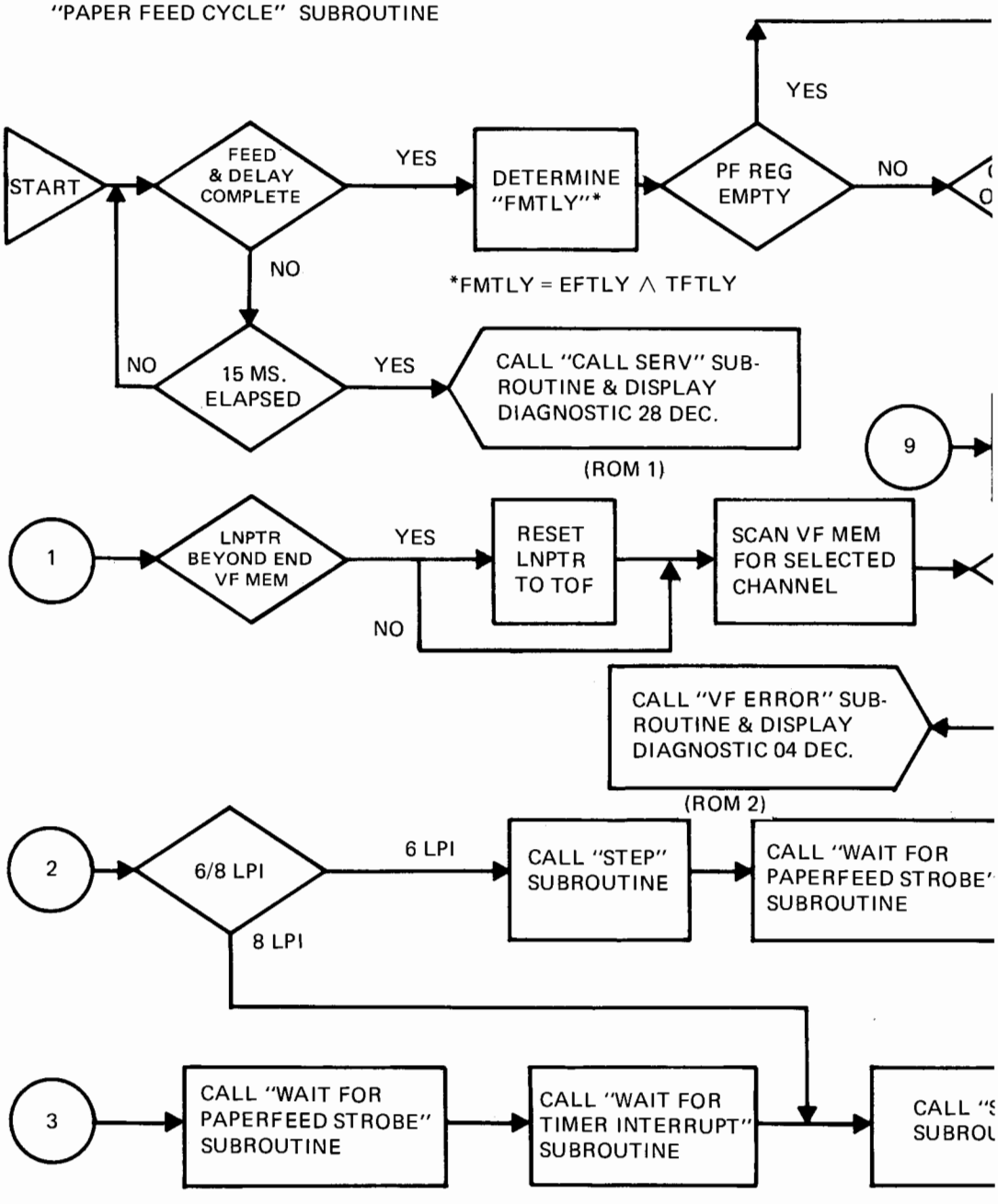
DATA PRINTER CORP.		
TITLE: PRINT CYCLE ROM #3		
DWG. NO.	SHEET ___of___	REV.

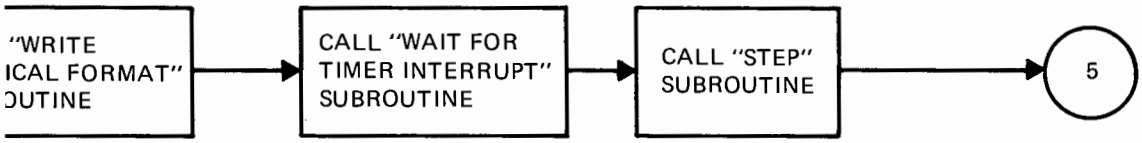

11
IN LOCAL OR REMOTE
REMOTE
AUTO-LINE FEED
YES
SET PAPERFEED REGISTER FOR ONE LINE ADVANCE
DOUBLE SPACE
NO
LOCAL
RE-TURN
NO
RE-TURN
13
SET HIGH ORDER MATRIX MEMORY ADDRESS TO 80H
INCREMENT RIPPLE REGISTER
RIPPLE REGISTER=FONT COUNT +1
YES
RESET RIPPLE REGISTER
NO
14
INCREMENT LOW ORDER MATRIX MEMORY ADDRESS BY 2
SET BIT 4 AT MATRIX MEMORY ADDRESS TRUE
INCREMENT LOW ORDER MATRIX MEMORY ADDRESS BY 2
15
INCREMENT LOW ORDER MATRIX MEMORY ADDRESS BY 2
SET BIT 7 AT MATRIX MEMORY ADDRESS TRUE
INCREMENT LOW ORDER MATRIX MEMORY ADDRESS BY 2

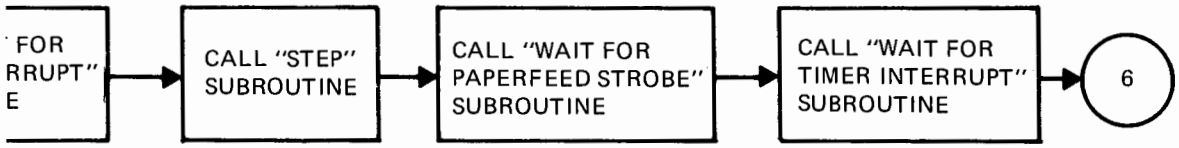


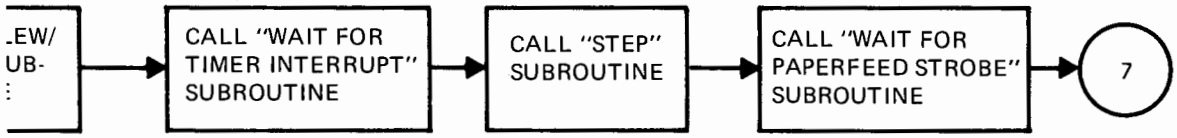
DATA PRINTER CORP.		
TITLE: PAPER FEED CYCLE ROMS 4 & 6		
DWG. NO.	SHEET __of__	REV.

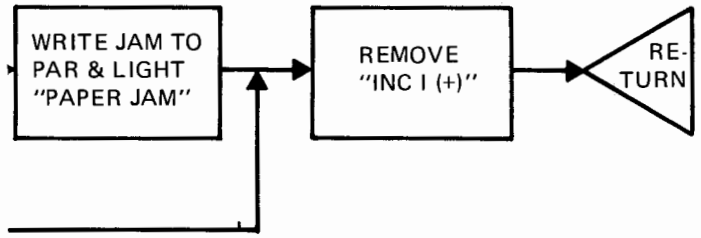
"PAPER FEED CYCLE" SUBROUTINE

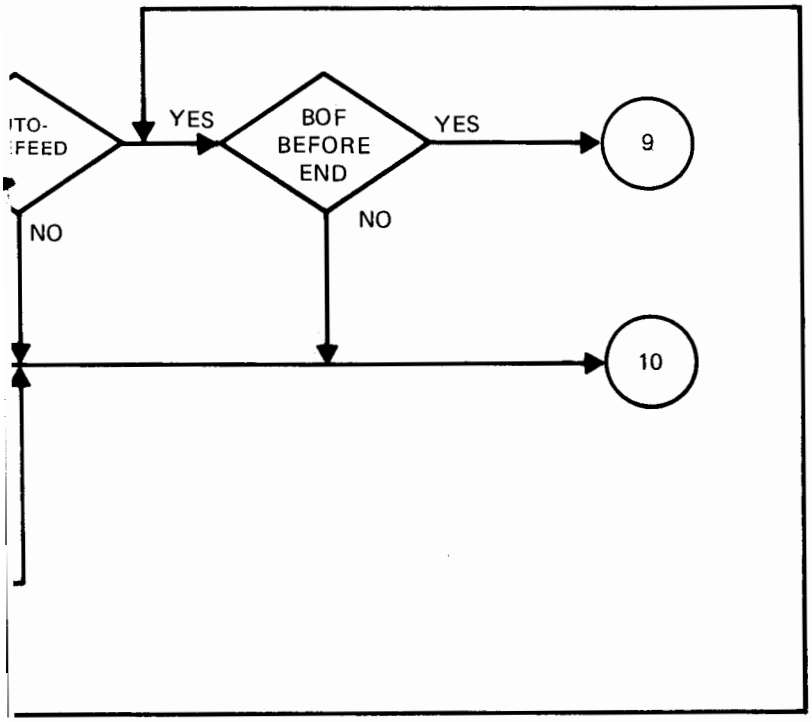






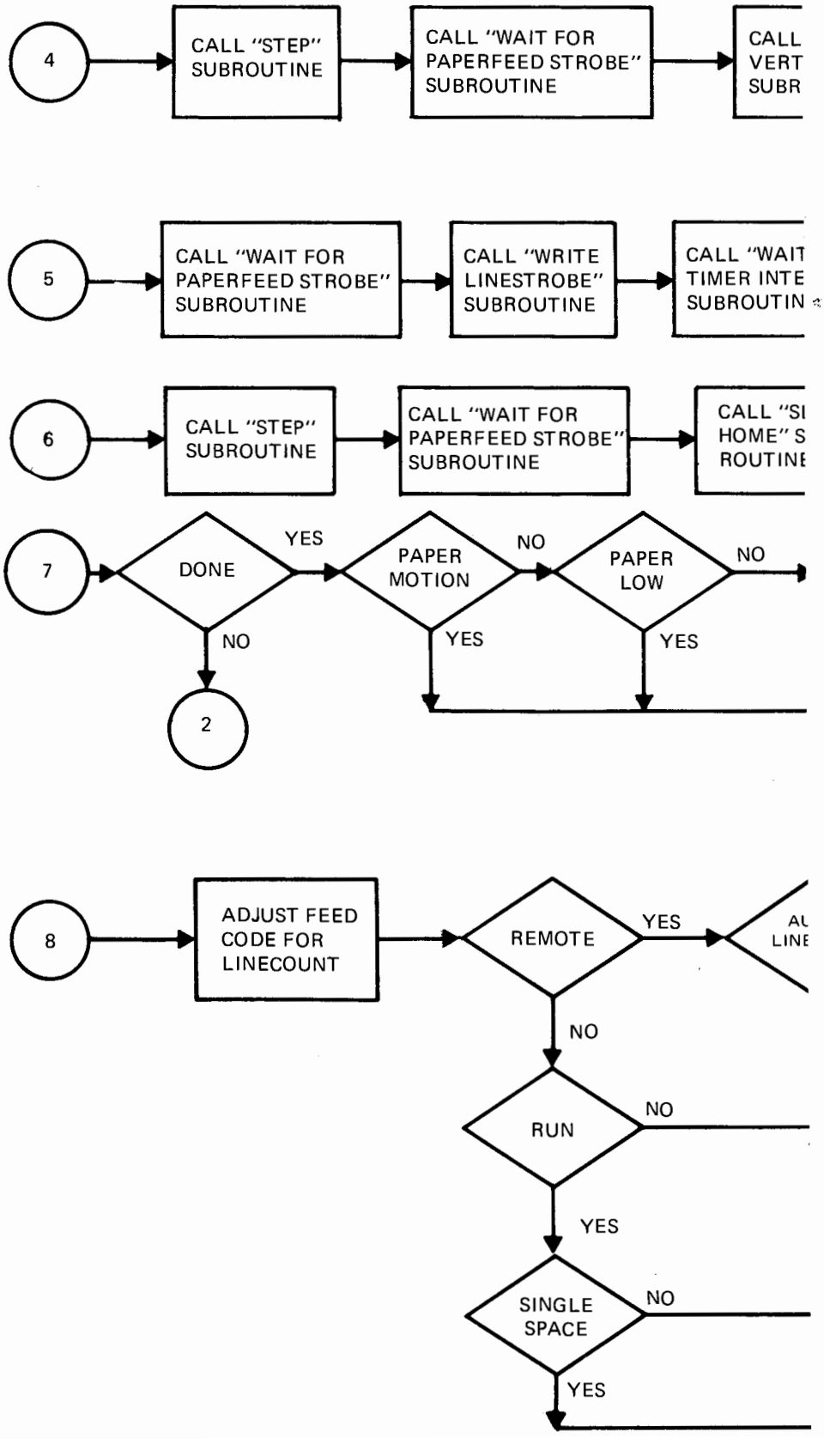


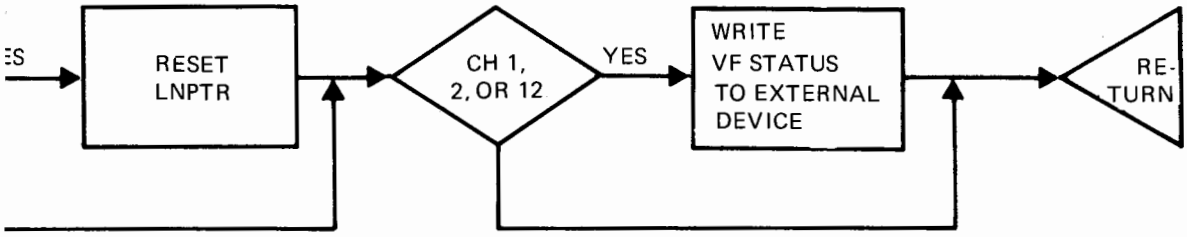


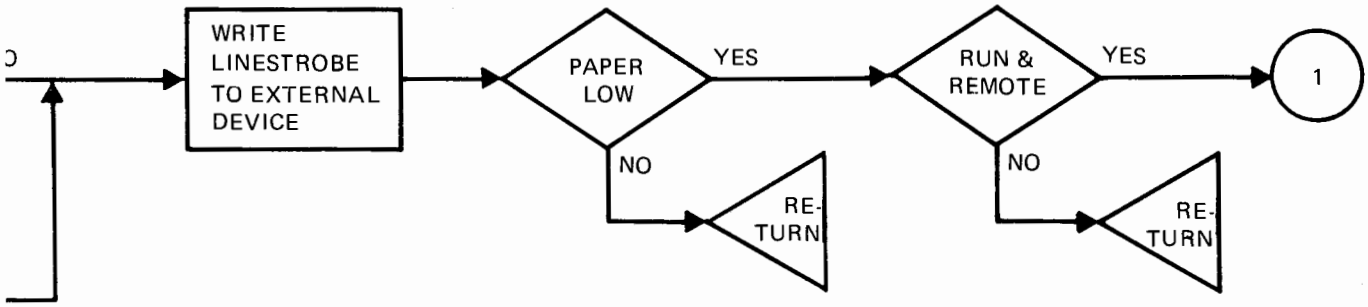


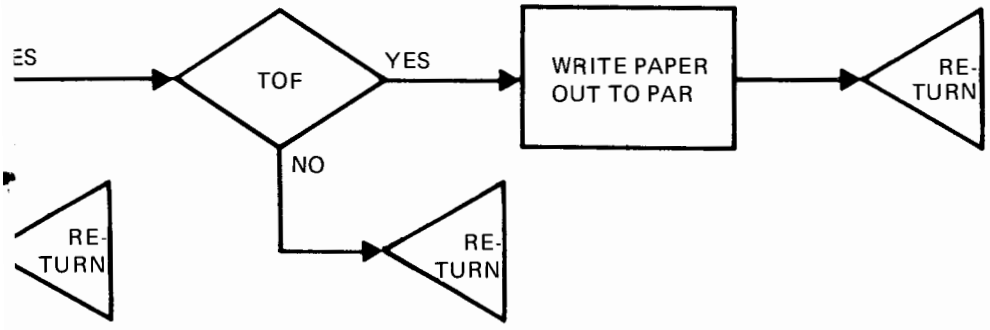
DATA PRINTER CORP.		
TITLE: PAPER FEED CYCLE ROMS 4 & 6		
DWG. NO.	SHEET __of__	REV.

"PAPER FEED CYCLE" SUBROUTINE (CONT.)



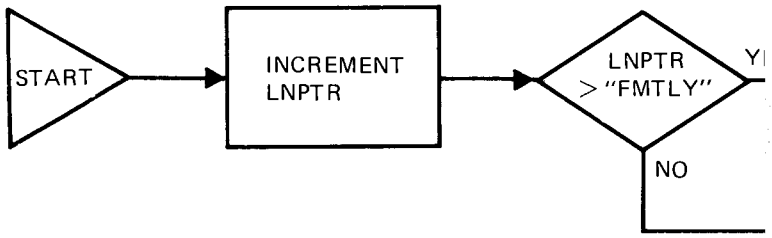




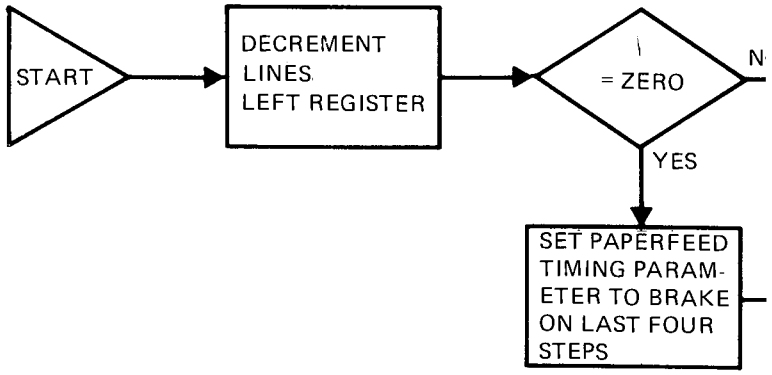


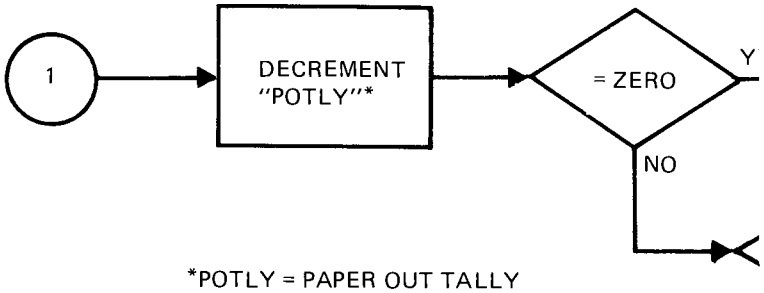
DATA PRINTER CORP.		
TITLE: PAPER FEED CYCLE ROMS 4 & 6		
DWG. NO.	SHEET ___of___	REV.

"WRITE VERTICAL FORMAT" SUBROUTINE

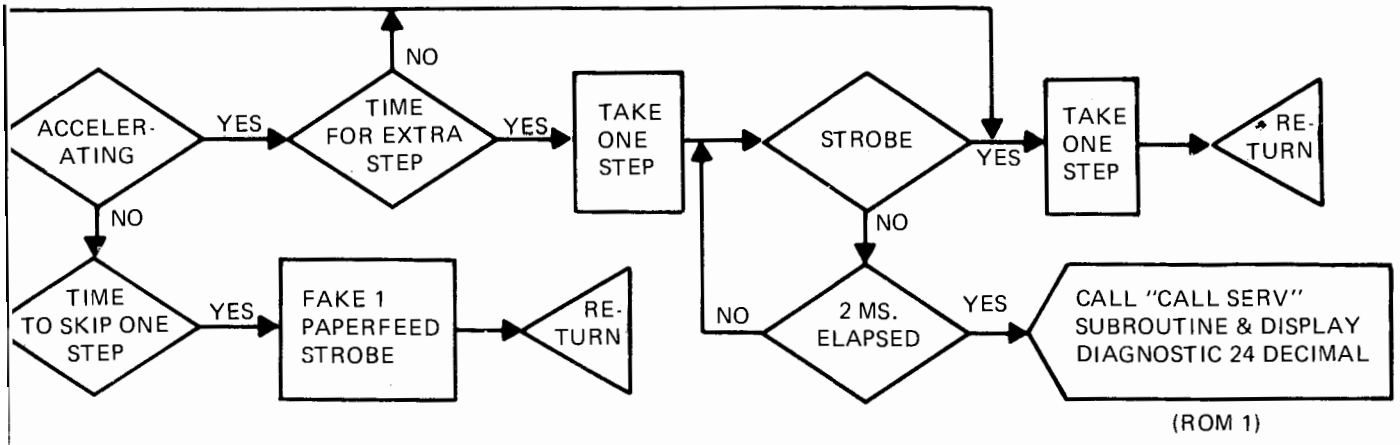


"WRITE LINESTROBE" SUBROUTINE

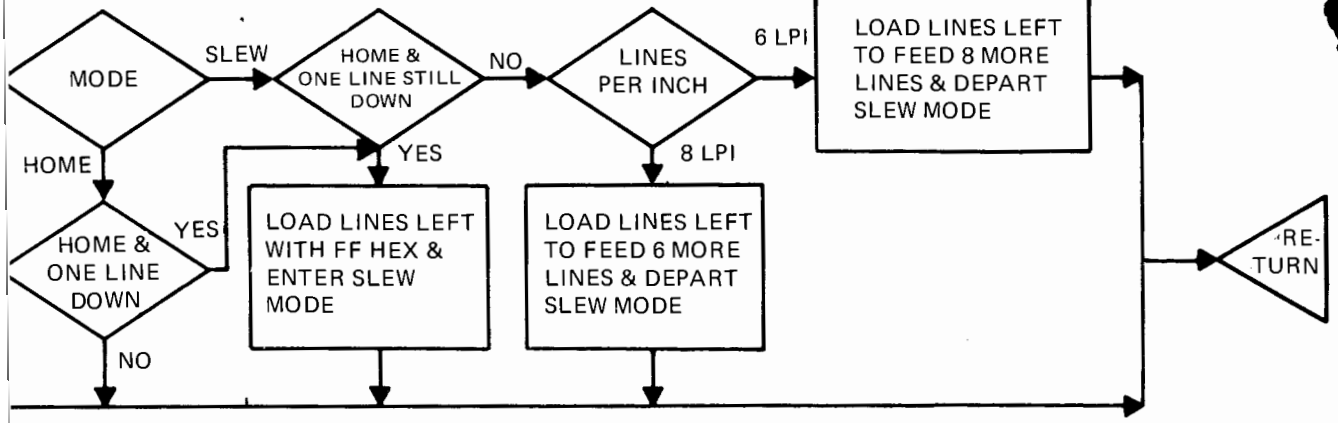


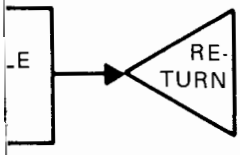


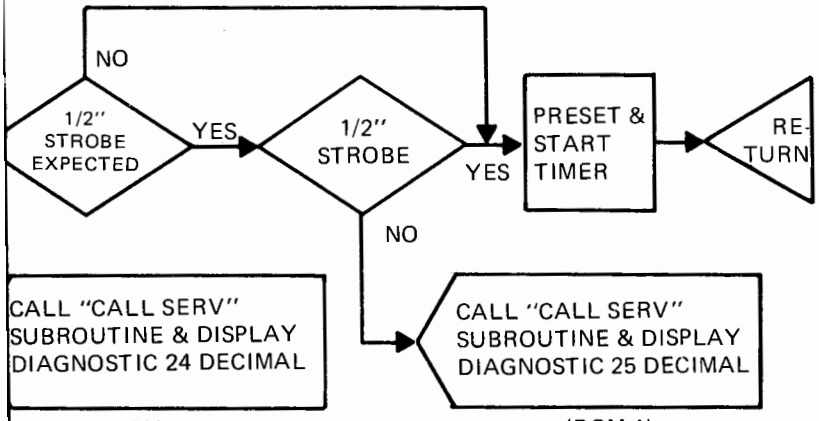
*POTLY = PAPER OUT TALLY



(ROM 1)







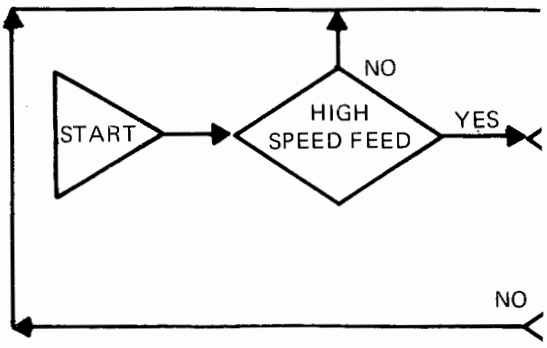
(ROM 1)

(ROM 1)

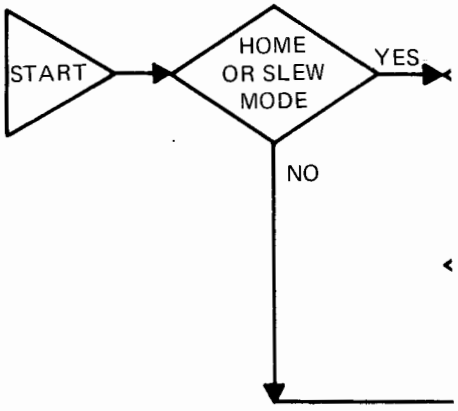
DATA PRINTER CORP.

TITLE	PAPER FEED CYCLE ROOM 4 & 6		
DWG. NO.		SHEET ___of___	REV.

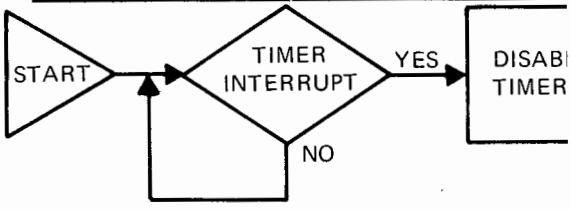
"STEP" SUBROUTINE



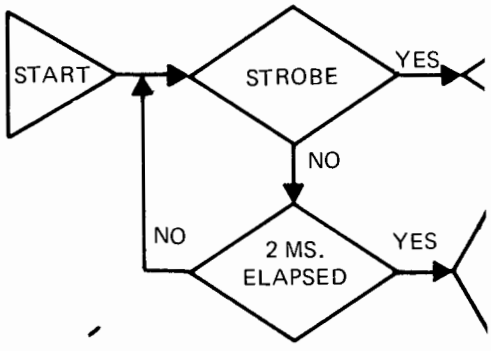
"SLEW/HOME?" SUBROUTINE

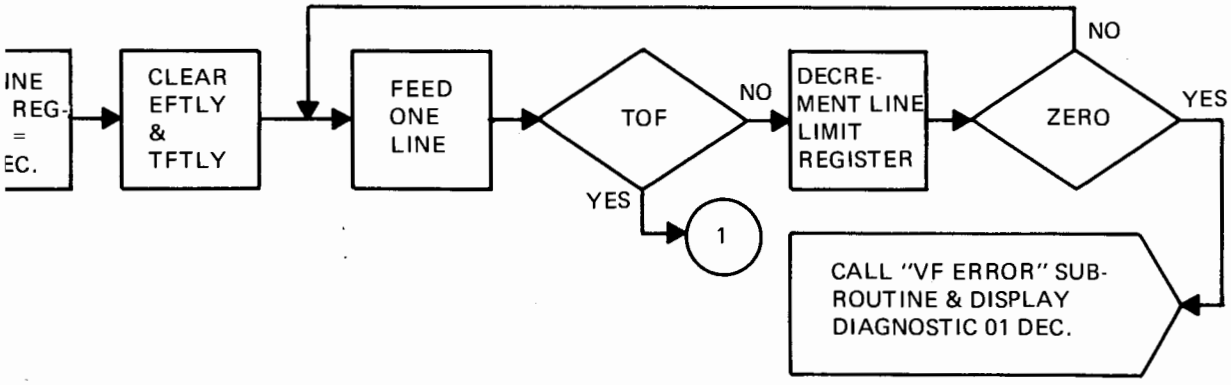


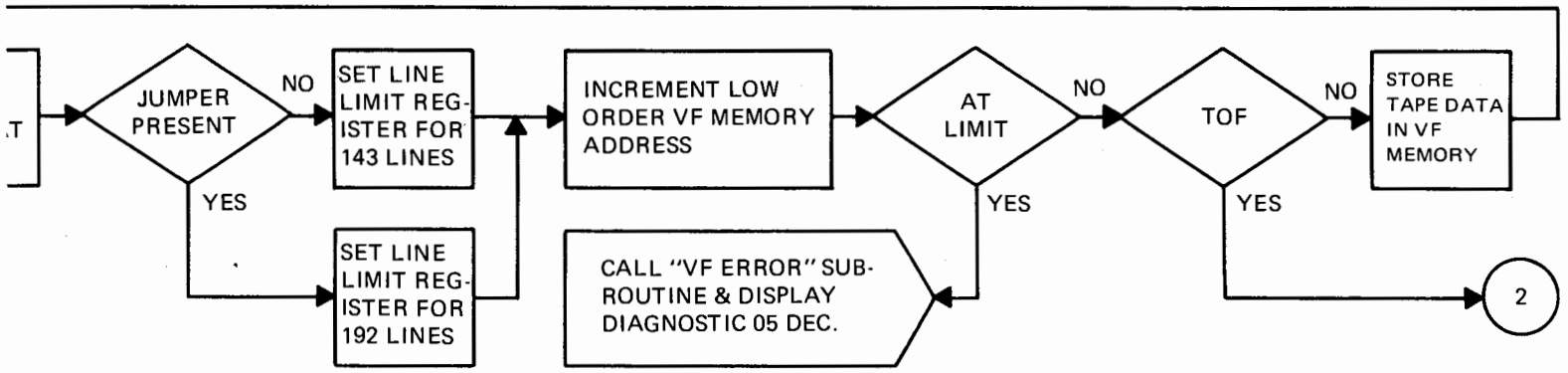
"WAIT FOR TIMER INTERRUPT" SUBROUTINE

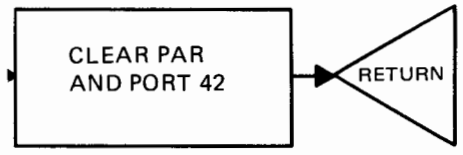


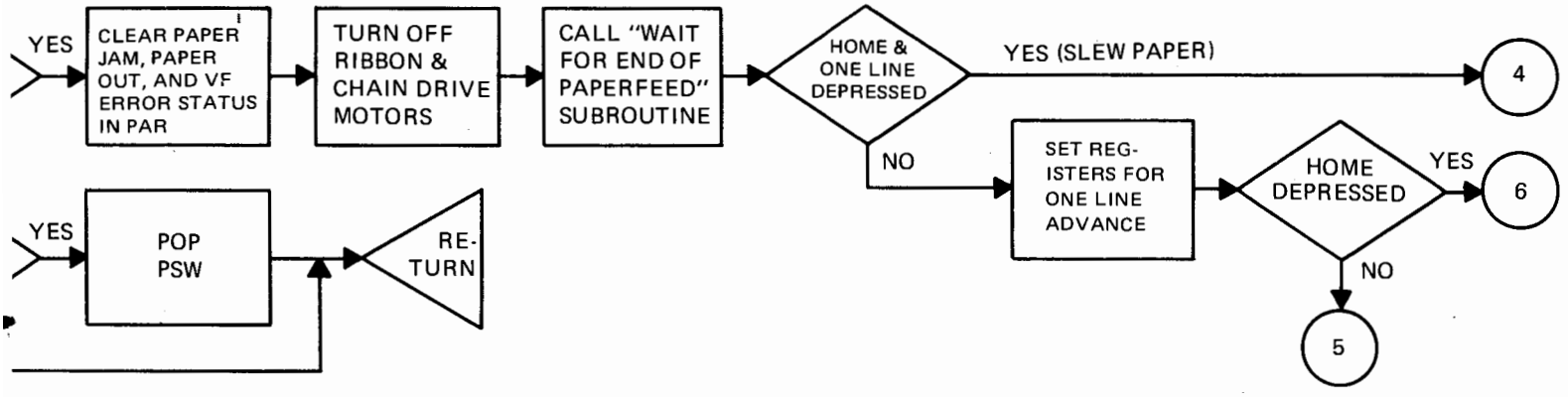
"WAIT FOR PAPERFEED STROBE" SUBROUTINE

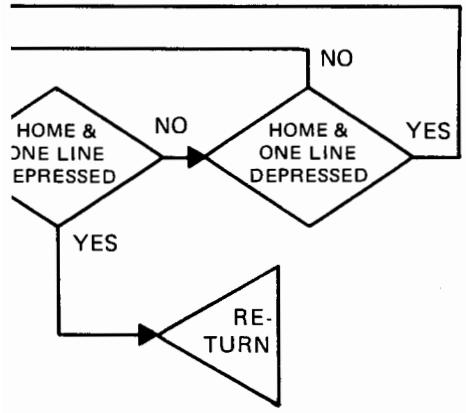






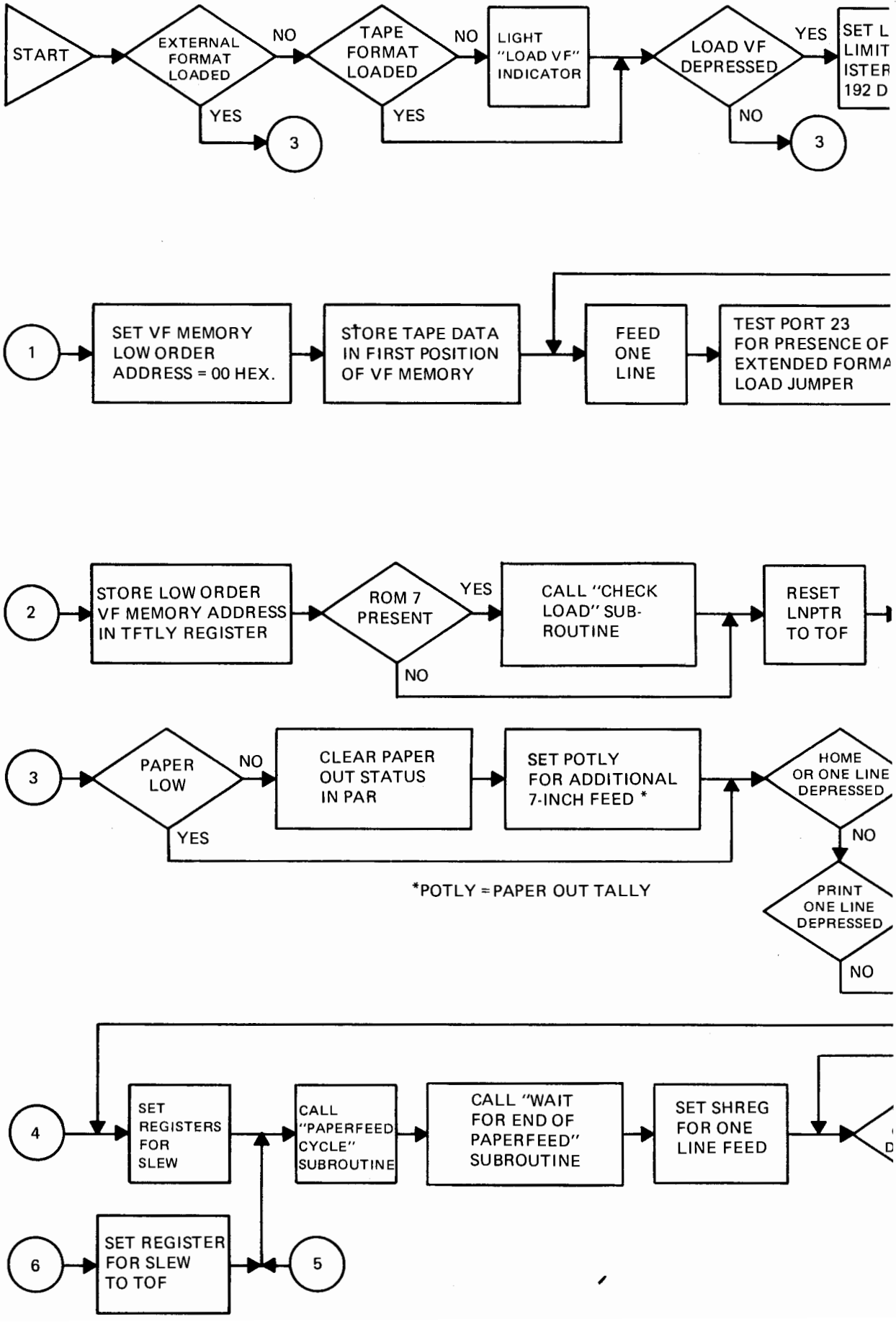


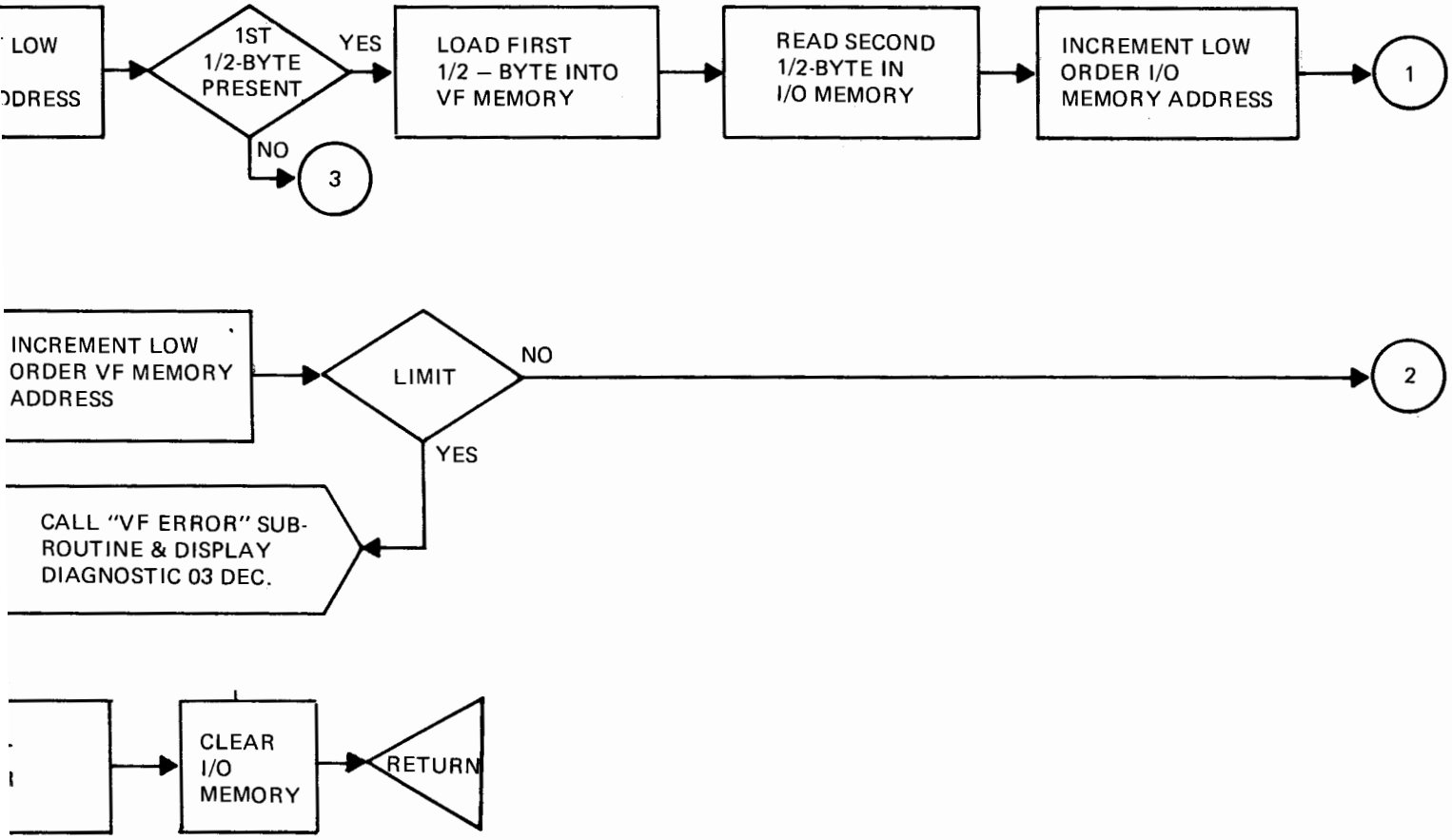




DATA PRINTER CORP.		
TITLE: VF SAMPLE ROM #5		
DWG. NO.	SHEET ___of___	REV.

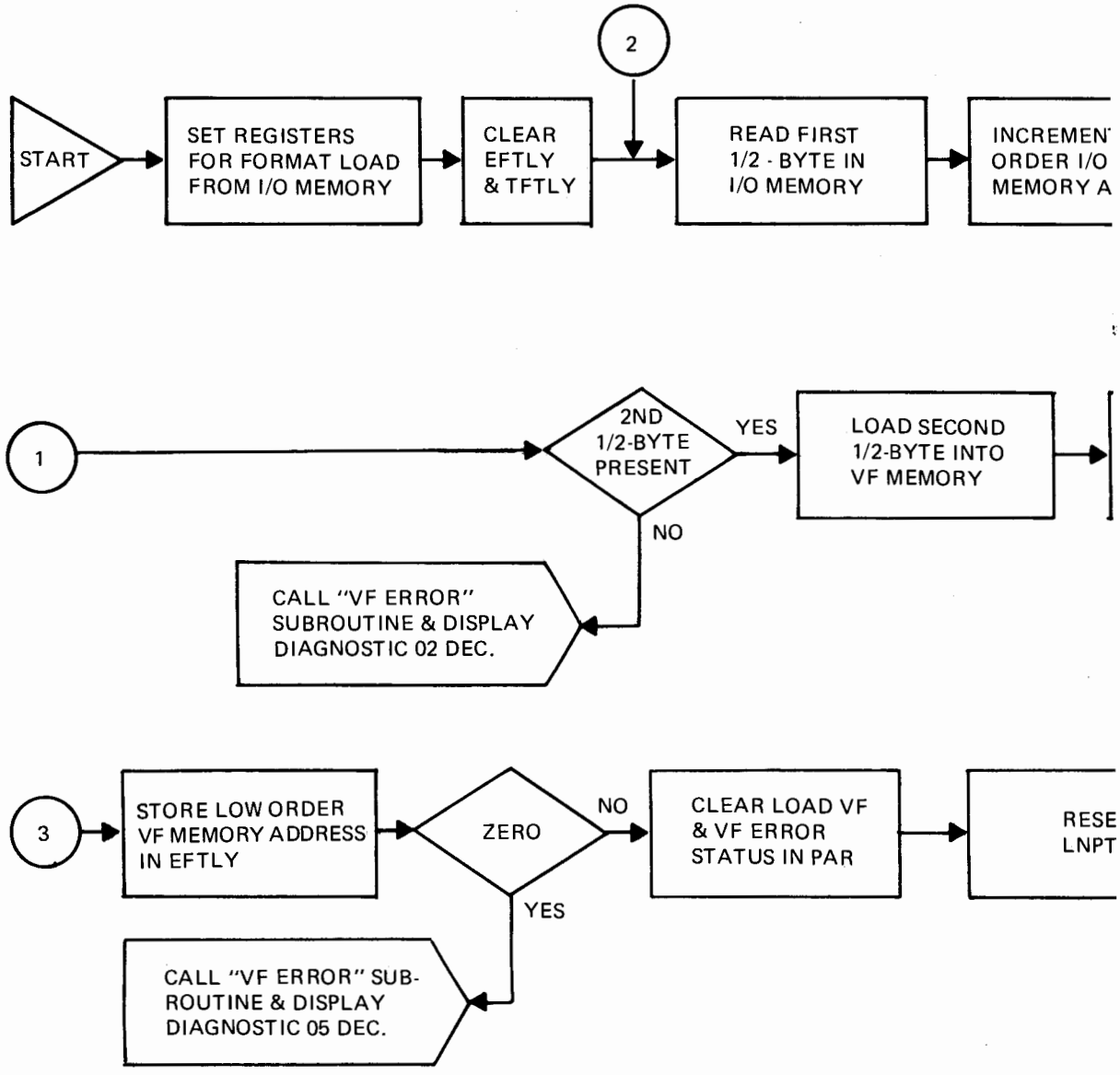
"VF SAMPLE" SUBROUTINE

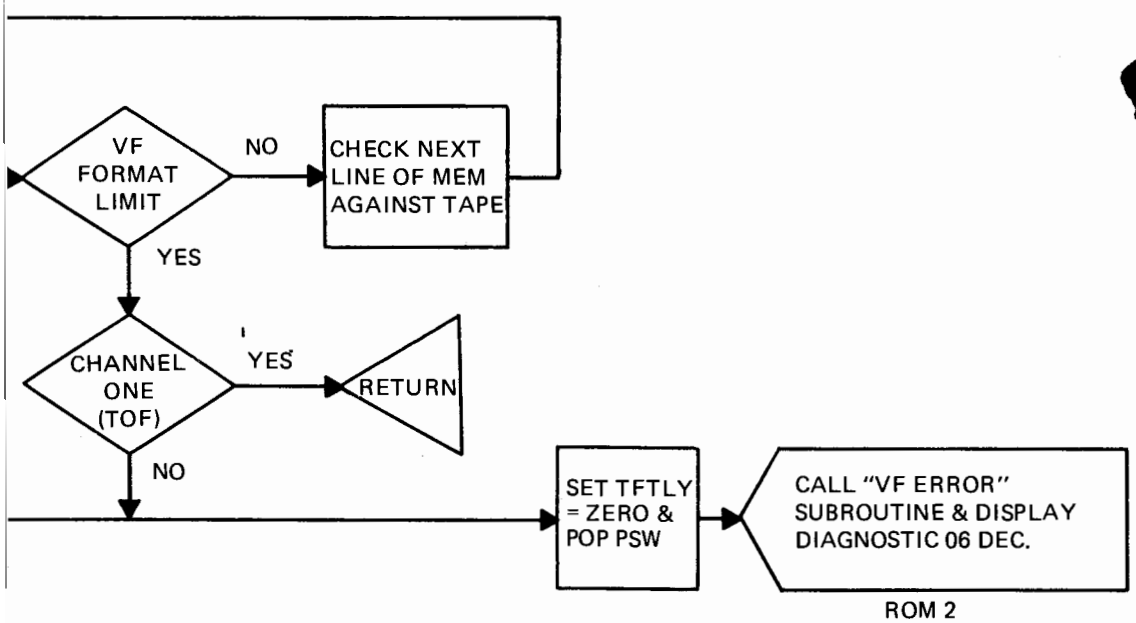




DATA PRINTER CORP.		
TITLE VF SAMPLE ROM #5		
DWG. NO.	SHEET __of__	REV.

"EXTERNAL FORMAT LOAD" SUBROUTINE

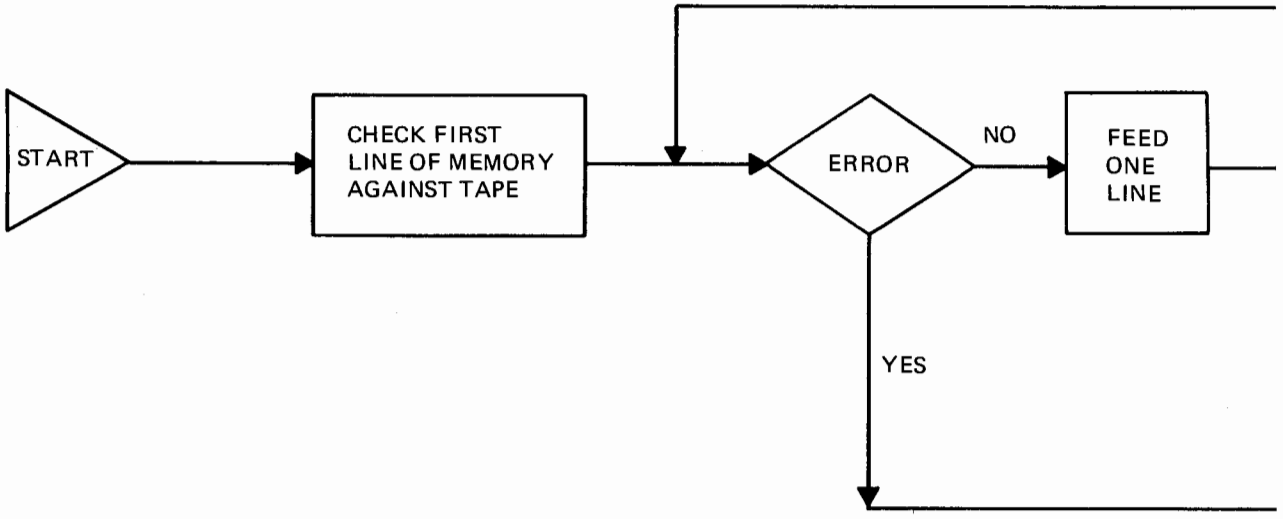




ROM 2

DATA PRINTER CORP.		
TITLE: CHECK LOAD ROM #7		
DWG. NO.	SHEET 1 of	REV.

"CHECK LOAD" SUBROUTINE



APPENDIX B
DIAGNOSTIC ERROR CODES

Examination of the flow charts in Appendix A reveals that numerous self-diagnostic routines have been incorporated into the operating program. When one of these routines detects an error it illuminates "V.F. ERROR" or "CALL SERV" (whichever is appropriate) and displays a binary error code on five Diagnostic LED's, located on the CPU Board (IPB 67-16 and CD 2.3.0). The LED's, which are visible through the plastic panel at the rear of the printer, have the meanings shown in Table B-1 when "CALL SERV" is illuminated and the meanings shown in Table B-2 when "V.F. ERROR" is illuminated. Table 3-8 in the Maintenance Instructions manual (DPC Form 1260/90/10-3) lists possible causes and recommended corrective action for the "CALL SERV" diagnostics.

Table B-1. "CALL SERV" Diagnostic Error Codes.

Decimal Value	Binary Error Code (LED 5 4 3 2 1)	Meaning
1	0 0 0 0 1	Extended Matrix Memory Test Error
2	0 0 0 1 0	Standard Matrix Memory Test Error
3	0 0 0 1 1	Scratch Pad and Matrix Extension Memory Test Error
4	0 0 1 0 0	Stack and 8 Ch. VFU Memory Test Error
5	0 0 1 0 1	Twelve-Channel VFU Memory Test Error
6	0 0 1 1 0	I/O Memory Test Error
7	0 0 1 1 1	ROM 1 Checksum Error
8	0 1 0 0 0	ROM 2 Checksum Error
9	0 1 0 0 1	ROM 3 Checksum Error
10	0 1 0 1 0	ROM 4 Checksum Error
11	0 1 0 1 1	ROM 5 Checksum Error
12	0 1 1 0 0	ROM 6 Checksum Error
13	0 1 1 0 1	ROM 7 Checksum Error

Decimal Value	Binary Error Code LED 5 4 3 2 1	Meaning
14	0 1 1 1 0	Not Used
15	0 1 1 1 1	Not Used
16	1 0 0 0 0	Stepper Initialization Error
17	1 0 0 0 1	Hardware Timer Test Error
18	1 0 0 1 0	Clear I/O Memory Error
19	1 0 0 1 1	No Character Strobe
20	1 0 1 0 0	No Index Strobe
21	1 0 1 0 1	Font Count Error
22	1 0 1 1 0	Character Strobe Too Soon
23	1 0 1 1 1	Character Strobe Too Late
24	1 1 0 0 0	Paperfeed Strobe Too Late
25	1 1 0 0 1	Half-Inch Strobe Error
26	1 1 0 1 0	Font Configuration Read Error
27	1 1 0 1 1	Not Used
28	1 1 1 0 0	Paperfeed Cycle Incomplete
29	1 1 1 0 1	Not Used
30	1 1 1 1 0	Not Used
31	1 1 1 1 1	Diagnostic Decode Error (ROM 1 Fault)

Table B-2. "V.F. ERROR" Diagnostic Error Codes.

Decimal Value	Binary Error Code	Meaning
	LED 5 4 3 2 1	
01	0 0 0 0 1	No channel 1 (Top-of-Form) loaded.
02	0 0 0 1 0	No format loaded.
03	0 0 0 1 1	Only Half-line loaded (i.e., only 1 byte of 2-byte line has been loaded from external device).
04	0 0 1 0 0	No selected channel (i.e., the program has called for a channel that has no "punch").
05	0 0 1 0 1	Format too long (i.e., over 143/192 lines)
06	0 0 1 1 0	"Check Load" tape read error.

APPENDIX C
INTEL 8080A CPU AND RELATED SUPPORT DEVICE DATA SHEETS

Data sheets for the following devices are included in this appendix:

8080A	Single Chip, 8-bit Microprocessor (CPU)
8224	Clock Generator & Driver for 8080A CPU
8228	System Controller & Bus Driver for 8080A CPU
8205	High Speed 1 of 8 Binary Decoder
8212	Eight Bit Input/Output Port
8214	Priority Interrupt Control Unit

These data sheets have been reprinted from the Intel 8080 Microcomputer System User's Manual (copyright 1976) by permission of the Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051. That manual has been superseded by the MCS 80 User's Manual (Order No. 204000), which is available for $7.50 by writing to Intel at the above address. The newer manual includes the 8085 CPU and its support devices as well as the 8080A. It in no way invalidates the data sheets reprinted here from the earlier, no-longer-available manual.

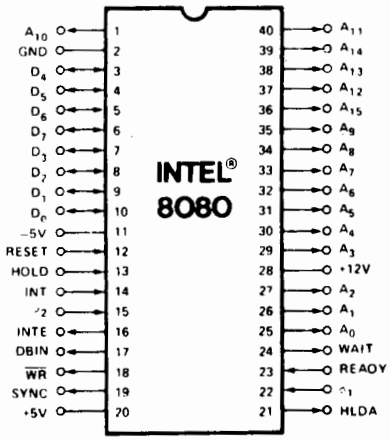
If you are unfamiliar with microcomputer systems, you might be better off with The 8080A BUGBOOK^{R}: Microcomputor Interfacing and Programming (Order No. 62-2014), which is available from your local Radio Shack^{R} store for $6.95. "BUGBOOK^{R}" is a registered trademark of E & L Instruments, Inc., Derby, Connecticut 06148. "Radio Shack^{R}" is a division of the Tandy Corporation, Fort Worth, Texas 76102.

Silicon Gate MOS 8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

The 8080 is a complete 8-bit parallel, central processor unit (CPU) for use in general purpose digital computer systems. It is fabricated on a single LSI chip (see Figure 3-1). using Intel's n-channel silicon gate MOS process. The 8080 transfers data and internal state information via an 8-bit, bidirectional 3-state Data Bus (D_0-D_7). Memory and peripheral device addresses are transmitted over a separate 16-bit 3-state Address Bus (A_0-A_{15}). Six timing and control outputs (SYNC, DBIN, WAIT, $\overline{WR}$, HLDA and INTE) emanate from the 8080, while four control inputs (READY, HOLD, INT and RESET), four power inputs (+12v, +5v, 5v, and GND) and two clock inputs (ϕ_1 and ϕ_2) are accepted by the 8080.



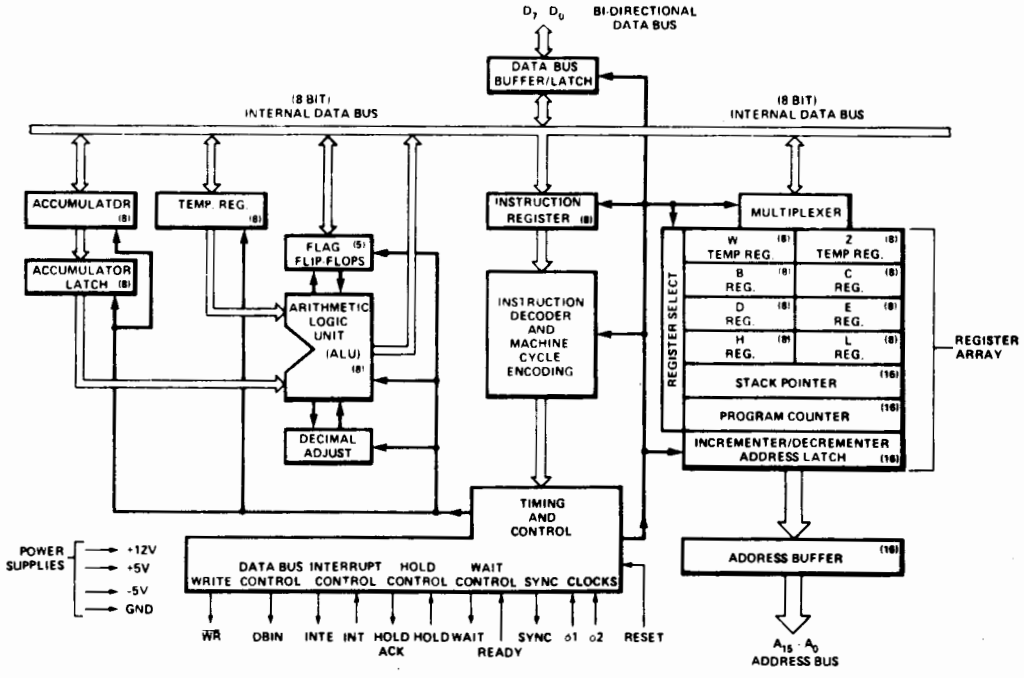


Figure 2-2. 8080 CPU Functional Block Diagram

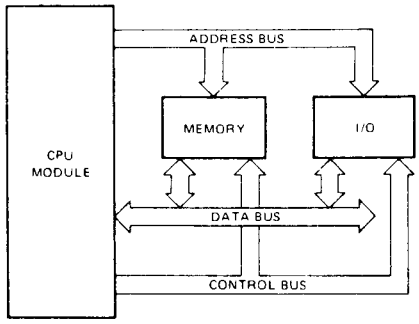


Figure 3-1. Typical Computer System Block Diagram

ARCHITECTURE OF THE 8080 CPU

The 8080 CPU consists of the following functional units:

- Register array and address logic
- Arithmetic and logic unit (ALU)
- Instruction register and control section
- Bi-directional, 3-state data bus buffer

Figure 2-2 illustrates the functional blocks within the 8080 CPU.

Registers:

The register section consists of a static RAM array organized into six 16-bit registers:

- Program counter (PC)
- Stack pointer (SP)
- Six 8-bit general purpose registers arranged in pairs, referred to as B,C; D,E; and H,L
- A temporary register pair called W,Z

The program counter maintains the memory address of the current program instruction and is incremented automatically during every instruction fetch. The stack pointer maintains the address of the next available stack location in memory. The stack pointer can be initialized to use any portion of read-write memory as a stack. The stack pointer is decremented when data is "pushed" onto the stack and incremented when data is "popped" off the stack (i.e., the stack grows "downward").

The six general purpose registers can be used either as single registers (8-bit) or as register pairs (16-bit). The temporary register pair, W,Z, is not program addressable and is only used for the internal execution of instructions.

Eight-bit data bytes can be transferred between the internal bus and the register array via the register-select multiplexer. Sixteen-bit transfers can proceed between the register array and the address latch or the incrementer/decrementer circuit. The address latch receives data from any of the three register pairs and drives the 16 address output buffers (A_0-A_{15}), as well as the incrementer/decrementer circuit. The incrementer/decrementer circuit receives data from the address latch and sends it to the register array. The 16-bit data can be incremented or decremented or simply transferred between registers.

Arithmetic and Logic Unit (ALU):

The ALU contains the following registers:

- An 8-bit accumulator
- An 8-bit temporary accumulator (ACT)
- A 5-bit flag register: zero, carry, sign, parity and auxiliary carry
- An 8-bit temporary register (TMP)

Arithmetic, logical and rotate operations are performed in the ALU. The ALU is fed by the temporary register (TMP) and the temporary accumulator (ACT) and carry flip-flop. The result of the operation can be transferred to the internal bus or to the accumulator, the ALU also feeds the flag register.

The temporary register (TMP) receives information from the internal bus and can send all or portions of it to the ALU, the flag register and the internal bus.

The accumulator (ACC) can be loaded from the ALU and the internal bus and can transfer data to the temporary accumulator (ACT) and the internal bus. The contents of the accumulator (ACC) and the auxiliary carry flip-flop can be tested for decimal correction during the execution of the DAA instruction

Instruction Register and Control:

During an instruction fetch, the first byte of an instruction (containing the OP code) is transferred from the internal bus to the 8-bit instruction register.

The contents of the instruction register are, in turn, available to the instruction decoder. The output of the decoder, combined with various timing signals, provides the control signals for the register array, ALU and data buffer blocks. In addition, the outputs from the instruction decoder and external control signals feed the timing and state control section which generates the state and cycle timing signals.

Data Bus Buffer:

This 8-bit bidirectional 3-state buffer is used to isolate the CPU's internal bus from the external data bus (D_0 through D_7). In the output mode, the internal bus content is loaded into an 8-bit latch that, in turn, drives the data bus output buffers. The output buffers are switched off during input or non-transfer operations.

During the input mode, data from the external data bus is transferred to the internal bus. The internal bus is precharged at the beginning of each internal state, except for the transfer state

SILICON GATE MOS 8080A

8080A FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

WR (output)
WRITE; the WR signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

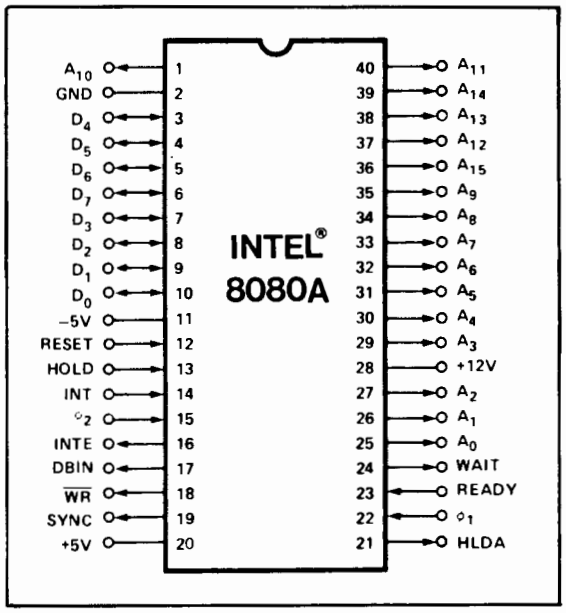
- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.



Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST, the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input)[1]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

Schottky Bipolar 8224

CLOCK GENERATOR AND DRIVER FOR 8080A CPU

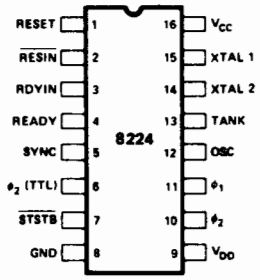
- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

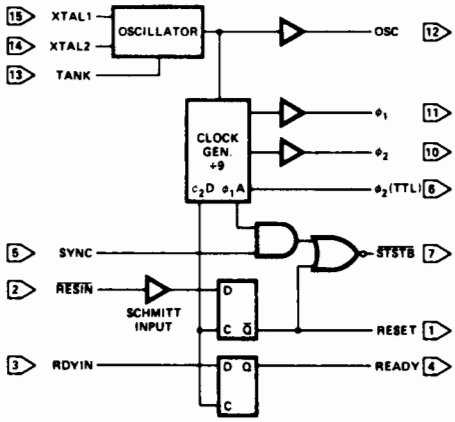
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
φ1	8080 CLOCKS
φ2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
φ2 (TTL)	φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

SCHOTTKY BIPOLAR 8224

FUNCTIONAL DESCRIPTION

General

The 8224 is a single chip Clock Generator/Driver for the 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions.

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the 8080A is to be run at. Basically, the oscillator operates at 9 times the desired processor speed.

A simple formula to guide the crystal selection is:

$$\text{Crystal Frequency} = \frac{1}{t_{CY}} \text{ times } 9$$

Example 1: (500ns t_{CY})
2mHz times 9 = 18mHz*

Example 2: (800ns t_{CY})
1.25mHz times 9 = 11.25mHz

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has much lower "gain" than the fundamental type so an external LC network is necessary to provide the additional "gain" for proper oscillator operation. The external LC network is connected to the TANK input and is AC coupled to ground. See Figure 4.

The formula for the LC network is:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

The output of the oscillator is buffered and brought out on ΦSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

*When using crystals above 10mHz a small amount of frequency "trimming" may be necessary to produce the exact desired frequency. The addition of a small selected capacitance (3pF - 10pF) in series with the crystal will accomplish this function.

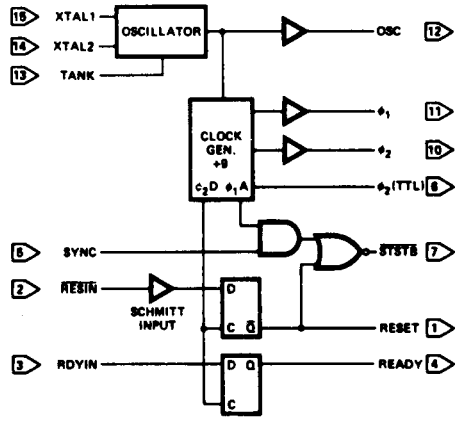
Clock Generator

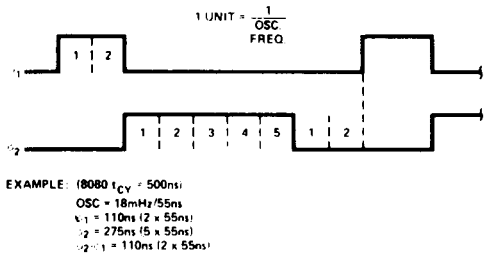
The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two 8080A clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; phase 1 and phase 2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the 8080A CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependant activities. This signal is used to gate the requesting device onto the bus once the 8080A CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe ($\overline{STSTB}$) is achieved.





SCHOTTKY BIPOLAR 8224

$\overline{\text{STSTB}}$ (Status Strobe)

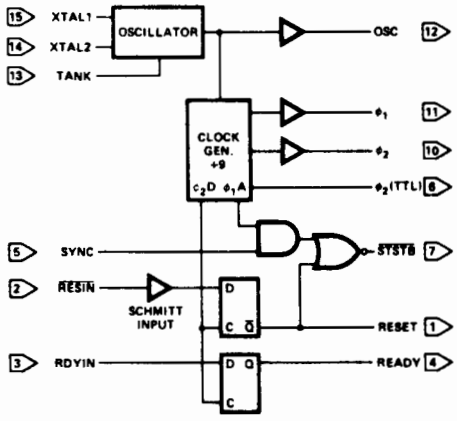
At the beginning of each machine cycle the 8080A CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ1A), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{\text{STSTB}}$ signal connects directly to the 8228 System Controller.

The power-on Reset also generates $\overline{\text{STSTB}}$, but of course, for a longer period of time. This feature allows the 8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

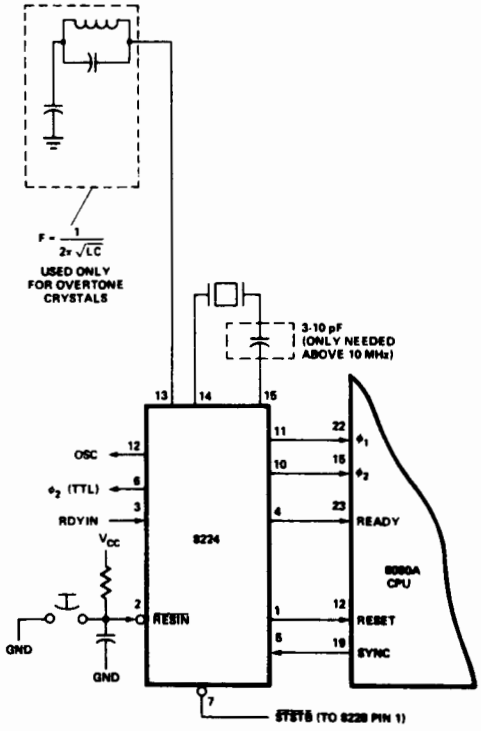
A common function in 8080A Microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The 8224 has a built in feature to accomplish this feature.

An external RC network is connected to the $\overline{\text{RESIN}}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ2D (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the 8080A input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the $\overline{\text{RESIN}}$ input in addition to the power-on RC net-network.



The READY input to the 8080A CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The 8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ2D, a synchronized READY signal at the correct input level, can be connected directly to the 8080A.

The reason for requiring an external flip-flop to synchronize the "wait request" rather than internally in the 8080 CPU is that due to the relatively long delays of MOS logic such an implementation would "rob" the designer of about 200ns during the time his logic is determining if a "wait" is necessary. An external bipolar circuit built into the clock generator eliminates most of this delay and has no effect on component count.



Schottky Bipolar 8228

SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS-80 Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**

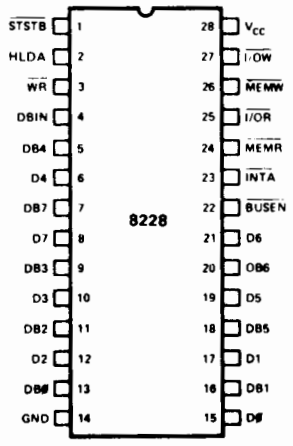
The 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems deisgner to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

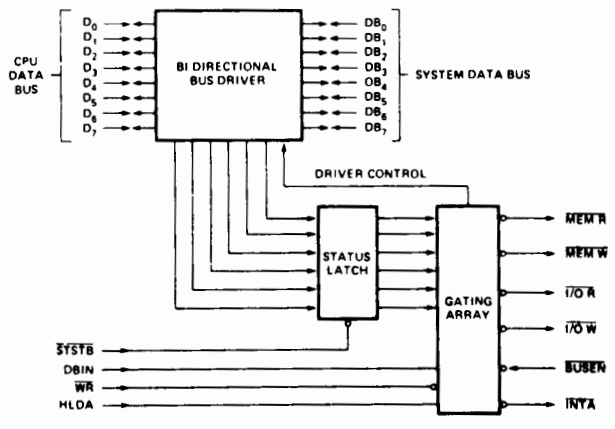
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



8228 BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/OR	I/O READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	VCC	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

SCHOTTKY BIPOLAR 8228

FUNCTIONAL DESCRIPTION

General

The 8228 is a single chip System Controller and Data Bus driver for the 8080 Microcomputer System. It generates all control signals required to directly interface MCS-80™ family RAM, ROM, and I/O components.

Schottky Bipolar technology is used to maintain low delay times and provide high output drive capability to support small to medium systems.

Bi-Directional Bus Driver

An eight bit, bi-directional bus driver is provided to buffer the 8080 data bus from Memory and I/O devices. The 8080A data bus has an input requirement of 3.3 volts (min) and can drive (sink) a maximum current of 1.9mA. The 8228 data bus driver assures that these input requirements will be not only met but exceeded for enhanced noise immunity. Also, on the system side of the driver adequate drive current is available (10mA Typ.) so that a large number of Memory and I/O devices can be directly connected to the bus.

The Bi-Directional Bus Driver is controlled by signals from the Gating Array so that proper bus flow is maintained and its outputs can be forced into their high impedance state (3-state) for DMA activities.

Status Latch

At the beginning of each machine cycle the 8080 CPU issues "status" information on its data bus that indicates the type of activity that will occur during the cycle. The 8228 stores this information in the Status Latch when the $\overline{STSTB}$ input goes "low". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array

The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch with signals from the 8080 CPU (DBIN, $\overline{WR}$, and HLDA).

The "read" control signals ($\overline{MEM\ R}$, $\overline{I/O\ R}$ and $\overline{INTA}$) are derived from the logical combination of the appropriate Status Bit (or bits) and the DBIN input from the 8080 CPU.

The "write" control signals ($\overline{MEM\ W}$, $\overline{I/O\ W}$) are derived from the logical combination of the appropriate Status Bit (or bits) and the $\overline{WR}$ input from the 8080 CPU.

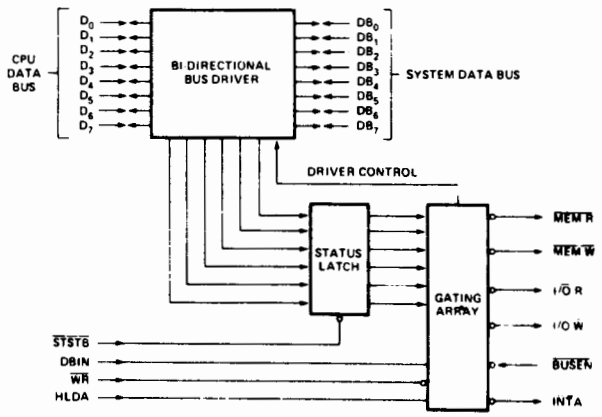
All Control Signals are "active low" and directly interface to MCS-80 family RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the 8228. If only one basic vector is needed in the interrupt structure, such as in small systems, the 8228 can automatically insert a RST 7 instruction onto the bus at the proper time. To use this option, simply connect the $\overline{INTA}$ output of the 8228 (pin 23) to the +12 volt supply through a series resistor (1K ohms). The voltage is sensed internally by the 8228 and logic is "set-up" so that when the DBIN input is active a RST 7 instruction is gated on to the bus when an interrupt is acknowledged. This feature provides a single interrupt vector with no additional components, such as an interrupt instruction port.

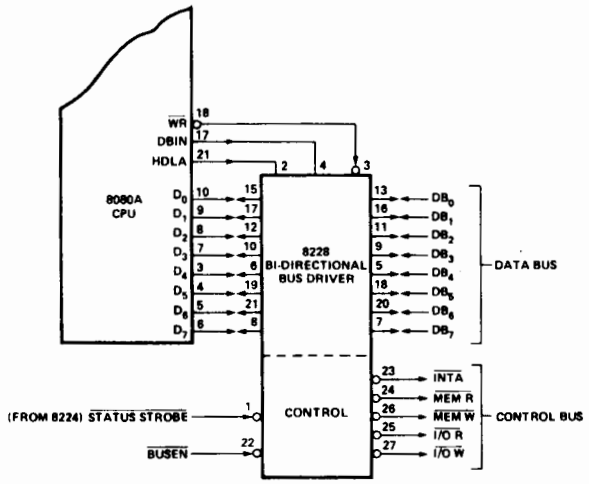
When using CALL as an Interrupt instruction the 8228 will generate an $\overline{INTA}$ pulse for each of the three bytes.

The $\overline{BUSEN}$ (Bus Enable) input to the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "one". If $\overline{BUSEN}$ is a "zero" normal operation of the data buffer and control signals take place.

8228 BLOCK DIAGRAM



SCHOTTKY BIPOLAR 8228



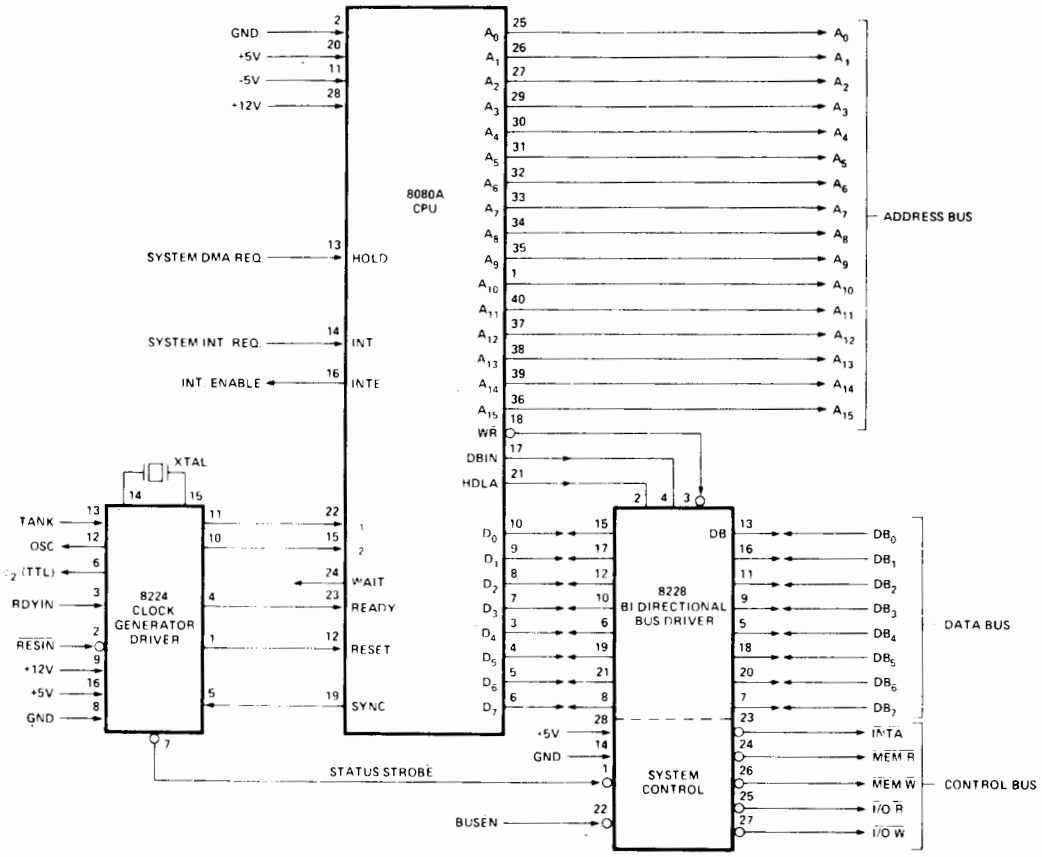
STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INTERRUPT ACKNOWLEDGE WHILE HALT
											Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

CONTROL SIGNALS:
- $\overline{INTA}$
- (NONE)
- $\overline{INTA}$
- $\overline{I/O\ W}$
- $\overline{I/O\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ R}$

SCHOTTKY BIPOLAR 8228



8080A CPU Standard Interface

Schottky Bipolar 8205

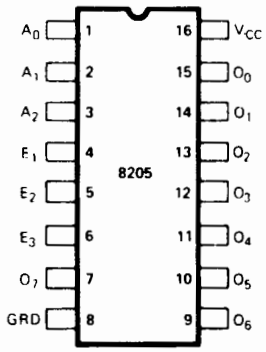
HIGH SPEED 1 OUT OF 8 BINARY DECODER

- **I/O Port or Memory Selector**
- **Simple Expansion — Enable Inputs**
- **High Speed Schottky Bipolar Technology — 18ns Max. Delay**
- **Directly Compatible with TTL Logic Circuits**
- **Low Input Load Current — .25 mA max., 1/6 Standard TTL Input Load**
- **Minimum Line Reflection — Low Voltage Diode Input Clamp**
- **Outputs Sink 10 mA min.**
- **16-Pin Dual-In-Line Ceramic or Plastic Package**

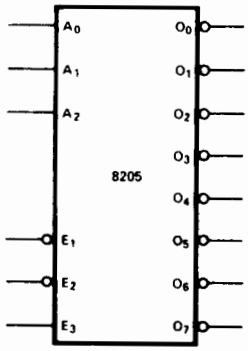
The 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive eight other decoders for arbitrary memory expansions.

The Intel® 8205 is packaged in a standard 16 pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0-A_2	ADDRESS INPUTS
$\overline{E_1}$-$\overline{E_3}$	ENABLE INPUTS
$\overline{O_0}$-$\overline{O_7}$	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

SCHOTTKY BIPOLAR 8205

FUNCTIONAL DESCRIPTION

Decoder

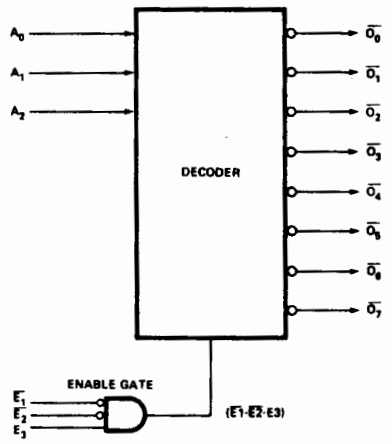
The 8205 contains a one out of eight binary decoder. It accepts a three bit binary code and by gating this input, creates an exclusive output that represents the value of the input code.

For example, if a binary code of 101 was present on the A0, A1 and A2 address input lines, and the device was enabled, an active low signal would appear on the $\overline{O5}$ output line. Note that all of the other output pins are sitting at a logic high, thus the decoded output is said to be exclusive. The decoders outputs will follow the truth table shown below in the same manner for all other input variations.

Enable Gate

When using a decoder it is often necessary to gate the outputs with timing or enabling signals so that the exclusive output of the decoded value is synchronous with the overall system.

The 8205 has a built-in function for such gating. The three enable inputs ($\overline{E1}$, $\overline{E2}$, E3) are ANDed together and create a single enable signal for the decoder. The combination of both active "high" and active "low" device enable inputs provides the designer with a powerfully flexible gating function to help reduce package count in his system.



ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

Schottky Bipolar 8212

EIGHT-BIT INPUT/OUTPUT PORT

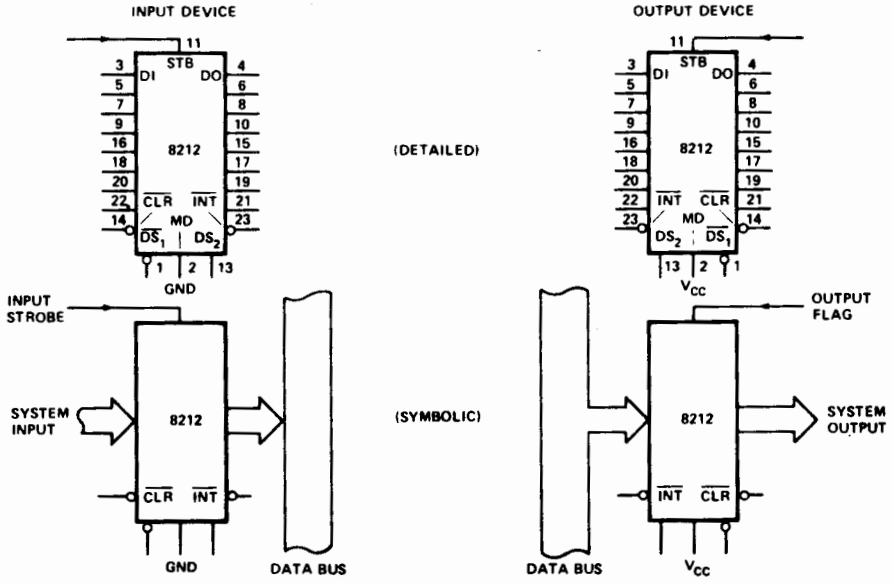
The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

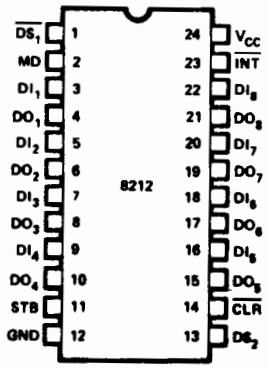
I. Basic Schematic Symbols

Two examples of ways to draw the 8212 on system schematics—(1) the top being the detailed view showing pin numbers, and (2) the bottom being the symbolic view showing the system input or output as a system bus (bus containing 8 parallel lines). The output to the data bus is symbolic in referencing 8 parallel lines.

BASIC SCHEMATIC SYMBOLS



PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

SCHOTTKY BIPOLAR 8212

Functional Description

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

This high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

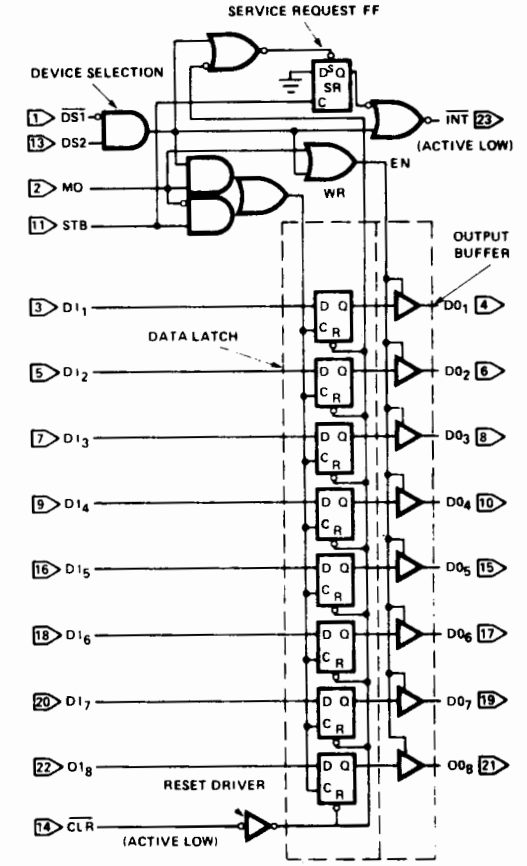
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	(DS_1, DS_2)	DATA OUT EQUALS
0	0	0	3-STATE
1	0	0	3-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR	(DS_1, DS_2)	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	1	~	0	0
1	1	0	1	0
1	0	0	1	1
1	1	~	1	0

*INTERNAL SR FLIP FLOP

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP FLOP
(NO EFFECT ON OUTPUT BUFFER)

Schottky Bipolar 8214

PRIORITY INTERRUPT CONTROL UNIT

- **Eight Priority Levels**
- **Current Status Register**
- **Priority Comparator**
- **Fully Expandable**
- **High Performance (50ns)**
- **24-Pin Dual In-Line Package**

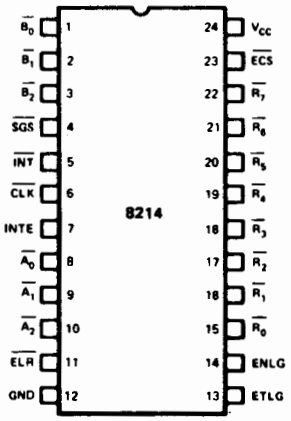
The 8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

The 8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

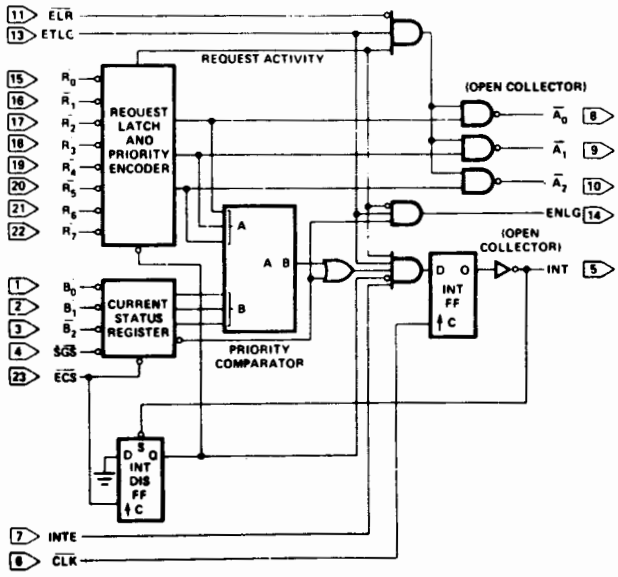
PIN CONFIGURATION



PIN NAMES

INPUTS	
$\overline{A_0}$-$\overline{A_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS
$\overline{SGS}$	STATUS GROUP SELECT
$\overline{ECS}$	ENABLE CURRENT STATUS
INTE	INTERRUPT ENABLE
$\overline{CLK}$	CLOCK (INT F-F)
$\overline{ELR}$	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS	
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS (OPEN COLLECTOR)
$\overline{INT}$	INTERRUPT (ACT. LOW) (OPEN COLLECTOR)
ENLG	ENABLE NEXT LEVEL GROUP

LOGIC DIAGRAM



SCHOTTKY BIPOLAR 8214

FUNCTIONAL DESCRIPTION

General

The 8214 is a device specifically designed for use in real time, interrupt driven, microcomputer systems. Basically it is an eight (8) level priority control unit that can accept eight different interrupt requests, determine which has the highest priority, compare that level to a software maintained current status register and issue an interrupt to the system based on this comparison along with vector information to indicate the location of the service routine.

Priority Encoder

The eight requests inputs, which are active low, come into the Priority Encoder. This circuit determines which request input is the most important (highest priority) as preassigned by the designer. ($\overline{R7}$) is the highest priority input to the 8214 and ($\overline{R0}$) is the lowest. The logic of the Priority Encoder is such that if two or more input levels arrive at the same time then the input having the highest priority will take presidence and a three bit output, corresponding to the active level (modulo 8) will be sent out. The Priority Encoder also contains a latch to store the request input. This latch is controlled by the Interrupt Disable Flip-flop so that once an interrupt has been issued by the 8214 the request latch is no longer open. (Note that the latch does not store inactive requests. In order for a request to be monitored by the 8214 it must remain present until it has been serviced.)

Current Status Register

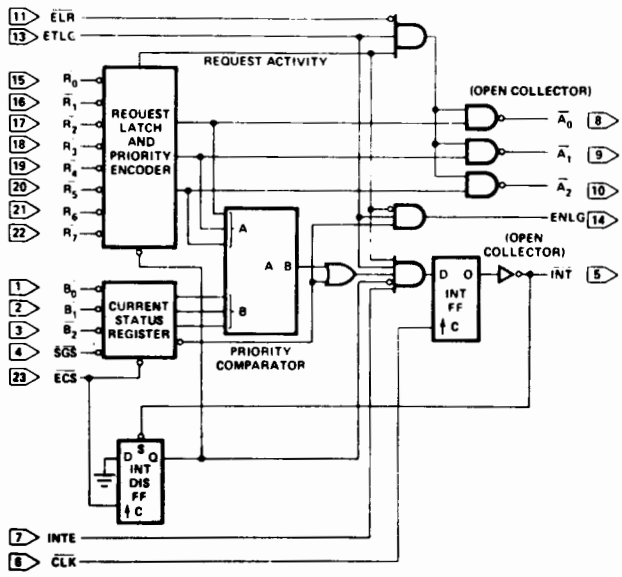
In an interrupt driven microcomputer system it is important to not only prioritize incoming requests but to ascertain whether such a request is a higher priority than the interrupt currently being serviced.

The Current Status Register is a simple 4-bit latch that is treated as an addressable outport port by the microcomputer system. It is loaded when the $\overline{ECS}$ input goes low.

Maintenance of the Current Status Register is performed as a portion of the service routine. Basically, when an interrupt is issued to the system the programmer outputs a binary code (modulo 8) that is the compliment of the interrupt level. This value is stored in the Current Status Register and is compared to all further prioritized incoming requests by the Priority Comparator. In essence, a copy of the current interrupt level is written into the 8214 to be used as a reference for comparison. There is no restriction to this maintenance, other level values can be written into this register as references so that groups of interrupt requests may be disallowed under complete control of the programmer.

Note that the fourth bit in the register is $\overline{SGS}$. This input is part of the value written out by the programmer and performs a special function. The Priority Comparator will only issue an output that indicates the request level is greater than the Current Status Register. If both comparator inputs are equal to zero no output will be present. The $\overline{SGS}$ input allows the programmer to, in effect, disable this comparison and allow the 8214 to issue an interrupt to the system that is based only on the logic of the priority encoder.

LOGIC DIAGRAM



SCHOTTKY BIPOLAR 8214

Control Signals

The 8214 also has several inputs that enable the designer to synchronize the interrupt issued to the microprocessor and to allow or disallow such an issuance. Also, signals are provided that permit simple expansion to other 8214s so that more than eight levels can be controlled.

INTE, $\overline{CLK}$

The INTE (Interrupt Enable) input allows the designer to "shutoff" the interrupt system under control of external logic or possibly under software maintenance. A "zero" on this line will not allow interrupts to be issued to the microcomputer system.

The $\overline{CLK}$ (Clock) input is actually the trigger that strobes the Interrupt Flip-Flop. It can be connected to one of the clocks of the microprocessor so that the interrupt issued meets the CPU set-up time specification. Note that due to the gating of the input to the Interrupt Flip-Flop the $\overline{INT}$ output will only be active for the time of a single clock period, so external latching may be required to hold this signal.

$\overline{ELR}$, ETLG, ENGL

These three signals allow 8214s to be cascaded so that more than eight levels of interrupt requests can be controlled.

Basically, the ENLG output of one 8214 is connected to the ETLG input of the next and so on, with the first 8214 having its ETLG input pulled "high" and assigned the highest priority. When the ENLG output is "high" it indicates that there is no interrupt pending on that device and that interrupts can be monitored on the next lower priority 8214.

This "cascading" can be expanded almost indefinitely to accomodate even the largest of interrupt driven system architectures.

$\overline{A0}$, $\overline{A1}$, $\overline{A2}$

In order to identify which device has interrupted the processor so that the service routine associated with it can be addressed, a pointer or "vector" must accompany the interrupt issued to the microcomputer system.

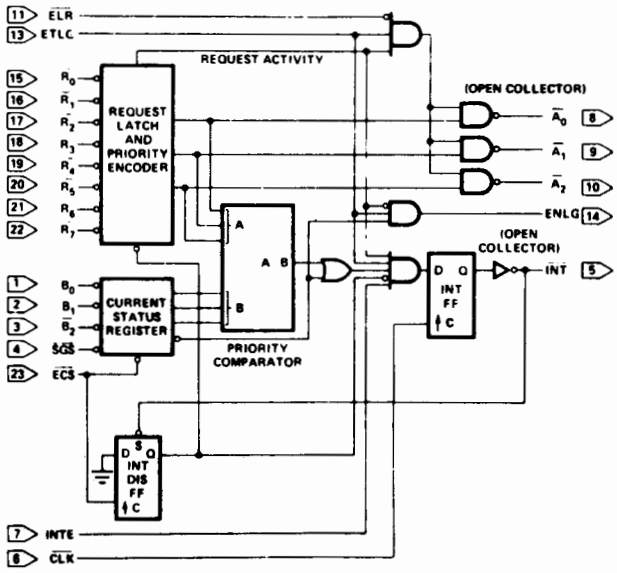
The $\overline{A0}$, $\overline{A1}$ and $\overline{A2}$ outputs represent the complement of the active interrupt level (modulo 8). By using these signals to encode the special instruction, RST, the program counter of the microprocessor, can point to the location of the service routine. Note that these three outputs are gated by the $\overline{ELR}$ input and are open collector so that expansion is simplified.

$\overline{INT}$

The $\overline{INT}$ output of the 8214 is the signal that is issued to the microprocessor to initiate the interrupt sequence. As soon a $\overline{INT}$ is active the INT DIS FF is set, inhibiting further requests from entering the Request Latch. Only the writing out of the current status information by strobing the $\overline{ECS}$ input will clear the INT DIS FF and allow requests to enter the latch.

Note that $\overline{INT}$ is also open collector so that when cascaded to other 8214s an interrupt in any of the active devices will set all INT DIS FFs in the entire array.

LOGIC DIAGRAM



APPENDIX D
ABBREVIATIONS

-A-

A	ADDRESS BUS (8080 SIDE)
A_0-A_2	REQUEST LEVELS (OUTPUT 8214)
AB	ADDRESS BUS (SYSTEM SIDE)
ACN	AC NEUTRAL
ADL	LOW ORDER ADDRESS
ADH	HIGH ORDER ADDRESS

-B-

BOF	BOTTOM-OF-FORM
BUSEN	BUSS ENABLE
B_0-B_2	CURRENT STATUS (8214)

-C-

CE	CHIP ENABLE
CH	CHANNEL
CHAR	CHARACTER
CHN	CHAIN
CLK	CLOCK
CLR	CLEAR
CMD	COMMAND
CNT	COUNT
CNTR	COUNTER
CNTR Vcc	CONTROLLED Vcc
CPU	8080A MICROPROCESSOR
CS	CHIP SELECT
CSTB	CHARACTER STROBE
CT	CHAIN TRAIN

-D-

D	DATA BUS (8080 SIDE)
DB	DATA BUS (SYSTEM SIDE)
DBIN	DATA BUS IN
DC	DIRECT CURRENT
DI	DATA IN
DMA	DIRECT MEMORY ACCESS
DO	DATA OUTPUT
DS	DEVICE SELECT

-E-

E	ENABLE
ECS	ENABLE CURRENT STATUS
EFTLY	EXTERNAL FORMAT TALLY
ELR	ENABLE LEVEL READ
EN	ENABLE
ENLG	ENABLE NEXT LEVEL GROUP
ETLG	ENABLE THIS LEVEL GROUP

-F-

FBP	FEED BEFORE PRINT
FLSSW	FORM LENGTH SELECTOR SWITCH
FMTLY	FORMAT TALLY
FP	FIRE PULSE

-G-

GND	GROUND

-H-

HD	HAMMER DRIVER
HDSR	HAMMER DRIVER SHIFT REG.
HI	HIGH (LOGICAL "1")
HLD	HOLD
HLDA	HOLD ACKNOWLEDGE
HOVFUEN	HIGH ORDER VFU ENABLE
HS	HIGH SPEED

-I-

IN	INCH
INC I(+)	INCREASE CURRENT TO STEPPER MOTOR (CD 4.0.0)
IND	INDICATOR
INDEX	INDEX STROBE
INH	INHIBIT
INP	INPUT
INT	INTERRUPT
INTA	INTERRUPT ACKNOWLEDGE
INTE	INTERRUPT ENABLE
INTLK	INTERLOCK
I/O	INPUT/OUTPUT
I/OP	INPUT/OUTPUT PORT
I/OR	INPUT/OUTPUT READ

I/O RW	INPUT/OUTPUT, READ WRITE
I/OW	INPUT/OUTPUT WRITE

-L-

LED	LIGHT EMITTING DIODE
LD	LOAD
LO	LOW (LOGICAL "0")
LNPTR	LINE POINTER
LPI	LINES PER INCH
LS	LOW SPEED
LSI-HDCC	LSI HAMMER DRIVER CONTROL CIRCUIT IC

-M-

MD	MODE
MEM	MEMORY (ADDRESS LINES TO RAM)
MEMR	MEMORY READ
MEMW	MEMORY WRITE
MOT	MOTOR
MROCA	MOTOR RUN OPTICAL COUPLER ANODE
MROCC	MOTOR RUN OPTICAL COUPLER CATHODE
MSOCA	MOTOR START OPTICAL COUPLER ANODE
MSOCC	MOTOR START OPTICAL COUPLER CATHODE

-O-

O	OUTPUT
OD	OUTPUT DISABLE
OSC	OSCILLATOR
OX(+)	ZERO CROSS PULSE

-OTHER-

Ø	PHASE

-P-

PAP	PAPER
PAR	PENDING ALARM REGISTER
PC	PRINTED CIRCUIT
PEN	PORT ENABLE
PF	PAPERFEED
PFREG	PAPERFEED REGISTER
PFLD	PAPERFEED LOAD
PICU	PRIORITY INTERRUPT CONTROL UNIT
POP PSW	POP PROGRAM STATUS WORD MNEMONIC
PR	PRINTER
PRG SEL	PROGRAM SELECT
PRO SEL	PROGRAM SELECT
PROG	PROGRAM
PSOCA	POWER SUPPLY OPTICAL COUPLER ANODE
PSOCC	POWER SUPPLY OPTICAL COUPLER CATHODE

-R-

R_0-R_7	REQUEST LEVELS (8214)
RAM	RANDOM ACCESS MEMORY
RD	READ (TO RAM)
RDY	READY
REN	ROM ENABLE
REQ	REQUEST
RES	RESET
RIB	RIBBON
RMOCA	RIBBON MOTOR OPTICAL COUPLER ANODE
RMOCC	RIBBON MOTOR OPTICAL COUPLER CATHODE
ROM	READ ONLY MEMORY
RST	RESET
RTN	RETURN
R/W	READ/WRITE
RWAY	RUNAWAY

-S-

SERV	SERVICE
SGS	STATUS GROUP SELECT
SHREG	SLEW HOME REGISTER
SP	SPARE
SP	SPEED
SPEN	SCRATCH PAD MEMORY ENABLE
SS	SINGLE SPACE
STB	STROBE
STSTB	STATUS STROBE
SW	SWITCH
SYNC	SYNCHRONIZING SIGNAL

-T-

TA	TIMER ADDRESS
TCE	TIMER CHIP ENABLE
TEN	I/O MEMORY ENABLE
TFTLY	TAPE FORMAT TALLY
T MEM	I/O MEMORY
TOD	TIMER OUTPUT DISABLE
TOF	TOP-OF-FORM
TR/W	TIMER READ/WRITE
TTL	TRANSISTOR TRANSISTOR LOGIC

-V-

V	VOLTAGE
V_{BB}	-5VDC
V_{CC}	+5VDC
V_{DD}	+12VDC
V_G	1K RESISTOR TO Vcc
V_{GB}	1.8K RESISTOR TO Vcc
V_S	+5VDC FROM T1 (CD 3.0.0)
V_{SG}	1.8K RESISTOR TO V_S
V_{SS}	DC RETURN
VFSEN	VERTICAL FORMAT SENSE ENABLE
VFU	VERTICAL FORMAT UNIT TAPE READER

-W-

WR	WRITE

-X-

XTAL	CRYSTAL