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Motorola 68040

information and customer presentation materials for the Motorola 68040

Field Training Manual
April 1990
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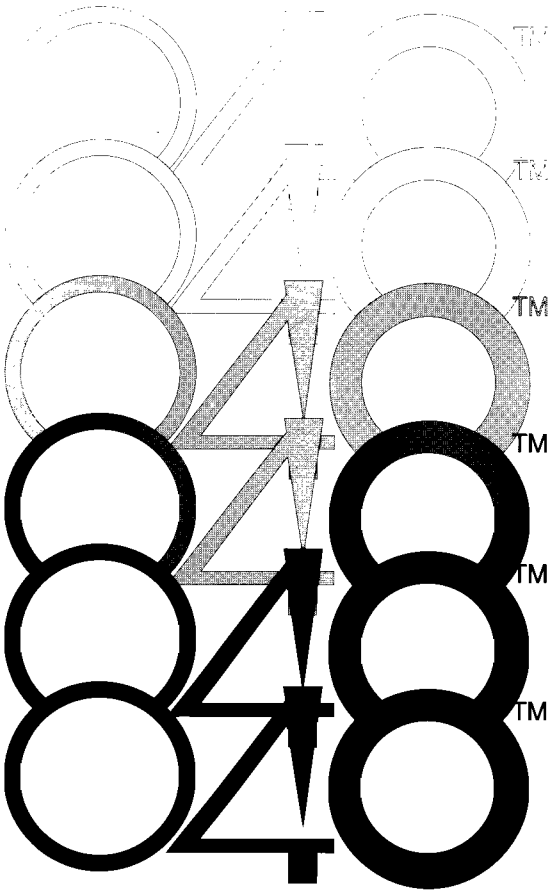

Table of Contents

Introduction

This 68040 Field Training Manual is provided so that you have 040 sales tools which you can start using today! It contains copies of Motorola 68040 slides along with a story board - a presentation which has been designed to help you and your customers understand the advantages the 040 will provide. Please keep in mind that this information has been gathered from Motorola introduction materials and is not necessarily guaranteed by Hewlett-Packard. Performance figures quoted for the 68040 chip do not necessarily guarantee performance levels for HP workstations based on this chip.

Motorola has given HP permission to include in this FTM the slides they used during the 68040 introduction, and you may use them in your presentations. RSSMs told us that they will be of most use to you if you can use the actual Motorola slides by thermofaxing these copies.

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"Motorola's 68040 Boost for Mac, NeXT, and HP/Apollo", *Personal Workstation*, March 1990. Publication Number 5952-1817

This article describes the architecture of the 68040 chip and the performance gains Motorola believes it will provide.

"... the upcoming 68040 is a fast, highly integrated 32-bit microprocessor that combines RISC-like integer performance with floating-point power beyond that of any standard microprocessor."

"... several companies are looking forward to using the 68040 to compete with low-end RISC-based workstations."

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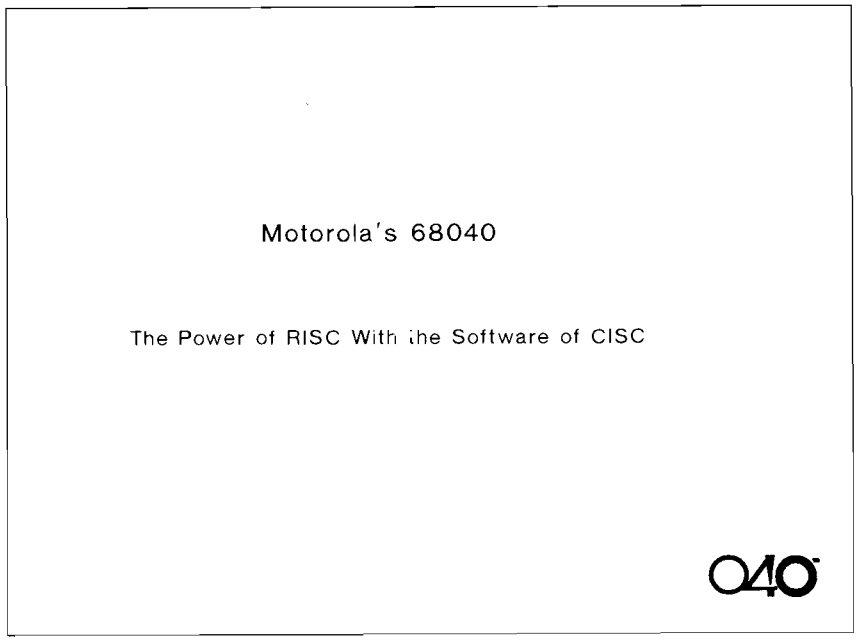
SLIDE #1: Motorola's 68040

On January 22, 1990, Motorola introduced its newest member of the 68000 family, the 68040. In spite of its seamless support for existing software, *the 040 should not be seen as a mere extension of past 680X0 chips.* Though the chip's architecture provides full compatibility with the earlier members of the family, the underlying circuitry has been redesigned from top to bottom. It is a revolutionary product, as big a leap over the 68030 as the 68020 was over the 68000 and the 68000 was over the 8-bit 6800. *68000 progress won't stop with the 040; Motorola is already laying plans for the 68050.*

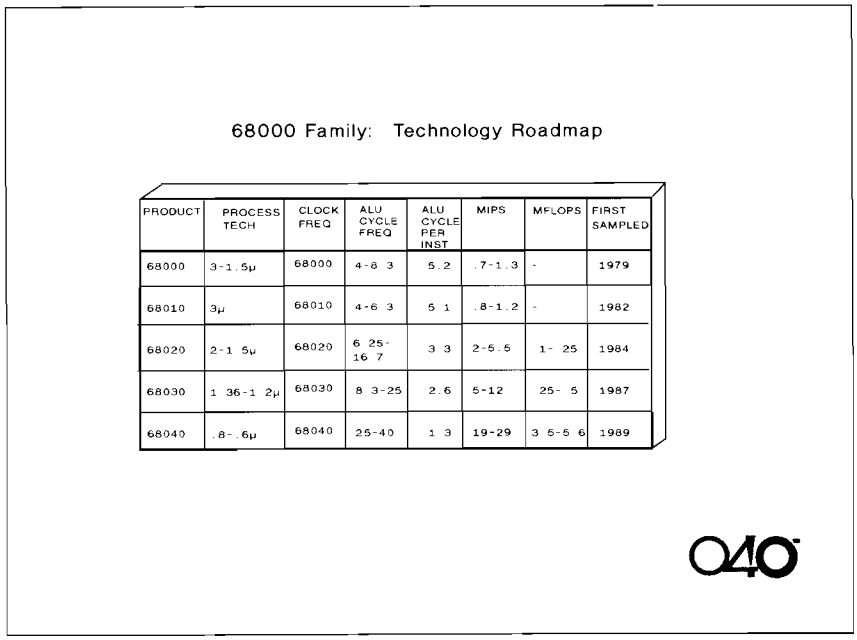


The 68040 is a fast, highly integrated 32-bit microprocessor that combines RISC-like integer performance with floating-point power beyond that of any standard microprocessor. Throughout this presentation you will learn that the 040 was designed using many RISC features which allow it to make the claim offering "the performance of RISC with the software of CISC".

SLIDE # 2: 68000 Family: Technology Roadmap

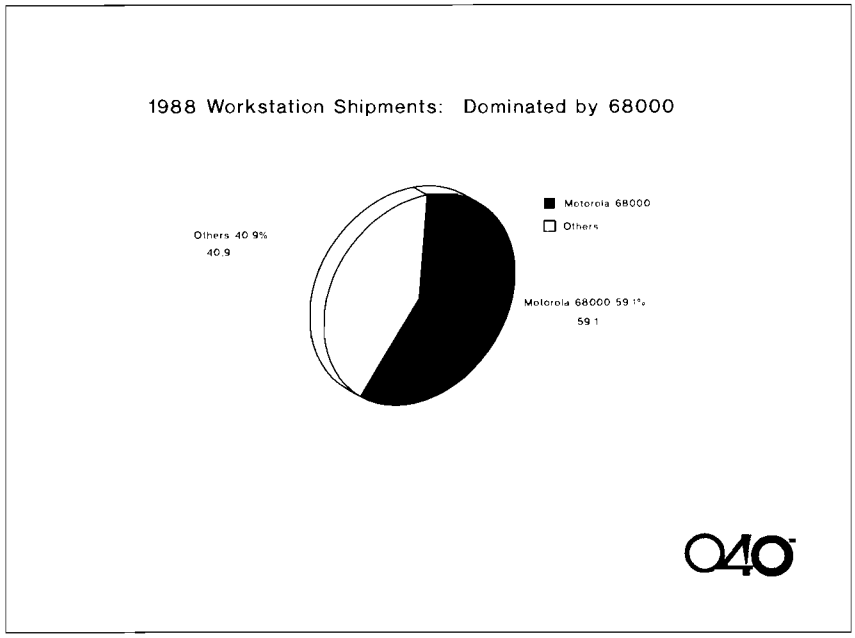
In the decade since its introduction, Motorola's 68000 microprocessor family has established the largest 32-bit computing base in existence. Thousands of companies have built systems around the 68000 series, and they and their *end-user customers have invested billions of dollars in 68000-based hardware and software.* With each succeeding generation, "680X0" processors have given computer manufacturers a means of both capitalizing on this investment and besting their competitors in features and performance. For the enormous 68000 family constituency, the 040 is a win-win proposition. It is 100-percent software compatible with the earlier Motorola processors and it eclipses rival microprocessors in functionality and speed.

The foundation chip for the 68000 family, the 68000 microprocessor, featured a flexible 32-bit internal architecture that could be expanded and added to efficiently. Such has not been the case with other established processor families, some of which have their roots in outmoded 16-bit architectures and whose efforts at upgrades have seen diminishing returns with each new product release.



PRODUCT	PROCESS TECH	CLOCK FREQ	ALU CYCLE FREQ	ALU CYCLE PER INST	MIPS	MFLOPS	FIRST SAMPLED
68000	3-1.5μ	68000	4-8 3	5.2	.7-1.3	-	1979
68010	3μ	68010	4-6 3	5 1	.8-1.2	-	1982
68020	2-1 5μ	68020	6 25-16 7	3 3	2-5.5	1- 25	1984
68030	1 36-1 2μ	68030	8 3-25	2.6	5-12	25- 5	1987
68040	.8-.6μ	68040	25-40	1 3	19-29	3 5-5 6	1989

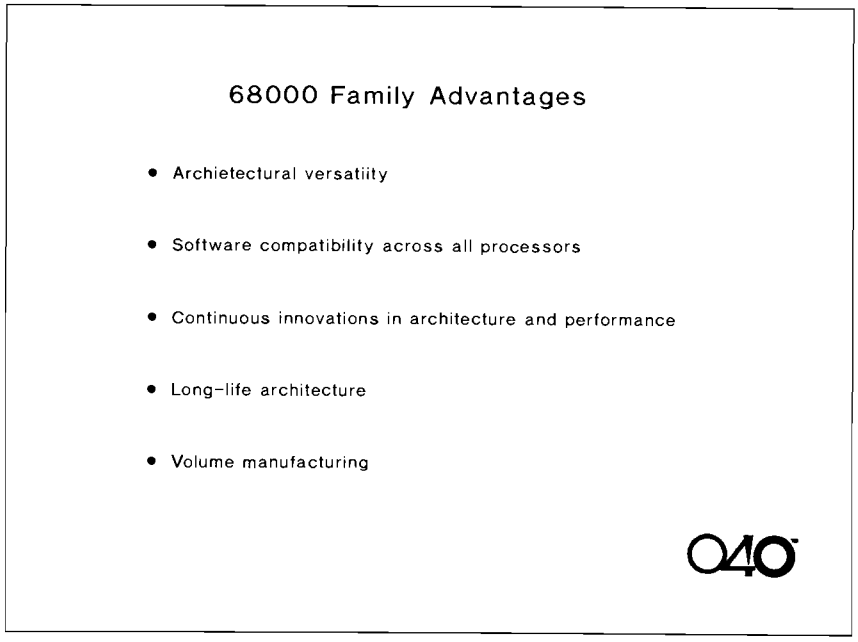
SLIDE # 3: 1988 Workstation Shipments: Dominated by 68000



Motorola anticipates that 95 percent of the 030 customer base will move up to the 040. This is hardly surprising when you consider that few designers of new computing systems start with a completely blank slate. If they have sold any previous products, then they have established customers, and these customers have usually spent large sums of money on software and other products geared to a specific computer architecture. *Preserving this capital investment isn't a luxury; it's an economic imperative.* As the subscribership for long-standing processor families grows, the need for a continued commitment to the architecture becomes more critical.

One indication of the 040's market potential is this huge base of existing 68000-family products. More than 30 million 68000-series processors have been delivered to date. In 1989 alone, 68000-family shipments topped ten million units. The Motorola chips dominate the markets for 32-bit workstations, multiuser business systems, and 32-bit embedded control. *The International Data Corporation (IDC) estimates, for instance, that 68000-family systems accounted for roughly 60 percent of all 1988 workstation shipments.*

SLIDE # 4: 68000 Family Advantages



Architectural versatility

The 680X0 family's range of compatibility, price, and performance options extend from the 040 all the way down to the 68000 microprocessor. Customers benefit from an unequalled ability to create their own diverse product families, running the scale from low to high end.

Software compatibility across all processors

The 68040 draws on the world's most extensive 32-bit software library. *In excess of 6,000 Unix application programs have been developed for 68000 systems,* for use in business, technical, scientific, and industrial environments. The 68000 family has generated an estimated $4 billion in 32-bit programs, and the 040 can run them all.

Continuous innovations in architecture and performance

Simply maintaining compatibility generation after generation is meaningless if technological innovation ceases or performance improvements stop.

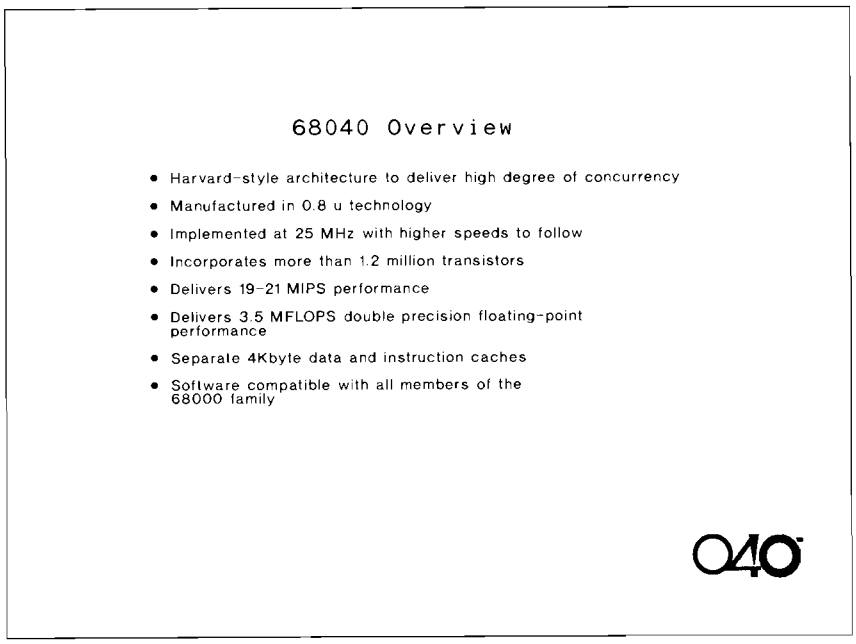
Long-life architecture

The 68000 line of microprocessors has been in existence for over ten years and promises to play a significant role in workstation computing for years to come. The January 24, 1990, issue of the *Microprocessor Report* predicts that "CISC processors will continue to dominate shipments for at least the next few years."

Volume manufacturing

Motorola is a global leader in CMOS semiconductor production. Of Motorola's 20 worldwide silicon wafer fabrication facilities, seven are for CMOS. Motorola also has a formidable background in leading-edge chip technology. The company's Advanced Product Research and Development Labs employ some of the world's leading CMOS technologists in the development of new fabrication processes. This expertise has contributed to the unmatched performance, density, and integration of the 68040.

SLIDE # 5: 68040 Overview



The 040 is the most integrated of the 32-bit processors, gathering a daunting array of computing functions on a single chip. Rivals of the 68040 include both conventional "CISC" processors and the majority of "RISC" chips as well.

The 040 demonstrates that it is possible to push the state of the art without abandoning the installed base. This is true for the 040 because the 68000 family was designed from the outset to provide a platform for rapid, unfettered evolution.

It is a mistake to make performance assumptions purely on the fact that a processor is a RISC (reduced instruction-set computer) device or a CISC (complex instruction-set computer) device. First of all, the boundary between the two technologies is not as clear-cut as it is sometimes portrayed. RISC and CISC are general design philosophies, and a given microprocessor can take lessons from both schools. The basic idea behind RISC is that by pruning the computer's instruction set down to the bare essentials, processing can be streamlined. CISC, on the other hand, aims to pack more work into individual instructions, sometimes increasing the time it takes to perform them. (Instructions are the elementary commands that computer programs issue to microprocessors. Different microprocessor families use different instruction sets.) Both philosophies, in other words, attempt to maximize the amount of work accomplished per unit of time.

The 68040 runs the 68000-family instruction set — a necessity if the chip is to support the established software base. To that extent, the 040 is a CISC processor. *But in its instruction execution speed, it is more like a RISC processor than traditional CISC products.* On the average, the 040 completes one instruction every 1.3 clock cycles (performance relative to a VAX 11/780). This is extremely fast, and makes the 040 more competitive with RISC chips (which aim for one instruction per clock cycle) than traditional CISC processors. This accomplishment is especially impressive in view of the fact that the 040's instructions are much more powerful than typical RISC instructions.

"Pure" RISC chips, it must be noted, are no automatic ticket to higher performance. RISC processors can't match the 040 on processing power alone; add to this the fact that no RISC line has even one percent of the 68000 hardware, software, and user experience base, and the 040 comes out the clear winner in many potential application areas. The economy and ease with which an 040 system can be designed, delivered, and outfitted with suitable software combined for a system price-performance ratio that no RISC processor can approach.

Harvard-style architecture to deliver high degree of concurrency

The 040 caches are linked to the integer unit by separate pathways, so that data and instructions can be transmitted in parallel. This is termed a Harvard architecture. The two caches combine for an extremely high information transfer rate of 200 megabytes per second.

Manufactured in 0.8 micron technology

The 040's submicron implementation allows for a high

level of integration. It is the first commercial microprocessor with a feature size below 1 micron. The .8-micron HCMOS (high-performance complementarymetal-oxide silicon)implementation allows the over one million transistors contained on the 040 to be squeezed onto a single chip.

Implemented at 25 MHz with higher speeds to follow

The current 25 MHz version of the chip will be joined in the future by 33 and 50 MHz releases.

Incorporates more than 1.2 million transistors

At 1.2 million transistors, the 040 is the largest commercial microprocessorever.

Delivers 19-21 MIPS performance

At a sustained clip of 20 million instructions per second (MIPS) and 3.5 million floating-point operations per second (MFLOPS), the 040 is considerably faster than Intel's 80486 CISC processor and RISC engines such as Sun's SPARC. *It is flat-out the most powerful microprocessor in its class ever produced.*

Delivers 3.5 MFLOPS double precision floating-point performance

Providing an FPU (floating point unit) on the 040 greatly reduced the number of clocks required to execute the most-used instructions. The 68040 is claimed to run dual-precision floating-point code over three times faster than the 80486 and over 30% faster than the Weitek coprocessor.

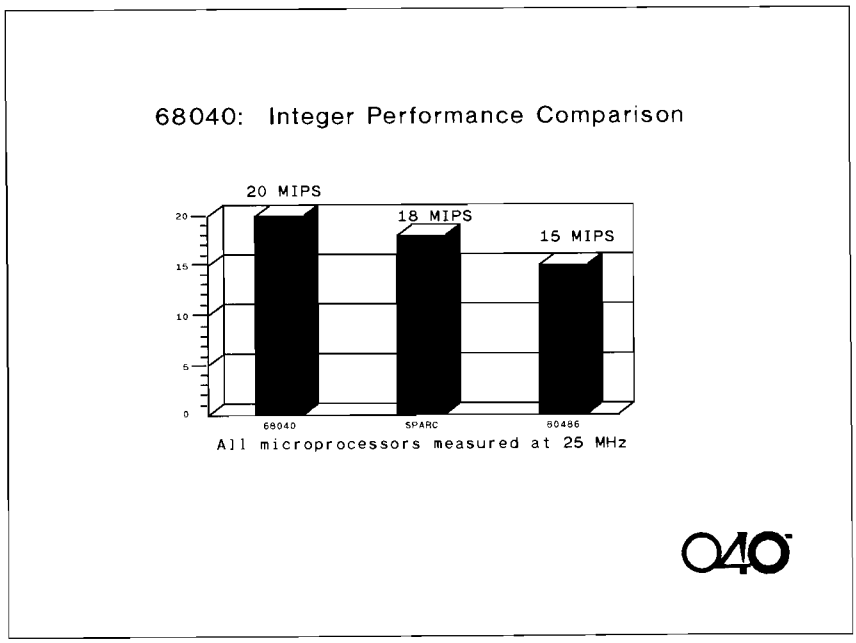
Separate 4Kbyte data and instruction caches

Motorola has put separate 4-Kbyte instruction and data caches on-chip, so that much code executes with little bus access. The caches are tied to separate instruction and data memory management units.

Software compatible with all members of the 68000 family

SLIDE # 6: 68040: Integer Performance Comparison

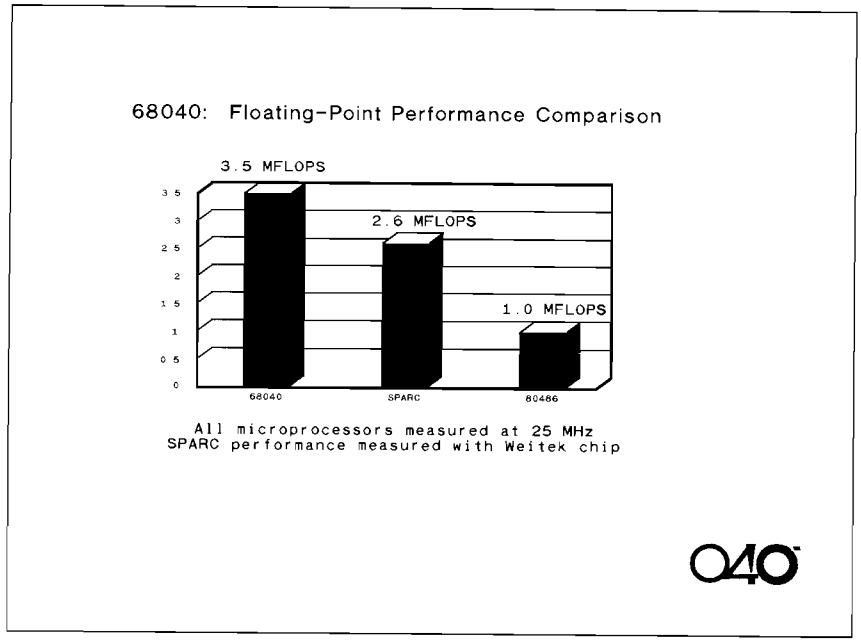
The 040 turns in a sustained performance of 20 MIPS (VAX MIPS - relative to a DEC VAX 11/780) at its initial clock speed of 25 MHz. This compares quite favorably with the Intel 486, the Sun SPARC and the AMD 29000, which weigh in respectively at 15, 18, and 17 MIPS at equivalent clock rates.* Note that MIPS measures the instruction processing rate under the simplest, most straightforward conditions; it does not reflect the processor's ability to cope with the inevitable complexities of workaday computing. *In practical situations the 040's performance lead is even wider than the MIPS figures suggest.*



* The 040's MIPS performance is very nearly as high as the SPARC's 33 MHz clock-rate version. The 040's own 33 MHz version will go well beyond that. The 040's customers can either match the SPARC's MIPS rates at lower clock speeds (meaning easier and less expensive system design) or surpass the SPARC at equivalent clock rates.

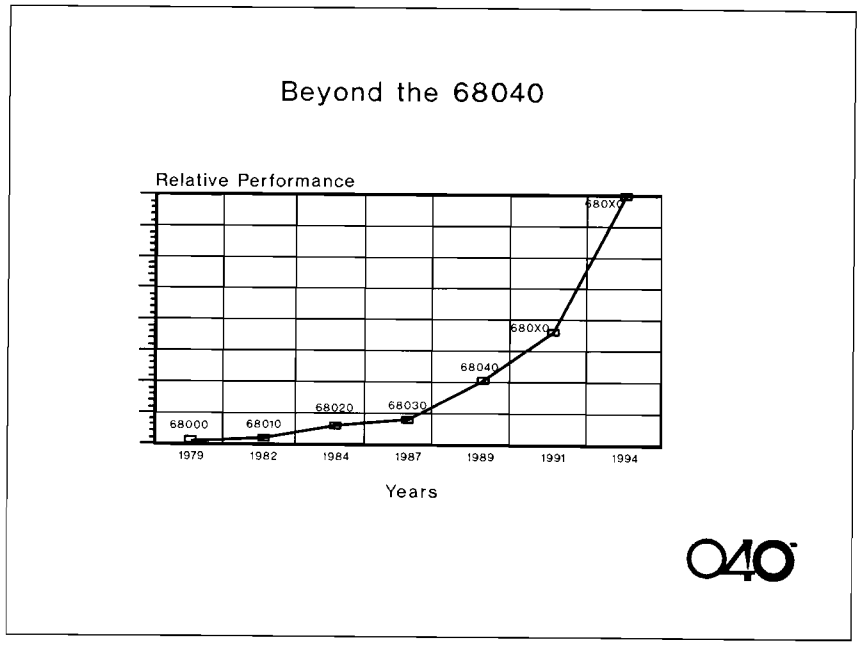
SLIDE # 7: 68040: Floating-Point Performance Comparison

The 040's speed in floating-point math — the number crunching functions critical to scientific, engineering, industrial, graphics, and many business applications — is likewise head and shoulders above the competition. The chip sustains 3.5 million floating-point operations per second (MFLOPS),* compared with 1 MFLOPS for the 486 and 2.6 for the SPARC (the latter using special math accelerator chips).



SLIDE # 8: Beyond the 68040

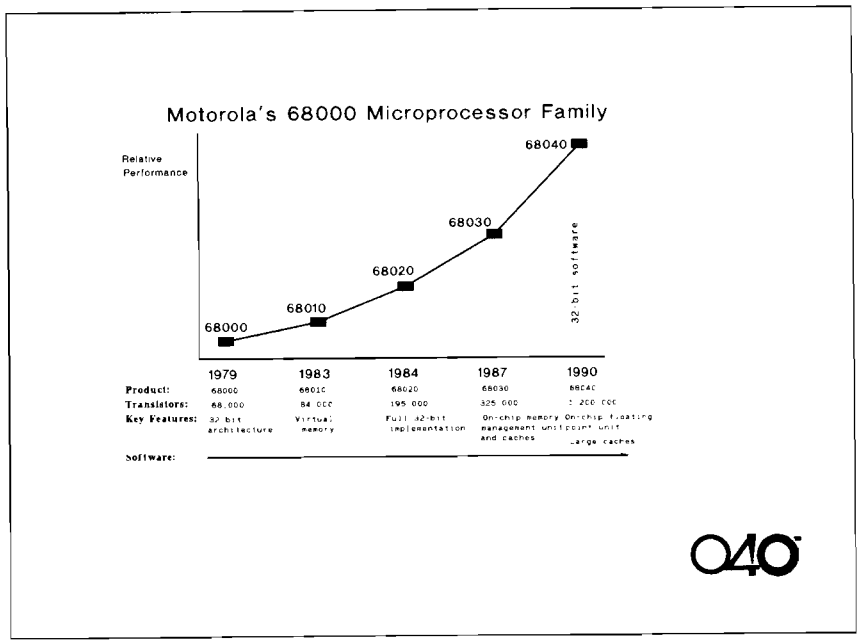
The 68000 family has been at the forefront of the microprocessor market for 10 years, and with advanced-generation chips such as the 68040 and the planned 68050, the product line will continue to lead the field for decades.



* All figures are double-precision Linpack ratings, run on the inner loop (DAXPY). The data cache was in copy-back mode.

SLIDE # 9: Motorola's 68000 Microprocessor Family

The success of the 68000 family is unprecedented. As 68000 technology has improved over the last ten years, these improvements have permitted more and more components on each successive chip, permitting a greater range of capabilities which improve performance. Motorola's valuable commitment to compatibility allows workstation customers to maximize their investments through competitive performance and software compatibility.



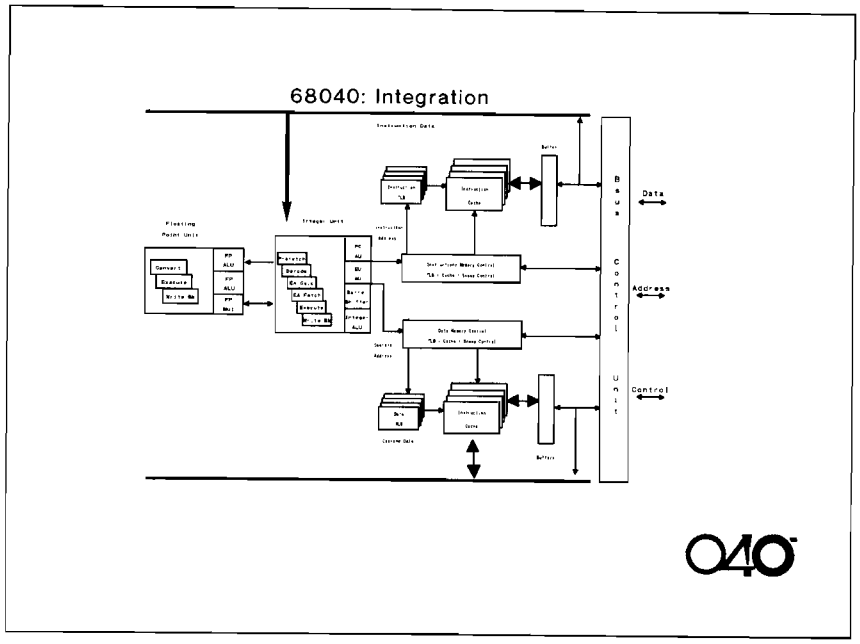
Appendix A: 68040: Integration

Designed for Real-World Conditions

The 040 is the result of some of the most exhaustive design analyses ever undertaken for a microprocessor. Motorola engineers studied a number of commercial 68020-based computers as they ran a range of application programs. A data collection system tracked the progress of each application in microscopic detail: keeping tabs on which processor instructions were executed, when and how often the microprocessor used its cache memory, to what effect and how often it used its system bus, and so on.

In all, a record of thirty million instructions were collected from each system. By analyzing the statistical record, *design engineers found just what processor features contributed the most to performance — and what design changes would yield the biggest improvements.*

The key to this study is that it was conducted on real-world systems, doing real-world tasks. The 040, after all, would have to serve the same sort of applications and support the very same software that the 020-based test systems were running. *Concrete analysis of this kind is not always the rule in the industry.* Some microprocessors are planned according to theoretical models. Many are designed to maximize speed on *synthetic benchmark programs, not real applications. Unsurprisingly, such products fall short of customer expectations when put to work in actual operating environments.*



The thoroughness of Motorola's effort was not just a matter of methodology, but of access to appropriate machines and applications. The 68000 family's long presence and preeminence in such markets as workstations and UNIX multiuser systems allowed Motorola to run its tests on a range of mature systems and software directly applicable to the task at hand. Competing chip vendors, lacking long track records in these markets, must rely more on theory and less on hard data.

Setting New Standards

The outcome of the 040 design effort was a chip that sets new standards in nearly every functionality and performance category. The instruction cycle rate was trimmed from an average of 3.4 clock cycles per instruction on the 68030 to 1.3 on the 040. Unlike conventional CISC processors, whose instructions must first be converted into lower-level micro-instructions prior to execution, the 040 has many of its key instructions, "hard-wired" in silicon. They can be executed directly, without an intermediate conversion step.

Historically general-purpose microprocessors have had to depend on add-on coprocessors and accelerators such as Motorola's 68882 for fast floating-point capabilities. The 040 features a complete built-in floating point unit. Consolidating this important function on-chip speeds up the overall processing and does away with some of the interfacing overhead required for external accelerators. The 040 floating point unit operates in parallel with the integer unit. When the integer unit encounters a floating-point instruction, it simply hands it off to the math unit. The math unit does the numeric calculation while the integer unit moves on to another task. Like the integer unit the floating-point unit has its own pipelining. It can overlap three operations: the conversion of integer to floating-point numbers (or vice versa) and instruction execution and write-back. The 040 floating-point unit is fully compliant with floating-point standards set by the IEEE (the Institute of Electrical and Electronics Engineers).

The 040 floating point unit is compatible with Motorola's 68881 and 68882 math coprocessors, so that 680X0 systems that employed those chips will be able to run their software on the 040. The 040 runs basic math functions such as floating-point addition and multiplication directly on dedicated circuitry. The 040 performs transcendental functions such as sine, cosine and square root calculations by means of software routines. A software package providing these routines is provided by Motorola. Like the 040's hardware-based math functions, the software functions are compatible with the 882, which in contrast to the 040 supported transcendentals in hardware. Here again the 040 is speedier than the coprocessor, racing through transcendentals at a 50 percent faster rate than a 68030/68882 combination (at 33 MHz).

The horsepower of the 040's floating-point machinery is sufficient for a range of numerics-intensive applications. In order to handle comparable applications, users of competing processors have had to run to special numeric accelerator chips, added to systems at considerable cost. Both the 486 and SPARC, for instance, use coprocessors developed by Weitek Corporation. The 040, by contrast, needs no coprocessor.

Caches and Memory Management

Caches are small, fast memory arrays that give processors rapid access to frequently-used information. Placing these devices on the microprocessor chip puts data and instructions within easy reach of the execution units. Motorola's 68020 was the first microprocessor to integrate a cache on chip. The processor had a single 256-byte cache for instructions. The 68030 was the first processor to add a second cache on chip, allowing instructions and data to be stored separately and fetched simultaneously. This is also classified as a RISC feature (separate data and instruction caches). The 030's caches were 256 bytes each. The 040 has gone even farther, expanding the data and instruction caches to a full 4 kilobytes a piece. Moreover, the 040 has equipped each cache with its own on-chip memory management unit (MMU) and cache controller. The 030, by contrast, had a single MMU, through which both data and instruction addresses had to pass and a single cache controller. Likewise the 486, has only a single cache, cache controller, and MMU and competing RISC chips lack even that; their caches are provided by external devices.

The 040 caches are linked to the integer unit by separate pathways, so that data and instructions can be transmitted in parallel. This is termed a Harvard architecture. The two caches combine for an extremely high information transfer rate of 200 megabytes per second.

Caches work as follows: a block of data or instructions is loaded into the cache from main memory, usually an off-chip RAM. When the processor needs information, it looks first in the cache. If it finds what it wants there, that's called a cache "hit." If it doesn't, a new block of information must be shipped in from main memory, forcing the processor to pause for a moment while waiting for the information. This is a cache "miss," and it inflicts a performance penalty. Naturally, the bigger the caches, the greater the probability of finding sought-after information on-chip and the higher the hit rate.

The hit rate is also boosted if the cache controllers are intelligent and flexible in their placement of information. There's only so much room in the cache, and when new data or instructions are sent in, they elbow aside other data and instructions (actually the new information is written over the old). It makes the best sense for the cache to bump those data and instructions that won't be needed again in the near future. The 040 provides a great deal of flexibility in doing this, allowing incoming information to be stored in a choice of four locations. This is called four-way set associativity. Processors that are "direct-mapped" on the other hand, give no choice as to where the new information is put, forcing it to overwrite important information, so their hit rates suffer. *The 040's hit rates for the MMU and ATC exceed 99 percent—that is, ninety-nine times out of a hundred, the processor will find what it is looking for in these caches. And the hit rate for the I/O cache is 92%!*

Still, even with hit rates as high as this, cache misses can take a toll. When a miss occurs, a processor must search for the desired information in main memory. This requires a physical address, which specifies the precise storage location of a given piece of information. It is the MMU's job to keep track of these locations. The integer unit itself knows nothing about the physical placement of memory contents. When, as explained above, the integer unit calculates an address, it is a "logical" address, which must then be converted by the MMU into a physical address. The execution unit is like a library patron who knows a book's call number but has no idea where it is shelved. The MMU is the librarian who goes and finds the volume requested.

In translating the address from logical to physical, the MMU uses a so-called address translation cache (ATC) also known as the translation look-aside buffer (TLB), which contains a list of translated addresses. The MMU gets a logical address from the integer unit, then looks in the ATC to find the correct physical address. The physical address is used to fetch the information from off-chip main memory. When the translation of a specific address isn't found in the ATC, a new batch of translated addresses must be moved in from translation tables stored in main memory, slowing the processing. This is especially likely to occur in multitasking situations, where the processor is switching constantly from one job and program to another, moving widely among memory locations and their corresponding addresses.

Appendix B Customer Presentation Slides

These slides, made available from Motorola, will help you present the advantages and benefits of the 040 to your customers.

Motorola has given HP permission to use these slides during the 68040 introduction.

Your RSSMs told us that they will be of most use to you if you can use the actual Motorola slides by thermofaxing these copies.

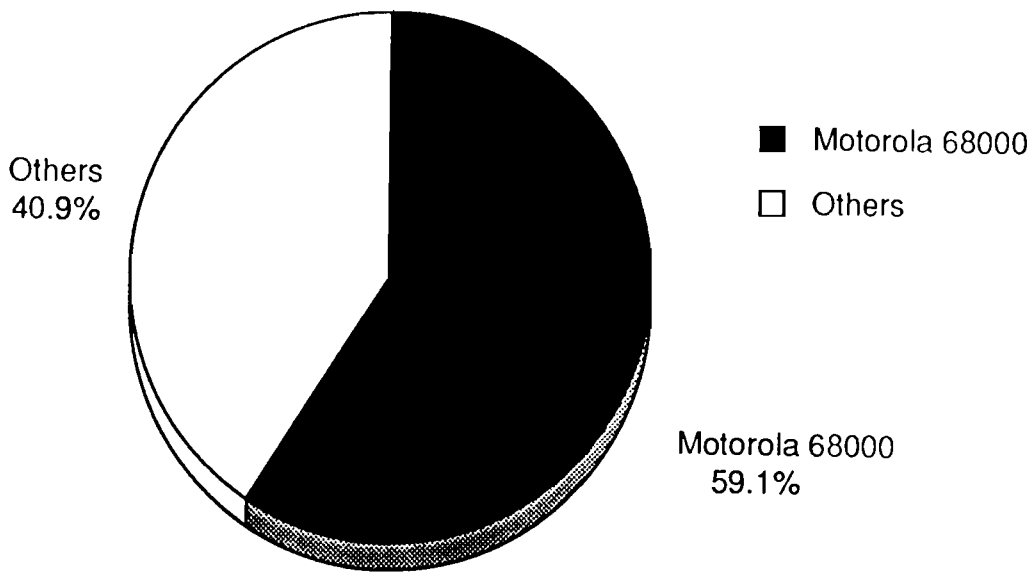
Motorola's 68040

The Power of RISC With the Software of CISC

68000 Family: Technology Roadmap

PRODUCT	PROCESS TECH	CLOCK FREQ	ALU CYCLE FREQ	ALU CYCLES PER INST	MIPS	MFLOPS	FIRST SAMPLED
68000	3-1.5µ	8-16.7	4-8.3	5.2	.7-1.3	-	1979
68010	3µ	8-12.5	4-6.3	5.1	.8-1.2	-	1982
68020	2-1.5µ	12.5-33.3	6.25-16.7	3.3	2-5.5	.1-.25	1984
68030	1.35-1.2µ	16.6-50	8.3-25	2.6	5-12	.25-.5	1987
68040	**.8-.6µ**	**25-40**	**25-40**	**1.3**	**19-29**	**3.5-5.6**	**1989**

1988 Workstation Shipments: Dominated by 68000



Compiled by International Data Corp. 1989

040™

68000 Family Advantages

- Architectural versatility
- Software compatibility across all processors
- Continuous innovations in architecture and performance
- Long-life architecture
- Volume manufacturing

68040 Overview

- Harvard-style architecture to deliver high degree of concurrency
- Manufactured in 0.8 μ technology
- Implemented at 25 MHz with higher speeds to follow
- Incorporates more than 1.2 million transistors
- Delivers 20 MIPS performance
- Delivers 3.5 MFLOPS double precision floating-point performance
- Separate 4Kbyte data and instruction caches
- Software compatible with all members of the 68000 family

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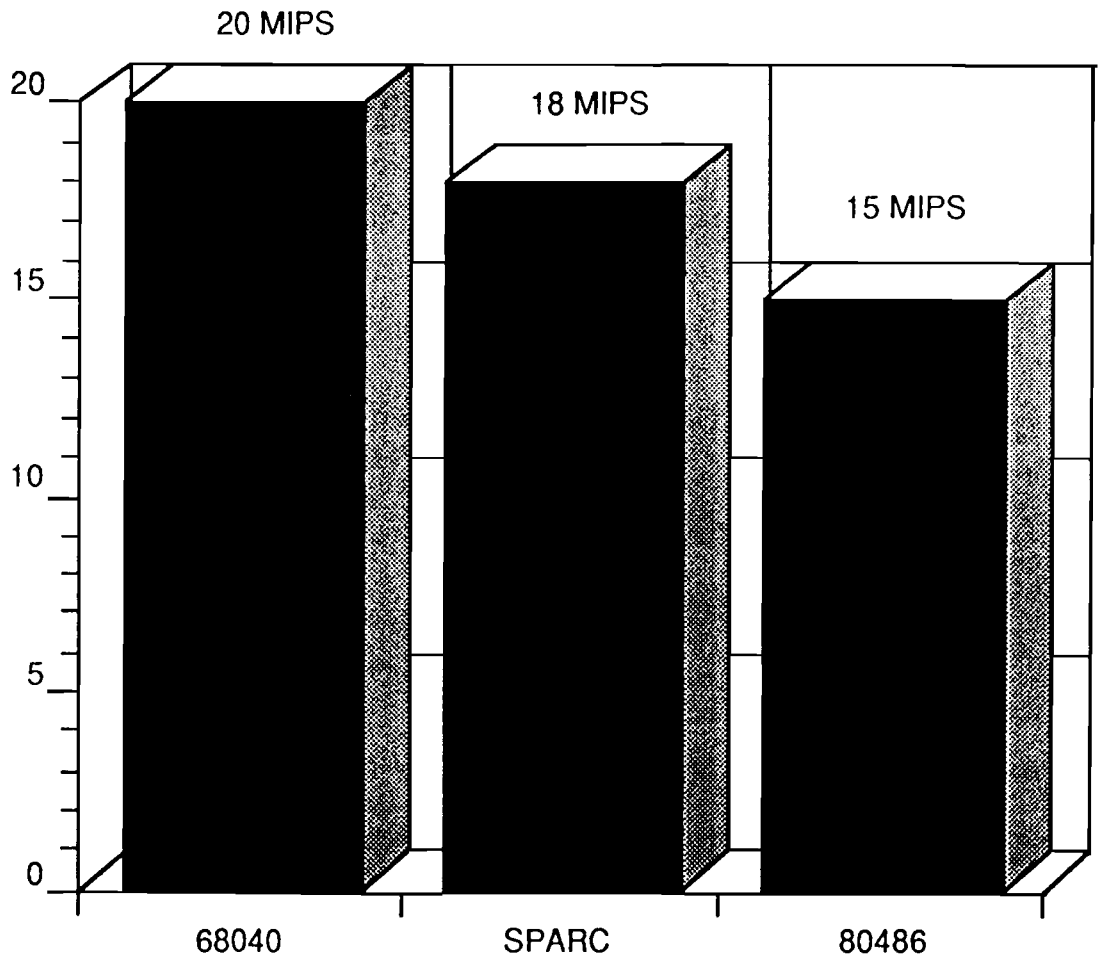
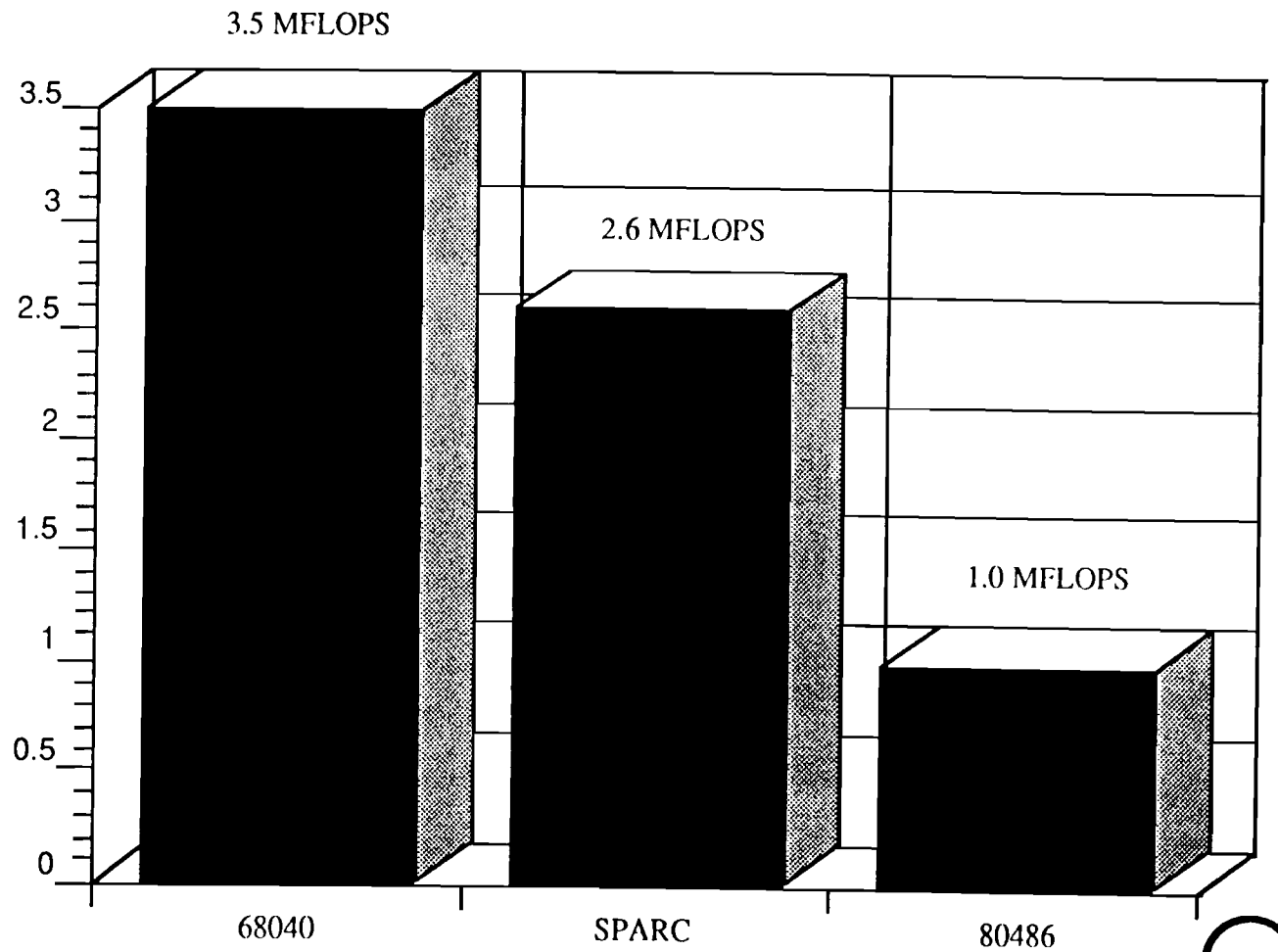
68040: Integer Performance Comparison



All microprocessors measured at 25 MHz

68040: Floating-Point Performance Comparison



All microprocessors measured at 25 MHz
SPARC performance measured with Weitek chip

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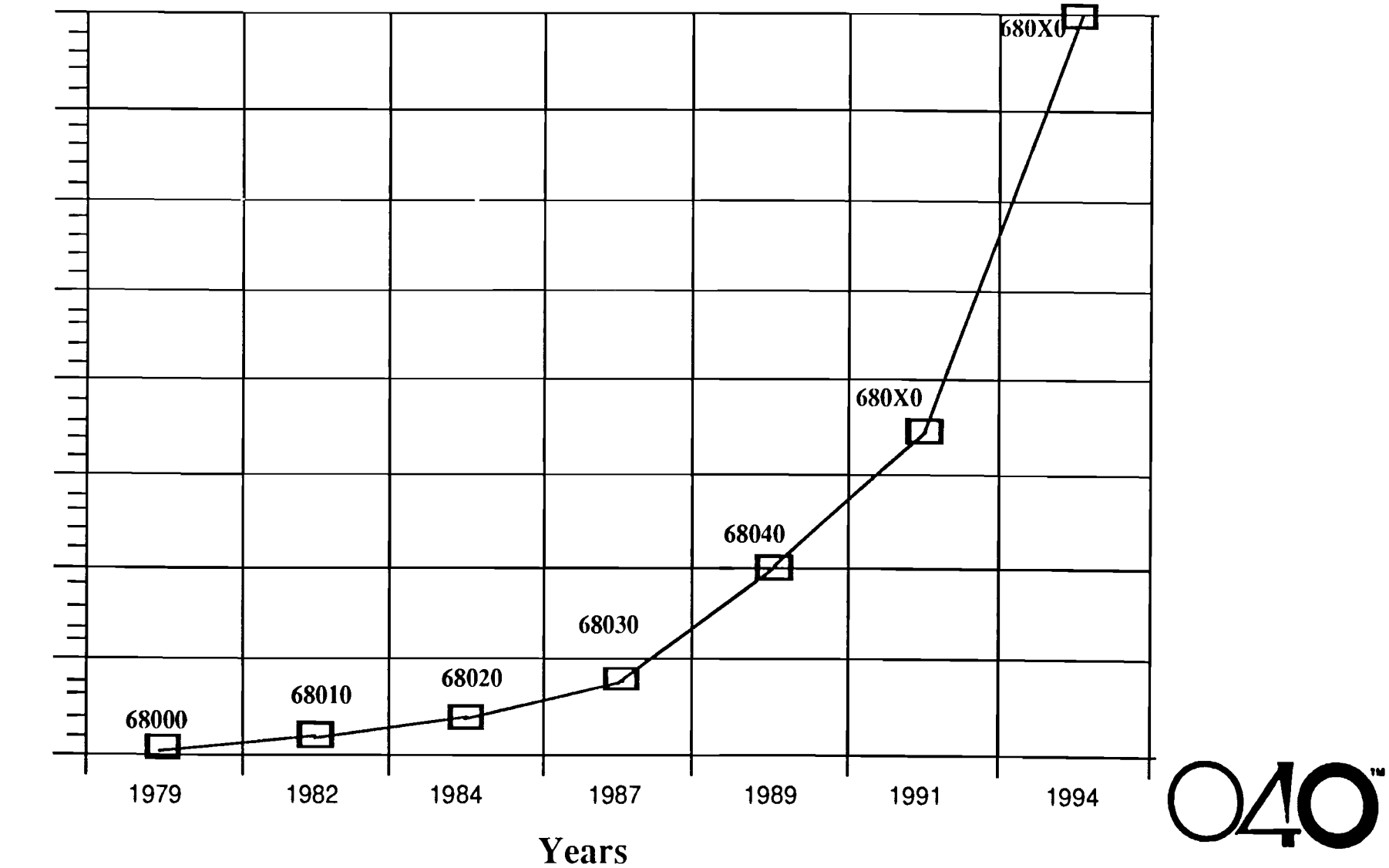
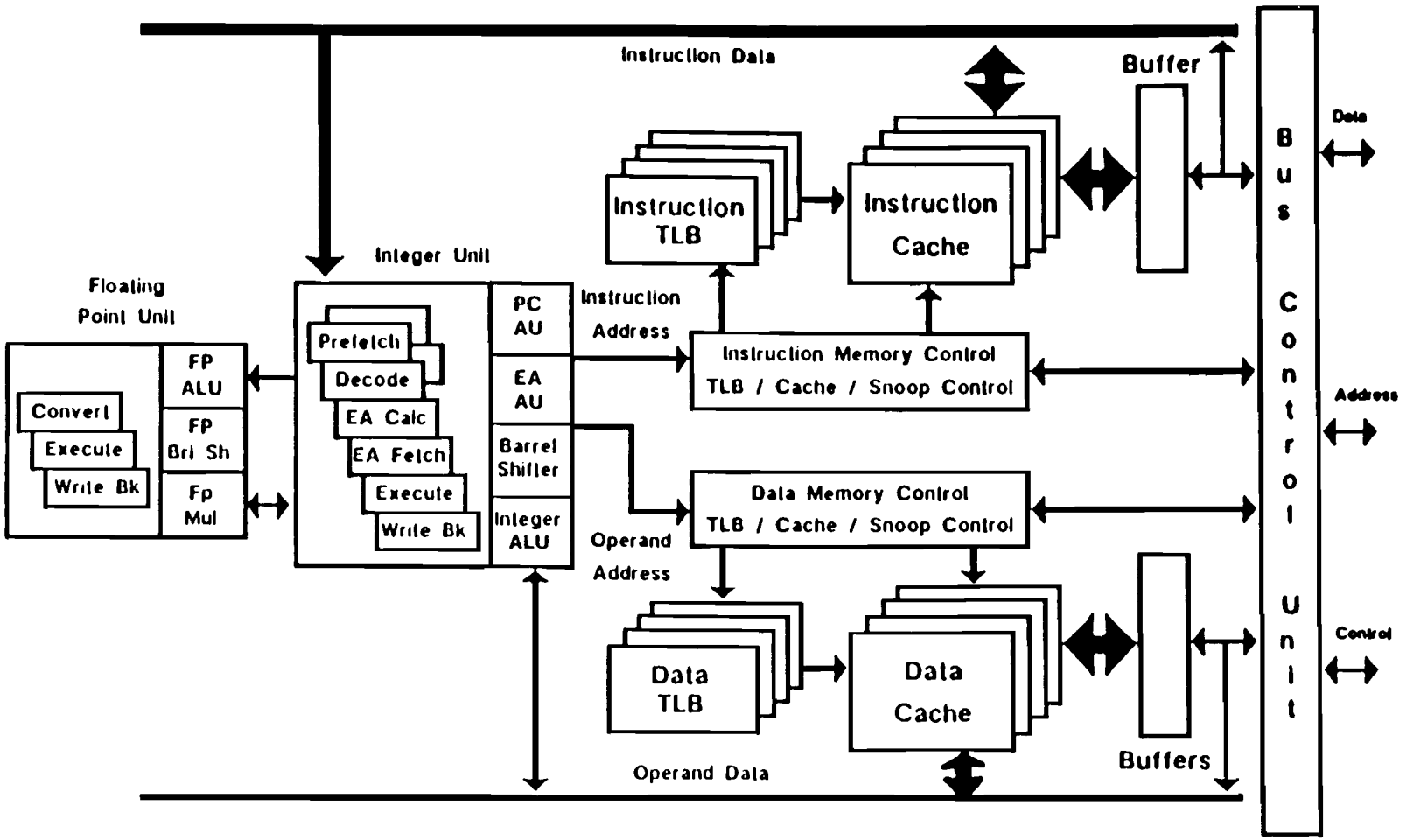
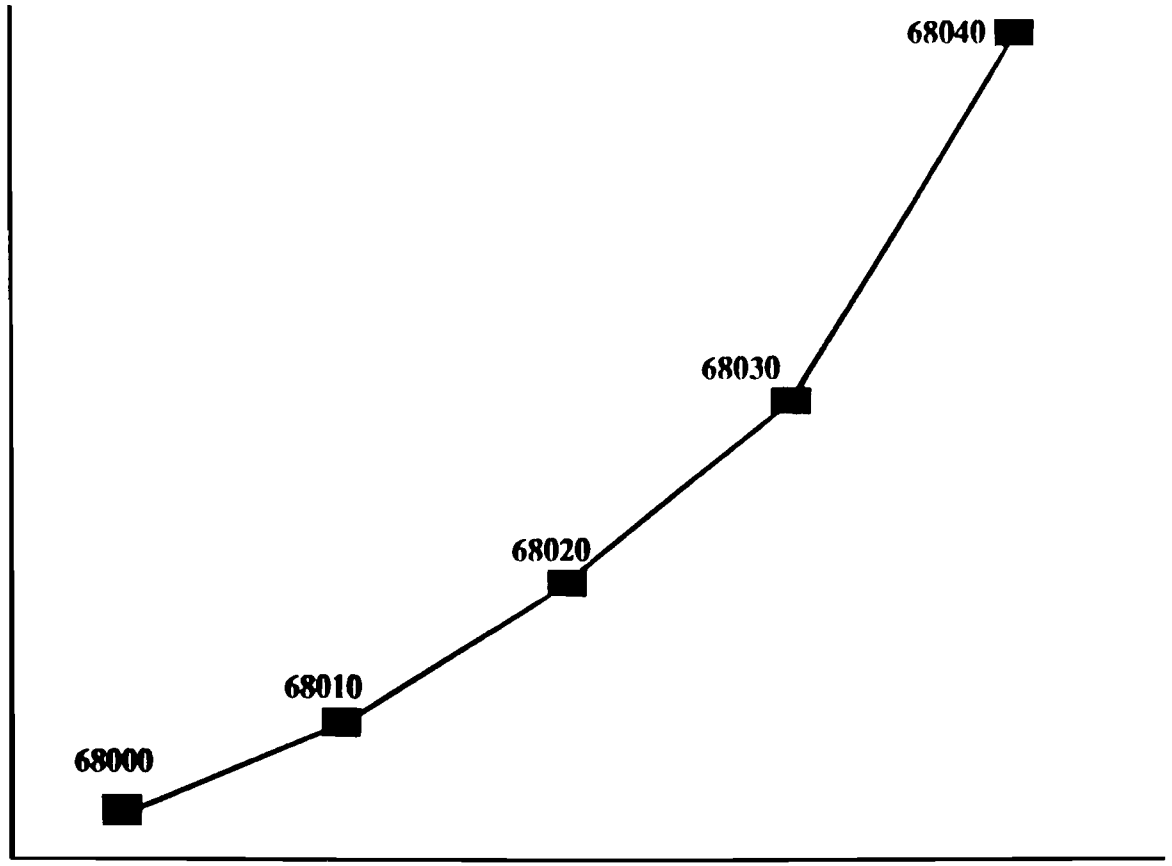
Beyond the 68040



68040: Integration



Motorola's 68000 Microprocessor Family



Product:	68000	68010	68020	68030	68040
Transistors:	68,000	84,000	195,000	325,000	1,200,000
Key Features:	32-bit architecture	Virtual memory	Full 32-bit implementation	On-chip memory management unit and caches	On-chip floating point unit Large caches
Software:	32-bit software				

040™

Printed in U.S.A. April, 1990