HEWLETT PACKARD

L/A-Series Programmable Serial Interface (PSI) (MODEM)

Installation and Service Manual

Card Assembly: 5061-4912
Date Code: 2138

HEWLETT-PACKARD COMPANY
Roseville Division
8000 Foothills Boulevard
Roseville, California 95678

Manual Part No. 12042-91001
Printed in U.S.A.
February 1982

PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition ..... February 1982

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends upon the type of material. Insulators can easily build up static charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields. *The resulting damage can range from complete destruction to latent degradation.* Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The basic concept of static protection for electronic components is the prevention of static build-up where possible and the quick removal of already existing charges. The means by which these charges are removed depend on whether the charged object is a conductor or an insulator. If the charged object is a conductor such as a metal tray or a person's body, grounding it will dissipate the charge. However, if the item to be discharged is an insulator such as a plastic box/tray or a person's clothing, ionized air must be used.

Effective anti-static systems must offer start-to-finish protection for the products that are intended to be protected. This means protection during initial production, in-plant transfer, packaging, shipment, unpacking and *ultimate use.* Methods and materials are in use today that provide this type of protection. The following procedures are recommended:

1. All semiconductor devices should be kept in "antistatic" plastic carriers. Made of transparent plastics coated with a special "antistatic" material which might wear off with excessive use, these inexpensive carriers are designed for short term service and should be discarded after a period of usage. *They should be checked periodically to see if they hold a static charge greater than 500 volts in which case they are rejected or recoated.* A 3M Model 703 static meter or equivalent can be used to measure static voltage, and if needed, carriers (and other non-conductive surfaces) can be recoated with "Staticide" (from Analytical Chemical Laboratory of Elk Grove Village, Ill.) to make them "antistatic."

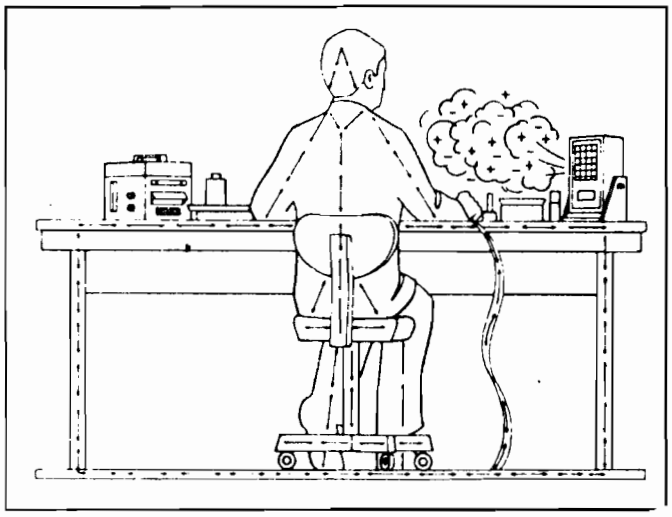
2. Antistatic carriers holding finished devices are stored in transparent static shielding bags made by *3M Company.* Made of a special three-layer material (nickle/polyester/polyethylene) that is "antistatic" inside and highly conductive outside, they provide a Faraday cage-like shielding which protects devices inside. "Antistatic" carriers which contain semiconductor devices should be kept in these shielding bags during storage or in transit.

HP Computer Museum
www.hpmuseum.net

For research and education purposes only.

Individual devices should only be handled in a static safeguarded work station.

3. A typical static safeguarded work station is shown below including grounded conductive table top, wrist strap, and floor mat to discharge conductors as well as ionized air blowers to remove charge from nonconductors (clothes). Chairs should be metallic or made of conductive materials with a grounding strap or conductive rollers.



SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

Glossary of Terms

The following terms are defined as they are used in Hewlett-Packard computer products manuals. Some of the terms defined below may not be used in this manual.

Asynchronous transmission - No timing signals are sent with the data. Start and stop bits serve to delimit transmitted words.

Binary Synchronous Protocol - Bisync - BSC - These terms are synonymous, and stand for a character-oriented, half-duplex protocol.

Buffer - A segment of contiguous random-access memory locations used for temporary storage of input/output messages.

Card - The Printed Circuit Assembly (PCA).

CCITT - International Telephone and Telegraph Consultive Committee.

CRC-16 - Cyclic Redundancy Check - An error detection scheme used in data communications.

CRC-CCITT - Cyclic Redundancy Check - An error detection scheme defined by the International Telephone and Telegraph Consultive Committee.

DCE - Data Circuit-terminating Equipment - In most references, an entry node of the network.

DCPC - Dual Channel Port Controller.

DIP - Dual In-line Package - A type of integrated circuit package.

DMA - Direct Memory Access - The transfer of data directly to or from memory.

Driver - In a hardware sense, a driver refers to a circuit which is capable of supplying specific current and voltage requirements. In a software sense, a driver is a program that is capable of controlling a specific input/output device.

DS - Distributed System - A term used to refer to networks using Hewlett-Packard Distributed Systems hardware and software products.

DTE - Data Terminal Equipment - In most references, the local node which resides outside the network and communicates with the DCE.

EIA - Electronics Industries Association.

Firmware - Software code packaged in read-only memory (EPROM/ROM).

FCS - Frame Checking Sequence - A 16-bit sequence derived from an algorithm common to DCE and DTE. The sequence is appended to each frame and used as a verification of data transmission.

Flag - The LAP-B and HDLC synchronization character with a binary representation of "01111110". Because LAP-B and HDLC require zero insertion after a string of five "1" bits, the flag bit string is unique and cannot be misinterpreted.

Frame - A LAP-B and HDLC unit of information exchange, bounded by flags, consisting of an address field, control field, optional data field, and an FCS field.

Full-duplex - Communications systems or equipment capable of simultaneous two-way data communication.

Half-duplex - Communications system or equipment capable of transmission in either direction, but not both directions simultaneously.

Handshaking - The alternating exchange of predetermined signals between two communicating devices for purposes of control.

HDLC - High-Level Data Link Control. Types of protocols which eliminate much of the handshaking (and resultant time-consuming line turnarounds).

Host - The computer housing the circuit card.

HP-DLC-II - Hewlett-Packard Data Link Control II - A Hewlett-Packard HDLC standard defining the elements and procedures for a balanced, bit-oriented, Level-II protocol. HP-DLC-II is compatible with CCITT X.25 LAP-B, and LAP-B implementations by TELENET and TRANSPAC packet-switching networks.

I-Frame - A LAP-B and HDLC unit of information exchange containing a data field.

Interface - A device providing electrical and mechanical compatibility between two communicating devices.

ISO - International Standardization Organization.

k - Maximum number of outstanding I-frames: a system parameter (less than eight) defining the most unacknowledged information frames permissible at any given time.

LAP-B - Link Access Protocol -Balanced - A CCITT Recommendation X.25 Level II protocol. LAP-B, a bit-oriented protocol, uses the principles and terminology of ISO's HDLC.

LED - Light Emitting Diode - A component used on many printed circuit assemblies to provide a visual indication of desired information.

Link - Communication lines, modems, and other equipment which permit the transmission of information in data format between two or more devices.

Modem - Modulator-Demodulator - Equipment capable of digital-to-analog and analog-to-digital signal conversion for transmission and reception via common carrier telephone lines.

Modulus - Used by LAP-B and HDLC in the sequential numbering of I-frames; modulus equals eight.

N1 - Maximum number of bits in an I-frame; N1 is a system parameter used by LAP-B and HDLC.

N2 - Maximum (re)transmission; a LAP-B and HDLC system parameter specifying the number of times the local node will transmit and retransmit a frame before some recovery procedure is begun.

N(R) - Receive sequence number - Found in LAP-B and HDLC information, receiver ready, receiver not ready, and reject frames. N(R) denotes the expected sequence number of the next received I-frame.

N(S) - Send sequence number - Found in LAP-B and HDLC information frames, it denotes the sequence number of the transmitted I-frame.

Octet - A sequence of eight bits, i.e., a byte.

PCA - Printed Circuit Assembly - Circuit cards are commonly referred to as PCAs.

Primary - In LAP-B and HDLC, that logical portion of a DCE or DTE responsible for sending commands and receiving/processing the resulting responses. In Bisync, a primary is the node which initiated the call.

Primary System - A preconfigured operating system included with all HP 1000 Computer systems. It can be reconfigured to meet specific system I/O and memory requirements.

Receiver - Any device capable of reception of electrically transmitted signals.

SDLC - Synchronous Data Link Control - An IBM High-Level Data Link Control protocol.

Secondary - In LAP-B and HDLC, that logical portion of a DCE or DTE responsible for receiving commands from the remote DTE/DCE, processing these commands, and generating the correct responses. (Each LAP-B or HDLC DCE/DTE is a combined station, composed of both logical primary and secondary functions.) In Bisync, a secondary is the node which receives a call.

Synchronous transmission - Timing signals are transmitted with the data. No start and stop bits are used. Defined protocol characters must be used to delimit message blocks or frames.

System Parameter - As used in HP manuals, a parameter necessary for DCE/DTE communication; its value is agreed upon before network communication is attempted.

T1 - Timer T1 - In LAP-B and HDLC, the period of time that elapses while awaiting acknowledgement of an outstanding frame.

T2 - Timer T2 - In LAP-B and HDLC, the maximum period of time a node will allow without an exchange of frames while the link is logically connected. (T1 excludes T2.)

TELENET - A packet-switching network owned and operated by GTE.

TRANSPAC - The French packet-switching network.

V(R) - Receive state variable - In LAP-B and HDLC, V(R) denotes the sequence number of the next in-sequence information the node expects to receive.

V(S) - Send state variable - In LAP-B and HDLC, V(S) denotes the sequence number of the next in-sequence information frame to be transmitted by the node.

Contents

Chapter 1 General Information

Chapter 2 Installation

Chapter 3 Principles of Operation

Contents (Cont.)

Chapter 4 Maintenance

Chapter 5 Replacement Parts

Chapter 6 Servicing Diagrams.....6-1

PREFACE

The Programmable Serial Interface is a multiusage hardware interface which must be complemented by Hewlett-Packard, or user-designed firmware installed directly on the board.

This manual documents the uncharacterized PSI card (that is, without firmware installed). If you purchased the card with firmware installed, you should have received another manual, providing information specific to the firmware.

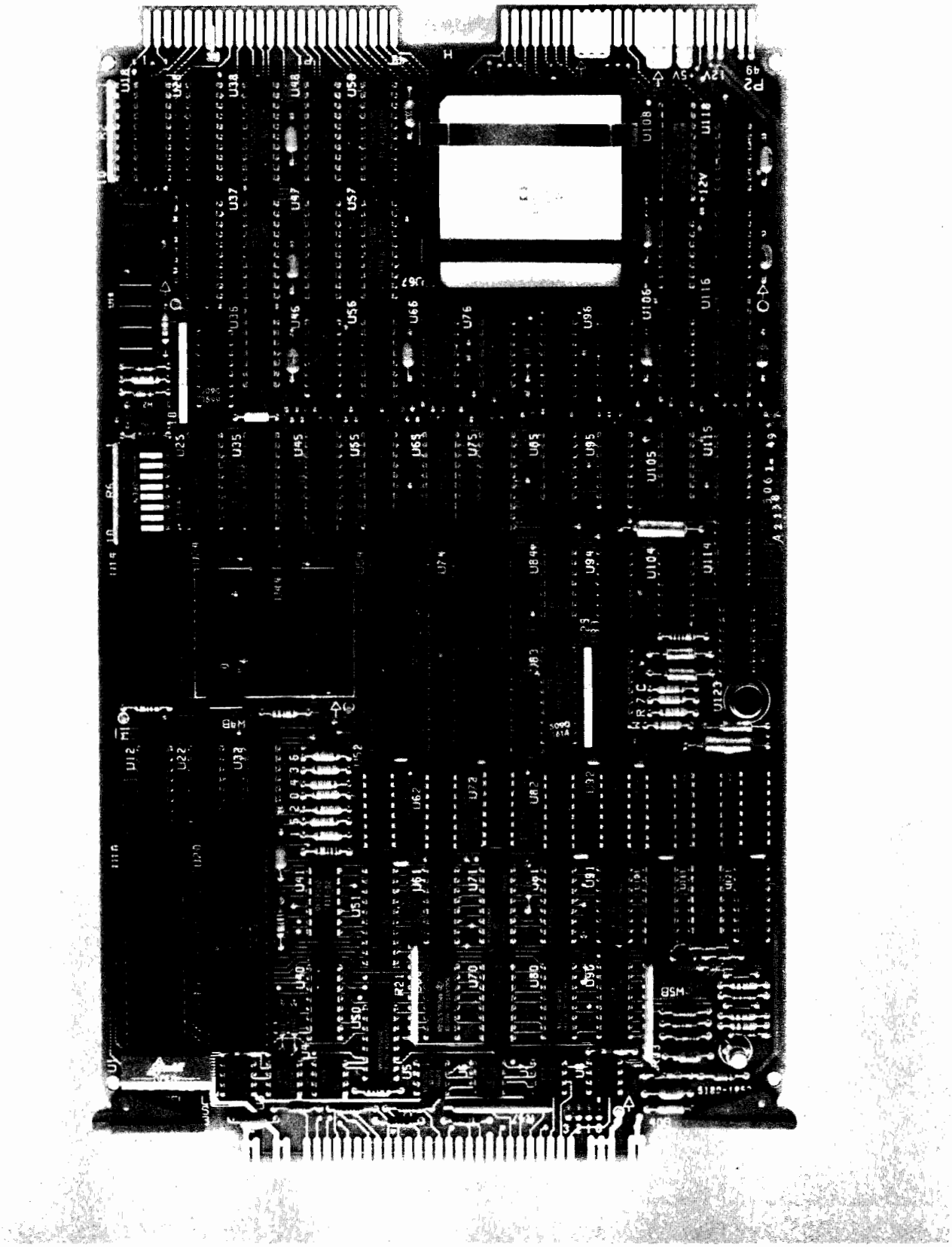


Figure 1-1. PSI Card

General Information
Chapter 1

This manual provides general information, installation procedures, principles of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the L/A-Series Programmable Serial Interface (PSI) Card. This chapter contains general information concerning the PSI, and includes a description and specifications.

Description

The PSI circuit card is shown in figure 1-1. Two 50-pin edge connectors connect the card to an HP 1000 L/A-Series Computer backplane, and one 80-pin edge connector connects the card, via an interface cable, to a modem.

The PSI card provides an HP 1000 L/A-Series Computer with the capability to support a modem communications link in accordance with various communications protocols. These protocols are defined by such specifications as Electronic Industries Association Standards RS-449, RS-232-C, etc., and the International Telegraph and Telephone Consultive Committee Recommendations V.24, V.28, X.25, etc.

Up to two ROMs/EPROMs are used to program the card for different applications. The ROM firmware is explained in separate manuals, depending on the application. Thus, a product of which the PSI is a part will consist of:

The PSI Printed Circuit Assembly (also referred to as a card in this manual), part number 5061-4912.

One or two ROMs or EPROMs (mounted on the card).

ROM/EPROM firmware installation manual (the part number will depend on the product).

Up to nine jumper plugs (mounted on the card).

L/A-Series I/O Processor (IOP), part number 1AF5-6001. This part will be mounted on the card using two spring clips, part number 1200-0845.

An EIA RS-232-C interface cable (standard), or an optional RS-449 interface cable.

This manual, part number 12042-91001.

Functional Description

A simplified block diagram of the PSI is shown in figure 1-2. The PSI is an intelligent interface card utilizing the IOP and related circuitry and a Z-80A microprocessor, and, in addition to supporting many different communications protocols, is capable of relieving a large amount of host CPU overhead.

The PSI communicates with the HP 1000 host computer through the IOP. A Z-80A Counter/Timer Circuit (CTC) and a Z-80A Serial Input/Output (SIO) are used to handle interface to the modem; and two Z-80A Direct Memory Access (DMA) controllers are used to control DMA between the card and the host CPU and between the card memory and SIO channel A.

A Z-80A CPU controls the SIO, CTC, and DMAs.

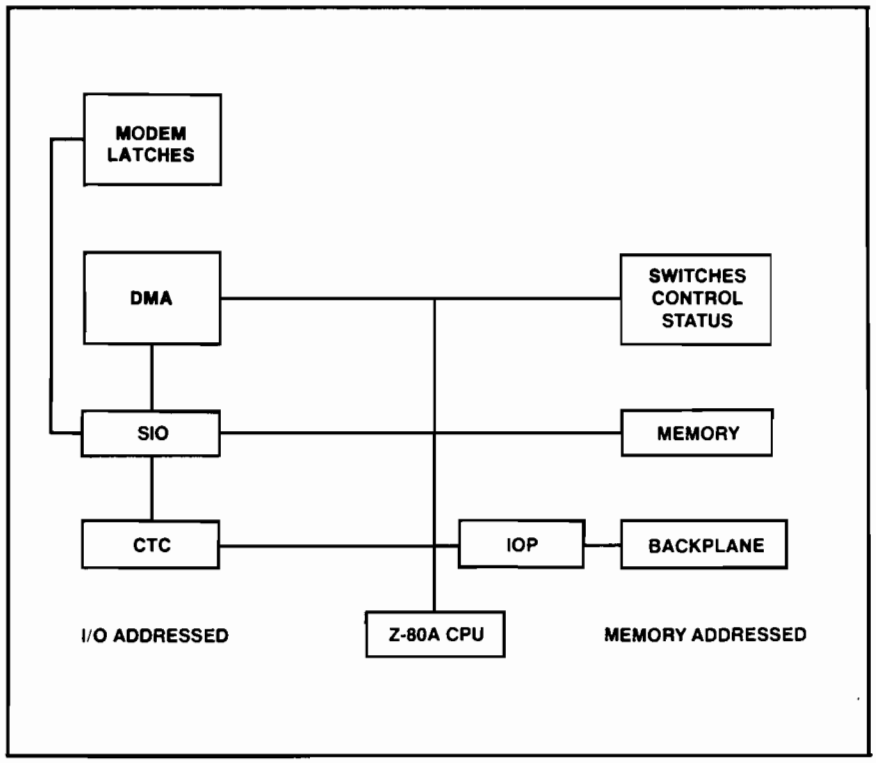


Figure 1-2. PSI Simplified Block Diagram

Identification

The Product

Five digits and a letter (e.g., 12042A) are used to identify HP products used with HP computers. The five digits identify the product, and the letter indicates the revision level. Note that the PSI card is not a product by itself, it is merely one part of an HP 1000 Computer System interface product (other parts of the product are the manuals, ROMS (or EPROMs), an interface cable, etc.). The complete product is described in the firmware manual.

The Circuit Card

The PSI card is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a four-digit date code (e.g., A-2138). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number of the PSI card is:

5061-4912
A-2138

If the date code on the card does not agree with the one on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (offices are listed at the back of this manual).

Service Manual

The manual supplied with the PSI card is identified by its name and part number. The part number (12042-91001) and publication date are printed on the title page. If the manual is revised, the publication date is changed. The Print History page (page ii) records the reprint dates.

Modem Compatibility

There are many modems that can be used with the PSI card. All modem control lines for EIA RS-232-C and RS-449, and CCITT V.10, V.11, V.24, and V.28 are made available by the hardware. The firmware, however, will determine compatibility with specific modems.

Specifications

Table 1-1 lists the specifications of the PSI Card. Note that these specifications are for the PSI card hardware only; they do not reflect the characteristics of a complete product with ROMs/EPROMs mounted. Product specifications are contained in the firmware manual which describes that particular product.

Table 1-1. Specifications

HARDWARE CHARACTERISTICS Z-80A CPU based microprocessor control 4 mHz Z-80A-family microprocessor components
One Z-80A SIO/2 dual Serial I/O channel controller: Two independent full duplex channels Data rates Asynchronous 57K bits per second maximum 50 bits per second minimum Synchronous 460K bits per second maximum 50 bits per second minimum Maximum speed with external clock: 810K bps 810K bps (the firmware will be the limiting factor in achieving this speed) Asynchronous features 5, 6, 7 or 8 bits per character 1, 1-1/2 or 2 stop bits Even, odd, or no parity X1, X16, X32, or X64 clock modes Break generation and detection Parity, overrun, and framing error detection

Table 1-1. Specifications (Continued)

Character-oriented protocol (BISYNC) features
One or two sync characters
Automatic sync character insertion and deletion
CRC generation and checking
Bit-oriented protocol (HDLC, SDLC) features
Abort sequence generation and checking
Automatic zero insertion and deletion
Address field recognition
Support for one to eight bits per character
Valid receive messages protected from overrun
CRC generation and checking
CRC-16 or CRC-CCITT block frame check
Two modem control inputs and two modem control outputs per channel.

Table 1-1. Specifications (Continued)

The option of generating a vectored interrupt per channel: When the state of an SIO modem control input changes, When the transmit buffer is empty, When a receive character is available, When Special Receive Conditions occur: Parity error Receiver overrun error CRC/Framing error End of frame (HDLC, SDLC, LAP-B)
Two Z-80A DMA Direct Memory Access Controllers, Between memory and channel A of the SIO Between memory and the backplane I/O data latches
16K bytes of dynamic RAM, for tables, buffers, and/or firmware.
Two ROM/EPROM sockets (max 8K bytes per socket, 16K bytes max total), capable of using almost any combination of: 2716s, 2732s, 2764s, 2516s, 2532s, and other similar devices.
EIA RS-422 and EIA RS-423 Line Drivers and Receivers. 6 input lines (pairs) with balanced receivers 4 output lines (pairs) with balanced drivers, with duplicate unbalanced drivers. 8 output lines with unbalanced drivers 8 input lines with unbalanced receivers

Table 1-1. Specifications (Continued)

The drivers and receivers are capable of implementing:

A single EIA RS-449 compatible link

Two (2) EIA RS-232-C compatible links which can control Bell 201(B,C), 208(A,B), or 209(A,B) modems.

A single fully supported EIA RS-232-C compatible link

A CCITT V.24/V.28 compatible link

Self-test Mode. Via firmware control, the PSI card's line interface can be placed into a self-test mode where:

The output of the Send Data line driver is looped back to the receive data input of the SIO on both channels A and B.

The CTC generated data clocks are routed back into the transmit and receive clock inputs of their respective SIO channels.

Multi-Drop Capability:

The EIA RS-422 line drivers for Terminal Timing and Request-to-Send can be placed in a high impedance state under firmware control. The Terminal Ready and Send Data line drivers can individually be placed into a high impedance state under firmware control.

Four programmable indicator lights (LEDs).

Eight switches, accessible as a single byte.

POWER REQUIREMENTS

VOLTAGE	CURRENT	POWER DISSIPATION
+ 5 V	2.550 A	12.75 W
+12 V	0.351 A	4.21 W
-12 V	0.174 A	2.09 W
	Total:	19.05 W

Table 1-1. Specifications (Continued)

PHYSICAL CHARACTERISTICS:	
Size:	17.15 by 28.91 centimeters (6.75 by 11.38 inches)
Weight:	
Backplane Interconnects:	Two 50-pin edge connectors plug into two sockets (P1 and P2) mounted on the backplane.
Device Interconnects:	One 80-pin edge connector (J1) on which a cable hood may be connected.

Installation
Chapter 2

This chapter provides information on unpacking, inspecting, installing, and checking the operation of the PSI Card.

Unpacking and Inspection

Inspect the shipping package immediately upon receipt to detect any evidence of mishandling during transit. If the package is damaged, ask that the carrier's agent be present when the product is unpacked. Carefully unpack the card and accessories and inspect for damage (scratches, broken components, etc.). If damage is noticed, notify the carrier and the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Return the carton and packing material for the carrier's inspection.

After inspecting all components, refer to the equipment supplied information in the product manual to ensure that the product is complete. Also check the part numbers listed in that chapter against the part numbers on the product components. If the product is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

After unpacking, inspecting, and checking part numbers of all parts of the product, follow installation and checkout procedures as defined in this chapter.

Computation of Current Requirements

The PSI obtains its operating voltages from the computer power supply through the backplane. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the PSI card are listed in the power requirements entry of table 1-1. Current specifications for all other interfaces can be found in the appropriate Reference or Installation and Service Manuals.

Firmware Installation

CAUTION

STATIC SENSITIVE DEVICES

THE IOP, ROMS/EPROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

Refer to figure 2-1 for correct installation positioning of the firmware EPROM/ROMS.

Configuration Jumpers

A set of jumpers on the PSI card provides the option of using different ROM/EPROM parts. The set consists of a 14-pin socket housing seven removable jumpers (XW1A through XW1G), and one hardwired jumper (W6). Check to see that XW1A through XW1G are configured as described in tables 2-1 and 2-2 for the specific ROM/EPROMs that are installed. (The hardwired jumper, W6, is configured at the factory.) Refer to figure 2-1 for the physical locations of the jumpers on the card. Functional locations of the jumpers are shown on the schematic logic diagram (figure 6-2, sheet 2, in Chapter 6).

Two additional jumpers, W4 and W5 (see figure 2-1 for the physical locations and figure 6-2, sheet 2, for the functional locations), are configured according to the function for which the card is to be used. Jumper W4 must be in the A position during normal operation and when testing the interface with a Diagnostic or Loop-back hood installed. This configuration releases the Terminal Ready line (TR) to firmware control. Refer to the applicable firmware manual for applications requiring this jumper to be placed in position B. Jumper W5, normally in the A position, should be set to the B position when the PSI card is to be used as an HP Data Link Master. Refer to the applicable firmware manual for the exact configurations of jumpers W4 and W5.

Table 2-1. ROM/EPROM Categories According to Part Type

CATEGORY	HP PART NO.	PART TYPE NO.
A	1818-0762	TI 2532
B	1818-0498	TI 2516 Intel 2716
C	1818-0850 (No HP P/N) 1818-1747	Intel 2732 Intel 2332 Intel 2764

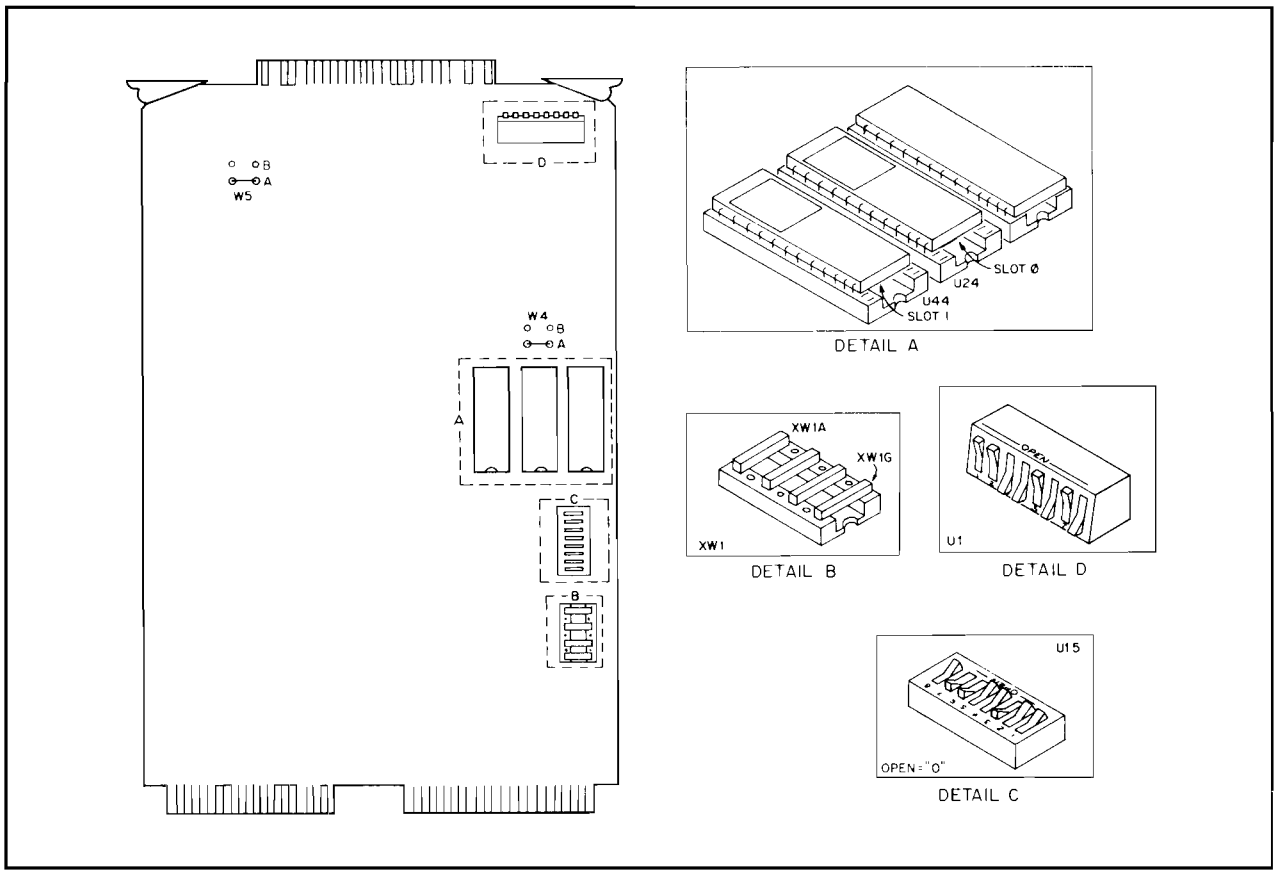


Figure 2-1. ROM/EPROM, Jumpers, and DIP Switch Locations

Table 2-2. Jumper Requirements for all ROM/EPROM Combinations (X denotes a required jumper)

ROM/EPROM CATEGORY		X W 1 A	X W 1 B	X W 1 C	X W 1 D	X W 1 E	X W 1 F	X W 1 G
U24	U44							
C	C					X		
A	A				X	X	X	X
C	A			X		X	X	
B	A			X		X	X	X
B	B			X	X	X	X	X
A	C	X				X		X
C	B	X			X	X	X	
A	B	X		X	X	X	X	X
B	C	X		X		X		X

DIP Switch U15 Configuration

The card provides a Dual In-line Package (DIP), U15, containing eight switches which may be sensed by the firmware. This set of switches can be used to determine such parameters as the information field size, the transmit clock rate, and associated time-out values, etc., depending on the firmware implementation. The transmit clock rate should be set to indicate the clock rate that is supplied by the modem being used. Refer to figure 2-1 for switch positions on the card, and to the firmware manual for switch settings.

DIP Switch U1 Configuration

The card provides another pack of eight switches, U1, which is used to specify interface configuration information such as Virtual Control Panel (VCP) interface selection, ground reference, and interface card select code. Locations of the switches are shown in figure 2-1, and the functions of the eight switches are presented in table 2-3. Refer to the firmware manual for settings.

Switch 2 of DIP Switch U1 is used to compensate the grounding conditions for the card. Under normal operation, the card obtains its ground reference via a ground clip on the interface cable which makes contact with the chassis when the card cage door is shut. Switch 2 MUST BE OPEN when the door is closed to eliminate conflicting ground references. To operate with the card cage door open, Switch 2 must be closed.

Table 2-3. DIP Switch U1 Configuration

SWITCH	FUNCTION
1	Closed to enable VCP. Open to disable VCP.
2	Must be OPEN if card cage door is closed. Must be CLOSED if card cage door is open.
3 - 8	Card select code (octal). Switch 8 is the least significant bit.

Backplane Interface

All interface between the PSI card and the host computer occurs on the computer backplane. Two 50-pin edge connectors (P1 and P2) connect the PSI card to the backplane. Connections to P1 and P2 are shown in tables 2-4 and 2-5.

Datacomm Interface

The front edge (datacomm) connector is an 80-pin connector which allows the PSI card to be connected to a modem. Connections to this connector (J1) are shown in table 2-6.

A comparison of EIA RS-232-C and RS-449, and CCITT V.24/V.28 circuits and their respective signal connector pin assignments is shown in table 2-7.

Card and Cable Installation

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO FOLLOW THESE DIRECTIONS COULD RESULT IN DAMAGE TO THE EQUIPMENT.

After ensuring that the computer power supply can handle the added load, that the ROMs/EPROMs are properly installed, and that the DIP switches and jumpers are configured properly (see the firmware manual), perform the following steps:

1. Turn off power at the computer and the modem. Install the PSI card in the desired slot in the computer card cage, noting the select code. The card should be oriented the same as all other cards in the computer: components on the top side of the card in a horizontal rack, on the right side in a vertical rack. Press the card firmly into place.

2. Connect the cable supplied with the product to the interface card and modem. Ensure that the cable connectors are oriented in the same manner as the connectors on other cards in the computer.

3. Restore power to the computer and modem.

Interface Card LEDS

There are four LEDs on the interface card. Located on the right side of the card next to the front edge connector, the LEDs are visible when the card is installed in the computer and are referenced as 0 through 3 with 0 being the LED on the right. These LEDs can be used as firmware controlled indicators.

Checkout Procedure

Checkout procedure for the PSI card depends on the firmware and whether or not a self-test is programmed into the ROM/EPROMs. Refer to the firmware manual for your particular product for PSI card checkout.

Reshipment

If the PSI card is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the PSI card.

Remove the IOP (see Chapter 4 for removal instructions) and the ROMs/EPROMs from the card. Pack the card in the original factory material. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack the item.

Table 2-4. Backplane Connector P1

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
1	ICHID-	Interrupt Chain In Disable
2	ICHOD-	Interrupt Chain Out Disable
3	MCHID-	Memory Chain In Disable
4	MCHOD-	Memory Chain Out Disable
5	MLOST-	Memory Lost
6	MCHODOC-	Mem Chain Out Disable Open Collector
7	PFW-	Power Fail Warning
8	(SPARE 1)	
9	SCB0	Select Code Bus Bit 0
10	SCB1	Select Code Bus Bit 1
11	SCB2	Select Code Bus Bit 2
12	SCB3	Select Code Bus Bit 3
13	GND	Ground
14	GND	Ground
15	(SPARE 2)	
16	GND	Ground
17	SCB4	Select Code Bus Bit 4
18	SCB5	Select Code Bus Bit 5
19	AB0	Address Bus Bit 0
20	AB1	Bit 1
21	AB2	Bit 2
22	AB3	Bit 3
23	AB4	Bit 4
24	AB5	Bit 5
25	AB6	Bit 6

Table 2-4. Backplane Connector P1 (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
26	AB7	Bit 7
27	AB8	Bit 8
28	AB9	Bit 9
29	AB10	Bit 10
30	AB11	Bit 11
31	AB12	Bit 12
32	AB13	Bit 13
33	AB14	Bit 14
34	WE-	Write Enable
35	DB0	Data Bus Bit 0
36	DB1	Bit 1
37	DB2	Bit 2
38	DB3	Bit 3
39	DB4	Bit 4
40	DB5	Bit 5
41	DB6	Bit 6
42	DB7	Bit 7
43	DB8	Bit 8
44	DB9	Bit 9
45	DB10	Bit 10
46	DB11	Bit 11
47	DB12	Bit 12
48	DB13	Bit 13
49	DB14	Bit 14
50	DB15	Bit 15

Table 2-5. Backplane Connector P2

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
1	(SPARE 3)	
2	ISOGND	Isolated Ground
3	REMEM-	Remote Memory
4	VALID-	Data Valid
5	IORQ-	I/O Handshake Request
6	INTRQ-	Interrupt Request
7	MP	Memory Protect
8	RNI	Read Next Instruction
9	MEMGO-	Memory Cycle Initiation
10	PE-	Parity Error
11	SCHID-	Slave Chain In Disable
12	SCHOD-	Slave Chain Out Disable
13	IAK-	Interrupt Acknowledge
14	IOGO-	I/O Handshake Request Acknowledge
15	ISOGND	Isolated Ground
16	SLAVE-	Slave Request
17	ISOGND	Isolated Ground
18	MRQ-	Memory Request
19	ISOGND	Isolated Ground
20	FCLK-	Fast Clock
21	ISOGND	Isolated Ground
22	CCLK-	Communications Clock
23	PS-	Parity Sense
24	SCLK-	System Clock
25	CRS-	Control Reset

Table 2-5. Backplane Connector P2 (Continued

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
26	PON	Power On
27	ISOGND	Isolated Ground
28	BUSY-	Memory Busy
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	GND	Ground
33	GND	Ground
34	GND	Ground
35	+5V	
36	+5V	
37	+5V	
38	+5V	
39	+12V(MEM)	
40	-12V(MEM)	
41	+12V	
42	+12V	
43	-12V	
44	-12V	
45	+5V(MEM)	
46	+5V(MEM)	
47	25KHz	
48	25KHz	
49	25KHz	
50	25KHz	

Table 2-6. Datacomm Connector J1

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
1A	---	No Connection
1B	+12V	+12 Volts Power
2A	---	No Connection
2B	+12V	+12 Volts Power
3A	SSD	Secondary Send Data
3B	---	No Connection
4A	---	No Connection
4B	-12V	-12 Volts Power
5A	---	No Connection
5B	-12V	-12 Volts Power
6A	---	No Connection
6B	---	No Connection
7A	SRS	Secondary Request to Send
7B	TR(A)	Terminal Ready
8A	SD(U)	Send Data
8B	TT(B)	Terminal Timing
9A	RS(U)	Request to Send
9B	TT(U)	Terminal Timing
10A	TR(B)	Terminal Ready
10B	DAMPRT(B)	
11A	RS(A)	Request to Send
11B	TR(U)	Terminal Ready
12A	TT(A)	Terminal Timing
12B	---	No Connection
13A	SD(B)	Send Data
13B	SD(A)	Send Data
14A	---	No Connection
14B	RS(B)	Request to Send
15A	DAMPST(B)	
15B	RT(B)	Receive Timing
16A	CS(B)	Clear To Send
16B	DAMPRD(B)	
17A	CS(A)	Clear to Send
17B	---	No Connection
18A	SQ	Signal Quality
18B	RC	Receive Common
19A	ST(B)	Send Timing
19B	---	No Connection
20A	RD(B)	Receive Data
20B	ST(A)	Send Timing
21A	---	No Connection
21B	**BX16IN	
22A	SRR	Secondary Receiver Ready
22B	DM	Data Mode (RS-423, RS-449)

Table 2-6. Communication Line Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
23A	RD(A)	Receive Data
23B	TM	Test Mode
24A	RR(B)	Receiver Ready
24B	IC	Incoming Call
25A	SG	Signal Ground
25B	SC	Signal Common
26A	RR(A)	Receiver Ready
26B	**BDATACLK+	
27A	DM(A)	Data Mode (RS-232-C)
27B	DM(B)	Data Mode (RS-232-C)
28A	SF/SR	Select Frequency/Signaling Rate
28B	DD	Receive Timing
29A	**ASYNCCLK+	
29B	DA	Terminal Timing
30A	**X16IN	
30B	RT(A)	Receive Timing
31A	SCS	Secondary Clear to Send
31B	DB	Send Timing
32A	SRD	Secondary Receive Data
32B	RL	Remote Loopback
33A	LL	Local Loopback
33B	NS	New Signal
34A	IS	Terminal In Service
34B	---	No Connection
35A	---	No Connection
35B	GND	Power Ground
36A	---	No Connection
36B	GND	Power Ground
37A	---	No Connection
37B	GND	Power Ground
38A	(SHIELD)	
38B	---	No Connection
39A	---	No Connection
39B	+5V	+5 Volts Power
40A	---	No Connection
40B	+5V	+5 Volts Power

* The (A) or (B) after a mnemonic indicates portions of a differential input or output.
The (U) after a mnemonic indicates a single ended version of a signal that appears elsewhere as differential.

** These are TTL level signals for compatibility, they should be used only to loop back for proper firmware operation.

Table 2-7. Serial I/O Circuits and Equivalents

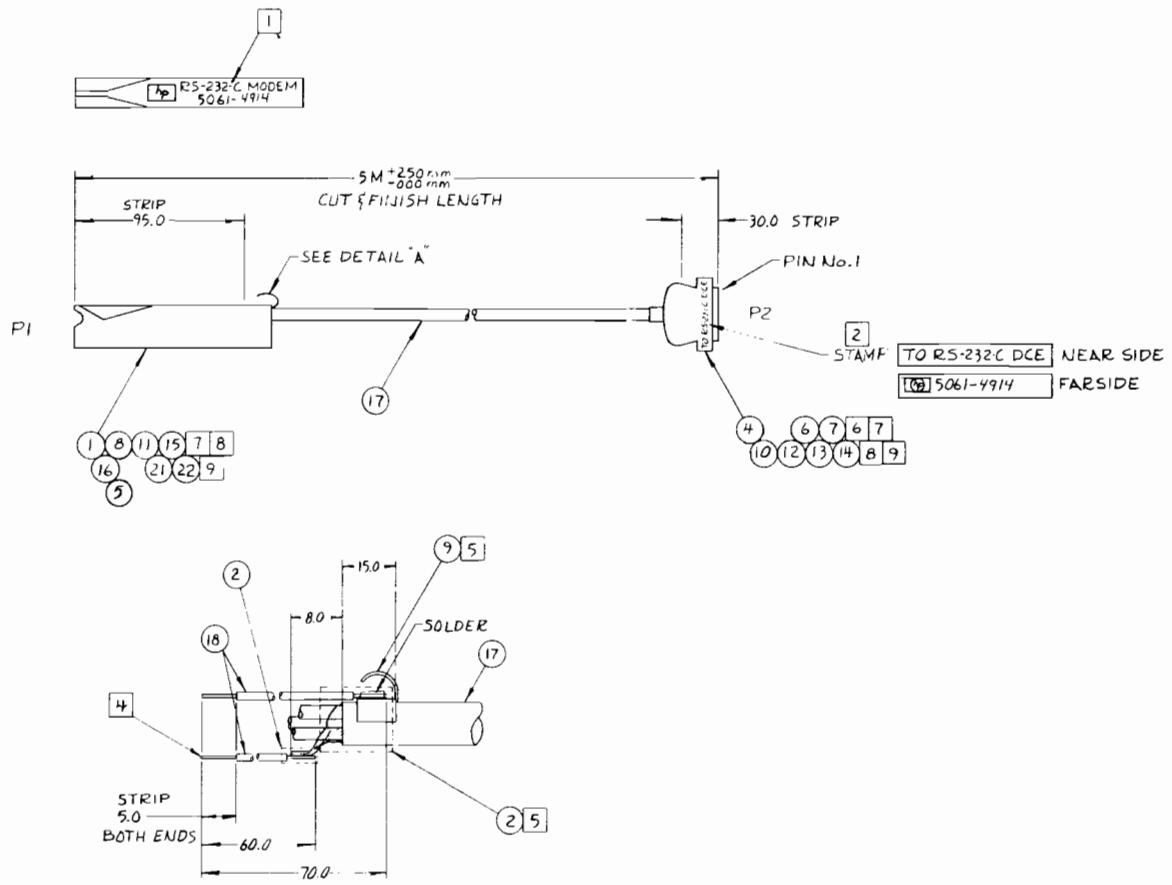
SIGNAL DESIGNATION			DEFAULT VALUE	FUNCTION
RS-449	RS-232-C	CCITT V.24/V.28		
RD	BB	104	---	RECEIVE DATA
SD	BA	103	1	SEND DATA
CS	CB	106	---	CLEAR TO SEND
RS	CA	105	0	REQUEST TO SEND
TR	CD	108.2	0	TERMINAL READY
RR	CF	109	---	RECEIVER READY
ST	DB	114	---	SEND TIMING
RT	DD	115	---	RECEIVE TIMING
TT	DA	113	---	TERMINAL TIMING
IC	CE	125	---	INCOMING CALL
DM	CC	107	---	DATA MODE
TM	--	142	0	TEST MODE
LL	--	141	0	LOCAL LOOPBACK
RL	--	140	0	REMOTE LOOPBACK
SQ	CG	110	---	SIGNAL QUALITY
SF	CH	126	0	SELECT FREQUENCY
SR	CH	111	0	SELECT SIGNALING RATE
IS	--	---	1	TERMINAL IN SERVICE
NS	--	---	0	NEW SIGNAL
SRD	SBB	119	---	SEC. RECEIVE DATA
SSD	SBA	118	1	SEC. SEND DATA
SRS	SCA	120	0	SEC. REQUEST TO SEND
SCS	SCB	121	---	SEC. CLEAR TO SEND
SRR	SCF	122	---	SEC. RECEIVER READY
SG	AB	102	---	SIGNAL GROUND
SC	--	102a	---	SEND COMMON
RC	--	102b	---	RECEIVE COMMON
--	AA	101	---	PROTECTIVE GROUND

NOTES:

1. STAMP P1 HOOD AS SHOWN, REF DWG A-5950-5669-1.
2. STAMP P2 SHELL HALVES AS SHOWN, REF DWG A-5951-3021-1.
3. STRIPPING TABLE

CONNECTOR	JACKET	SHIELD	WIRE
P1	95.0	87.0	6.0
P2	30.0	30.0	4.0

4. FABRICATE SHIELD, P1 (SEE DETAIL A) TWIST 8.0 OF SHIELD, CUT A 60.0 PIECE OF WIRE (ITEM 18), STRIP BOTH ENDS 5.0, SOLDER ONE END OF WIRE ONTO TWISTED SHIELD, SLIDE A 10.0 PIECE OF SHRINK TUBING (ITEM 3) OVER SOLDERED AREA AND SHRINK.
5. FABRICATE GROUNDING SPRING (ITEM 9) - SEE DETAIL "A", CUT A 70.0 PIECE OF WIRE (ITEM 18), STRIP BOTH ENDS 5.0 AND SOLDER ONE END ONTO GNDG SPR. PLACE GNDG SPR ON CABLE, SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) OVER GNDG SPR AND SHRINK.
6. SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) COVERING 10.0-15.0 OVER THE END OF THE OUTER JACKET.
7. CAPTURE UNUSED WIRE WITH A 15.0 PIECE OF SHRINK TUBING (ITEM 3).
8. SLIDE A 8.0 PIECE OF SHRINK TUBING (ITEM 3) TO INSULATE ADJACENT CONNECTION.
9. ASSEMBLE P1 PER B-5951-5613-1, P2 PER B-5951-7369-1
10. TEST FINISHED CABLE ASSY ON BED CABLE TESTER



DETAIL 'A'

P1

PC-EDGE MNEMONIC	WIRE COLOR	A	B	WIRE COLOR	PC-EDGE MNEMONIC
SSD	917	3	3		
SRS	903	7	7		
SD(U)	91X	8	8		
RS(U)	912	9	9	94X	RT(U)
		10	10		
		11	11	4XX	TR(U)
		12	12		
		13	13		
		14	14		
		15	15		
		16	16		
C3(A)	913	17	17		
SQ	915	18	18		
		19	19		
		20	20	96X	ST(A)
		21	21		
SRR	905	22	22		
RD(A)	93X	23	23		
		24	24	3XX	IC
SG	1XX	25	25		
RR(A)	914	26	26		
DM(A)	6XX	27	27		
SF/SR	916	28	28		
		29	29		
		30	30	901	RT(A)
SCS	904	31	31		
SRD	902	32	32		
		33	33		
		34	34		
		35	35		
		36	36		
		37	37		
AA	SHIELD	38	38		
		39	39		
		40	40		

19
GNDG SPRG

CABLE ENTRY WIRE VIEW

P2

RS-232-C MNEMONIC	WIRE COLOR			WIRE COLOR	RS-232-C MNEMONIC
AA	SHIELD	1	14	917	SBA
BA	91X	2	15	96X	DB
BB	93X	3	16	902	SBB
CA	912	4	17	901	DD
CB	913	5	18		
CC	6XX	6	19	903	SCA
AB	1XX	7	20	4XX	CD
CF	914	8	21	915	CG
		9	22	3XX	CE
		10	23	916	CH
		11	24	94X	DA
SCF	905	12	25		
SCB	904	13			

WIRE VIEW

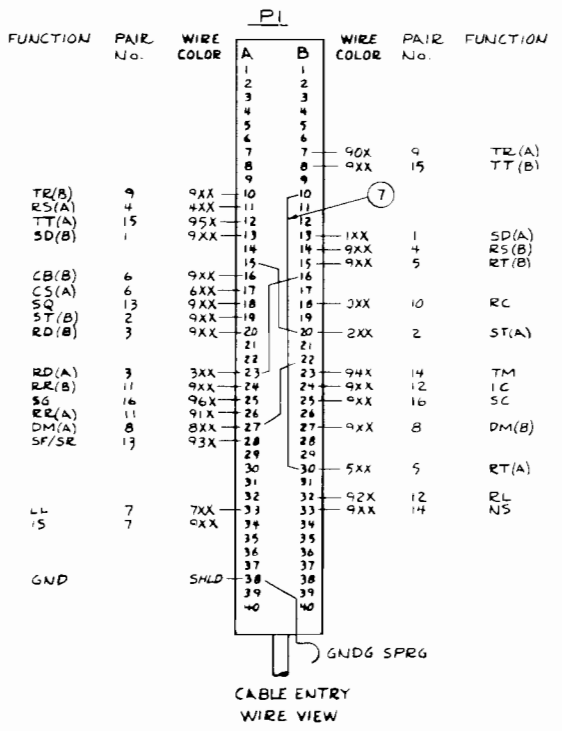
Figure 2-2.
RS-232-C Modem Interface Cable Schematic Diagram

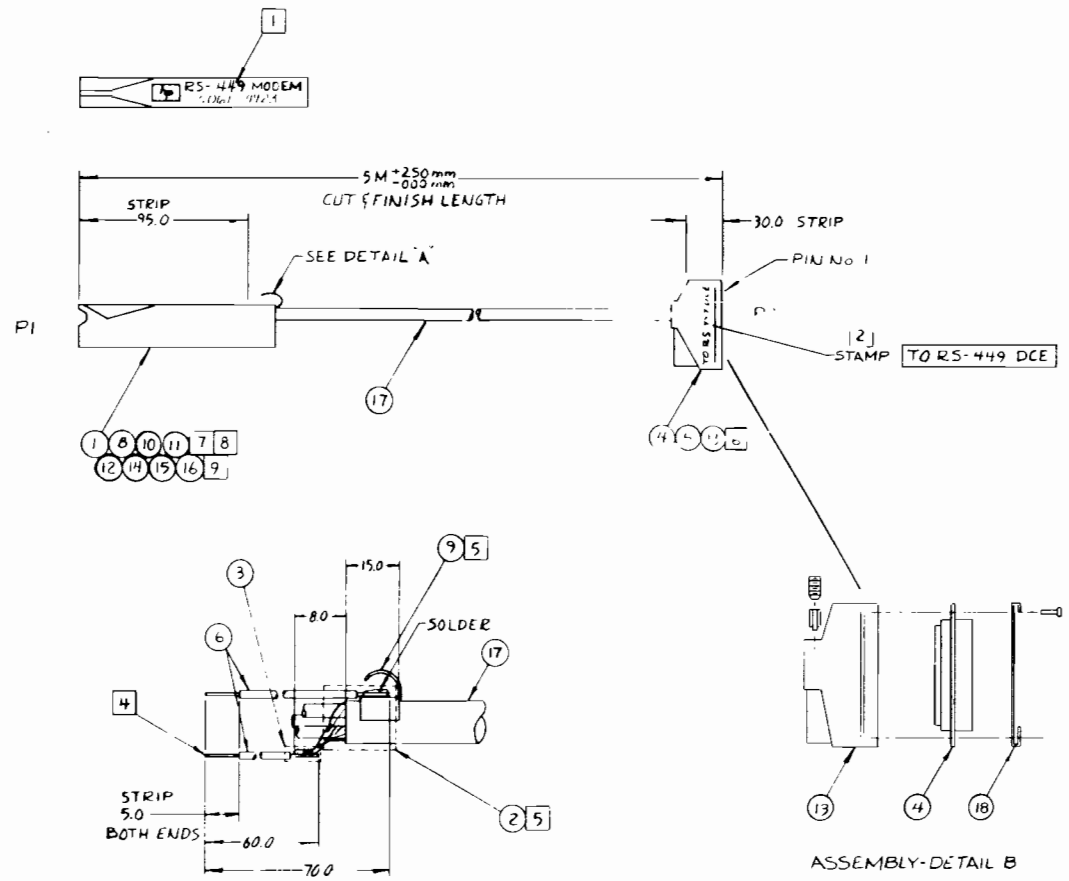
NOTES:

1. STAMP P1 HOOD AS SHOWN, REF DWG A-5950-5669-1.
2. STAMP P2 SHELL HALVES AS SHOWN.
3. STRIPPING TABLE

CONNECTOR	JACKET	SHIELD	WIRE
P1	95.0	87.0	6.0
P2	30.0	30.0	4.0

4. FABRICATE SHIELD, P1 (SEE DETAIL A) TWIST 8.0 OF SHIELD, CUT A 60.0 PIECE OF WIRE (ITEM 6), STRIP BOTH ENDS 5.0, SOLDER ONE END OF WIRE ONTO TWISTED SHIELD, SLIDE A 10.0 PIECE OF SHRINK TUBING (ITEM 2) OVER SOLDERED AREA AND SHRINK.
5. FABRICATE GROUNDING SPRING (ITEM 9) - SEE DETAIL "A", CUT A 70.0 PIECE OF WIRE (ITEM 18), STRIP BOTH ENDS 5.0 AND SOLDER ONE END ONTO GNDG SPR. PLACE GNDG SPR ON CABLE, SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) OVER GNDG SPR AND SHRINK.
6. SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) COVERING 10.0-15.0 OVER THE END OF THE OUTER JACKET.
7. CAPTURE UNUSED WIRE WITH A 15.0 PIECE OF SHRINK TUBING (ITEM 3).
8. SLIDE A 8.0 PIECE OF SHRINK TUBING (ITEM 3) TO INSULATE ADJACENT CONNECTION.
9. ASSEMBLE P1 PER B-5951-5613-1, P2 PER DETAIL "B".
10. TEST PER A-5950-~~0975~~-1 "CABLE TESTER" USE ET-4530-018 AND ET-4530-007





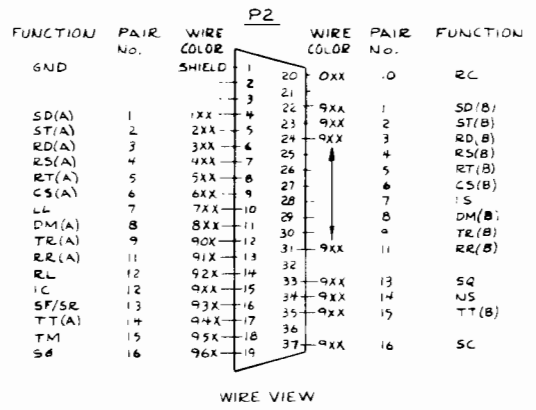


Figure 2-3.
RS-449 Modem Interface Cable
Schematic Diagram (Opt. 002)

Principles of Operation
Chapter 3

This chapter contains a description of the operation of the PSI card. The card consists of the following major functional areas:

HP 1000 L/A-Series Computer I/O Master interface with IOP

Z-80A Microprocessor subsystem (CPU, SIO/2, DMA and CTC)

Read-Only Memory (ROM/EPROM)

Random-Access Memory (RAM)

Communication line interface

A block diagram illustrating the major functional areas of the card is presented in figure 3-1. Each area is explained in detail in the following sections.

I/O Master-Communications Card Interface

The card communicates with the HP 1000 host computer through the I/O Master circuitry physically implemented on the card. The I/O Master consists of the I/O Processor (IOP) and related circuitry. The circuitry that interfaces this card to the I/O Master can be divided into two major sections: the I/O data latches and the control circuitry section.

The I/O data latches consist of two 8-bit input latches and two 8-bit output latches. The input latches hold 16-bit data words or commands from the host computer until the card is ready to accept them. Similarly, the output latches hold 16-bit status words or data output to the computer.

The control circuitry consists of two flip-flops, a Bus Control State latch and various other gate-level logic elements. The primary function of this section is to handle the control signals to and from the I/O Master. These signals are used to generate and acknowledge interrupts, to handshake data between the host and the card and to conform to the standard HP 1000 L/A-Series Computer I/O Master signal conventions. For a more detailed discussion of these and other I/O signals, refer to the HP 1000 L/A-Series I/O Interfacing Guide, HP part number 02103-90005.

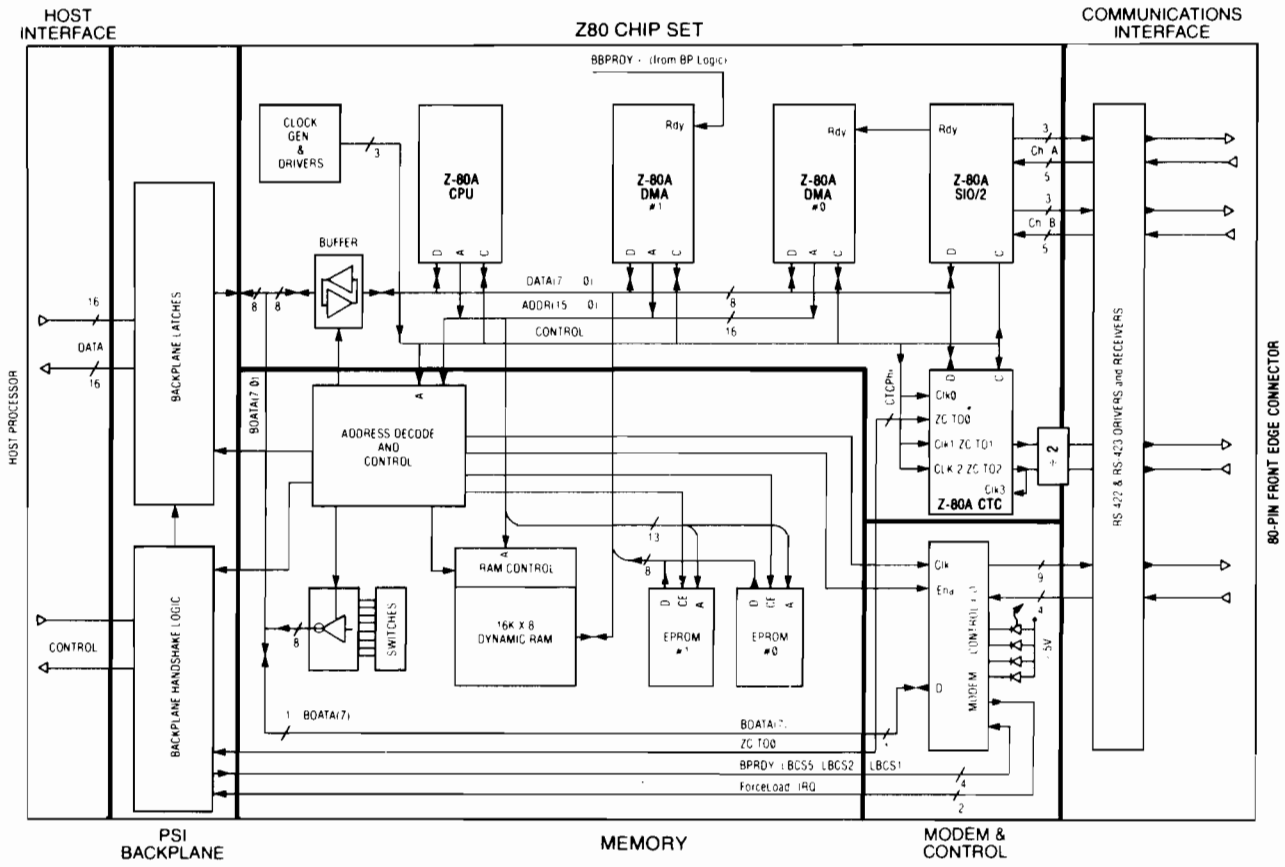


Figure 3-1. PSI Card Functional Block Diagram

Z-80A Microprocessor Subsystem

The heart of the PSI card is the Z-80A CPU (Central Processing Unit). This MOS LSI microprocessor operates from a single 5-volt supply, uses a single phase clock and has a typical instruction execution time of 1 microsecond. The data bus is eight bits wide, and the address bus is sixteen bits wide. All CPU pins are TTL compatible.

The Z-80A CPU employs a register-based architecture which includes two sets of six general-purpose registers which can be used as 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include stack pointer, program counter and two index registers. The Z-80A CPU provides the intelligence for the card to function as a preprocessor to relieve the host computer of a majority of protocol processing.

An important pin on the Z-80A CPU as far as this interface is concerned is the NMI (Non-Maskable Interrupt) input pin. By pulling this input low with an STC instruction, the host computer can "get the attention of" the Z-80A CPU. An NMI is the highest priority interrupt to the Z-80A CPU and forces it to start fetching and executing instructions from a predetermined location in the firmware. The host software driver uses this feature to issue commands to the card (commands from the host cannot be ignored).

Various support circuits are used in conjunction with the Z-80A CPU to facilitate the card's operation as an intelligent serial interface. These circuits are discussed in the paragraphs that follow.

Serial Input/Output (SIO)

A Z-80A SIO is used on the card to provide the serial data communications channel. The major functions performed by the SIO are serial-to-parallel conversion of input data and parallel-to-serial conversion of output data.

Direct Memory Access (DMA)

Two Z-80A LSI DMA conntrollers are used by the PSI card. One of the DMAs is used to transfer data between the SIO channel and the card memory; the other is used to transfer data between the host computer and the card memory. The function of the DMA logic is to transfer bytes of data in a manner that will be transparent to the Z-80A CPU. This enables the card to achieve higher throughput rates.

Counter Timer Circuit (CTC)

One Z-80A Counter/Timer Circuit (CTC) is used to provide four independent counter/timers. One of the counter/timers may be used as a baud rate generator for SIO channel A. Another may be used as a baud rate generator for SIO channel B. Either of these could be used as timers by the firmware if they are not needed as baud rate generators. A third timer is available to the firmware. The fourth timer is used to maximize the effective throughput of the card by controlling the frequency of DMA cycle stealing.

Read-Only Memory (ROM/EPROM)

Two 28-pin sockets are provided for ROMs/EPROMs. All of the software required for the Z-80A CPU to implement the functions of protocol generation, modem control, and backplane interaction control is contained in these ROMs/EPROMs and is referred to as firmware.

Random-Access Memory (RAM)

The card has 16K bytes of dynamic RAM. This memory is used for data buffers and the storage of firmware variables. The refresh capability of the Z-80A CPU is used to provide the appropriate refresh signals to the dynamic RAM.

Communication Line Interface

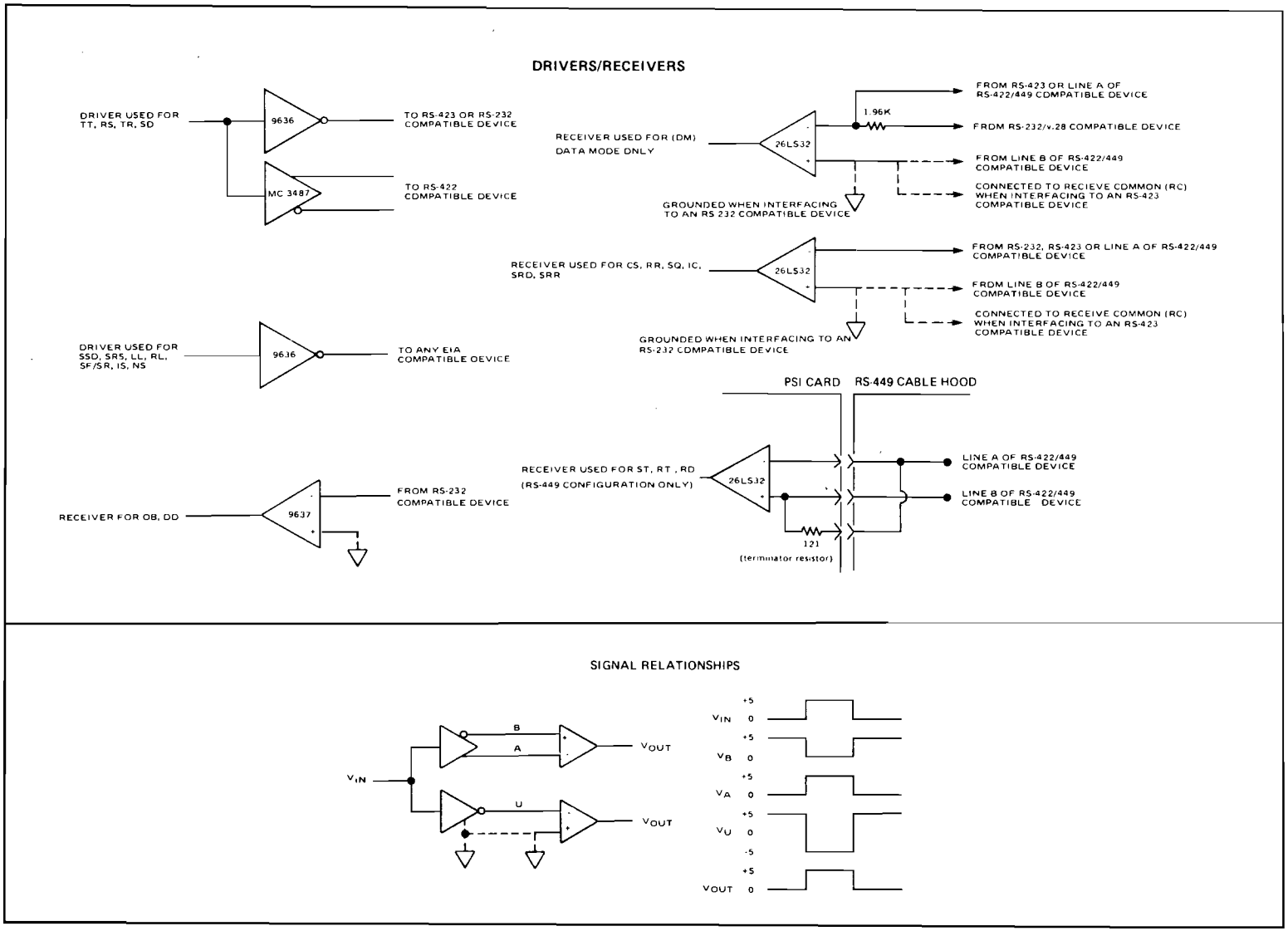
The communication line interface is the point at which the various signals used are received onto the card or driven onto the communications line. The card is capable of supporting the EIA RS-232-C, CCITT V.28, and EIA RS-449, CCITT V.24 serial I/O standards. For the purposes of this discussion, the various interface circuits are referred to by their EIA RS-449 mnemonics. A comparison of EIA RS-232-C, EIA RS-449 and CCITT V.24/V.28 circuits and their respective signal connector pin assignments is given in Chapter 6.

The EIA RS-449 standard consists of a combination of single-ended (EIA RS-423) and differential (EIA RS-422) drivers and receivers. The card uses both single-ended and differential drivers on some lines and only single-ended drivers on others. All of the receivers on the card are differential although some are connected in such a way that they can only receive single-ended signals. The manner in which each signal is driven or received is illustrated in figure 3-2.

A single-ended driver produces one inverted output whereas its differential counterpart drives both the inverted and non-inverted signals. It is important to note that the mark and space conventions of the protocol are preserved in both cases. The advantage of the differential drivers and receivers is that they offer higher noise immunity than single-ended drivers and receivers, thus allowing longer cable lengths and higher data signaling rates.

When a differential receiver is connected to a single-ended driver, the remaining input is either connected to ground (EIA RS-232-C or CCITT V.24/V.28) or to the Receive Common (RC) circuit of the driving device (EIA RS-449). The various driver/receiver combinations are illustrated in figure 3-2. The combination used depends on the requirements of the modem. The receivers on the card can survive an input voltage range of +/- 25 volts and can operate with a maximum common mode input voltage of +/- 7 volts.

Figure 3-2. Driver/Receiver Combinations



Maintenance
Chapter 4

This chapter provides maintenance information for the PSI card. Included are preventive maintenance instructions, and IOP handling procedures.

Preventive Maintenance

There is no preventive maintenance (PM) necessary for the PSI card other than a routine inspection of the equipment which can be performed at the same time that PM is done for the entire system. The card and cables should be checked for broken components, or the presence of foreign objects.

If the card is being used with an HP firmware product, a self-test (included in the firmware ROM/EPROM) is executed each time that power is applied to the card or the card is reset. In this manner the card is checked automatically, and only requires more thorough testing when specific failures occur.

Removal and Installation Procedures for the IOP

WARNING

OBSERVE EYE HAZARD SAFETY PRECAUTIONS WEAR SAFETY GLASSES WHEN REMOVING OR INSTALLING THE RETAINING CLIPS ON THE IOP.

CAUTION

STATIC SENSITIVE DEVICES

USE ANTI-STATIC HANDLING PROCEDURES WHEN REMOVING OR INSTALLING THE IOP.

Removing the IOP

Remove the IOP from its socket as follows:

1. Remove the PSI card from the computer and place it on a flat surface.
2. While pressing down on one of the IOP retaining clips (see figure 4-1) with your thumb, insert the flat blade of a screwdriver or similar instrument between the retaining clip and the side of the socket.
3. Twist the bottom portion of the blade away from the socket to free the retaining clip (A) from the bottom edge of the socket.
4. When the retaining clip (A) is free, lift it up and over the IOP.
5. Remove the second retaining clip by following steps 2 through 4.
6. Carefully tip the card on edge and remove the IOP. Observe the anti-static handling precautions when handling the chip.

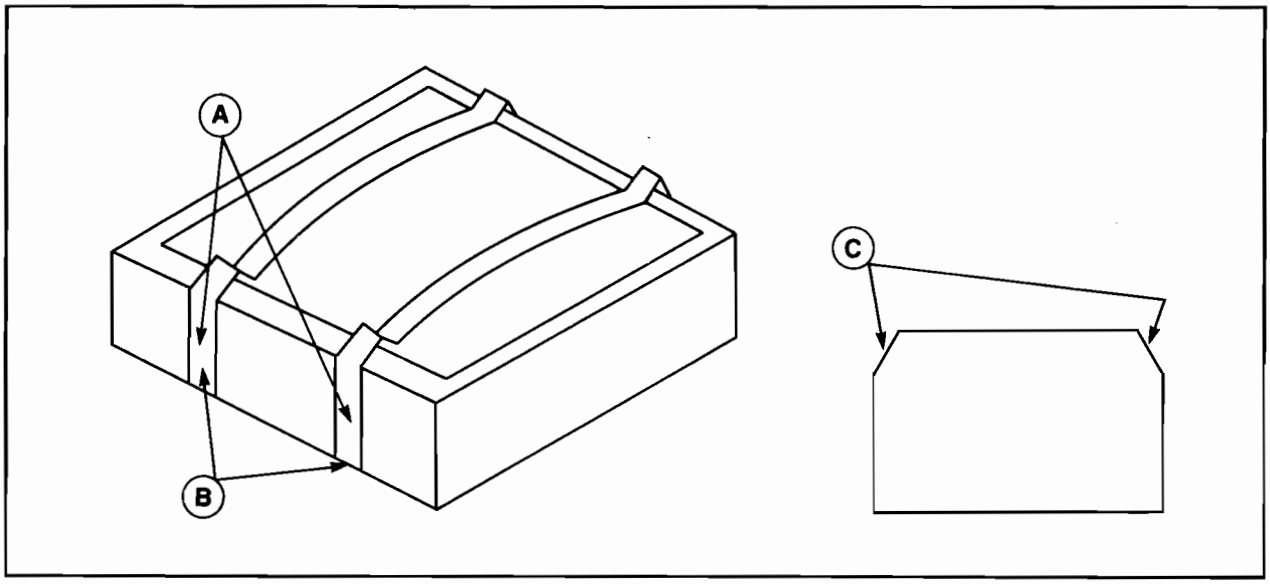


Figure 4-1. IOP Socket with IOP and Retaining Clips in Place

Installing the IOP

Install the IOP in its socket as follows:

1. Observe the anti-static handling precautions when handling the IOP.
2. Place the card on a flat surface with the component side up.
3. Remove both retaining clips from the socket, if they are in place (see figure 4-1).
4. Place the IOP in the socket, locating the two flat corners (C) of the socket facing the two flat corners of the IOP. The trace side of the IOP package must be on the bottom when the IOP is placed in the socket.
5. Place the retaining clips in the two places provided for them in the side of the socket.
6. Press down with your thumb on the retaining clip (A) and press the retaining clip over the edge of the socket until it snaps under the bottom edge of the socket (B).
7. Install the second retaining clip, following steps 3 through 6.

Troubleshooting Techniques

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS

OR CABLES. FAILURE TO DO SO COULD RESULT IN DAMAGE TO THE EQUIPMENT.

CAUTION

STATIC SENSITIVE DEVICES

THE IOP, ROMS/EPROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

Once it has been determined that the PSI card is failing, proceed as follows to localize the failure to the specific component:

1. Check the card configuration as outlined in Chapter 2 of this manual.

2. If the card is being used with an HP firmware product, run the self-test which is included in the firmware ROM/EPROM. The self-test examines Z-80A CPU operation, on-board DMA operation (channels 0 and 1), counter/timer (CTC) performance, RAM and ROM/EPROM memory, and some parts of the driver/receiver circuits and Z-80A SIO. Refer to the firmware manual for information on the self-test, and additional diagnostic tests.

3. If a failure is found using the above described tests, replace the PSI card, firmware ROM/EPROM, or IOP and re-run the test to ensure that the problem has been corrected. For information on repair or replacement of the failing components (other than user-supplied firmware), contact the nearest Hewlett-Packard Sales and Service Office. (Sales and Service offices are listed at the back of this manual.) Each component (card, IOP and clips, or ROM/EPROM) is handled separately by the HP service organization. Return only the failed part under the HP Assembly Exchange or Repair Program (if the card is bad, return it without the ROM/EPROM, configuration jumpers, IOP, or the IOP clips).

4. If desired, further isolation to a defective part (other than the firmware ROM/EPROMs or IOP) may be performed. Such work is at the descretion of and under the responsibility of the customer. Refer to the Servicing Diagram information given in Chapter 6 of this manual and replaceable parts information given in Chapter 5.

Replaceable Parts
Chapter 5

This chapter contains information for ordering replaceable parts for the PSI card. Table 5-1 gives a list of replaceable parts, and table 5-2 contains the names and addresses of the manufacturers indexed by the code numbers used in table 5-1.

Replaceable Parts

Table 5-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 5-2 for a cross reference of the manufacturers.
7. The manufacturer's part number.

Ordering Information

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

Table 5-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	5061-4912	6	1	PCA PROGRAMMABLE SERIAL INTERFACE	28480	5061-4912
C1	0160-0576	5	8	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C2	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C3	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C4	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C5	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C6	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C7	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C8	0180-0197	8	3	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C9	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C10	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C11	0180-0100	3	2	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C12	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C13	0160-4835	7	14	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4807	3	2	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C29	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
CR1	1990-0662	0	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0662
CR2	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR3	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR4	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR6	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
E1	0360-1682	0	2	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
F1	2110-0301	1	1	FUSE .125A 125V .281X.093	28480	2110-0301
F2	2110-0423	8	1	FUSE 1.5A 125V NTD .281X.093	28480	2110-0423
F3	2110-0099	4	1	FUSE 1A 125V .281X.093	28480	2110-0099
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	1810-0280	8	2	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R3	0757-0442	9	7	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R4	0698-3429	2	13	RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R5	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R6	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R7	1810-0276	2	2	NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R8	0757-0199	3	6	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R9	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R10	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R11	0757-0403	2	3	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R12	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R13	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R14	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R15	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R16	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R17	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R18	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R20	0757-0403	2		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R21	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R21	1810-0517	4	3	NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R25	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R26	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R29	0698-4590	0	1	RESISTOR 422 1% .250W F TC=0+-100	24546	C5-1/8-T0-422R-F

See introduction to this section for ordering information
*Indicates factory selected

Table 5-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R30	0757-0403	2		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R32	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R33	1810-0517	4		NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R35	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R36	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R37	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R38	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R39	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R40	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
R41	0698-0082	7	3	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R42	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R43	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R44	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R45	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R46	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R47	1810-0517	4		NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R48	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R50	0757-1094	9	2	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R51	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R52	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R53	0698-0083	8	1	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
U1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U2	1820-2117	5	6	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U3	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U4	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U5	1820-2198	2	1	IC RCVR TTL S LINE RCVR DUAL	07263	9637ATC
U6	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U7	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U8	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U10	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
U12	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U14	1820-2301	9	1	IC-Z80A CTC	28480	1820-2301
U15	3101-1983	9	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-1983
U18	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U20	1820-2300	8	1	IC-Z80A SIO/2	28480	1820-2300
U22	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U25	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U26	1816-0916	9	1	IC TTL S 256-BIT PROM 50-NS 3-S	18324	N82S123F
U27	1820-2024	3	5	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U32	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
U35	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U36	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U38	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U40	1820-2145	9	1	IC DRVR TTL LINE DRVR QUAD	04713	MC3487P
U41	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U45	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U46	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U50	1820-2594	2	4	IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U51	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U52	1818-1396	5	8	IC NMOS 16384 (16K) DYN RAM 200-NS	50545	UP416C-2(SELECTED)
U54	1820-2299	4	2	IC-Z80A DMA	28480	1820-2299
U55	1820-1677	0	2	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U60	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U61	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U62	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 200-NS	50545	UP416C-2(SELECTED)
U65	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U66	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U70	1820-1244	7	2	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U71	1820-1729	3	2	IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U72	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 200-NS	50545	UP416C-2(SELECTED)
U74	1820-2299	4		IC-Z80A DMA	28480	1820-2299
U75	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U76	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U80	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U81	1820-1729	3		IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U82	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 200-NS	50545	UP416C-2(SELECTED)
U83	1816-1371	2	1	IC TTL S 2048 (2K) PROM 70-NS	01295	TBP18S22J(PER HP DWG)
U84	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U85	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U90	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U91	1820-1298	1	1	IC MUXR/DATA-SEL TTL LS 8-TO-1 LINE	01295	SN74LS251N
U92	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 200-NS	S0545	UP416C-2(SELECTED)
U93	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U94	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U95	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U96	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U101	1820-1244	7		IC MUXR/DATA-SEL TTL LS 4 TO-1-LINE DUAL	01295	SN74LS153N
U102	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 200-NS	S0545	UP416C-2(SELECTED)
U104	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U105	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U106	1820-0601	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U107	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2 INP	01295	SN74LS00N
U112	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 200-NS	S0545	UP416C-2(SELECTED)
U114	1820-0693	8		IC FF TTL S D TYPE POS-EDGE-TRIG	01295	SN74S74N
U115	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2 INP	01295	SN74S02N
U118	1820-1451	8		IC GATE TTL S NAND QUAD 2 INP	01295	SN74S38N
U121	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS EDGE-TRIG	01295	SN74LS161AN
U122	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 200-NS	S0545	UP416C-2(SELECTED)
U123	1826-0220	9	1	IC V RGLTR TO-39	27014	LM320H-05
	1200-0185	9	1	INSULATOR-XSTR NYLON	28480	1200-0185
U124	1820-2096	9	1	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
	1251-1556	7	6	CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
	1258-0124	7	2	PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-4756
	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
	1258-0124	7		PIN PROGRAMING JUMPER .30 CONTACT	91506	8136-4756
W6	8159-0005	0	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
XW1	1200-0483	0	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0483
	0403-0289	3	2	EXTR-PC BD RFD POLYC .063-BD-THKNS	28480	0403-0289
	1200-0567	1	3	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
	1200-0607	0	8	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0654	7	4	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
	1200-0848	1	1	SOCKET-SBSTR 64-CONT CERAMIC DIP-SLDR	28480	1200-0848
	1480-0116	8	2	PIN GRV .062-IN-DIA .25-IN-LG STL	28480	1180-0116

See introduction to this section for ordering information
*Indicates factory selected value

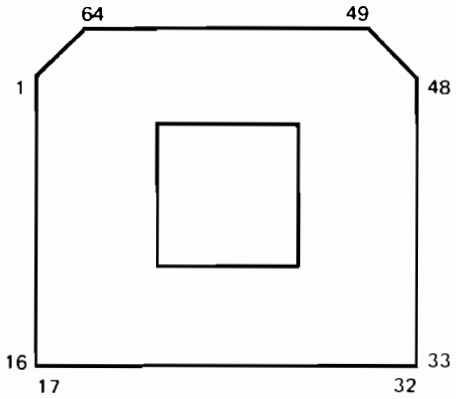
Table 5-2. Manufacturers Code List

MFR NO.	MANUFACTURER'S NAME	ADDRESS		ZIP CODE
S0545	NIPPON ELECTRIC CO	TOKYO	JP	
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR SEMICOND DIV	DALLAS	TX	75222
03888	K D I PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PROD	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORP HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
91506	AUGAT INC	ATTLEBORO	MA	02703

Servicing Diagrams
Chapter 6

This chapter contains servicing diagrams for the PSI Card.

U67
1AF5-6001



1AF5-6001 I/O PROCESSOR (IOP) CHIP OUTLINE (COMPONENT SIDE)

PIN DEFINITIONS							
PIN	**SIGNAL**	**PIN**	**SIGNAL**	**PIN**	**SIGNAL**	**PIN**	**SIGNAL**
1	DMACYC-	17	GND	33	BRNI+	49	VCC
2	LDMAR+	18	VDD	34	CRS +	50	GND
3	SCEN-	19	CW1 -	35	IEN -	51	VDD
4	REMOTE-	20	BCW2 +	36	DIAG -	52	CB7 +
5	INTCYC +	21	BCW1 +	37	DVCMD -	53	CB8 +
6	DMAEN -	22	BCW0 +	38	PLSLV+	54	CB9 +
7	LOBYT -	23	BVALID+	39	PON +	55	CB10 +
8	SACK -	24	BIOGO+	40	SLACK +	56	CB11 +
9	NC	25	ICHID-	41	SLRQ+	57	CB12 +
10	SCLK +	26	BIAK+	42	CB0 +	58	CB13 +
11	LSBYT -	27	CFF-	43	CB1 +	59	CB14 +
12	BPE+	28	PULIOR-	44	CB2 +	60	CB15 +
13	BMP-	29	IOEN -	45	CB3 +	61	MEMGO+
14	CHSRQ-	30	IOCLK +	46	CB4 +	62	MRQ +
15	IRQ -	31	PRDIS -	47	CB5 +	63	NC
16	VCC	32	GND	48	CB6 +	64	GND

Figure 6-1. IOP Base Diagram

Servicing Diagrams

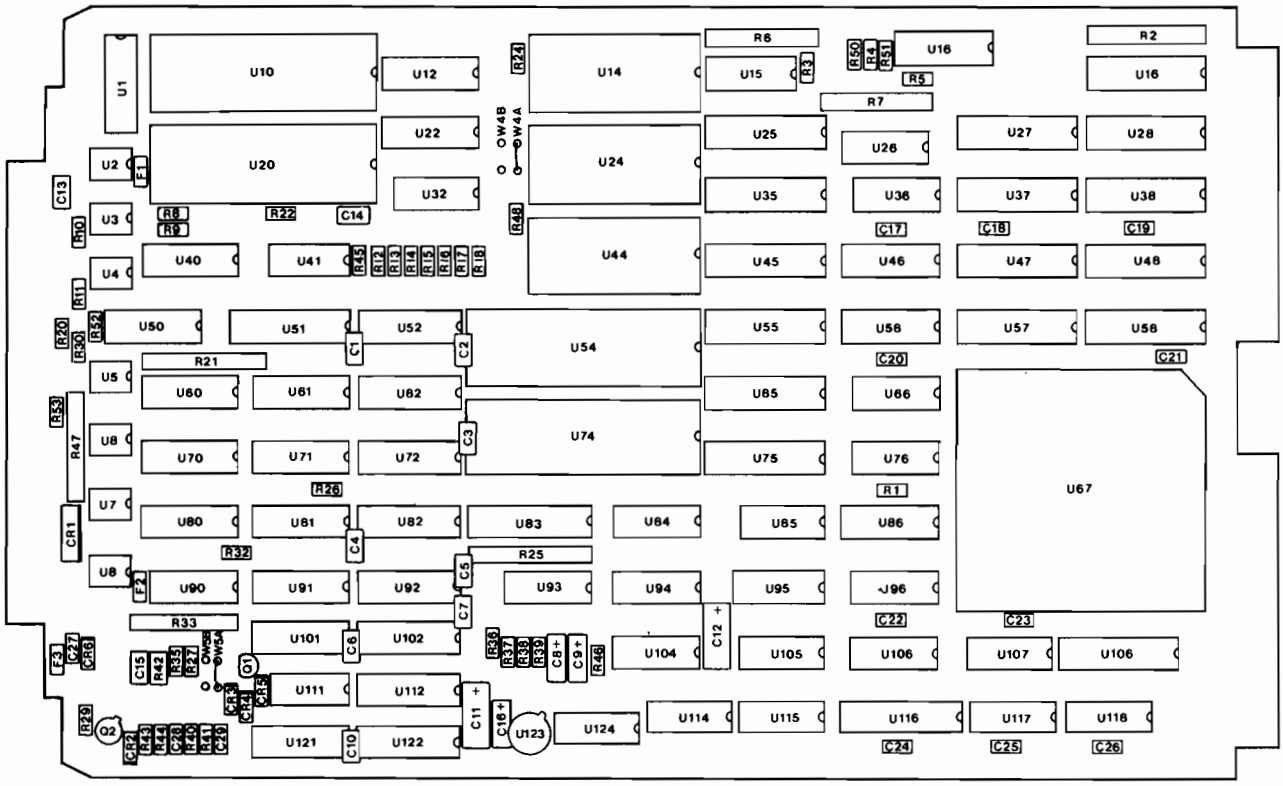


Figure 6-2. PSI Card Parts Location Diagram

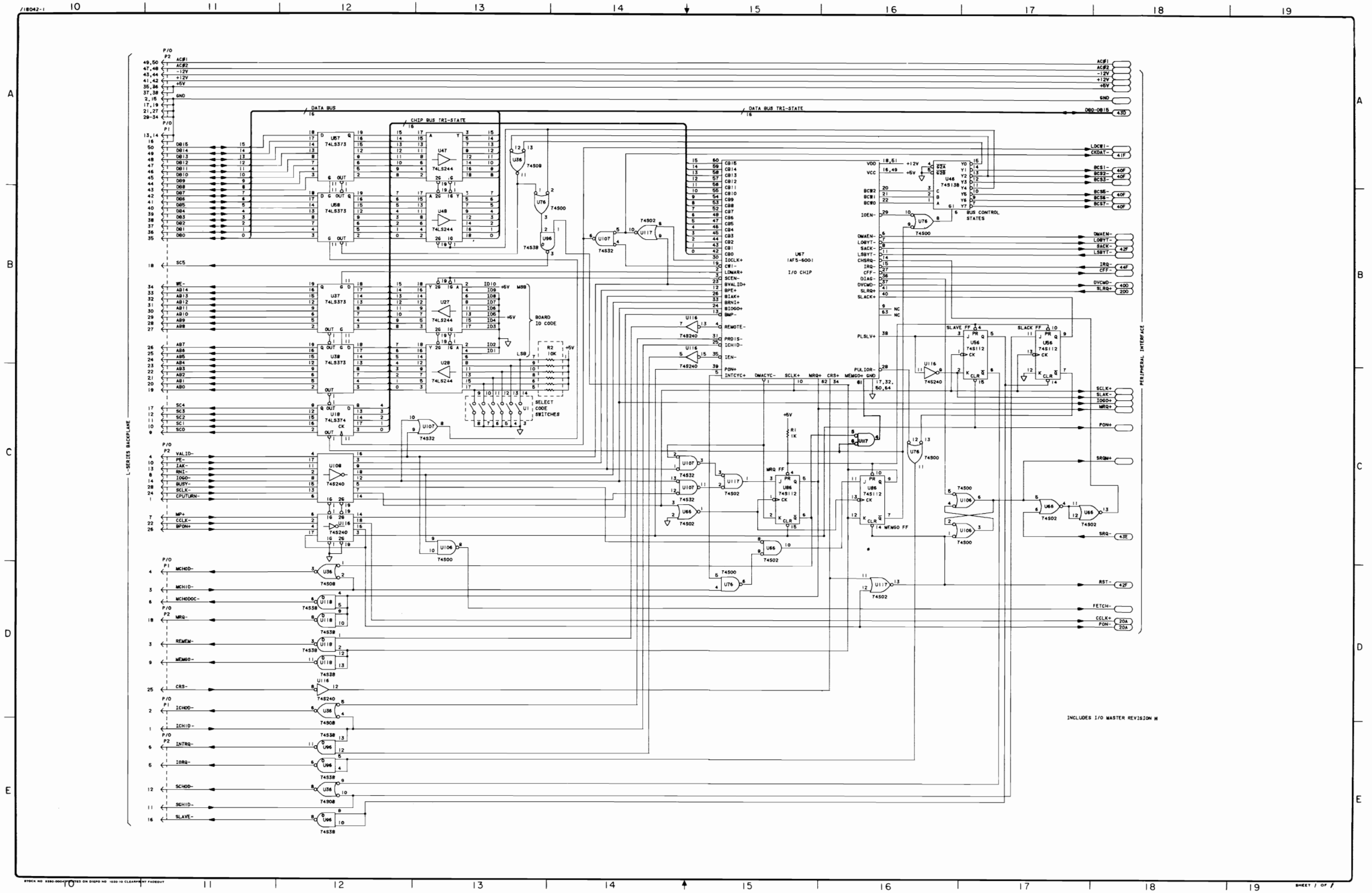


Figure 6-3. PSI Card Schematic Logic Diagram (Sheet 1 of 4)

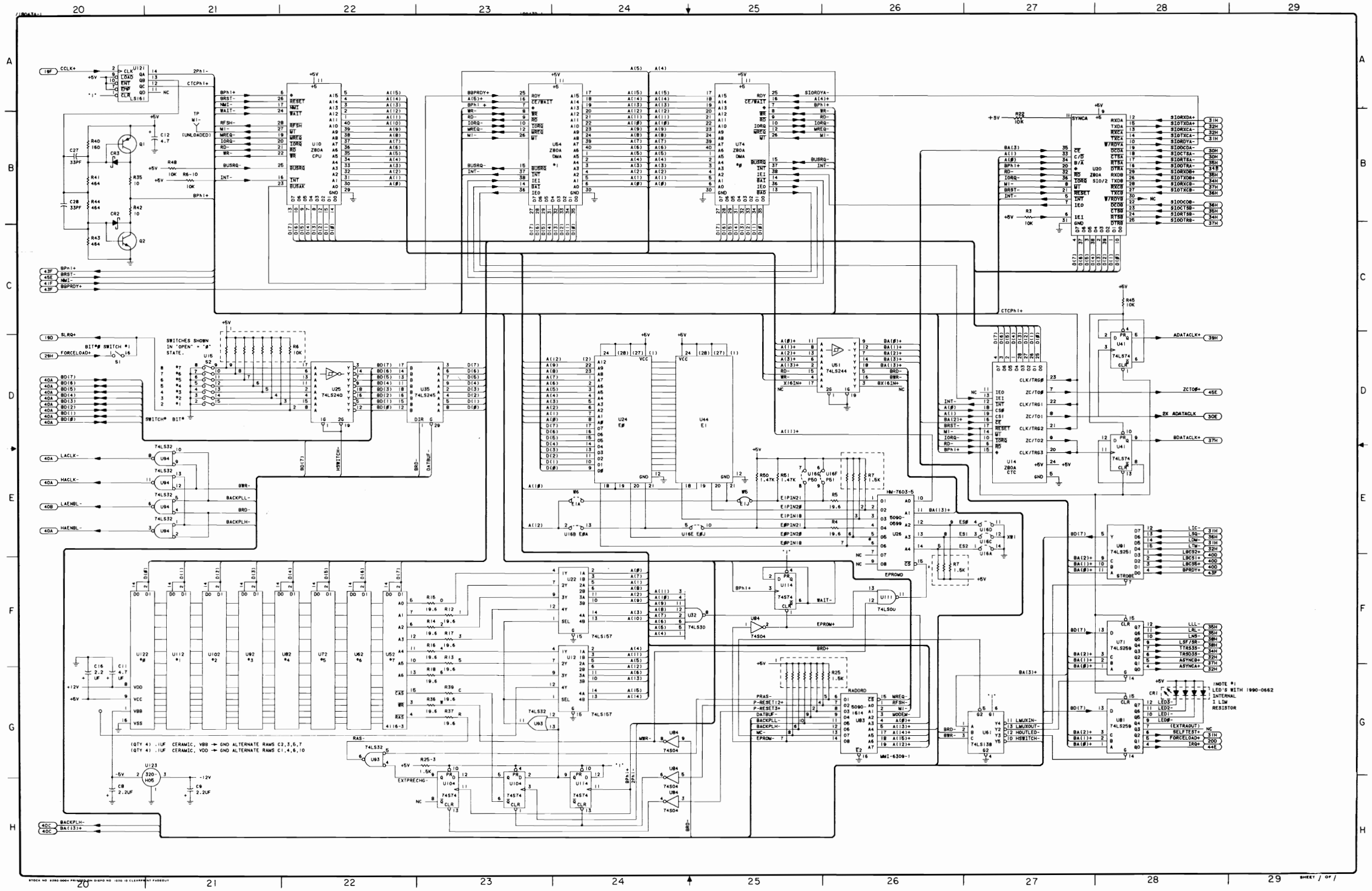


Figure 6-3. PSI Card Schematic Logic Diagram (Sheet 2 of 4)

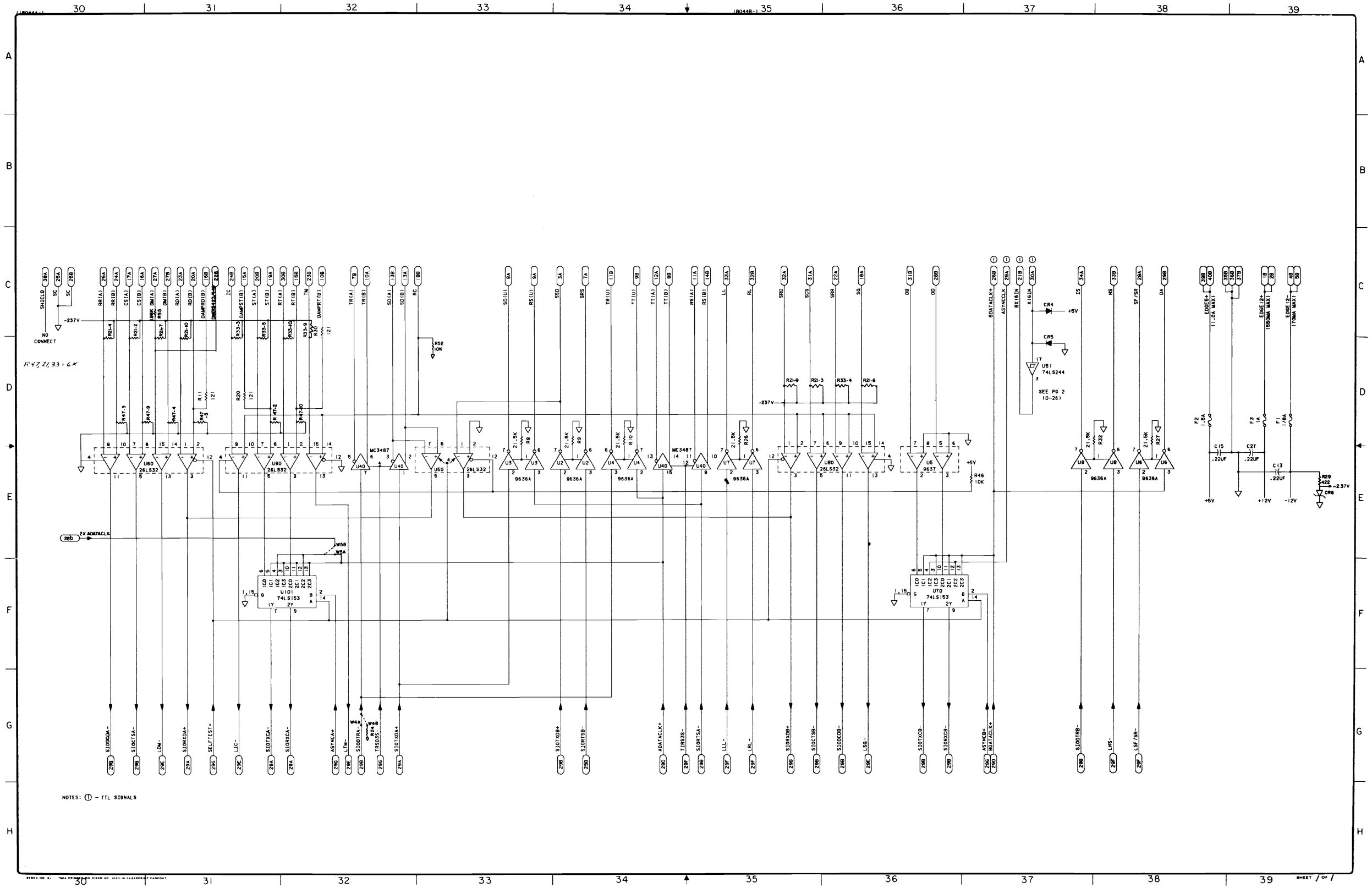


Figure 6-3. PSI Card Schematic Logic Diagram (Sheet 3 of 4)

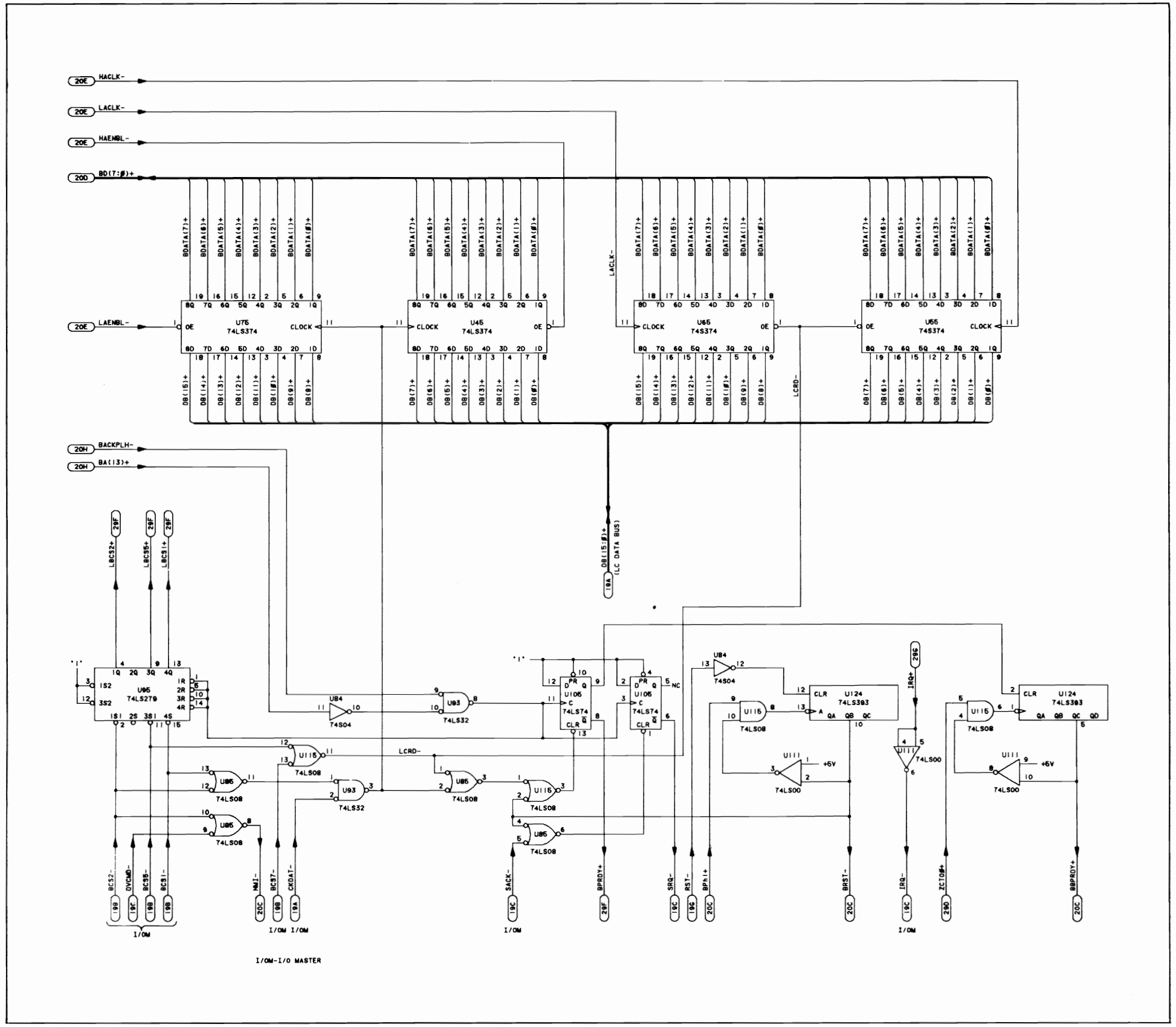


Figure 6-3. PSI Card Schematic Logic