PAPER TAPE NO. 12979-16001

I/O CHANNEL DIAGNOSTIC

for

2100 SERIES COMPUTER AND I/O EXTENDER

reference manual

HEWLETT hp PACKARD

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Section I

INTRODUCTION

1-1. GENERAL

This diagnostic program checks the operation of the I/O channels within the computer mainframe or within the I/O extender. Each I/O channel is checked for initialization, control, priority, I/O channel address, interrupt, and I/O bus signals.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. HP 2100 series computer with a minimum 4K memory.
b. HP 12566 Microcircuit Interface Card
c. HP 2116-6110 Priority-jumper Card
d. HP 5060-8339 Connector Kit (Test Hood)
e. A paper tape reading device (used only for loading)
f. A console teleprinter device for message reporting (recommended but not required).

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator, Product No. 24296 used for equipment configuration and as a console device driver. The product includes the following part no.:

Binary object tape	Part No. 24296-60001
Manual	Part No. 02100-90157

b. HP I/O Channel Diagnostic Binary Object Tape:

Part No. 12979-16001

The Diagnostic serial numbers (DSN) is contained in memory location 126_8 of the program. The DSN is 143020_8.

Section II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

This diagnostic program contains a control and initialization section and three tests. The initialization and control section prepares the diagnostic by accepting the select code and option required by the tests.

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device for operator information then executes the tests according to the options selected on the Switch Register by the operator. The control section mainly checks Switch Register bits 15, 13 and 12.

The program also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 10 is clear), the count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed. (Refer to Paragraph 3-3.)

2-3. SELECTION OF TESTS BY OPERATOR

The operator has the capability to select his own test or sequence of tests with the help of bit 9 in the Switch Register. Paragraph 3-3 outlines the test selection.

2-4. MESSAGE REPORTING

There are two types of messages: error and information. Error messages are used to inform the operator when the interface fails to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some operation related to the function of the unit. In this case, an associated halt will occur to allow the operator time to perform the function. The operator must then press RUN. If a console device is used, the printed message will be preceded by the letter E (error) or the letter H (information) and a number (in octal). The number is also related to the halt code when a console device is not available. Examples of error and information messages are as follows:

Example - Error with halt
Message: E030 Data is XXXXXX should be YYYYYY
Halt Code: 102030_8

Example - Information with halt
Message: H024 PRESS PRESET (EXT & INT), RUN
Halt Code: 102024_8

Example - Information only
Message: H025 BI-O COMP
Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors. The A-Register contains the actual status and the B-Register contains the expected status when an error halt takes place.

Information messages are suppressed by setting Switch Register bit 10. Operator intervention is suppressed by setting Switch Register bit 8 (i.e., Preset Test in BI-O). When Switch Register bit 12 is set the tests that are selected will be repeated. All operator intervention will be suppressed.

2-5. PRIORITY STRING

To check the priority circuit from a lower select code to the next highest select code, a priority jumper card must follow the 12566 interface card that is testing the I/O channel. The priority jumper card must have its jumper installed between PRL and 4.5 Volts. If the I/O channel under test does not receive priority (i.e., PRH (priority high) from the next lower select code) an error E014 NO INT will occur. To test for denying of priority to the I/O channel under test, remove the priority jumper card and run the Basic I/O test and the above mentioned error should occur. The Basic I/O test should first be run in I/O channel 10_8 to insure that the priority system within the CPU is working properly.

Section III

OPERATING PROCEDURE

3-1 OPERATING PROCEDURES

A flowchart of the operating procedures is provided on the following page.

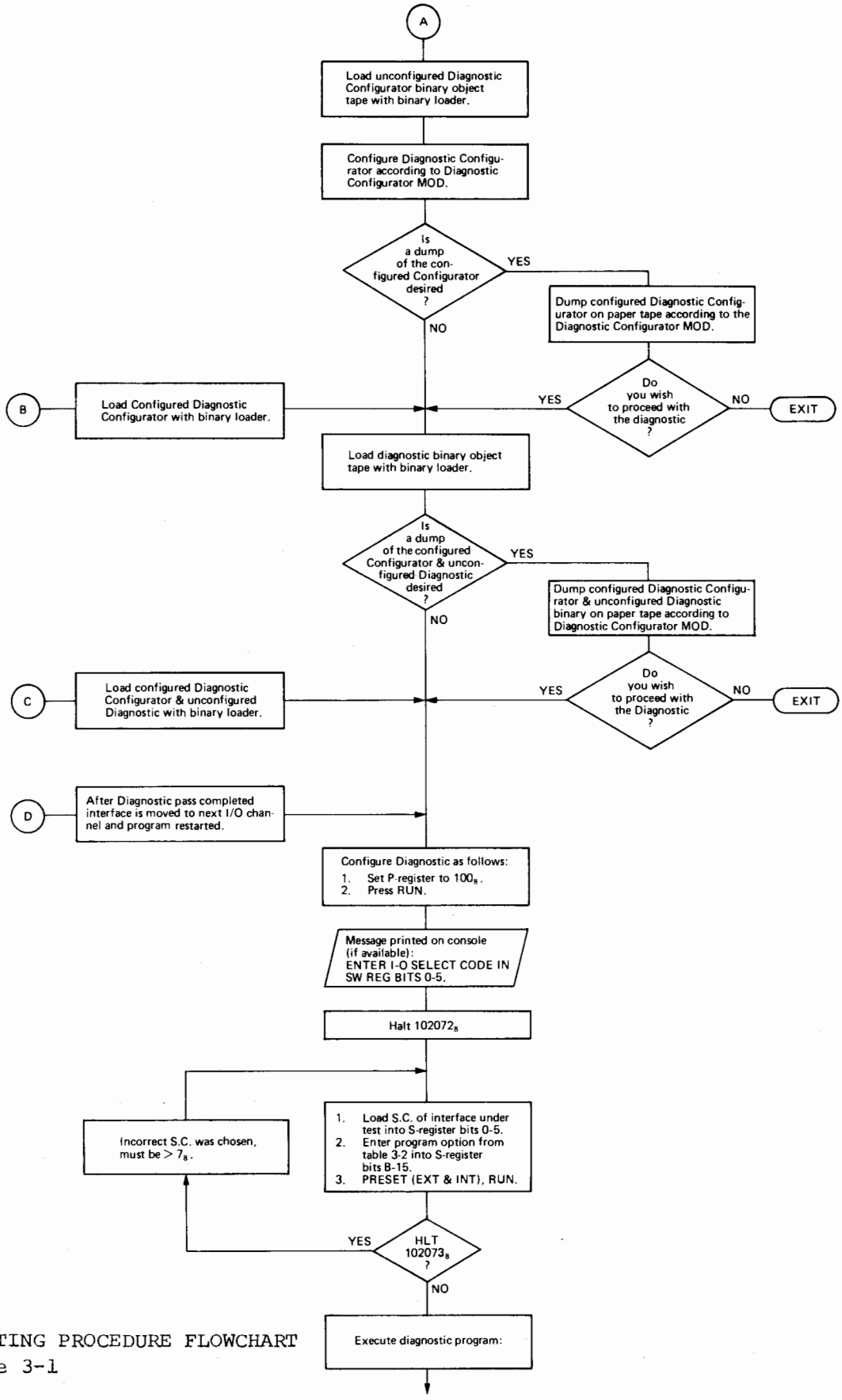
If an unconfigured Diagnostic Configurator is available start at entry point A.

If a configured Diagnostic Configurator is available start at entry point B.

If a combined configured Diagnostic Configurator and an unconfigured Diagnostic is available start at entry point C.

After the diagnostic has completed a pass on the I/O channel, the 12566 microcircuit card is moved to the next I/O channel. The diagnostic program is restarted at entry point D in the Operating Procedure Flowchart.

CAUTION be sure to turn off the power to the CPU or I/O extender before removing and/or installing the microcircuit card.



OPERATING PROCEDURE FLOWCHART
Figure 3-1

3-2. RUNNING THE DIAGNOSTIC

At the completion of each pass of the diagnostic, the pass count is output to the console for operator information. If Switch Register bit 12 was not selected, the computer will halt with 102077_8 in the Memory Data Register (T-Register). At this point, the A-Register contains the pass count. To run another pass, the operator need only to press RUN. Bit 12, if set, is used to loop on the diagnostic; bit 13 is used to loop on a given test that is running at the time; and bit 15, if set, will halt the computer at the completion of a test. After the diagnostic has completed a pass, the operator turns off the power to the computer (and/or I/O extender) removes the microcircuit card (and priority jumper card) and installs the card(s) in the next I/O channel. Then turns the power on and restarts the program by returning to entry point D in the operating procedures (figure 3-1).

If a trap cell halt occurs (106077_8), the user must determine the cause of the interrupt or transfer of control to the location in the M-Register. The program may need to be reloaded to continue.

When a halt occurs and/or a message is printed on the console device, the operator must refer to Table 4-2 for the meaning of the halt.

3-3. TEST SELECTION BY OPERATOR

The control portion of the program allows the operator the option to select a test or sequence of tests to be run. The operator sets Switch Register bit 9 to indicate that he wants to make a selection and presses RUN. The computer will come to a halt 102075_8 to indicate it is ready for the selection. If the program is running, the test in progress will be completed and then the program will halt. Now the operator loads the A-register with the tests desired. Bit 0 of the A-Register represents Test 00, bit 1 represents Test 01, and so on up to bit 2 which represents Test 2. The operator must then clear Switch Register bit 9 and press RUN. The operator-selected test(s) will then be run. If the operator clears all bits, then all tests defined in Table 3-1 will be executed.

Table 3-1. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	Test 00 BI-O Test
1	Test 01 I-O Data Test
2	Test 02 DMA/DCPC Test
3-15	Reserved
B-Register	Reserved

3-4. RESTARTING

The program may be restarted by setting the P-register to 2000_8, load S-register with desired diagnostic option per Table 3-2, press PRESET (EXT & INT), RUN.

Table 3-2. Switch Register Options

BIT	MEANING IF SET
0	I/O Select Code
1	
2	
3	
4	
5	
6	Reserved
7	Reserved
8	Suppress tests requiring operator intervention
9	Abort current diagnostic execution and halt (102075); user may specify a new group of tests in the A-register (see Table 3-1) clear bit 9 and then press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or teletype is not present. Also, those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-Register will contain the test number in octal.

Section IV

DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

Refer to Table 4-2 for additional details on the content of each test.

4-2. BASIC I/O TEST 0 E000-E026

Subtest 1 - Checks the ability to clear, set, and test the interrupt system. The following instruction combinations are tested:

```
CLF 0 - SFC 0
CLF 0 - SFS 0
STF 0 - STC 0
STF 0 - SFS 0
```

Errors in the above sequences produce error messages E000-E003 as shown in Table 4-2.

Subtest 2 - Checks the ability to clear, set, and test the interface flag. The following instruction combinations are tested:

```
CLF CH - SFC CH
CLF CH - SFS CH
STF CH - SFC CH
STF CH - SFS CH
```

Errors in the above sequences produce error messages E005-E010 as shown in Table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the Flag and Control set on the interface and the interrupt system off. The sequence of instructions is shown below:

```
STF 0
STF CH
STC CH
CLF 0
```

The CLF 0 instruction should inhibit an interrupt from occurring. Error message E004 occurs if CLF 0 fails.

Subtest 4 - Checks that the Flag of the interface under test is not set when all other select code Flags are set. Error message E011 occurs if a Flag is set incorrectly.

Subtest 5 - Checks the ability of the interface to interrupt. With the Flag and Control set and the interrupt system on, there should be an interrupt on channel CH; if not, error message E014 occurs. Checks that the interrupt occurred where expected. The interrupt should not occur before a string of priority-affecting instructions are executed. The following instructions are used to check the hold off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages E012 and E015 will occur if the hold off fails. Checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if an interrupt does occur. Checks that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the CH Control and Flag set, there is no interrupt following a CLC CH instruction. The following sequence of instruction are used:

```
STC CH
STF CH
STF 0
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message E016 will occur.

Subtest 7 - Checks that the CLC 0 instruction inhibits interrupts when the CH Control and Flag are set. The following sequence of instructions is used.

```
CLF CH
STC CH
STF CH
STF 0
CLC 0
```

If the CLC 0 fails to inhibit an interrupt, error message E017 will occur.

Subtest 8 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) switches on the operator panel performs the following actions:

1. Sets interface Flag (EXTERNAL).
2. Clears Control (EXTERNAL).
3. Turns off the interrupt system (INTERNAL).
4. Clears the I/O data lines (EXTERNAL).
5. Clears the data register in the interface (interval).

4-3. I/O DATA TEST

The I/O data test checks the IOBO and IOBI data lines (0-15) on the I/O channel under test. Data patterns are sent to the IOBI lines from the IOBO lines via the 12566 Microcircuit Interface Card and test hood. When an error is detected a message follows:

"E030 DATA IS XXXXXX SHOULD BE YYYYYY"

The A-Register contains the actual data and the B-Register contains the expected data.

4-4. DMA/DCPC TEST

The direct memory access/dual-channel port controller test verifies that the I/O channel under test can be initialized for a DCPC operation and that a data transfer to the microcircuit interface and back to the CPU is unaltered. It is beyond the scope of this test to determine actual hardware failure within the logic of the DCPC.

To test the DCPC logic, the operator must run the 21XX Series Direct Memory Access Diagnostic:

Product No. 24322
Binary Tape No. 24322-16001
Manual 02100-90217

Table 4-1. Halt Code Summary

HALT	MEANING
TESTS 0_8 to 2_8 102000-102035	Error (E) and information (H) messages $00\text{-}35_8$.
CONTROL	
102073	Select code input error.
102075	User selection request.
102076	End of test (A = test number).
102077	End of diagnostic run.
106077	Trap cell halts in location $2\text{-}77_8$.
NOTE: See Table 4-2 for complete explanation of individual halts.	

Table 4-2. Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
102073	Configuration	None	I/O select code entered at configuration is invalid. Must be greater than 7_8. Reenter a valid select code and press RUN.
102072	Configuration	H072 ENTER I-O SELECT CODE IN SW-REG	Operator enters the I/O select code in to Switch Register bits 0-5 and the Switch Register Options from Table 3-2 into bits 8-15 and presses RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter in A-register the desired group of tests to be executed, clear bit 9 in Switch Register and press RUN. (See Table 3-1 and 3-2).
102076	Test Control	None	End-of-test halt resulting from Switch Register bit 15 being set (A-Register has the test number). To continue, press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. Register options may be changed (A-register has the pass count). To continue press RUN.
106077	Test Control	None	Halt stored in location $2\text{-}77_8$ to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-Register contains the I/O slot which interrupted. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.
None	Test Control	I-O CHANNEL DIAGNOSTIC	Introductory message.

Table 4-2. Error Information Messages and Halt Codes (continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
None	Test Control	TEST XX	Information message before error message (XX = test number). Message occurs only once within a test but is suppressed for any subsequent messages within the same test.
102000	Test 0	E000 CLF 0-SFC 0 ERROR	CLF/SFC 0 combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102001	Test 0	E001 CLF 0-SFS 0 ERROR	CLF/SFS 0 combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.
102002	Test 0	E002 STF 0-SFC 0 ERROR	STF/SFC 0 combination failed. STF did not set Flag or SFC caused skip with Flag set.
102003	Test 0	E003 STF 0-SFS 0 ERROR	STF/SFS 0 combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102004	Test 0	E004 CLF 0 DID NOT INHIBIT INT	With card Flag and Control set, CLF 0 did not turn off interrupt system.
102005	Test 0	E005 CLF CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear flag or SFC caused no skip with Flag clear.
102006	Test 0	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.
102007	Test 0	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set Flag or SFC caused skip with Flag set.
102010	Test 0	E010 STF CH-SFS CH ERROR	STF/SFS CH combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102011	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. A-register contains XX_8 where XX = select code that caused that card Flag to set.

Table 4-2. Error Information Messages and Halt Codes (continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURRED	Card interrupted a second time after initial interrupt was processed.
102014	Test 0	E014 NO INT	No interrupt occurred with card Flag and Control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0	E016 CLC CH ERROR	CLC CH did not clear card Control with the interrupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear Control with the interrupt system on.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card Flag.
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear Control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I-O LINES	PRESET (EXT) did not clear I/O data lines.
102024	Test 0	H024 PRESS PRESET (EXT & INT), RUN	Press PRESET (External, Internal) and RUN.
102025	Test 0	H025 BI-O COMP	Basic I/O Test complete.
102026	Test 0	E026 INT EXECUTION ERROR	Installations being executed prior to and just after interrupt did not execute correctly.

Table 4-2. Error Information Message and Halt Codes (continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102027	Test 0	E027 PRESET(ENT) DID NOT CLEAR DATA REG	PRESET(INT) did not clear the data register in the microcircuit interface card.
102030	Test 1	E030 DATA is XXXXXX SHOULD BE YYYYYY	The data received is XXXXXX and should be YYYYYY. A-Register contains XXXXXX B-Register contains YYYYYY.
102031	Test 2	H031 DMA NOT CONFIGURED	DMA was not specified during the configuration of the Diagnostic Configurators.
102032	Test 2	E032 DMA TIME OUT ON OUTPUT	A DMA output operation failed to complete within a specified time.
102033	Test 2	E033 I-O FLAG NOT SET AFTER DMA OUTPUT	The I/O flag was not set after a DMA output operation was completed.
102034	Test 2	E034 DMA TIME OUT ON INPUT	The I/O flag was not set after a DMA input operation was completed.
102035	Test 2	E035 I-O FLAG NOT SET AFTER DMA INPUT	The I/O flow was not set after a DMA input operation was completed.
102036	Test 2	E036 I-O DATA DID NOT COMPARE AFTER DMA TRANSFER	The data received during a DMA input operation did not compare with the data sent during the DMA output operation.