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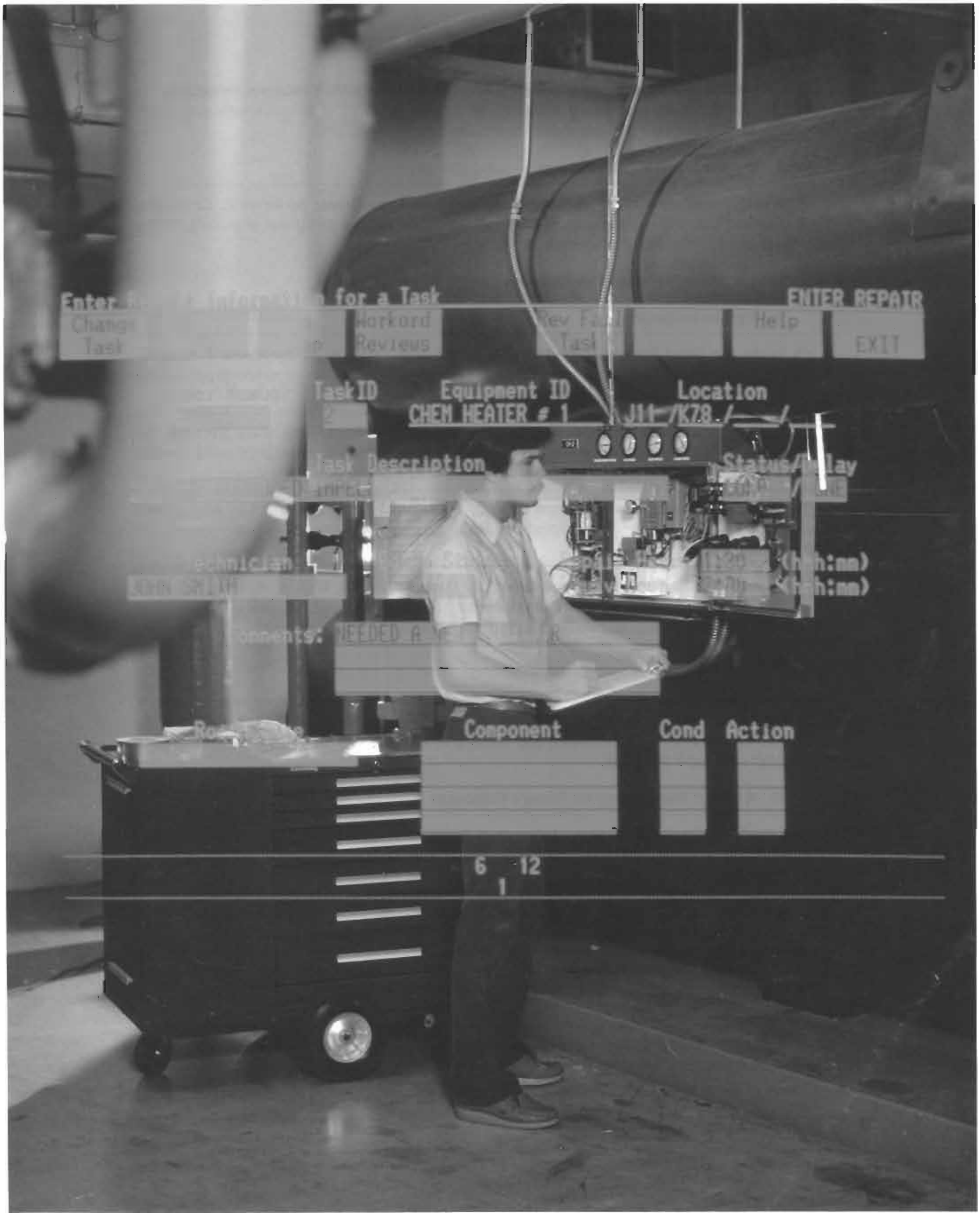

Development of a High-Performance, Half-Inch Tape Drive

The design of a low-cost, high-density tape drive for backup of large amounts of on-line computer system memory requires a sophisticated combination of technologies and careful project planning. This new drive's greatly improved reliability reduces maintenance costs and downtime.

by Hoyle L. Curtis and Richard T. Turley

SATISFYING EXISTING AND FUTURE customers with products that are price and performance competitive remains a constant goal in the computer equipment industry. Adding to the challenge is the desire to maintain compatibility with earlier generations of devices while making the continuing performance improvements and cost reductions that customers have come to expect from electronic product vendors. This is particularly apparent in the technology of tape drives used as computer peripherals.

Because of its versatility, a half-inch tape drive is often selected to provide backup of computer system memory, allowing recovery from system failures or other instances of data loss. It is historically associated with the computer industry to such an extent that often just the picture of a reel-to-reel tape drive is used to convey the image of a mainframe computer.

This identity is well-founded because of the different roles that half-inch tape has played in the growth of the computer industry. It was first used in 1952 by IBM in their Model 726 tape drive, which had a storage density of 100 bits per inch (bpi). Improvements have come on a regular basis with storage densities of 1600 characters per inch introduced in 1965, and 6250 characters per inch in 1973. Half-inch tape can be used for on-line memory, off-line storage, backup memory, data interchange, transaction logging, and software distribution. Although its use as on-line memory has all but disappeared because of its slower access speed, the other uses continue to flourish. Because of its early use in most computer systems, it is a universally accepted medium for data interchange between computers from different manufacturers. This has been assured by international standards such as those administered by the American National Standards Institute (ANSI).[1,2]

Hewlett-Packard's newest half-inch tape drive, the HP 7978A (Fig. 1), is an industry standard nine-track, reel-to-reel drive that provides improved functionality and reliability at a significantly lower cost. This tape drive is designed to provide HP computer systems with a reliable backup device for large amounts of on-line disc memory by placing up to 140 megabytes on a standard 10½-inch reel. It also provides for the interchange of data with other HP or non-HP computer systems by supporting both 6250 GCR (group coded recording) and 1600 PE (phase encoding) ANSI formats.

Compared with the earlier HP 7976A Magnetic Tape Subsystem which it replaces, the HP 7978A makes significant contributions in several areas. The HP 7978A is half the cost and five times more reliable. Additional improvements include better data reliability (full parity checking on internal data paths), half the size, less than half the power consumption at under 400 watts, lower acoustic noise (less than 60 dBA), and improved serviceability (30 minutes

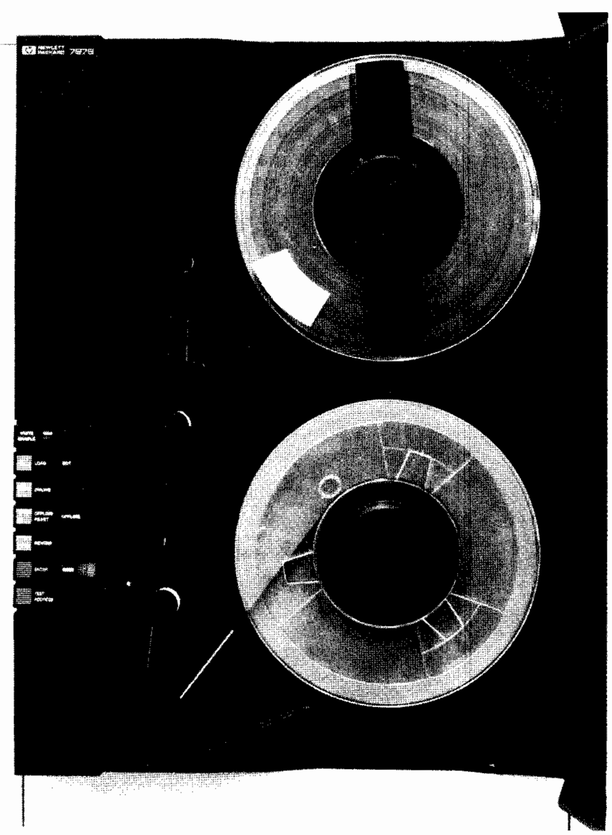

Fig 1. *Designed to back up computer systems with large amounts of on-line disc storage, HP's newest half-inch tape drive, the HP 7978A, features high performance and increased reliability for a low cost. This streaming tape drive uses both 6250 GCR and 1600 PE storage formats.*

MTTR). These attributes were gained by combining a market-driven product definition, a good technical implementation, and proper project execution. While these three areas may seem obvious, their correct sequencing and interaction are the heart of both the product and the project.

Product Definition

When HP's Greeley Division surveyed the market for contributions that could be made in half-inch tape drives, they found cost of ownership (purchase price plus maintenance costs) to be the highest on the list of customer concerns. Increased reliability was also found to be an area where HP could make a contribution. The study noted that the complexity of existing tape drives was primarily responsible for their high cost and low reliability. This complexity was required to provide the performance needed to achieve a high data rate. However, raw performance means little if a system cannot use it, so extensive modeling of entire computer systems was conducted.

Prices in the tape drive industry had not followed the cost reduction trends experienced by the rest of the computer industry, making the cost of a tape drive an increasingly larger percentage of the system price. An astounding increase in magnetic disc storage on systems meant that backup time had become an increasing burden on system uptime. This trend created a demand for higher capacity and faster transfer rates, which could only be satisfied by a drive capable of using the 6250 GCR format. Because of the large tape libraries at most computer centers and the need to interchange data, it was apparent that the older 1600 PE format should also be usable in a new tape drive.

The task then became the definition of a tape drive that could satisfy all of the customer needs and that would fit into the HP computer family. While this may seem straightforward, the integration of a new peripheral into an extensive family of mainframes and a large diverse software base proved to be no mean feat.

A number of studies were done to determine whether current standards (either industry or HP) and/or leveraged designs could be used in the HP 7978A definition, since this would reduce engineering effort and make development easier in general. The most obvious of these were the previously mentioned ANSI data format standards for 6250 GCR and 1600 PE.[1,2] Others included the HP-IB (IEEE 488) interface and a command set leveraged from earlier tape and disc drives. A powerful microprocessor (the 68000) was chosen because development tools were already available for it in-house, left over from the design of the HP 9000 Model 226 Computer.

The choice of 6250 GCR as the recording format had significant implications. This is currently the most advanced and complex recording technology used for tape. It requires real-time encoding of data into a nine-track format with three bytes being added to every seven bytes of data. Reading GCR data requires real-time decoding and error correction of up to two bits per byte. A density of 9042 magnetic flux reversals per inch must be placed on the tape. To optimize performance, a tape speed of 75 inches per second (ips) is used for both reading and writing. A rewind speed of 250 ips is used. The resulting drive provides a data rate of about 470,000 bytes per second.

Technical Implementation

An architecture had to be defined that would allow HP's technology, the market definition, and areas of leverage to be combined into a viable product. See Fig. 2 for a high-level diagram of the HP 7978A architecture. This architecture permitted the establishment of a detailed, low-level product definition based on modularity with minimum connectivity. Each module was then divided into submodules that reached a level of complexity that could be assigned to individuals for implementation. A further benefit of the early architecture definition was allowing tests to be designed for functional modules, both for internal diagnostics and for manufacturing test.

After the overall architecture of the HP 7978A was established, it was possible to review the technologies that could be best used to implement the product. The following technologies became crucial to the final performance and reliability of the HP 7978A:

(continued on page 14)

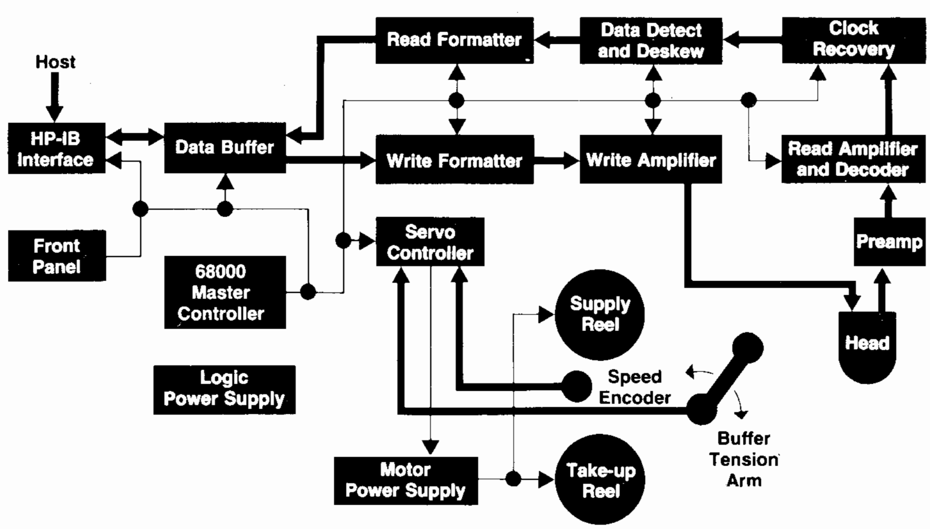

Fig. 2. *Basic architecture of the HP 7978A Magnetic Tape Subsystem.*

LSI Simplifies Tape Drive Electronic Design

LSI technologies of various forms are used in the HP 7978A Magnetic Tape Subsystem. The decision to use LSI was made early, allowing certain advantages during the development of the product. There are a number of good reasons to use custom and semicustom LSI circuits in addition to standard off-the-shelf LSI components. Among these are reductions in cost and size. Although not of direct importance in a large tape drive, certain advantages come from size reduction. The reduction in parts count directly affects large system problems such as noise, propagation delay, and timing. In addition, the use of LSI circuits reduces the need for complex designs, thereby reducing the problems associated with these designs.

When LSI components are used, the power supply requirements are greatly reduced, because the number of parts required is vastly reduced. An example of this is the HP 7978A's read formatter electronics. Were it not for the use of two LSI parts, hundreds of off-the-shelf parts would have been required (see article on page 19).

Architectural freedom is a prime motivation for using custom and semicustom LSI components. Having the freedom to decide the discipline best suited for design and being able to implement functions not found in standard off-the-shelf parts allows the designer to go straight to the solution with fewer restrictions.

Design Philosophy

The very nature of LSI technology lends itself well to the "Do it right the first time!" strategy used within quality circles. In keeping with this strategy, the approach for the HP 7978A was to design for LSI from the start. This affected the architecture and design strategy a great deal.

A primary consideration was tool development. HP's Greeley Division's strategy was aimed at developing tools for LSI design and making those tools available to every designer. In addition, the support of development projects such as the HP 7978A was of primary concern. Each custom LSI chip developed for the HP 7978A's electronics was done by two designers and one of the designers was provided by the HP 7978A design team. An efficient mix of LSI design skills, tools, and product knowledge resulted from this approach.

The Mead/Conway approach to LSI design was chosen.[1] This incorporated the use of lambda-based design having simplified electrical and topological rules. Additionally, having two "tall-thin" designers on each custom part helped guarantee success. This concept simply means that the designers are knowledgeable in every aspect of the chip design from the highest level of architecture down to the layout of individual cells.

Software Simulation

The need to check the design to verify correctness led to the use of software simulation of LSI on the HP 7978A. This was chosen over emulation techniques for several reasons. First, it was very easy to try new ideas and make modifications in software. In addition, the designer could choose the level at which the design was simulated, thereby simulating only the most critical timing situations at the transistor level and keeping the remainder of the design at a much higher level.

Closing the loop on a design requires two steps. Initially, the functional design must be completed. This requires the designers to define the function of each subsystem thoroughly, beginning at the topmost level. From the top, a functional decomposition must be done to yield concise blocks that can be fit together into a floor plan. These blocks should be fairly autonomous. Software simulation of the architecture gives the designers confidence in the design and verifies algorithm correctness.

Once the functional design is complete, the second step, verification, requires a transistor-level layout simulation. The simulator we used was extracted directly from the layout of the chip. Verification requires that the chip be simulated using the same stimulus as the functional simulator and the results compared with the simulator's results. Verification of the layout in this manner guarantees correctness, with the exception of critical timing situations.

Cells with layouts that are timing critical were checked using HPSpice, a simulation program used to model the analog behavior of a circuit. It is useful in modeling digital circuits where timing information is important. An HPSpice deck was extracted from the cell layout data and used by HPSpice. Once critical timing matters were resolved, the layout simulator was used to guarantee correctness.

This method of software simulation requires that the designer thoroughly investigate the environment of the chip to create realistic stimuli. The point of vulnerability is the designer's imagination.

Following this procedure resulted in fully functional LSI parts. Testing of these components in the HP 7978A yielded zero layout mistakes and a very small number of design errors.

Architecture

The HP 7978A's formatter function was broken down into two blocks, the data path and the control for the data path. The register-to-register construction of the data path fits well into the structured MOS design methodology. In addition, extensive modulo 2 arithmetic with large numbers of lookup tables and registers can be readily implemented using custom LSI. Once designed, the channel was stepped and repeated to form the parallel 9-bit environment inherent in the HP 7978A.

Controlling the data path using a series of state machines and counters fits well into PLA-based logic. The technology chosen for the HP 7978A was that of the universal synchronous machine (USM) developed at HP's Greeley Division. Its ease of implementation and other benefits made the USM fit nicely into the "designed for LSI" strategy of the HP 7978A project.

A PLA-based synchronous machine allows simplicity of programming in the sum-of-products form. Within the USM, the PLA area is segmented to allow its product lines to be broken and independent or semi-independent PLAs to be constructed. Storage at the PLA outputs in the form of flip-flops and feedback paths facilitates state-machine design. The flip-flops can be of several types to allow even more versatility.

Where great flexibility was needed, or in the case where the design did not have a good functional description, off-the-shelf LSI components such as microprocessors were used. The main controller in the HP 7978A makes use of a Motorola 68000 and the servo controller is an Intel 8051.

Reference

1. C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison-Wesley, 1980.

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■ LSI circuits
■ Intelligent systems
■ Electronics/mechanics optimizations
■ Modeling
■ Magnetics
■ Analog/digital electronics
■ Precision mechanics.

LSI became a critical factor in implementing a high-reliability product by replacing approximately 1200 TTL parts with eleven LSI circuits and 100 TTL support parts. Microprocessor control within the architecture allowed great flexibility and improved stand-alone capabilities of the product such as self-test and diagnostics. (See box, page 15.)

Electronic and mechanical optimizations, such as using random-access memory buffers to match host system performance rather than high-speed and high-acceleration mechanisms to do start/stop operations, allowed more reliability to be obtained and cost reductions to occur. Modeling was an essential part of all design decisions. Models allowed us to predict system performance for various tape drive parameters accurately. A tape drive specification was not selected randomly, but rather based on its effect on overall system performance. A good example is the chosen tape read/write speed of 75 inches per second. A higher speed was physically possible, but would not have provided improved performance in operation with a computer. However, a rewind speed of 250 inches per second could be implemented since no system interaction occurs and a minimal rewind time is a performance goal.

The magnetic characteristics of the tape and the read/write head were viewed both as a magnetics problem (waveforms and bit shift) and as a communication theory problem (transmission of data through various transforming media). At all times, data reliability was the most important design criterion.

Analog and digital electronics played roles in each subsystem. The read amplifier was an especially sensitive area with large signal amplification needed and minimal noise injection required for low error rates. The data buffer area had to be designed both to accept and to transfer data asynchronously, which led to a semicustom LSI controller design.

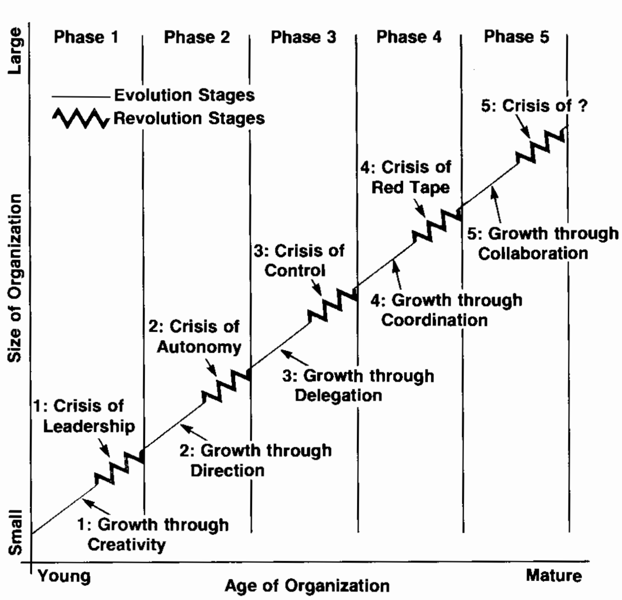

Fig. 3. *Organizational growth model as discussed by Greiner.*[3]

Precision mechanics is the heart of the tape handling system. The tape is sensitive and delicate and must be guided precisely. Many component tolerances are held to a few ten-thousandths of an inch to ensure a parallel tape path from reel to reel. At 9042 flux reversals per inch, the data can be easily distorted or destroyed unless exact speed, acceleration, and tension control are maintained.

Working in the above technologies required a major commitment to design tools. These tools came from various sources (HP proprietary, commercial CAD vendor, HP 64000 Logic Development System, etc.).

The architecture permitted design trade-offs that minimized real effects and used HP's strengths to a maximum. This was particularly noticeable in the decisions on hardware versus software implementations. Major revisions, such as the addition of "immediate response" to improve system performance (see page 30), could be made without a total redesign. The architecture was firmed up by specifications that defined each design area. These specifications were considered to be contracts between the design engineers. If any deviation was proposed or required, a formal change in the appropriate specification was made. With boundaries clearly defined, designs and subsystem testing could be carried on concurrently. By using this technique, designs with significantly different characteristics (LSI, software, mechanics, etc.) could be combined into a single product and efficiently managed. The specifications and other related documentation were put together in a book that was updated regularly and republished for anyone who needed data on the product or its design project.

Program Management

Since this was the largest project that HP's Greeley Division had ever undertaken, the plan for the project implementation received early attention. It was also very apparent that more than just an R&D team had to be assembled if the HP 7978A project was to achieve the improvements that other functional departments felt to be essential. These covered the range from accurate cost estimates to manufacturability goals. Meeting HP's corporate objective of significantly improving product reliability, the HP 7978A design goal of lowering the failure rate of an half-inch tape drive by a factor of five required a divisional commitment.

Thus, the project became a program very early. This program was centered around a business team, which drew members from all departments in the division and the R&D team. The milestones that determined when the project was ready to move to the next phase of development were established by these two teams. These goals formed a formal development plan, which was published and used as the final test to judge if a development phase was complete. This *a priori* definition avoided many arguments about what constituted a phase and limited discussion to considerations of whether or not a fixed set of goals had been

System Integration

The design of the HP 7978A tape drive was a challenging task involving large project groups and new technologies. Yet the completion of the product effort was only the first step in making the product successful. Without host system support, a new tape drive cannot be used for its intended purpose. For all of its capability, this new drive would remain unable to perform any useful function without complete integration of the product into computer systems. Initially this might seem as simple as writing a quick software routine to transfer data from system disc drives to the HP 7978A tape drive. However, an HP 3000 computer system involves a very complex set of interacting subsystems which all need to be considered when a new product is supported. The HP 3000 file system, tape drivers, diagnostics, and intrinsic system functions had to be modified to take full advantage of the advanced features available in the HP 7978A. In addition, complete environmental, EMC (electromagnetic compatibility), safety, reliability, and performance testing was required on all supported system configurations. Thus the addition of an HP 7978A drive to an existing HP 3000 system represented a complete product design in itself.

There are a few keys to successful system integration. These keys are:

- Designing the right product
- Communicating well
- Anticipating needs
- Using in-house expertise.

Designing the right product is a simple rule often overlooked by product designers. Attributes of the right product include low cost, high reliability, and high performance. However, just as important are the attributes that make it easier to integrate the product. Consistent architecture and I/O requirements make the design of drivers easier. Advanced internal diagnostics must complement system-level diagnostics. Complete and consistent documentation of the product contributes to easier integration.

Timely and accurate communication is the key to eliminating confusion and providing rapid feedback on problems. The HP 3000 Computer is produced by HP's Computer System Division in Cupertino, California. The HP 7978A is a product of HP's Greeley Division in Colorado. Early in the program all of the key players were identified with each department represented. Counterparts in each division were encouraged to interact directly with one another. One manager in each division formed the primary contact and was charged with full responsibility for coordinating the efforts of that division. Face-to-face meetings were held with all participants from each division and each department. The frequency of meetings increased as deadlines approached. This encouraged personal responsibility for assigned tasks. Since the HP 3000 division had many programs proceeding in parallel, this was an important way to focus everyone's efforts on the HP 7978A periodically.

With two divisions committing large resources to the program, it was imperative that all the required support be available when it was needed. From the HP 7978A team's point of view, we needed to provide everything required to make the other division's effort efficient and successful. We used PERT charts to schedule all development and testing. This gave us a clear idea of when prototype units would be required and in what quantity. Since prototype HP 7978A drives were at a premium, it fell to the coordinating manager to understand the HP 3000 division's tests well enough to provide efficient scheduling. One of the most difficult tasks proved to be the tracking of prototype hardware upgrades. These upgrades usually consisted of ROM changes, but often included hardware changes. It was critical that these changes be coordinated and tracked so that errors reported in the other division's testing could be appropriately evaluated. Eventually we found that all prototypes had to be upgraded at the same time so that there was never a question of product "generation." A particularly successful aspect of anticipating needs grew out of our own need for consistent and complete documentation. Since the HP 7978A project was large, it was imperative that even early documentation be controlled. Valuable time can be lost when one engineer proceeds using dated or erroneous information. Since our documentation was standardized from the start, it made it much easier to provide everyone with useful information before the information was needed.

Using in-house expertise to augment host division efforts was very useful. Our division already enjoyed a proven reputation for design and manufacture of reliable, high-quality hardware products. Our coworkers from the HP 3000 division were software experts drawn from the HP 3000 R&D labs. Thus our experience made us the more logical group to work with the other division's environmental test and reliability engineering departments on hardware testing. To this end, we performed most of the required system hardware testing, leaving the HP 3000 R&D team to concentrate on driver development and software performance testing.

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achieved. Thus, the entire organization was always aware of the goals for each development phase.

The goal of the business team was to manage the HP 7978A product development as a program. Other departments could assign members well in advance of critical interaction periods, permitting them to contribute to the conceptual definition of the product. Their continuing role in the program ensured that the product was optimized in all areas of concern. Each member of the business team was responsible for publishing an interaction and support plan that stated the exact relationship of that member's department to the program.

The R&D team was initially an architectural definition team with key members from all relevant engineering disciplines. After the architecture was solidified, subteams began detailed planning for the product. An early realization was that the use of LSI technology would be an extremely important part of the HP 7978A. A separate project group was formed to ensure that appropriate processes and tools were available (see box, page 13). Thus, from its very inception, the development of the HP 7978A was a multigroup project.

The early knowledge of this program's complexity and potential staffing growth led the management team to evaluate the structure of the program and their own roles in it on a continuous basis. The management of complex and dynamic projects can be viewed as similar to organizational growth as detailed in reference 3. This model, shown in Fig. 3, implies that a number of crisis stages of management will be reached as an organization grows. This pattern was true for the HP 7978A program. As the size of the organization and the complexity of the interactions increased, several management crises arose. In the early stages the problem was the division of responsibility and the span of control, so that the project managers felt that each of them was a full partner in the program. Later, it was realized that management specialists were required in certain areas such as software or system integration. The later stages of the program required that a program manager make decisions across department and division boundaries.

Many management lessons were learned as the program evolved. While none was unique or new, they still were learned by the traditional methods of finding a problem and working it out. The management team's approach to ensuring success was an outstanding experience, a classic example of management by objectives. The objectives for the product were agreed upon by the division's functional staff and the implementation was delegated to the responsible managers. The program was placed under a program manager with each functional area providing resources to ensure that the program was successful. Reviews were held for major checkpoints or when serious issues surfaced.

The critical management tools for this program turned out to be technical competence and flexibility, egoless and noncompetitive management teams, willingness to experiment with the organization, immediate response to critical issues, and ownership of all problems. This tool set allowed a broad and changing group of managers to contribute to the program effectively.

Acknowledgments

The HP 7978A program had a rather large project team and it would be very difficult to single out each of the many individuals who contributed during the long development cycle in the wide range of technical and management issues. To those not mentioned here, thank you for your contribution to the success of the HP 7978A.

The authors would like specifically to recognize the project managers on the HP 7978A, who were able to be significant technical contributors while accepting the responsibility for managing all aspects of the project. These were Alan Richards, Gordon Thayer, Clair Nelson, John Meredith, Tom Bendon, and Don Stavely.

Jim Jonez provided invaluable market information and was an integral contributor in making major product decisions.

Special thanks must also go to Curt Brown, our section manager, and Rex James, our R&D lab manager, for their inspiration and program focus.

References

1. *ANSI X3.54-1976 GCR.*
2. *ANSI X3.39-1973 PE.*
3. L.E. Greiner, "Evolution and Revolution as Organizations Grow," *Harvard Business Review*, July-August 1972.

Write and Read Recovery Systems for a Half-Inch Tape Drive

by Wayne T. Gregory

THE ANALOG ELECTRONICS SYSTEMS connected to the head assembly in the HP 7978A Magnetic Tape Subsystem are responsible for writing and reading data on the tape in an error-free manner. These basic functions are separated into the write electronics, data protection, and read electronics.

Analog Write Electronics

The purpose of the analog write system is threefold. First and foremost, the circuitry must ensure that data is never accidentally altered or destroyed. Second, the circuit is responsible for recording digital data in the form of magnetic flux transitions on half-inch-wide magnetic tape. This second task must be accomplished such that the recorded amplitude and flux transition spacing are within the limits specified in the ANSI specification for data interchange using half-inch magnetic tape. Last, this system must be able to erase all data formats that have previously been specified for half-inch tape by ANSI. These formats are 800 NRZI,[1] 1600 PE,[2] and 6250 GCR.[3]

Fig. 1 shows a block diagram of the analog write electronics. Control signals from the master controller set up the current drivers for operation in either PE (phase encoding) or GCR (group coded recording) mode and control operation of the erase current driver. The other control signals to the write system come from the write enable sensor on the tape drive hub and from the system power supply. These signals are used by the write enable electronics. The write system returns to the master controller the write enable status and a signal that indicates that the magnetic recording head is plugged in.

The circuit shown in Fig. 2 translates the digital data signals from the write formatter to currents flowing in the recording head. Since the magnetic flux generated by the recording head is approximately proportional to these currents, the digital data becomes regions of alternating flux polarity stored on the magnetic media.

The circuit is a cascode differential current driver which is used to switch current from either of the two windings of the center-tapped recording head. Connected in the emitter circuit are two magnitude-controlling current sources. One current source is set for a constant value and the other is pulsed each time a data transition occurs. The common-base transistors are used as an externally controlled write-protect circuit.

The HP 7978A uses a dc erase system which, when energized, sets up a constant magnetic flux across the half-inch width of the recording tape. Whenever data is recorded, the erase head is energized and the magnetic tape is passed across it before reaching the data recording head. The erase circuit is a simple switched current source with write protection features.

Write compensation is used during the recording of data to improve the quality of the recorded flux transitions. This compensation improves two undesirable attributes of the recorded data: bit shift caused by a low-frequency-response head/media system and baseline shift caused by a system using a dc erase with a nonsaturating recording format.

A simple way to understand the main cause of bit shift is to think of the output of the recording system as a summation of the responses caused by each flux transition. Each transition produces an output pulse from the recovery head with a pulse width that is a significant portion of the nominal bit spacing (see Fig. 3). Furthermore, because of the shape of the recording head flux distribution and the media motion, the pulse is not symmetrical. As can be seen in Fig. 3, when two adjacent pulses are summed, the locations of their peaks are pushed apart. Since the digital information is stored in the location of each peak (i.e., each digital transition), compensation that decreases bit shift yields a low recovery error rate and simplifies the recovery problem. The HP 7978A's write compensation scheme reduces bit shift by effectively narrowing the isolated pulse response so that the summation of two adjacent pulses does not push their peaks apart. This is accomplished by including a small opposing current transition following each data transition. This accelerates the decay of the waveforms shown in Fig. 3, effectively narrowing the pulses. This technique, which is commonly used in half-inch magnetic tape recording, has been described in detail

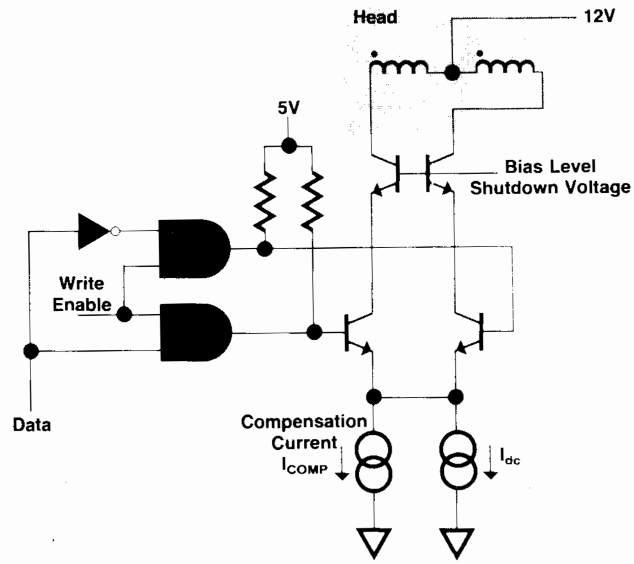

Fig. 2. *Simple schematic of current driver for magnetic recording head.*

in articles and texts on magnetic recording.[4,5] The same circuitry also aids data recovery by improving the baseline shift caused by the dc erase current. This improvement is made by driving the write driver with more current when it is recording a flux transition. This current is of the opposite polarity to the current generating the erase state flux.

Data Protection

The recording and erase circuitry for a mass storage device must provide protection against accidental destruction of data. This is true for any storage device and even more true if the device is a backup device such as the HP 7978A. The ANSI standards for half-inch data formats provide for a plastic ring which fits into the back of each tape reel. If this ring is removed, the tape is write protected. When a tape reel is loaded on the HP 7978A, an optical sensor measures whether this write enable ring is installed. This information is reported to the master controller and on a direct line to the analog write circuitry. If the write enable ring is not installed on the tape reel, then the record and erase circuits are disabled by hardware. The analog write

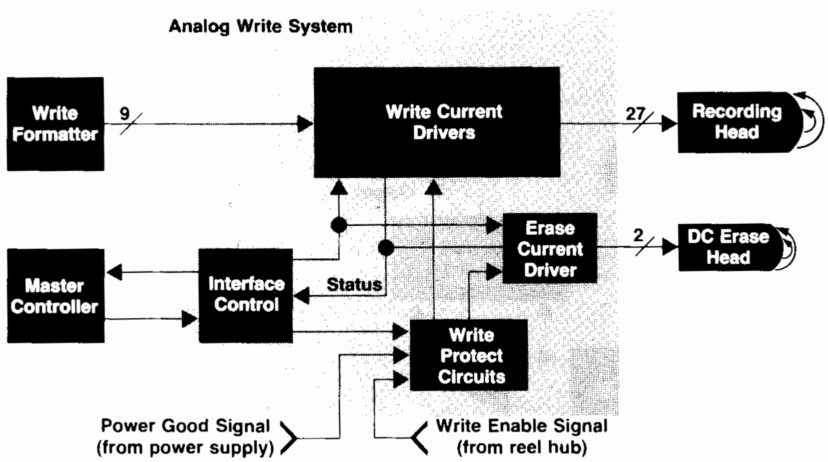

Fig. 1. *Block diagram of the analog write system for the HP 7978A Magnetic Tape Subsystem.*

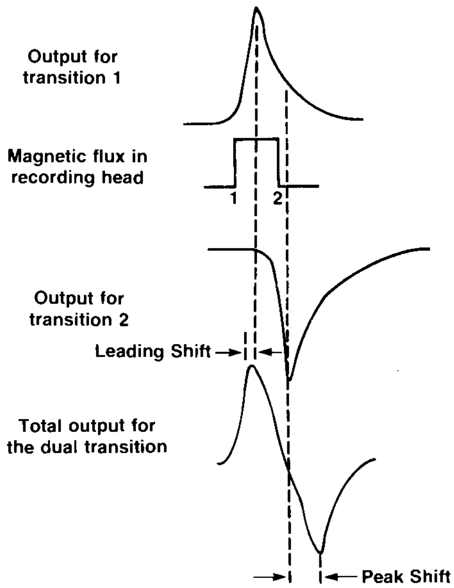

Fig. 3. *Bit shift can occur when two adjacent signal pulses of opposite polarity are recorded. The locations of their peaks tend to be pushed apart on the tape.*

circuit also reports to the master controller the state of this write enable signal. Therefore, the write-protect condition is signaled to the master controller by two different pieces of hardware and the write/erase functions are disabled by circuitry in the write/erase system.

Another condition that must be prevented is an accidental destruction of recorded data during a power-fail condition. The HP 7978A provides this protection by monitoring the output of a signal generated from the primary switching voltage on the system power supply board. When this signal falls below a specified level, the write/erase system is held in a special power-fail write-protect mode.

The final data protection scheme is a self-check used by the master controller to verify that the erase and write enable control signals are functioning properly. This allows the master controller to detect faulty write or erase hardware.

Working together, these write protect systems ensure that valuable backup data is never lost through a system malfunction or during system power failure.

Analog Read Electronics

The purpose of the analog read recovery system is to convert the flux transitions recorded on the tape to digital transitions. This conversion must be accomplished without altering the transition spacing by more than 1% relative to the nominal transition spacing of the data rate.

As shown in Fig. 4, the read recovery system is a standard recovery scheme which uses a preamplifier, low-pass filter, active differentiator, and zero-crossing detector to convert the magnetic flux transitions to logic-level signals. These circuits, working together with an amplitude threshold detector, provide a recovery system that is capable of detecting dropouts and data gaps, automatic adjustment of system gain level, and recovery with a 33-dB signal-to-noise ratio, which adds less than 1% phase error.

The system preamp, which for noise reasons is mounted close to the magnetic recovery head, provides a gain of 40 dB with a 3-dB bandwidth of about 10 MHz. After it is amplified by the preamp, the data signal is amplified further in an adjustable gain control stage which is capable of providing a gain from 0 to 9 V/V. The gain control stage drives a passive fourth-order, linear-phase low-pass filter which has a 1-dB bandwidth of about 400 kHz. After this point, the signal is processed by the differentiator stage. The differentiator converts the amplitude peaks to zero crossings by passing the signal through a bandpass filter function that has a peak amplitude response around 500 kHz (1.5 × the maximum data frequency) and then rolls off at a rate of −60 dB/decade. The signal is then input to the zero-crossing voltage comparator and converted to a TTL-level signal. The TTL signal is processed by the amplitude threshold circuits to determine if a logic transition is valid data and then sent to the clock recovery phase-locked loop to be processed further.

References

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2. Group coded recording, *ANSI X3.54-1976.*
3. Nonreturn to zero, inverted, *ANSI X3.22-1973.*
4. F. Jorgensen, *Magnetic Recording*, TAB Books, 1980, pp. 262 and 270.
5. L.E. Ambrico, "Pulse Crowding Compensation for Magnetic Recording," Computer Design, Vol. 11, no. 6, June 1972, pp. 55-60.

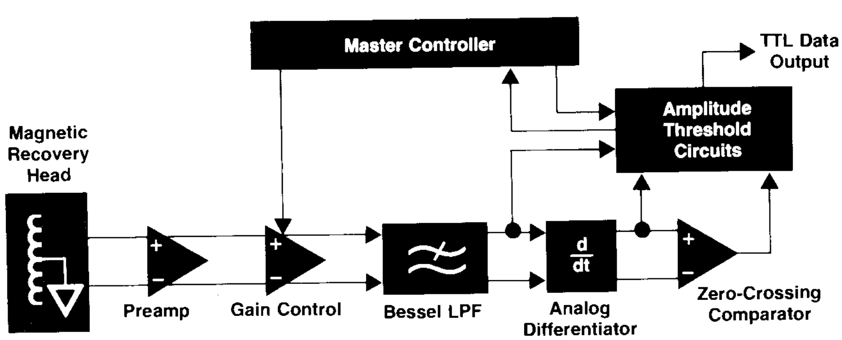

Fig. 4. *Block diagram of analog read recovery system.*

Digital Formatting and Control Electronics for Half-Inch Tape Data Storage

by Jimmy L. Shafer

READ RECOVERY and read/write formatting of the nine-track data in the HP 7978A Magnetic Tape Subsystem are fairly complex tasks. Made up of four major assemblies, the digital formatting and control electronics handles read formatting, write formatting, data deskewing, clock recovery, and on-board diagnostics. The system is designed to support both GCR (group coded recording) and PE (phase encoding) formats in a transparent manner. To minimize board space and reduce cost, the functions are heavily integrated.

Read Formatter

The read formatter in the HP 7978A must read and decode data, correct errors, and detect problems in the retrieved and corrected data. The read formatter design (Fig. 1) centers around two LSI parts. The Read IC is a custom LSI chip that contains the data path portion of the design. A semicustom LSI chip is used to implement the read formatter controller for the data path. Together, the two integrated circuits perform the task of formatting the read data, which includes error correction and detection.

The Read IC is largely composed of a register-to-register data path that is controlled by the read formatter controller. The Read IC makes use of synchronous logic design and is required to run at a slower clock rate than would otherwise be possible with TTL design. The result is that the Read IC contains pipelining to allow parallel calculations while the data propagates along the path. In this way, an MOS design structure is maintained. The cost of pipelining in LSI is relatively cheap, thereby justifying the trade-offs.

GCR Format Architecture. The overall block diagram for the Read IC appears in Fig. 2. This block diagram includes the circuitry used for all three data formats. Some portions of this circuitry are used less extensively for particular formats. The data path consists of a 5-to-4-bit converter, mark detection circuitry, error detection circuitry, error correction circuitry, track-in-error accumulator, and error correction verification. The chip architecture is based primarily on the requirements of the GCR data format. ANSI Standard X3.54-1976 gives the details of this format,[1] but the following brief overview should be enough to understand the read formatter.

The GCR format is designed to add sufficient data redundancy so that errors in up to two tracks of recorded data can be corrected. To make this possible, the data is divided into seven-character blocks. An eighth character must be added to complete a data group. This character is supplied by the error correction character (ECC.)[1] The ECC is formed by using the preceding seven data characters as input to a polynomial generator. Each data group is divided into two four-character subgroups (see Table I).

Each subgroup of four characters (including the parity bits) is now expanded to a storage subgroup of five charac-

Table I

Data Group to Storage Group Conversion

	Data Group		Storage Group	
Physical Tape Tracks	Data Subgroup "A"	Data Subgroup "B"	Storage Subgroup "A"	Storage Subgroup "B"
1	D D D D	D D D E	X X X X X	X X X X X
2	D D D D	D D D E	X X X X X	X X X X X
3	D D D D	D D D E	X X X X X	X X X X X
4	P P P P	P P P P	X X X X X	X X X X X
5	D D D D	D D D E	X X X X X	X X X X X
6	D D D D	D D D E	X X X X X	X X X X X
7	D D D D	D D D E	X X X X X	X X X X X
8	D D D D	D D D E	X X X X X	X X X X X
9	D D D D	D D D E	X X X X X	X X X X X
Group Positions:	1 2 3 4	5 6 7 8	1 2 3 4 5	6 7 8 9 10

NOTE: Data is recorded in 9-bit characters (across the tape) in blocks 10-bits long. This 90-bit group is called a "storage group." Before conversion to the recorded code valnes, there are eight linear bits made up of seven data bits and one check bit. This group of 72 bits is called a "data group."

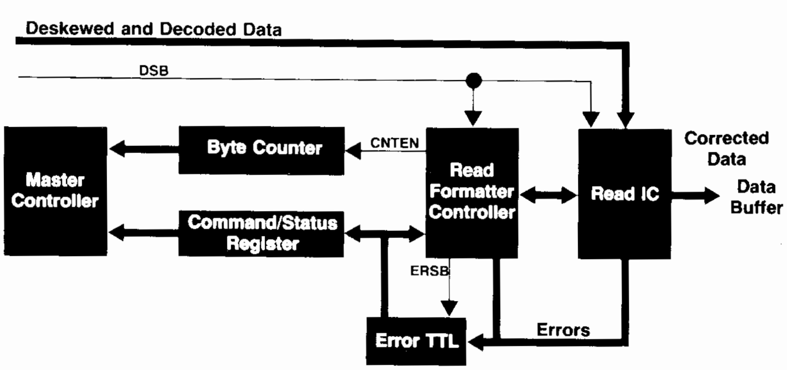

Fig. 1. *Block diagram of read formatter subsystem for HP 7978A Magnetic Tape Subsystem.*

ters. This is done by taking four bits, one from the same bit position of each character, and translating them to a 5-bit code as defined by the ANSI standard. (See Table II for conversion definition.) When reading, these 5-bit storage subgroups must be decoded back into the 4-bit data subgroups. This is handled by the 5-to-4-bit converter within the Read IC.

Data reliability has already been enhanced three ways. First, the extra bits added to the data groups increase the Hamming distance* between data bytes, making it less likely to read one byte as another. These bits are actually added to ensure that no more than two zeros occur in a row, making self-clocking possible with NRZI (nonreturn to zero, inverted) encoding. Second, a parity bit is included to identify characters with single-bit errors. Finally, the ECC contains redundant information about the data in the group, making it possible to determine which bits, if any, are in error. The read electronics also provides track-in-error signals for any track with low output or excessive phase delay, thus increasing the correction capability.

*The number of symbol places in which two words of the same length differ from one another. Also called the Hamming metric.

As an extra margin of safety, the GCR format is designed to ensure that any data bit changed as the result of an error correction is one that really should have been changed. The format uses two overall cyclic redundancy checks (CRC and Auxiliary CRC) as verifications for data integrity. The checks are meant to indicate the occurrence of errors, but they have no capability to correct them. Two CRCs are used so that one will identify any errors that the other is incapable of detecting. CRCs (like the ECC) are generated by modulo 2 polynomial arithmetic. This arithmetic is performed by the read formatter and the results are compared to the CRC and ACRC supplied with the data, thereby verifying both good and corrected data.

The CRC is used in its own group, known as the CRC group. The CRC group also contains a character called the residual character. This character is two counts (modulo 32 and modulo 7) of the number of characters in the full data block. The modulo 7 count indicates how many valid data characters will appear in another group called the residual group, and the modulo 32 count is used to determine whether an odd or even number of characters exist in the block.

The residual group (see Fig. 3) contains other information of interest. It contains any extra data characters when there are not seven characters left to make a group. Thus the residual group will contain at most six valid data characters for the entire record. Pad characters are added as required to ensure that six characters in the residual group are filled. The seventh character is the ACRC. This group is treated as any other. An ECC is generated and the 8-character group

Table II

Record Code Values

Data Values (Group Positions: 1 to 4/5 to 8)	Record Storage Values (Group Positions: 1 to 5/6 to 10)
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

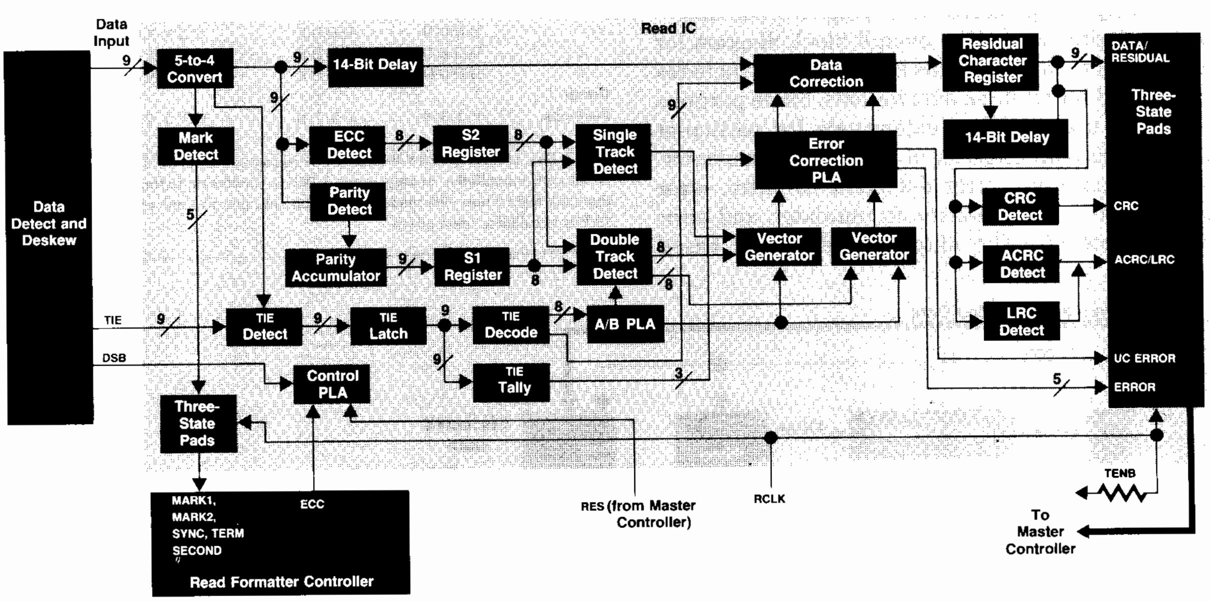

Fig. 2. *Block diagram of custom LSI Read IC used in the read formatter.*

is translated to a 10-character storage group.

The CRC and ACRC are arranged in the architecture so that the CRC generator can include the ACRC as an input to its polynomial. The CRC also makes use of whatever pad characters are inserted into the data blocks while the ACRC does not. However, both the ACRC and the CRC are grouped into 7-byte data blocks. Each of these blocks has an ECC generated and appended at the end. The blocks are then translated into two 5-character storage subgroups as illustrated by Tables I and II.

The blocks described so far have explained the generation of data groups, the CRC group, and the residual group. All that remains in any data record are the control marks. Control marks include the preamble, the postamble, the resync fields, and the end mark. Referring to Fig. 3, the preamble is used to announce the arrival of a data block under the read head. It identifies the beginning of the record with the TERM and SECOND marks. It provides 14 sync subgroups to allow the read electronics to sync with the data. A MARK1 indicates the arrival of data. Next, a set of 156 data groups is written on the tape. This set is followed by a resync burst to allow the read electronics to relocate its position. A resync burst consists of a MARK2, two SYNCs and a MARK1. This sequence of 156 data groups followed by a resync burst continues until all data (except for any residual amount of data less than seven characters) is written to the tape. Now an end mark is written. Following the residual group and the CRC group, a postamble is written. The postamble is a mirror copy of the preamble except that the last character ensures that the tape will be left in the unfluxed state. The postamble signals that the end of the block has occurred and can be used as a preamble if the tape is read backwards.

Additional control marks can be written outside of a data block. These marks serve to identify the start of the tape and indicate the recording format being used. In the GCR format, there is an automatic read amplification burst to help calibrate the read electronics to the signal levels on the tape. Finally, a tape mark is available for the host computer to use to indicate file bounds. Interblock gaps appear between data blocks or tape marks.

This discussion leads to the use of the mark detect function indicated on the Read IC block diagram (Fig. 2). This block contains nine decoder PLAs (programmable logic arrays). The Read IC decodes the control marks with each clock and the read formatting controller decides which ones are valid. These marks become internally generated stimuli that are used in the read formatting controller for decision making and timing of control functions.

PE Format Architecture. The Read IC can read data in the phase encoding format at 1600 characters per inch.[2] Referring to the data path block diagram (Fig. 2), the PE data path uses the GCR data path with certain areas used less extensively. Transition information from the read head is encoded to include a phase and data window for each byte, according to ANSI Standard X3.39-1973. The PE format has no imbedded control marks or any redundancy codes. The data block consists of a preamble, the data, and a postamble. The only additional marks are a format identification at the beginning of the tape and tape marks included at the host computer's option.

PE guarantees that a transition occurs in every data window. Each phase window (level restoring) may have a clock transition, depending upon the data to be written and the previous state of the tape.

Read Interfacing. As shown in Fig. 1, the interface for the read formatter is made up of three functions. The first is the interface to the master controller. The read formatter

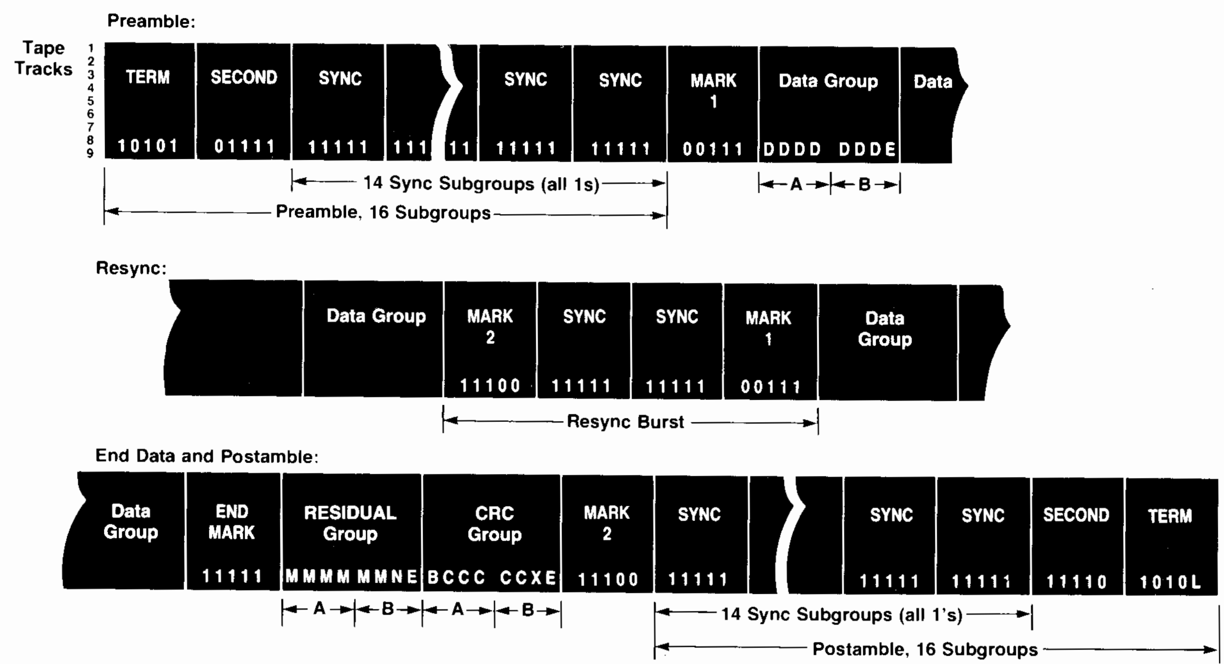

Fig. 3. *GCR tape format. Legend: D = data character, H = pad or data character, X = residual character, E = ECC, C = CRC, N = ACRC, L = last character, and B = CRC or pad character.*

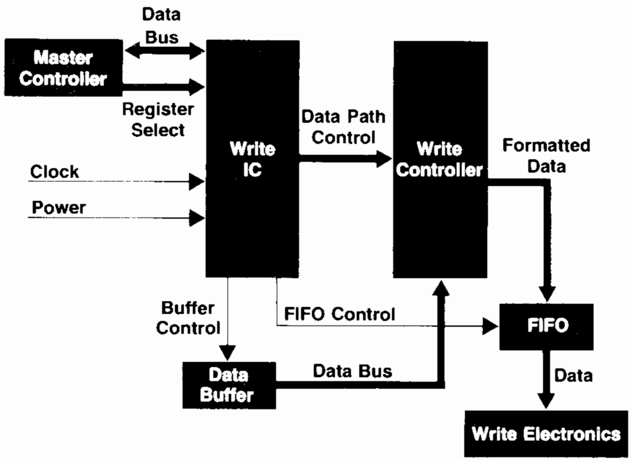

Fig. 4. *Block diagram of write formatter subsystem.*

accepts information from the master controller that indicates the density of recording and the mode of operation. A status word indicating the success of the read operation is accessible via this interface to the master controller. Finally, the master controller can access the byte count to determine the number of bytes passed through the read formatter.

The data buffer interface allows the read formatter to pass the corrected and formatted bytes to the data buffer. A full handshake occurs between the two functions to ensure data integrity. The data is in the form of an 8-bit byte with a parity bit.

The last function is the data detect and deskew interface. This function deskews the data before sending it to the read formatter. In addition to the nine data tracks, nine track-in-error pointers are generated by the deskew function and provided to the read formatter through this interface.

Write Formatter

The format recorded on the tape by the HP 7978A is selected by the host. For GCR, the write formatter must encode the data into GCR storage groups, which include the error correction character ECC. Also, control groups must be inserted into the data stream properly to meet the specifications according to ANSI. PE data also requires control groups, but not the error correction information. To allow read verification, the cyclic redundancy checks must be calculated and inserted into the data stream. In addition to these, other bursts required by the supported formats must be generated by the write formatter. These include tape marks, density IDs, and automatic read amplification bursts.

Two LSI parts make up the heart of the write formatter design (Fig. 4). The Write IC is a custom CMOS LSI chip, which makes up the data path of the write formatter. The other LSI chip, a semicustom design, forms the write controller. Some TTL circuitry, including a FIFO (first-in, first-out) buffer, makes up the remainder of the system.

Using the register-to-register pipelining scheme previously mentioned for the Read IC, the Write IC forms the data path portion of the design. Like the read formatter, it is synchronous and controlled externally by its controller, the write controller. The Write IC is implemented using HP's NMOS-CP process and replaces approximately 90 SSI/MSI/LSI parts, thereby reducing cost and enhancing reliability. As shown in the block diagram (Fig. 5), the circuit consists of a parity checker, a 7-byte-deep shift register, polynomial generators for CRC, ACRC, and ECC characters, a residual character generator, a 4-to-5-bit encoder, a control mark generator, a phase/flux encoder, and multiplexers for controlling the flow of data across the chip.

Write Interfacing. Referring to Fig. 4, the interface for the write formatter is made up of three functions. The master controller indicates to the write formatter the mode of operation and the density of recording across a command interface. Also, the master controller issues to the write formatter the type of block that needs to be formatted. These include data, tape mark, or some other control burst. The status of the write operation can be read by the master controller across the status interface.

Next is the data buffer interface. Eight-bit bytes of data are sent across this interface with a parity bit. An end-of-data (EOD) bit accompanies the last byte. A full handshake takes place between these two subsystems to guarantee data integrity.

Finally, the write formatter interfaces to the write electronics. This is accomplished using a FIFO buffer. The purpose of the FIFO buffer is to create a synchronization boundary between two asynchronous systems. Data leaves the write formatter system in nine-track form.

Data Detect and Deskew

Before the read formatter can attempt to read the data, the data bits must be realigned across the nine tracks. Misalignment of the bits is caused by mechanical variances (such as head skew) and electrical propagation delays. The job of realigning the nine-bit bytes is done by the data detect and deskew (DDD) circuitry. In addition to realigning the data in the nine tracks, this circuitry must also identify

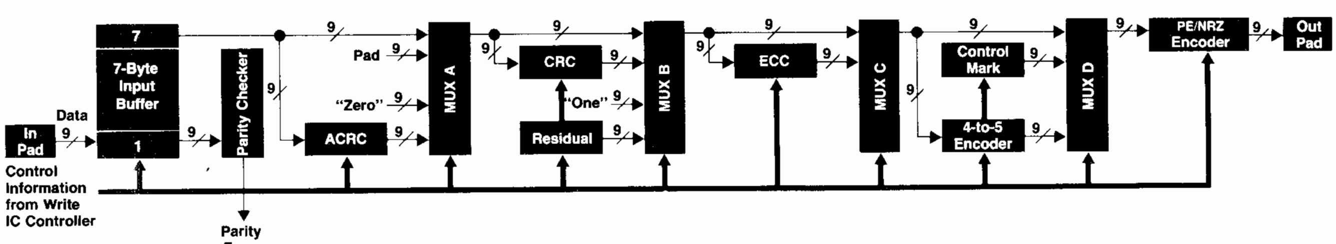

Fig. 5. *Block diagram of custom LSI Write IC used in the write formatter.*

the type of burst under the head and report this information to the master controller. This allows the master controller to manage the read/write operations appropriately.

In Fig. 6, the block detection portion of the architecture can be seen. Track activity recognition is fed to the master block detect to allow a tally to be done for block detection purposes. Block type information is relayed to the master controller. In addition, gap information is sent to the read formatter and to the servo controller.

The job of recognizing track activity is performed within each of the slave deskew subassemblies. The slave deskew subassemblies are implemented using semicustom LSI chips called USMs (universal synchronous machines; see box, page 13). There are two tracks of slave deskew in each 40-pin USM, requiring that five of these chips be used.

The nine slave deskew subassemblies send their track activity information to a single USM called the master block detect. Here, a tally of this information is used to determine the type of block currently under the head. These include data blocks, automatic read amplification bursts (in GCR), tape marks, and density IDs. Upon encountering a new block type under the head, the DDD circuitry interrupts the master controller and makes this information available to it. In addition, the master block detect USM acts as an interface to the master controller. A bidirectional read/write port allows handling of commands and status. Information from the master controller is relayed to the remainder of the DDD circuitry by the master block-detect USM.

In addition to detecting track activity, the slave deskew USMs must also detect control marks for deskewing the data. This requires that each track identify sync marks within the data stream and report this information to the master deskew USM. Each slave deskew USM has control over its individual FIFO buffer. These 64×4-bit buffers allow deskewing across the nine data tracks and create a synchronization boundary between the clock recovery subsystem and the DDD circuitry.

To ensure that the maximum allowable skew of 25 bits is not exceeded, the master deskew USM checks the skew and can force the release of the FIFO buffers as necessary. A majority vote is taken by the master deskew USM to determine when enough of the tracks have been deskewed to recover the data. In all cases, the master deskew USM will wait as long as possible to allow all nine tracks to be deskewed.

Error pointers are generated within the deskew portion of the DDD circuitry. These track-in-error pointers accompanying each track are an accumulation of the lock-detect information provided by the clock recovery subassembly and the internally generated error information of the DDD circuitry. Tracks that cannot be deskewed and "dead tracks" fall in the second category.

As shown in Fig. 6, the DDD subassembly interfaces to the master controller, the clock recovery circuit, and the read formatter. Data into this subassembly is from the clock recovery circuitry in the form of nine tracks of data accompanied by individually recovered clocks. An indication of data integrity from the clock recovery circuitry in the form of a lock-detect signal also accompanies each data track.

Deskewed data leaves the subassembly and is sent to the read formatter with error pointers indicating bad tracks. The data is strobed to the read formatter in 9-bit bytes and a full handshake is done between the two systems.

The master controller has access to information about what type of block is currently under the head, as well as information about the success of the deskew operation. Blocks are verified by the data detect and deskew circuitry, both when they are written and when they are read.

Clock Recovery

The clock recovery board contains nine channels, each made up of a phase-locked loop and a discriminator (Fig. 7). The phase-locked loop reconstructs a data clock that is used to clock the data into the DDD circuitry. Detection of phase lock and loop control are performed by the discriminator.

The phase-locked loop for each channel is made up of the phase detector, filter, bias network, and VCO as shown in the block diagram. Each loop feeds back the data clock signal DCLK to the phase detector where it is compared with the incoming data and correction is applied to the VCO. The amount of correction is determined by the phase detector. The filter integrates the correction signal and filters out high-frequency phenomena such as bit shift, asymmetry, and noise. The resulting error voltage is filtered and applied to the VCO.

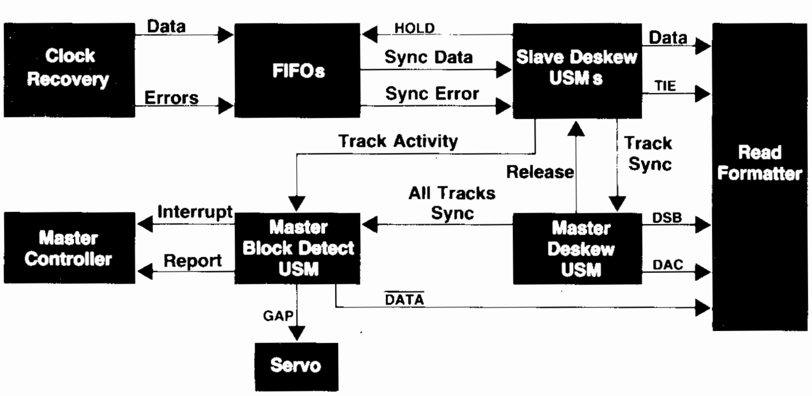

Fig. 6. *Block diagram of the data detect and deskew circuitry.*

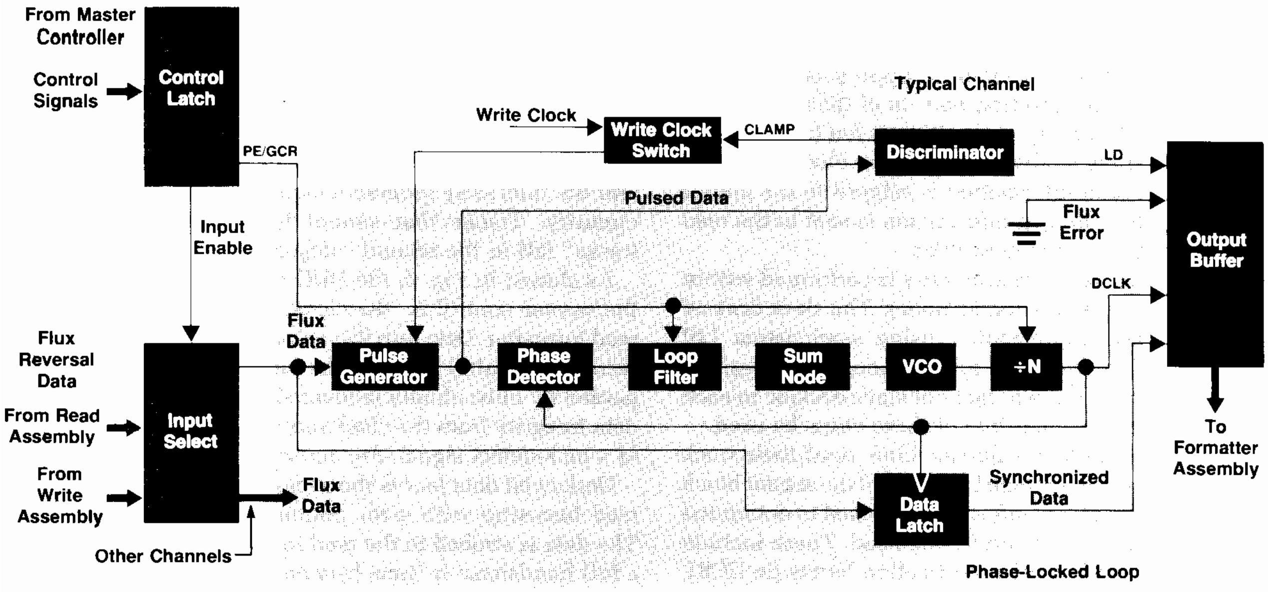

Fig. 7. *Typical channel of the clock recovery subsystem with common control circuits.*

The discriminator is a state machine that creates two signals. The lock detect signal LD is sent to the data detect and deskew section of the formatter board. This signal indicates when the probability is high that the loop has acquired the data and is locked.

CLAMP is the second signal created by the discriminator. It is used to select between data entering the phase-locked loop or the write clock. The write clock is the data rate clock created on the write subsystem for writing data to tape. The ability to switch between the two is used to force the loop to maintain lock to a frequency that is very close to the actual data frequency. If CLAMP is true, forcing the loop to lock to the write clock, and data is encountered, the discriminator sets CLAMP low, allowing the loop to acquire real data. Whenever an extensive dropout occurs (128 windows without data) the discriminator sets CLAMP high, forcing acquisition to the write clock.

Control signals from the master controller determine the environment in which the phase-locked loop is expected to function. When the density of recording is changed from GCR to PE, the loop switches its divide-by-N circuitry by a factor of three to allow recovery at PE densities.

Diagnostics

Diagnostics have been built into the read electronics to allow self-test capability. Two modes of this self-test can be selected by the master controller. One mode loops data from the data buffer through the write formatter, data detect and deskew circuitry, and read formatter back to the data buffer. This mode checks the formatter subsystem. Errors can be injected by allowing the master controller to select various tracks to be "killed." In this way the error correction capability of the read formatter can be checked.

Second, the data can be looped in a similar fashion with the addition of the clock recovery subassembly. This checks the clock recovery circuit's ability to acquire the data and maintain lock. In addition, the inherent delays associated with the electronics force the data detect and deskew subsystem to perform synchronization and deskewing.

References

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Streaming Tape Drive Hardware Design

by John W. Dong, David J. Van Maren, and Robert D. Emmerich

AS A STREAMING TAPE DRIVE, the HP 7978A Magnetic Tape Subsystem requires much simpler mechanical and electrical hardware then a start/stop drive with a capstan motor. The main items that are simplified are the tape path hardware and the servo electronics. Fig. 1 shows a block diagram of the HP 7978A. A start/stop capstan drive would require another motor as well as an extra tape buffering device. Capstan motors and tape buffering devices are fairly expensive. Eliminating these items reduces the factory cost substantially.

The HP 7978A uses two controllers to run the drive, a master controller and a servo controller. Based on a 68000 microprocessor, the master controller controls the data path electronics, the HP-IB (IEEE 488) interface, the front-panel display and keyboard, and the servo controller. The servo controller, which uses an 8051 microprocessor, controls the tape movement servo system and corresponding mechanical hardware.

Performing the same function on both drives, the data path electronics for a start/stop drive are very similar to the electronics for a streaming drive. The data path electronics are much more complex in a drive that uses the group coded recording (GCR) method of formatting data. In previous tape drives, this method of formatting data was implemented in TTL circuitry. The HP 7978A tape drive uses LSI components to reduce the data path electronics parts count from thousands to hundreds, resulting in a great increase in reliability and a large reduction in cost (see box on page 13).

Tape Path

The HP 7978A tape path has several major components: the main casting, the head plate assembly, the buffer assembly, the speed sensor, the supply hub and motor, and the take-up reel and motor. The latter five components are mounted on the main casting as shown in Fig. 2.

These components serve two major functions. The first is to guide the magnetic tape past the head in a predictable manner, compatible with the standard written tape formats used by the HP 7978A. These include the usual tracking and constant-speed constraints. Nine-track tape drives also have the additional constraint of writing the nine parallel bits of a single byte within a given distance along the tape. The distance is specified by the established tape format for compatibility. This is the skew requirement, which for the 1600 PE (phase encoding) format is 625 microinches over the width of the half-inch tape.

The HP 7978A tape path is designed to minimize skew caused by the variations in the positions of various components. These effects were modeled by treating the tape as a cantilever beam with four supports. These supports are the buffer and speed rollers and the two fixed guides on the head plate assembly. The model worked well in predicting the effects of component variances on skew, and was used in determining the final positions and allowable tolerances of the various tape path components.

The second major function of the tape path components is to move the tape gently and without damage from one reel to the other. This is facilitated by minimizing the

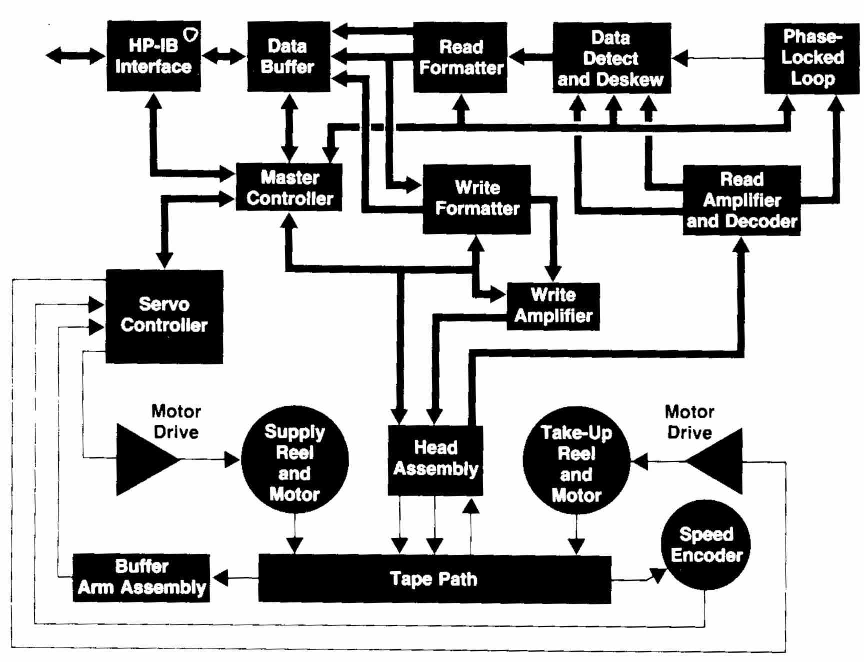


Fig. 1. *Block diagram of HP 7978A Magnetic Tape Subsystem. This half-inch tape drive is based on a streaming tape design as opposed to the more common start/stop tape drive designs.*

number of components touching the tape. Only seven items contact the tape between reels. Only three of them contact the oxide side of the tape, which is the side where the data is written.

The rollers are set at less than ten minutes of arc from perpendicular to minimize edge stresses on the tape. High edge stresses are one of the major causes of tape damage and subsequent loss of data. The spring washers on the fixed guides, which help guide the tape, exert a very low edge pressure on the tape, gently persuading the tape to move up against a known reference edge to minimize off-track errors. The tape cleaner has five ceramic blades, each flat on top. The resulting ten edges, two per blade, remove loose oxide and other debris as the tape passes over them. These blades exert a low contact pressure on the tape compared to other tape cleaner designs using sapphire or tungsten carbide blades, which exert a very high contact pressure on the tape.

These low edge and contact pressures are easy on the tape, but they are also easy on the components themselves. The components of the tape path are designed to achieve an 8000-hour tape running life. With the exception of the main casting, these components are modular. Since they are precisely set at the factory, none of the components require any adjustments when they are replaced by service personnel in the field. In comparison, most other half-inch tape drives require the use of specially written tapes and/or special height adjustment tools to replace some of their major tape path components.

One of the major components that requires no adjustment is the head plate assembly. The two fixed guides, the tape cleaner, and the magnetic head are mounted together on this assembly. To obtain the modular, no-adjustment feature, the magnetic write gaps must be aligned to one half minute of arc. This is done by mounting the head on an adjustable tongue integral to the head plate as shown in Fig. 3. A differential screw with a pitch of 288 threads per inch provides the fine mechanical adjustment necessary. The head is mounted on the tongue so that the write and read gaps are centered above the tongue's pivot point. This is done so that the off-track error caused by the skew adjustment is negligible. The full travel of the skew adjustment causes an off-track error of only 60 microinches.

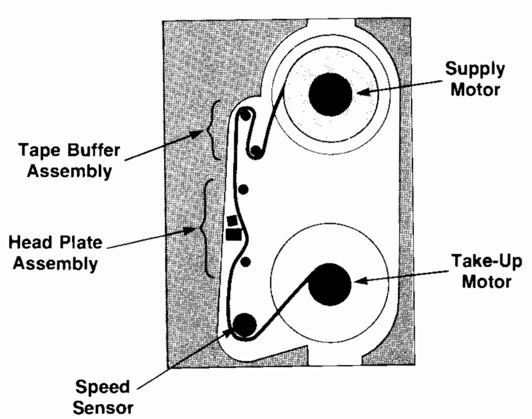


Fig. 2. *Main casting assembly and location of tape-path components for the HP 7978A.*

The magnetic head is ceramic coated to meet the 8000-hour design life. The fixed guide washers are made of alumina ceramic, as is the tape cleaner. This very hard material resists the abrasive action of the tape very well and enables these parts to meet the design life.

The 8000-hour design life also applies to the buffer assembly. The tape is very abrasive on its edges where it is slit to size. Therefore, the roller flanges are chrome plated to reduce wear. In tape drives, one of the major causes of bearing failure is lubricant washout caused by the liberal use of tape-drive cleaning solutions. The rollers on the buffer assembly use shielded bearings and plastic caps to prevent cleaning solutions from washing out their lubrication.

The buffer assembly is an important part of the tape servo system. It maintains the tape tension and helps buffer the servo from any major tape movement to which the tape servo can't respond. Therefore, the servo requirements played a major role in the design of the buffer assembly. The amount of tape buffering was increased several times and the effective mass of the tension arm was reduced to enable the tape servo to function well.

The buffer assembly uses a differential optical sensor, which uses a slotted mask over two phototransistors. The optical sensor gives absolute position feedback to the tape servo telling the location of the buffer assembly arm.

The tape servo also influenced the speed sensor design. The speed roller diameter was optimized to minimize the effective inertia on the tape. This also helps reduce the chance of the tape's slipping on the roller during high tape accelerations. The roller is grooved to prevent tape slippage by allowing air to escape from between the tape and the roller. The sensor itself is an HP one-thousand-line optical encoder. The roller is made of hard-anodized aluminum and is designed to last 8000 hours.

During development of the HP 7978A, a very interesting tape vibration problem occurred. It was a high-pitched squeaking sound, which occurred while the tape was running. The sound could be turned off by pushing the lower fixed-guide spring washer away from the tape. The tape and the washer were acting as a spring mass system. If the spring-mass-system resonant frequency was close enough to the longitudinal resonant frequency of the tape, a squeak would result. The longitudinal resonant frequency of the tape is determined by the length of tape between the rollers on the buffer arm and the speed sensor.

Once this was understood, the problem was solved by changing the two resonant frequencies so that they were farther apart and wouldn't couple into each other. Changing the longitudinal resonant frequency by changing the distance between the rollers was undesirable in terms of design time, skew, and the need to minimize the solution's impact on the other components. The mass of the washer was therefore increased, reducing the spring mass resonant frequency substantially below the longitudinal resonant frequency of the tape span.

Servo

The HP 7978A's servo system is responsible for all tape handling and motion control across the read/write heads. A major design criterion was to provide this motion control at a constant tape velocity with minimum speed or tension perturbation error. Since the servo system is a major electrical-to-mechanical interface, another focal point in the development effort was to provide high reliability and reduced service costs. HP's earlier half-inch tape drives (the HP 7970 and HP 7676) had start/stop servos. This means that they stopped between accessing records on the tape. All the accelerating and decelerating had to take place within the gaps between records on the tape. Since gaps can get as small as 0.28 inch (0.71 cm), the tape had to be accelerated very quickly. The reel motors could not provide enough acceleration, so a capstan motor was used. It had to be isolated from the large inertias of the reels to accelerate so quickly. This isolation was provided by large buffer arms or vacuum columns. They allowed the tape over the head to be accelerated quickly by the capstan motor, while the reels followed a slower acceleration profile.

The HP 7978A, on the other hand, is a streaming tape drive. That is, it is capable only of much lower accelerations and therefore tries to avoid stopping. The reduced acceleration requirements allow the servo to be greatly simplified. In the HP 7978A, the reel motors provide the necessary acceleration, so an inexpensive position encoder has virtually replaced the capstan motor and its drive electronics. One of the buffer arms has been eliminated also. This simplification contributes greatly to the reliability and reduced costs of the HP 7978A. Since starting and stopping are minimized, the acceleration duty cycle is greatly reduced. This reduces stress and strain on the tape, mechanics, and electronics, which contributes to improved reliability and reduced service costs.

Servo Design

The tape handling system is made up of two servo systems: the velocity servo and the tension servo. Regardless of the specific tape motion operation, the velocity servo maintains the required steady-state tape speed to within a $\pm 1.5\%$ tolerance and the tension servo simultaneously maintains an absolute tape tension of 10 oz ± 2.6 oz. Servo system isolation is stressed in the design by having the velocity servo control only the take-up reel, and the tension servo control only the supply reel. Hence, the two servos are physically connected only by the tape.

A good way to understand how these two servo systems work together is to view the velocity servo as the master servo and the tension servo as its slave. For example, the master velocity servo is fed a velocity profile input to follow, which will accelerate the tape up to a specific speed and then maintain this speed thereafter. While the master

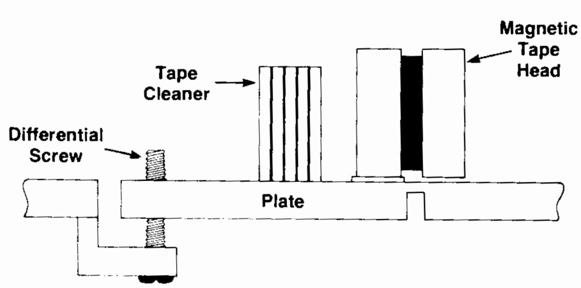


Fig. 3. *Magnetic recording head plate assembly. Skew is adjusted by turning the very-fine-pitch differential screw.*

servo is following its new velocity profile input, the tension servo, which knows nothing of tape speed profiles, sees a perturbation error in its own control system—a tension error. The slave tension servo then attempts to reduce this tension error, and in so doing, it effectively forces the tape speed of the supply reel, which it controls, to match exactly the tape speed of the take-up reel, which the master servo controls.

The velocity servo is a Type I control system which uses integral-plus-proportional control action. It is primarily a digitally controlled servo system implemented using a digital position encoder, an 8051 microprocessor, a digital-to-analog converter (DAC), a motor drive amplifier, and the take-up reel motor (see Fig. 4). The position encoder increments or decrements a counter in response to tape motion. The counter is read by the processor at precise, fixed time intervals to determine the speed. The processor performs the necessary control calculations and outputs a voltage to the motor drive board via the DAC. This voltage is amplified and applied to the appropriate speed-controlling motor, the take-up motor, which then moves the tape onto the take-up reel past the speed encoder, thus completing the speed control loop.

The tension servo is also a Type I control system which uses series lead compensation as well as feedforward control action. It is primarily an analog control system consisting of a buffer arm assembly, a motor drive amplifier, and the supply reel motor (see Fig. 4). The intelligence for this servo resides in the buffer assembly, which senses the actual buffer arm position using a differential optical sensor and provides the appropriate servo lead compensation. The output of the buffer assembly is summed with the D-to-A converter output of the velocity servo to achieve feedforward control action. This result is sent to the motor drive board where it is amplified and applied to the buffer-arm control motor, the supply reel motor. This motor moves the buffer arm via the tape on the supply reel, thus completing the tension control loop.

The tension servo is virtually transparent and yet entirely subservient to the velocity servo. It is transparent to the velocity servo in that it presents a relatively large mechanical impedance to the velocity servo system, which produces little perturbation in the velocity servo's frequency transfer function response. It is subservient to the velocity servo in that the controlling input to the tension servo is the velocity servo's controlled output, the speed of the tape.

The HP 7978A servo system was designed using localized feedback compensation techniques. This can be looked upon as a decentralized-intelligence system design. The velocity servo knows virtually nothing of the tension servo and sees it only as a relatively high and virtually nonexistent mechanical load impedance. The tension servo knows nothing of the velocity servo, but merely tries to maintain its buffer arm near its set location, regardless of the disturbances existing outside its own control loop. While the tension servo is maintaining this buffer arm position, it is the specially designed spring mechanism in the buffer arm that actually controls the tape tension. The reel motors are driven directly by voltage amplifiers, which make direct use of the motors' own individual back-EMF properties. This yields a useful velocity feedback compensating drive scheme.

The HP 7978A servo system maintains its tension and velocity within specification over a great range of different conditions. Tape reel sizes and pack radii can vary over a large range, but since neither detection of reel sizes nor the knowledge of tape pack radii on the reels is needed, the design's simplicity is maintained.

Starting and Stopping

The simplicity afforded by making the HP 7978A a streaming tape drive instead of a start/stop drive is not without price. Such simple actions as starting and stopping the tape lose their simplicity and become more of a technical challenge.

Stopping and then starting the tape within the distance of an interrecord gap is impossible in the HP 7978A because of its slower accelerations. It moves 4.3 inches of tape over the head just to bring the tape to a stop. Even though it must leave the gap to stop and start, it must be able to return to the gap at full speed to resume reading or writing where it left off. The HP 7978A performs this "repositioning" using the velocity encoder and its counter as an odometer. This same odometer setup is used when a record is retried. In that case, the HP 7978A needs to return the tape to the previous gap so that it can retry reading or writing.

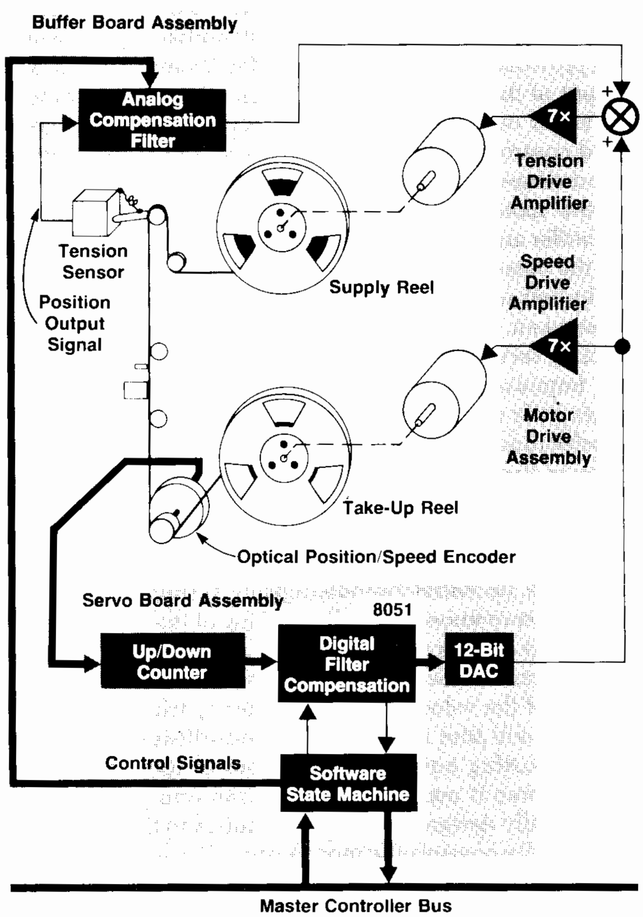


Fig. 4. *Diagram of HP 7978A servo system.*

One difficulty that emerges is caused by tape stretching. The tape tension at the buffer arm is fairly constant over its entire range of travel. But when the tape is moving, its tension at the velocity encoder changes because of the friction of the tape against the head assembly. When the tape is moving forward, the frictional drag *increases* the tension at the speed encoder. However, when the tape is moving in reverse, the frictional drag *decreases* the tension at the encoder. So the tape stretches more and becomes longer when traveling in reverse than when traveling forward. This introduces a cumulative error in the encoder-based odometer. Thus, when the odometer says that the correct gap is over the head, it is actually a small distance in front of it. This makes the preceding block move slightly closer to the head each time it is retried. To ensure that the HP 7978A is in the correct gap, the HP 7978A detects whether the preceding block is over the head when the odometer says that the gap should be. If it is, the odometer is updated to match the new position of the gap. This zeros out the accumulated errors from previous retries.

Gentle Tape Handling

The reliability of the data is another important concern in the HP 7978A design. The servo is designed to minimize the risk of damaging the data on the tape. This is helped by a very smooth loading process. When the tape tension is being established, the error signal in the speed control loop is forced to zero, so that when the loop is activated, the tape will not be jerked. The buffer-arm control loop is also activated at the point where it will jerk the tape the least. In addition, the loading process is somewhat tolerant of incorrectly threaded tapes. Small mistakes in loading the tape around the tape path will rarely result in any tape damage.

In the event something causes the servo to lose control (e.g., a hardware failure or loss of power), the servo is shut down using passive electrical components that sink energy from the motors in such a way as to protect the tape from bunching up or stretching. The user is also protected from injury in the event of a hardware failure. If the door should be opened while the motors are still turning (made possible only by a hardware failure), a safety shutdown mechanism implemented redundantly in both software and hardware forces the motors to stop.

Diagnostics and Confidence Tests

Key contributors to the reduced service costs of the HP 7978A are the diagnostics and confidence tests. They provide very good checking of the mechanism and electronics. The digital portion of the servo electronics is able to diagnose its own problems very well. This includes the 8051 processor and its system of chips, the state machines and I/O electronics, and the DAC and comparators.

Some of the servo's hardware, however, can only be tested with a user's help. Extensive confidence tests were therefore implemented. The BOT (beginning-of-tape) and EOT (end-of-tape) sensors, which are part of the servo hardware set, can be tested by selecting a confidence test that displays their status at the front panel. As a reflective surface is waved in front of them, the display shows whether or not they see the surface. Another test allows the speed encoder to be checked by displaying a count that increases as the encoder is rotated clockwise and decreases as it is rotated counterclockwise. The user can also test the buffer arm by moving it through its range. The front panel displays whether it is over or under tension, when it crosses through zero, and whether or not its optical sensor is operating properly. A failure is indicated by the numbers in the display not going through the proper sequence. The motor driver also has a confidence test. As the user steps through the different parts of the test, the motors are moved in various ways, exercising the basic capabilities of the motor drive amplifiers. With this test, a failure is indicated if the motors do not move properly.

Acknowledgments

Among those who played a major part in the hardware design of the HP 7978A were Kevin Wilson and Bob Gilbert, master controller design, Alfred Natrasevschi, HP-IB interface design, Peter Way and Bob Emmerich, servo design, and Martha Chavez-Simmons, motor drive board design. Gordon Thayer was responsible for a major part of the GCR VLSI design, along with Mike Tremblay, Bob Sobol, Jeff Osborne, and Rick Turley. Gene Briles designed a large part of the read circuitry. The phase-locked loop was designed and debugged by Jeff Kato and Tom Holmquist.

The tape buffer arm assembly and the speed sensor assembly were designed by Dave Sims and Dave Jarrett, respectively. Dave Jarrett also designed the hubs and the door. The industrial design was done by Jim Dow. Doug Domel and Dave Jones did the product design. Dave Jones also designed the aluminum base plate casting. Mel Crane was a great help in solving many of the mechanical problems that arose during the development of the HP 7978A.

Thanks to John Meredith, Tom Bendon, Alan Richards, Gordon Thayer, and Rick Turley for managing the later stages of the program in getting the product from the lab into production.

Many thanks also to Rex James for helping manage the program through to the end.

Firmware for a Streaming Tape Drive

by David W. Ruska, Virgil K. Russon, Bradfred W. Culp, Alan J. Richards, and John A. Ruf

THE MASTER CONTROLLER FIRMWARE of the HP 7978A Magnetic Tape Subsystem is responsible for the highest level of control. This firmware handles all interactions with the host system and the operator and oversees the execution of both the operational and the diagnostic functions of this half-inch tape drive.

The host system sends commands to the tape drive over the Hewlett-Packard Interface Bus (HP-IB, IEEE 488). The master controller firmware must receive and execute these commands and then respond with the appropriate results. In the execution of commands, the firmware will set up the tape drive's hardware subsystem and then detect either successful completion or an error condition. When an error occurs, the master controller firmware will process recovery procedures, retrying the operation if possible.

The operator interacts with the HP 7978A through the front panel. The master controller firmware receives the requests from the front-panel buttons, executes them, and updates the front-panel displays.

An important responsibility of the firmware is validating the fitness of the tape drive's hardware. If a failure is detected, the firmware will aid service personnel in the diagnosis of the problem.

Architecture

The architecture of the master controller firmware was designed using the principle of functional decomposition. The firmware contains three main subsystems: the channel program, the device program, and the diagnostic program. Each of these programs performs a specific function within the tape drive. These programs use a command/report transactional communications scheme when interacting with each other. This architecture exhibits strong functional binding within the subsystems and a minimal amount of coupling between subsystems.

To facilitate maximum tape drive use, the master controller firmware supports queued operations. This is made possible by concurrent execution of the channel and device programs along with internal queues for commands and reports (Fig. 1). Through the use of read aheads when reading and "immediate responses" when writing, the tape can be kept streaming without the need of a complex queuing protocol with the host.

Channel Program

The channel program is responsibile for processing all user interactions with the drive, that is, interface requests over the HP-IB from the host and front-panel requests from the operator. These requests generate command sequences which are sent to the device program for execution.

Streaming tape mechanisms require either a constant supply of data from the host or a constant acceptance of data by the host to maintain streaming. Otherwise, the mechanism must perform a tape reposition cycle whenever the data stream is interrupted.

There are two methods for smoothing data transfers with the host to help maintain streaming. Data can be buffered either within the host or within the tape drive. Buffering data in the host requires memory resources and the ability to queue requests to the I/O driver. Buffering data within the tape drive frees the host from any special requirements to support a streaming drive. This buffering is also more advantageous, because it allows the drive to monitor the amount of used and unused buffer space. While writing, this capability lets the drive perform write holdoffs as necessary to extend streaming. When reading, the drive's data buffer allows the device to perform read aheads, anticipating the following host read requests.

Along with the data buffer, the channel program maintains command and report queues within the tape drive to monitor the placement of data within the buffer. These queues are also used to allow file marks and motion commands to be queued to the device by the channel program. Buffering and command queuing are transparent to the host system.

To allow data records to be queued in the buffer during writes, a new feature was added to the interface protocol. This feature is called "immediate response." Data sent from the host is stored in the drive's buffer and a command is placed in the command queue. An immediate report is sent to the host indicating that the data has been accepted. The host is then free to gather and send more data to the drive.

Data sent to the host system that was read off the tape is also stored in the drive's data buffer. Upon completing a requested read command from the host, the HP 7978A continues reading additional data records into the data buffer. This read-ahead operation continues until the data buffer becomes filled, the end of the tape is reached, or an error condition is encountered. In parallel with this read-ahead operation, the HP 7978A can continue to accept read commands from the host and fulfill them immediately with data records already stored in the buffer. Only when the host lags the tape drive to the point where the data buffer becomes full will the drive need to perform a reposition cycle.

The HP-IB interface protocol is a modification of the protocol used with the earlier HP 7976A tape drive. The HP 7976A allows command queuing of two read or two write operations. This allows an overlap of transfers between the host and the HP 7976A's buffer, and between the buffer and the tape. This queueing has to be performed explicitly by the host. To use this feature usually implies rewriting applications programs. The HP 7978A does not support queuing in its protocol. Instead, immediate response and read-ahead functions are used to make the streaming tape drive perform like a start/stop drive.

Device Program

The functionality of a streaming tape transport mechanism can be maximized if the transport is allowed to run independent of outside timing constraints, and if it can implement intelligent algorithms for control under all situations. The device program provides this type of control.

All control of the tape mechanism and read/write electronics during normal operation is performed by the device program. As requests are received from the host or operator interface, they are placed into the queues by the channel program for the device program to act upon. The device program executes each of the commands, formats and returns a report to the channel program, and then goes on to the next command. The device program processes each command completely, including all exceptions.

A wide variety of recording errors and exceptions can occur during the processing of a host transaction. The ability to perform the proper recovery from errors automatically without burdening the host with unnecessary information and responsibility is built into the intelligent device program. Recording errors caused by such things as tape imperfections or debris in the tape path are recovered by the execution modules performing automatic retries.

Write retries involve repositioning the tape back before the record that was recorded with errors, erasing that portion of tape, and then skipping the next section of tape to attempt the write again. The data for the record is maintained intact in the data buffer until the record has been successfully written so that the host does not need to retransmit the information.

When a record is not read successfully on the first attempt, read retries are performed by repositioning the tape back before the record and reading it again with the read signal amplified. Retries for reads and writes occur until the transaction is successful or a maximum limit occurs, resulting in a hard error.

Different host and streaming tape data rates require that there be a decoupling of the two rates if high performance is to be maintained. In the HP 7978A, the decoupling is provided by queuing, data buffering, and a device program that runs independently. The channel program runs in sync with the host, handles the bursting needs of the interface, and queues them for the device program, which in turn runs in sync with the needs of the tape mechanism. The device program's only interaction with the channel program is at the beginning and end of each block of data, when it reports on one request and accepts a new one.

By running the device program in sync with the tape drive, the high-performance features of the HP 7978A can be implemented. Read aheads are performed by the device program's independently reading records in anticipation

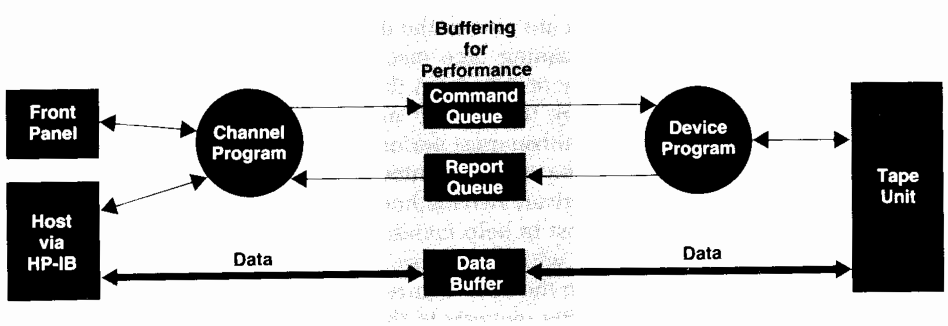


Fig. 1. *The firmware of the HP 7978A Magnetic Tape Subsystem contains three main modules: channel program, device program, and diagnostic program (not shown).*

of the host's needs. The only interaction required is for the channel program to indicate when conditions are right for the host to desire read records. During writes, it is the implementation of immediate response that gives the drive its high performance. However, when the channel program is operating in immediate response mode, a report has already been sent to the host, leaving the device program free to write buffered data in the most convenient way. The device program holds off writing the data until a sufficient amount of data has been placed in the buffer or until a moderate timeout period occurs. This write holdoff groups write operations together and avoids an appearance of thrashing the tape back and forth.

Diagnostics

Diagnostics in the HP 7978A are split between the read/write functional electronics and the servo electronics. A 68000 microprocessor controls the read/write circuitry while a parallel 8051 processor controls the servo system. The 8051 accepts motion/diagnostic commands from the 68000 and returns status.

The 68000-based diagnostics verify the hardware operations of the HP-IB, data buffering and manipulation, and the read/write circuitry. The 8051-based diagnostics verify the servo hardware: buffer tension arm, speed encoder, motors, and servo control board.

The goal throughout the HP 7978A's diagnostics is to locate a failure to the board level. Once a failure is located, no further attempt is made to uncover any other failures. By testing from a core of independent hardware outward to the increasingly dependent hardware, the number of failures recorded without specific causes is minimized.

Approximately 75% of the drive is tested at power-on. The remaining 25% of the drive can be tested using the diagnostic tape tests or through normal operation. Any drive failure that is discovered is encoded into the host command report status and the internal diagnostic error log.

The HP 7978A has 62 diagnostic functions. Sixteen of these functions are performed during power-on self-test. The diagnostic functions can be categorized as follows: 12 utility/environment setting functions, 16 servo system tests, 15 board-level tests for the read/write functional electronics, 10 tape exercising functions, and 9 special functions of the HP 7978A. The utility/environment functions allow front-panel access to internal drive information and set the diagnostic test environments.

The servo system and read/write functional tests are designed to exercise a board or major subassembly. Examples of these tests include injecting signals into a circuit and verifying the outputs, or performing data loopbacks along the functional data paths.

The tape exercising functions allow reading and writing data from and to tape.

The nine special functions are: host-to-drive data loopback, remote download diagnostics, local and remote firmware update, image dumps of RAM and EEPROM, programmatically adjusting the read gain values, monitoring the amount of tape traveling over the read/write head, and an excessive soft-error rate function.

Execution of the HP 7978A's diagnostics is quite simple. A diagnostic test can be requested from the drive's front panel or through an HP-IB command from a host computer. Most diagnostics can be executed from either interface. However, some diagnostic tests require that special conditions be met before execution and some simply are not available from both interfaces. For example, the power-on self-test can be accessed remotely through a host or locally by an operator. Although the power-on self-test can be accessed remotely, the tape drive must be off-line for the test to be executed. If the drive is on-line, an error message is returned indicating the reason for nonexecution.

Acknowledgments

The authors acknowledge the efforts of other members of the firmware design team. The device program was written in part by Bruce Thompson, Dave Ellis, and Dave Burton. Diagnostics were written in part by Kevin Wilson and Dave Van Maren (servo diagnostics). Thanks also to Dave Jarrett, Doug Domel, and Alfred Natrasevschi, who helped with the firmware QA effort.

Authors

March 1985

4 Maintenance Management

Irving Bunton, Jr.

Irv Bunton is a native of Chicago, Illinois and a graduate of the University of California at Berkeley (BSCS 1983). He joined HP's Manufacturing Productivity Division in 1983 and has contributed to the development of HP Maintenance Management. He is a resident of Oakland, California and enjoys music, especially jazz and blues.

Joseph L. Malin

A native of Washington, D.C., Joe Malin earned a BS degree in chemistry from Haverford College in 1978. He also did graduate work at the University of Pennsylvania. At HP since 1982, he worked on HP Maintenance Management and now develops manufacturing management software for the HP 3000 system. Joe's professional interests include manufacturing systems design and software engineering techniques. He also teaches Pascal programming at a local college. Now a resident of Cupertino, California, he enjoys skiing, drawing cartoons, and bicycling.

11 Half-Inch Tape Drive

Hoyle L. Curtis

Hoyle Curtis was born in Petersburg, Texas and attended Texas Tech University (BSME 1971 and MSME 1972). After joining HP in 1973 he contributed to the development of the HP 9871A Printer, was an R&D project manager for several printer projects and for the HP 9895A Disc Drive, and was both an R&D project manager and section manager for the HP 7978A. Now a resident of Fort Collins, Colorado, he likes aquatic sports including sailing, windsurfing, and scuba diving. He participated in the Hobie 18 National Championships for sailing.

Richard T. Turley

With HP since 1977, Rick Turley managed the HP 7978A Tape Drive project and also contributed to the electronic design for the unit. Earlier, he was both a development and a production engineer for the HP 9876A Printer. Rick was born in Cranford, New Jersey and graduated from Case Western Reserve University in 1977 with undergraduate degrees in both electrical engineering and mathematics. He continued his education at Colorado State University, from which he received an MSCS degree in 1981. He also attended Stanford University as an HP fellow in 1984 and received an MSEE degree. He lives in Fort Collins, Colorado with his wife and young son and enjoys hiking and cross-country skiing.

16 Write and Read Recovery Systems

Wayne T. Gregory

Tom Gregory joined HP's Civil Engineering Division in 1979 and was the responsible production engineer for the HP 3805, 3808, and 3810 distance and angle meters. After transferring to the Greeley Division, he contributed to the analog electronic design of the HP 7978A. Tom was born in Oceanside, California and now lives in Loveland, Colorado with his wife. In his spare time he enjoys backpacking, chess, and skiing.

19 Digital Formatting

Jimmy L. Shafer

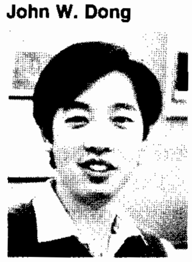
Jim Shafer was born in Shreveport, Louisiana, and attended Louisiana Technical University, from which he received a BSEE degree in 1981. He joined HP in the same year and was responsible for several aspects of the electronic design of the HP 7978A. He also had production engineering responsibilities after the product was introduced. Most recently he has worked on VLSI design for hard disc drives. Jim lives with his wife and new baby in Greeley, Colorado. His interests include skiing, softball, hiking, hunting, fishing, and camping.

25 Tape Drive Hardware

Robert D. Emmerich

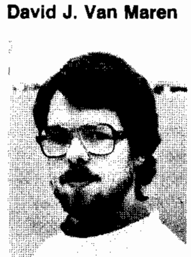
Currently lead engineer for the Greeley Division technical analysis lab, Robert "Diamond Bob" Emmerich has been with HP since 1976. His contributions include work on the HP 250 Computer, NMOS II process control and IC testing, quality testing for the HP 9895A Disc Drive, and evaluation of wear on flexible disc media. A native of Colorado, Bob was born in Denver, was educated at the University of Colorado (BSEE 1976), and is a resident of Loveland. He says he spends his spare time "reconstructing electronic hulks."

John W. Dong



John Dong was born in Phoenix, Arizona and educated at the Massachusetts Institute of Technology, from which he received the degrees of BSME (1975) and MSME (1976). With HP since 1976, he was the product designer for the HP 9876A Printer, a production engineer for the HP 9825 and 9815 Computers, and a mechanical designer for the HP 7978A. John's work on the head plate assembly for the 7978A has resulted in a patent application. He is a registered professional engineer in the state of Colorado and a resident of Fort Collins. When he is not working on the basement of his house, he enjoys skiing and hiking.

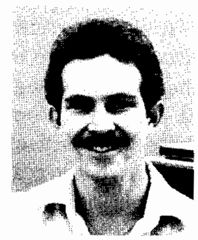
David J. Van Maren



Dave Van Maren has been with HP since 1980, the same year he was awarded a BSEE degree from the University of Wyoming. He first worked in the Vancouver Division on the HP 293X Printers and then was a production engineer in the Greeley Division. He was responsible for the servo controller firmware for the HP 7978A. Dave is a native of Casper, Wyoming and presently lives with his wife and two sons in Fort Collins, Colorado. He is a member of Right to Life and both he and his wife are instructors in natural family planning methods.

29 Tape Drive Firmware

David W. Ruska



A native of Detroit, Michigan, Dave Ruska attended Michigan Technological University, from which he received a BSEE degree in 1982. After coming to HP in the same year, he was responsible for channel program and HP-IB interface specifications for the HP 7978A and 7974A Tape Drives. Dave is a resident of Greeley, Colorado and has many outside interests. He raises Arabian horses, plays the piano, and is currently designing a digital music synthesizer. He also makes stained glass windows and enjoys photography and bicycling.

Bradfred W. Culp

Born in Ogden, Utah, Brad Culp received a BSEE degree from Virginia Polytechnic Institute in 1978 and joined HP in the same year. He resumed his studies in 1984 through the HP resident fellowship program and recently earned an MSEE degree from the University of Illinois. At HP, he has contributed to the development of an inkjet printer as well as the HP 7978A. Brad is a resident of Fort Collins, Colorado and enjoys hiking, bicycling, and skiing.

Virgil K. Russon

Virgil Russon was educated at Brigham Young University, from which he received BSME and MSME degrees in the same year (1979). At HP since 1981, he worked on the buffer assembly and firmware for the HP 7978A Tape Drive. Virgil was born in Lehi, Utah and now lives in Greeley, Colorado with his wife and four children. He is active in his church and works on numerous home projects. He also enjoys woodworking and art.

John A. Ruf

A native of Milwaukee, Wisconsin, John Ruf served for four years in the U.S. Air Force before receiving a BSCS degree from the University of Wisconsin at La Crosse (1981). A short time later he joined HP's Greeley Division, where he has worked as a software engineer on the 7978A Tape Drive. John lives with his wife and two sons in Fort Collins, Colorado. He enjoys tennis, jogging, and developing software design aids.

Alan J. Richards

Now R&D manager for Colorado Time Systems in Loveland, Colorado, Alan Richards came to HP in 1968. He was a project leader or manager on the HP 9825A Tape System, the HP 9874A Graphics Digitizer, and the HP 7978A. In addition, he was a production engineering manager for the Greeley Division and HP's campus recruiting manager at Kansas State University. Alan lives in Loveland, Colorado, is married, and has two children. He likes hiking, backpacking, orienteering, and cross-country skiing. Last summer he realized a lifelong ambition by taking his family on an extended vacation to Alaska.

34 Winchester Backup

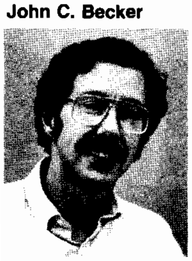
Sterling J. Mortensen

Sterling Mortensen received his BSEE degree from Brigham Young University in 1974 and came to HP in the same year. As a design engineer, production engineer and a project manager, he has contributed to the hardware and software design of the HP 250 Computer and the HP 9895 and HP 82901 Disc Drives. He was the software architect for the HP 9144A. He was born in Rexburg, Idaho, lives in Fort Collins, Colorado, is married and has twin sons as well as two other children. His interests include target shooting, photography, and church activities.

Donald A. DiTommaso

Currently manager of a new product development program at HP Laboratories in Bristol, England, Don DiTommaso was program manager for the HP 9144A. He also originated the idea for the project, managed design work on the 9144A drive mechanism, and contributed to controller design. Don is an alumnus of the University of Cincinnati (BSEE 1973) and the University of Colorado (MSEE 1975) and came to HP in 1975. He first worked on the design for HP 9845 Computers and later set up an R&D laboratory team in HP's Singapore Operation. He is also named as a coinventor on a patent on the design of the HP 9144A read after write technique.

John C. Becker



Now project manager for the HP 9144A, John Becker has been with HP since 1964. He also managed the development effort for the 9144A drive mechanism. Earlier, he managed a production engineering group and contributed to the development of the HP 9835 and 9825 Computers. He is named coinventor on a reed relay patent and is an author of papers published by the IEEE and the HP Journal. Born in Lincoln, Nebraska, John received his BSEE and MSEE degrees from Colorado State University in 1972 and 1974. He currently resides in Loveland, Colorado, is married, and has four children. His outside pursuits include tennis, jogging, sailing, church activities, and travel.

37 Tape/Disc Controller

Mark L. Gembarowski

Author's biography appears elsewhere in this section.

Craig L. Miller

A native of Sandy, Utah, Craig Miller attended Brigham Young University (BSEE and MSEE, both 1976) and joined HP in 1977. He was a hardware designer for the HP 9144A as well as for the HP 250 Computer and the HP 9895A Disc Drive. At present, he is working on the design of a mass storage controller. Craig is married, has five children, and lives in Fort Collins, Colorado. His interests include softball, volleyball, basketball, church activities, and travel. He also coaches for an elementary school soccer league.

39 Tape Data Integrity

K. Douglas Gennetten

Doug Gennetten came to HP in 1978 and has worked on the HP 9144A controller and mechanism, as well as on high-speed dynamic RAM test hardware and fault detection algorithms. He received his BSEE from Walla Walla College in 1978 and is continuing graduate level study at Colorado State University and at National Technical University. Doug lives in Fort Collins, Colorado and is married. His outside interests include skiing, sailing, hiking, woodworking, visual arts, and exploring the back country by jeep.

44 Head/Tape Interface

Mark E. Wanger

Mark Wanger joined HP in 1980 with a background in satellite control systems. He worked first as a production engineer, and then became an R&D engineer and contributed to tape path control and hardware design for the HP 9144A. A native of Long Beach, California, Mark studied at the University of California at Santa Barbara (BSME 1979), the Massachusetts Institute of Technology (MSME 1980), and Colorado State University (MSEE 1983). He lives in Fort Collins, is married, and enjoys backpacking, basketball, and sailing.

David J. Schmeling

Dave Schmeling has worked on the HP 9144A Tape Drive since coming to HP in 1979. He contributed to the mechanical design, environmental testing, and production of the product. Dave was born in Santa Ana, California and graduated from Stanford University with an MSME degree in 1979. He lives in Fort Collins, Colorado and is newly married. His outside interests include Bible study, skiing, woodworking, and finishing the basement of his home.

Walter L. Auyer

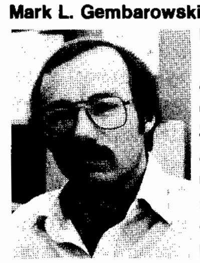
A native of central New York State, Walt Auyer joined HP in 1971 and has worked as an R&D laboratory engineer in both the Civil Engineering Division and the Greeley Division. He received an MSME degree from Arizona State University in 1969. Before coming to HP, he was employed in the aerospace industry. Walt lives in Fort Collins, Colorado, is married, and has four children. He enjoys golf, bridge, and vacation travel with his family.

Charles H. McConica

A native of Ventura, California, Chuck McConica is an alumnus of the University of Denver (BSME 1974 and MBA 1976). He also studied at Stanford University, where he received an MSAM in 1975 and is presently a PhD candidate in mechanical engineering. Since joining HP in 1979, Chuck has contributed to the development of inkjet head technologies and the manufacturing process for flexible disc heads and magnetic tape head mounting. His work has resulted in a patent on inkjet multiple-drop suppression. Chuck is a resident of Windsor, Colorado, is married, and has two children. His interests include family activities, backpacking, skiing, bicycle touring, and sports cars. He also serves as a soccer coach and helps local high school math and science teachers with lecture material.

47 Software Methodology

Mark L. Gembarowski



Mark Gembarowski joined HP in 1978 after receiving an electrical engineering degree from Michigan State University. In his first assignments, he contributed to the hardware design of the HP 9111A Graphics Tablet. Currently, he is manager for a half-inch tape drive project. A native of Saginaw, Michigan, he now lives in Fort Collins, Colorado and enjoys softball, water and snow skiing, and photography. He also started a Fort Collins youth soccer program in 1979.