HEWLETT PACKARD

HIGH LEVEL DATA LINK (HDLC) INTERFACE FIRMWARE INSTALLATION MANUAL

For Products: HP 12794B
HP 12825A
HP 12007B
HP 12044A

HEWLETT PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition ..... March 1982

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends upon the type of material. Insulators can easily build up static charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields. *The resulting damage can range from complete destruction to latent degradation.* Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The basic concept of static protection for electronic components is the prevention of static build-up where possible and the quick removal of already existing charges. The means by which these charges are removed depend on whether the charged object is a conductor or an insulator. If the charged object is a conductor such as a metal tray or a person's body, grounding it will dissipate the charge. However, if the item to be discharged is an insulator such as a plastic box/tray or a person's clothing, ionized air must be used.

Effective anti-static systems must offer start-to-finish protection for the products that are intended to be protected. This means protection during initial production, in-plant transfer, packaging, shipment, unpacking and *ultimate use.* Methods and materials are in use today that provide this type of protection. The following procedures are recommended:

1. All semiconductor devices should be kept in "antistatic" plastic carriers. Made of transparent plastics coated with a special "antistatic" material which might wear off with excessive use, these inexpensive carriers are designed for short term service and should be discarded after a period of usage. *They should be checked periodically to see if they hold a static charge greater than 500 volts in which case they are rejected or recoated.* A 3M Model 703 static meter or equivalent can be used to measure static voltage, and if needed, carriers (and other non-conductive surfaces) can be recoated with "Staticide" (from Analytical Chemical Laboratory of Elk Grove Village, Ill.) to make them "antistatic."

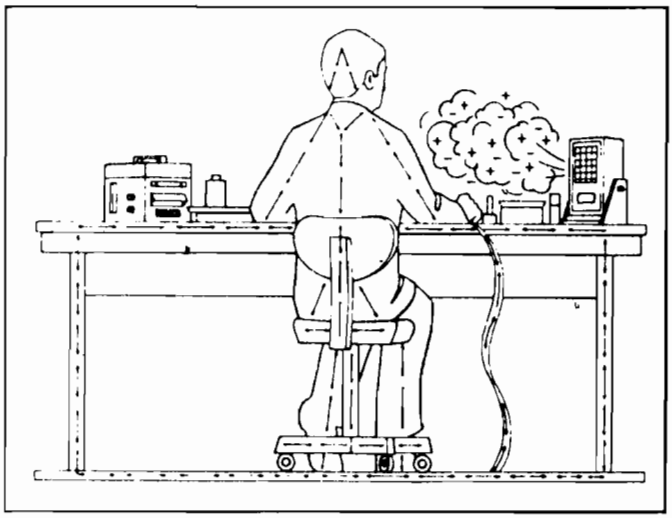
2. Antistatic carriers holding finished devices are stored in transparent static shielding bags made by *3M Company.* Made of a special three-layer material (nickle/polyester/polyethylene) that is "antistatic" inside and highly conductive outside, they provide a Faraday cage-like shielding which protects devices inside. "Antistatic" carriers which contain semiconductor devices should be kept in these shielding bags during storage or in transit.

HP Computer Museum
www.hpmuseum.net

For research and education purposes only.

Individual devices should only be handled in a static safeguarded work station.

3. A typical static safeguarded work station is shown below including grounded conductive table top, wrist strap, and floor mat to discharge conductors as well as ionized air blowers to remove charge from nonconductors (clothes). Chairs should be metallic or made of conductive materials with a grounding strap or conductive rollers.



SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

GLOSSARY OF TERMS

The following terms are defined as they are used in Hewlett-Packard computer product manuals. Some of the terms defined below may not be used in this manual.

ASCII American Standard Code for Information Interchange.

asynchronous transmission No timing signals are sent with the data. Start and stop bits serve to delimit transmitted words.

block A contiguous stream of data words. In BSC protocol, a block is usually referred to as a message.

BSC (Binary Synchronous Communications) Synonymous terms for data communications based on character oriented, half duplex protocol.

buffer A segment of contiguous random-access memory (RAM) locations used for temporary storage of input/output messages.

card The printed circuit assembly (PCA).

CRC-16 (Cyclic Redundancy Check) An error detection scheme used in data communications.

CRC-CCITT (Cyclic Redundancy Check) An error detection scheme defined by the International Telephone and Telegraph Consultive Committee.

DCE Data Circuit-terminating Equipment. In most references, an entry node of the network.

DCPC Dual Channel Port Controller.

DIP (Dual In-line Package) A type of integrated circuit package.

DMA (Direct Memory Access) The transfer of data directly to or from memory.

driver In a hardware sense, a driver refers to a circuit which is capable of supplying specific current and voltage requirements. In a software sense, a driver is a program that is capable of controlling a specific input/output device.

DS (Distributed System) A term used to refer to networks using Hewlett-Packard Distributed Systems hardware and software products.

DTE (Data Terminal Equipment) In most references, the local node which resides outside the network and communicates with the DCE.

EIA Electronics Industries Association.

firmware Software code packaged in read-only memory (ROM).

FCS (Frame Checking Sequence) A 16-bit sequence derived from an algorithm common to DCE and DTE. The sequence is appended to each frame and used as a verification of data transmission.

Flag A LAP-B and HDLC synchronization character with a binary representation of "01111110". Because LAP-B and HDLC require zero insertion after a string of five "1" bits, the flag bit string is unique and cannot be misinterpreted.

Frame A LAP-B and HDLC unit of information exchange, bounded by flags, consisting of an address field, control field, optional data field, FCS field.

full-duplex Communications system or equipment capable of simultaneous two-way data communication.

half-duplex Communications systems or equipment capable of transmission in either direction, but not both directions simultaneously.

handshaking The alternating exchange of predetermined signals between two communicating devices for purposes of control.

HDLC (High Level Data Link Control) Types of protocols which eliminate much of the handshaking and resultant time consuming line turnarounds.

host The computer housing the communication card.

HP-DLC-II (Hewlett-Packard Data Link Control II) A Hewlett-Packard HDLC standard defining the elements and procedures for a balanced, bit oriented, Level-II protocol. HP-DLC-II is compatible with CCITT X.25 LAP-B, and LAP-B implementations by TELENET and TRANSPAC packet switching networks.

I-frame A LAP-B and HDLC unit of information exchange containing a data field.

interface A device providing electrical and mechanical compatibility between two communicating devices.

ISO International Standardization Organization.

k Maximum number of outstanding I-frames: a system parameter (less than eight) defining the most unacknowledged information frames permissible at any given time.

LAP-B (Link Access Protocol-Balanced) A CCITT Recommendation X.25 Level II protocol. LAP-B, a bit oriented protocol, uses the principles and terminology of ISO's HDLC.

LED (Light Emitting Diode) A component used on many printed circuit assemblies to provide a visible indication of desired information.

link Communication interfaces, lines, modems, and other equipment which permit the transmission of information in data format between two or more devices.

modem (modulator-demodulator) Equipment capable of digital-to-analog and analog-to-digital signal conversion for transmission and reception via common carrier telephone lines.

modulus Used by LAP-B and HDLC in the sequential numbering of I-frames; modulus equals eight.

N1 Maximum number of bits in an I-frame; N1 is a system parameter used by LAP-B and HDLC.

N2 Maximum number of (re)transmissions; a LAP-B and HDLC system parameter specifying the number of times the local node will transmit, and retransmit a frame before some recovery procedure is begun.

N(R) Receive sequence number. N(R) denotes the expected sequence number of the next received I-frame (found in LAP-B and HDLC information, receiver ready, receiver not ready, and reject frames).

N(S) Send sequence number. N(S) denotes the sequence number of the transmitted I-frame (found in LAP-B and HDLC information frames).

Octet A sequence of eight bits; a byte.

PCA Printed Circuit Assembly, sometimes referred to as a card.

Primary In LAP-B and HDLC, that logical portion of a DCE or DTE responsible for sending commands and receiving/processing the resulting responses. In BISYNC, a primary is the node which initiated the call.

Primary System A preconfigured operating system included with all HP Computer systems. It can be reconfigured to meet specific system I/O and memory requirements.

Receiver Any device capable of receiving electrically transmitted signals.

SDLC (Synchronous Data Link Control) An IBM High-Level Data Link Control protocol.

Secondary In LAP-B and HDLC, that logical portion of a DCE, or DTE responsible for receiving commands from the remote DTE/DCE, processing these commands, and generating the correct responses. (Each LAP-B or HDLC DCE/DTE is a combined station, composed of both logical primary and secondary functions.) In BISYNC, a secondary is the node which receives a call.

synchronous transmission Timing signals are transmitted with the data. No start and stop bits are used. Defined protocol characters must be used to define message blocks or frames.

system parameter As used in HP manuals, a parameter necessary for DCE/DTE communication; its value is agreed upon before network communication is attempted.

T1 Timer 1. In LAP-B and HDLC, the period of time that elapses while awaiting acknowledgement of an outstanding frame.

T2 Timer 2. In LAP-B and HDLC, the maximum period of time a node will allow without an exchange of frames while the link is logically connected. (T1 excludes T2.)

TELENET A packet switching network owned and operated by GTE.

TRANSPAC The French packet switching network.

V(R) Receive state variable. In LAP-B and HDLC, V(S) denotes the sequence number of the next in-sequence information frame the node expects to receive.

V(S) Send state variable. In LAP-B and HDLC, V(S) denotes the sequence number of the next in-sequence information frame to be transmitted by the node.

CONTENTS

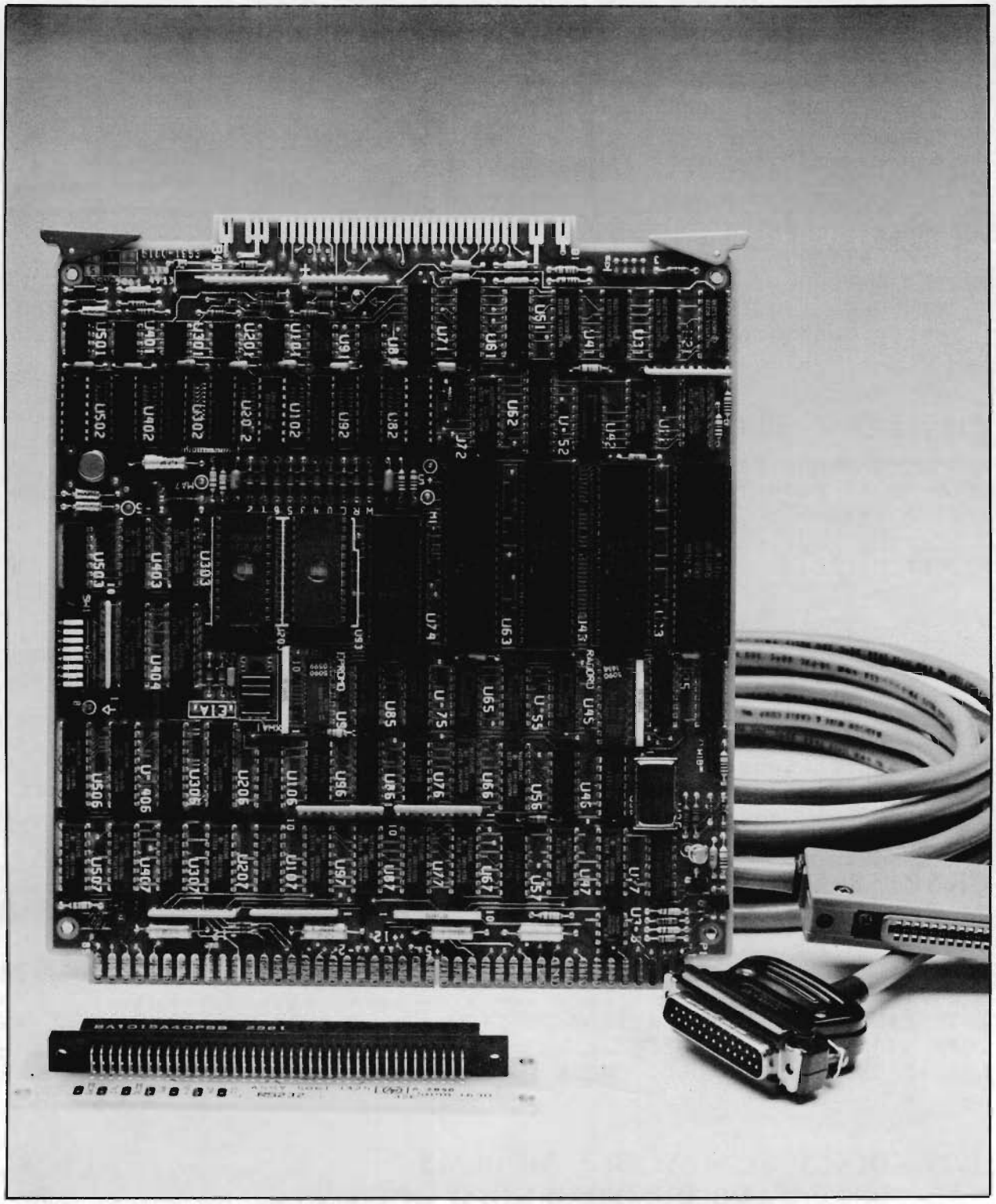


Figure 1-1. HP 12794B HDLC Modem Programmable Serial Interface for M/E/F-Series Computers

CHAPTER 1
GENERAL INFORMATION

DESCRIPTION

This manual provides installation procedures for DS/1000 High Level Data Link Control (HDLC) firmware used in conjunction with the Programmable Serial Interface card assembly, and a description of HDLC Level II protocol. HDLC provides a data link between two HP 1000 computers via modem or hardwire connection. The following table defines the application of the four HDLC products:

PRODUCT	FUNCTION
12044A	L/A-Series direct connecting interface to any HP 1000.
12007B	L/A-Series synchronous modem interface to any HP 1000.
12825A	M/E/F-Series direct connecting interface to any HP 1000.
12794B	M/E/F-Series synchronous modem interface to any HP 1000.

The L/A-Series configurations are used with ID.66 of the HP 91750 DS 1000-IV software. The M/E/F-Series cards are used with DVA66 of the 91750A software package.

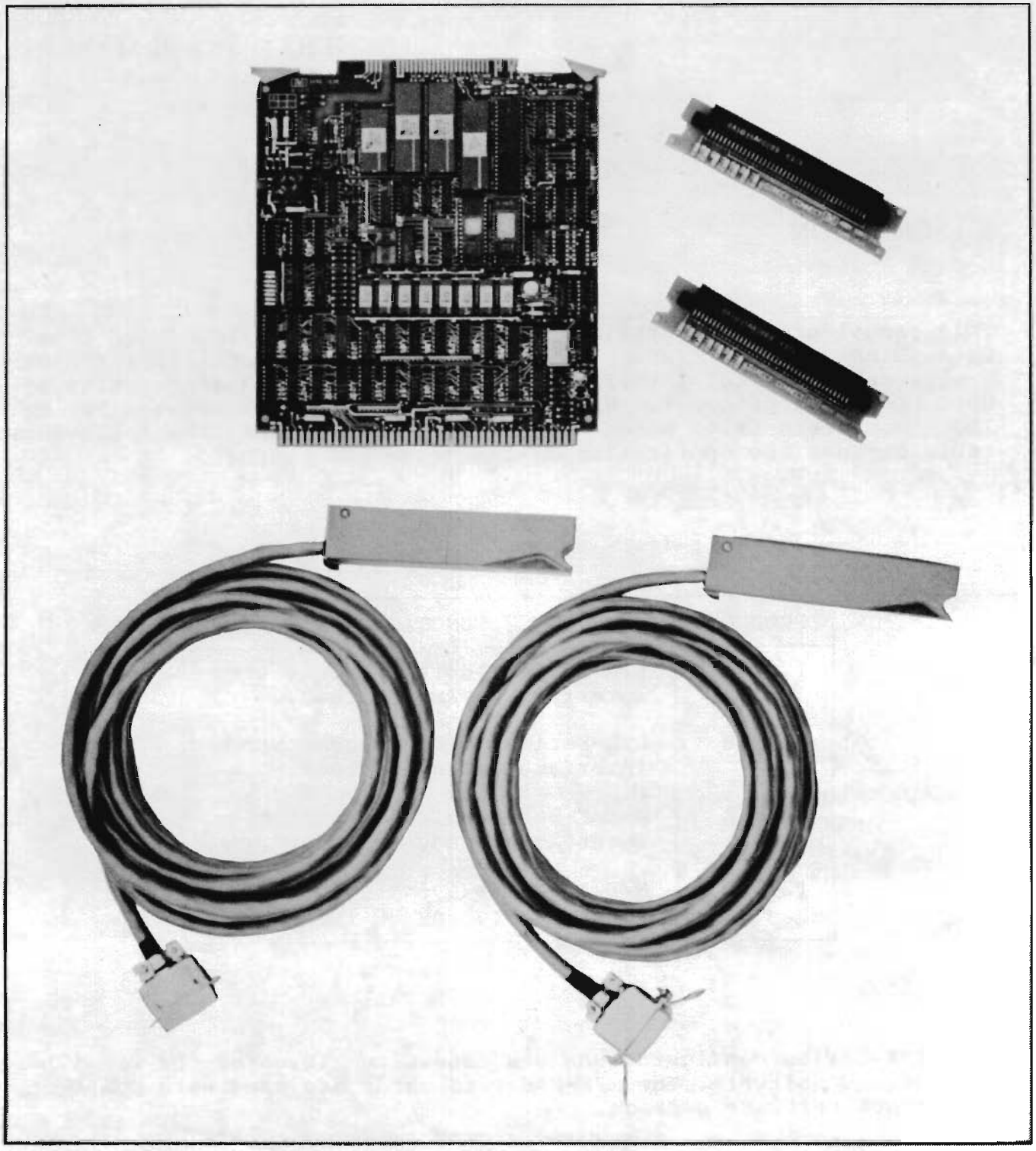


Figure 1-2. HP 12825A HDLC Direct Connect Programmable Serial Interface for M/E/F-Series Computers

EQUIPMENT SUPPLIED

Two HDLC encoded ROMs/EPROMs are installed on each PSI card, HP part numbers 91750-80008 and 91750-80009 and date coded 2040. This manual, HP part number 5955-7626 is supplied with each HDLC product. The product-specific components are listed below:

HP 12794B

The printed circuit assembly, HP part number 5061-4913, with six removable jumpers.

RS-232-C modem interface cable (5 meters, 16.4 feet), HP part number 5061-4914.

Loop-back verifier hood, HP part number 5061-3425.

PSI hardware installation manual, HP part number 12826-91001.

HP 12007A

The printed circuit assembly, HP part number 5061-4912, with six removable jumpers.

RS-232-C modem interface cable (5 meters, 16.4 feet), HP part number 5061-4914.

Loop-back verifier hood, HP part number 5061-3425.

PSI hardware installation manual, HP part number 12042-91001.

HP 12825A

The printed circuit assembly, HP part number 5061-3432, with seven removable jumpers.

One 5 meter (16.4 feet) interface cable with male connector, HP part number 5061-3422. (See Equipment Available.)

One 5 meter (16.4 feet) interface cable with female connector, HP part number 5061-4908. (See Equipment Available.)

Two loop-back verifier hoods, HP part number 5061-3421.

PSI hardware installation manual, HP part number 12042-91002.

HP 12044A

The printed circuit assembly, HP part number 5061-3434, with seven removable jumpers.

One 5 meter (16.4 feet) interface cable with male connector, HP part number 5061-3422. (See Equipment Available.)

One 5 meter (16.4 feet) interface cable with female connector, HP part number 5061-4908. (See Equipment Available.)

Two loop-back verifier hoods, HP part number 5061-3421.

PSI hardware installation manual, HP part number 12042-91002.

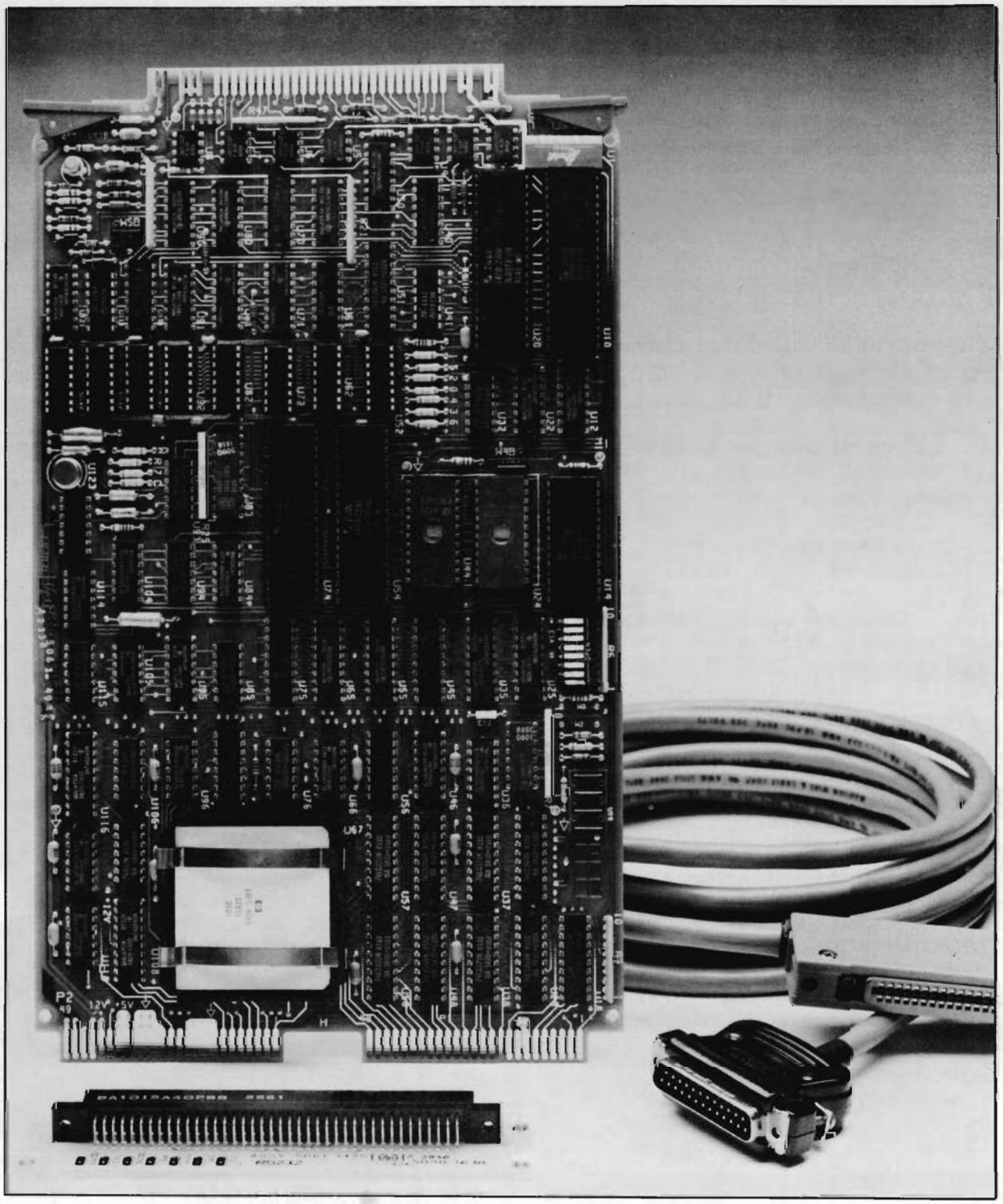


Figure 1-3. HP 12007B HDLC Modem Programmable Serial Interface for L/A-Series Computers

OPTIONS AVAILABLE

Option 001: (All models) Upgrade discount for latest revision of interface firmware. This is available to customers with previously purchased HDLC firmware only.

Option 002: (12794B and 12007A only) Replaces the RS-232 modem interface cable and loop-back hood with an EIA RS-449 interface cable and loop back-hood, HP part numbers 5061-4923 and 5061-4915 (or 5061-3441), respectively.

EQUIPMENT AVAILABLE

Additional cables are available for use with the HDLC direct connect cards (HP 12825A and HP 12044A). The cable description and model numbers are provided below:

HP 91712A: 75 meter (246 feet) interface extension cable with assembled connectors.

HP 91713A: Connector kit which includes one male and one female connector with hoods and clamps, and a wiring diagram.

Opt. 001: Replaces the standard cable connectors with two printed-circuit edge connectors used to fabricate a longer interface cable (eliminates the need for an additional extension cable).

HP 91714A: Custom cable kit which includes 300 meters (984 feet) of cabling and the connector kit described above.

SPECIFICATIONS

Table 1-1, in the applicable PSI manual, describes the maximum capabilities of the PSI, exempt from firmware control. Table 1-1, below, lists the specifications of the interface as governed by the HDLC firmware.

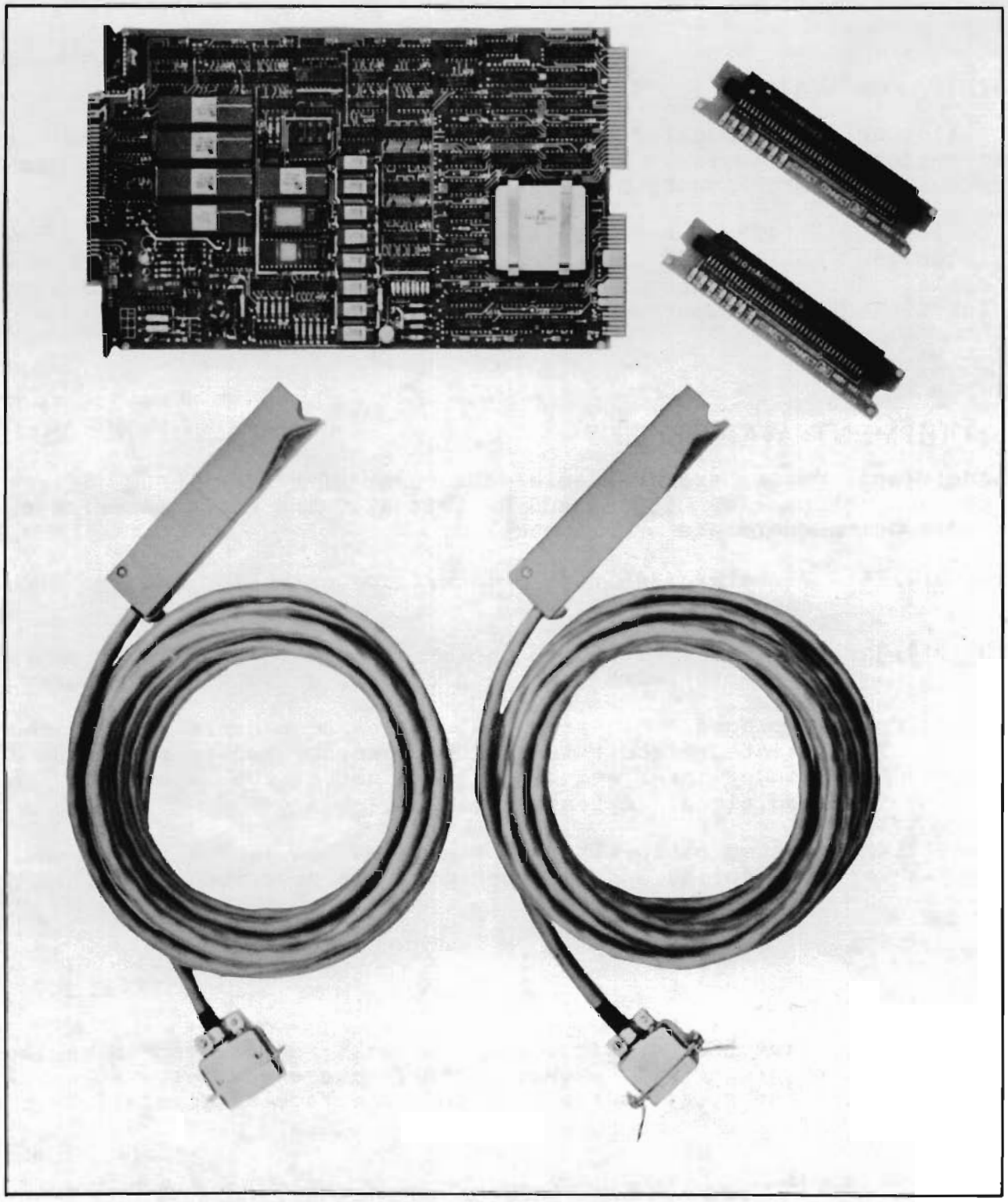


Figure 1-4. HP 12044A HDLC Direct Connect Programmable Serial Interface for L/A-Series Computers

Table 1-1. High Level Data Link Control Specifications

TRANSMISSION MODE:	Bit serial; synchronous.
TRANSMISSION LINK	
Direct Connect:	Full duplex over four individually shielded twisted pairs. Lines are optically isolated at the receivers on the card.
Modem:	Full duplex only.
ISOLATION PROVIDED	
Direct Connect:	1 kilovolt common mode.
MAXIMUM CABLE LENGTH	
Direct Connect:	1 kilometer at 230K baud. 2.2 kilometers at 57.6K baud.
INTERFACE	
Direct Connect:	EIA Standard RS-422: Balanced drivers and receivers.
Modem:	Conforms to RS-232-C and RS-449 and CCITT V.28.
DATA TRANSFER LENGTH:	Selectable frame size (128 or 1024 byte information field length).
DATA TRANSFER RATE:	Approximately 300, 1200, 2400, 4800, 9600, 19200, 57600, or 230000 bps.
MODEM TYPES:	Synchronous, full duplex only.
MODEM COMPATIBILITY:	Refer to Appendix A.
ERROR DETECTION:	CRC-CCITT.
ERROR CORRECTION:	Retransmission under firmware control.

INSTALLATION

Prior to installing the PSI card, ensure that the ROMs are mounted on the card. Figure 2-1 in the applicable PSI Installation and Service Manual shows the location of the ROMs. The matrix below correlates ROM part numbers with their location on the board. Then, ensure that the configuration switches have been set in accordance with switch assignment tables 1-2 and 1-3, and that the proper jumpers have been installed for the present application.

ROM PART NO. / PRODUCT NO.	91750-80008	91750-80009
HP 12007B	U24	U44
HP 12044A	U93	U73
HP 12794B	U93	U203
HP 12825A	U54	U44

Switch Configuration

Each PSI card contains at least one set of eight switches, used to set the information field size (switch 2) and the communications clock (switches 6,7, and 8).

Table 1-2. Switch Assignments
U15 (L/A-Series) or SW1 (M/E/F-Series)

SWITCH	FUNCTION
1	M/E/F/-Series: Open to disable Forced Cold Load capability. L/A-Series: Not used.
2	Closed to select *128 byte information field. Open to select 1024 byte information field. BOTH SIDES OF THE LINK MUST HAVE THIS SWITCH SET THE SAME TO AVOID DATA OVERRUN.
3,4,5	Not used.
6,7,8	Select transmission clock rate. See Table 1-3.

* 128 byte information field is recommended to minimize frame retransmissions.

Communications Clock. Switch numbers 6 through 8 on the 8-position DIP switch determine the clock rate being supplied to the modem or I/O device.

The "0" state equates with an open switch; the "1" state equates with a closed switch. Bit rates and associated switch settings are given in Table 1-3.

Table 1-3. Communications Clock Rates

SWITCH SETTINGS			COMMUNICATIONS BIT RATE (BPS)
SW8	SW7	SW6	
0	0	0	300
0	0	1	1200
0	1	0	2400
0	1	1	4800
1	0	0	9600
1	0	1	19.2K
1	1	0	57.6K
1	1	1	230.0K

Jumper Configuration

One set of selectable jumpers (or two, depending on the card) must be configured for the ROM/EPROM device type used. Consult the applicable PSI manual.

Modem Card Jumpers. Two additional jumpers must be configured on each of the PSI modem interface cards:

(1) W4 on the L/A-Series card and W1 on the M/E/F-Series card must be installed in the "A" position for normal operation and for use with a loop-back or diagnostic hood. This configuration releases TERMINAL READY (TR) to firmware control.

The only application for jumpers W1 or W4 installed in the "B" position is when the card is interfacing to a 2-wire switched network (dial up) modem (e.g., Bell 212), for the following applications: when downloading programs via the Communications Bootstrap Loader (CBL in M/E/F-Series computers) or the Distributed Systems Virtual Control Panel (DSVCP in L/A-Series computers). Position "B" holds TR high, preventing the modem from disconnecting each time the Bootstrap Loader firmware resets the PSI card. Refer to the DS/1000-IV Network Manager's Manual for details on the use of CBL or DSVCP.

Note that some 2-wire switched network modems, especially in Europe, may not be able to Auto-Answer when TR is held high. (Manual Answer and Originate are not affected.) This means that bootstrap downloading of programs and Auto-Answer operation over the same modem may be mutually exclusive in some geographical areas. Consult a local data communications expert for information about applicable modems in your area.

(2) W5 on the L/A-Series card and W6 on the M/E/F-Series card must be strapped in the "A" position. The "B" position is not defined for HDLC firmware.

CHAPTER 2
PROTOCOL

There are many levels of protocol involved in an HP DS/1000 communications link. Two of these levels are handled on the HDLC PSI cards: line protocol and communications protocol. The first level involves timing and control signals, and electrical specifications for computer-to-computer connections. Line protocol, used by HDLC firmware, is compatible with EIA standards RS-232-C, RS-449, and CCITT standard V.24 serial I/O implementations. The second level involves the more complex set of rules used to control the flow of data over the communication link. Both line and communications protocols are firmware controlled on the PSI card. Additional information about this HDLC implementation can be obtained in the CCITT Recommendation X.25, and Link Access Protocol (LAP).

COMMUNICATIONS PROTOCOL

With the ROMs installed, the PSI card will implement High Level Data Link Control (HDLC) protocol. HDLC is a synchronous, bit oriented protocol designed for use over full-duplex communications channels. The following paragraphs discuss the main characteristics of HDLC.

HDLC FRAME FORMAT

Data transfers using HDLC protocol are bit oriented as opposed to character oriented. Blocks of data are transmitted in frames, a frame being a bit stream starting and ending with a flag. For this implementation, the flag is the following bit pattern:

01111110

A frame may or may not contain data but always contains control information. A frame consists of several fields as illustrated in Figure 2-1 and described in the following paragraphs.

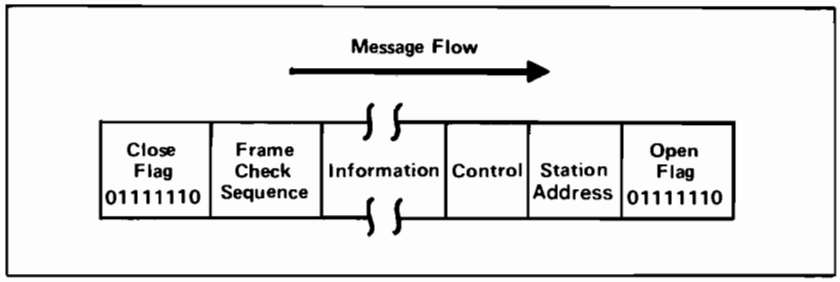


Figure 2-1. HDLC Frame Format

Flag Field

HDLC uses positional significance, not control characters, to identify the various elements of a message. The flag field is the first eight bits of a frame which the receiver uses to count down the incoming bit stream in order to identify the other fields within the frame. The close flag is used to indicate the end of the frame. The firmware also uses the close flag to count back to the frame check sequence field.

Zeroes are inserted and deleted as required to prevent a flag bit pattern from appearing within the frame. When five 1's appear, the transmitter inserts a 0 into the bit stream after the last 1. The receiver detects the five 1's followed by a 0 and deletes the 0. The inserted and deleted zeroes are not included in the frame check sequence. This zero insertion/deletion scheme is controlled by the Z-80A SIO chip on the PSI card.

Each interface on the link is continuously searching for the flag pattern. During lulls in message flow, a series of flags is transmitted to keep the link active and synchronized.

Station Address Field

Since all links in a DS network are point-to-point, station address information is not needed as such. Instead, this field is used to convey whether the frame contains a response or a command. This information is necessary due to the data handling organization at each station on the link. Outgoing commands and incoming responses are handled by the primary portion of the firmware driver. Incoming commands and outgoing responses are handled by the secondary portion of the driver. This primary/secondary scheme is one way of implementing a full-duplex communications protocol.

Control Field

The control field consists of eight bits containing a command or response pattern required for control of the data link. The primary station uses the field to command the secondary to perform an operation. The secondary uses it to respond to the primary. The control field has three formats, indicating the contents and purpose of the frame as follows (refer to Table 2-1 also):

1. Information Transfer. This control field format indicates that the present frame contains information being transferred from the local primary to the remote secondary.

2. Supervisory Response. A frame with a supervisory format in the control field contains no information (the information field is interpretted to be of zero length), and is used to regulate traffic and request retransmission of missed or erroneous frames.

3. Unnumbered Command/Response. This format consists of commands and responses used to establish or disconnect the communications channel, reject commands (those not recoverable by retransmission), or request a remote node to go into front panel mode.

Information Field

A non-zero length information field only exists in frames designated as information transfer frames by the control field. When used, the information field is the vehicle for moving data between stations and it is unrestricted in format and contents. Information field length is selected to be 128 or 1024 bytes using one of the configuration switches on the interface card.

Frame Check Sequence Field

This field is 16 bits in length and preceeds the closing flag. Frame check sequence follows the information field when present, otherwise it follows the control field. Its purpose is to detect errors that occur during transmission. For each of the PSI cards, the frame check sequence is computed under Z-80A SIO chip control using the CRC-CCITT, cyclic redundancy check, block check method. This consists of dividing a constant into the first group of bits being transmitted after the opening flag. The quotient is discarded and the remainder added to the next group of bits, which is again divided by the same constant. This continues until the closing flag is detected. At that time, the 16-bit CRC-CCITT remainder is sent in the frame check sequence field before the closing flag.

Table 2-1. HDLC Protocol Bytes (Control Field)

TYPE	MNEMONIC	DESCRIPTION	ENCODING							
			7	6	5	4	3	2	1	0
INFO.	I	Information	Nr			P	Ns			0
SUPRV.	RR	Receiver Ready	Nr			F	0	0	0	1
	RNR	Receiver Not Ready	Nr			F	0	1	0	1
	REJ	Reject	Nr			F	1	0	0	1
UNNUM.	SARM	Set Asynchronous	0	0	0	0	1	1	1	1
	DISC	Disconnect	0	1	0	0	0	0	1	1
	UA	Unnumbered Acknowl.	0	1	1	0	0	0	1	1
	CMDR	Command Reject	1	0	0	0	0	1	1	1
	SIM	Set Initial. Mode	0	0	0	0	0	1	1	1

Abbreviations:

P - Poll Bit
F - Final Bit
Nr - Receive Sequence Number
Ns - Send Sequence Number

ERROR CONTROL

As described in a previous paragraph, CRC-CCITT is used by the PSI to detect errors in transmitted frames. There are other types of error control methods used on an HDLC link as described in the following paragraphs.

Frame Sequencing Checks

Sequencing counts are kept on each interface card and transmitted as necessary to be used to acknowledge frames received correctly. The values of these counts are sent in the control field as the following variables:

Ns - Send Sequence Number.
Ns is only transmitted in information frame control words and is used to tell the receiver the number of the frame being sent.

Nr - Receive Sequence Number.
Nr is transmitted in the control field for supervisory and information frames only and is used to convey the number of frames received successfully. The value of Nr sent is equal to the number of the next frame that is expected.

The counts kept for Nr and Ns are only incremented when frames containing information are sent or received. Supervisory and unnumbered command/response frames do not affect these counts. These frames are acknowledged by proper response words. By keeping track of frames sent and received in this manner, it is possible for transmitting stations to transmit frames before the response is returned for previously transmitted frames. Also, one response can serve to acknowledge more than one received frame. This increases overall link throughput. The number of unacknowledged frames allowed in this implementation of HDLC is seven. After that, outgoing messages are put in a queue and sent only when the proper responses are received.

If a sequence error is detected by a transmitting station, it will retransmit the frame after the last acknowledged frame and set the P (Poll) bit to signal that it is a retransmission. The P bit set also demands that the receiving station respond with a supervisory frame instead of the standard information frame acknowledgement. In the response supervisory frame, the F (Final) bit is set to indicate that it is responding to a received poll.

Severe Error Processing

The HDLC interface card is capable of detecting other types of errors besides invalid frames (CRC-CCITT detected errors) and sequence errors. The other detectable errors are referred to as severe errors and include such cases as:

* Unknown frame type
* Information field larger than available frame buffer
* Ns greater than seven
* Failure to acknowledge after maximum allowable retries

These errors are reported to the software driver by the firmware on the card, and then an attempt is made to recover. For failure to acknowledge, the link is reset. This is similar to the original connect sequence whereby the primary station sends a SARM frame and waits to receive a UA frame from the secondary. For the other severe errors, a command reject frame is sent.

LINE PROTOCOL

HDLC is capable of implementing line protocol compatible with EIA standard RS-232-C, or EIA RS-449 and CCITT V.24 (for modem interfaces). In the following paragraphs, interface circuits are referenced by RS-449 nomenclature. The applicable PSI manual provides a cross reference of RS-232-C, RS-449, and CCITT V.24 signal names.

The following discussion assumes the HP 1000 has been powered up and the communications line is not yet operational. At power up, a reset signal is asserted which resets all logic on the card, including the Z-80 components. Resetting the Z-80 CPU invokes a firmware-resident self-test routine. The of this test are available to the host driver.

Connect Sequence

The communications line is powered up with TR (Terminal Ready) for modems possessing an Auto-Answer feature.

The two ends of the communications line must be logically connected (physical connection is assumed at this point). The primary sends a SARM frame and waits for a UA frame from the secondary. In our HP 1000-to-HP 1000 configuration, each card sends a SARM frame and waits for a UA frame. When this handshake sequence is complete, a logical connection exists between the two computers.

Modem interfaces require further handshaking. The host asserts RS (Request to Send) and waits for CS (Clear to Send) from the modem. The receive handshake involves waiting for the host to assert RR (Receiver Ready). The host then hunts for a flag field for synchronization

Disconnect Sequence

The communications line is logically disconnected after each station sends a DISC frame and receives a UA frame. Either end of the DS link can initiate the disconnect sequence.

The modem interface is physically disconnected after TR and RS have been dropped.

I/O Backplane Processing

Command and Status Words. In addition to data words, command and status words are also exchanged between the host and the card. These additional words are transferred across the data bus and the data latches to aid in the process of communication between the host and the card.

Command words are initiated by the host driver and fall into the following four basic categories:

Type 0 - initiates a data transfer from a card buffer to a host computer buffer.

Type 1 - a single word command sent directly to the card firmware. Examples include disconnect, abort current operation, discard input buffer, etc.

Type 2 - initiates a data transfer from a host computer buffer to a card buffer.

Type 3 - specifies that a multiple-word command follows.

Status words are generated by the card to inform the host of events that have occurred, are occurring or will be occurring on the card or communications line. Examples of these messages include transfer buffer ready, connect complete, error condition and message block size (and modem input line status if applicable).

Data Transfer. The steps involved in an output transfer from the host computer to the communications line (i.e., an output transfer) are as follows:

1. The host (software) driver enables a request for output buffers (command type 1) into the data latches and then causes a Z-80A non-maskable interrupt (NMI). Because of the NMI, the firmware interprets the data in the latches as a command.

2. When a buffer becomes available, the host driver requests a transfer (command type 2) and enables the DMA hardware of the host.

3. The card writes zeros to the output latches. This starts the DMA transfer from the host, involving the backplane latches, control logic, data bus, Z-80A DMA chip and RAM.

4. The card interrupts the host when data transfer is complete.

5. The host may transfer additional blocks of data to the the card as buffer space becomes available. Steps 2 through 4 are repeated until the messsage is transferred from the host to the card in its entirety.

6. Each data block in the RAM buffer on the card is transferred via DMA to the SIO when the SIO chip becomes ready for the transfer. The SIO chip transmits the data as it is received via DMA. The CRC frame check sequence is sent as required.

Keep in mind that the Z-80A CPU is controlling all of the processing on the card by executing instructions that it fetches from ROM. This is referred to as the card firmware.

The steps involved in a transfer from the communications line to the host computer (i.e., an input transfer) are as follows:

1. The host driver enables inputs from the card by writing a command word (command type 1) into the data latches.

2. The card firmware then sends a status word via the data latches to the host driver informing it that an input buffer is available.

3. The host driver issues a request for input data (command type 0) and enables the host DMA hardware.

4. The card enables the first data word into the data latches and asserts SRQ via the backplane logic.

5. The host driver begins the data transfer and the data block is transferred from the RAM on the card to the host via a DMA chip, the data bus, the backplane latches and the backplane handshake logic. Steps 2 through 5 are repeated until the entire message has been transferred.

6. The host driver re-enables the card for status inputs.

CHAPTER 3
DIAGNOSTICS

If it has been established that a hardware failure exists in the HP 1000-to-HP 1000 link, several diagnostic procedures are available which help to localize the problem. This chapter documents the use of self-test, interprets LED patterns occurring during normal operation and self-test execution, and instructs the user in accessing card configuration information and exercising the communication link. Cables and loop-back connectors are illustrated at the end of the chapter.

SELF TEST

Self-test is located in firmware and is performed automatically, each time power is applied to the card. The test is also initiated by resetting the card. This can be implemented by cycling power to the computer or executing a "CLC 0" instruction to reset all I/O cards in the computer backplane. Self-test will also execute upon pressing the Preset button on the front panel (M/E/F-Series), pressing the Reset button on the CPU card (L/A-Series), or entering the %P command on the Virtual Control Panel (L/A-Series).

NOTE

It is recommended that the node be quiesced before running self-test. This will allow all pending DS transactions to be completed and new ones from starting. To quiesce the node, enter the commands:

```
RU,DSMOD<cr>   (DSMOD will prompt for a command.)
/Q             (DSMOD will prompt for security code.
                Obtain code from network manager.)
DS             (default code)
```

Once the "NODE IS QUIESCENT" message appears on the screen, cycle power to the computer. (For a description of DSMOD, refer to the Network Manager's Manual.)

Description

The following is a brief description of the self-test feature:

ROM TEST:

Performs checksum on ROM contents.

CPU TEST:

Checks for stuck-at faults in the data lines, address lines, and registers. The ALU operations, addressing modes, and I/O are also checked.

RAM TEST:

Checks for permanent faults in RAM. RAM control circuitry is tested, as is the CPU's ability to read and write to RAM.

DMA TEST:

Checks all registers, control lines, data lines, and address lines for stuck-at faults. Tests for proper operation including memory-to-memory transfer, and search-transfer.

CTC TEST:

Tests the CTC's basic functions, such as decrementing the down counters, and both generating, and holding off interrupts.

SIO TEST:

Tests SIO operations. Includes both synchronous and asynchronous transmission and reception at 19.2K baud and 1200 baud respectively.

MODEM/CONTROL TEST:

Checks Modem/Control lines and latches for stuck-at faults.

INTERFACE LEDs

There is a row of four LEDs on three of the PSI cards, referenced from left to right as LED3 through LED0. These LEDs are located to the left of the frontplane edge connector on the M/E/F-Series cards; on the L/A-Series modem card, they can be found behind the rightmost edge connector pins. The LEDs on the L/A-Series direct connect card are arranged in columnar format and located to the left of the edge connector with LED0 nearest the frontplane.

During normal operation LED0 and LED1 are used by HDLC firmware to indicate card states. LED0 "on" indicates that the interface is logically connected to the other interface on the link. LED1 "on" indicates that a DMA data transfer is taking place over the backplane. LED2 and LED3 are not used and should be off during normal operation.

Self Test Patterns

Self-test initially turns all LEDs on. Shortly thereafter LED0 is turned off. Upon successful completion of self-test, LED0 is again turned on. This display is rather brief as the completion of self-test is immediately followed by the execution of HDLC; one of the first tasks in HDLC is to clear all LEDs.

Should the card fail self-test, the LEDs will continuously display the pattern peculiar to the failure mode.

If the card fails self-test, LED0 and LED1 will be off, LED2 and LED3 will be on.

Only LED0 off at the end of self-test indicates the card has failed and is hung up in a loop.

LED2 senses the presence of a Diagnostic Hood. (Not supplied with card. The HDLC product is supplied with a loop-back hood.) LED2 blinks a few moments into the test if a Diagnostic Hood was sensed; otherwise it remains continuously on.

LED3 always remains on during self-test.

After successful completion of self-test, LED2 and LED3 will be off while LED0 and LED1 will indicate card states during normal operation as described above.

INTERFACE CARD CONFIGURATION CHECK

The following procedure provides further verification of successful self-test completion. It also ensures that the backplane interface is operational by reading the card configuration switch settings. To perform the check, enter the commands:

1. RU,DSINF<cr>

   DSINF is a DS/1000-IV utility program that can be used to obtain information such as network communication parameters, etc. For more information on DSINF, consult the Network Manager's Manual.

2. LU,##,AL<cr>

   LU returns information on the configuration of a specified DS/1000 interface card, where ## is the lower (or transmit) LU (Logical Unit) number of that card. Information will only be returned if the card passed the self-test.

DSINF returns card configuration information as well as other useful parameters. Verify that the returned information complies with the card configuration. Unexpected values should be checked against switch settings on the card. If in error, repeat the installation procedures to correctly configure the card. Repeat all check-out procedures.

COMMUNICATION LINK CHECK

Before following the procedures described in this section, it is important to understand the message re-routing capabilities of the network. If there is an alternate path to the remote node being tested, message re-routing must be disabled to ensure that the desired link is being exercised. Check with the network manager about network topology and message re-routing before proceeding.

The communication link can be exercised by implementing a few REMAT commands. To do this, type in the following commands (note that the system prompt has been included with the command string):

1. :RU,REMAT<cr>

   REMAT is a program that handles operator commands for communication from one HP 1000 to another in a Distributed Systems network. It schedules the appropriate monitors to handle all outgoing and incoming requests. REMAT will prompt with a dollar sign ($) when commands are referred to the local node only. When a remote node is referenced, REMAT prompts with a number sign (#).

2. $SW,NODE1,NODE2,SC<cr>

   The SW (Switch) instruction defines the action and destination nodes. Set NODE1 to the node number of the neighbor node that is to be exercised. Set NODE2 to the local node's number. SC is the security code for the network, defined at network initialization.

3. #TI<cr> or #TM<cr>

   The TI or TM commands obtain the time from the remote node and display it on the local terminal being used for this exercise. The TI command should be used if the remote node is an HP 1000 M/E/F-Series computer; TM should be used with HP 1000 L/A-Series remote nodes. If the remote node does not have the necessary monitor to handle the TI or TM command, or does not have a real-time clock, try a DL (Directory List) or CL (Cartridge List) command.

4. #EX<cr>

   The EX (Exit) command terminates REMAT.

If the foregoing procedure is carried out successfully, the described results will be displayed. If an error message is returned, refer to error code information supplied in the Operating System's User's manual. procedures are provided in the following paragraphs and in the Network Manager's Manual.

LOOP-BACK VERIFIER HOOD CHECK

Another method of exercising the interface is to install the loop-back verifier hood supplied with the PSI card. This tool allows the user to configure the card to actually talk to itself: any message sent by the interface will be "looped back" onto the card. Thus, sending and receiving capabilities of the card, as well as computer-card communications are verified.

Install W4 (L/A-Series modem card) or W1 (M/E/F-Series modem card) in position A.

1. Quiesce the node and remove power from the computer. Follow the same procedure outlined under SELF-TEST.

2. Remove the cable from the front edge connector and install the loop-back verifier hood in its place, orienting the connector the same as all other connectors in the card cage. (The loop-back verifier hood is supplied with the product. HP part numbers are referenced in Chapter 1.)

3. Restore power to the system. When this occurs, the self-test is automatically executed on the card. The results of the test are returned to the software driver. Restore the operating system and check that the self-test completed successfully. Consult the foregoing text for available procedures to verify self-test results. (Note that DSINF does not sense the presence of the loop-back verifier hood.)

4. Once it has been established that the card has passed the self-test, a further check can be accomplished by sending a message to the card and having it looped back on itself. To configure the card to talk to itself, run DSMOD. Enter the command CN. DSMOD will prompt for the network security code which can be obtained from the network manager. After that has been entered, DSMOD will prompt for the node number to be changed. Enter the local node number. DSMOD will display the current routing vector for the local node which should specify LU 0. Then, after the prompt for the new configuration, enter the lower (or transmit) LU number of the card that has the loop-back verifier hood installed on it. Now enter /E in response to the prompt for the next node number to be changed, and another /E to exit DSMOD. The card is now configured to talk to the local node.

5. Run REMAT (see previous discussion) and execute some REMAT commands such as TI or DL. When this happens, the routing vector will specify that all commands to be executed at the local node should be sent out to the configured interface card. The card will transmit the data, it will be looped back through the hood, and the card will receive the data and send it back to the local CPU. If no errors are returned, this is a very good indication that the interface card and backplane circuitry are operational.

   If no errors were detected, construct a loop-back connector using the wiring diagram provided (figure 3-1 or 3-2) and the mating connector for the interface cable in use. Connect the loop-back at the remote end of the cable and run REMAT as described above. If errors are now detected, the interface cable is defective.

6. After the test is complete, run DSMOD and reconfigure the local node routing vector to again specify LU 0.

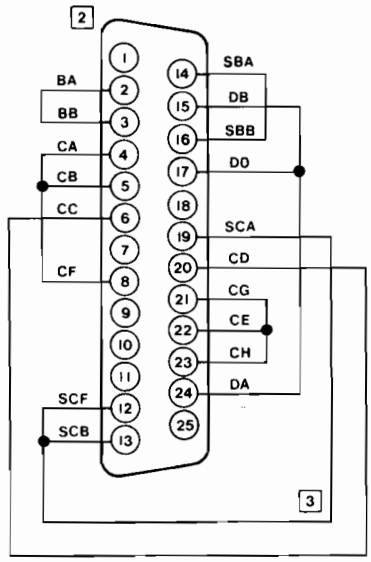
7. Remove power from the system and replace the loop-back verifier hood with the cable.

8. Restore power to the computer and reinitialize the system and DS software.

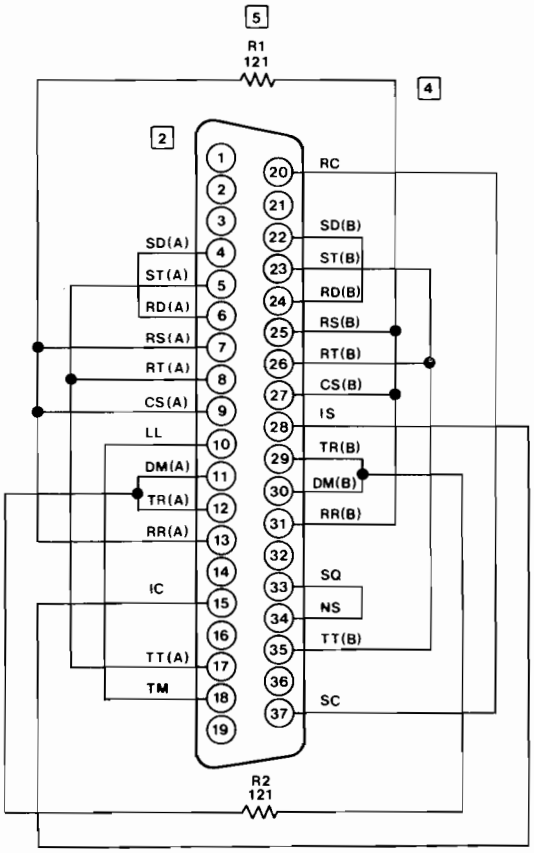
Since the loop-back verifier hood test checks more areas of the card (specifically the line drivers/receivers area of the interface, and the backplane interface circuitry), it is possible for the card to pass the self-test and fail the loop-back hood test.

ITEM	QTY.	MAT'L DESCRIPTION	MAT'L PART NO.
4	2	JACK SOCKET 4-40 THD x .25	0380-1107
3	A/R	WIRE 24 AWG	8150-0299
2	1	CONN MOULDED "D", 25P FEM	1251-0064
1	A/R	MOULDING COMPOUND	4093-0376

Figure 3-1. Loop-back Wiring Diagram for RS-232-C Modem Cable



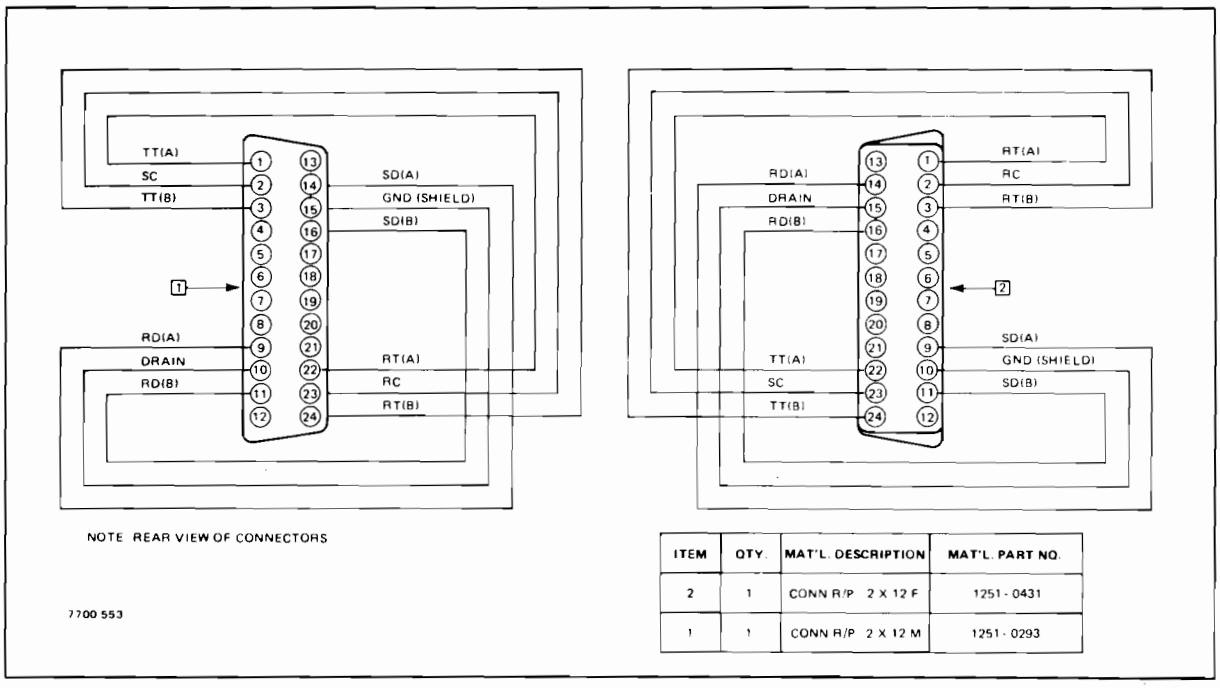
FRONT VIEW OF
ASSEMBLED RS 232 CONNECTOR
HP PART NUMBER 0960 - 0475



FRONT VIEW OF ASSEMBLED
RS 449 CONNECTOR

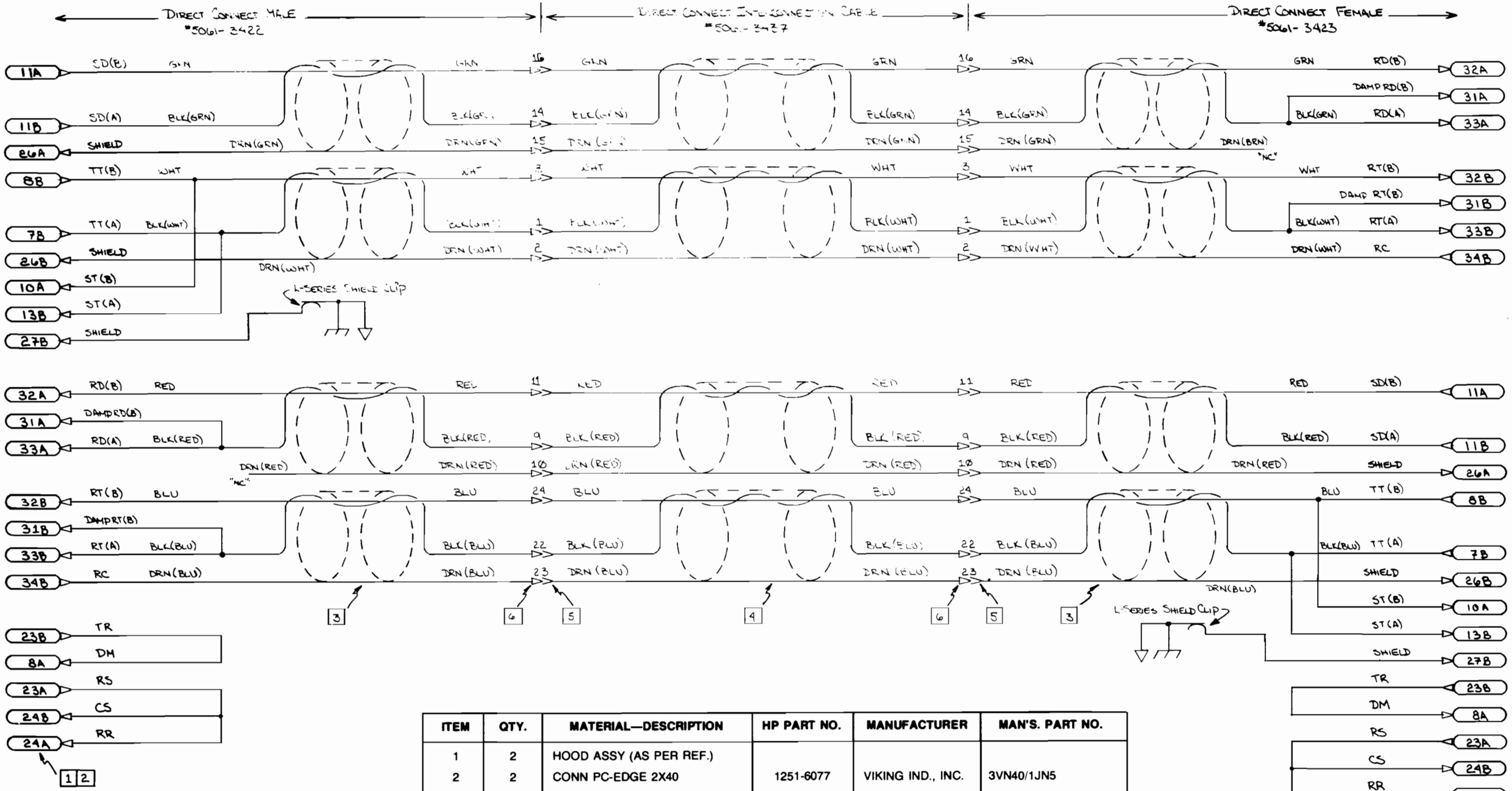
ITEM	QTY.	MAT'L DESCRIPTION	MAT'L PART NO.
5	2	R121 0.1%, .125W	0757-0403
4	A/R	WIRE 24 AWG	8150-0299
3	1	SLIDE LOCK	1251-1029
2	1	CONN F D-SUBMIN	1251-4585
1	1	CONN SHELL	1251-6664

Figure 3-2. Loop-back Wiring Diagram for RS-449 Modem Cable



ITEM	QTY.	MAT'L. DESCRIPTION	MAT'L. PART NO.
2	1	CONN R/P 2 X 12 F	1251-0431
1	1	CONN R/P 2 X 12 M	1251-0293

Figure 3-3. Loop-Back Wiring Diagram
for Direct Connect Cable



ITEM	QTY.	MATERIAL—DESCRIPTION	HP PART NO.	MANUFACTURER	MAN'S. PART NO.
1	2	HOOD ASSY (AS PER REF.)			
2	2	CONN PC-EDGE 2X40	1251-6077	VIKING IND., INC.	3VN40/1JN5
3	(2)5m	CABLE 4TWPR IND.SH. W 4DR.	8120-3096	BELDEN	QUOTE NO. 81379-9
4	75m	CABLE 4TWPR IND.SH. W 4DR.	8120-3096	BELDEN	QUOTE NO. 81379-9
5	2	CONN R&P 2X12 FEMALE	1251-0431	AMPHENOL	57-60240
6	2	CONN R&P 2X12 MALE	1251-0293	AMPHENOL	57-30240

Figure 3-4. Direct Connect Extension Cable Wiring Diagram

APPENDIX A
COMPATIBLE MODEMS AND RECOMMENDED OPTIONS

GDC 212 MODEM

The GDC (General DataComm Industries, Inc.) 212A Modem provides full-duplex, synchronous or asynchronous data communications over 2-wire switched networks. It will operate in an asynchronous mode, at 0 to 300 bits per second with 103, 113, and 212A types of modems, or 1200 bits per second, synchronously or asynchronously, with other 212A modems. The options available and recommended for use with the HDLC Modem Interface Kit are:

CUSTOMER SPECIFIED OPTIONS

GDC CODE	FEATURE SELECTION	RECOMMENDATION
2a	Async/Start-Stop	
2b	Sync Tx/Rx Clk	2b (required)
5a	9 bits per asynchronous character.	Don't Care
5b	10 bits per asynchronous character.	
6a	Dir. conn. between signal and chassis ground.	6a
6b	100 ohm resistor between signal and chassis ground.	
7a	CC on during analog loopback test.	7a
7b	CC forced off during analog loopback.	
9a	CB off whenever CF is off.	9a
9b	CF has no effect on CB.	
10a	CE remains on in Answer Mode.	
10b	CE on only during ringing.	10b
11a	CI speed indicator signal enabled.	
11b	CI speed indicator signal disabled.	11b
12a	CN circuit controls make busy and analog loopback.	
12b	CN inactive.	12b

GDC 212A MODEM (cont.)

TELEPHONE COMPANY SPECIFIED OPTIONS

GDC CODE	FEATURE SELECTION	RECOMMENDATION
1a	Call is dropped upon receipt of 1.5 second steady space.	
1b	Steady space has no effect on modem.	1b
3a	No steady space transmitted before disconnecting.	3a
3b	Steady space transmitted before disconnecting.	
4a	Disconnect upon loss of carrier signal.	4a
4b	No disconnect upon loss of carrier signal.	
8a	Auto-answer enabled.	8a
8b	Manual answer required.	
13a	Timing from DD receive clock (slave timing).	
13b	Timing from DB transmit clock in modem (internal timing).	13b (required)
13c	Timing from DA external source (external timing).	
14a	Tip-ring busy during analog test.	
14b	Tip-ring not busy during analog test.	14b
15a	High-speed (1200 bits per second only)	Don't care
15b	Either high-speed (1200) or low-speed (300 bits per second)	
16a	Receiver responds to digital loopback test command from remote modem.	Don't care
16b	Receiver responds to digital loopback test command from local modem only.	

GDC 212A MODEM (cont.)

OTHER OPTIONS

GDC CODE	FEATURE SELECTION	RECOMMENDATION
17a	TM signal enable.	17a
17b	TM signal disable.	
18a	565/2565 Telephone.	
18b	502/RTC Telephone.	18b
19a	CN line to business machine on pin 18.	19a
19b	CN line not connected.	
20a	RDL line on pin 19.	
20b	RDL line on pin 21.	20b
20c	RDL line disconnected.	
21a	CH from business machine connected.	21a
21b	CH from business machine disconnected.	

BELL 212A MODEM

The Bell 212A Modem provides full duplex, synchronous or aynchronous communications over a 2-wire switched network. It can operate at 0 to 300 bits per second in an asynchronous mode for operation with 103, 113, or 212A types of modems, or at 1200 bits per second, synchronously or asynchronously with other 212A modems. The options available and recommended for use with the HDLC Interface are:

CUSTOMER OPTIONS

OPTION	DESCRIPTION	RECOMMENDATION
ZF	CC circuit on during AL test.	ZF
ZE	CC circuit off during AL test.	
XJ	CH circuit controls speed.	
XK	HS button controls speed.	XK
YE	AL/Make Busy controlled by CN circuit or AL button.	
YF	AL/Make Busy controlled only by AL button, CN internally held off.	YF(required)
YC	1200 BPS transmitter driven by internal clock.	YC(required)
YD	1200 BPS transmitter driven by DA circuit.	
WI	1200 BPS transmitter driven by Receive clock (DD).	
YG	Character-oriented operation in the high speed mode.	
YH	Bit synchronous operation in the high speed mode.	YH(required)
YI	9-bit character for 1200 bps async./start-stop operation.	
YJ	10 bit character for 1200 bps async./start-stop operation.	YJ
YK	Digital loop can be remotely activated in the high speed mode.	YK
YL	No response to remote request for a digital loop.	
XL	RL circuit enabled to activate remote digital loop.	
XM	RL circuit not connected to interface.	XM(required)

BELL 212 MODEM (cont.)

CUSTOMER OPTIONS (CONT.)

OPTION	DESCRIPTION	RECOMMENDATION
S	Call is dropped if Loss of Carrier occurs.	S
R	Loss of Carrier does not drop call.	
V	Call is dropped if steady space is received.	
Y	Space signal has no effect on modem.	Y
A	CB circuit is turned off whenever CF circuit goes off.	
B	CB circuit is not affected by CF circuit.	B
T	Steady space transmitted before disconnecting.	
U	No space transmitted before disconnecting.	U
ZH	Auto answer enabled.	ZH
ZG	No response to ringing indication.	
X	Circuit CE remains on after call is answered.	
W	Circuit CE turns off after call is answered.	W
YO	Data can cross interface only in the high speed mode.	
YP	Data can cross the interface in both speed modes.	YP
YQ	Circuit CI indicates speed mode.	
YR	Circuit CI disconnected from interface.	YR
XO	CN on pin 25, TM not connected.	XO
XN	CN on pin 18, TM not connected.	
XR	CN on pin 18, TM on pin 25.	
Q	Protective ground and signal ground tied together.	Q
P	No connection between protective ground and signal ground.	

HP 37210T MODEM

The Hewlett-Packard 37210T modem provides half-duplex via dial-up or full-duplex via leased lines at transfer rates to 4800 bits per second. The options available (determined by assembly switches) and recommended for use with the HDLC Modem Interface are (full-duplex operation only):

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
CONTROL ASSEMBLY	
Factory Set Switches. Must remain as set at factory.	
S10-1, S10-6, S10-7	O O O
S11-4, S11-5	O C
S11-7, S11-8	C C
S12-1 thru S12-4	O O O O
Train Sequence.	
S10-2	C
Receiver Turn-on Delay.	
S10-3	C
External Rate Control Enable/Disable.	
S10-4	C
24 Pushbutton Enable/ Disable.	
S10-5	O
Auto Answer Telephone Select.	
S10-8, S10-9	O C
Transmit Clock.	
S11-1, S11-9	O O
Request-to-Send Delay.	
S11-2	O
2-wire/4-wire Mode.	
S11-3	O

HP 37210T MODEM (cont.)

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
Carrier Select.	
S11-6	C
DISPLAY/PROCESSOR ASSEMBLY	
Factory Set Switches. Must remain as set at factory.	
S1-1 thru S1-6	all OPEN
S1-7	C
S1-8, S1-9	O O
ANALOG/MEMORY ASSEMBLY	
Amplitude and Delay Equalizers.	
S1-1, S1-2	O C
S2-1 thru S2-4	C O O C
Output Power Programming Resistor.	
S1-3	C
Receiver Threshold Level.	
S1-4	O
Transmitter Output Power Level.	
S3-1 thru S3-4	C O C O
Secondary Channel Select.	
S4-1 thru S4-3	O C C
Phone Line Loop-back.	
S4-1	C
4-wire/2-wire Operation.	
wire link, P/R	R

HP 37210T MODEM (cont.)

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
SECONDARY CHANNEL	
Receiver threshold S3-1,S3-2	O O
Tx/Rx Interlock Trans. S3-3	O
2-wire,4-wire S3-4	C
Secondary Tx O/P Power Level S2-1 thru S2-9	COOOOOOOO
Constant/Controlled Carrier S1-1	C
Secondary channel Enable S1-2	C
Primary channel Enable S1-3	C
Secondary channel Analog Loop-back enable S1-4	O
REMOTE COMMAND ASSEMBLY	
Receive Address. S1-1 thru S1-4	Master O O O O Slave any number
Receiver Input Attenuation. S2-1	O

HP 37210T MODEM (cont.)

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
Remote Command Transmitter Output Level. S2-2, S2-3, S2-4	C O O
Address Thumbwheel. Front Panel Control	O (Slave)

Notes:

* Refer to the HP 37210T Operating and Service Manual for the correct switch setting.

** OPEN - The modem has the auto-answer option (003).
CLOSED - The modem does not have auto-answer.

*** With auto-answer, always set to 0 dbm (C O C O).
Without auto-answer, refer to the HP 37210T Operating and Service Manual for the correct setting.

HP 37220T MODEM

The HP 37220T Modem provides full-duplex, synchronous communications via leased lines at transfer rates to 9600 bits per second. The options available (determined by strapping configurations) and recommended for use with the HDLC Modem Interface Kit are:

SWITCH FUNCTION	SWITCH SETTINGS	O=OPEN C=CLOSED
TRANSMITTER STRAPPING		
Factory Set Switches. Must remain as set at factory.	S1-1 S1-8, S1-9 S2-2, S2-3, S2-9	C O O O O O
Request-to-Send/ Clear-to-Send Delay.	S1-2, S1-3, S1-4	C O C
Data-Set-Ready Control.	S1-5, S1-6, S1-7	O O O
Auto-Retain Enable/ Disable.	S2-1	O
Transmit Clock.	S2-4, S2-5, S2-6	O C O
Remote Loop-back Selection.	S2-7, S2-8	O C
Transmit Power Level.	S3-1 thru S3-8	all OPEN
Telephone Line Loop-back Amplifier.	S3-9	O
RECEIVER STRAPPING		
Input Threshold Level.	S1-1, S1-2	C O
Factory Set Switches. Must remain as set at factory.	S1-3 thru S1-6 S1-7, S1-8, S1-9	O O O O C C O
EXTERNAL RATE SELECT VIA THE RS232C/V24 INTERFACE	Jumper Wire	Out disabled