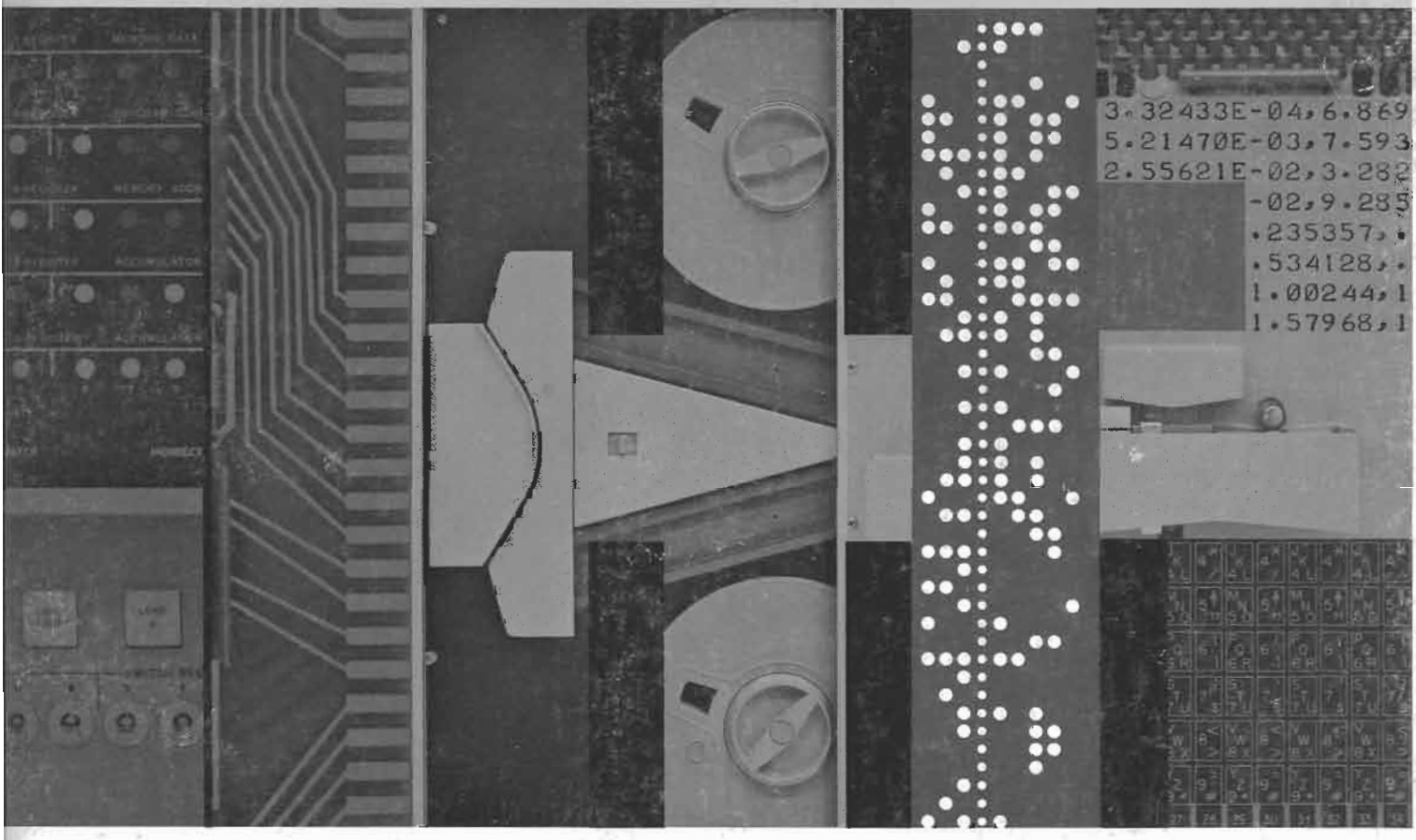
HEWLETT PACKARD

COMPUTER MAINTENANCE COURSE



VOLUMES V, VI, VII, VIII, IX

CENTRAL PROCESSOR OPTIONS

HEWLETT-PACKARD

COMPUTER MAINTENANCE COURSE

VOLUMES V, VI, VII, VIII & IX

STUDENTS MANUAL

CENTRAL PROCESSOR OPTIONS

(HP STOCK NO. 5950-8707)

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Printed in U.S.A. APR 69

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VOLUME V

MEMORY PROTECT

CONTENTS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

1-2. GENERAL DESCRIPTION

1-3. The Memory Protect Option will protect a selected portion of core memory in an HP2116A or 2116B Computer against alteration by Memory Reference or Input/Output Instructions. (Memory Protect is not available for an HP 2114A or 2115A Computer.) This option is contained in a single printed circuit card that plugs into slot A114 in the 2116A or slot A21 in the 2116B. When included in a purchase order for an HP2116B, the Memory Protect Option will be installed at the Hewlett-Packard factory. For field installation, this option is available as Kit Model 12581A. Field installation requires minor wiring changes in the basic computer.

1-4. The Memory Protect Option will protect from 1 to 32,767 words (2^{15}-1) of memory. It contains a Fence Register, a Violation Register, a Summing Network, and various logic circuits. The boundary of protected memory is set by loading into the Fence Register the address of the next higher word above those to be protected. All addresses below the fence address will be protected against alteration except 00000 and 00001 (the address of A Register and B Register). When an instruction is addressed to protected memory, a violation signal from the Summing Network will inhibit execution of the instruction, and the address of the instruction will be retained in the Violation Register. Addresses below the fence address are also protected against wrap-around. For example, if a 4K HP2116A with Memory Protect is given an instruction addressed to the upper half of an 8K memory, wrap-around into the lower 4K, below the fence address, will be prevented.

1-5. APPLICATION

1-6. One application for the Memory Protect Option is in the HP2005 Real Time Monitor System. This system is used for industrial process control. As shown on Figure 1-1 all memory locations below the fence (C) are protected. The protected area of memory is controlled by the Real Time Executive (A) in lower core. The background area of memory is available for operating simultaneous programs. That is, the real time system shares the computer. There are three conditions that will cause the system to interrupt:

a. attempts to alter a protected memory location

b. attempts to jump into a protected area

c. attempts to execute any I/O instruction other than from a trap cell

Note that when memory protect is turned on (under program control), I/O instructions must be executed under control of a subroutine.

1-7. INSTALLATION AND OPERATION

1-8. INSTALLATION

1-9. To install the Memory Protect Option in the HP2116A Computer, do the following:

a. Turn off the computer POWER switch.

b. Pull out the Power Turn-On card (Part No. 02116-6095) from slot A115 and make sure that jumper W8 (labeled on the component side of the card) is removed.

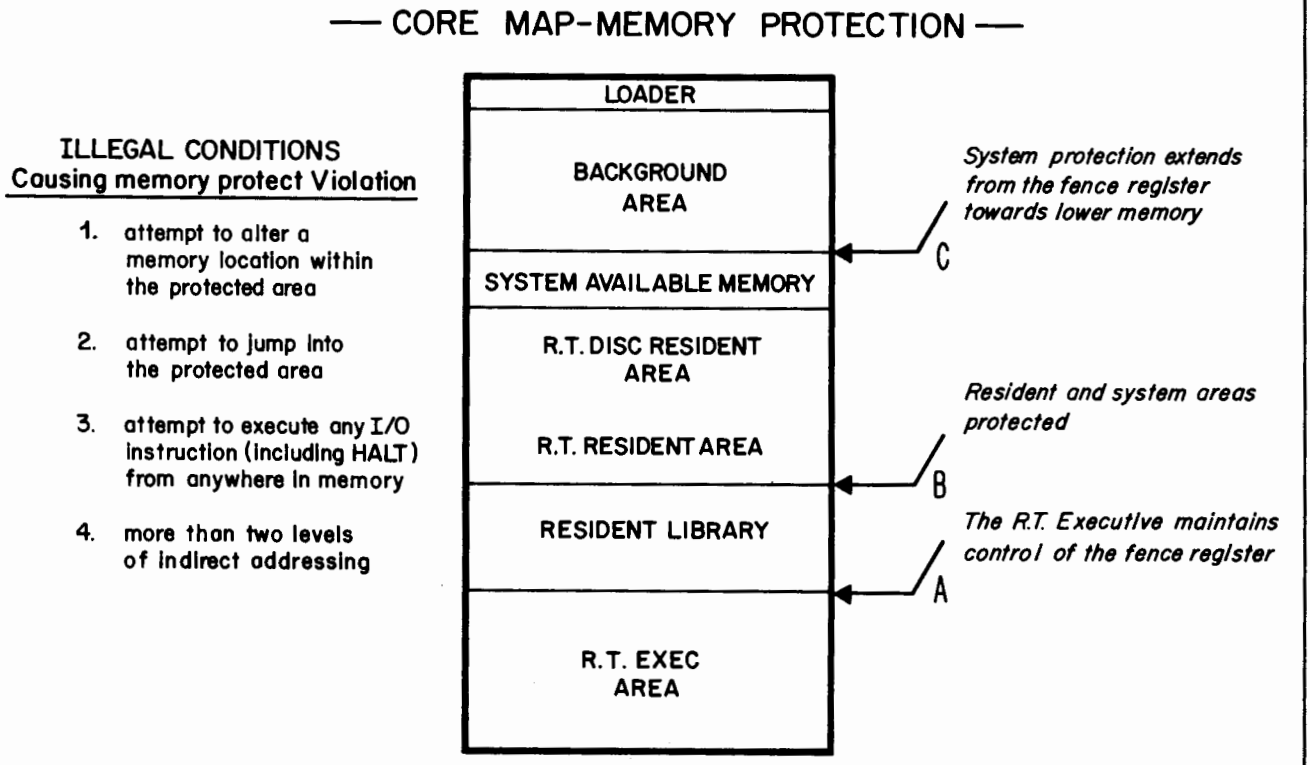


Figure 1-1. Real Time Monitor with Memory Protect

c. Return the Power Turn-On card to slot A115.

d. Turn the component side of the Memory Protect card to the right, as you face the front of the computer, and plug it into slot A114.

e. Turn on the computer POWER switch and resume operation.

To install the Memory Protect Option in the HP2116B Computer, do the following:

a. Turn off the computer POWER switch.

b. Pull out the Input/Output Control card (Part No. 02116-6041) from slot A201 and make sure that jumper W 3 (labeled on the component side of the card) is removed.

c. Return the Input/Output Control card to slot A201.

d. Turn the component side of the Memory Protect card to the right, as you face the front of the computer, and plug it into slot A21.

e. Turn on the computer POWER switch and resume operation.

-NOTE-

One corner of the Memory Protect card contains three jumpers labeled: W3, W2 and W1. These jumpers are used to prevent memory violation wrap-around by adapting the Memory Protect option to various sizes of core memory. The three jumpers should be connected as shown in Table 1-1.

TABLE 1-1. MEMORY PROTECT CARD JUMPERS

Core Memory Capacity	Jumper W3 From MC 56 Pin 4	Jumper W2 From MC 56 Pin 7	Jumper W1 From MC 56 Pin 11
32K	To Card Pin 72	To Card Pin 77	To Card Pin 74
24K	To Card Pin 72	To Ground	To Card Pin 74
16K	To Ground	To Card Pin 77	To Card Pin 74
8K	To Ground	To Ground	To Card Pin 74
4K	To Ground	To Ground	To Ground

1-10. OPERATION

1-11. When Memory Protect is turned on, no Input/Output instructions except those referencing Select Code 01 (Switch Register or Overflow) can be executed. A JMP (Jump) instruction addressed to protected memory is a violation. Any HLT (Halt) instruction is a violation. However, any single Input/Output instruction, except HLT, may be executed from an interrupt trap cell (memory cell with a Select Code address) without turning off Memory Protect. All other trap cell instructions turn it off. To preclude a series of indirect instructions from forming one large loop and disabling the Interrupt System, interrupt is held off for only two levels of a JMP, I (Jump, Indirect) or a JSB, I (Jump to Subroutine, Indirect) instruction, and then enabled. When enabled, an interrupt is not forced to any location.

1-12. Memory Protect can be turned off in only two ways: (1) by pushing the PRESET button on the front panel while the computer is in the HALT mode; (2) by programming an interrupt. When an instruction is addressed to protected memory, execution of the instruction is inhibited and an interrupt request is issued. When the interrupt request is acknowledged, the IAK (Interrupt Acknowledge) signal causes the Control Flip-Flop in Memory Protect to be reset. This turns off Memory Protect. To turn it on again, the Control Flip-Flop must be set under program control.

SECTION II

PROGRAMMING

2-1. PROGRAM CONTROL

2-2. CONTROL WORDS

2-3. Memory Protect is controlled through Select Code 05, by using the following instructions:

a. STC 05 (102705) Turn on the Memory Protect Option.

b. OTA 05 (102605) Set the Fence Register, A contains the address of the next word above those to be protected.

c. OTB 05 (106605) Set the Fence Register, B contains the address of the next word above those to be protected.

d. LIA 05 (102505) Load into A the address of the violating instruction.

e. LIB 05 (106505) Load into B the address of the violating instruction.

2-4. PROGRAMMING

2-5. SAMPLE PROGRAM

2-6. After initializing Memory Protect as described in paragraph 2-3, it is necessary to program the interrupt subroutine. A typical subroutine is given in Table 2-1.

TABLE 2-1. SAMPLE MEMORY PROTECT INTERRUPT SUBROUTINE

Label	Opcode	Operand	Comments
MPPE	NOP		Memory Protect/Parity Error Subroutine
	CLF	0	Turn off Interrupt System to inhibit I/O devices
	CLC	5, C	Turn off Parity Error interrupt during subroutine
	STA	SVA	Save A-Register
	STB	SVB	Save B-Register
	LIA	5	Get contents of Violation Register on Memory Protect card
	SSA		Check bit 15 to determine kind of error
	JMP	PERR	If a 1, go to Parity Error routine
	JMP	MPTR	If a 0, go to Memory Protect routine
MPTR	---		User's routine in case of Memory Protect violation

	LDA	SVA	Restore A-Register
	LDB	SVB	Restore B-Register
	STF	5	Turn on Parity Error interrupt
	STC	5	Turn on Memory Protect interrupt
	JMP	MPPE, I	Exit the subroutine
PERR	---		User's routine in case of parity error

	JMP	PERR-5	Restore accumulators, turn on interrupts, exit

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION

3-2. MEMORY PROTECT LOGIC

3-3. The purpose of the Memory Protect Option logic is four-fold:

a. It checks in Phase 1 for I/O instructions.

b. It checks in Phase 1 for JMP instructions.

c. It checks for violating Memory Reference instructions in Phase 3

d. It counts the number of indirect addresses occurring in Phase 2.

If any violations are encountered, the computer interrupts to location 05 (which is shared with the Parity Error Interrupt Option). The violating address is then loaded into the A or B Register under control of a subroutine (LIA/B05).

3-4. The Memory Protect Logic is given as Figure 3-3. The following descriptions implicitly reference this drawing.

3-5. LOGIC BLOCK AND FLOWCHART

3-6. A Logic Block and Flowchart is shown on Figure 3-1. In Phase 1, the Indirect Logic resets the Phase 2 Counter to zero. The I/O Protect Logic then checks for an I/O instruction in the T-Register. If an I/O instruction has been fetched, the I/O Logic then tests for a halt instruction. If HLT, the Interrupt Logic causes an interrupt to location 05. If not a HLT, the I/O Logic tests for select code 01. If not 01, the Interrupt Logic causes an interrupt to location 05.

3-7. If during Phase 1, the I/O Logic had not detected an I/O instruction, then the M Register is saved in the Violation Register Logic. The Jump Protect Logic tests for a JMP instruction. If JMP, the contents of the Fence Register are compared with the contents of the Violation Register. If the Fence Register exceeds the contents of the Violation Register, then a MEV (Memory Violation) signal is enabled and the interrupt Logic causes an interrupt to location 05. The contents of the Violation Register are then loaded into the A or B Register under control of trap cell instructions.

3-8. In Phase 2, the Indirect Counter in the Indirect Logic is indexed. The Indirect Logic then tests for a 3 in the Counter. An interrupt, however, is not forced; the indirect loop is simply broken.

3-9. In Phase 3, the contents of the Violation Register are compared with the Fence Register. If a violation exists, the Memory Protect Logic then tests for the AAF or BAF functions (addresses 0 and 1). If not AAF or BAF, the Interrupt Logic causes an interrupt to location 05.

3-10. If not Phase 1, 2, or 3 then we have either Phase 4 (Interrupt) or Phase 5 (DMA) and the memory cycle will be completed.

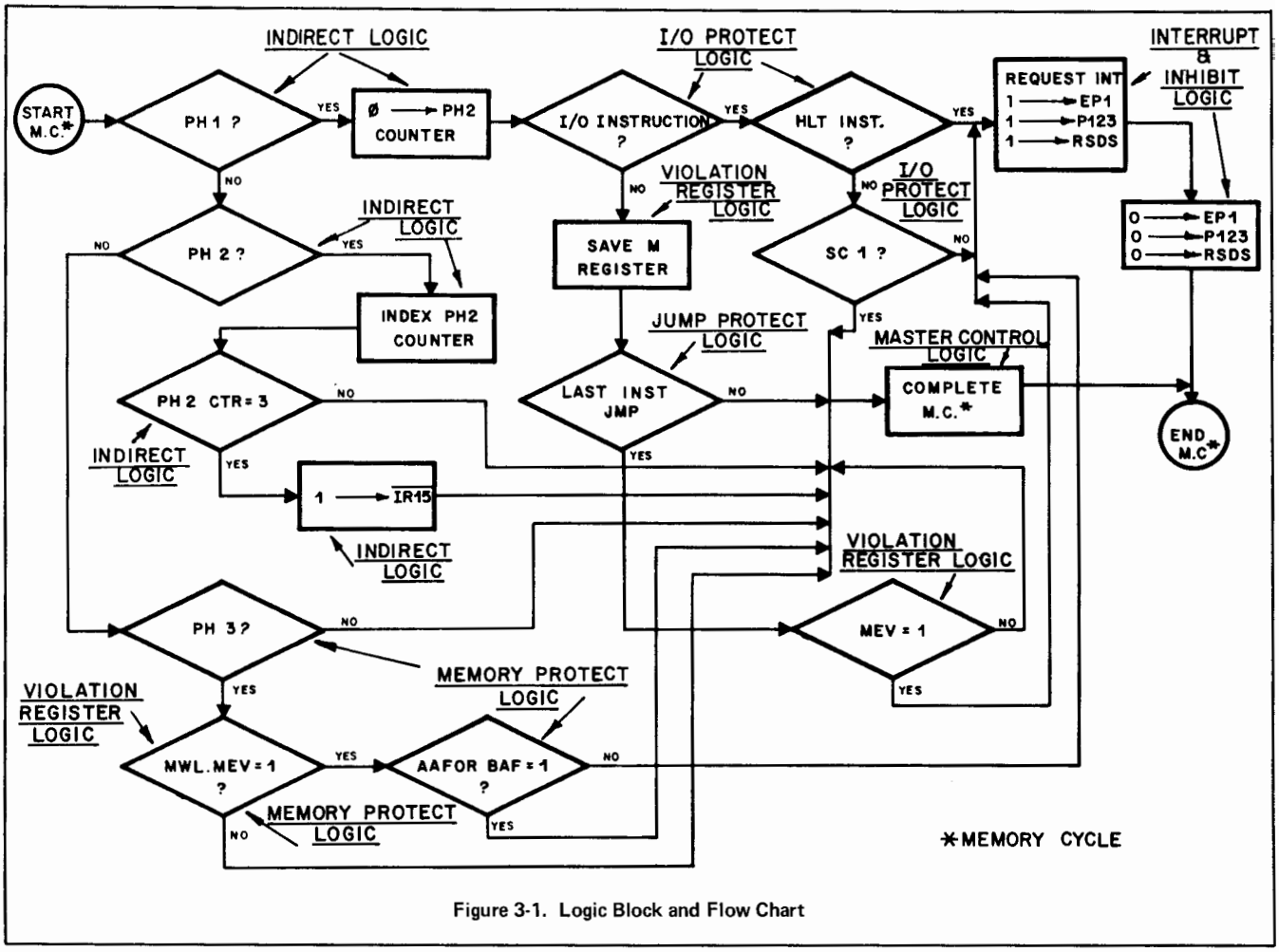


Figure 3-1. Logic Block and Flow Chart

3-11. THEORY OF OPERATION

3-12. INPUT-OUTPUT LOGIC

3-13. The purpose of the I/O Protect Logic is three-fold:

a. It tests for I/O instructions not referencing SC01.

b. It tests for the HLT instruction.

c. It provides logic signals used by other logic circuits on the board.

3-14. At T3TS gate MC43B is made true. This provides one true input to MC44C. Another input to this gate is the IOG signal which comes up in Phase 1 if an I/O instruction. The last enabling input to MC44C is $\overline{\text{IOGE}}$ which is derived from MC34A. This gate is normally enabled unless one of three conditions exist:

a. the IAK FF is set or

b. the SC is 01 or

c. the Memory Protect Control FF is reset ($\overline{\text{MPC}}$)

If one of these three conditions exist, then MC34A is disabled and gate MC44C cannot be made. If MC44C cannot be made, then MC44D cannot be made which inhibits any I/O violation interrupt (IOV) signal. This means that if an I/O instruction having SC = 01 is programmed, then no interrupt can occur. If however, the I/O instruction does not reference SC = 01, then MC44D is made and the IOV signal will cause an interrupt.

3-15. Any programmed HLT instruction (HIN) with the MPC FF set (MPC) will make MC15B. This signal is also gated into MC44C to provide a true input to MC44D regardless of the select code used. That is, even with SC = 01, the (HIN) (MPC) signal (which is not gated with MC34A) will cause an interrupt.

3-16. The I/O Logic provides several signals used elsewhere on the board:

a. The T4 GEN FF is toggled at the end of T3 and provides a pseudo T4 timing signal to the Register Control Logic which strobes data into the Violation Register.

b. The IAK FF is used to acknowledge an interrupt. It is normally reset at T5 of an interrupt phase by the SIR signal (Service Interrupt Request). The IAK FF must be reset to make MC44D and issue an I/O violation signal. When set, this IAK FF issues an IAC (Interrupt Acknowledge Clear) signal via MC43C to reset the IRQ FF in the Interrupt Control Logic.

c. The (IOG) (T3) (TS) (HIN + $\overline{\text{IOGE}}$) signal which enables MC44D is also routed to the Register Control Logic as the VRCE (Violation Register Clock Enable) signal. This strobes data into the Violation Register.

d. Gate MC25A provides the Select Code 05 signal for several other logic sections.

3-17. MASTER CONTROL LOGIC

3-18. The purpose of the Master Control Logic is to initialize the Memory Protect Option. The MPC FF acts as the Control FF in the I/O configuration. The POPIO signal is gated through MC65B to reset the MPC FF at power turn on. Thereafter, the MPC FF can be turned off only by the IAC signal from the IAK FF in the I/O Protect Logic. The Memory Protect Option is turned on with a STC 05 instruction. The STC signal is gated with SC 05 through MC75B to set the MPC FF. The MPC signal is routed several places:

a. To the Parity Error Option board via pin 25.

b. To the I/O Protect Logic previously described.

c. To the Register Control Logic to clock the Violation Register.

d. To the Memory Reference Protect Logic to gate the Memory Reference Violation signal (MRV).

The HIN and SIR signals are routed straight through and have no effect on the Master Control Logic.

3-19. REGISTER CONTROL LOGIC

3-20. The purpose of the Register Control Logic is three-fold:

a. It clocks the Violation Register.

b. It clocks the Fence Register

c. It strobes the data out of the Violation Register when an interrupt occurs. Gate MC104B provides the latching input to the Violation Register. This gate is made under one of two conditions:

a. (IOG)(T3)(TS)(HIN + $\overline{\text{IOGM}}$)

b. (PH1)(T4)(HIN)(MPC)($\overline{\text{IF}}$)

The Fence Register clock is provided by MC85A. This gate is made when an OTA/B 05 instruction is programmed. The VR Output Enable signal strobes the Violation Register into the A or B Register (via the IOBI buses) when a LIA/B 05 instruction is programmed. Gate MC85B is used for this purpose.

3-21. VIOLATION REGISTER LOGIC

3-22. The purpose of the Violation Register Logic is to compare the M Register address with the Fence Register address and provide a Memory Violation signal (MEV) if the input address is "below" the fence. This signal (MEV) will then enable the interrupt circuit. The Violation Register Logic is comprised of a

Violation Register which stores the M Register address; a Fence Register which stores the fence address; and a Summing Network which tests for address violations.

3-23. The Fence Register is loaded with an OTA/B 05 instruction at T4 when IOO comes up and makes MC85A (FRC) in the Register Control Logic. Any subsequent memory reference instruction falling below the fence will result in the Summing Network issuing a MEV (Memory Violation) signal. The MEV signal is sent to the Jump Protect Logic and Memory Reference Protect Logic to initiate an interrupt. In the meantime, at T3 (for IOG instructions) or T4 (for memory reference instructions) the Violation Register will be loaded with the violating address (VRC). Then at T5 of the memory cycle following the interrupt phase (when IOI comes up) the Violation Register will be strobed into the A or B Register with a LIA/B 05 instruction (VROE).

3-24. The switches shown on Figure 3-3 prevent memory violation wrap-around. That is, with a 4K machine an input address falling below a fence in the upper 8K region will not cause an interrupt since all switches will be off. If an 8K machine, then the Bit 12 switch would be on and any violations of fences in the upper 8K region would be detected.

3-25. The Summing Network is simplified in Figure 3-2. This network is an adder but the sum outputs are not used. That is, the carry outputs only are required for our purposes. These carry outputs are labeled A, B, C and D. Notice that when carry D is true, it is inverted providing a false MEV signal. When carry D is false, it is inverted and provides a true MEV signal. The Summing Network operates as follows:

a. The M Register address is complemented by the Fence Register. Then a 1 (+4.5v) is added to the complemented value of the fence. In other words, we are subtracting by adding the two's complement of the fence to the address in M.

b. An example will be used to illustrate the logic: suppose a fence of 004000 and an M address of 004001. In this case no violation should occur:

```
  73777    complement of 04000
      1    add 1
  74000
  04001    add M
1 00001    carry is 1
```

When this carry is inverted it provides a false MEV signal which is what we expected.

Now suppose a fence of 04000 and an M address of 03777.

```
  73777    complement of 04000
      1    add 1
  74000
  03777    add M
  77777    no carry
```

With no carry a true MEV signal is enabled.

3-26. INTERRUPT LOGIC

3-27. The purpose of the Interrupt Logic is to cause an interrupt to a trap cell location: when an I/O instruction not referencing SC 01 is detected (IOV); when a Memory Reference instruction has addressed a protected area of core (MRV); when a JMP instruction references a protected area of core (JMV); or whenever a HLT instruction has been programmed (IOV). The trap cell instruction will normally be a LIA/B 05 instruction which will load the Violation Register into the A or B Register. Of course, any set of instructions may follow this instruction in the subroutine.

3-28. The Interrupt FF acts as the flag. It is reset (cleared) by POPIO at power turn on or IAC after an interrupt. It can be set by any of three violation signals:

a. IOV

b. MRV

c. JMV

Gate MC44A can be made by any of these signals unless a Phase 5 operation is in effect. In this case, MC54B inhibits MC44A. When the Interrupt FF sets, it provides one true input to MC75A. With a true PRH input (at pin 38) MC75A is made at T5 when SIR comes true. This output sets the IRQ FF (MC64). The set output from MC64B is then gated through MC63A as the IRQ5 signal and MC15A and MC75B as the INT (Interrupt)signal. Note that the INT signal is gated with the $\overline{PH5}$ signal so no interrupt can occur when in Phase 5 (DMA).

3-29. The IRQ FF is initially reset by one of three signals:

a. IAC

b. POPIO

c. T2

The T2 FF is set on the trailing edge of T1 and reset on the leading edge of T3.

3-30. JUMP PROTECT LOGIC

3-31. The purpose of the Jump Protect Logic is to detect programmed jumps into protected areas of core. The Jump Protect FF is reset at every T3 (P123) via MC22D or on every IAK at T1 following an interrupt phase. It is set on a JMP instruction at T4 (P123) via MC25C. If the Jump instruction references a protected area of core, a MEV signal will be generated in the Summing Network and, during Phase 1, MC55C will be made issuing a Jump Violation (JMV) signal.

3-32. MEMORY REFERENCE PROTECT LOGIC

3-33. The purpose of the Memory Reference Protect Logic is to test for Jump Violation signals (JMV) and the AAF or BAF functions (remembering that accesses to locations 0 and 1 are legal). This logic also tests to see if memory is actually being violated; that is, it checks the MWL signal before allowing an interrupt (no interrupts occur during ASG or SRG instructions because memory is not referenced and MWL is inhibited). Gate MC55A tests the JMV, AAF, BAF and MWL signals. Gate MC45A gates MEV with T1TS to provide the (MRV + JMV) signal.

3-34. INHIBIT LOGIC

3-35. The purpose of the Inhibit Logic is to disable the I Register when a Memory Protect Violation occurs. The IIR FF controls this function. The RSDS FF is used to reset the double-store logic on the EAU board. The IIR FF is reset on the trailing edge of T7TS via MC23D. The IOV + MRV + JMV signal directly sets the flip-flop. When set, the IIR FF issues an IIR signal via MC83D and a P123 signal via MC83A (remembering the IOV + MRV + JMV signal is enabled at T3T4. The RSDS FF issues the RSDS (Reset Double Store) signal and a pseudo MWL signal. The pseudo MWL signal ensures that the (IOV + MRV + JMV) signal will remain true if the interrupt references a subroutine in the protected area of core.

3-36. INDIRECT PROTECT LOGIC

3-37. The purpose of the Indirect Protect Logic is to keep a count of the number of indirect levels referenced. That is, only two indirect phases (Phase 2) are allowed. An interrupt, however, is not forced. The Indirect Counter (MC13 and MC14) is cleared to zero at every Phase 1 via MC63C. At PH2 and SIR (T5) the counter is set. After three pulses via MC23B, gate MC23A is made. This enables the $\overline{IR15}$ signal true which inhibits the I Register.

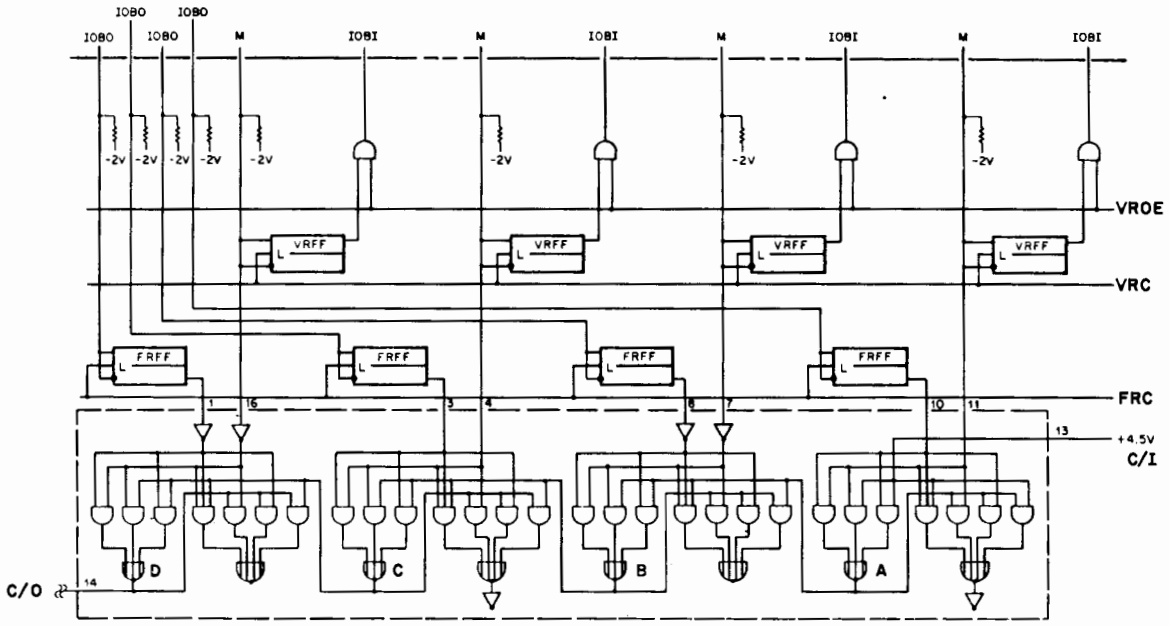


Figure 3-2. Memory Protect Summing Network

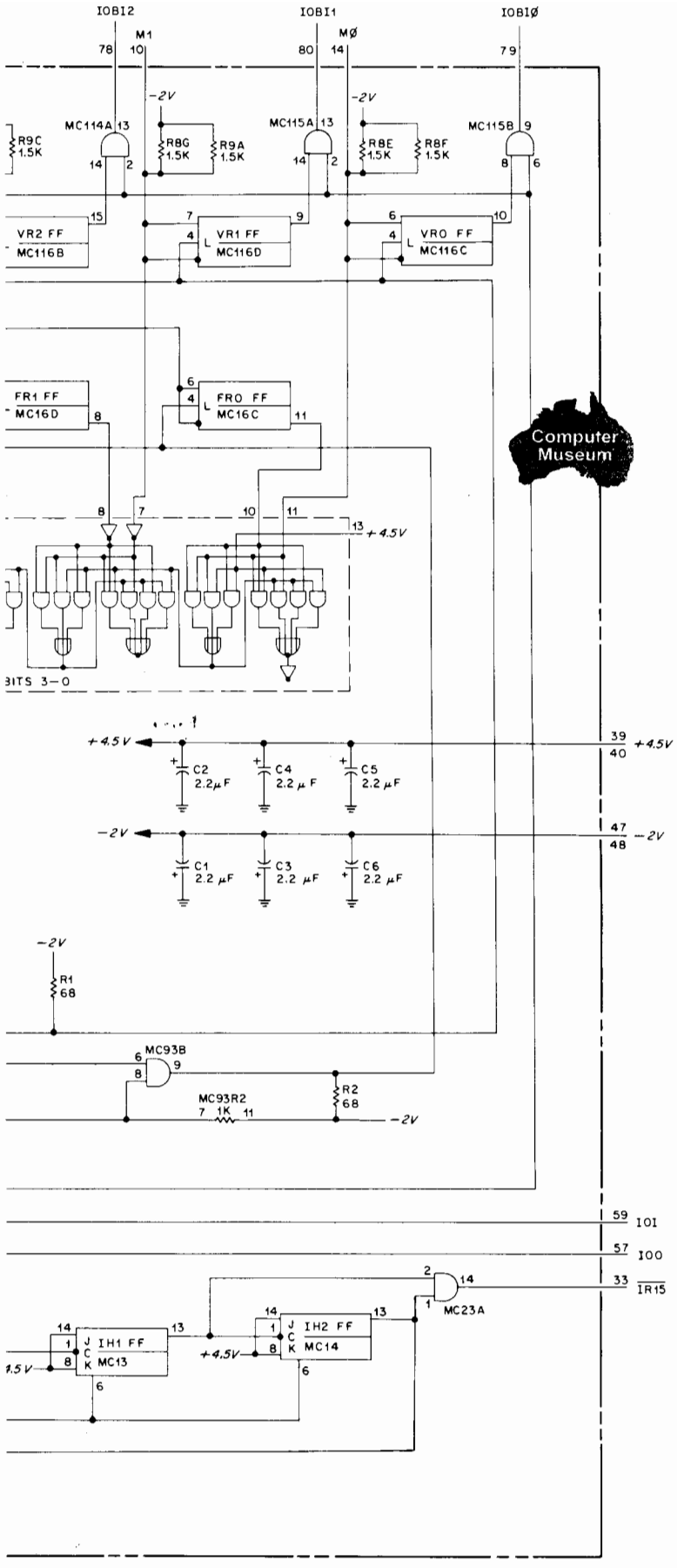
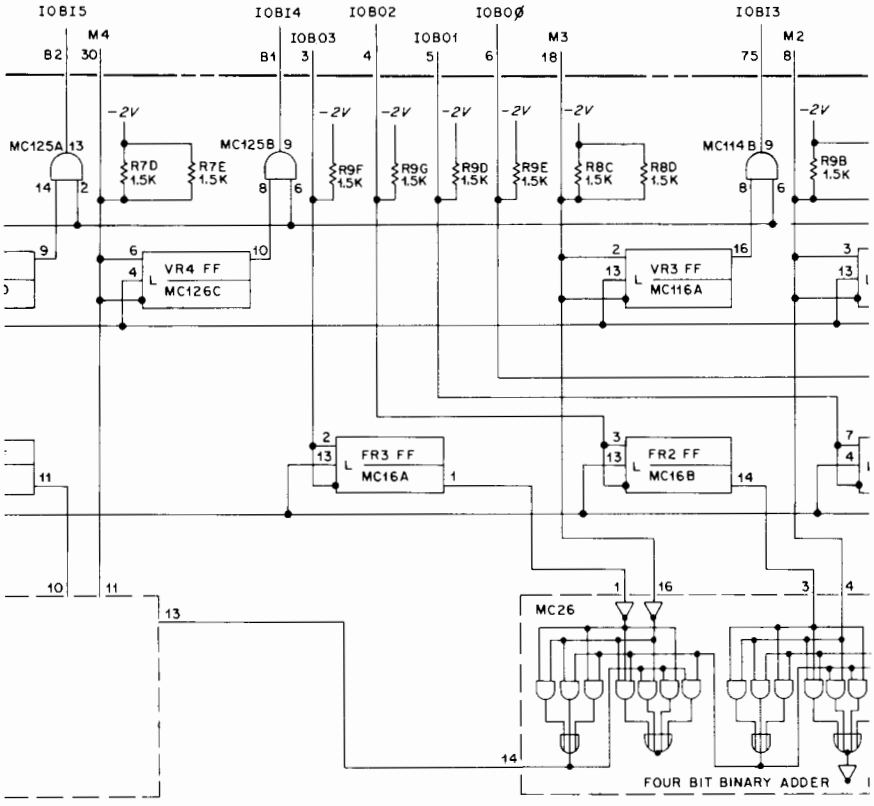


Figure 3-3. Memory Protect Logic Diagram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IOBO2
IOBOØ
IOBI3
IOBO3
IOBO1
M4
M3
M2
B2
B1
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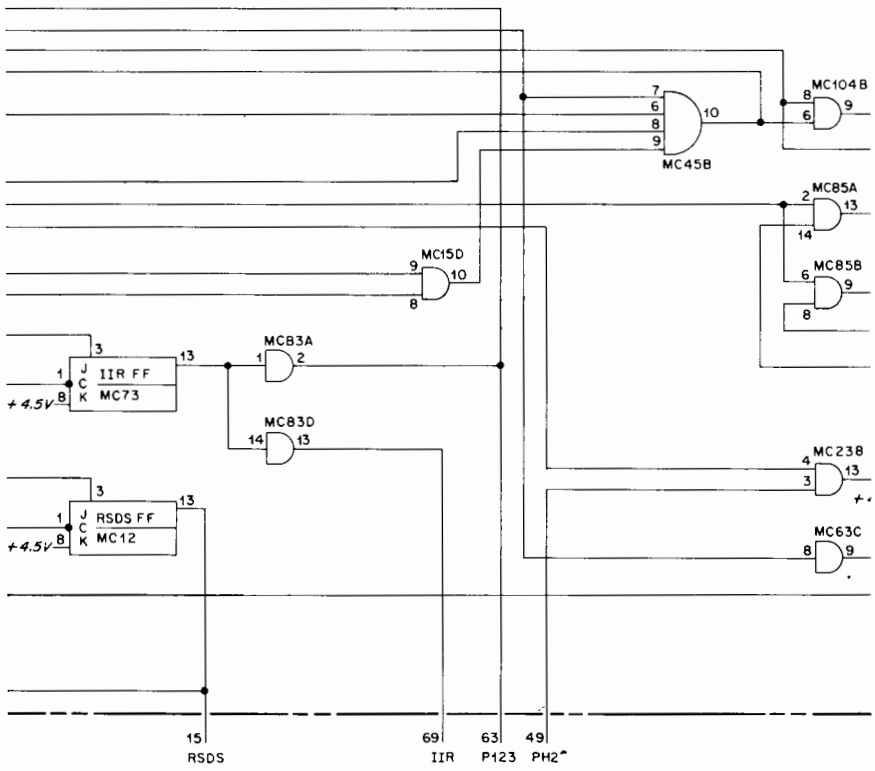
MC125B
MC114B
R7D 1.5K
R7E 1.5K
R9F 1.5K
R9G 1.5K
R9D 1.5K
R9E 1.5K
R8C 1.5K
R8D 1.5K
R9B 1.5K
VR4 FF
MC126C
VR3 FF
MC116A
FR3 FF
MC16A
FR2 FF
MC16B
MC26
FOUR BIT BINARY ADDER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MC85A
MC85B
MC15D
MC83A
MC83D
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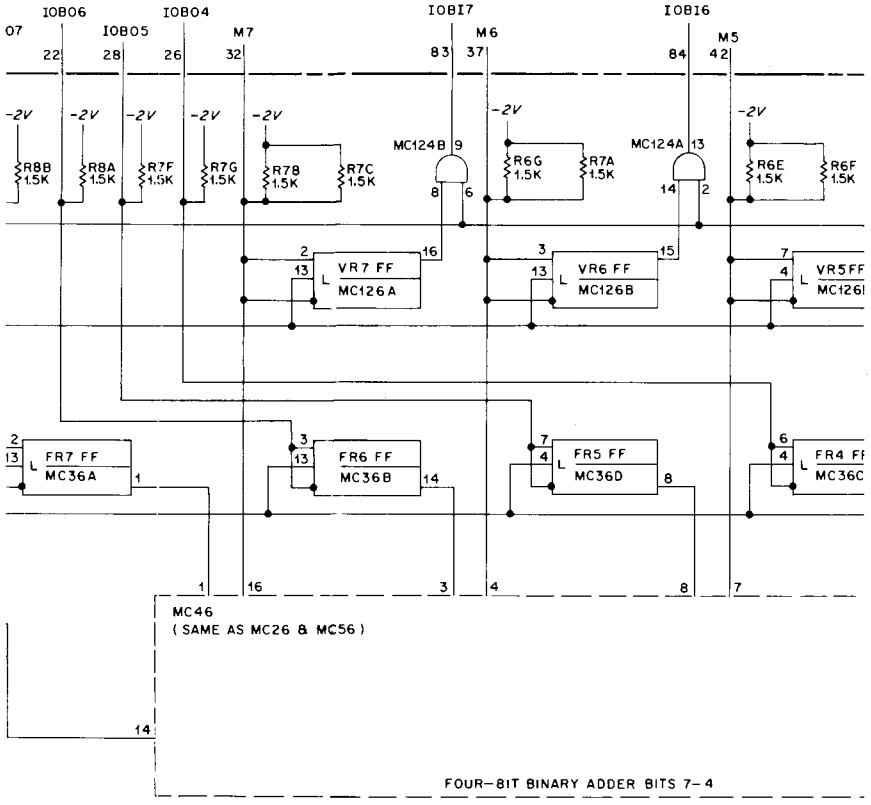
MC63C
+4.5V
RSDS
IIR
P123
PH2*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IOB05
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IOBI7
M6
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R7B 1.5K
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VR7 FF
MC126A
VR6 FF
MC126B
VR5FF
MC126
FR7 FF
MC36A
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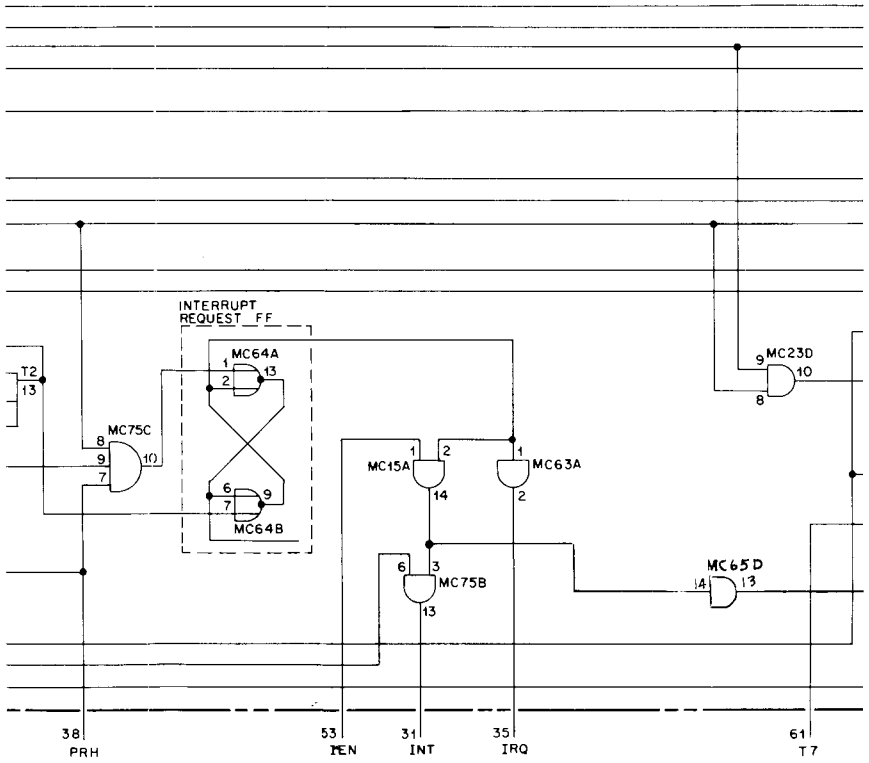
MC36C
MC46
(SAME AS MC26 & MC56)
FOUR-BIT BINARY ADDER BITS 7-4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MC64A
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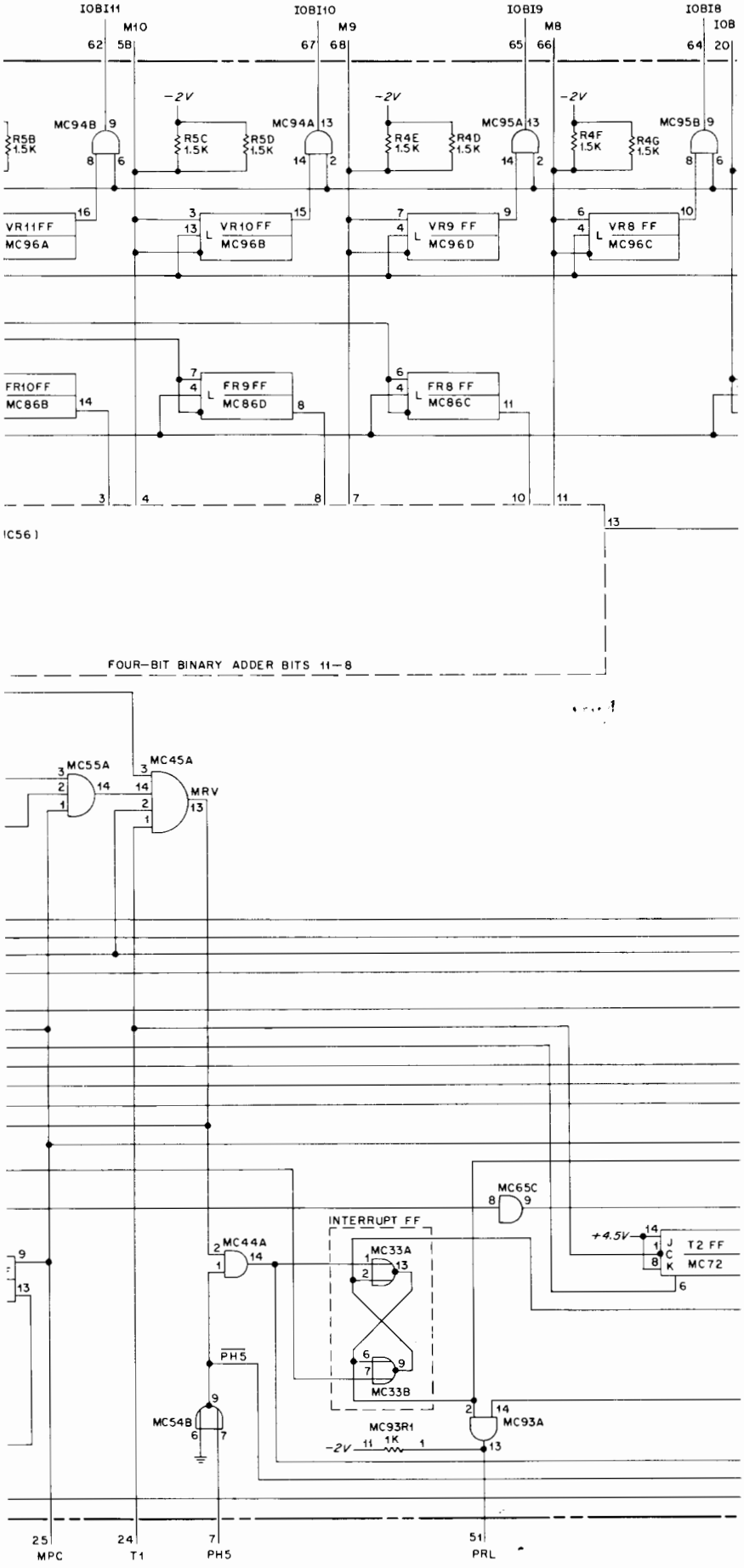
T7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58
IOBI10
M9
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68
IOBI9
M8
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66
IOBI8
IO8
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-2V
MC94B
MC94A
MC95A
MC95B
R5B 1.5K
R5C 1.5K
R5D 1.5K
R4E 1.5K
R4D 1.5K
R4F 1.5K
R4G 1.5K
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VR10FF MC96B
VR9 FF MC96D
VR8 FF MC96C
FR10FF MC86B
FR9FF MC86D
FR8 FF MC86C
IC56)
FOUR-BIT BINARY ADDER BITS 11-8
MC55A
MC45A
MRV
MC65C
INTERRUPT FF
MC44A
MC33A
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MC93A
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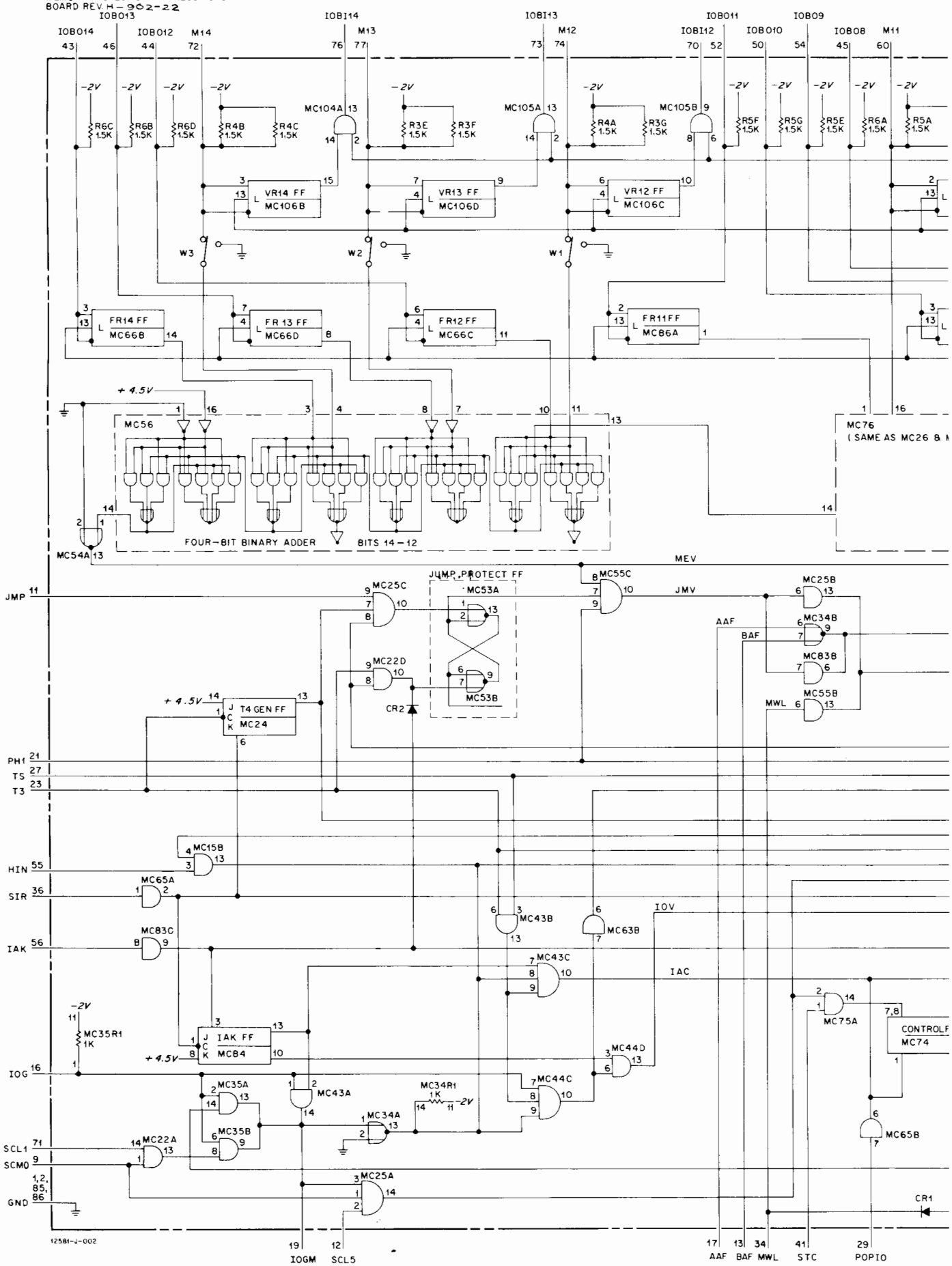
24 T1
7 PH5
51 PRL


MEMORY PROTECT OPTION 12581-6001-S
BOARD REV. H – 902-22
IOBO13
IOBO14
IOBO12
M14
IOBI14
M13
IOBI13
M12
IOBO11
IOBI12
IOBO10
IOBO9
IOBO8
M11
MC104A
MC105A
MC105B
R6C 1.5K
R6B 1.5K
R6D 1.5K
R4B 1.5K
R4C 1.5K
R3E 1.5K
R3F 1.5K
R4A 1.5K
R3G 1.5K
R5F 1.5K
R5G 1.5K
R5E 1.5K
R6A 1.5K
R5A 1.5K
VR14 FF MC106B
VR13 FF MC106D
VR12 FF MC106C
W3
W2
W1
FR14 FF MC66B
FR13 FF MC66D
FR12FF MC66C
FR11FF MC86A
+4.5V
MC56
FOUR-BIT BINARY ADDER
BITS 14-12
MC54A
MC76
(SAME AS MC26 &
MEV
JUMP PROTECT FF
MC53A
MC53B
MC25C
MC22D
MC55C
JMV
MC25B
MC34B
MC83B
MC55B
AAF
BAF
MWL
CR2
T4 GEN FF MC24
JMP
PH1
TS
T3
HIN
SIR
IAK
IOG
SCL1
SCM0
GND
MC15B
MC65A
MC83C
MC43B
MC63B
IOV
MC43C
IAC
MC35R1 1K
IAK FF MC84
MC44D
MC35A
MC35B
MC43A
MC34R1 1K
MC34A
MC44C
MC22A
MC25A
MC75A
CONTROLF MC74
MC65B
CR1
12581-J-002
IOGM
SCL5
AAF
BAF
MWL
STC
POPIO

VOLUME VI

MEMORY PARITY CHECK

CONTENTS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

1-2. DESCRIPTION

1-3. The Memory Parity Check Option provides the HP 2116B Computer with "odd" parity (an odd total of true bits, including the parity bit, in each computer word in memory). This option also monitors the parity of all words transferred from the computer memory. If a bit (or any number of bits) is either added or dropped in the transfer process, a parity "error" signal is generated to either interrupt or halt computer operation. The interrupt is to memory location 05. Installation of the option is easily accomplished in the field with one plug-in Parity Error printed circuit board (12591-6001). This board is installed at the Hewlett-Packard factory when the option is ordered as part of the initial computer system For subsequent installation, the same option is obtainable as Field Kit HP12591A.

1-4. INSTALLATION AND OPERATION

1-5. INSTALLATION

1-6. To install the Memory Parity Check Option, do the following:

a. Make certain that the computer POWER switch is in the "off" position.

b. Remove the jumper on the I/O Control card (A201) labeled W3.

c. Install the Parity Error printed circuit board in slot A3 of the HP 2116B computer. Make certain that the components mounted on the board face to the right as you face the front of the computer.

d. Switch computer POWER on. The parity bit (Bit 16) of each computer word will now be automatically set to the correct value for "odd" parity when the programs are reloaded.

1-7. OPERATION

1-8. Operation of the Memory Parity Check option is completely automatic during normal computer operation and requires no special attention of the computer user. The option may be operated with either the Parity Error Interrupt function or the Parity Error Halt function enabled as determined by the position of the switch S1, which is mounted on the Parity Error card. If a parity error appears during computer operation, it is recommendable to reload the complete computer program before resuming normal computer operation. However, it is also possible to continue computer operation without reloading the program (see paragraph 2-12).

1-9. Any programs stored in memory (including the loader program) before the option is installed must be reloaded, after installation of the option, to initialize the parity bit. This must be done even if the computer is run only temporarily for any time without the Parity Error card installed. The parity of the Basic Binary Loader can be initialized by stepping through its memory locations with the DISPLAY MEMORY pushbutton.

SECTION II

PROGRAMMING

2-1. PROGRAMMING MODES

2-2. GENERAL

2-3. The HLT - INT switch (S1) on the Parity Error Board (A3) selects one of two operating modes:

a. Interrupt Mode

b. Halt Mode

These modes are described in paragraphs 2-4 and 2-7 respectively.

2-4. INTERRUPT MODE

2-5. The interrupt capability of the Parity Error Interrupt card is enabled when computer power is turned on and, unlike external I/O devices, does not have to be initialized by the computer program. However, if desired by the computer user, the interrupt capability of the Parity Error Interrupt card may be re-initialized by program control following the occurrence of a parity error interrupt by use of a STF 05 instruction.

2-6. With switch S1 in the down position the Interrupt function of the Parity Error card is enabled. With the Interrupt function enabled, the Parity Error card will cause the computer program to interrupt to memory location 00005 (octal) if a parity error should appear during operation. (Memory location 00005 may contain any type of instruction as desired by the computer user.) If the Memory Protect option is not installed in the computer and a parity error appears, it is necessary to use the program listing in order to determine at what memory location the parity error occurred. By inserting a LDA XXX instruction (Load A Register with the first word of the interrupt subroutine; i.e., with the program address from which the Parity Error card interrupted) within the interrupt subroutine, it is possible to determine the contents of the P Register when the parity error occurred. This assumes that a JSB instruction is used in location 00005 and that the error location does not contain a JMP instruction. If the Memory Protect option is installed in the computer and a parity error appears, the computer memory location at which the parity error occurred is stored in the Violation Register on the Memory Protect card. By inserting the LIA/B 05 instruction (Load Input into A/B Register, from Select Code 05 in the interrupt subroutine, the location of the parity error is presented to the computer user in the A/B Register.

2-7. HALT MODE

2-8. When switch S1 on the Parity Error card is in the up position, the Halt function of the option is enabled. If a parity error occurs with switch S1 in this position, the Parity Error card will cause the computer to halt, as indicated by the illumination of the PARITY HALT lamp on the computer front panel. In this case the option does not cause an interrupt of the computer program but, rather, halts at the location following the error location.

2-9. PROGRAMMING

2-10. INTERRUPT MODE

2-11. Table 2-1 provides a sample interrupt subroutine; a JSB instruction referencing this routine is assumed to be stored in location 00005.

-NOTE-

If both Memory Protect and Memory Parity Check options are used simultaneously in the computer, it will be necessary to distinguish which type of error is responsible for occurrence of an interrupt. This is because these two options share Select Code 05. If, after the LIA 05 instruction, bit 15 of the A Register is a 1, the interrupt was caused by a parity error; if a 0, the interrupt was caused by a memory protect violation. The SSA instruction in the subroutine is used for checking.

TABLE 2-1. SAMPLE PARITY INTERRUPT SUBROUTINE

LABEL	OPCODE	OPERAND	COMMENTS
MPPE	NOP		Memory Protect/Parity Error Subroutine
	CLF	0	Turn off Interrupt System to inhibit I/O devices
	CLC	5,C	Turn off P.E. interrupt during subroutine
	STA	SVA	Save A-Register
	STB	SVB	Save B-Register
	LIA	5	Get contents of Violation Register on MP card
	SSA		Check bit 15 to determine kind of error
	JMP	PERR	If a 1, go to Parity Error Routine
	JMP	MPTR	If a 0, go to Memory Protect Routine
MPTR	-		User's routine in case of Memory Protect violation
	-		
	-		
	etc.		
	-		
	-		
	-		
	LDA	SVA	Restore A-Register
	LDB	SVB	Restore B-Register
	STF	5	Turn on Parity Error interrupt
	STC	5	Turn on Memory Protect interrupt
	JMP	MPPE,I	Exit the subroutine
PERR	-		User's routine in case of parity error
	-		
	-		
	etc.		
	-		
	-		
	-		
	JMP	PERR-5	Restore accumulators, turn on interrupts, exit

2-12. At this point it may be desirable to continue the program in operation without reloading the complete computer program. Use the following procedure:

a. Using the data obtained in paragraph 2-6, determine what operations have taken place during the execution of the instruction that experienced the parity error. Affected memory locations may be checked, and any errors may be corrected by loading the proper information into respective memory locations. It may also be necessary at this point to correct the software, if it is affected by the error.

b. Normal computer operation may now be resumed.

2-13. HALT MODE

2-14. After a parity halt, it is recommended that the entire program be reloaded. However, it is also possible to continue the program without reloading as follows:

a. First ensure that the instruction executed during the parity error has not altered the contents of any of the registers or memory locations that affect program operation. To do this, read the information contained in the T Register as visible on the computer front panel and check the phase status of this information. By using this data and a program listing it is possible to determine what operations have taken place during the execution of the information contained in the memory location that had the parity error. Affected memory locations may now be checked, and any errors may be corrected by loading the proper information into respective memory locations.

b. After reloading the program or correcting the parity error of the original program, normal computer operation may be resumed.

SECTION III

THEORY OF OPERATION

3-1. GENERAL

3-2. BASIC OPERATION

3-3. In order to ensure that the total number of true bits in each computer word is always odd, it is necessary to control the value (true or false) of the parity bit. The Parity Error card does this by monitoring the T Register bits to determine if each computer word (16 bits plus the parity bit), transferred from the memory, has an odd number of true bits. If even parity is detected, an error signal is generated on the Parity Error card which interrupts or halts computer operation, as determined by the position of switch S1 on the Parity Error card. A simplified Parity Calculating Network is shown in Figure 3-1.

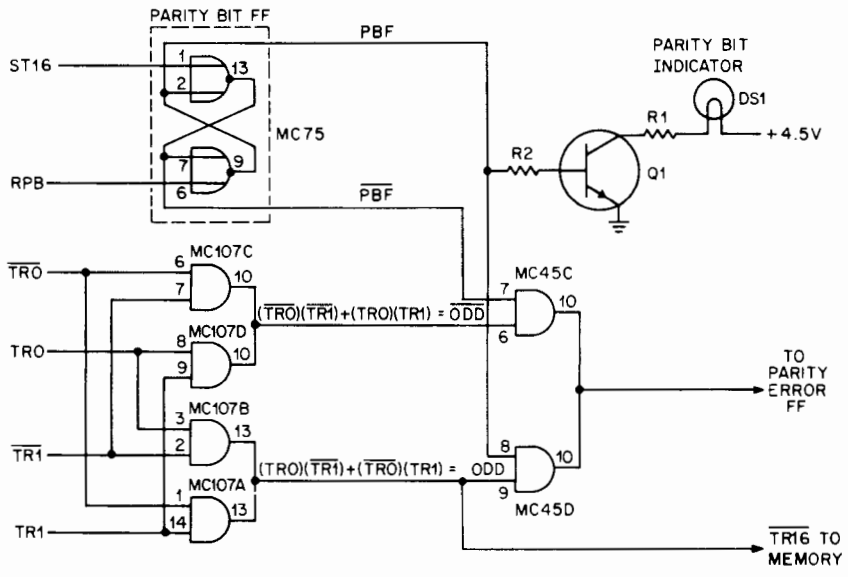


Figure 3-1. Simplified Parity Calculating Network

3-4. PARITY CALCULATING NETWORK

3-5. The purpose of the Parity Calculating Network is to determine whether the sum of all true bits in the T Register is odd or even, during both read and write operations. It produces two complementary output signals, representing the odd or even sum of all true bits in the T Register. These are applied to Error Detect gates MC45C and MC45D as check signals during read operations. One of these signals is also used, during write operations, to control the parity bit $(\overline{TR16})$.

3-6. In order to simplify explanation of the Parity Calculating Network, Figure 3-1 has been provided to show its basic operation by using only four input signals. The resulting two output signals signify whether the sum of true bits in a hypothetical 2-bit T Register is odd (ODD) or even ($\overline{\text{ODD}}$). These signals are representative of the two complementary output signals described above for the 16-bit T Register (paragraph 3-5).

3-7. Refer to Figure 3-1 while reading the following circuit explanation. In Figure 3-1, "and" gate MC107C in the Calculating Network receives the $\overline{\text{TR0}}$ and the $\overline{\text{TR1}}$ signals from the T Register as input signals. If both of these signals are true, there will be a true output on the $\overline{\text{ODD}}$ line to pin 6 of "and" gate MC45C, indicating that there is an even number of true bits in the T Register (00) and that the parity bit must be true in order to provide "odd parity". Similarly, "and" gate MC107D will drive the $\overline{\text{ODD}}$ line true if the TR0 and TR1 signals are both true, again indicating an even number of true bits in the T Register (11) and that the parity bit must be true in order to provide "odd parity". On the other hand, "and" gates MC107B and MC107A drive the ODD line true when the contents of the hypothetical T Register are 01 or 10 indicating that the parity bit must be false in order to provide "odd parity". The ODD and $\overline{\text{ODD}}$ signals are then applied to the Error Detect gates (MC45C and MC45D) where they are compared to the output signals of the Parity Bit Flip-Flop, MC75.

3-8. The Error Detect gates, MC45C and MC45D, act as a comparison network between what the T Register contents indicate the parity bit should be (the ODD and $\overline{\text{ODD}}$ lines) and the actual state of the Parity Bit Flip-Flop (the PBF and the $\overline{\text{PBF}}$ lines). To do this, the output signal of the parity bit Sense Amplifier, ST16, is applied to Parity Bit flip-flop MC75. This signal, if true, sets the flip-flop and is applied as a true PBF signal to pin 8 of "and" gate MC45D, and as a false $\overline{\text{PBF}}$ signal to pin 7 of "and" gate MC45C. With a true $\overline{\text{ODD}}$ signal from the parity calculating network applied to pin 6 of MC45C (indicating the need of a true parity bit, due to an even number of true bits in the T Register) the PBF signal must be false to prevent an error signal out of MC45C. Similarly, if the ODD signal were true (indicating the need of a false parity bit, due to an odd number of true parity bits in the T Register), the PBF signal must be false to prevent an error signal out of MC45D. Also, if $\overline{\text{PBF}}$ is true, $\overline{\text{ODD}}$ must be false; or if PBF is true, ODD must be false. If a parity error appears, indicating that a bit has been dropped or picked-up in a computer memory word or that the parity bit is incorrect, the two input signals to one of the two Error Detect gates (MC45C and MC45D) will be true and will then cause a true Error signal to be applied to the Parity Error flip-flop.

3-9. PARITY BIT INDICATOR

3-10. The PBF signal, representing the "true/false" state of the parity bit in the 2-bit T Register, is also applied through resistor R1 to the base of transistor Q1. If the parity bit is "true", (PBF to the base of transistor Q1 is true), transistor Q1 conducts and the Parity Bit Indicator Lamp DS1 illuminates. If the parity bit is "false" (PBF false at the base of transistor Q1), transistor Q1 does not conduct and the Parity Bit Indicator Lamp DS1 does not illuminate. Thus, by observing the illumination of Parity Bit Indicator DS1, the computer user may determine the "true/false" state of the parity bit of each computer word while stepping the computer (by use of the SINGLE CYCLE or DISPLAY MEMORY buttons) through the desired memory locations. Note, however, that since parity is checked while reading (not while writing) the light indication following execution of STA/B, JSB, or ISZ instructions is not valid. In the cases of STA/B and JSB, the light remains off regardless of the word stored (signal MWL inhibits an error indication); in the case of ISZ, the word is incremented after reading and checking.

3-11. THEORY OF OPERATION

3-12. ERROR SIGNAL

3-13. The Parity Error Interrupt card is given as Figure 3-2. The following paragraphs implicitly reference that drawing.

3-14. Table 3-1 summarizes the functions of command lines to Parity Error and Memory Protect cards. When two true signals are simultaneously applied as inputs to either of the two Error Detect gates (MC45C and MC45D), a true output Error Signal is then applied to pin 4 of "and" gate MC45B (and also to pin 1 of "and" gate MC35A). With the true Error signal at pin 4, it is then necessary that "and" gate MC45B receive a true signal at pin 3 before it is enabled. In order for the signal at pin 3 to be true, the following conditions must first exist:

a. Either the ISZ (Increment and Skip if Zero) signal and the PH3 (Phase 3) signal, applied to pins 44 and 43 respectively of the Parity Error card, must both be true thus causing a true output from "and" gate MC15A, or the MWL (Memory Write Level) signal applied to pin 54 of the Parity Error card must be false causing inverting "or" gate MC25B to apply a true output signal to pin 3 of "and" gate MC15B.

b. Both the AAF (A Addressable Flip-Flop) and the BAF (B Addressable Flip-Flop) signal, pins 1 and 2 respectively of inverting "or" gate MC25A, must be false in order to cause a true signal to be applied to pin 4 of "and" gate MC15B.

c. There must be a true signal applied from inverting "or" gate MC55B to pin 3 of "and" gate MC35A (caused by a false MPT signal at pin 34 of the Parity Error Interrupt card and a false signal from pin 13 of the Parity Error Interrupt flip-flop, MC24).

d. When the conditions described above exist, a true output signal from "and" gate MC35A (during a Phase 1, 2, or 3) is applied to pins 2 and 3 of "and" gate MC64A. Timing signals T3 (input at board pin 23), and TS (pin 17) then will strobe this output to pin 3 of MC45B (as well as three isolation gates, discussed later).

TABLE 3-1. COMMAND LINES TO PARITY ERROR AND MEMORY PROTECT CARDS

COMMAND	USED IN	DESCRIPTION
STC 5	MP	Used to turn on Memory Protect.
STF 5	PE	Enables the interrupt feature on the Parity Error card.
CLF 5	PE	Disables interrupt on the Parity Error card.
IAK	PE	If IRQ 5 was generated by the Parity Error card, IAK will turn off interrupt capability on the card.
	MP	Turns off Memory Protect; clears Control bit
LIA/B 5	PE/MP	Gets contents of MP Violation Register; contains address of parity or memory protect violation, and identification bit (Bit 15) to indicate which kind of error.
IOG, HIN, MPC	MP	Lines to Memory Protect card from Parity Error card, to cause the Violation Register to get the address of any parity error.

3-15. With "and" gate MC45B receiving a true Error signal at pin 4 (paragraph 18) and a true signal at pin 3 (from "and" gate MC13A), this gate is enabled and applies a true output signal to pin 6 of Parity Error flip-flop MC85, setting it. This action causes a true signal to be applied from pin 13 of the Parity Error flip-flop to pin 2 of "and" gate MC34A (to enable the interrupt circuits) and to board pin 61 (Parity Error Halt). The Parity Error Halt function may be disabled by opening switch S1. The PEI signal is applied to the Timing Generator where it causes the PARITY HALT lamp on the computer front panel to illuminate.

3-16. HALT OPERATION

3-17. If switch S1 is in the up (closed) position, the output signal at pin 13 of Parity Error flip-flop MC85 is sent out pin 62 of the Parity Error Interrupt card as the PEH (Parity Error Halt) signal. The PEH signal goes to the Timing Generator and causes the computer to halt before the Parity Error Interrupt circuitry can cause an interrupt.

3-18. PARITY BIT CONTROL

3-19. In order for the ST16 signal at pin 60 of the Parity Error Interrupt card to be representative of the parity bit, the parity bit must first be correctly written into all computer memory locations. To accomplish this, the output ODD signal of the Parity Calculating Network is sent out pin 53 of the Parity Error Interrupt card as the TR16 signal. This signal is then applied to the parity bit Inhibit Driver where it controls the writing (0 or 1) of the parity bit. If the TR16 signal is true, a false parity bit is written into memory. If the TR16 signal is false, a true parity bit is written into memory.

3-20. PARITY ERROR CONTROL

3-21. The MPC (Memory Protect Control) signal is sent out pin 63 of the Parity Error Interrupt card, via isolation gate MC57B, whenever there is a true output from "and" gate MC14A. This signal is then applied to the Memory Protect card, Option 01.

3-22. The HIN (Halt Instruction, decoded) signal is the output signal of "and" gate MC57C and is sent out of the Parity Error Interrupt card at pin 69. This signal is also applied to the Memory Protect card, Option 01, whenever there is a true output from "and" gate MC13A.

3-23. The IOG (Input/Output Group, decoded) signal is input at pin 59 of the Parity Error Interrupt card and is normally caused by any I/O instruction. However, when there is a true output signal from "and" gate MC13A, isolation gate MC105D will send a true signal out pin 59 of the Parity Error Interrupt card. This signal is then applied, via the backplane wiring, to the Memory Protect card where it causes the memory address of the location that has the parity error to be strobed into the Violation Register on the Memory Protect card.

3-24. When the computer power is turned on, or whenever the PRESET button on the computer front panel is pushed, the POPIO (Power On Pulse to the I/O section) signal is applied to pin 45 of the Parity Error Interrupt card. In order to initialize the interrupt capability, the POPIO signal is applied to the following places:

a. Through isolation gate MC14D to pin 2 of Parity Error Interrupt flip-flop MC24. This action initializes, or sets, the flip-flop.

b. Through isolation gate MC14A to pin 1 of PE/MPT Violation flip-flop MC66. This action sets the flip-flop.

c. Through isolation gate MC56B and to pin 1 of Parity Error flip-flop MC85, which resets the flip-flop.

3-25. INTERRUPT OPERATION

3-26. When the POPIO signal is applied to pin 2 of the Parity Error Interrupt flip-flop MC24, it sets the flip-flop, causing a true output signal at pin 9, which is then applied to pin 1 of "and" gate MC34A. The interrupt circuits of the Parity Error Interrupt card now remain in this state, ready to initiate an interrupt if a parity error should be detected by Error Detect gates MC45C and MC45D. If a parity error is detected during normal computer operation, a true Error signal is applied from pin 13 of Parity Error flip-flop MC85 and to pin 6 of PE/MPT Violation flip-flop MC66 and to pin 3 of "and" gate MC56A. With a true input at pin 6, the PE/MPT Violation flip-flop resets and applied a true output signal to pin 9 of "and"

gate MC67C. At the same time, the true output signal from "and" gate MC34A is applied to "and" gate MC56A along with the PRH (5) (Priority High, Select Code 5) signal, from the Power Fail Interrupt card, and the SIR (Set Interrupt Request) signal, from the I/O Control card (see HP 2116B Volume Three, Input/Output System Operation). When all three of these inputs are true, they cause "and" gate MC56A to apply a true output signal to pin 1 of IRQ (Interrupt Request) flip-flop MC95. This action sets the flip-flop and causes a true output at pin 9 which is then sent through isolation gate MC105C to pin 1 of "and" gate MC45A and out of the Parity Error Interrupt card at pin 77 as the IRQ 5 (Interrupt Request, Select Code 05) signal. This signal is then applied to the I/O address card where it is encoded to form the Service Request Address. The true output of the IRQ flip-flop MC95 is also applied to pin 6 of "and" gate MC94B. When the computer is not operating in Phase 5 (PH5), inverting "or" gate MC103A applies a true signal to pin 8 of "and" gate MC94B. When both of these inputs are true, a true output signal is sent out of the Parity Error Interrupt card at pin 79 as the INT (Interrupt) signal. This signal is then applied to the Timing Generator where it causes an interrupt of normal computer operation.

3-27. INTERRUPT IDENTIFICATION

3-28. With PE/MPT Violation flip-flop MC66 applying a true signal to pin 9 of "and" gate MC67C, the computer program must furnish the two other input signals needed to enable the gate. When the parity error occurred and caused an interrupt to memory location 00005 (octal), the instruction contained in location 00005 may tell the computer to execute a subroutine. Contained in the subroutine must be a LIA, MIA, LIB, or MIB instruction which, when executed, causes the IOI signal input at pin 15 of the Parity Error card to be applied to pin 7 of "and" gate MC67C as a true signal. At the same time, execution of one of these instructions also causes the SCM0 (Select Code, Most Significant Digit 0), the SCL5 (Select Code, Least Significant Digit 5), and the IOG signals input at pin 7, 9, and 59 respectively to be applied to "and" gate MC56C as true input signals. This causes a true output from "and" gate MC56C to be applied to pin 2 of "and" gate MC67A and to pin 8 of "and" gate MC67C. With all inputs to "and" gate MC67C true, this gate applies a true output signal through isolation gate MC65B and out of the Parity Error Interrupt card at pin 28 as the IOB115 (I/O Bus Input, bit 15) signal. This signal is then sent to the A or B Register on the Arithmetic Logic card. If the 10BI15 signal is true, it indicates that the interrupt at memory location 00005 was a Parity Error function. If it is false, it indicates that the interrupt at memory location 00005 was a Memory Protect function.

3-29. PRIORITY CONTROL

3-30. When there is not an existing parity error (true input from the Parity Error flip-flop to MC67B) and neither the Power Fail Interrupt card (true PRH5 to MC94A) nor the Memory Protect card (Priority Control flip-flop reset by true RSDS) have requested an interrupt, a true PRH(6)(Priority High, Select Code 06) is sent from pin 27 of the Parity Error Interrupt card to the interface card using Select Code 06. This allows I/O devices using Select Codes of 06 and below (06 through 70) to interrupt normal computer operation. When the PRH(6) signal is false, it inhibits all I/O devices using Select Codes of lower priority (06 through 70) from interrupting. The PRH(6) signal will be false only when the Power Fail Interrupt card, the Memory Protect card, or the Parity Error Interrupt card have requested an interrupt.

3-31. INTERRUPT ACKNOWLEDGE

3-32. At time T1 of Phase 1 (the next machine cycle after the Interrupt phase), the IAK (Interrupt Acknowledge) signal is true. This signal is then applied to pin 9 of "and" gate MC34D and to pin 2 of "and" gate MC45A. With the true output of the IRQ flip-flop MC95 applied to pin **8**, "and" gate MC34D is enabled and applies a true output signal to pin 6 of Parity Error Interrupt flip-flop MC24. This resets the flip-flop after a Parity Error Interrupt. At the same time, the true output from the IRQ flip-flop is also applied to pin 1 of "and" gate MC45A, making the gate true. The true output resets Parity Error flip-flop MC85 (clearing the error indication on the board) and sets Priority Control. Flip-flop MC104 (re-enabling lower priority devices). For this reason, a CLF0 instruction is normally inserted to hold off external devices while in the service routine.

3-33. The CLF (Clear Flag) signal at pin 51 of the Parity Error Interrupt card becomes true when a CLF instruction is executed during the Parity Error Interrupt subroutine program. This signal is applied to pin 7 of "and" gate MC34C. When the signal at pin 6 of "and" gate MC34C (output of "and" gate MC56C) is also true, a true output signal is applied to Parity Error Interrupt flip-flop MC24. This action inhibits the interrupt circuitry during the execution of the interrupt subroutine program.

3-34. The STF (Set Flag) signal at pin 18 of the Parity Error Interrupt card becomes true when a STF instruction is also executed by the interrupt subroutine. This signal is applied, as an input, to "and" gate MC34B along with the true output signal from "and" gate MC56C. This causes a true output signal to set Parity Error Interrupt flip-flop MC24. The STF signal is also applied to pin 1 of "and" gate MC67A where, along with the true output signal of "and" gate MC56C, it causes a true output signal to be applied to PE/MPT Violation flip-flop MC66. This action sets the flip-flop, and the board is then enabled to detect further parity errors.

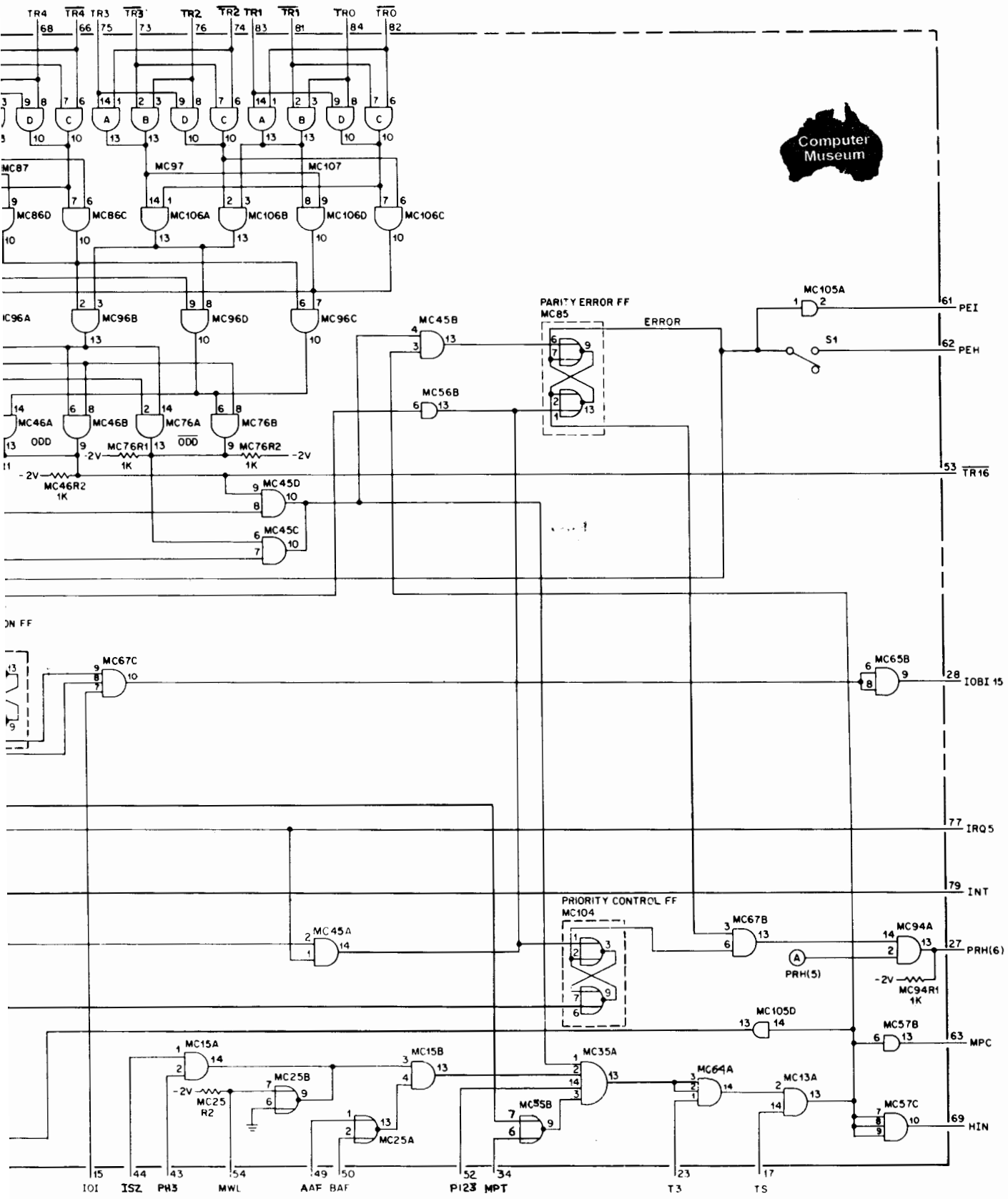
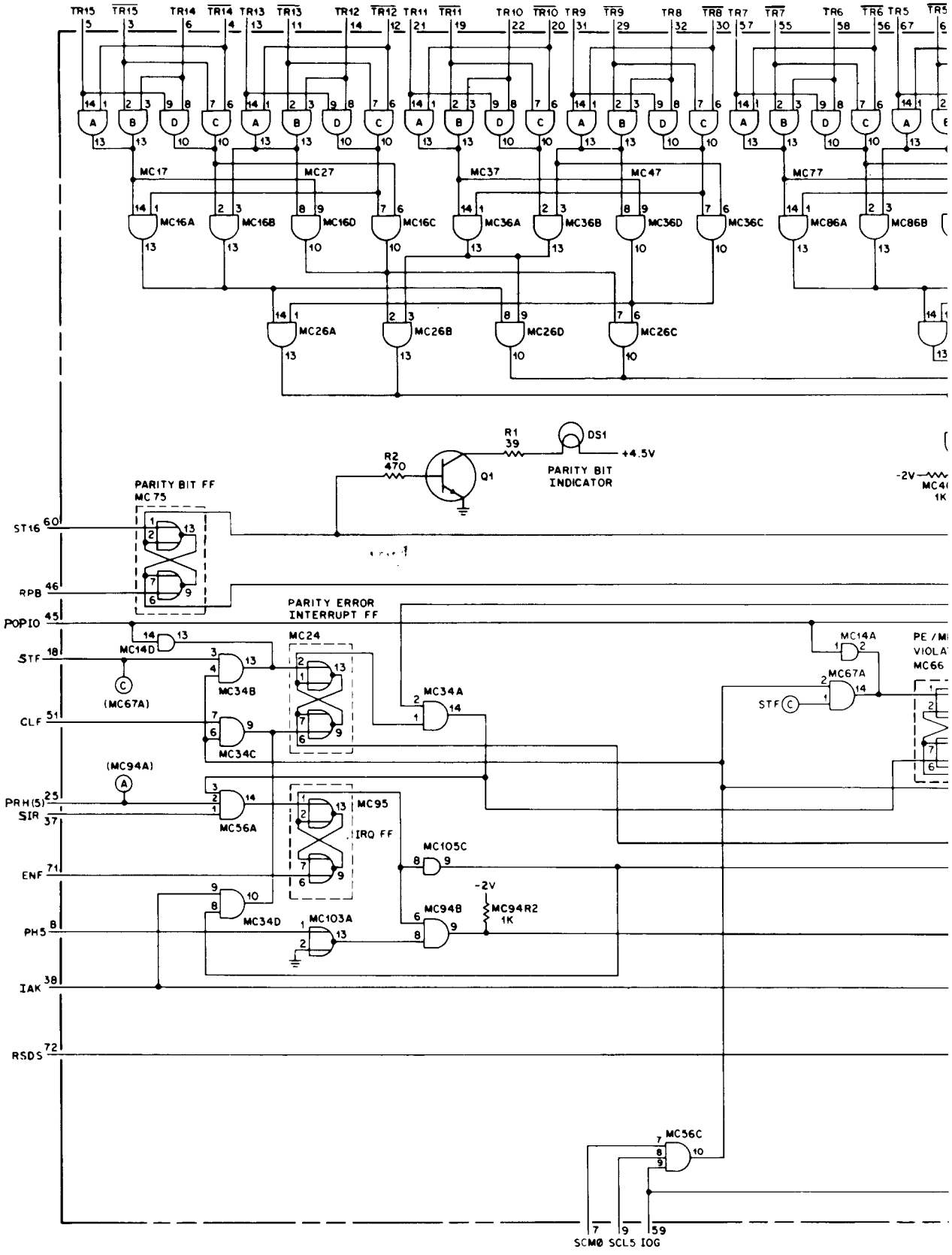


Figure 3-2. Parity Error Interrupt Card


TR15
TR14
TR13
TR12
TR11
TR10
TR9
TR8
TR7
TR6
TR5
MC17
MC27
MC37
MC47
MC77
MC16A
MC16B
MC16D
MC16C
MC36A
MC36B
MC36D
MC36C
MC86A
MC86B
MC26A
MC26B
MC26D
MC26C
R1
39
DS1
+4.5V
R2
470
Q1
PARITY BIT
INDICATOR
PARITY BIT FF
MC75
ST16
RPB
POPIO
STF
CLF
PRH(5)
SIR
ENF
PH5
IAK
RSDS
PARITY ERROR
INTERRUPT FF
MC24
MC14D
MC34B
MC34C
MC34A
MC14A
MC67A
(MC67A)
(MC94A)
MC56A
MC95
IRQ FF
MC105C
MC94B
MC94R2
1K
-2V
MC103A
MC34D
MC56C
SCM0
SCL5
IOG

VOLUME VII

POWER FAIL AUTO RESTART

CONTENTS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

1-2. DESCRIPTION

1-3. The HP 12588A Power Failure Auto-Restart option can save the memory and register contents of an HP 2116B Computer when primary power fails (interrupt) and allow a program to continue from the point of interruption as soon as power is restored (auto-restart). This option utilizes the capacity of the computer to compete 200 memory cycles after a power failure (200 X 1.6μs = 3.2ms). As soon as power drops below a safe operating level, the Power Failure board signals an interrupt request to start an orderly shut down routine that saves addresses, data, and instruction words in registers and memory. The automatic restart feature of this option will restart the computer program automatically or in response to external signals. In addition to protecting a basic HP 2116B Computer, the Power Failure Interrupt option will also protect HP 2116B systems that have the following options: HP 2150B Input/Output Extender; HP 2151A Input/Output Extender; and HP 2160A Power Supply Extender.

1-4. The Power Failure Auto-Restart option consists of a single printed circuit card (Part No. 12588-6001) that plugs into slot A1 in the HP 2116B computer. The board contains the wiring that restarts the computer program automatically or in response to external signals. Environmental specifications for this option are the same as those for an HP 2116B Computer. When included in a purchase order for an HP 2116B Computer the Power Failure Auto-Restart option will be installed at the Hewlett-Packard factory.

1-5. INSTALLATION AND OPERATION

1-6. INSTALLATION

1-7. The Power Fail Auto-Restart option board (HP Stock No. 12588-6001) is installed in slot A1. Proceed as follows:

a. Turn computer power off.

b. Remove the standard Power Fail Interrupt board from A1.

c. Install the Power Fail Auto-Restart board in slot A1.

d. Hold down the PRESET or HALT pushbutton and press the POWER pushbutton.

1-8. OPERATION

1-9. The RESTART/HALT switch, mounted on the front edge of the Power Failure Interrupt With Automatic Restart card, controls the mode of operation. When the switch is in the RESTART position, the complete capability of the option is made available to the computer. In this position, both shutdown and start up routines will initialize automatically. When the switch is in the HALT position, however, the shutdown routine will be initialized automatically as soon as power falls to the threshold voltage, but the computer will then go into a HALT mode as soon as power is restored.

1-10. When Power Failure Auto-Restart is connected for automatic restart, the computer will restart automatically every time the POWER switch is turned on. This can be prevented by a subroutine in memory, or by holding down either the HALT or the PRESET button while turning on the POWER switch.

SECTION II
PROGRAMMING

2-1. GENERAL

2-2. POWER FAIL INSTRUCTION SET

2-3. The Power Fail instruction set is given in Table 2-1. The reaction of Power Failure Auto-Restart to certain input/output instructions differs from that of most input/output channels. When an HP 2116B Computer does not have Power Failure Auto-Restart, a primary power failure will cause the computer to halt. When it does have this option, a primary power failure will cause the option to signal an IRQ (Interrupt Request) to Select Code location 04. If the computer memory does not contain a subroutine to service the IRQ, Select Code location 04 should contain the following instruction: HLT, C04 (103004). If this is done, when power fails the computer will be halted, the restart circuits will be turned off and the PRESET lamp on the front panel will be turned on to indicate a power failure.

2-4. Power Failure Auto-Restart is program-controlled through the interrupt system. So that it will have enough time to save the contents of the computer when power fails, it is given the highest priority in the system, Select Code 04. Unlike other I/O cards used with the system, Power Failure Auto-Restart has no Control Flip-Flop. This prevents inadvertently turning it off with a CLC 04 or a CLF 00 instruction (see Table 2-1). To turn off Power Failure Auto-Restart, first turn off the POWER switch, then set the HALT-RESTART switch (S1) on the circuit board to HALT.

2-5. PROGRAMMING

2-6. PROGRAM CONTROL

2-7. Table 2-2 is a minimal program for the Power Failure Auto-Restart option. If the computer is running and power fails, this program will do the following: save the contents of registers A, B, and P; return the contents after power is restored; and allow the main program to be resumed. If the computer is not running and power fails, this program will protect the register contents in the same way, and then halt the computer.

2-8. A second power failure might occur immediately after a start-up routine has begun. To protect against such an occurrence, there should be enough time remaining at the end of a start-up routine to complete a shut-down routine. The total number of memory cycles in the two routines, start-up and shut-down, should be less than 200. For example, the total should be less than the number of memory cycles in a routine of 50 Memory Reference Instructions (2 cycles each) and 100 Register Reference instructions (1 cycle each).

2-9. When the Flag Flip-flop in Power Fail Auto-Restart is set, all I/O devices are prevented from interrupting, and DMA is prevented from making data transfers.

MNEMONIC & SELECT CODE	DEFINITION AND REACTION IN MOST I/O CHANNELS	MACHINE LANGUAGE	REACTION IN THIS OPTION
CLC 04	CLEAR CONTROL BIT OF SELECTED CHANNEL. RESETS CONTROL FLIP-FLOP OF SELECTED I/O CHANNEL, DISABLING THAT CHANNEL.	106704	Turns on Restart Logic, so that the computer will restart when power is restored
CLF 00	CLEAR FLAG OF SELECTED I/O CHANNEL. DISABLES THE ENTIRE INTERRUPT SYSTEM.	103100	Does not disable Power Failure interrupt.
CLF 04	CLEAR FLAG OF SELECTED I/O CHANNEL. RESETS FLAG FLIP-FLOP OF SELECTED I/O CHANNEL.	103104	Turns off Restart Logic. Does not reset flag flip-flop.
HLT C04	HALT THE PROGRAM, STOPS THE COMPUTER AND CLEARS THE FLAG OF SELECTED I/O CHANNEL.	103004	Turns off restart Logic and stops the computer. Does not clear the flag.
SFC 04	SKIP if FLAG CLEAR. TESTS THE FLAG FLIP-FLOP OF THE SELECTED I/O CHANNEL AND IF IT IS RESET SKIPS TO THE NEXT INSTRUCTION.	102204	Skips to the next instruction if interrupt was caused by power failure. Does not skip if interrupt occurred while power was going back up.
SFS 04	SKIP if FLAG SET THE NEXT INSTRUCTION IS SKIPPED IF THE FLAG FLIP-FLOP OF THE SELECTED I/O CHANNEL IS SET.	102304	No reaction.
STC 04	SET CONTROL FLIP-FLOP SETS THE CONTROL FLIP-FLOP AND ENABLES THE FLAG FLIP-FLOP OF THE SELECTED I/O CHANNEL.	102704	Resets Flag flip-flop, so that when power fails again, another interrupt request will be signaled by Power Failure
STF 04	SET FLAG FLIP-FLOP SETS THE FLAG FLIP-FLOP OF THE SELECTED I/O CHANNEL.	102104	No reaction.

TABLE 2-1. POWER FAIL AUTO RESTART INSTRUCTION SET

```
         ORG   4B
         JSB   SUBR
         ORG   100B

SUBR     NOP
         SFC   4B          Test fail versus restart
         JMP   UP

DOWN     STA   A STR       Save A
         CCA
         STA   AL          Signal that computer was running
         STB   B STR       Save B
         LDA   SUBR

         STA   P STR       Save P
         CLC   4B          Set up for restart when power is up
         HLT
         JMP   UP

UP       LDA   AL
         SZA,  RSS TEST    Was computer running when power failed?
         JMP   NR          No
         CLA               Yes
         STA   AL          Restore signal
         LDA   A STR       Restore A
         LDB   B STR       Restore B
         STC   4B          Set up Power Failure logic for next power failure
         JMP   PSTR, I     Jump back to program

NR       CLF   4B          Turn off restart
         HLT               Was not running when power failed
A STR    OCT   0
B STR    OCT   0
P STR    OCT   0
AL       OCT   0
         END
```

TABLE 2-2. POWER FAIL AUTO RESTART PROGRAM

SECTION III

THEORY OF OPERATION

3-1. GENERAL

3-2. POWER FAILURE DETECTION

3-3. The Power Fail Auto Restart logic is shown in Figure 3-1. A complete circuit schematic is provided as Figure 3-2. The following paragraphs implicitly reference these diagrams.

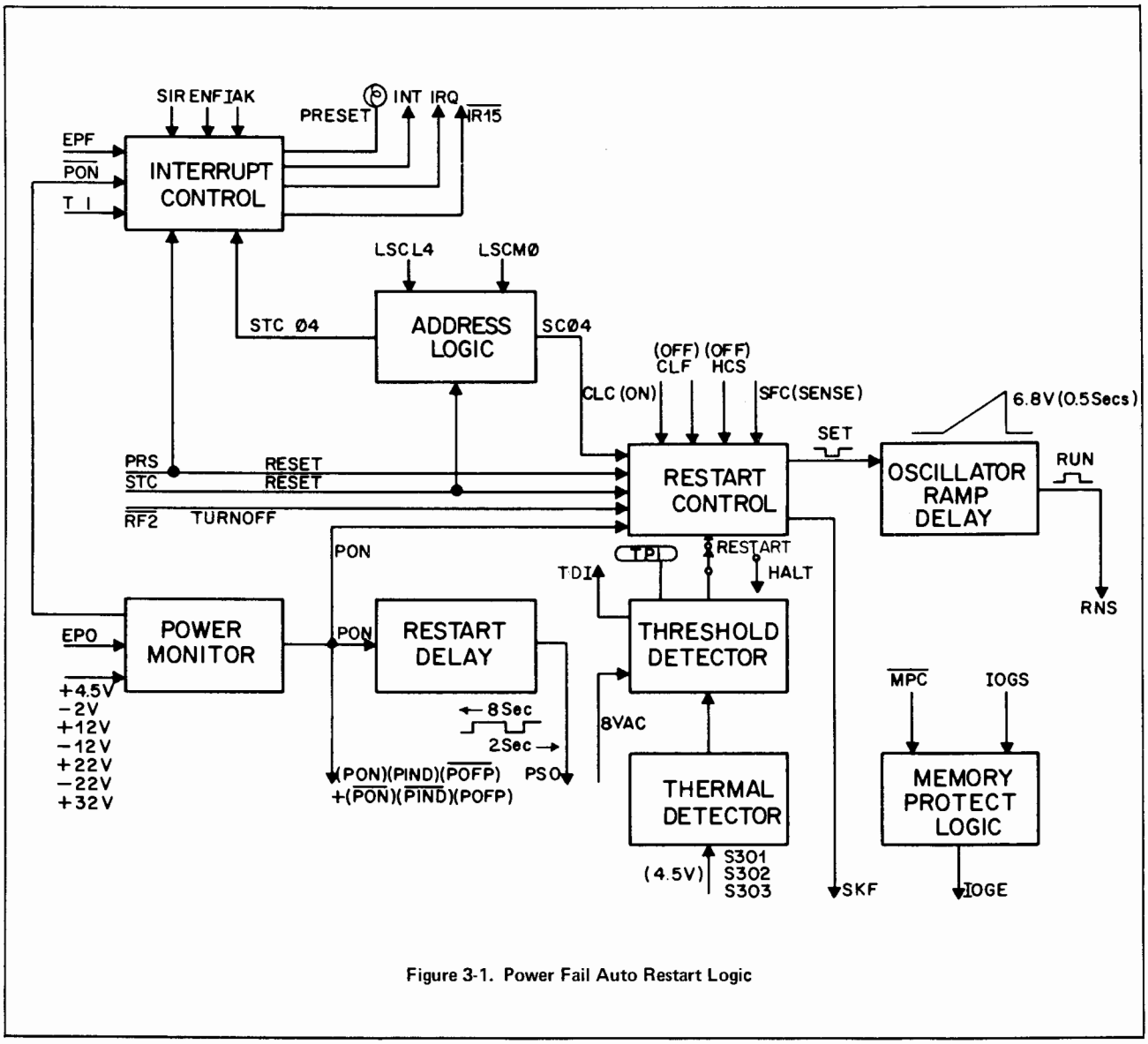


Figure 3-1. Power Fail Auto Restart Logic

3-4. Power failure detection is made up of the Power Monitor, Restart Delay, Thermal Detector and Threshold Detector. The Power Monitor circuit senses all seven regulated supplies in the computer and also the supplies in the Power Supply Extender (HP2160A). When power is normal, the (PON) (PIND) ($\overline{\text{POFP}}$) signal is generated. The PON signal is sent to the FPC board (A101) and the PIND signal is used to light the POWER lamp. When a regulated supply falls below normal, the ($\overline{\text{PON}}$) ($\overline{\text{PIND}}$) (POFP) signal is generated. The POFP signal enables the Fetch Phase Flip-flop on the STG board (A106). The $\overline{\text{PON}}$ signal is used to initiate an interrupt, inhibit the PSO signal and to disable the Restart Control circuit.

3-5. The Restart Delay circuit is used to hold off the regulated supplies after a power failure until all supplies have had a chance to reach operating level. The PSO signal is gated on and off at 8 second intervals until PON comes up. At that time, the Restart Delay circuit latches up and PSO is held true. This is done to prevent the supplies from shutting themselves off during the restart run-up period.

3-6. The Threshold Detector monitors the line power through the 18VAC unregulated bus. If the line input drops below 100 volts, the Threshold Detector generates an interrupt and disables the Restart control circuit. A switch selects the HALT or RESTART modes. The Threshold Detector also monitors the Thermal Detector. When a thermal switch opens, the Thermal Detector enables the Threshold Detector.

3-7. INTERRUPT LOGIC

3-8. The Interrupt logic is very similar to all computer I/O interrupt circuits, except that it cannot be turned off by a CLF OO instruction or any other instruction. The Interrupt logic is initialized with a STC O4 instruction or by the front panel PRESET pushbutton (PRS). An interrupt can be initiated by a $\overline{\text{PON}}$ signal, an EPF (External Power Fail) signal, or a TDI (Threshold Detector Interrupt) signal. When an interrupt occurs, the PRESET lamp is lighted, and the required INT and IRQ signals are sent to the computer. An IR15 signal is also sent to the STG board (A106) to override any Phase 2 in progress. Notice that this is a departure from normal interrupts which cannot override the Indirect Phase.

3-9. AUTO RESTART LOGIC

3-10. The Auto-Restart logic consists of the Restart Control and Oscillator Ramp Delay. This logic is used to control the re-start operation of the computer. The Restart Control can be turned on with a CLC O4 instruction. It is turned off with a CLF O4 or HLT instruction, and reset after a power failure with a PRS signal or a STC O4 instruction.

3-11. After a power failure, and the supplies have recovered, the PON signal and RESTART signal enable the Restart Control. A negative output starts the Oscillator Ramp Delay. When this ramp reaches 6.8 volts (after about 0.5 seconds), a true RNS signal is sent to the STG board (A106) to enable the RUN mode. A true RNS signal makes $\overline{\text{RF2}}$ go false and the Restart Control circuit is turned off. Since the first instruction of a power fail subroutine is SFC O4, a SKF signal is generated if power is failing (Restart Control flag is clear).

3-12. ADDRESS AND MEMORY PROTECT LOGIC

3-13. The Address logic merely decodes Select Code O4 which is used to address the Power Fail Auto Retart option. The Memory Protect logic has nothing to do with the Power Fail Auto Restart option; it is used only in computers having the Memory Protect option.

3-14. THEORY OF OPERATION

3-15. POWER FAILURE DETECTION

3-16. As stated in Paragraph 3-4, the Power Failure Detection circuits are used to monitor power and initiate an interrupt under abnormal power conditions. This circuit is comprised of the Power Monitor, the Restart Delay, the Thermal Detector and the Threshold Detector. These circuits are shown on Figure 3-2.

3-17. The power monitor circuit which generates the PON and PIND signals (or the POFP signal when power fails) is located in the upper right-hand corner of the schematic. This circuit senses the positive and negative regulated supplies. It is so arranged that all supplies feed a common bus which is gated with +4.5V through MC27. The output of MC27 is then gated with the EPO (External Power On) signal, supplied by the HP2160A Power Supply Extender, through MC87 as the PON signal. A driver (MC76) is used as the PON output. At the same time, MC77 is inhibited and provides a false POFP signal. The PON signal also enables the POWER lamp driver (Q10 and Q9) to provide a true PIND signal. The power sensing circuit is arranged so that when a negative supply fails, one or more transistors are turned off pulling down the common bus. If a positive supply fails, one or more transistors are turned on pulling down the bus.

3-18. The PON output of MC27 is also routed to the Restart Delay logic in the lower left-hand corner on the schematic. This signal turns on Q18 which in turn enables Q16 and Q17 if transistor Q12 is on. Transistor Q12 is normally on except when a thermal switch opens. With Q18 and Q12 on, the turn-on-turn-off of Q16 and Q17 is being gated on and off by the Astable Multivibrator (Q13, Q14 and Q19. The output of Q14 is a 10 second square-wave (positive for 8 seconds and negative for 2 seconds). Thus, Q15 is gated on for only 2 seconds of every cycle. This is done to prevent the supplies from shutting themselves down during initial turn-on. When Q15 turns on, it turns on Q16 (Q17 having been turned on by Q18). The PSO (Power Supply On) signal is therefore gated on and off at a 10 second rate. Now, after one or two cycles, Q15 latches up in the on state and holds Q16 on so that PSO is held true. Again, PSO can be inhibited by a false PON signal (turns off Q18) or a thermal switch opening (turns off Q12).

3-19. Transistors Q11 and Q12, and diode CR22, form the Thermal Detection circuit. Transistors Q11 and Q12 are normally turned on and CR22 is forward biased. This makes MC67 true and provides a false input to the Restart Control gate MC56. The Restart logic is then turned off. After a delay (provided in the Q11 circuit) transistor Q11 is turned off and diode CR22 is reverse biased. This then provides one enabling input to the Restart Control gate MC56.

3-20. Transistors Q21 and Q22 form the Threshold Detector circuit. The 18VAC bus is monitored through CR23 and CR24. When power comes up, Q21 is normally on and Q22 is turned off. This provides a false input to MC67 which then enables the Restart Control gate. When the line input drops below 100 volts, Q21 is turned off and Q22 is turned on. A true input to MC67 now disables the Restart Control gate.

3-21. The Threshold Detector has a HALT-RESTART switch in the logic chain. With the switch in the HALT position, gate MC57 is inhibited and the Restart Control gate cannever be enabled. With the switch in the RESTART position, gate MC57 is always made (except when power is going down) and the restart logic can be enabled. Gate MC16 sets the Flag Buffer FF in the interrupt logic when power comes up. Test point TP1 is used to set the threshold adjustment R66. This test point should have a 1.0 to 1.5V pulse amplitude when the line input drops to 100VAC.

3-22. INTERRUPT CIRCUIT

3-23. The purpose of the Interrupt circuit is to initiate an interrupt when power fails. This logic is very similar to all I/O device interrupt logic.

3-24. Initially, when power is first applied or returns after a power failure, a PRS or STC signal is inverted and resets the Flag Buffer and Flag Flip-flops. The Flag FF being reset turns off the PRESET lamp. The Flag Flip-flop also provides a true PRL4 signal (via MC77) and resets the IRQ Flip-flop (MC66). With the IRQ Flip-flop reset; false IRQ, INT and IR15 signals are output to the computer. When power fails (PON goes low or external power fails EPF), the Flag Buffer FF(MC47) is set. At T2 the ENF signal comes up, and the Flag FF is set. This turns on the PRESET lamp via Q1, and at T5 when SIR comes up, sets the IRQ Flip-flop. With the IRQ Flip-flop set; true IRQ, INT and IR15 signals are output to the computer. At T1 of the next machine cycle, IAK again resets the Flag Buffer Flip-flop.

3-25. AUTO RESTART CIRCUIT

3-26. The purpose of the Auto-Restart circuit is to generate a true RNS signal to the computer when power returns to normal. The logic consists of a Restart Flip-flop, Restart Control gate, and a Restart Ramp Generator. Normally, the Restart Control gate has at least one input false and allows MC56 to output a true signal. This signal allows Q23 to conduct and keeps C17 discharged. The normally true signals to MC56 are PON, the output from the Threshold Detector, and the set state of the Restart Flip-flop. The false input is $\overline{RF2}$ when the computer is running. When power returns, after a power failure, the $\overline{RF2}$ signal is made true on the STG board by the POFP signal. Under this condition, the Restart Control gate MC56 has all true inputs and a false output enables the Restart Ramp Generator.

3-27. The Restart Control Flip-flop acts as the flag for the restart logic. When set, the Restart Control gate is allowed to initiate the restart cycle. The flip-flop (MC47, MC56) can be set by a CLC O4 instruction. It can be turned off with a CLF O4 instruction, or reset by the PRS or STC O4 signals.

3-28. When power fails (going down), PON goes low and sets the flip-flop. This enables the Restart Control logic when the $\overline{RF2}$ signal comes up after power is returned. The reset output from MC56 is also sensed by a SFC instruction. If reset (indicating a power failure has occurred), MC27 and MC17 are made enabling the SKF signal. This puts the computer in the power fail subroutine.

3-29. The Ramp Delay Generator is a modified Schmidt Trigger. When MC56 outputs a false signal, Q23 is cut off. Capacitor C17 charges towards 6.8 volts and the Zener (CR28) then fires and turns on Q25. The output is squared via Q26 and coupled through CR29 and MC76 as the RNS signal. When the RNS signal goes true on the STG board, $\overline{RF2}$ goes false and inhibits the Restart Control gate MC56.

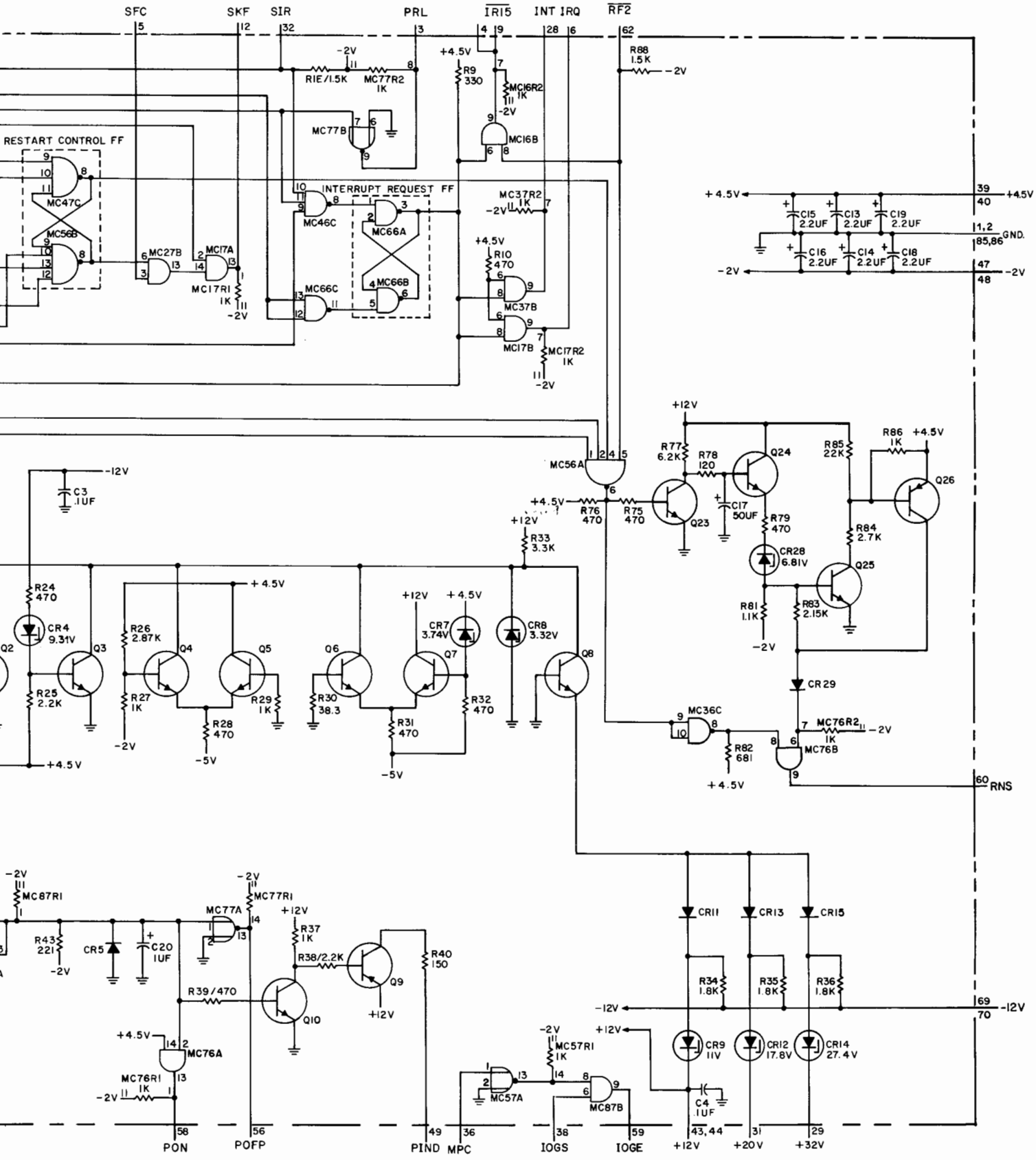
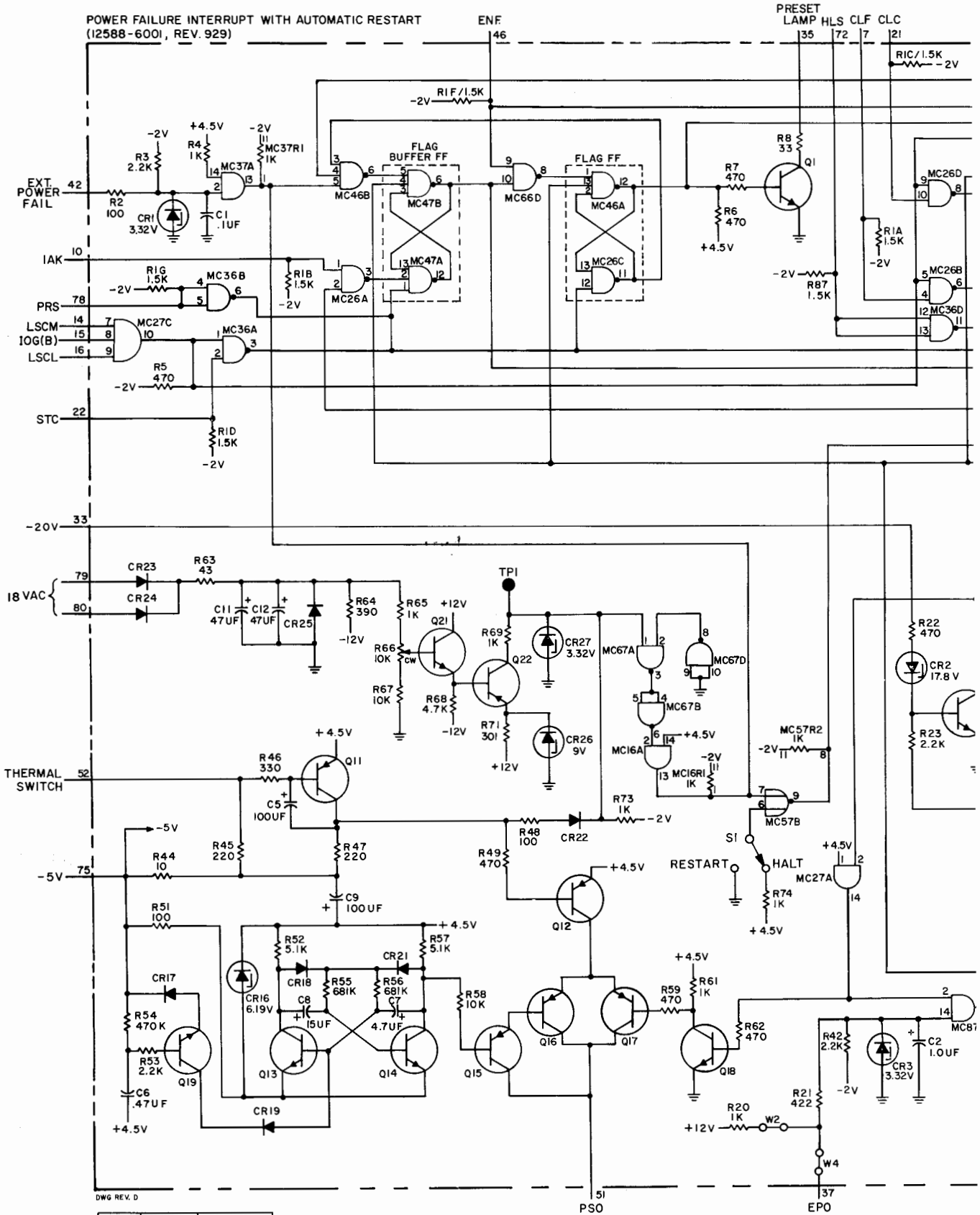


Figure 3-2. Power Fail Auto Restart Schematic



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	B-844-6
B	PC 22-1071	B-915-6
C	ERRATA	NO CHANGE
D	PC 22-1095	C-929-22

VOLUME VIII

TIME BASE GENERATOR

CONTENTS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

1-2. DESCRIPTION

1-3. Interface Kit 12539A for the HP2116A/B Computer Systems consists of one Time Base Generator Card (HP Part No. 02116-6119). This card plugs into any of the interface-card Input/Output slots of the computer and assumes the lower Select Code of the slot. The slot connector transfers all signals to and from the computer; no additional cabling is required. The card contains the standard interface-card control and interrupt logic. It also contains a 100 KHz Oscillator and eight decade frequency dividers. The dividers initiate interrupt signals to the computer in decade steps from 0.1 millisecond to 1,000 seconds (16-2/3 minutes). A flip-flop (on revision H-741-6 cards) provides an indication to the computer when an interrupt is not acknowledged at the end of the programmed time interval. Stability of the card is better than 2 parts in 10^6 per week; temperature effects are less than 20 parts in 10^6 over the temperature range of 15° to 35°C. Thus, stability is better than 1/2 second per 24-hour day.

1-4. INSTALLATION AND OPERATION

1-5. INSTALLATION

1-6. Open the computer for access to the I/O Cards and insert the Time Base Generator card in the desired I/O slot of the computer. The slot connector transfers all signals to and from the Computer; no additional cabling is required. Close the Computer.

1-7. OPERATION

1-8. A control word to the Time Base Generator determines the time intervals that the TBG will output a clock pulse. The output of the TBG may be used to control a digital voltmeter, thermometer, or any instrument to operate at a specific time interval.

SECTION II

PROGRAMMING

2-1. PROGRAM CONTROL

2-2. TYPICAL PROGRAM

2-3. Table 2-1 provides a typical program example. This example is a subroutine which provides an execution delay of 8 milliseconds using the Time Base Generator. The "flag-test" (SFS) method is used, rather than interrupt.

TABLE 2-1. PROGRAM EXAMPLE

```
DELAY   NOP
        LDA     .8      GET 8 FOR COUNTER
        CMA,    INA     MAKE NEGATIVE
        STA     COUNT   INITIALIZE COUNTER
        LDA     .1      GET CONTROL WORD FOR
        OTA     TBG     1 MILLISEC FLAGS & OUTPUT
LOOP    STC     TBG,C   START TIME BASE GEN.
        SFS     TBG     HAS PERIOD ELAPSED
        JMP     *-1     NO - CONTINUE TO WAIT
        ISZ     COUNT   1 PERIOD HAS ELAPSED
        JMP     LOOP    NOT THE LAST ONE, START ANOTHER
        JMP     DELAY,I TOTAL DELAY HAS ELAPSED, RETURN
*
TBG     EQU     nn      I/O ADDRESS OF TIME BASE GEN.
COUNT   NOP             LOCATION OF FLAG COUNTER
.8      DEC     8       FOR 8 FLAGS
.1      OCT     1       CONTROL WORD FOR 1 MILLISEC
```

2-4. As shown in Table 2-1, this program generates timing pulses at intervals of eight milliseconds. The first step is to initialize a counter to eight (the delay desired). Next, the TBG control word specifying the selected time interval is output (OTA, TBG). Finally, after eight milliseconds has elapsed, control is returned to the main program.

SECTION III

THEORY OF OPERATION

3-1. GENERAL

3-2. PROGRAMMING

3-3. The Time Base Generator logic is given in Figure 3-1. The following paragraphs implicitly reference that diagram.

3-4. An Output from A (OTA) or an Output from B (OTB) instruction applies a 3-bit binary number to the Time Base Selection Flip-flops, Bit 0, Bit 1, and Bit 2. This 3-bit number (IOBO0, IOBO1, and IOBO2) determines the time interval between interrupt (or SKF) signals to the computer and are the three least significant bits of the A or B Register. When a different time interval is desired, the 3-bit number is changed (with another OTA/B instruction). For non-decade time intervals (e.g., 3 milliseconds), the nearest decade interrupt must be counted in software to form the desired interval. Interrupt (or SKF) signals can be programmed to occur every 10^{n-1} milliseconds, where n is the 3-bit binary number from the A or B Register. Table 3-1 shows the status bits required for decaded time intervals.

TABLE 3-1. SELECTED TIME INTERVALS

I/O BUS OUTPUT (IOBO)			TIME INTERVAL
Bit 2	Bit 1	Bit 0	
0	0	0	0.1 Millisecond
0	0	1	1 Milliseconds
0	1	0	10 Milliseconds
0	1	1	0.1 Second
1	0	0	1 Second
1	0	1	10 Seconds
1	1	0	100 Seconds
1	1	1	1000 Seconds

3-5. TIME INTERVALS

3-6. As a result of the OTA/B instruction, the IOO signal causes the Time Base Selection Flip-flops and the eight decade dividers to be reset to establish proper initial conditions. The IOBO signals cause the Time Base Selection Flip-flops to set or remain reset, as applicable, and the flip-flop outputs provide enabling signals to the "and" gates on the outputs of the decade dividers. At this time, the output of the 100 kHz Oscillator is not enabled to the decade dividers since the Control Flip-flop is still in a reset state.

3-7. A Set Control, Clear Flag (STC, CLF) instruction to the Time Base Generator Card initiates the time interval programmed by the OTA/B instruction. The STC portion of the instruction sets the Control Flip-flop, which enables the Oscillator output to the decade dividers and resets the Error Flip-flop. The Error Flip-flop is set if the interrupt signal at the end of the programmed time interval is not acknowledged. The CLF portion of the instruction resets the Flag Flip-flop so that it can be set to indicate the end of the selected time interval using the SFS instruction.

3-8. THEORY OF OPERATION

3-9. TIME BASE SELECTION

3-10. The outputs of the decade dividers are "anded" with the outputs of the Time Base Selection Flip-flops. The output of the particular enabled "and" gate is combined with the true output of the Control Flip-flop, and the true reset output of the Flag Flip-flop to provide a true output from "and" gate MC87C. The output of MC87C is applied to the Flag Buffer Flip-flop. The Flag Buffer Flip-flop will not set until its input signal drops. This occurs when the applicable decade divider square-wave output drops, causing the output of gate MC87C to become false.

3-11. After the Flag Buffer Flip-flop is set, the Flag Flip-flop sets on the arrival of the ENF signal at time T2 of the machine cycle. The interrupt or SKF signal (as applicable) is then initiated to the computer, indicating the end of the selected time interval. (If the SKF method is to be used, a Skip on Flag Set (SFS) or a Skip on Flag Clear (SFC) instruction must be issued to test the condition of the Flag Flip-flop).

3-12. Assume a 3-bit (IOBO) input to the Time Base Selection Flip-flops of 000. The true reset outputs of the flip-flops are applied to "and" gate MC45B. All other "and" gates contain at least one false input from the Time Base Selection Flip-flops. When a STC instruction is issued, the Oscillator output is enabled to decade divider MC93. The square-wave output of MC93 becomes true and then returns to a false condition 0.1 millisecond after the STC instruction is issued. During the 0.1 millisecond interval, a true signal is applied to the Flag Buffer Flip-flop. At the end of the interval, the Flag Buffer Flip-flop sets and the interrupt and SKF circuits are initiated.

3-13. ERROR DETECTION

3-14. The output of the particular enabled "and" gate on the output of the decade divider is oombined with the set output of the Flag Flip-flop at "and" gate MC123A. Therefore, the Error Flip-flop is set if the Flag Flip-flop is set. The Flag Flip-flop will be set during the present time interval only when the previous time interval was not acknowledged by the computer. (A Clear Flag (CLF) instruction must be issued after each time interval to permit recognition of the following time interval). The condition of the Error Flip-flop can be tested by a Load Into A (LIA) or a Load Into B (LIB) instruction. The IOI signal resulting from the LIA or LIB instruction enables "and" gate MC107A to provide a true IOBI4 signal to the A or B Register of the computer. Therefore, if bit 4 of the applicable Register is true, at least one time interval was missed. The Error Flip-flop is reset again by a CLF, STC instruction.

3-15. At completion of the use of the Time Base Generator card, a Clear Control (CLC) instruction should be programmed to reset the Control flip-flop and all decade dividers.

3-16. Instructions Which Have Special Uses.

3-17. The following I/O Instructions are used by the Time Base Generator to accomplish special functions.

STC Set Control

1) enables oscillator outputs to Divider String
2) enables divider output to Flag Buffer
3) enables Flag FF to IRQ
4) clears Error FF.

CLC Clear Control

1) resets divider string to zero condition
2) prevents operation of flag and interrupt circuits.
3) prevents oscillator output to divider string

OTA/B Output A register (Oct 0 to 7)

1) Sets up Time Base Selection FF's.

IN A/B Input to A register

1) interrogates Error FF on bit 4

CLF Clear Flag

1) after each timed interval the CLF prevents sitting Error FF on subsequent time period.

The other instructions (STF, SFS, SFC) have only the normal uses.

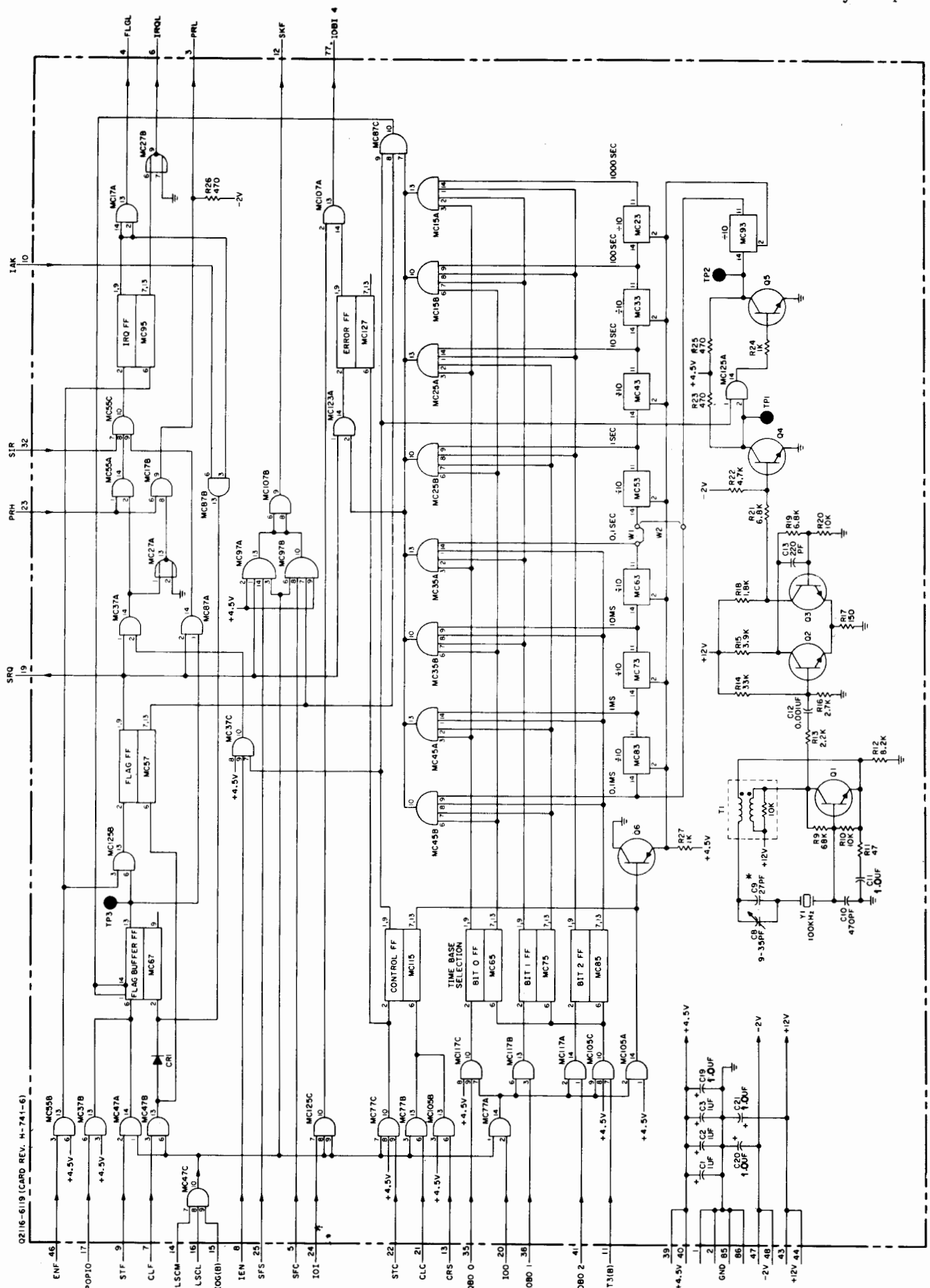


Figure 3-1. Time Base Generator Logic Diagram

VOLUME IX

TELEPRINTER MULTIPLEXER

CONTENTS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

1-2. INTERFACE KIT HP 12584A

1-3. The HP Teleprinter Multiplexer Interface Kit permits up to 16 Teleprinters or Bell System Data Sets, or any combination of the two, to be connected to a Hewlett-Packard Computer. The Teleprinter Multiplexer card is plugged into input/output slot 203 and is assigned Select Code 10. This interface kit provides for bit-serial transfer of data between the computer and the external device, and permits simultaneous input and output. Effectively, the interface kit converts one 16-bit input/output channel to 16 one-bit input/output channels. The standard kit requires at least one option to be operable (see para. 1-9) depending on the intended application.

1-4. DESCRIPTION

1-5. The Teleprinter Multiplexer Interface Card permits bi-directional transfer of data between the HP Computer and HP 2749A Teleprinters (or equivalent). The connection to the teleprinters may be made by direct wiring (up to approximately one mile) or via Bell System Data Sets (when option 02 is provided). The card is a single-address I/O card and plugs into any input/output connector in the computer. The card uses the interrupt system, and due to its relatively rapid, asynchronous interrupt rate it should be assigned a relatively high priority I/O address (most applications use I/O address 10_8). The card contains an 880 Hz clock, control and interrupt logic, 16 receiver circuits and gates to sample input data, and 16 flip-flops with output driver circuits to hold and transmit output data.

1-6. GENERAL OPERATION

1-7. The Teleprinter Multiplexer card causes interrupts to the computer at a rate eight times faster than the rate of the input data from a teleprinter. When an interrupt occurs, software determines if data at any input port has changed from a "one" (Mark) state to a "zero" (start) state, indicating that a character is being received. If this change in the input signal occurs, the software counts 12 interrupts and reads the first bit into the A or B Register of the computer. Succeeding bits are input every eighth interrupt. This continues until all eight data bits are read into the A or B Register. The software monitors for a change from a mark condition to a start condition for the following characters.

1-8. When the computer is ready to transfer a character through the output port of the option, the character bit is made a "0" for eight interrupts which is interpreted by the teleprinter as a start bit. On the ninth interrupt and every eighth interrupt thereafter, a new bit is transferred through the port until a complete character (8 bits) and two stop bits have been transferred. The output port is then left in a "1" state, which is the quiescent state for the communications line, until the next character is to be sent.

1-9. TELEPRINTER MULTIPLEXER OPTIONS

1-10. GENERAL

1-11. The standard HP 12584A Interface Kit provides only the basic multiplex capacity of 16 input/output parts. In order to be useful in such applications as time-shared systems (HP2000A), one or more options must be used.

1-12. OPTION 01

1-13. Interface Kit HP12584A-01 is Option 01 to the standard interface kit. This option is the basic Teleprinter Multiplexer Interface Kit for the HP2000A Time-Shared BASIC system. This interface kit includes the I/O Multiplexer cable and I/O Multiplexer Panel to connect the teleprinters or data sets to the computer in the system. This option connects the Data Terminal Ready lines of all data sets together, resulting in single line control by the computer. Status information from the data sets is not brought into the computer. The 12584A-01 option is best suited for use in a multiple teleprinter situation where all the teleprinters are local (not connected by communication lines). The 12584A-01 Interface Kit consists of the following (the blank card secures connector XA1 to the Multiplexer Panel):

a. Teleprinter Multiplexer I/O card, HP Part No. 12584-6001.

b. Multiplexer Panel, HP Part No. 12584-6002.

c. Blank card, HP Part No. 12584-2001.

d. I/O Multiplex Test Connector, HP Part No. 12584-6003.

e. I/O Multiplexer Jumper Plug, HP Part No. 12584-6004.

f. I/O Multiplexer Cable, HP Part No. 12584-6005.

g. Teleprinter Multiplexer Test - Binary Tape, HP Accessory No. 20439A.

1-14. OPTION 02

1-15. Interface Kit HP 12584A-02 is Option 02 to the standard interface kit. This option must be used with the 12584A-01 option and provides additional ports into and out of the computer for data set control. This interface kit includes the Data Set Disconnect cable which connects another Teleprinter Multiplexer I/O card to the Multiplexer Panel. A Ring Carrier Interface card transfers either the CF Carrier signal or the CE Ringing Indicator signal to the computer in the system as REC signals. When using this option, the status of each data set can be transferred into the computer and tested. The Data Terminal Ready line for each data set is individually answered and disconnected. The 12584A-02 Interface Kit consists of the following:

a. Teleprinter Multiplexer I/O card, HP Part No. 12584-6001.

b. Ring Carrier Interface card, HP Part No. 12584-6011.

c. I/O Multiplex Test Connector, HP Part No. 12584-6003.

d. Data Set Disconnect Cable, HP Part No. 12584-6008.

e. Teleprinter Multiplexer Test -Binary Tape, HP Accessory No. 20439A.

SECTION II

INSTALLATION AND OPERATION

2-1. INSTALLATION

2-2. MULTIPLEXER CONFIGURATION

2-3. Connection from the Teleprinter Multiplexer Interface Card to the Teleprinters or Data Sets is made through an opening in the Multiplexer Panel. Located on the Multiplexer Panel are a Ring Carrier Interface Card connector, 18 receptacle connectors, and connector cabling. Receptacle connectors J0 thru J15 are connected to the Teleprinters or Data Sets, or any combination of each, with a maximum of 16. Connector J16 is used only with the 02 option of the interface kit. When option 02 is not used, an I/O Multiplexer Jumper Plug, Part No. 12584-6004, must be inserted in J16 at all times, and a Blank Card (Part No. 12584-20001)is inserted in the Ring Carrier Interface Card connector to secure connector XA1 to the Multiplexer Panel. Connector J17 is used with the 01 and 02 options of the interface kit. The Ring Carrier Interface Card is used only with the 02 option.

2-4. OPERATION

2-5. OPTION 01

2-6. This option offers only limited control over any data sets connected to it. If an input port is inactive, there is no way for the system to monitor for a disconnect; also, if the operator at the remote terminal has completed transmissions there is no way for the computer to cause a disconnect. A Set Control (STC) instruction will make the Data Terminal Ready signal true for all data sets. A Clear Control (CLC) instruction will make the Data Terminal Ready signal false. Individual control for each data set is not available using only the 01 option.

2-7. OPTION 02

2-8. When this option is used, each data set can be controlled individually by the computer. The Data Terminal Ready signal is made true for a given data set by placing a "1" in the output control port dedicated to that data set. Up to 16 data sets can be controlled in this manner since the 02 option has 16 output control ports. In addition to the output control ports, an input status port exists for each of the data sets being controlled. The information available on these status lines is the logical "or" function of the Carrier Detect and Ringing signals. The computer must sample these lines periodically and properly interpret the results. A logic "1" detected on a status line indicates the presence of a Ringing signal from a data set. The computer responds by making the Data Terminal Ready signal true for that data set and thus, the data set is "answered". The computer continues to sample the status line; if a "1" is still present after the data set has been answered, the data set is transmitting data to the computer. If a "1" is not sensed after a time established by computer software, the computer responds by making the Data Terminal Ready signal false, disconnecting the data set. This provides protection against "housewife" calls. Also, if an input port is inactive for a time established by computer software, the computer causes a disconnect. The assumption here is that the operator at the remote terminal has completed transmissions but has not properly terminated the data set.

2-9. PROGRAMMING

2-10. Programming the Teleprinter Multiplexer varies so much with each application that it is beyond the scope of this manual. The user should reference the software manuals provided with all HP computer systems for instructions on programming the Multiplexer option.

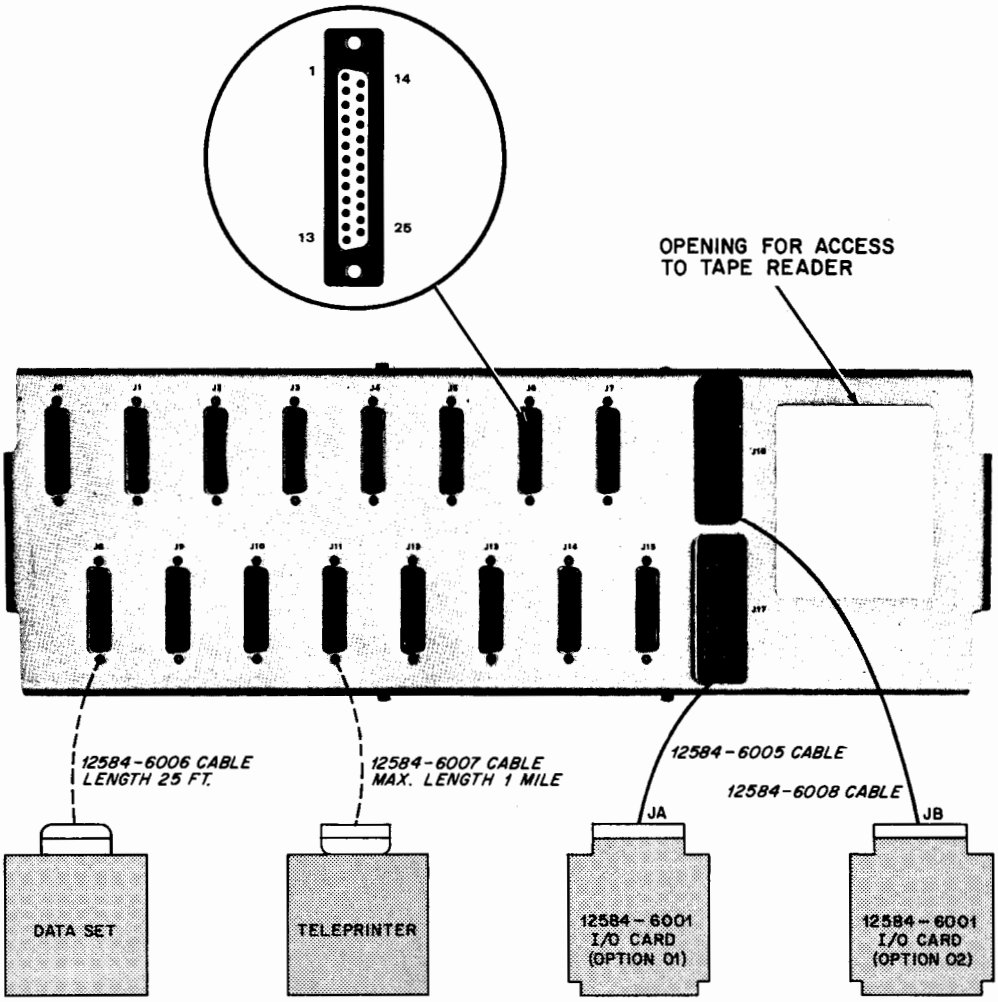


Figure 2-1. Multiplexer Panel, Options and Accessories

SECTION III

THEORY OF OPERATION

3-1. GENERAL

3-2. DATA INPUT OPERATIONS

3-3. A Teleprinter Multiplexer Logic Diagram is given as Figure 3-1. The following descriptions implicitly reference that diagram.

3-4. The computer checks each data input line under program control and the input lines are not buffered. The 880 Hz oscillator is used by software to establish the sampling rate of the input lines. This timing is also used to determine the data transfer rate of 110 bits per second.

3-5. An input operation is initiated by a Set Control, Clear Flag (STC, CLF) instruction to the Teleprinter Multiplexer card. The STC portion of the instruction sets the Control Flip-Flop (FF) which enables the Flag circuit and makes the Data Terminal Ready signal true (option 01 only). The CLF portion of the instruction resets the Flag Buffer and Flag FF's to prevent false interrupt signals from being sent to the computer.

3-6. A Flag signal is applied to the Teleprinter Multiplexer card every 1.14 milliseconds by the 880 Hz oscillator. The Flag signal sets up a request for service (Interrupt Request, or Skip Flag if the interrupt system is not being used). At time T2, the Enable Flag (ENF) signal and the set-side output of the Flag Buffer FF sets the Flag FF. If a device of higher priority has not requested an interrupt, the output from the Flag FF initiates an interrupt signal to the computer, indicating that data is available at the input lines.

3-7. To accomplish an input operation, the computer must accept the data from the Input Register. This is done by a Load Into A/B (LIA/B) or a Merge Into A/B (MIA/B) instruction. When one of these instructions is issued, the IOI (I/O IN) signal enables the data on the input "and" gates to the IOBI (I/O Bus In) lines. These lines transfer the data to the A- or B-Register.

3-8. The set or reset condition of the Flag FF may be checked by a Skip on Flag Set (SFS) or a Skip on Flag Clear (SFC) instruction to determine when an input operation should be performed. When using this method, the Interrupt System Enable FF on the I/O Control card must be reset by a CLF instruction with a Select Code of 00.

3-9. DATA OUTPUT OPERATIONS

3-10. Computer software determines which output lines will be used to output data to the Teleprinters and/or Data Sets; all output lines are buffered. The 880 Hz oscillator determines the output data transfer rate of 110 bits per second.

3-11. If the interrupt system is to be used during the output operation, the Interrupt System Enable FF, on the I/O control card, must be set by a Set Flag (STF) instruction with a Select Code of 00. An Output from A/B (OTA/B) instruction must be issued by the computer program to output data from the A-or B-Register to the Teleprinter Multiplexer card. The IOO (I/O out) signal to the card, which results from the OTA/B instruction, enables the bits from the A or B Register to set the Output Register FF's on the Teleprinter Multiplexer Card.

3-12. The computer program initiates an output operation with a STC, CLF instruction and the address of

the Teleprinter Multiplexer card. The STC portion of the instruction sets the Control FF. The output from the Control FF is "nanded" with the Run signal (from the STG card in the computer) providing a true Data Terminal Ready signal to the Data Set or Teleprinter (option 01 only). If the Data Terminal Ready signal is false, an incoming call will not be answered; if true, it will be answered. If a call is answered and the Data Terminal Ready signal is then made false (by a CLC instruction), the connection will be broken. Therefore, setting the Data Terminal Ready signal true (by an STC, SC instruction) is equivalent to answering the phone. Normally, the computer sets the Data Terminal Ready signal to the true state and waits for calls to arrive. The calls are then automatically answered and data transfer can proceed. The STC portion of the instruction also provides an enable signal to the Interrupt Control logic. The CLF portion of the instruction resets the Flag Buffer and Flag FF's (which were set by the POPIO signal when power was initially applied to prevent a false interrupt signal from being sent to the computer before the I/O device has accepted data.

3-13. The Internal Clock signal (pin 22) is formed by the free-running 880 Hz oscillator. This signal causes interrupts every 1.14 milliseconds and is applied to pin 22 and then to pin Z through the jumper plug (option 01 only). The Internal Clock signal resets the Flag Storage FF, and is transferred through "nand" gate MC17B, setting the Flag Buffer FF. The Flag Storage FF stores one interrupt in case the first interrupt is not cleared by the computer before a second interrupt occurs.

3-14. THEORY OF OPERATION

3-15. COMPUTER POWER ON

3-16. When power is initially applied by the computer POWER switch, the POPIO and CRS signals are received simultaneously by the interface card from the computer. These signals establish initial conditions for operation of the interface card. The POPIO signal is applied through connector pin 17 to "nand" gate MC67D. All inputs to the "nand" gate are then true and its false output sets the Flag Buffer FF (the input to the FF is inverted). At time T2, the ENF signal is applied through connector pin 46 to "nand" gate MC37C. The output from gate MC37C resets the IRQ FF. The output from "nand" gate MC37C is also transferred through "nand" gate MC37D and with the output of the Flag Buffer FF, sets the Flag FF and Flag Storage FF. The POPIO signal is transferred through "nand" gate MC77D and applied to "nand" gates MC97A and MC97B. The output from these gates directly sets the 16 output Register FF's to a mark condition to prevent the teleprinters from running open.

3-17. When power is first applied, the positive pulse of the Control Reset signal is received at pin 13 and inverted by "nand" gate MC67B. The output from this gate resets the Control FF. Therefore the card is always in the input state after power turn on or whenever the computer PRESET switch is pressed.

3-18. FLAG AND CONTROL LOGIC

3-19. A programmed STC instruction with the address of the Teleprinter Multiplexer card provides STC, LSCL, LSCM, and IOG signals to the Teleprinter Multiplexer card. The STC signal is applied to connector pin 22 and transferred as one true input to "nand" gate MC77A. The LSCL, LSCM, and IOG signals are applied to "nand" gate MC47A, transferred through "nand" gate MC57D providing the second true input to gate MC77A. The false output of "nand" gate MC77A sets the Control FF at Time T4. The set-side output of the Control FF is applied as one true input to "nand" gate MC36A. The other inputs to this gate are the true IEN signal (generated by the set-side of the Interrupt System Enable FF on the I/O Control card) and the true output from the set-side of the Flag FF. The output of "nand" gate MC36A is applied to "nand" gate MC26A and MC15A. Gate MC15A will have a true output after the Flag FF is reset and a device of higher priority has not requested an interrupt (PRH true). Gate MC16 B will have a false output if at time T5 (SIR) the PRH signal is true, the Flag Buffer FF is set (true), and the output of "nand" gate MC26A is true. The false output of MC16B sets the Interrupt Request (IRQ) FF. This FF is reset at the next time

T2 (ENF) to allow devices of higher priority to interrupt. If no higher priority device requested an interrupt, the IRQ FF sets again and interrupts the computer program. The set-side output of the IRQ FF is applied to "nand" gate MC57B. The output of this "nand" gate or the output of "nand" gate MC77B resets the Flag Buffer FF to permit recognition of the next interrupt.

3-20. DATA TERMINAL READY

3-21. A STC, CLF instruction with the address of the Teleprinter Multiplexer Card enables the Teleprinter Multiplexer card. The STC instruction sets the Control FF. The true output of the Control FF is applied to "nand" gate MC87A. The other true input to this gate is the Run signal, received from the computer STG card. The run signal is transferred through connector pin 50 and applied to MC87A. This gate is enabled, transferred through "nand" gate MC87B, where a positive voltage is applied to transistor Q52, turning the transistor on. With Q52 conducting, the Data Terminal Ready signal is in a true state indicating that the computer is running and the Data Terminal Ready signal is present on pins AA and 23 (option01). If the Data Terminal Ready signal is in a false state, incoming calls will not be answered. The Ring Carrier Interface card performs this function for option 02.

3-22. INPUT REGISTER

3-23. Logic levels from the external I/O device are as follows:

Logic "1" = negative voltage (more than -5 volts)
Logic "0" = positive voltage (more than +5 volts)

3-24. When REC 0 through REC 15 signals are transferred from the I/O device to the input Register, a negative voltage (external transistor off) is received at the input to the register. Since REC 0 through 15 circuits are identical, only REC 0 will be explained.

3-25. A negative voltage (logic "1"), from the I/O device is applied through connector pin 1 to the base of transistor Q1. Transistor Q1 is cut off which applies a positive voltage (logic "0") to pin 2 of "and" gate MC45A. The other true signal, applied to pin 14 of "and" gate MC45A, is the IOI· [LSCL · LSCM · IOG] signal. This enables "and" gate MC45A, and data (positive voltage) is transferred to the computer through pin 26 of the 86-pin connector, as a true IOBI 0 signal.

3-26. A positive voltage (logic "0") from the I/O device, is applied through connector pin 1 to the base of transistor Q1. Transistor Q1 conducts, which applies a ground potential to pin 2 of "and" gate MC45A. With any ground input to "and" gate MC45A, the output (pin 13) is also ground and is transferred to the computer through pin 26 of the 86-pin connector as a false IOBI 0 signal.

3-27. OUTPUT REGISTER

3-28. Logic levels to the external I/O device are as follows:

Logic "1" = negative voltage (more than -5 volts)
Logic "0" = positive voltage (more than +5 volts)

3-29. When IOBO signals are transferred from the computer (via backplane wiring) to the Output Storage Register, -0.5 volts (logic "0") or +2.5 volts (logic "1") is received at the input to the storage register. Since all IOBO circuits are identical, only IOBO 0 will be explained.

3-30. A positive voltage (logic "1") from the computer, received through connector pin 35 is applied to the set-side of flip-flop MC46A. An $\overline{IOO \cdot [LSCM \cdot LSCL \cdot IOG]}$ signal is applied to pin 4 of MC46A. This strobes the data through the flip-flop where a positive potential is output on pin 5. When this occurs, transistor Q18 conducts and applies a ground potential on the base of emitter follower, Q17, which is always conducting. Zener diode CR49 is reversed biased, transferring -5.11 volts through connector pin A as a true (mark) data bit.

3-31. A ground potential (logic "0") from the computer, received through connector pin 35, resets the flip-flop, MC46A, during IOO . [LSCM . LSCL · IOG]. The flip-flop is clocked when IOO · [LSCM · LSCL · IOG] goes positive. The set-side output of this FF is at ground and is applied to the base of transistor Q18, turning the transistor off. With transistor Q18 in the off state, a positive voltage is applied to the base of emitter follower, transistor Q17. Zener diode CR49 is reversed biased, transferring +5.5 volts through connector pin A as a false (space) data bit.

3-32. FLAG AND INTERRUPT

3-33. The Flag and Interrupt circuitry is standard except for the addition of the Flag Storage FF. Refer to Figure 3-2 for a Functional Block Diagram of the Flag and Interrupt circuitry.

The oscillator provides a pseudo device flag which sets the Flag Buffer. At T2 the Flag FF is set. At T5 the IRQ FF is set, generating the IRQ and FLG signals. These signals request the phase 4 interrupt, and encode the select code. Following Phase 4 the IAK clears the Flag Buffer. ENF at T2 clears the IRQ. The Flag FF is cleared under Interrupt Subroutine control by the CLF (SC) instruction. This instruction is located at the end of the subroutine just prior to the JMP, I through the NOP location.

3-34. The Flag Storage FF serves as a flag queue. It reduces the danger of losing a flag signal when tied up servicing a higher priority device. The oscillator output (Internal Clock) is coupled to pin Z through the Multiplexer cable. The negative oscillator signal (+.5V) sets the Flag Storage FF. At T5 following the negative to positive transistion the flag buffer is set and the Flag and Interrupt circuit performs normally.

If the previous multiplexer interrupt service routine had been started, but was then interrupted by a higher priority device (such as DMA) the Flag FF will not have been cleared. The Flag Storage FF is set by the current oscillator flag input, but does not set the Flag Buffer. At the conclusion of the higher priority subroutine PRH goes high and the previous multiplexer interrupt subroutine is resumed. At its conclusion the Flag FF is cleared. The pseudo interrupt stored in the Flag Storage FF is now processed. Thus the Flag Storage FF allows a delay up to 1.1 milliseconds in servicing the oscillator clock without losing the interrupt.

3-35. DATA PHONE AUTO DISCONNECT.

3-36. The 12584A-02 option provides Auto Disconnect for Dataphone applications. The multiplexer board was designed to service Dataphones by providing a "Data Terminal Ready" signal to all ports. Serious problems arose in this mode of operation. A wrong number might call up and tie up a port intefinitely . And no method existed to clear the line. The second problem existed due to an unplanned termination or disconnect. A users time would continue to accumulate. A new user making connection with the port might also have access to the former users files and programs.

The 02 option provides an additional multiplexer board to monitor and process the dataphone signals. The input register monitors the Ringing and Carrier signals from the data set. If log onto the Time Share system is not accomplished within 2 minutes (time limit can be changed in Time Share Software) the Data Terminal Ready signal (Output Register bit) is dropped forcing dataphone disconnect. A user inadvertantly terminated is logged off the system.

This phone service routine checks for new inputs (Ringing or Carrier) in the input register. It initiates log on timing counters. When an existing input disappears it initiates a drop out 1 second timer. If the carrier is not re-established within this time period, log off is initiated.

3-37. MULTIPLEXER DATA

3-38. All data from dataphones as well as the hard wired teletypes is handled by the 01 Multiplexer assembly.

All output from the time share system is handled through the respective Output Register bit under control of the Multiplexer Interrupt Driver routine. The "ECHO-ON" command sets the bit in the Full Duplex word PLEX. The incoming data being processed by the Multiplexer Interrupt Driver is outputed bit by bit through the Output Register. This allows the teleprinter to print the character on the printer mechanism. In "ECHO-OFF" operation the data bits are not outputed and the teleprinter does not print the data being entered on the keyboard or tape reader.

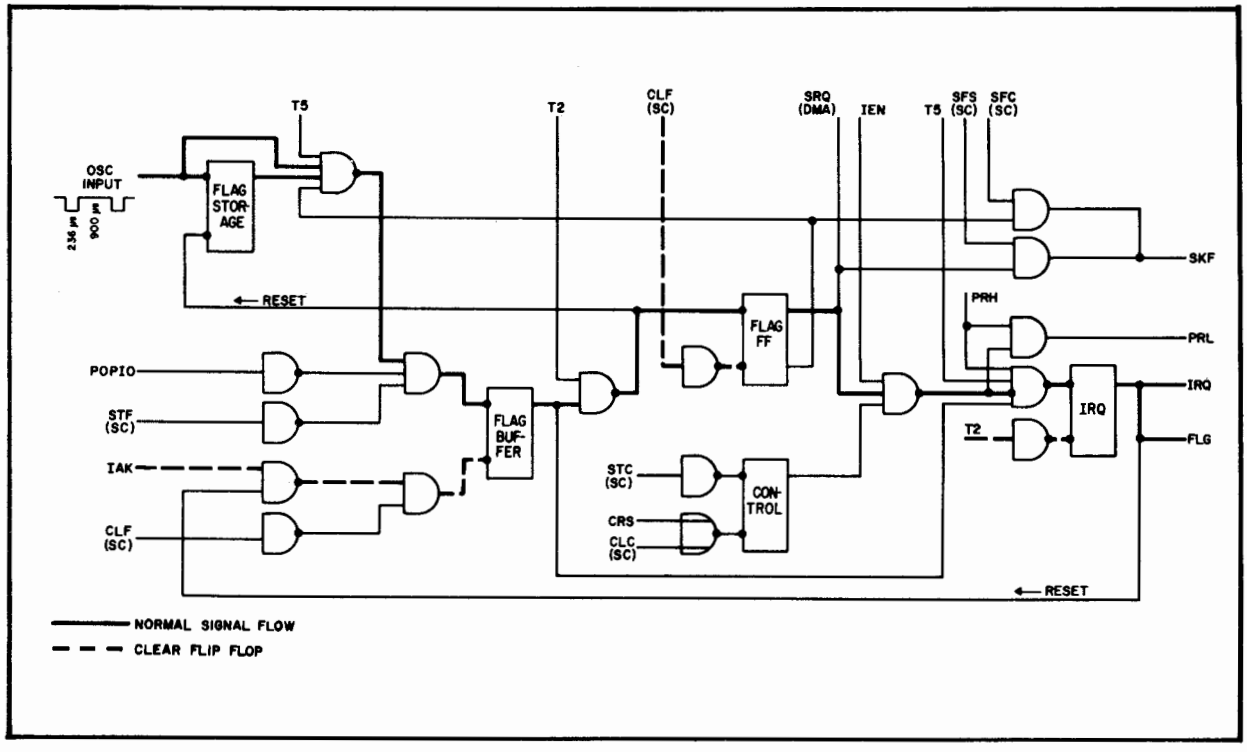
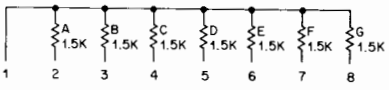


Figure 3-2 Flag and Interrupt Functional Blocks

NOTES:

1. ALL LOGIC IS POSITIVE - TRUE
2. IS EQUIVALENT TO
3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R129-R133



4. * INDICATES SIGNALS FROM/TO TELEPRINTER VIA 48-PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM/TO COMPUTER VIA 86-PIN CONNECTOR.

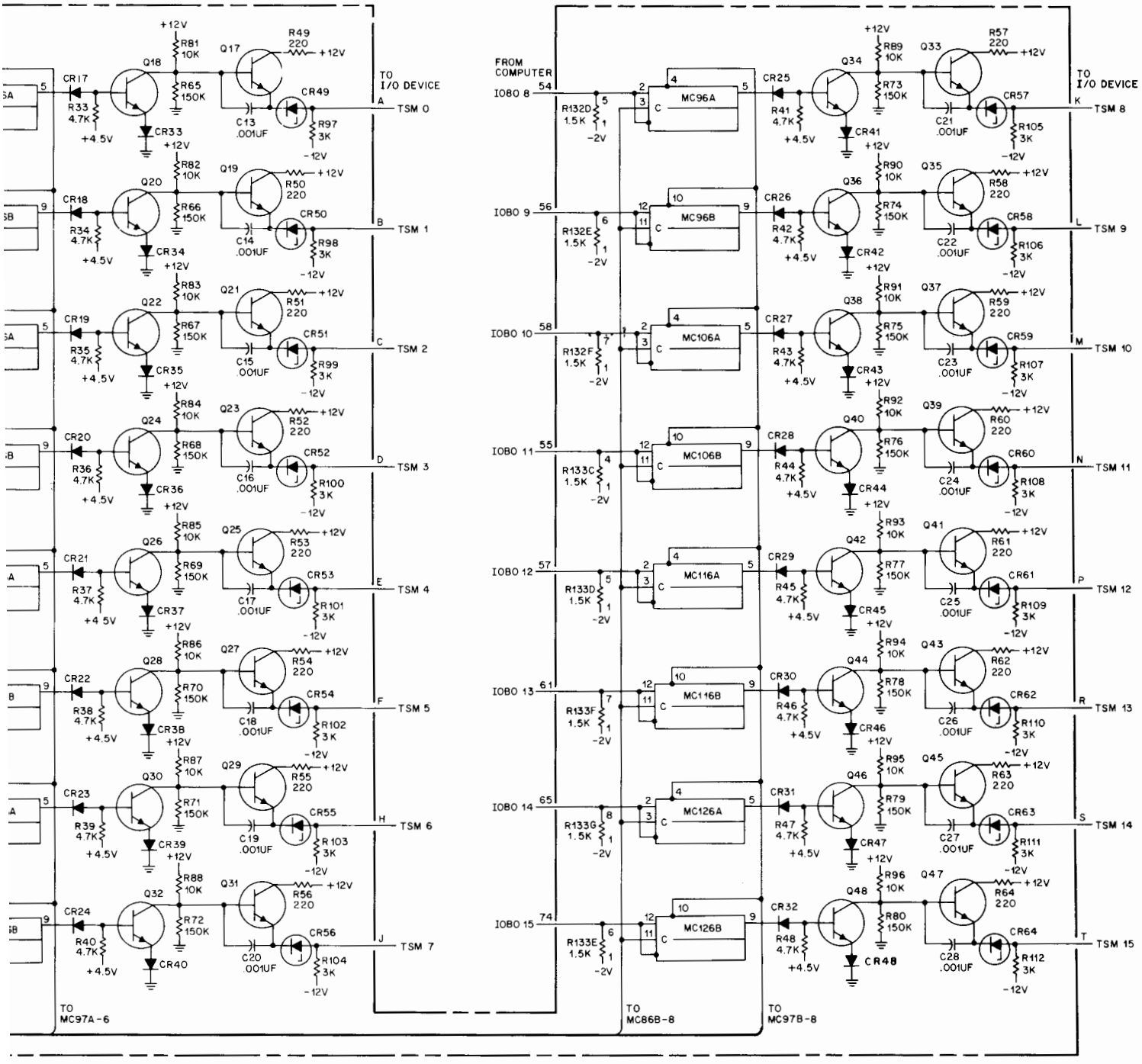
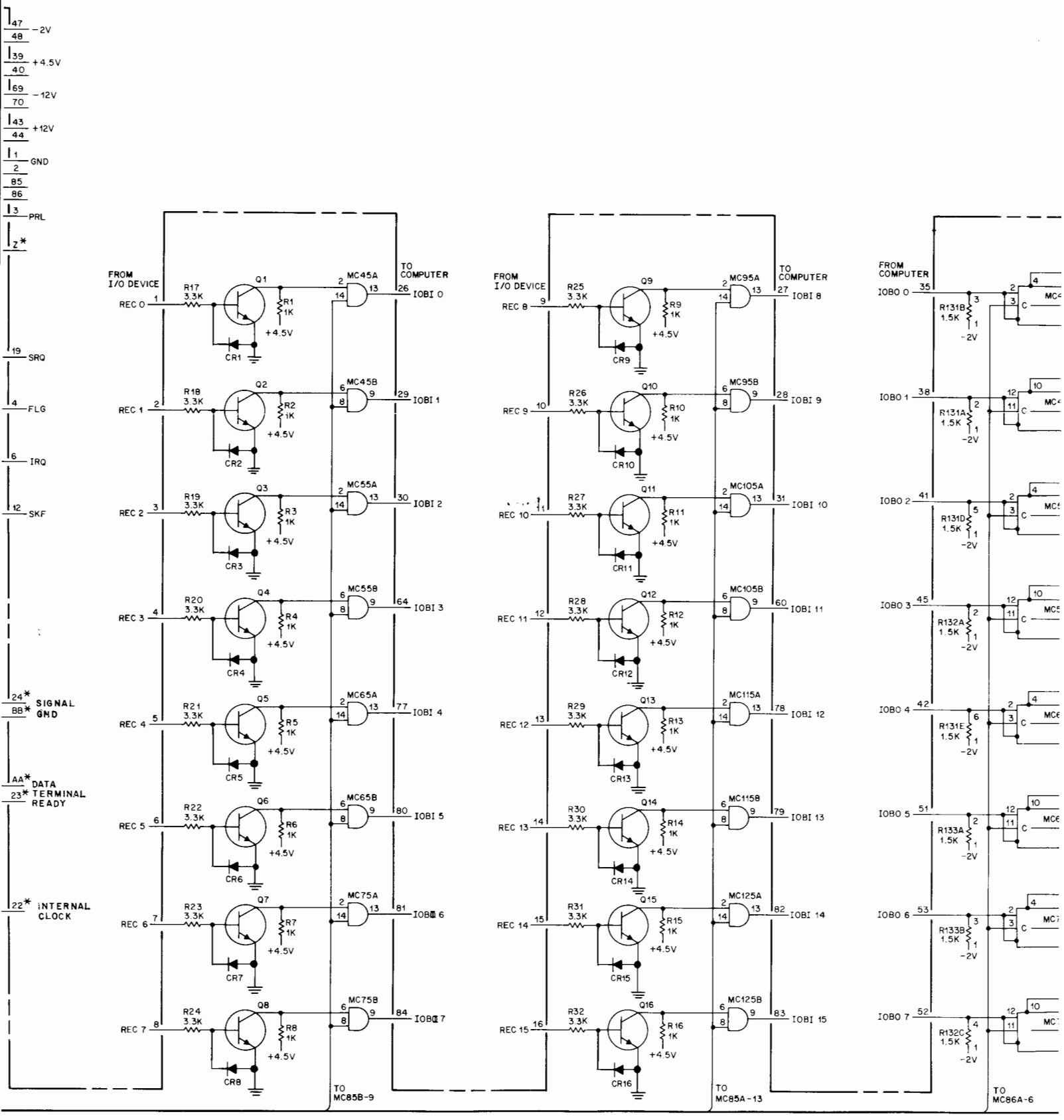
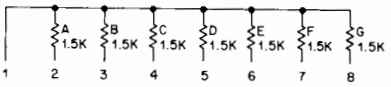


Figure 3-1. Teleprinter Multiplexer Logic Diagram


47
48
-2V
39
40
+4.5V
69
70
-12V
43
44
+12V
1
2
85
86
GND
3
PRL
Z*
19
SRQ
4
FLG
6
IRQ
12
SKF
24*
BB*
SIGNAL GND
AA*
DATA
23*
TERMINAL READY
22*
INTERNAL CLOCK
FROM I/O DEVICE
REC 0
REC 1
REC 2
REC 3
REC 4
REC 5
REC 6
REC 7
R17 3.3K
R18 3.3K
R19 3.3K
R20 3.3K
R21 3.3K
R22 3.3K
R23 3.3K
R24 3.3K
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
R1 1K
R2 1K
R3 1K
R4 1K
R5 1K
R6 1K
R7 1K
R8 1K
+4.5V
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
MC45A
MC45B
MC55A
MC55B
MC65A
MC65B
MC75A
MC75B
TO COMPUTER
IOBI 0
IOBI 1
IOBI 2
IOBI 3
IOBI 4
IOBI 5
IOBI 6
IOBI 7
TO MC85B-9
FROM I/O DEVICE
REC 8
REC 9
REC 10
REC 11
REC 12
REC 13
REC 14
REC 15
R25 3.3K
R26 3.3K
R27 3.3K
R28 3.3K
R29 3.3K
R30 3.3K
R31 3.3K
R32 3.3K
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
R16 1K
+4.5V
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
MC95A
MC95B
MC105A
MC105B
MC115A
MC115B
MC125A
MC125B
TO COMPUTER
IOBI 8
IOBI 9
IOBI 10
IOBI 11
IOBI 12
IOBI 13
IOBI 14
IOBI 15
TO MC85A-13
FROM COMPUTER
IOBO 0
IOBO 1
IOBO 2
IOBO 3
IOBO 4
IOBO 5
IOBO 6
IOBO 7
R131B 1.5K
R131A 1.5K
R131D 1.5K
R132A 1.5K
R131E 1.5K
R133A 1.5K
R133B 1.5K
R132C 1.5K
-2V
TO MC86A-6

NOTES:

1. ALL LOGIC IS POSITIVE - TRUE
2. IS EQUIVALENT TO
3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R129-R133



4. * INDICATES SIGNALS FROM/TO TELEPRINTER VIA 48-PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM/TO COMPUTER VIA 86-PIN CONNECTOR.

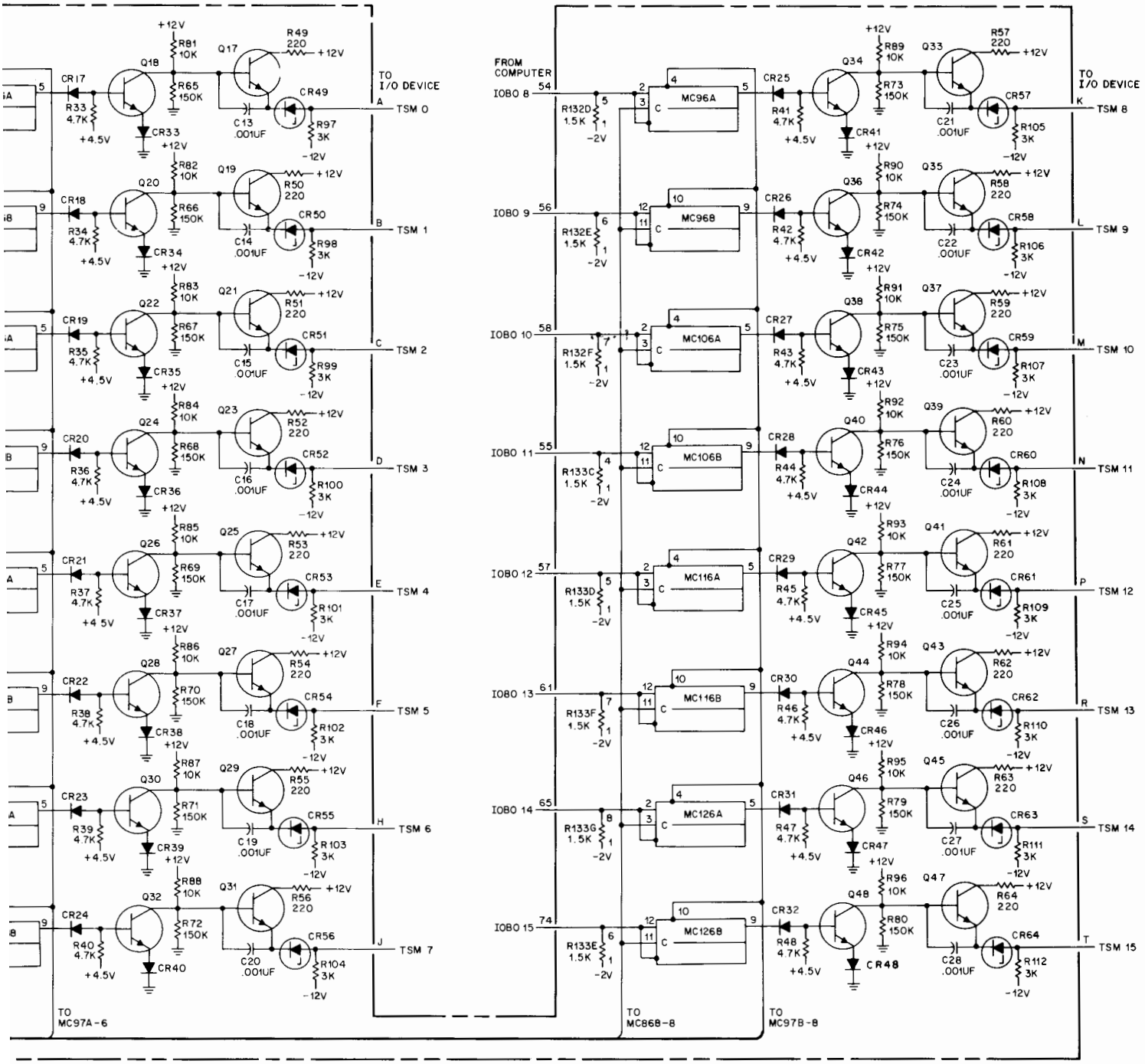


Figure 3-1. Teleprinter Multiplexer Logic Diagram

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