HEWLETT-PACKARD

COMPUTER MAINTENANCE COURSE

STUDENTS WORKBOOK

HP 2116B/HP 2115A
CENTRAL PROCESSOR UNITS

(HP STOCK NO. 5950-8720)

-NOTICE-

The information contained in this manual is for training purposes only. Consult the Hewlett-Packard documentation supplied with the computer for current information concerning the specific computer system furnished.

11000 Wolfe Road, Cupertino, California 95014 Area Code 408 257-7000 TWX 910-338-0221

Printed in U.S.A. APR 69

HP Computer Museum
www.hpmuseum.net

For research and education purposes only.

AAF	=	A Addressable Flip-Flop
ADD	=	And Instruction Decoded
ADF	=	Add Function
ANF	=	AND Function
ASG	=	Alter Skip Group Instruction Decoded
BAF	=	B Addressable Flip-Flop
CØ, C4, C8, C12, C16	=	Carry to Bits Ø, 4, 8, 12, 16 respectively
CFF	=	Carry Flip-Flop Set Output
CL1	=	Clock 1 Flip-Flop Set Output
CL2	=	Clock 2 Flip-Flop Set Output
CLC	=	Clear Control
CLF	=	Clear Flag
$\overline{\text{CMF}}$	=	Complement Function NOT
$\overline{\text{CMFE}}$	=	Complement Function (Inst. Decoder) NOT
CMFH	=	Complement Function (EAU)
CPR	=	Compare Instruction Decoded
CRS	=	Control Reset to I/O
CTFF	=	Control FF Set Output
DMS	=	Display Memory Switch
EFF	=	Extend FF Set Output
E. IND.	=	Extend Indicator
EIR	=	Enable Instruction Register
ENF	=	Enable Flag
$\overline{\text{EOF}}$	=	Exclusive OR Function NOT
$\overline{\text{EOFE}}$	=	Exclusive OR Function (Inst. Decoder) NOT
EOFH	=	Exclusive OR Function (EAU)
EPH	=	Enable Phase
ESR	=	Enable Service Request
FBFF	=	Flag Buffer FF Set Output
FLFF	=	Flag FF Set Output
FLGØ	=	Flag from Group Ø
FLG1	=	Flag From Group 1
FLG2	=	Flag From Group 2

FLG3	=	Flag From Group 3
HIN	=	Halt Instruction
HIS	=	Hold Interrupt System
HLS	=	Halt Switch
$\overline{\text{HLS}}$	=	Halt Switch NOT
HLSFF	=	Halt Switch FF Set Output
IAK	=	Interrupt Acknowledge
ICFF	=	Interrupt Control FF Set Output
IEN(6)	=	Interrupt Enable (6)
IEN(1Ø)	=	Interrupt Enable (1Ø)
IEN(2Ø)	=	Interrupt Enable (Group 2Ø)
IIR	=	Inhibit Instruction Register
ILS	=	Instruction Loop Switch
INT	=	Interrupt
IOBIØ-16	=	I/O Bus Input Bits Ø thru 16
IOCO	=	I/O Control, Output
$\overline{\text{IOF}}$	=	Inclusive OR Function NOT
IOG	=	I/O Instruction Decoded
IOGE	=	I/O Instruction Decoded (Buffered thru Power Fail)
IOGE(B)	=	I/O Instruction Decoded (Buffered thru Power Fail and I/O Control
IOI	=	I/O Input
IOO	=	I/O Output
IOS	=	I/O Switch Address
$\overline{\text{IR15}}$	=	I Register Bit 15 NOT
IRQ1-17	=	Interrupt Request Units 1-17
IRQFF	=	Interrupt Request FF Set Output
ISEFF	=	Interrupt System Enable FF Set Output
ISG	=	Inhibit Strobe Generator
ISR	=	Input Switch Register
ISZ	=	Increment and Skip if Zero
ITFF	=	Interrupt Timing FF Set Output
JMP	=	Jump Instruction Decoded
JSB	=	Jump Subroutine Instruction Decoded
LADS	=	Load Address Switch

LAS	=	Load A Switch
LBS	=	Load B Switch
LMS	=	Load Memory Switch
LOD	=	Load Instruction Decoded
LPS	=	Loader Protection Switch
MØ-14	=	Memory Address Bits Ø thru 14
MAC	=	Macro Instruction Decoded
MIT	=	Memory Inhibit Timing
MMD13	=	Memory Module Decoder Bit 13
MMD14	=	Memory Module Decoder Bit 14
MNS	=	Memory Normal Switch
MPT	=	Memory Protect
MPTØ	=	Memory Protect Ø
MPT1	=	Memory Protect 1
MPT2	=	Memory Protect 2
MPT3	=	Memory Protect 3
MPT4	=	Memory Protect 4
MRØ-13	=	M Register Bits Ø thru 13
$\overline{\text{MRØ-12}}$	=	M Register Bits Ø thru 12 NOT
MRT	=	Memory Read Timing
MST	=	Memory Strobe Time
MTE	=	Memory Timing Enable
MWL	=	Memory Write Level
MWT	=	Memory Write Time
$\overline{\text{OPO}}$	=	One Phase Operation NOT
OVFF	=	Overflow FF Set Output
OVF. IND.	=	Overflow Indicator
P123	=	Phase 1, 2 or 3
P123G	=	Phase 1, 2 or 3 (Buffered)
PEH	=	Parity Error Halt
PEI	=	Parity Error Interrupt
PH1	=	Phase 1
PH2	=	Phase 2
PH3	=	Phase 3
PH4	=	Phase 4

$\overline{\text{PH5}}$	=	Phase 5 NOT
PH1FF	=	Phase 1 FF Set Output
PH2FF	=	Phase 2 FF Set Output
PH3FF	=	Phase 3 FF Set Output
PH4FF	=	Phase 4 FF Set Output
PIND	=	Power Indicator
PNS	=	Phase Normal Switch
POFP	=	Power On/Off Pulse
PON	=	Power On Normal
POPIO	=	Power On Pulse I/O
POPIO(B)	=	Power On Pulse I/O (Buffered)
PRH5	=	Priority High Unit 5
PRH6	=	Priority High Unit 6
PRH1Ø-3Ø	=	Priority High Units 1Ø thru 3Ø
PRL4	=	Priority Low Unit 4
PRL5	=	Priority Low Unit 5
PRS	=	Preset Switch
$\overline{\text{PRS}}$	=	Preset Switch NOT
PRSFF	=	Preset FF Set Output
PSO	=	Power Supply On
RARB	=	Read A Register to the R Bus
RBØ-15	=	R Bus Bit Ø-15
RBRB	=	Read B Register to the R Bus
RF1	=	Run 1 FF
$\overline{\text{RF2}}$	=	Run 2 Flip-Flop NOT
$\overline{\text{RL4}}$	=	Rotate Left 4 Bits NOT
$\overline{\text{RLL}}$	=	Rotate Left to Least Significant Bit NOT
RMSB	=	Read M Register to S Bus
RNS	=	Run Switch
$\overline{\text{RNS}}$	=	Run Switch NOT
RPB	=	Reset Parity Bit
RPE	=	Reset Parity Error
RPRB	=	Read P Register to R Bus
$\overline{\text{RRS}}$	=	Rotate Right to Sign Bit NOT
RSM (6-9) (ISM)	=	Reset M Register Bits 6-9 (Interrupt Store in M Register)

RSM (1Ø-15)	=	Reset M Register Bits 1Ø-15
RST	=	Reset the T Register
RTSB	=	Read T Register to S Bus
S1FF	=	Step 1 FF Set Output
S2FF	=	Step 2 FF set Output
SBØ-15	=	S Bus Bit Ø-15
SC	=	Select Code
SCL(Ø)-(7)	=	Select Code Least Significant Ø thru 7
SCM(Ø)-(7)	=	Select Code Most Significant Ø thru 7
SCS	=	Single Cycle Switch
SEO	=	Switch Exclusive OR
SFC	=	Skip if Flag Clear
SFS	=	Skip if Flag Set
SIR	=	Service Interrupt Request
SKF	=	Skip on Flag
$\overline{\text{SL14}}$	=	Shift Left Bit 14 NOT
$\overline{\text{SL14E}}$	=	Shift Left Bit 14 (Shift Logic) NOT
SL14H	=	Shift Left Bit 14 (EAU)
$\overline{\text{SLM}}$	=	Shift Left Magnitude NOT
$\overline{\text{SLME}}$	=	Shift Left Magnitude (Shift Logic)
SLMH	=	Shift Left Magnitude (EAU)
SRAØ-77	=	Service Request Address Unit Ø-77
SRG	=	Shift Rotate Group Instruction Decoded
$\overline{\text{SRM}}$	=	Shift Right Magnitude NOT
$\overline{\text{SRME}}$	=	Shift Right Magnitude (Shift Logic) NOT
SRMH	=	Shift Right Magnitude (EAU)
SRQ1Ø-27	=	Service Request Units 1Ø thru 27
STØ-16	=	Sense Amp Output Bits Ø thru 16
STBA	=	Store T Bus in A Register
STBB	=	Store T Bus in B Register
STBT	=	Store T Bus in T Register
STC	=	Set Control
STF	=	Set Flag
STM(Ø-5), (Ø-9) (1Ø-11), (12-15)	=	Store M Register Bits Ø-5, Ø-9, 1Ø-11, 12-15 respectively

STP(Ø-9), (1Ø-11) (12-15)	=	Store P Register Bits Ø-9, 1Ø-11, 12-15 respectively
STR	=	Store Instruction Decoded
SWSA	=	Switch Store in A Register
SWSB	=	Switch Store in B Register
SWSM	=	Switch Store in M Register
SWSP	=	Switch Store in P Register
SWST	=	Switch Store in T Register
TØ-7	=	Time Ø thru 7
T3(B)	=	Time 3 (Buffered)
T7S	=	Time 7 with Strobe
TØT1	=	Time Period TØ thru T1
T1T2	=	Time Period T1 thru T2
T3T4	=	Time Period T3 thru T4
T4T5	=	Time Period T4 thru T5
T6T7	=	Time Period T6 thru T7
TAN1	=	T Bus ANDed Bits 0-3
TAN2	=	T Bus ANDed Bits 4-7
TAN3	=	T Bus ANDed Bits 8-11
TAN4	=	T Bus ANDed Bits 12-15
TBØ-15	=	T Bus Bits Ø thru 15
TRØ-15	=	T Register Bits Ø thru 15
$\overline{\text{TRØ-15}}$	=	T Register Bits Ø thru 15 NOT
TRØ(B)	=	T Register Bit Ø (Buffered)
TR2(B)	=	T Register Bit 2 (Buffered)
TS	=	Time Strobe
TSA	=	Time Strobe A
TTK	=	Memory Extender Present
YØ/1	=	Y Driver/Switch Ø/1 Select
Y2/3	=	Y Driver/Switch 2/3 Select

HP 2116B Equation Summary

$$AAF = TAN1 \cdot \overline{TB14}\,[TAN2 \cdot TAN3\,(\overline{TB12} \cdot \overline{TB13})]\,(T\emptyset \cdot P123G)$$

$$ADD = IR14\,(EIR \cdot \overline{IR12} \cdot \overline{IR13})$$

$$ADF = (ASG \cdot T4T5) + [T1T2\,(JSB \cdot PH3)] + [ADD + ISZ\,(PH3 \cdot T3T4)] + (PH4 \cdot T3T4) + (P123 \cdot T6T7)$$

$$ANF = \overline{IR11}\,(PH3 \cdot T3T4)\,(EIR \cdot \overline{IR14} \cdot \overline{IR13} \cdot IR12)$$

$$ASG = IR1\emptyset\,[\overline{IR15}\,(PH1 \cdot \overline{IR14}\,(\overline{IR12} \cdot \overline{IR13} \cdot EIR))]$$

$$BAF = TB\emptyset\,(T\emptyset \cdot P123G)\,[\overline{TB14} \cdot \overline{TB2}\,(\overline{TB3} \cdot \overline{TB1})]\,[TAN2 \cdot TAN3\,(\overline{TB12} \cdot \overline{TB13})]$$

$$C\emptyset = CFF \cdot T6T7$$

$$C1 = (RB\emptyset \cdot SB\emptyset) + (RB\emptyset \cdot C\emptyset) + (SB\emptyset \cdot C\emptyset)$$

$$C2 = (RB1 \cdot SB1) + (RB1 \cdot C1) + (SB1 \cdot C1)$$

$$C3 = (RB2 \cdot SB2) + (RB2 \cdot C2) + (SB2 \cdot C2)$$

$$C4 = (RB3 \cdot SB3) + (RB3 \cdot C3) + (SB3 \cdot C3)$$

$$C5 = (RB4 \cdot SB4) + (RB4 \cdot C4) + (SB4 \cdot C4)$$

$$C6 = (RB5 \cdot SB5) + (RB5 \cdot C5) + (SB5 \cdot C5)$$

$$C7 = (RB6 \cdot SB6) + (RB6 \cdot C6) + (SB6 \cdot C6)$$

$$C8 = (RB7 \cdot SB7) + (RB7 \cdot C7) + (SB7 \cdot C7)$$

$$C9 = (RB8 \cdot SB8) + (RB8 \cdot C8) + (SB8 \cdot C8)$$

$$C1\emptyset = (RB9 \cdot SB9) + (RB9 \cdot C9) + (SB9 \cdot C9)$$

$$C11 = (RB1\emptyset \cdot SB1\emptyset) + (RB1\emptyset \cdot C1\emptyset) + (SB1\emptyset \cdot C1\emptyset)$$

$$C12 = (RB11 \cdot SB11) + (RB11 \cdot C11) + (SB11 \cdot C11)$$

$$C13 = (RB12 \cdot SB12) + (RB12 \cdot C12) + (SB12 \cdot C12)$$

$$C14 = (RB13 \cdot SB13) + (RB13 \cdot C13) + (SB13 \cdot C13)$$

$$C15 = (RB14 \cdot SB14) + (RB14 \cdot C14) + (SB14 \cdot C14)$$

$$C16 = (RB15 \cdot SB15) + (RB15 \cdot C15) + (SB15 \cdot C15)$$

$$\begin{aligned} CFF = ASG \Big\{ & [\overline{TR\emptyset}\,(TAN1 \cdot TAN2 \cdot TAN3 \cdot TAN4 \cdot T5) + (TR4 \cdot T4 \cdot \overline{RB15}) + \\ & (TR3 \cdot T4 \cdot \overline{RB\emptyset}) + (TR5 \cdot T3 \cdot \overline{EFF})] + \\ & [TR\emptyset\,[(\overline{TAN1 \cdot TAN2 \cdot TAN3 \cdot TAN4 \cdot T5}) \cdot \\ & (\overline{TR4 \cdot T4 \cdot RB15}) \cdot (\overline{TR3 \cdot T4 \cdot RB\emptyset}) \cdot \\ & (\overline{TR5 \cdot T3 \cdot EFF})]\,[\overline{TR1} \cdot \overline{TR3} \cdot T5\,(\overline{TR4 + TR5}) + \\ & (TR1 \cdot T5) + (TR4 \cdot T4) + (TR5 \cdot T3)]\,]\Big\} + \\ & [T4 \cdot PH3 \cdot CPR\,(\overline{TAN1 \cdot TAN2 \cdot TAN3 \cdot TAN4})] + \\ & (T4 \cdot PH3 \cdot ISZ \cdot C16) + \\ & (T4 \cdot SKF) + \\ & (TR3 \cdot SRG \cdot \overline{RB\emptyset} \cdot T4) \end{aligned}$$

CL1 = CF1 · CF2

CL2 = CF1 · $\overline{CF2}$

CLC = TR11 [T4 · IOG (TR6 · TR7 · TR8)]

CLF = TR9 (T4 · IOG)

CMF = [ASG · T3(TR9)] + [PH4 (T1T2 + T5)]

CPR = EIR · IR14 · $\overline{IR13}$ · IR12

CRS = POPIO + [CLC (IOG · SCMØ · SCLØ]

CTFF = STC · SC Typical Interface

$\overline{CTFF}$ = CRS + (CLC · SC) Typical Interface

DMS = $\overline{RF2}$ · DISPLAY MEMORY SW · $\overline{POFP}$

EFF = [C16 (TR2B · ASG · T5) + (T4 · PH3 · ADD)] +
[R15B (SRG (TRØ · TR1 · TR2) + (TR6 · TR7 · TR8))] +
($\overline{TR6}$ · TR7 · T3 · ASG) + (TR6 · TR7 · ASG · T3) +
[RBØB (SRG (TRØ · $\overline{TR1}$ · TR2) + (TR6 · $\overline{TR7}$ · TR8))]

$\overline{EFF}$ = [$\overline{RBØ}$ (SRG (TRØ · $\overline{TR1}$ · TR2) + (TR6 · $\overline{TR7}$ · TR8))]
+ [$\overline{RB15}$ (SRG (TRØ · TR1 · TR2) + (TR6 · TR7 · TR8))]
+ (ASG · T3 · TR7 · $\overline{TR6}$) + (SRG · T4 · TR5) +
(ASG · TR6 · $\overline{TR7}$ · T3)

EIR = $\overline{IIR}$ [$\overline{PH3}$ + ($\overline{DMS}$ · $\overline{LMS}$)]

ENF = T2 (Buffered)

EOF = (T2 · SEO) + (P123 · TØT1) +
(PH3 · T3T4)[($\overline{IR11}$ · XOR) + LOD + CPR + JSB)] +
[$\overline{TR9}$ (ASG · T3)] + [IR12 · $\overline{CPR}$ (PH3 · T5)] +
(STR + PH3 · T2)

EPH = $\overline{PH5}$ · $\overline{IIR}$

ESR = ICFF ($\overline{POPIO}$ · ISEFF · $\overline{HIS}$)

FBFF = POPIO + (STF · SC) + EOF Typical Interface

$\overline{FBFF}$ = (CLF · SC) + (IAK · IRQFF) Typical Interface

FLFF = ENF · FBFF Typical Interface

$\overline{FLFF}$ = CLF · SC Typical Interface

HIN = IOG ($\overline{TR8}$ · $\overline{TR7}$ · $\overline{TR6}$)

HLS = HALT SW.

$\overline{HLS}$ = $\overline{HALT\ SW.}$ + POFP

IAK = ICFF (T1 · PH1)

ICFF = $\overline{ITFF}$

$\overline{ICFF}$ = CRS + (PH4 · T3B) + [$\overline{PH5}$ (T5 · IOGE (STC + CLC + STF + CLF))]

$$
\begin{aligned}
\text{IEN6} &= \text{ISEFF} \\
\text{IEN1}\emptyset &= \text{PRH1}\emptyset \cdot \text{ISEFF} \\
\text{IEN2}\emptyset &= \text{IEN6 (PRH1}\emptyset \cdot \text{PRL17)} \\
\text{INT} &= \text{ESR (FLG}\emptyset + \text{FLG1} + \text{FLG2} + \text{FLG3)} \\
\text{IOBO}\emptyset\text{-15} &= \text{IOCO} \cdot \text{RB}\emptyset\text{-15} \\
\text{IOCO} &= \overline{\text{TR6}} \cdot \text{TR7} \cdot \text{TR8 (IOG} \cdot \text{T4T5)} \\
\text{IOF} &= (\text{IOG} \cdot \text{T4T5}) + [\overline{\text{IR11}}\ (\overline{\text{IR14}} \cdot \overline{\text{IR13}} \cdot \overline{\text{IR12}})\ (\text{PH3} \cdot \text{T3T4})] \\
\text{IOG} &= \text{IR1}\emptyset\ [\text{IR15 (PH1} \cdot \overline{\text{IR14}}\ (\text{EIR} \cdot \overline{\text{IR12}} \cdot \overline{\text{IR13}}))] \\
\text{IOGE} &= \text{IOG} \cdot \overline{\text{MPC}} \\
\text{IOI} &= [(\text{T4T5} \cdot \text{IOG})\ (\overline{\text{TR7}}\ (\text{IOG} \cdot \text{TR8}))] + (\text{SEO} \cdot \text{T2}) \\
\text{IOO} &= \text{T3T4}\ (\overline{\text{TR6}} \cdot \text{TR7} \cdot \text{TR8}) \\
\text{IOS} &= \text{IOG} \cdot \text{SCM}\emptyset \cdot \text{SCL1} \\
\text{IRQFF} &= \text{SIR} \cdot \text{PRH} \cdot \text{FBFF (FLFF} \cdot \text{IEN} \cdot \text{CTFF)} \\
\overline{\text{IRQFF}} &= \text{ENF} \\
\text{ISEFF} &= \text{STF (SCM}\emptyset \cdot \text{SCL}\emptyset \cdot \text{IOG)} \\
\overline{\text{ISEFF}} &= \text{CLF (SCM}\emptyset \cdot \text{SCL}\emptyset \cdot \text{IOG)} \\
\text{ISR} &= \text{SEO} + [\text{IOS}\ (\overline{\text{TR7}}\ (\text{IOG} \cdot \text{TR8}))] \\
\text{ISZ} &= \text{IR11 (EIR} \cdot \text{IR12} \cdot \text{IR13} \cdot \overline{\text{IR14}}) \\
\text{ITFF} &= \text{STM 12-15} \\
\text{JMP} &= \text{IR11 (EIR} \cdot \overline{\text{IR12}} \cdot \text{IR13} \cdot \overline{\text{IR14}}) \\
\text{JSB} &= \text{IR11 (EIR} \cdot \text{IR12} \cdot \overline{\text{IR13}} \cdot \overline{\text{IR14}}) \\
\text{LADS} &= \text{LOAD ADDRESS SW} \cdot \overline{\text{RF2}} \cdot \overline{\text{POFP}} \\
\text{LAS} &= \text{LOAD A SW} \cdot \overline{\text{RF2}} \cdot \overline{\text{POFP}} \\
\text{LBS} &= \text{LOAD B SW} \cdot \overline{\text{RF2}} \cdot \overline{\text{POFP}} \\
\text{LMS} &= \text{LOAD MEMORY SW} \cdot \overline{\text{RF2}} \cdot \overline{\text{POFP}} \\
\text{LOD} &= \overline{\text{IR12}}\ (\text{EIR} \cdot \text{IR13} \cdot \text{IR14}) \\
\text{MAC} &= \overline{\text{IR10}}\ [\text{IR15 (}\overline{\text{IR14}} \cdot \text{PH1 (EIR} \cdot \overline{\text{IR12}} \cdot \overline{\text{IR13}}))] \\
\text{MIT} &= \text{MTE} \Big\{ (\text{T4T5}\ (\overline{\text{PH3} \cdot \text{ISZ}})) + \\
&\qquad (\text{T3T4} \cdot \text{CF2}\ (\overline{\text{PH3} \cdot \text{ISZ}})) + \\
&\qquad (\text{T5T6} \cdot \text{CF2 (PH3} \cdot \text{ISZ)}) + \\
&\qquad (\text{PH3} \cdot \text{ISZ})\ [(\text{S67 (PH3} \cdot \text{ISZ)}\ (\overline{\text{T0T1}} \cdot \overline{\text{T6T7}})) + \\
&\qquad (\text{T5T6} \cdot \overline{\text{T4T5}}\ (\text{PH3} \cdot \text{ISZ}))] \Big\}
\end{aligned}
$$

$$
\begin{aligned}
MPT &= LPS \cdot M6 \cdot M7 \cdot M8 \cdot M9 \cdot M1\emptyset \cdot M11 \\
&\quad [(M12 \cdot M14 \cdot TTK \cdot MPT1 \cdot MPT2) + \\
&\quad (M12 \cdot \overline{M13} \cdot \overline{M14} \cdot MPT1 \cdot \overline{MPT2}) + \\
&\quad (M12 \cdot M13 \cdot \overline{M14} \cdot \overline{MPT3}) + \\
&\quad (M12 \cdot M13 \cdot M14 \cdot MPT3 \cdot \overline{MPT4}) + \\
&\quad (M12 \cdot M13 \cdot M14 \cdot TTK \cdot MPT4)] \\
MRT &= MTE\ [T\emptyset + (T\emptyset T1 \cdot \overline{CF2}) + (T1T2 \cdot CF2)] \\
MST &= [T2(MRT + (MTE \cdot \overline{CF1}))] \quad [(\overline{LMS + ISG})\ (\overline{AAF + BAF}) \\
&\quad (PH3\ (\overline{JSB + STR}))] \\
MTE &= P123B \cdot \overline{MPT}\ (MNS) \\
MWL &= (PH3 \cdot ISZ) + [(LMS + ISG) + (AAF + BAF) + (PH3 + (JSB + STR))] \\
MWT &= MTE\ [(S67\ (PH3 \cdot ISZ)\ (\overline{T\emptyset T1} \cdot \overline{T6T7})) + \\
&\quad (T5T6 \cdot \overline{T4T5}\ (PH3 \cdot ISZ)) + (T4T5\ (\overline{PH3 \cdot ISZ}))] \\
OPO &= \overline{IR14} \cdot PH1\ (EIR \cdot \overline{IR12} \cdot \overline{IR13}) \\
\overline{OPO} &= IR14 + \overline{PH1} + (\overline{EIR} + IR12 + IR13) \\
OVFF &= (STF \cdot IOS) + [(ADD \cdot PH3 \cdot T4) + (TR2B \cdot ASG \cdot T5) \cdot \\
&\quad (TR15 \cdot \overline{RB15} \cdot \overline{SB15}) + (SB15 \cdot RB15B \cdot \overline{TB15})] \\
\overline{OVFF} &= CLF \cdot IOS \\
P123 &= (PH1FF + PH2FF + PH3FF)\ (RF2 \cdot EPH) \\
PH1 &= (PH1FF\ (RF2 \cdot EPH) \\
PH1FF &= (JMP \cdot PH2 \cdot \overline{TR15} \cdot \overline{PH4FF}) + \\
&\quad (\overline{PH4FF} \cdot PH3) + \\
&\quad (PRSFF + POFP) + \\
&\quad (PH4) \\
\overline{PH1FF} &= PH2FF + PH3FF + PH4FF \\
PH2 &= PH2FF\ (RF2 \cdot EPH) \\
PH2FF &= (TR15 \cdot PH1 \cdot \overline{PH4FF} \cdot \overline{OPO}) + (PH2 \cdot TR15) \\
\overline{PH2FF} &= PH1FF + PH3FF + PH4FF \\
PH3 &= PH3FF\ (RF2 \cdot EPH) \\
PH3FF &= (\overline{OPO} \cdot PH1\ (\overline{TR15} \cdot \overline{PH4FF} \cdot \overline{JMP})) + \\
&\quad (PH2\ (\overline{TR15} \cdot \overline{PH4FF} \cdot \overline{JMP})) + \\
&\quad [(LMS + DMS)\ (S1FF \cdot \overline{S2FF})] \\
\overline{PH3FF} &= PH1FF + PH2FF + PH4FF
\end{aligned}
$$

$$
\begin{aligned}
PH4 &= PH4FF(\,RF2 \cdot EPH) \\
PH4FF &= [INT \cdot RUN1\ (\overline{JSB} \cdot \overline{JMP})] + \\
&\quad (RUN1 \cdot INT \cdot \overline{IR15}) \\
\overline{PH4FF} &= PH1FF \\
POPIO &= T5\ (PRSFF + POFP) \\
PRS &= PRESET\ SW \cdot \overline{RF2} \\
\overline{PRS} &= \overline{PRESET\ SW.} + POFP \\
RARB &= AAF\ [(\overline{JSB} \cdot \overline{PH3})\ (P123 \cdot T1)] + \\
&\quad \overline{IR11} \Big\{ [(PH3 \cdot \overline{IR14} \cdot \overline{IR11} \cdot EIR)\ (PH3 \cdot T3T4)] + \\
&\qquad [CPR\ (PH3 \cdot T3T4)] + \\
&\qquad [ADD\ (PH3 \cdot T3T4)] + \\
&\qquad [(T3) + (T4T5)\ (SRG + (IOG \cdot \overline{TR6}))] + \\
&\qquad [\overline{TR8}\ (ASG \cdot T3)] + \\
&\qquad (STR \cdot PH3 \cdot T2) + \\
&\qquad (ASG \cdot T4T5) \Big\} \\
RB\emptyset &= RARB\ (AR\emptyset) + \\
&\quad RBRB\ (BR\emptyset) + \\
&\quad RPRB\ (PR\emptyset) + \\
&\quad ISZ\ (PH3 \cdot T3T4) \\
RB1\text{-}15 &= RARB\ (AR1\text{-}15) + \\
&\quad RBRB\ (BR1\text{-}15) + \\
&\quad RPRB\ (PR1\text{-}15) \\
RBRB &= BAF\ [(\overline{JSB} \cdot \overline{PH3})\ (P123 \cdot T1)] + \\
&\quad IR11 \Big\{ [(PH3 \cdot \overline{IR14} \cdot \overline{IR11} \cdot EIR)\ (PH3 \cdot T3T4)] + \\
&\qquad [CPR\ (PH3 \cdot T3T4)] + \\
&\qquad [ADD\ (PH3 \cdot T3T4)] + \\
&\qquad [(T3) + (T4T5)\ (SRG + (IOG \cdot \overline{TR6}))] + \\
&\qquad [\overline{TR8}\ (ASG \cdot T3)] + \\
&\qquad (STR \cdot PH3 \cdot T2) + \\
&\qquad (ASG \cdot T4T5) \Big\} \\
RF1 &= RNS\ (S1FF \cdot \overline{S2FF}) \cdot T5 \\
\overline{RF1} &= HLSFF + T5\ (PEH + HIN) \\
RF2 &= (S1FF \cdot S2FF)\ T7S \\
\overline{RF2} &= PRSFF + POFP + \overline{RF1}\ (T7S) \\
RL4 &= SRG\ [(TR\emptyset \cdot TR1 \cdot TR2) + (TR6 \cdot TR7 \cdot TR8)]
\end{aligned}
$$

$$
\begin{aligned}
\text{RLL} &= \text{SRG}\,[(\overline{\text{TR}\emptyset}\cdot \text{TR1}\cdot \overline{\text{TR2}}) + (\overline{\text{TR6}}\cdot \text{TR7}\cdot \overline{\text{TR8}})]\\
\text{RMSB} &= (\text{T}\emptyset\cdot \text{P123}) + [\text{T3T4}(\text{PH3}\cdot \text{JSB})]\\
\text{RNS} &= \text{RUN SW.}\cdot \overline{\text{POFP}}\\
\overline{\text{RNS}} &= \overline{\text{RUN SW.}} + \text{POFP}\\
\text{RPB} &= \text{P123B}\cdot \text{T}\emptyset\cdot \text{TS}\\
\text{RPE} &= \text{PRSFF} + \text{POFP}\\
\text{RPRB} &= (\text{PH4}\cdot \text{T3T4}) + (\text{PH3}\cdot \text{T6T7}) +\\
&\quad (\text{OPO}\cdot \text{T6T7}) + [\text{T1T2}\,(\text{JSB}\cdot \text{PH3})] +\\
&\quad [\text{PH4}\,(\text{T1T2} + \text{T5})]\\
\text{RRS} &= \text{SRG}\,[(\text{TR}\emptyset\cdot \text{TR1}\cdot \overline{\text{TR2}}) + (\text{TR6}\cdot \text{TR7}\cdot \overline{\text{TR8}})]\\
\text{RSM6-9} &= \text{T7}\cdot \text{PH4}\\
\text{RSM10-15} &= \text{RSM6-9} + [(\text{TS}\cdot \text{PH1}\cdot \overline{\text{IR10}}\cdot \overline{\text{OPO}})\ \text{T7}]\\
\text{RST} &= \text{TS}(\text{T}\emptyset\cdot \text{P123})\\
\text{RTSB} &= \text{EIR}\cdot \overline{\text{JSB}}\ (\text{PH3}\cdot \text{T3T4}) +\\
&\quad \text{T6T7}\,[\text{PH2} + (\text{PH1}\cdot \overline{\text{OPO}})] +\\
&\quad \text{CPR}\cdot \text{IR12}\ (\text{PH3}\cdot \text{T5})\\
\text{S1FF} &= \text{T2}\ (\text{RNS} + \text{SCS} + \text{LMS} + \text{DMS})\\
\text{S2FF} &= \text{S1FF}\cdot \text{T1}\\
\text{SB}\emptyset &= (\text{RMSB}\cdot \text{MR}\emptyset) + (\text{RTSB}\cdot \text{TR}\emptyset) +\\
&\quad (\text{IOI}\cdot \text{IOBI}\emptyset) +\\
&\quad (\overline{\text{T6T7}\cdot \text{ILS}})\ \{[(\text{PH4}\cdot \text{T3T4}) + (\text{PH3}\cdot \text{T6T7}) +\\
&\quad (\text{OPO}\cdot \text{T6T7})] +\\
&\quad [\text{T1T2}\,(\text{PH3}\cdot \text{JSB})] +\\
&\quad [\text{TR2}\,(\text{ASG}\cdot \text{T4T5})]\}\\
\text{SB1-15} &= (\text{RMSB}\cdot \text{MR1-15}) +\\
&\quad (\text{RTSB}\cdot \text{TR1-15}) +\\
&\quad (\text{IOI}\cdot \text{IOBI 1-15})\\
\text{SCL}\emptyset &= \overline{\text{TR}\emptyset}\cdot \overline{\text{TR1}}\cdot \overline{\text{TR2}}\cdot \overline{\text{PH5}}\\
\text{SCL1} &= \text{TR}\emptyset\cdot \overline{\text{TR1}}\cdot \overline{\text{TR2}}\cdot \overline{\text{PH5}}\\
\text{SCL2} &= \overline{\text{TR}\emptyset}\cdot \text{TR1}\cdot \overline{\text{TR2}}\cdot \overline{\text{PH5}}\\
\text{SCL3} &= \text{TR}\emptyset\cdot \text{TR1}\cdot \overline{\text{TR2}}\cdot \overline{\text{PH5}}\\
\text{SCL4} &= \overline{\text{TR}\emptyset}\cdot \overline{\text{TR1}}\cdot \text{TR2}\cdot \overline{\text{PH5}}\\
\text{SCL5} &= \text{TR}\emptyset\cdot \overline{\text{TR1}}\cdot \text{TR2}\cdot \overline{\text{PH5}}
\end{aligned}
$$

SCL6 = $\overline{TR\emptyset} \cdot TR1 \cdot TR2 \cdot \overline{PH5}$

SCL7 = $TR\emptyset \cdot TR1 \cdot TR2 \cdot \overline{PH5}$

SCM$\emptyset$ = $\overline{TR3} \cdot \overline{TR4} \cdot \overline{TR5} \cdot \overline{PH5}$

SCM1 = $TR3 \cdot \overline{TR4} \cdot \overline{TR5} \cdot \overline{PH5}$

SCM2 = $\overline{TR3} \cdot TR4 \cdot \overline{TR5} \cdot \overline{PH5}$

SCM3 = $TR3 \cdot TR4 \cdot \overline{TR5} \cdot \overline{PH5}$

SCM4 = $\overline{TR3} \cdot \overline{TR4} \cdot TR5 \cdot \overline{PH5}$

SCM5 = $TR3 \cdot \overline{TR4} \cdot TR5 \cdot \overline{PH5}$

SCM6 = $\overline{TR3} \cdot TR4 \cdot TR5 \cdot \overline{PH5}$

SCM7 = $TR3 \cdot TR4 \cdot TR5 \cdot \overline{PH5}$

SCS = SINGLE CYCLE SW $\cdot \overline{RF2} \cdot \overline{POFP}$

SEO = LMS + LADS + [LAS + (AAF $\cdot$ LMS)] +
[LBS + (BAF $\cdot$ LMS)]

SFC = IOG ($\overline{TR6} \cdot TR7 \cdot \overline{TR8}$)

SFS = IOG ($TR6 \cdot TR7 \cdot \overline{TR8}$)

SIR = T5 (Buffered)

SKF = (SFS $\cdot$ IOS $\cdot$ OVFF) +
(SFC $\cdot$ IOS $\cdot \overline{OVFF}$) +
SFS $\cdot$ ISEFF (IOGE $\cdot$ SCM$\emptyset \cdot$ SCL$\emptyset$) +
SFC $\cdot \overline{ISEFF}$ (IOGE $\cdot$ SCM$\emptyset \cdot$ SCL$\emptyset$) +
SFS $\cdot$ FLFF (IOGE $\cdot$ SCM- $\cdot$ SCL-) +
SFC $\cdot \overline{FLFF}$ (IOGE $\cdot$ SCM- $\cdot$ SCL-)

SL14 = SRG [($\overline{TR\emptyset} \cdot TR1 \cdot TR2$) + ($\overline{TR6} \cdot TR7 \cdot TR8$)] +
SRG [($\overline{TR\emptyset} \cdot TR1 \cdot \overline{TR2}$) + ($\overline{TR6} \cdot TR7 \cdot \overline{TR8}$)]

SLM = SRG ($\overline{TR6} + \overline{TR\emptyset}$)

SRG = $\overline{IR1\emptyset}$ [$\overline{IR15}$ (PH1 $\cdot$ IR14 ($\overline{IR12} \cdot \overline{IR13} \cdot$ EIR))]

SRM = SRG [($TR6 \cdot \overline{TR8}$) + ($\overline{TR\emptyset \cdot TR2}$) +
($TR6 \cdot \overline{TR7}$) + ($TR\emptyset \cdot \overline{TR1}$)]

ST$\emptyset$-16 = MST $\cdot$ SA$\emptyset$-16

$$
\begin{aligned}
\text{STBA} &= \text{SWSA} + \text{T4}\,(\overline{\text{IR14}} \cdot \overline{\text{IR11}} \cdot \text{EIR}) + \\
&\quad \text{AAF}\,[\overline{\text{CPR}} \cdot \text{IR12}\,(\text{PH3} \cdot \text{T5})] + \overline{\text{IR11}} \\
&\quad \Big\{(\text{TR2} \cdot \text{ASG} \cdot \text{T5}) + \\
&\quad (\text{TR4} \cdot \text{SRG} \cdot \text{T5}) + \\
&\quad (\overline{\text{TR7}} \cdot \text{TR8} \cdot \text{IOG}) + \\
&\quad (\text{TR9} \cdot \text{SRG} \cdot \text{T3}) + \\
&\quad (\text{ASG} \cdot \text{T3}) + \\
&\quad [\overline{\text{IR12}} \cdot \text{IR14} \cdot \text{EIR}\,(\text{T4} \cdot \text{PH3})]\Big\} \\
\text{STBB} &= \text{SWSB} + \text{BAF}\,[\overline{\text{CPR}} \cdot \text{IR12}\,(\text{PH3} \cdot \text{T5})] + \\
&\quad \text{IR11}\,\Big\{(\text{TR2}\quad \text{ASG}\quad \text{T5}) + \\
&\qquad (\text{TR4} \cdot \text{SRG} \cdot \text{T5}) + \\
&\qquad (\overline{\text{TR7}} \cdot \text{TR8} \cdot \text{IOG}) + \\
&\qquad (\text{TR9} \cdot \text{SRG} \cdot \text{T3}) + \\
&\qquad (\text{ASG} \cdot \text{T3}) + \\
&\qquad [\overline{\text{IR12}} \cdot \text{IR14} \cdot \text{EIR}\,(\text{T4} \cdot \text{PH3})]\Big\} \\
\text{STBT} &= \text{SWST} + (\text{AAF} + \text{BAF}\,(\text{P123} \cdot \text{T1})] + \\
&\quad [\text{STR} + \text{JSB}\,(\text{PH3} \cdot \text{T2})] + \\
&\quad (\text{ISZ} \cdot \text{T4} \cdot \text{PH3}) \\
\text{STC} &= \overline{\text{TR11}}\,[\text{T4} \cdot \text{IOG}\,(\text{TR6} \cdot \text{TR7} \cdot \text{TR8})] \\
\text{STF} &= \text{T3}\,(\text{TR6} \cdot \overline{\text{TR7}} \cdot \overline{\text{TR8}}) \\
\text{STM1}\emptyset\text{-15} &= \text{SWSM} + \text{T7}\,(\text{OPO} + \text{PH2} + \text{PH3}) \\
\text{STM6-9} &= \text{STM1}\emptyset\text{-15} + (\text{T7} \cdot \text{PH1} \cdot \text{OPO} \cdot \text{EIR}) \\
\text{STM}\emptyset\text{-5} &= \text{STM6-9} + (\text{T7} \cdot \text{PH4}) \\
\text{STP1}\emptyset\text{-15} &= \text{SWSP} + (\overline{\text{IR1}\emptyset} \cdot \text{JMP} \cdot \text{T5} \cdot \text{PH1}) + \\
&\quad [\text{PH4}\,(\text{T2} + \text{T4T5})] + [\text{T4}\,(\text{PH3} \cdot \text{JSB})] + \\
&\quad \Big\{\text{T7}\,[\text{OPO} + \text{PH3} + (\text{PH2} \cdot \text{JMP} \cdot \overline{\text{TR15}})]\Big\} \\
\text{STP}\emptyset\text{-9} &= \text{STP1}\emptyset\text{-15} + (\text{PH1} \cdot \text{T7} \cdot \text{JMP} \cdot \overline{\text{TR15}}) \\
\text{STR} &= \text{IR12}\,(\text{EIR} \cdot \text{IR13} \cdot \text{IR14}) \\
\text{SWSA} &= \text{T2}\,[\text{LAS} + (\text{AAF} \cdot \text{LMS})] \\
\text{SWSB} &= \text{T2}\,[\text{LBS} + (\text{BAF} \cdot \text{LMS})] \\
\text{SWSM} &= \text{T2} \cdot \text{LADS} \\
\text{SWSP} &= \text{T2} \cdot \text{LADS} \\
\text{SWST} &= \text{T2} \cdot \text{LMS} \\
\text{S67} &= (\overline{\text{T1T2}} \cdot \overline{\text{T3T4}})\ \Big\{\overline{\text{T7T}\emptyset}\,[(\overline{\text{PH3}} + \overline{\text{ISZ}}) + (\overline{\text{T5T6}})]\Big\}
\end{aligned}
$$

$T\emptyset = T7T\emptyset \cdot T\emptyset T1$

$T\emptyset T1 = T7T\emptyset \cdot CL1$

$T1 = T\emptyset T1 \cdot T1T2$

$T1T2 = T\emptyset T1 \cdot CL2$

$T2 = T1T2 \cdot T2T3$

$T2T3 = T1T2 \cdot CL1$

$T3 = T2T3 \cdot T3T4$

$T3T4 = T2T3 \cdot CL2$

$T4 = T3T4 \cdot T4T5$

$T4T5 = T3T4 \cdot CL1$

$T5 = T4T5 \cdot T5T6$

$T5T6 = T4T5 \cdot CL2$

$T6 = T5T6 \cdot T6T7$

$T6T7 = S67 \cdot CL1$

$T7 = T6T7 \cdot T7T\emptyset$

$T7T\emptyset = T6T7 \cdot CL2$

$TAN1 = \overline{TB\emptyset} \cdot \overline{TB1} \cdot \overline{TB2} \cdot \overline{TB3}$

$TAN2 = \overline{TB4} \cdot \overline{TB5} \cdot \overline{TB6} \cdot \overline{TB7}$

$TAN3 = \overline{TB8} \cdot \overline{TB9} \cdot \overline{TB1\emptyset} \cdot \overline{TB11}$

$TAN4 = \overline{TB12} \cdot \overline{TB13} \cdot \overline{TB14} \cdot \overline{TB15}$

$TB\emptyset = ADF\ [(RB\emptyset \cdot SB\emptyset \cdot C\emptyset) +$
$(RB\emptyset \cdot \overline{SB\emptyset} \cdot \overline{C\emptyset}) +$
$(\overline{RB\emptyset} \cdot SB\emptyset \cdot \overline{C\emptyset})] +$
$EOF\ [(\overline{RB\emptyset} \cdot SB\emptyset) +$
$(RB\emptyset \cdot \overline{SB\emptyset})] +$
$IOF\ (RB\emptyset + SB\emptyset) +$
$ANF\ (RB\emptyset \cdot SB\emptyset) +$
$CMF \cdot \overline{RB\emptyset} +$
$SRM\ (RB1 + SB1) +$
$RL4\ (RB12 + SB12) +$
$RLL\ (RB15 + SB15) +$
$RSM6\text{-}9 \cdot SRAX1, X3, X5 \text{ or } X7$
$EFF \cdot SRG\ [(T3 \cdot \overline{TR6} \cdot TR7 \cdot TR8) + (T5 \cdot \overline{TR\emptyset} \cdot TR1 \cdot TR2)]$

TB1 = ADF $[(RB1 \cdot SB1 \cdot C1) + (RB1 \cdot \overline{SB1} \cdot \overline{C1}) + (\overline{RB1} \cdot SB1 \cdot \overline{C1})]$ +
EOF $[(\overline{RB1} \cdot SB1) + (RB1 \cdot \overline{SB1})]$ +
IOF (RB1 + SB1) +
ANF (RB1 · SB1) +
CMF · $\overline{RB1}$ +
SRM (RB2 + SB2) +
SLM (RBØ + SBØ) +
RL4 (RB13 + SB13) +
RSM6-9 · SRAX2, X3, X6 or X7

TB2 = ADF $[(RB2 \cdot SB2 \cdot C2) + (RB2 \cdot \overline{SB2} \cdot \overline{C2}) + (\overline{RB2} \cdot SB2 \cdot \overline{C2})]$ +
EOF $[(\overline{RB2} \cdot SB2) + (RB2 \cdot \overline{SB2})]$ +
IOF (RB2 + SB2) +
ANF (RB2 · SB2) +
CMF · $\overline{RB2}$ +
SRM (RB3 + SB3) +
SLM (RB1 + SB1) +
RL4 (RB14 + SB14) +
RSM6-9 · SRAX4, X5, X6 or X7

TB3 = ADF $[(RB3 \cdot SB3 \cdot C3) + (RB3 \cdot \overline{SB3} \cdot \overline{C3}) + (\overline{RB3} \cdot SB3 \cdot \overline{C3})]$ +
EOF $[(\overline{RB3} \cdot SB3) + (RB3 \cdot \overline{SB3})]$ +
IOF (RB3 + SB3) +
ANF (RB3 · SB3) +
CMF · $\overline{RB3}$ +
SLM (RB2 + SB2) +
SRM (RB4 + SB4) +
RL4 (RB15 + SB15) +
RSM6-9 · SRA1X, 3X, 5X or 7X

$$
\begin{aligned}
TB4 = {} & ADF\,[(RB4 \cdot SB4 \cdot C4) + (RB4 \cdot \overline{SB4} \cdot \overline{C4}) + \\
& (\overline{RB4} \cdot SB4 \cdot \overline{C4})] + \\
& EOF\,[(\overline{RB4} \cdot SB4) + (RB4 \cdot \overline{SB4})] + \\
& IOF\,(RB4 + SB4) + \\
& ANF\,(RB4 \cdot SB4) + \\
& CMF \cdot \overline{RB4} + \\
& SRM\,(RB5 + SB5) + \\
& SLM\,(RB3 + SB3) + \\
& RL4\,(RB\emptyset + SB\emptyset) + \\
& RSM6\text{-}9 \cdot SRA2X, 3X, 5X \text{ or } 7X
\end{aligned}
$$

$$
\begin{aligned}
TB5 = {} & ADF\,[(RB5 \cdot SB5 \cdot C5) + (RB5 \cdot \overline{SB5} \cdot \overline{C5}) + \\
& (\overline{RB5} \cdot SB5 \cdot \overline{C5})] + \\
& EOF\,[(RB5 \cdot \overline{SB5}) + (\overline{RB5} \cdot SB5)] + \\
& IOF\,(RB5 + SB5) + \\
& ANF\,(RB5 \cdot SB5) + \\
& CMF \cdot \overline{RB5} + \\
& SRM\,(RB6 + SB6) + \\
& SLM\,(RB4 + SB4) + \\
& RL4\,(RB1 + SB1) + \\
& RSM6\text{-}9 \cdot SRA4X, 5X, 6X \text{ or } 7X
\end{aligned}
$$

$$
\begin{aligned}
TB6 = {} & ADF\,[(RB6 \cdot SB6 \cdot C6) + (RB6 \cdot \overline{SB6} \cdot \overline{C6}) + \\
& (\overline{RB6} \cdot SB6 \cdot \overline{C6})] + \\
& EOF\,[(\overline{RB6} \cdot SB6) + (RB6 \cdot \overline{SB6})] + \\
& IOF\,(RB6 + SB6) + \\
& ANF\,(RB6 \cdot SB6) + \\
& CMF \cdot \overline{RB6} + \\
& SRM\,(RB7 + SB7) + \\
& SLM\,(RB5 + SB5) + \\
& RL4\,(RB2 + SB2) +
\end{aligned}
$$

$$
\begin{aligned}
TB7 = {} & ADF\,[(RB7 \cdot SB7 \cdot C7) + (RB7 \cdot \overline{SB7} \cdot \overline{C7}) + \\
& \quad (\overline{RB7} \cdot SB7 \cdot \overline{C7})] + \\
& EOF\,[(RB7 \cdot \overline{SB7}) + (\overline{RB7} \cdot SB7)] + \\
& IOF\,(RB7 + SB7) + \\
& ANF\,(RB7 \cdot SB7) + \\
& CMF \cdot \overline{RB7} + \\
& SRM\,(RB8 + SB8) + \\
& SLM\,(RB6 + SB6) + \\
& RL4\,(RB3 + SB3) + \\
TB8 = {} & ADF\,[(RB8 \cdot SB8 \cdot C8) + (RB8 \cdot \overline{SB8} \cdot \overline{C8}) + \\
& \quad (\overline{RB8} \cdot SB8 \cdot \overline{C8})] + \\
& EOF\,[(RB8 \cdot \overline{SB8}) + (\overline{RB8} \cdot SB8)] + \\
& IOF\,(RB8 + SB8) + \\
& ANF\,(RB8 \cdot SB8) + \\
& CMF \cdot \overline{RB8} + \\
& SRM\,(RB9 + SB9) + \\
& SLM\,(RB7 + SB7) + \\
& RL4\,(RB4 + SB4) \\
TB9 = {} & ADF\,[(RB9 \cdot SB9 \cdot C9) + (RB9 \cdot \overline{SB9} \cdot \overline{C9}) + \\
& \quad (\overline{RB9} \cdot SB9 \cdot \overline{C9})] + \\
& EOF\,[(RB9 \cdot \overline{SB9}) + (\overline{RB9} \cdot SB9)] + \\
& IOF\,(RB9 + SB9) + \\
& ANF\,(RB9 \cdot SB9) + \\
& CMF \cdot \overline{RB9} + \\
& SRM\,(RB1\emptyset + SB1\emptyset) + \\
& SLM\,(RB8 + SB8) + \\
& RL4\,(RB5 + SB5) \\
TB1\emptyset = {} & ADF\,[(RB1\emptyset \cdot SB1\emptyset \cdot C1\emptyset) + (RB1\emptyset \cdot \overline{SB1\emptyset} \cdot \overline{C1\emptyset}) + \\
& \quad (\overline{RB1\emptyset} \cdot SB1\emptyset \cdot \overline{C1\emptyset})] + \\
& EOF\,[(RB1\emptyset \cdot \overline{SB1\emptyset}) + (\overline{RB1\emptyset} \cdot SB1\emptyset)] + \\
& IOF\,(RB1\emptyset + SB1\emptyset) + \\
& ANF\,(RB1\emptyset \cdot SB1\emptyset) + \\
& CMF \cdot \overline{RB1\emptyset} + \\
& SRM\,(RB11 + SB11) + \\
& SLM\,(RB9 + SB9) + \\
& RL4\,(RB6 + SB6)
\end{aligned}
$$

$$
\begin{aligned}
TB11 = {} & ADF\,[(RB11 \cdot SB11 \cdot C11) + (RB11 \cdot \overline{SB11} \cdot \overline{C11}) + \\
& \quad (\overline{RB11} \cdot SB11 \cdot \overline{C11})] + \\
& EOF\,[(RB11 \cdot \overline{SB11}) + (\overline{RB11} \cdot SB11)] + \\
& IOF\,(RB11 + SB11) + \\
& ANF\,(RB11 \cdot SB11) + \\
& CMF \cdot \overline{RB11} + \\
& SLM\,(RB1\emptyset + SB1\emptyset) + \\
& SRM\,(RB12 + SB12) + \\
& RL4\,(RB7 + SB7)
\end{aligned}
$$

$$
\begin{aligned}
TB12 = {} & ADF\,[(RB12 \cdot SB12 \cdot C12) + (RB12 \cdot \overline{SB12} \cdot \overline{C12}) + \\
& \quad (\overline{RB12} \cdot SB12 \cdot \overline{C12})] + \\
& EOF\,[(RB12 \cdot \overline{SB12}) + (\overline{RB12} \cdot SB12)] + \\
& IOF\,(RB12 + SB12) + \\
& ANF\,(RB12 \cdot SB12) + \\
& CMF \cdot \overline{RB12} + \\
& SRM\,(RB13 + SB13) + \\
& SLM\,(RB11 + SB11) + \\
& RL4\,(RB8 + SB8)
\end{aligned}
$$

$$
\begin{aligned}
TB13 = {} & ADF\,[(RB13 \cdot SB13 \cdot C13) + (RB13 \cdot \overline{SB13} \cdot \overline{C13}) + \\
& \quad (\overline{RB13} \cdot SB13 \cdot \overline{C13})] + \\
& EOF\,[(RB13 \cdot \overline{SB13}) + (\overline{RB13} \cdot SB13)] + \\
& IOF\,(RB13 + SB13) + \\
& ANF\,(RB13 \cdot SB13) + \\
& CMF \cdot \overline{RB13} + \\
& SRM\,(RB14 + SB14) + \\
& SLM\,(RB12 + SB12) + \\
& RL4\,(RB9 + SB9)
\end{aligned}
$$

$$
\begin{aligned}
TB14 = {} & ADF\,[(RB14 \cdot SB14 \cdot C14) + (RB14 \cdot \overline{SB14} \cdot \overline{C14}) + \\
& \quad (\overline{RB14} \cdot SB14 \cdot \overline{C14})] + \\
& EOF\,[(RB14 \cdot \overline{SB14}) + (\overline{RB14} \cdot SB14)] + \\
& IOF\,(RB14 + SB14) + \\
& ANF\,(RB14 \cdot SB14) + \\
& CMF \cdot \overline{RB14} + \\
& SRM\,(RB15 + SB15) + \\
& SLM\,(RB13 + SB13) + \\
& RL4\,(RB1\emptyset + SB1\emptyset)
\end{aligned}
$$

$$
\begin{aligned}
TB15 = {} & ADF\,[(RB15 \cdot SB15 \cdot C15) + (RB15 \cdot \overline{SB15} \cdot \overline{C15}) + \\
& \quad (\overline{RB15} \cdot SB15 \cdot \overline{C15})] + \\
& EOF\,[(RB15 \cdot \overline{SB15}) + (\overline{RB15} \cdot SB15)] + \\
& IOF\,(RB15 + SB15) + \\
& ANF\,(RB15 \cdot SB15) + \\
& CMF \cdot \overline{RB15} + \\
& SL14\,(RB14 + SB14) + \\
& RRS\,(RB\emptyset + SB\emptyset) + \\
& RL4\,(RB11 + SB11) + \\
& EFF \cdot SRG\,[(T3 \cdot TR6 \cdot \overline{TR7} \cdot TR8) + \\
& \quad (T5 \cdot TR\emptyset \cdot \overline{TR1} \cdot TR2)] + \\
& RB15 \cdot SRG\,[(\overline{TR7} \cdot \overline{TR8} \cdot T3) + (\overline{TR1} \cdot \overline{TR2} \cdot T5)]
\end{aligned}
$$

$$TS = \overline{CF1D} \cdot \overline{CF1}$$

$$TSA = \overline{CF1D} \cdot \overline{CF1}$$

$$X\emptyset = (\overline{TTK} \cdot \overline{M12} \cdot M13 \cdot M14) + (\overline{M12} \cdot \overline{M13} \cdot \overline{M14})$$

$$X1 = (\overline{TTK} \cdot M12 \cdot M13 \cdot M14) + (M12 \cdot \overline{M13} \cdot \overline{M14})$$

$$X2 = \overline{M12} \cdot M13 \cdot \overline{M14}$$

$$X3 = M12 \cdot M13 \cdot \overline{M14}$$

$$XOR = EIR \cdot \overline{IR14} \cdot IR13 \cdot \overline{IR12}$$

$$Y\emptyset/1 = (\overline{TTK} \cdot M13 \cdot M14) + (\overline{M14} \cdot \overline{M13})$$

$$Y2/3 = M13 \cdot \overline{M14}$$

HP 2116B BOARD LOCATION

(FRONT VIEW)

201	I/O CONTROL	02116-6041	101	FRONT PANEL COUPLER	02116-6184	1	PWR FAIL 02116-6175 PWR FAIL** (RESTART) 12588-6001
202	I/O ADDRESS ENCODE	02116-6194	102	ARITHMETIC LOGIC 12-15	02116-6026	2	MMD 02116-6274
203	†(I/O 10/11)		103	ARITHMETIC LOGIC 8-11	02116-6026	3	PE** 12591-6001
204	†(I/O 11/12)		104	ARITHMETIC LOGIC 4-7	02116-6026	4	ID3* 02116-6265
205	†(I/O 12/13)		105	ARITHMETIC LOGIC 0-3	02116-6026	5	SPARE
206	†(I/O 13/14)		106	TIMING GENERATOR	02116-6281	6	ID2* 02116-6265
207	†(I/O 14/15)		107	INSTRUCTION DECODER	02116-6027	7	SPARE
208	†(I/O 15/16)		108	SHIFT LOGIC	02116-6029	8	DSY 2/3* 02116-6266
209	†(I/O 16/17)		109	EAU*	02116-6196	9	DSX 2/3* 02116-6266
210	†(I/O 17/20)		110	EAU*	02116-6202	10	SA3* 02115-6001
211	†(I/O 20/21)		111	SPARE		11	SA 2* 02115-6001
212	†(I/O 21/22)		112	SPARE		12	SA 1 02115-6001
213	†(I/O 22/23)		113	SPARE		13	SAØ 02115-6001
214	†(I/O 23/24)		114	SPARE		14	DSY Ø/1 02116-6266
215	†(I/O 24/25)		115	SPARE		15	DSX Ø/1 02116-6266
216	†(I/O 25/26)		116	DMA* 02116-6206 DMI* 02115-6221		16	ID1 02116-6265
217	†(I/O 26/27)		117	DMA*	02116-6206	17	SPARE
218	†(I/O 27/30)		118	DMA*	02116-6205	18	IDØ 02116-6265
219	**I/O EXTENDER	02116-6182	119	DMA*	02116-6204	19	SPARE
220	**I/O EXTENDER	02116-6183	120	DMA*	02116-6203	20	DML 02115-6044
221	**MEMORY EXTENDER	02116-6181		POWER SUPPLY TEST POINTS		21	MEMORY PROTECT** 12581-6001
222	**MEMORY EXTENDER	02116-6181				22	SPARE

* *OPTIONAL BOARDS MAY BE ADDED AT ANY TIME.*

** *OPTIONAL BOARDS MAY BE ADDED AFTER ADDITIONAL BACK PLANE WIRING*

† *I/O PLUG-IN OPTIONS MAY BE ADDED AT ANY TIME PROVIDING THE CURRENT REQUIREMENTS DO NOT EXCEED THE POWER SUPPLY RATINGS.*

HP 2116B BOARD LOCATION

(FRONT VIEW)

201	I/O CONTROL	02116-6041
202	I/O ADDRESS ENCODE	02116-6194
203	⸗(I/O 10/11)	
204	⸗(I/O 11/12)	
205	⸗(I/O 12/13)	
206	⸗(I/O 13/14)	
207	⸗(I/O 14/15)	
208	⸗(I/O 15/16)	
209	⸗(I/O 16/17)	
210	⸗(I/O 17/20)	
211	⸗(I/O 20/21)	
212	⸗(I/O 21/22)	
213	⸗(I/O 22/23)	
214	⸗(I/O 23/24)	
215	⸗(I/O 24/25)	
216	⸗(I/O 25/26)	
217	⸗(I/O 26/27)	
218	⸗(I/O 27/30)	
219	⁂I/O EXTENDER	02116-6182
220	⁂I/O EXTENDER	02116-6183
221	⁂MEMORY EXTENDER	02116-6181
222	⁂MEMORY EXTENDER	02116-6181

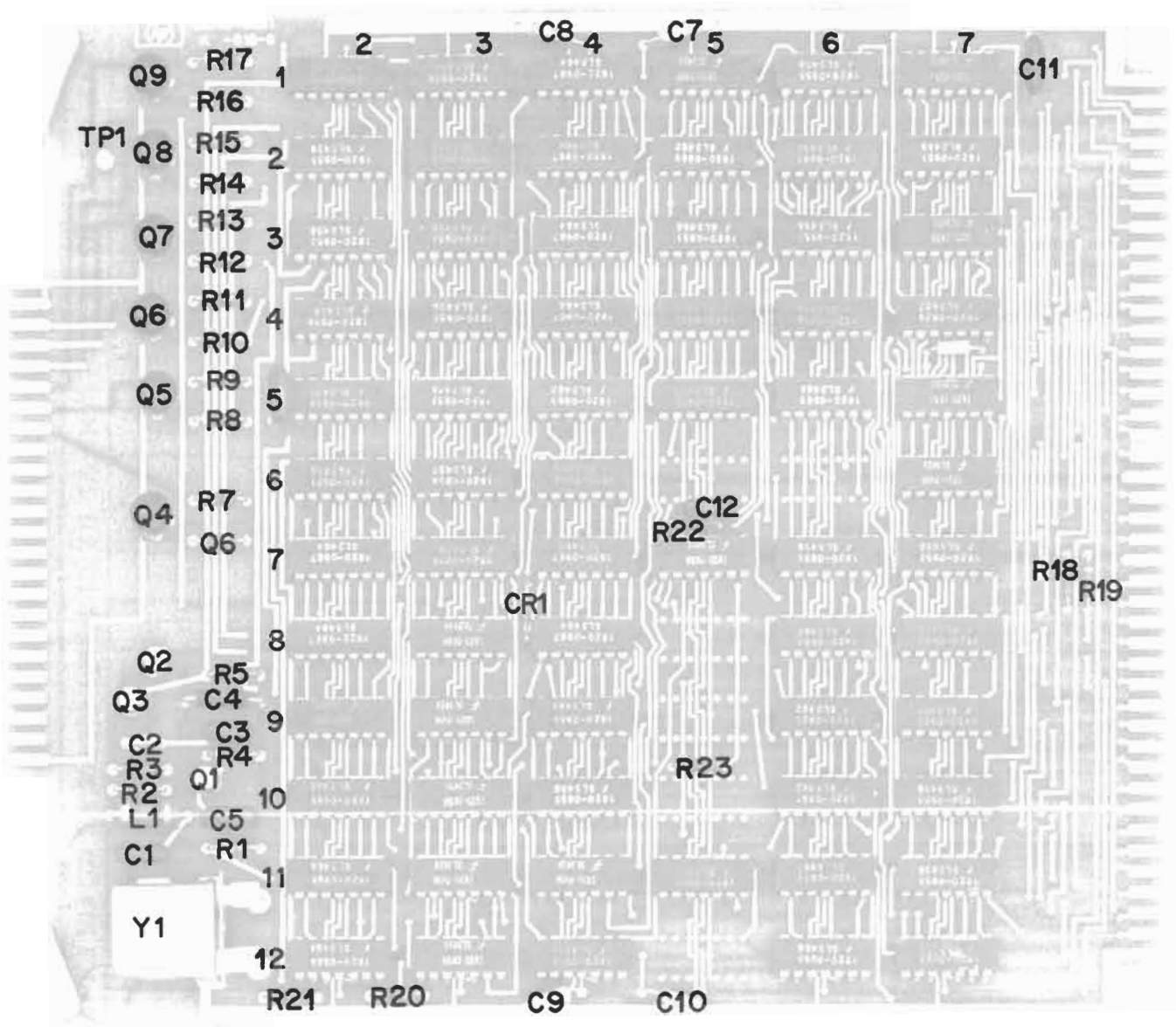
101	FRONT PANEL COUPLER	02116-6184
102	ARITHMETIC LOGIC 12-15	02116-6026
103	ARITHMETIC LOGIC 8-11	02116-6026
104	ARITHMETIC LOGIC 4-7	02116-6026
105	ARITHMETIC LOGIC 0-3	02116-6026
106	TIMING GENERATOR	02116-6281
107	INSTRUCTION DECODER	02116-6027
108	SHIFT LOGIC	02116-6029
109	EAU*	02116-6196
110	EAU*	02116-6202
111	SPARE	
112	SPARE	
113	SPARE	
114	SPARE	
115	SPARE	
116	DMA* DMI*	02116-6206 02116-6221
117	DMA*	02116-6206
118	DMA*	02116-6205
119	DMA*	02116-6204
120	DMA*	02116-6203
	POWER SUPPLY TEST POINTS	

1	PWR FAIL PWR FAIL**(RESTART)	02116-6175 12588-6001
2	MMD	02116-6274
3	PE**	12591-6001
4	ID3*	02116-6265
5	SPARE	
6	ID2*	02116-6265
7	SPARE	
8	DSY 2/3*	02116-6266
9	DSX 2/3*	02116-6266
10	SA3*	02115-6001
11	SA2*	02115-6001
12	SA 1	02115-6001
13	SAØ	02115-6001
14	DSY Ø/1	02116-6266
15	DSX Ø/1	02116-6266
16	ID1	02116-6265
17	SPARE	
18	IDØ	02116-6265
19	SPARE	
20	DML	02115-6044
21	MEMORY PROTECT**	12581-6001
22	SPARE	

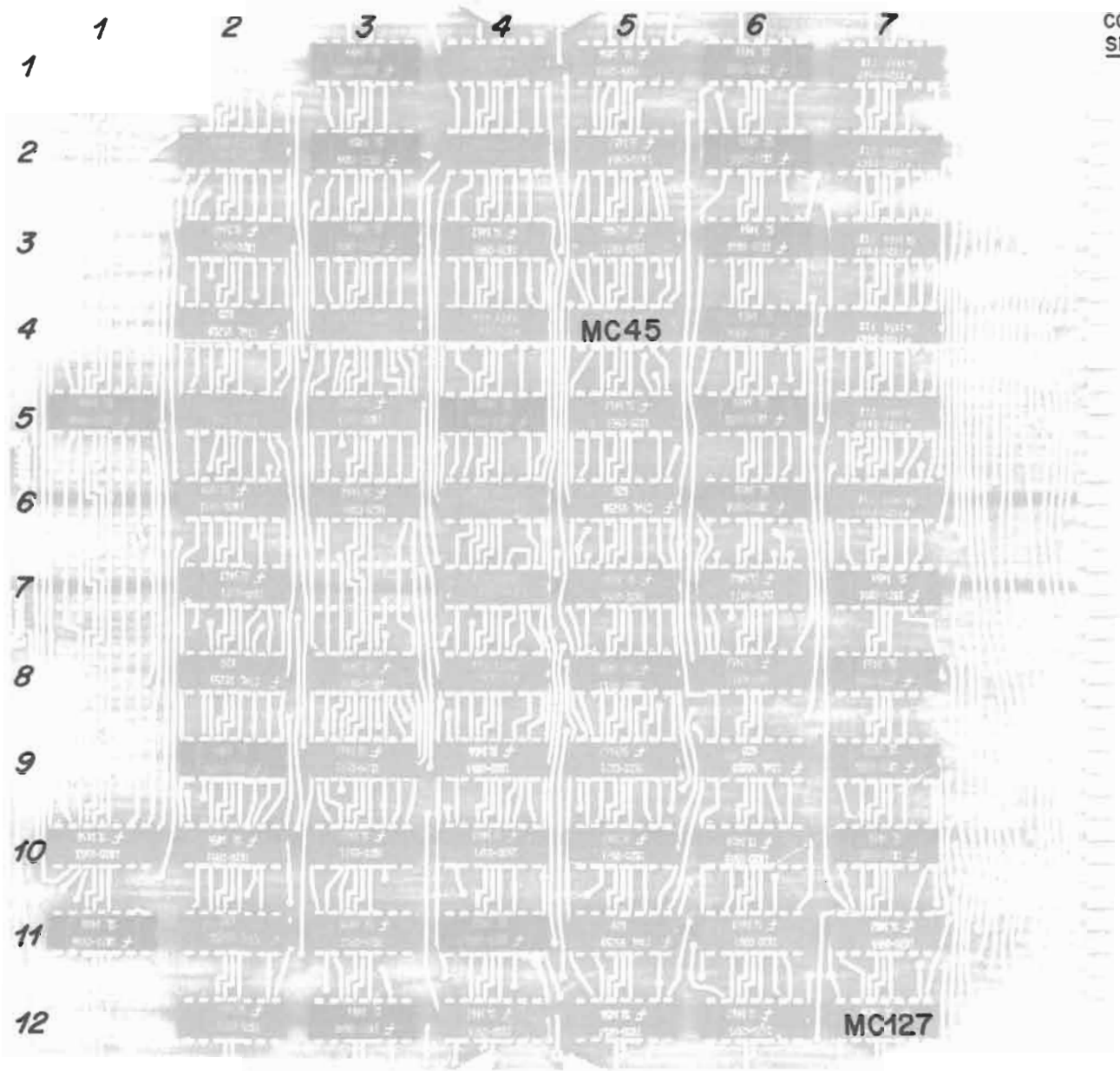
* *OPTIONAL BOARDS MAY BE ADDED AT ANY TIME.*

⁂ *OPTIONAL BOARDS MAY BE ADDED AFTER ADDITIONAL BACK PLANE WIRING*

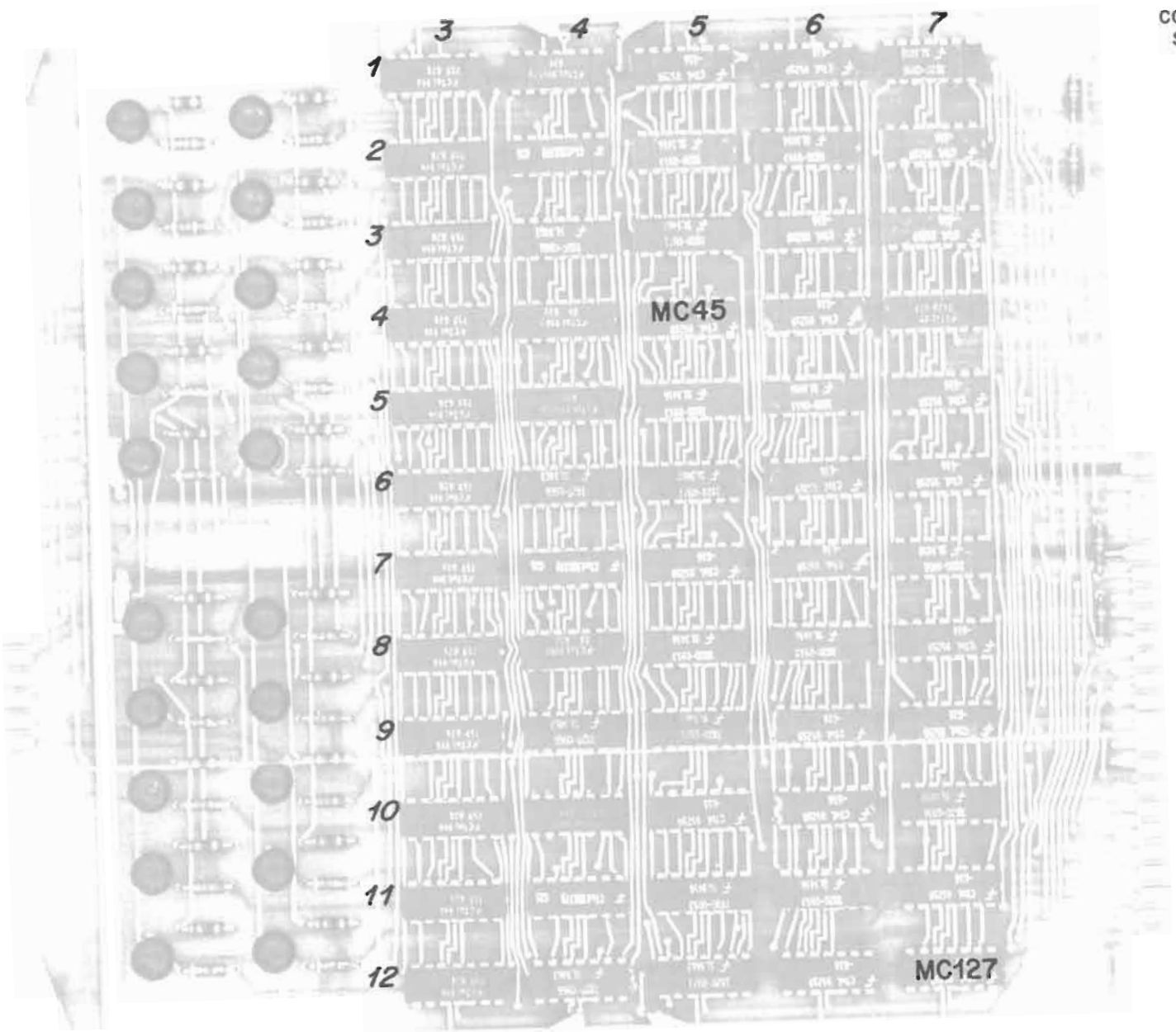
⸗ *I/O PLUG-IN OPTIONS MAY BE ADDED AT ANY TIME PROVIDING THE CURRENT REQUIREMENTS DO NOT EXCEED THE POWER SUPPLY RATINGS.*



2116B SYSTEM TIMING GENERATOR



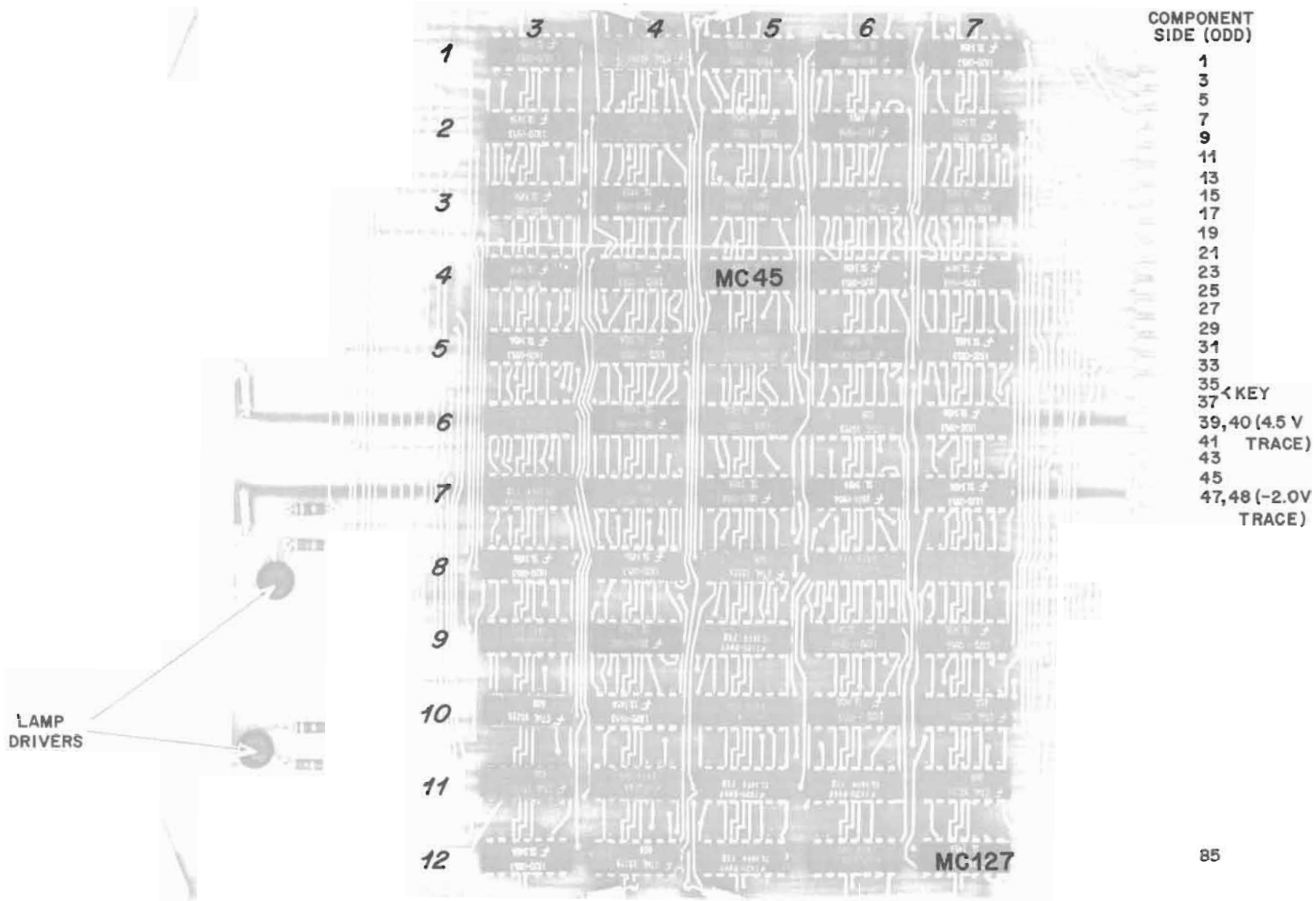
INSTRUCTION DECODER



COMPONENT SIDE (ODD)	
1	
3	
5	
7	
9	
11	
13	
15	
17	
19	
21	
23	
25	
27	
29	
31	
33	
35	< KEY
37	
39, 40	(4.5 Volt TRACE)
41	
43	
45	
47, 48	(-2.0 Volt TRACE)

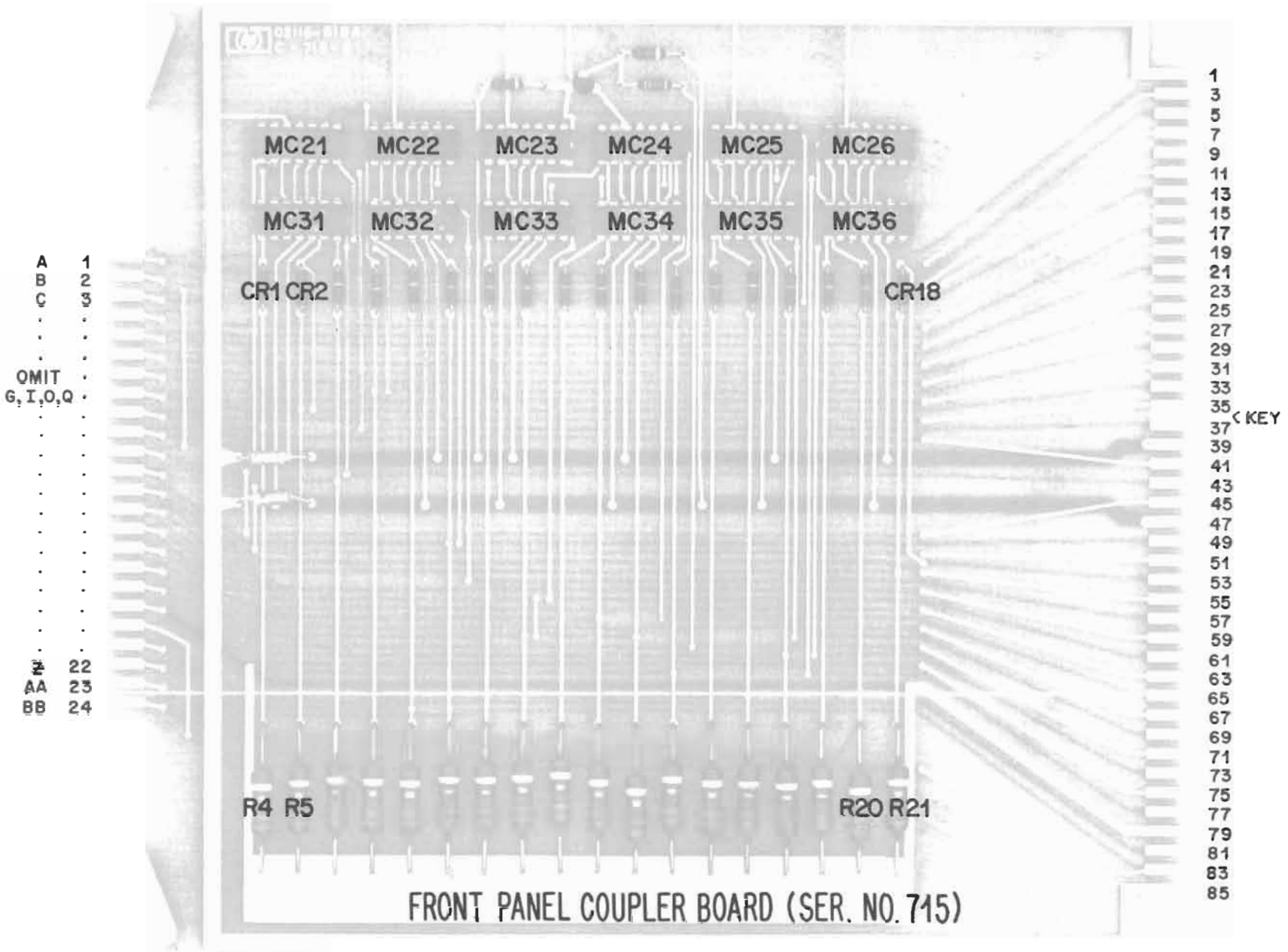
85

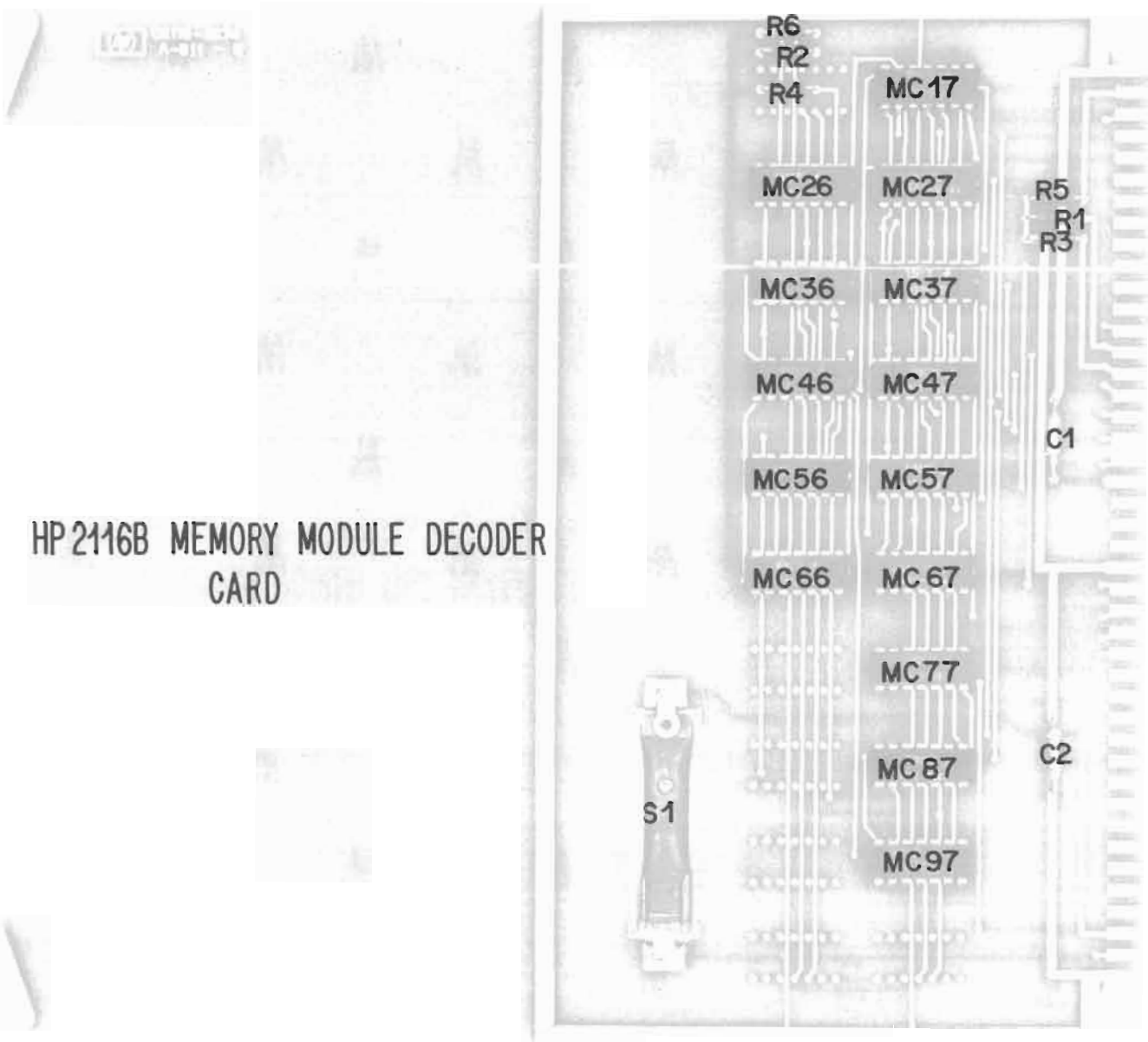
ARITHMETIC LOGIC BOARD



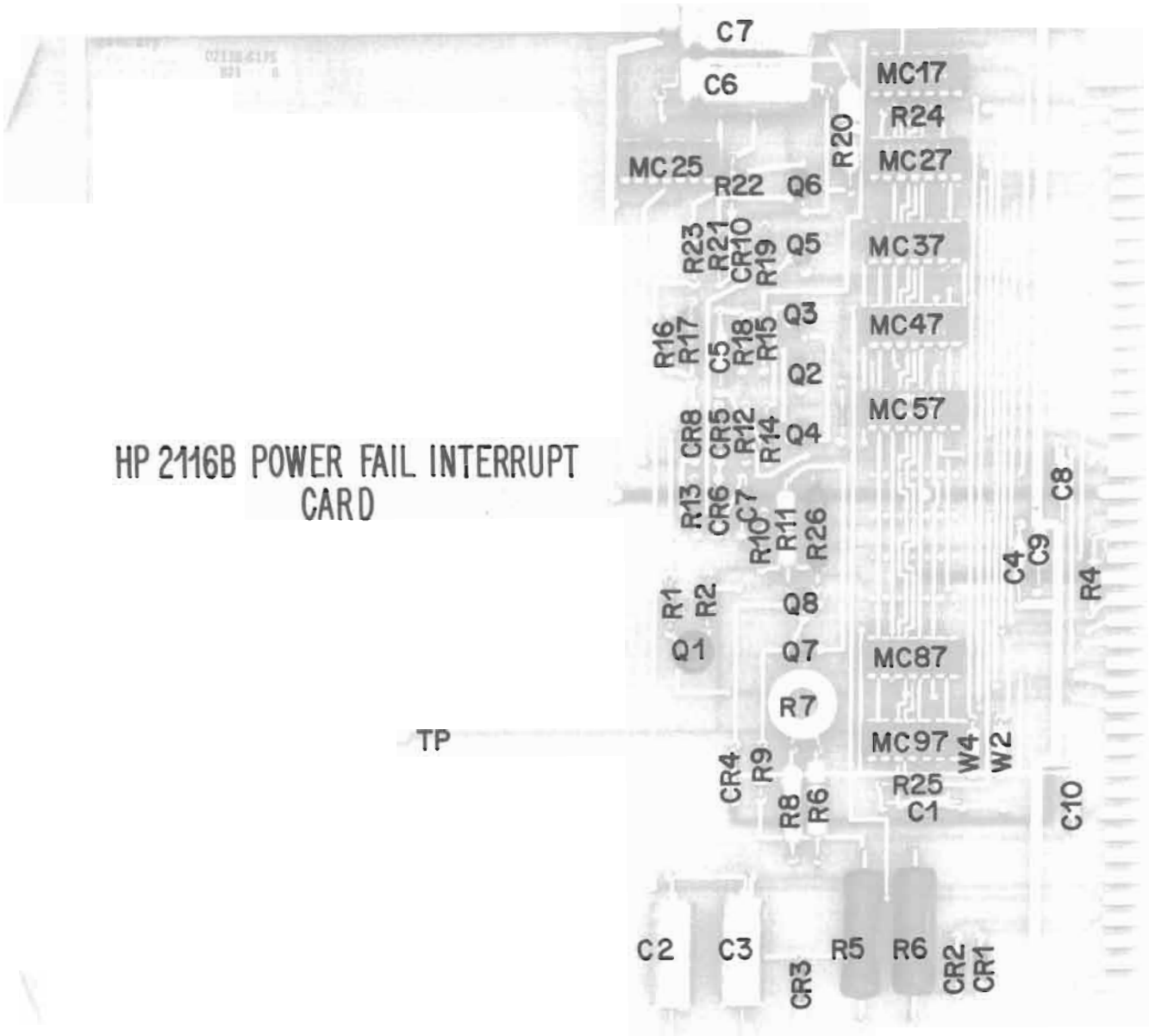
85

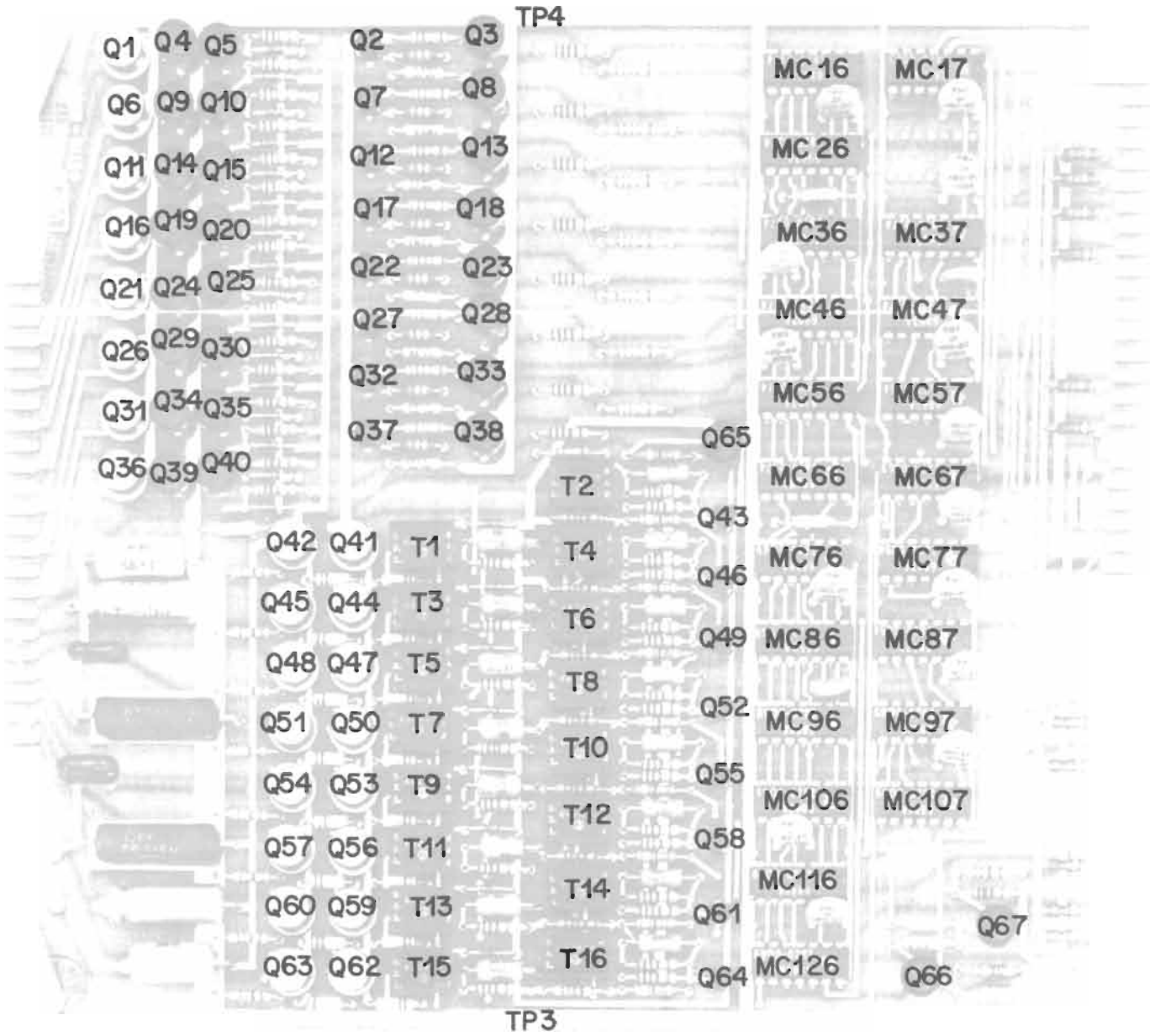
SHIFT LOGIC


MC21
MC22
MC23
MC24
MC25
MC26
MC31
MC32
MC33
MC34
MC35
MC36
CR1 CR2
CR18
R4 R5
R20 R21
A 1
B 2
C 3
OMIT
G, I, O, Q
AA 23
BB 24
1
3
5
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35
37
39
41
43
45
47
49
51
53
55
57
59
61
63
65
67
69
71
73
75
77
79
81
83
85
KEY
FRONT PANEL COUPLER BOARD (SER. NO. 715)

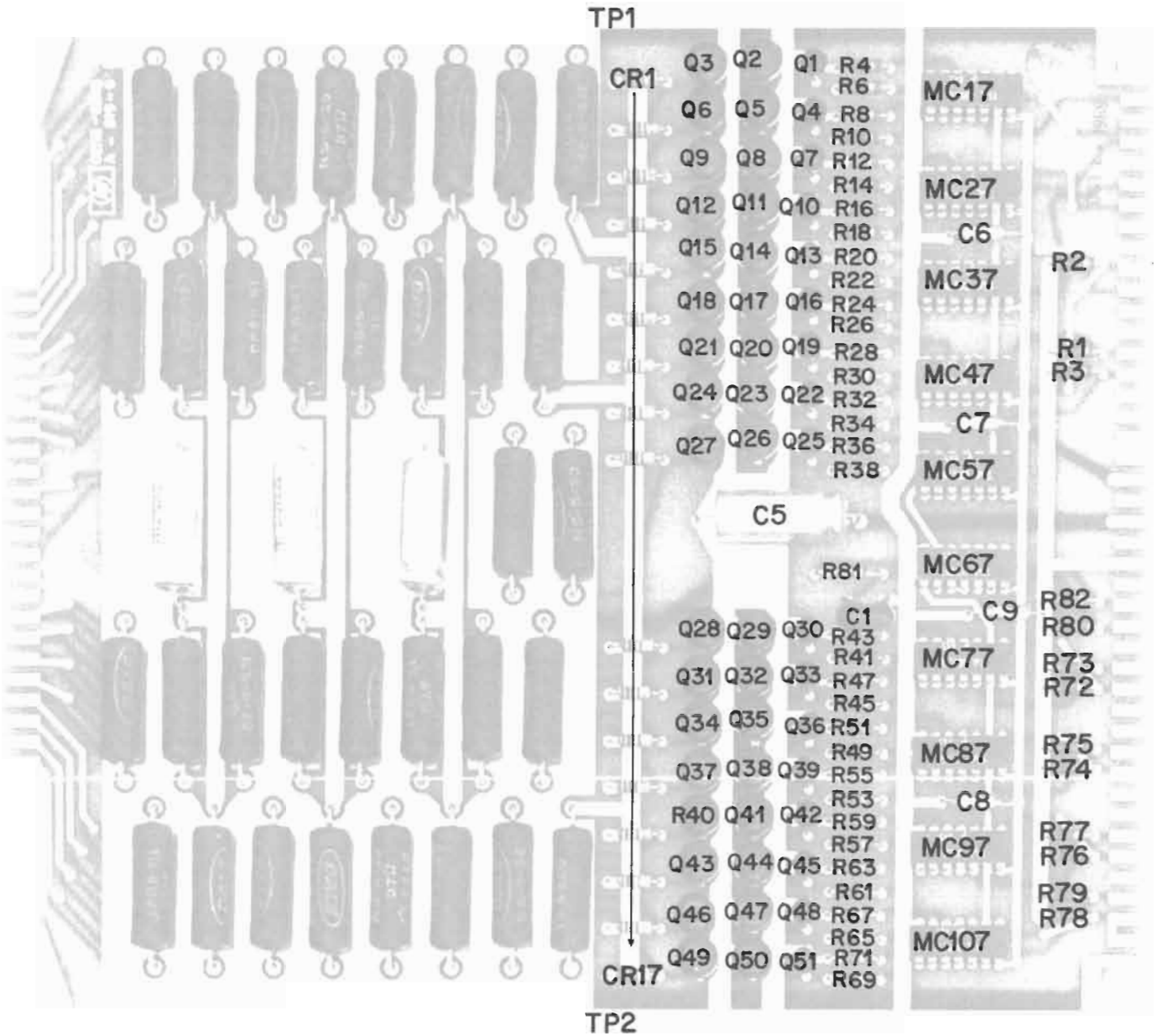


HP 2116B MEMORY MODULE DECODER CARD

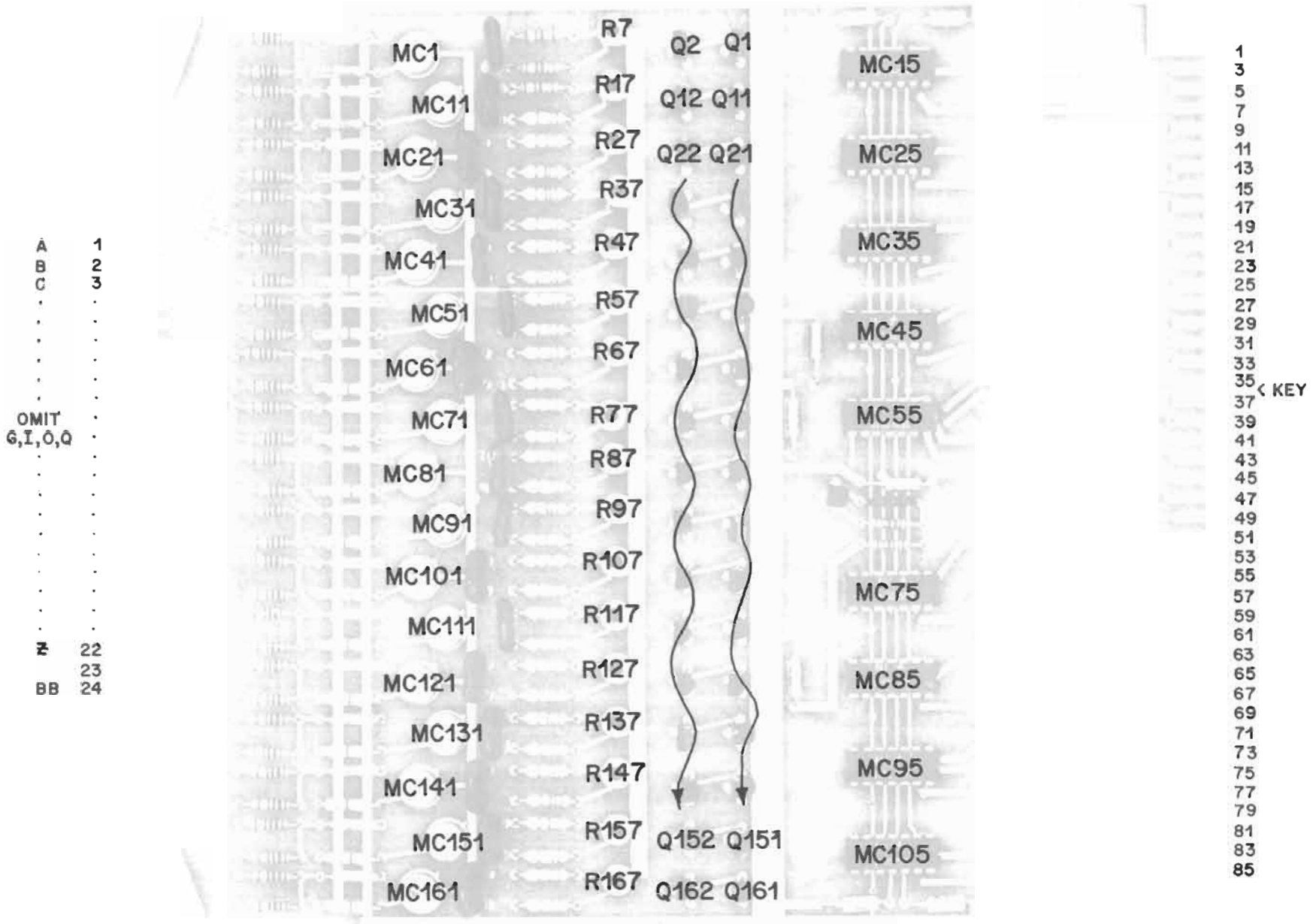

HP 2116B POWER FAIL INTERRUPT
CARD
C7
C6
MC17
R24
R20
MC25
R22
Q6
MC27
R23
R21
CR10
R19
Q5
MC37
R16
R17
C5
R18
R15
Q3
MC47
Q2
CR8
CR5
R12
R14
Q4
MC57
R13
CR6
C7
R10
R11
R26
C8
C4
C9
R4
R1
R2
Q8
Q1
Q7
MC87
R7
TP
MC97
W4
W2
CR4
R9
R25
R8
R6
C1
C10
C2
C3
R5
R6
CR2
CR1
CR3



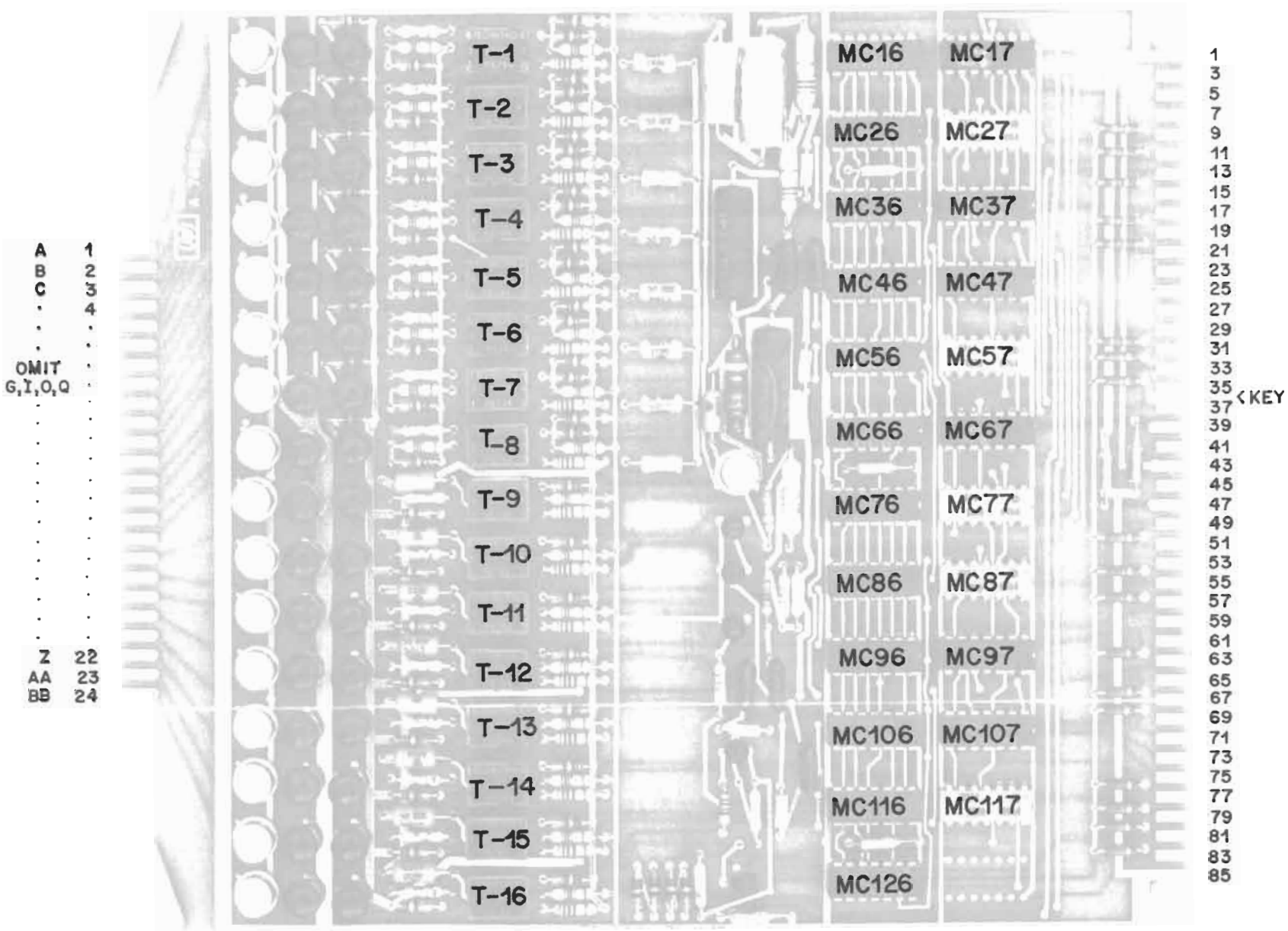
HP 2116B DRIVER/SWITCH CARD



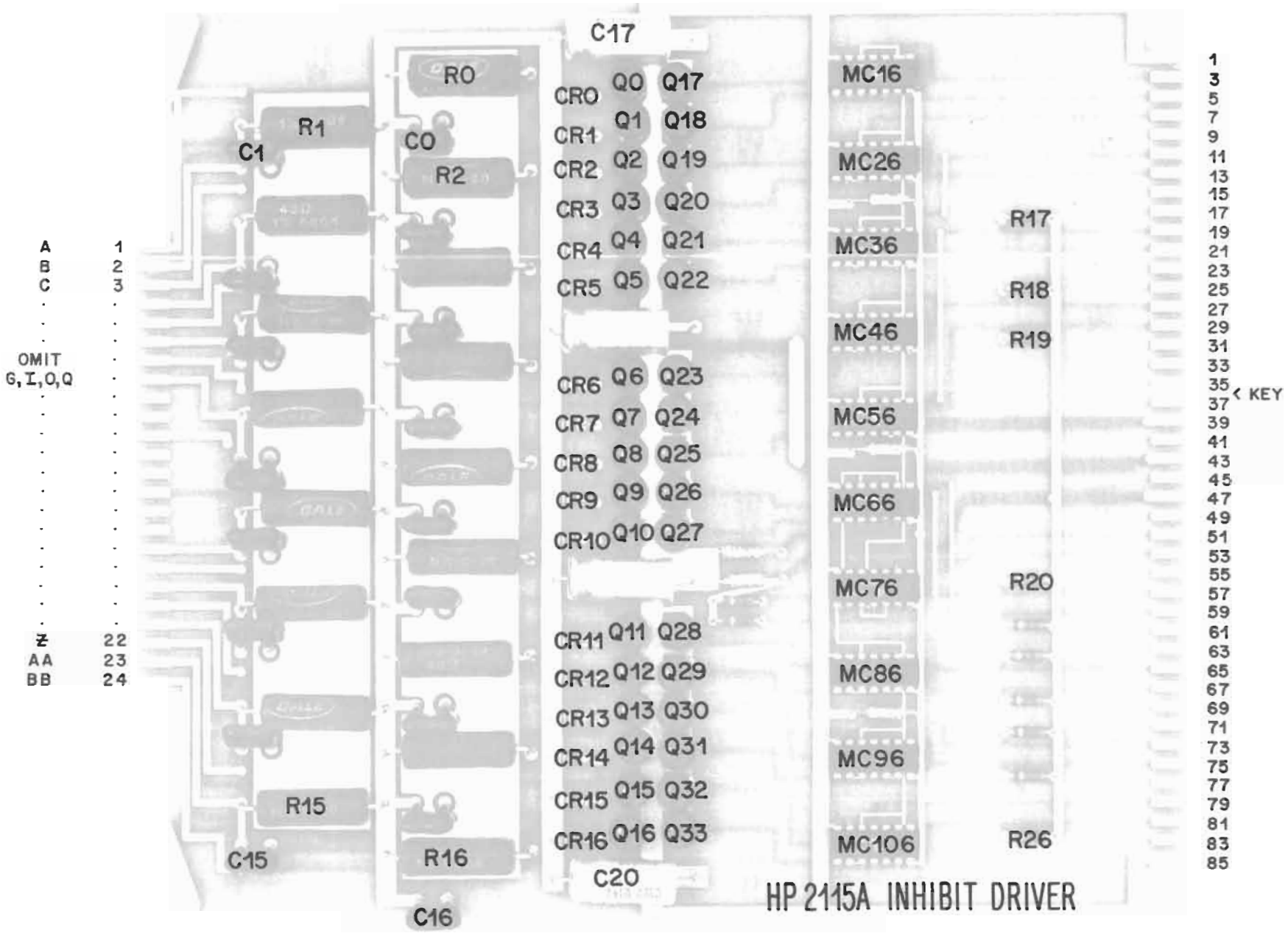
HP 2116B INHIBIT DRIVER

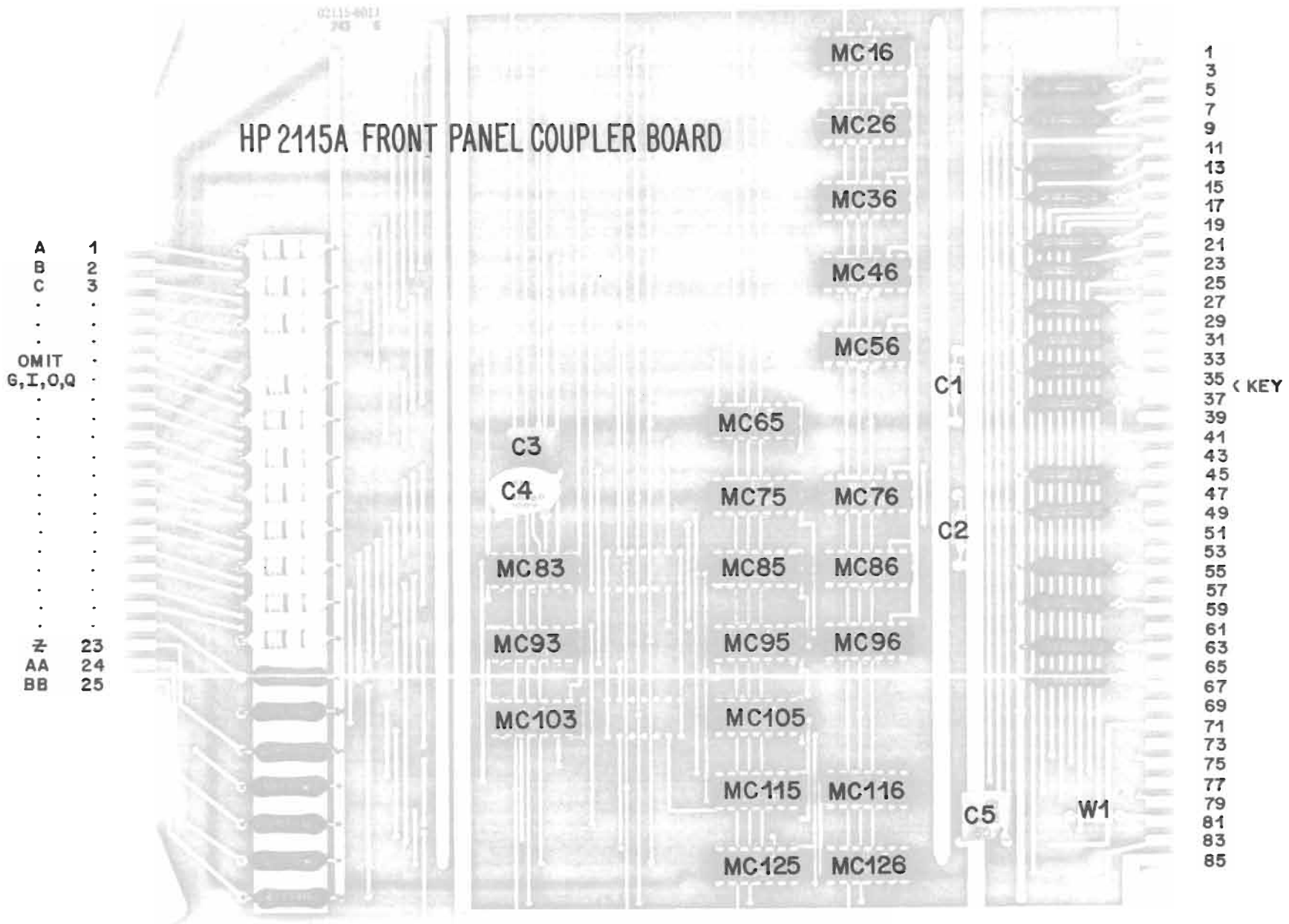


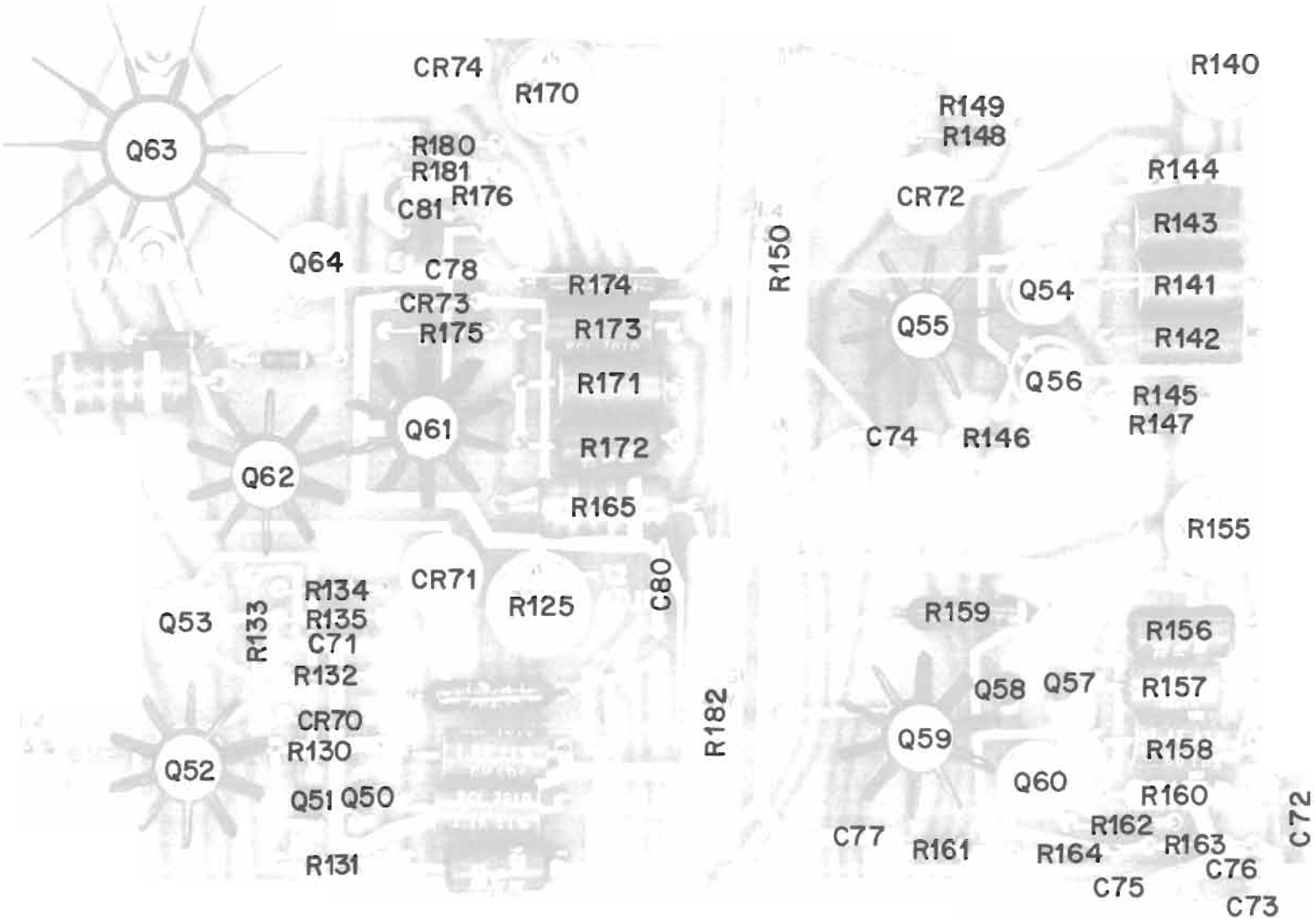
HP2116B / HP2115A SENSE AMPLIFIER



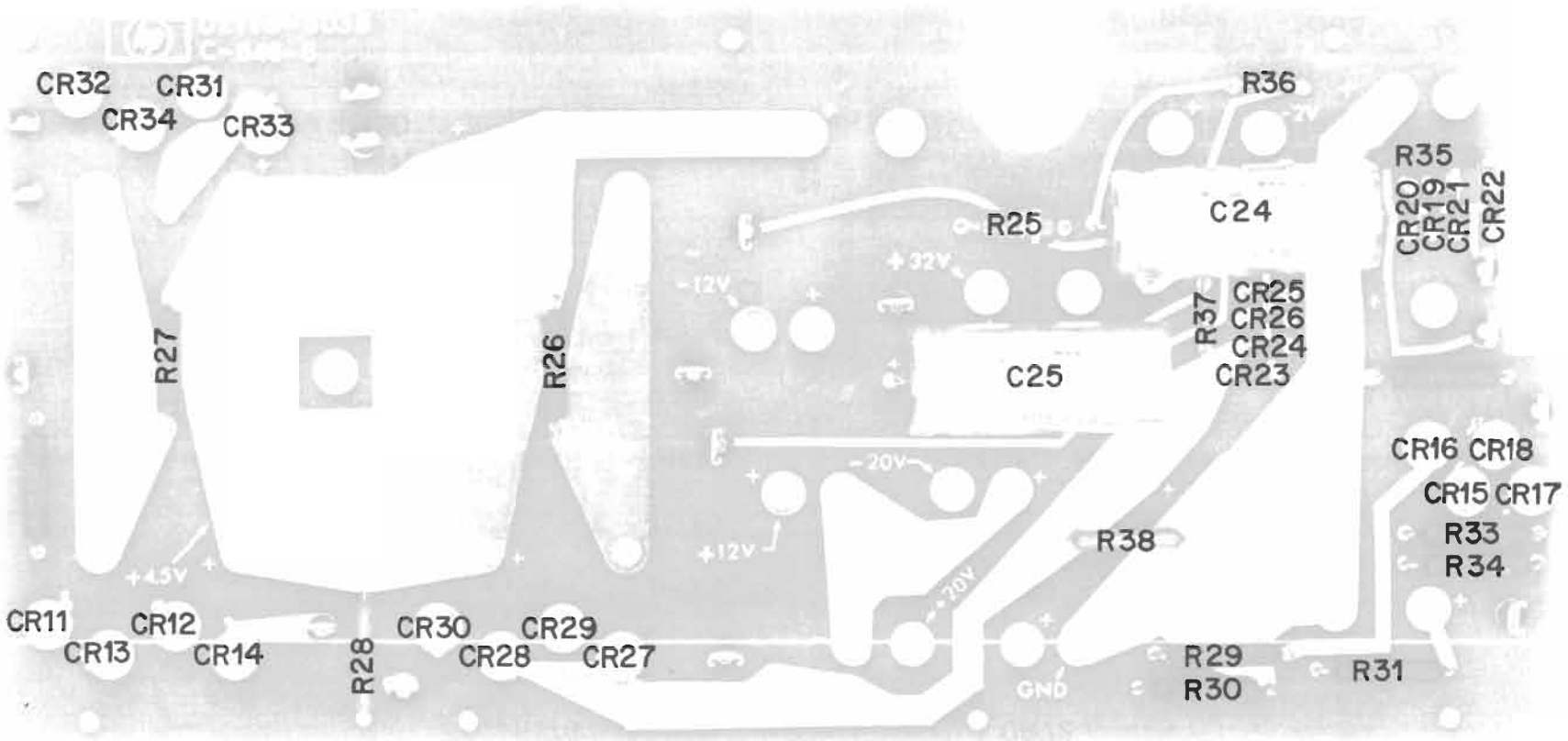
HP 2115A DRIVER/SWITCH


A 1
B 2
C 3
OMIT G, I, O, Q
Z 22
AA 23
BB 24
C17
R0
R1
C1
C0
R2
CR0 Q0 Q17
CR1 Q1 Q18
CR2 Q2 Q19
CR3 Q3 Q20
CR4 Q4 Q21
CR5 Q5 Q22
CR6 Q6 Q23
CR7 Q7 Q24
CR8 Q8 Q25
CR9 Q9 Q26
CR10 Q10 Q27
CR11 Q11 Q28
CR12 Q12 Q29
CR13 Q13 Q30
CR14 Q14 Q31
CR15 Q15 Q32
CR16 Q16 Q33
R15
C15
R16
C16
C20
MC16
MC26
MC36
MC46
MC56
MC66
MC76
MC86
MC96
MC106
R17
R18
R19
R20
R26
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49 51 53 55 57 59 61 63 65 67 69 71 73 75 77 79 81 83 85
KEY
HP 2115A INHIBIT DRIVER


HP 2115A FRONT PANEL COUPLER BOARD
A 1
B 2
C 3
OMIT
G,I,O,Q
Z 23
AA 24
BB 25
MC16
MC26
MC36
MC46
MC56
C1
MC65
C3
C4
MC75
MC76
C2
MC83
MC85
MC86
MC93
MC95
MC96
MC103
MC105
MC115
MC116
C5
W1
MC125
MC126
1
3
5
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35
37
39
41
43
45
47
49
51
53
55
57
59
61
63
65
67
69
71
73
75
77
79
81
83
85
KEY

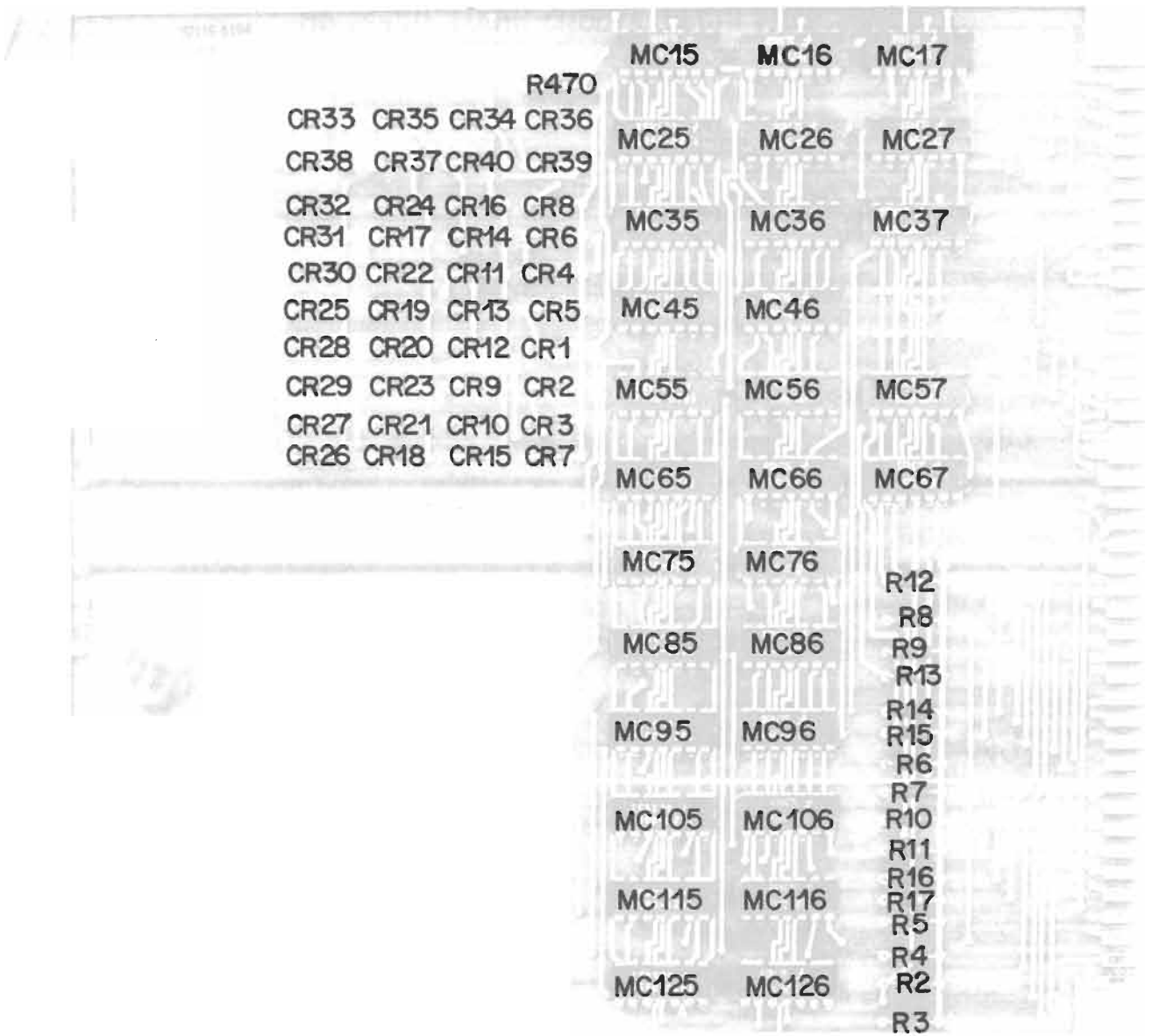


HP 2116B MEMORY SUPPLY REGULATOR

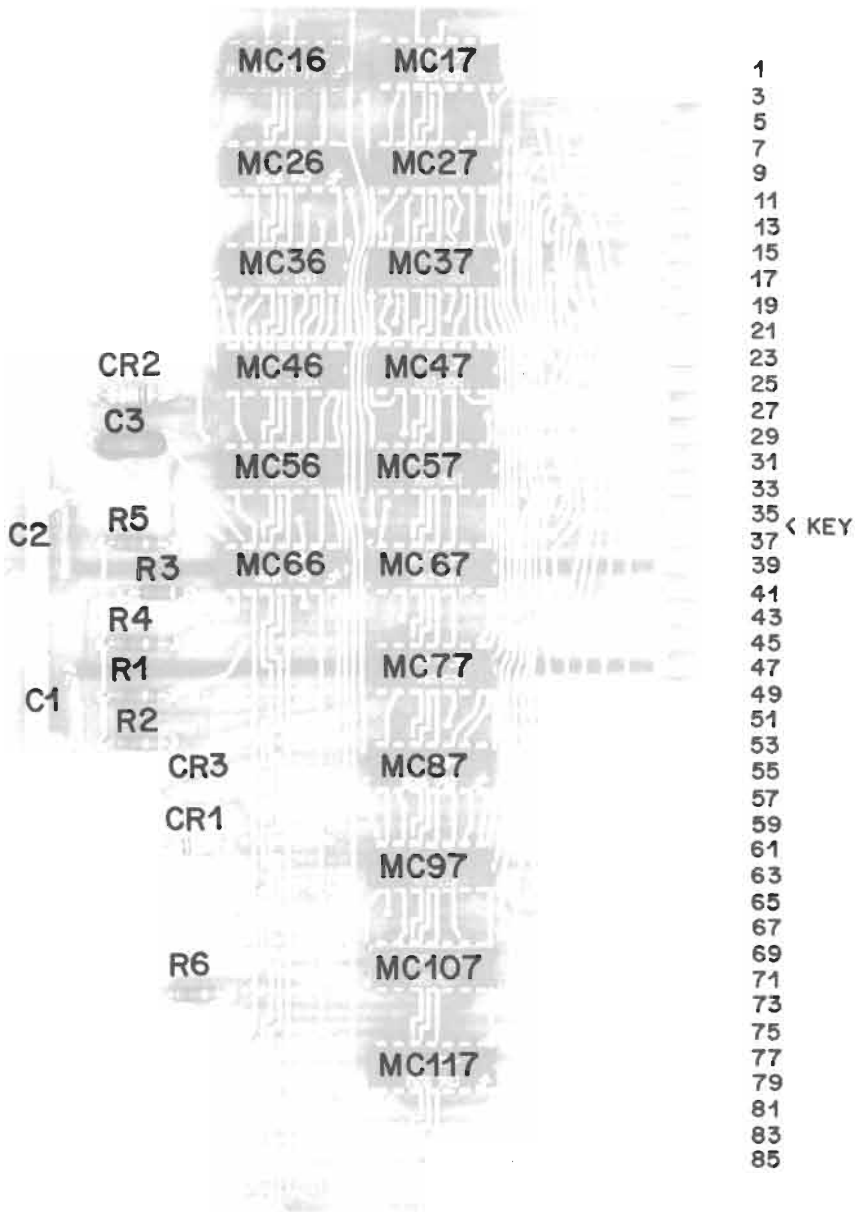


HP 2116B CAPACITOR BOARD (A303)

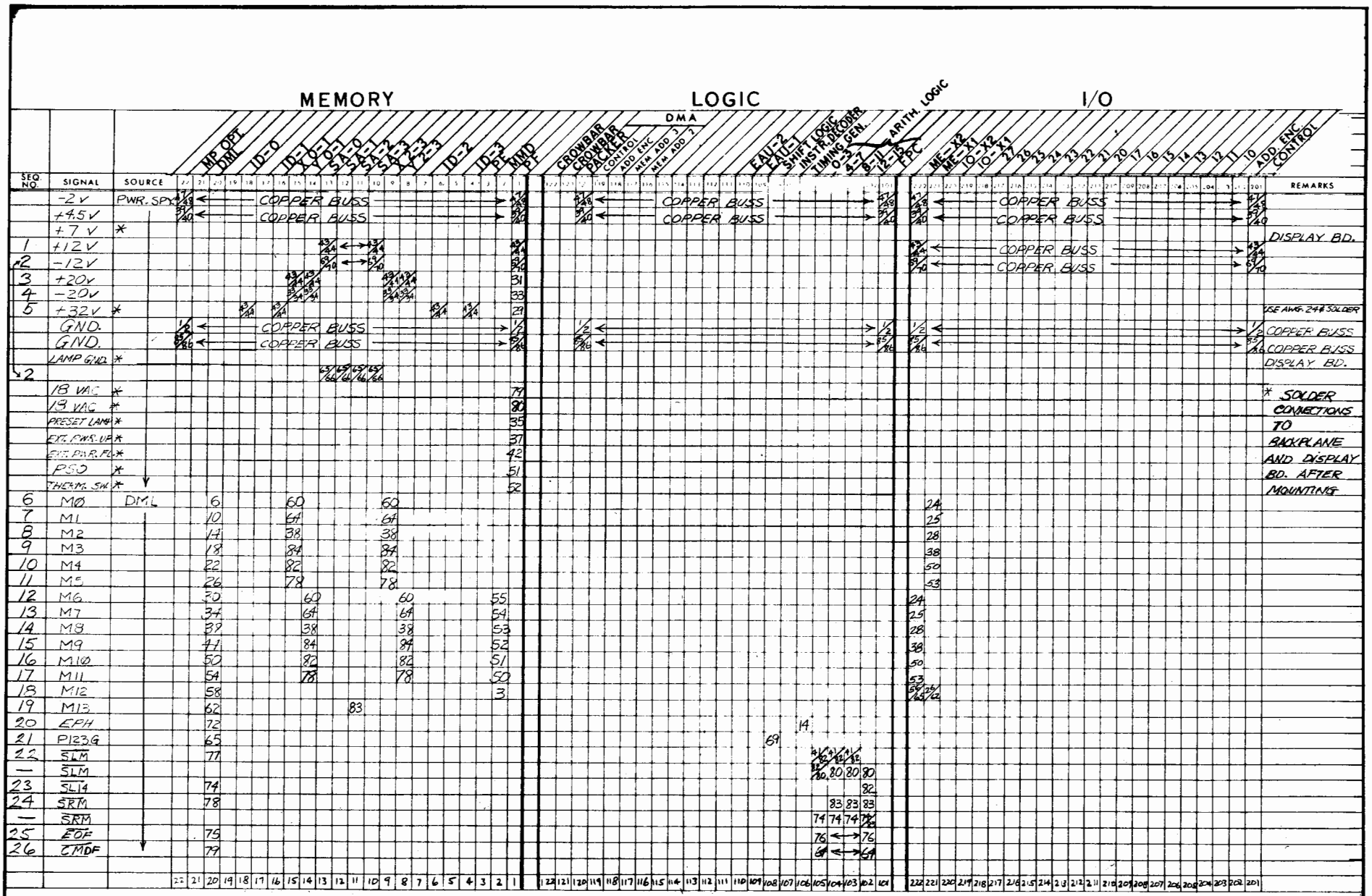
HP 2116B LOGIC SUPPLY REGULATOR
(A301)



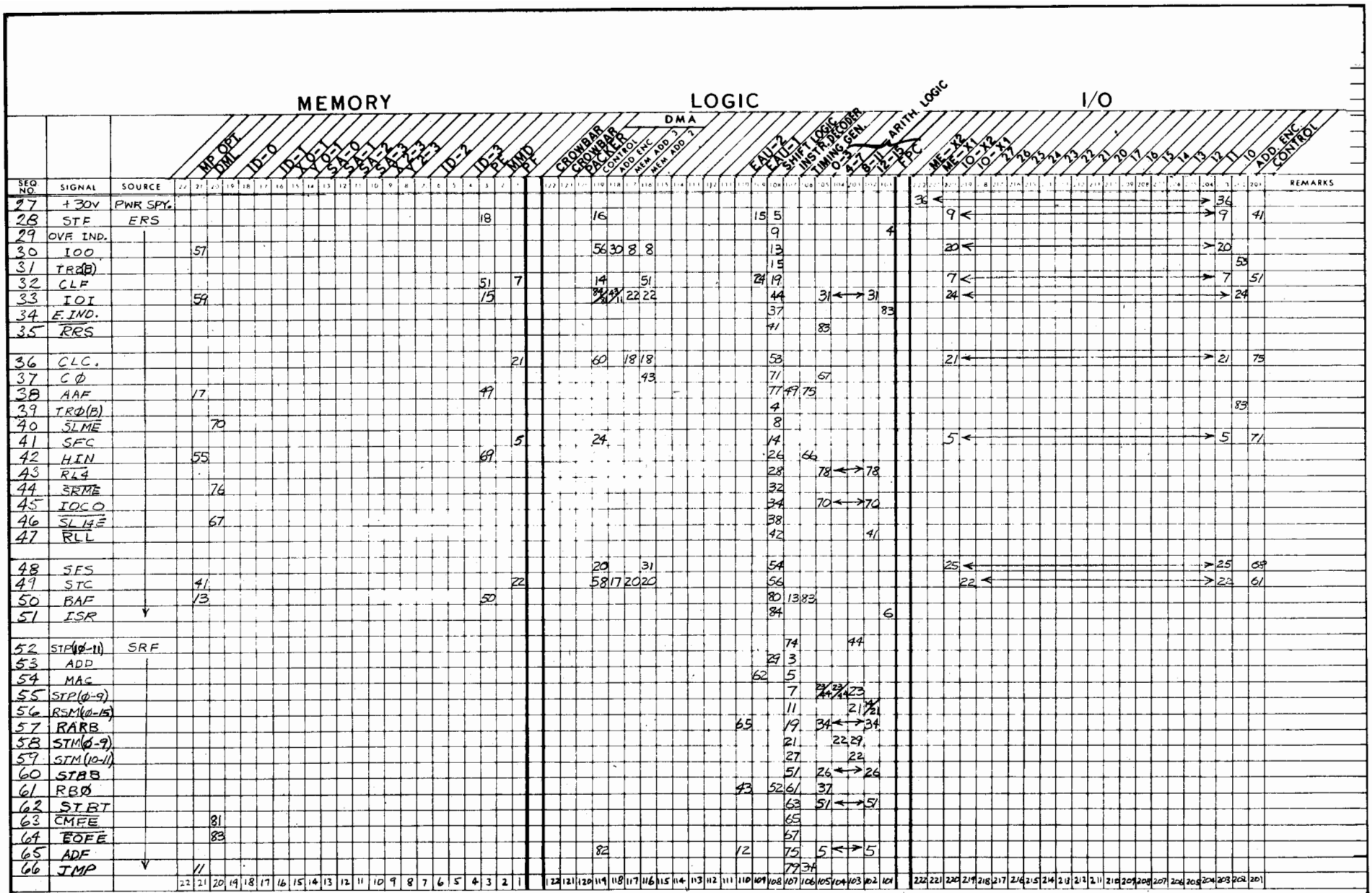
HP 2116B/2115A I/O ADDRESS CARD



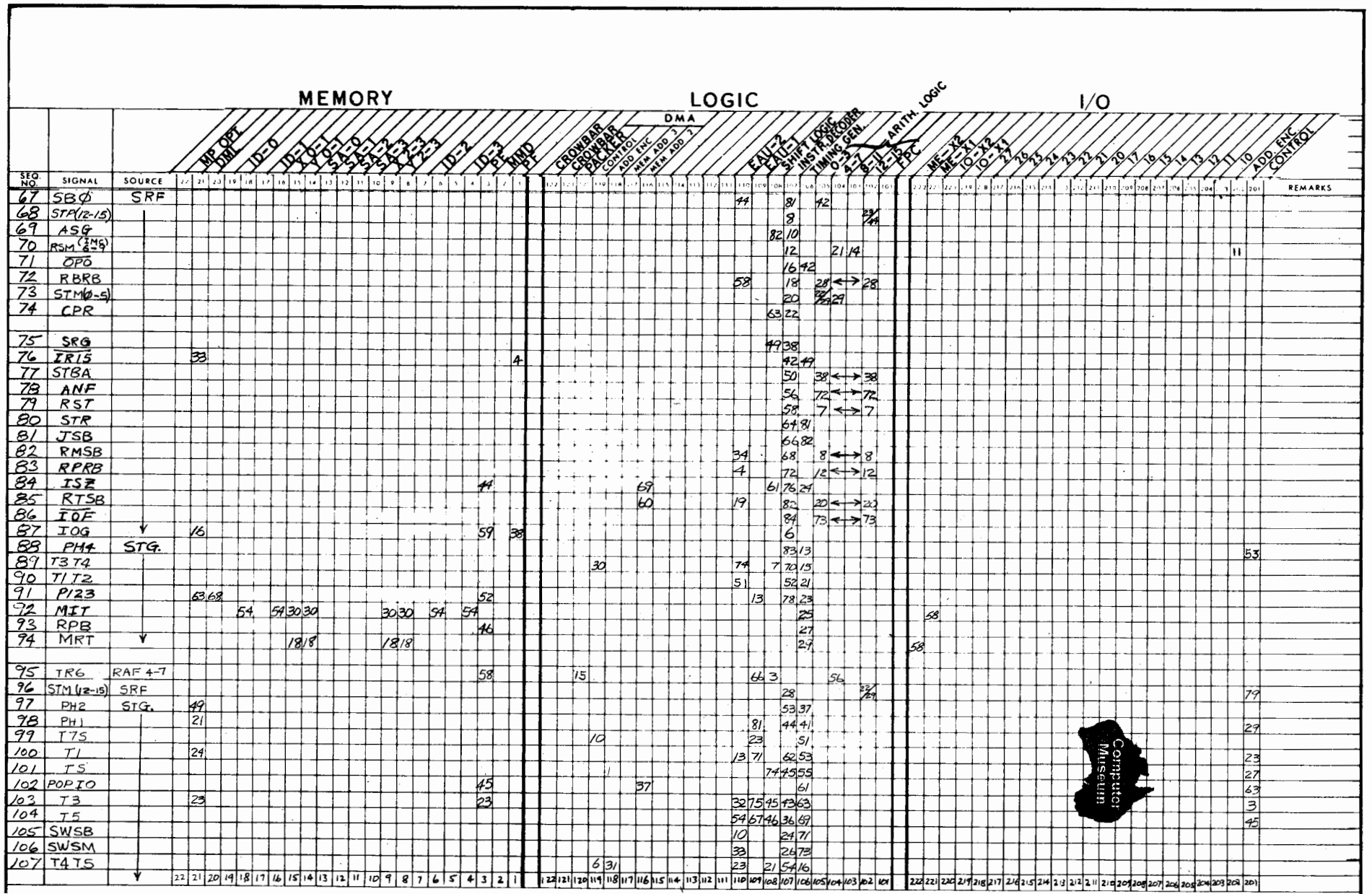
HP 2116B I/O CONTROL CARD



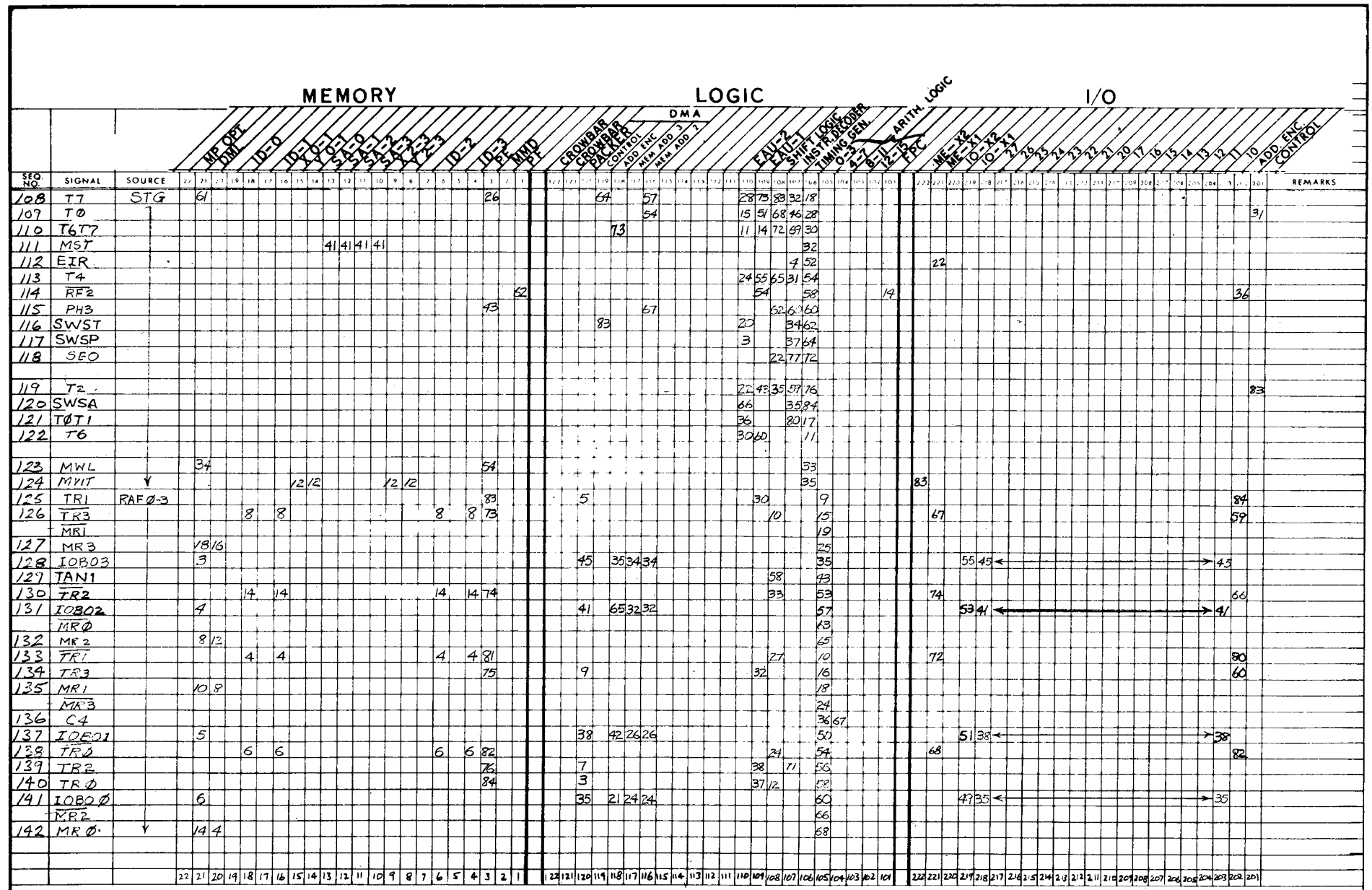
HP 2116B
BACKPLANE WIRE LIST



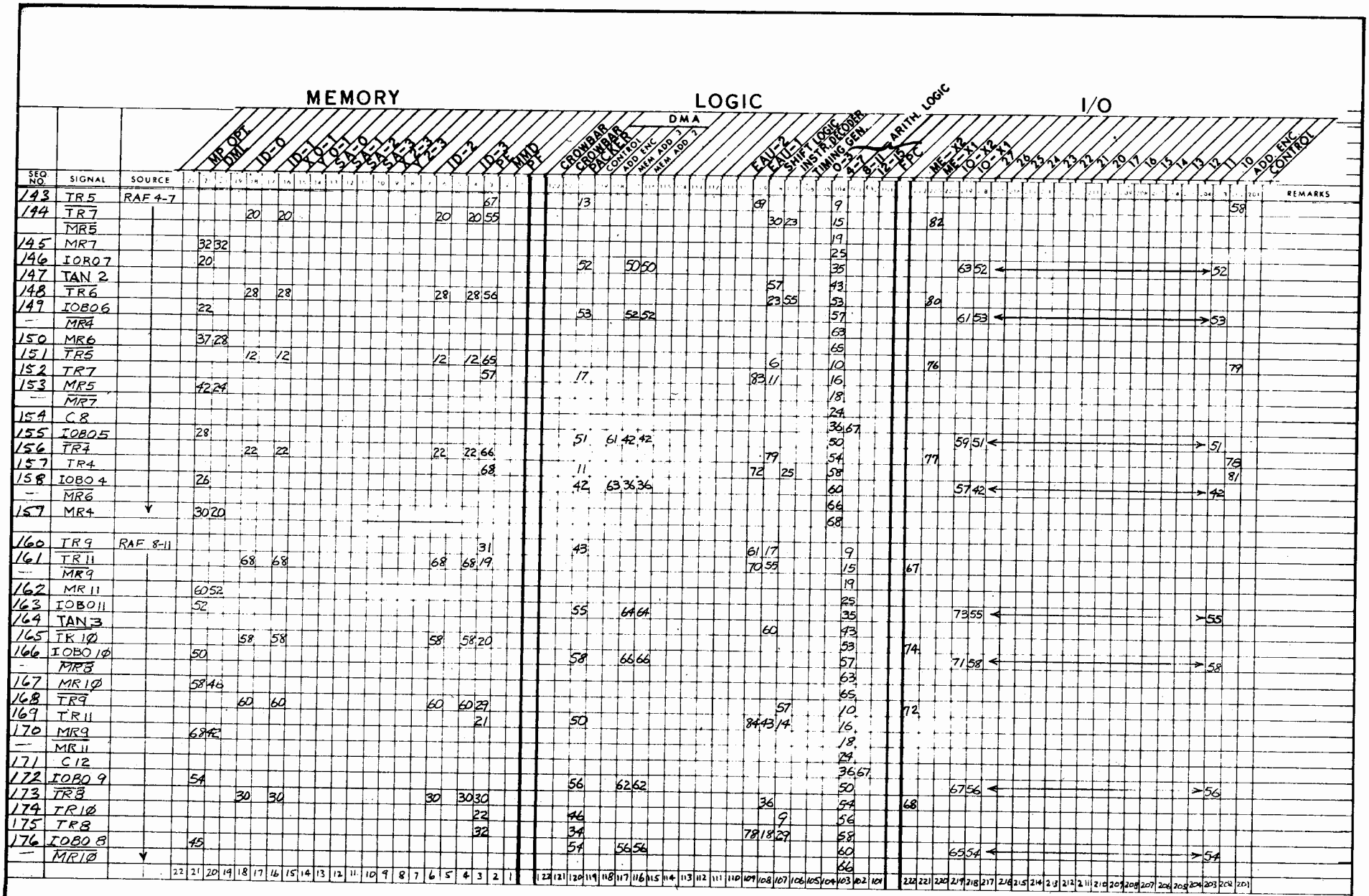
HP 2116B
BACKPLANE WIRE LIST



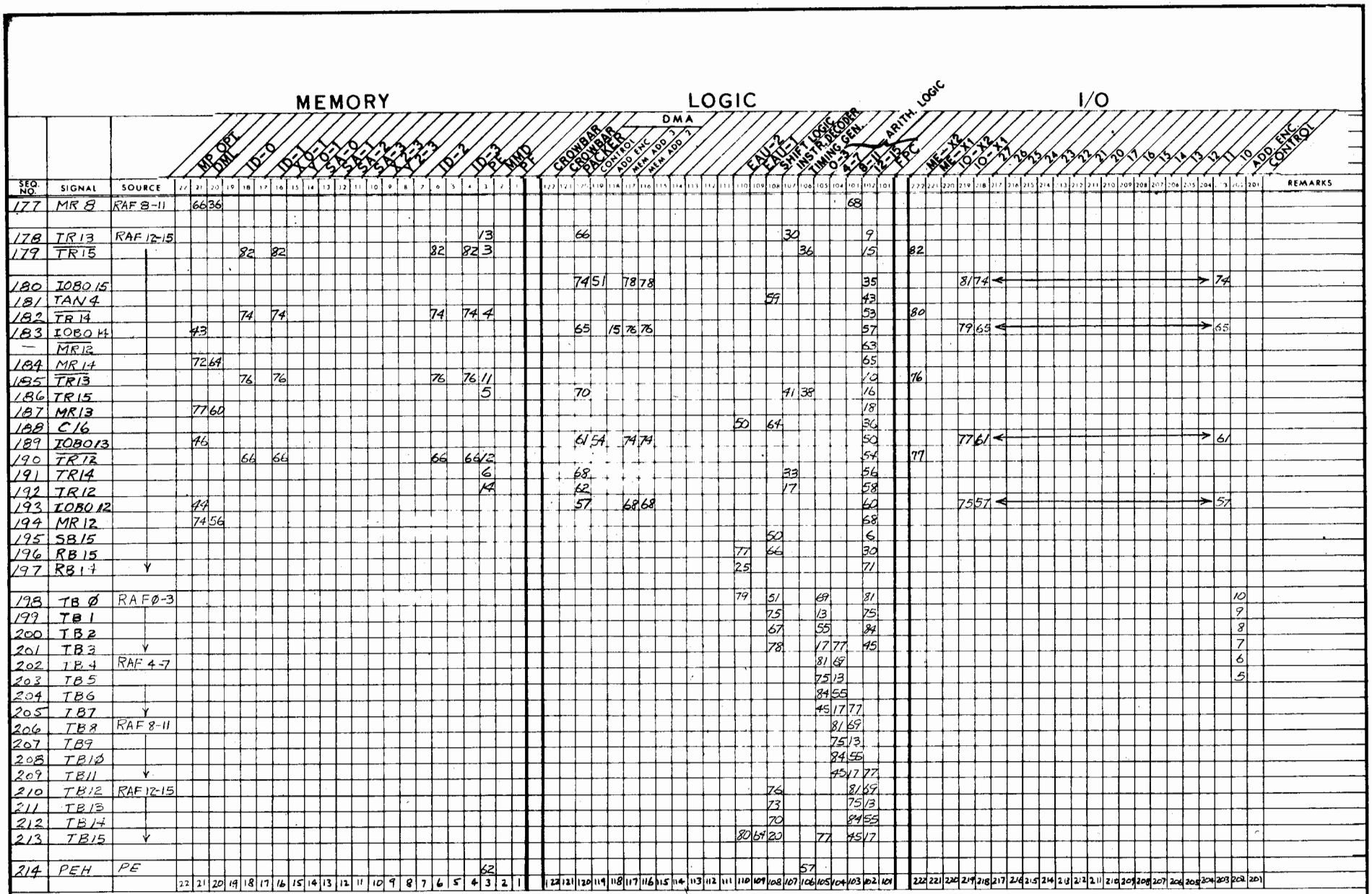
HP 2116B
BACKPLANE WIRE LIST



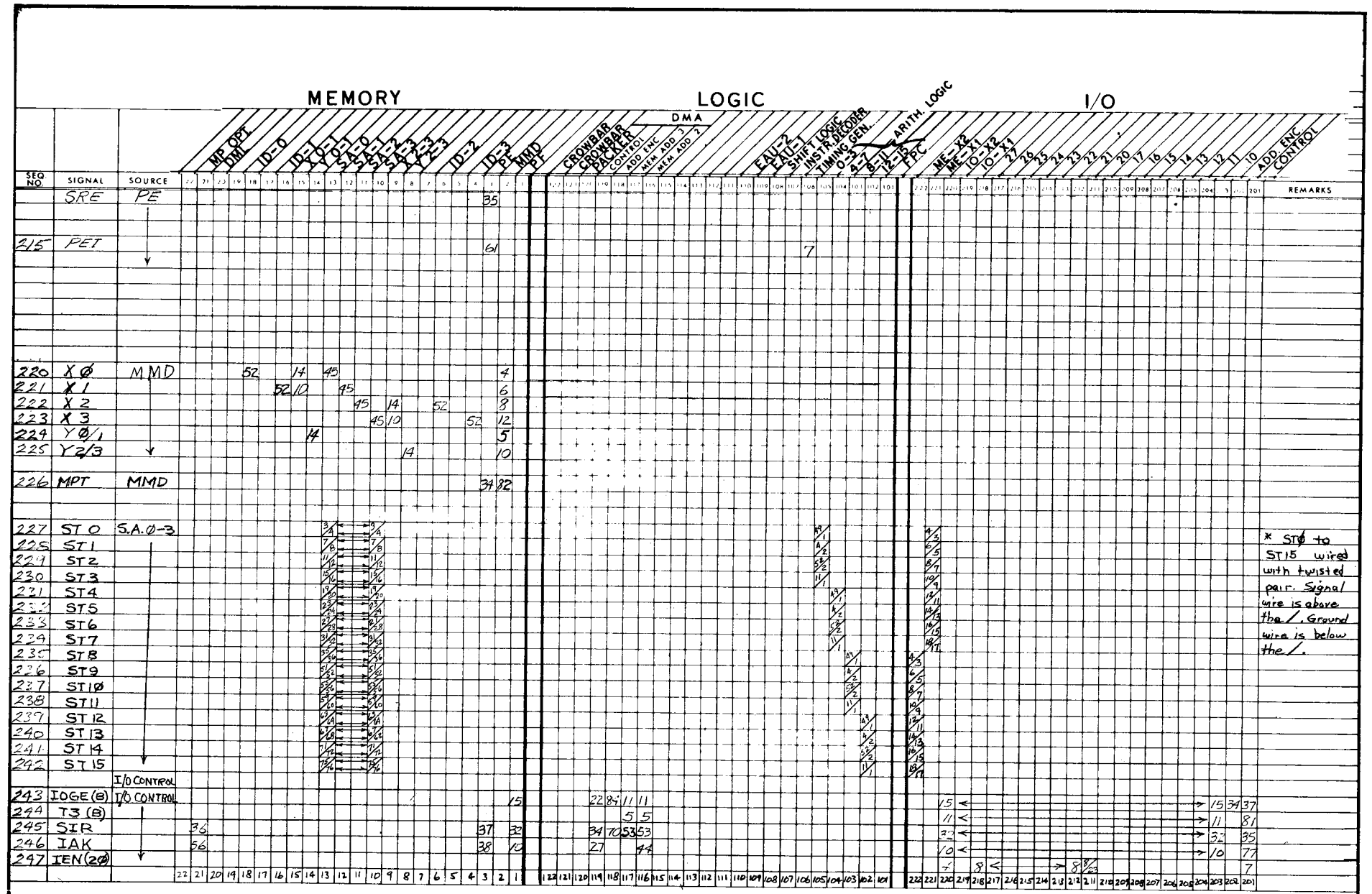
HP 2116B
BACKPLANE WIRE LIST



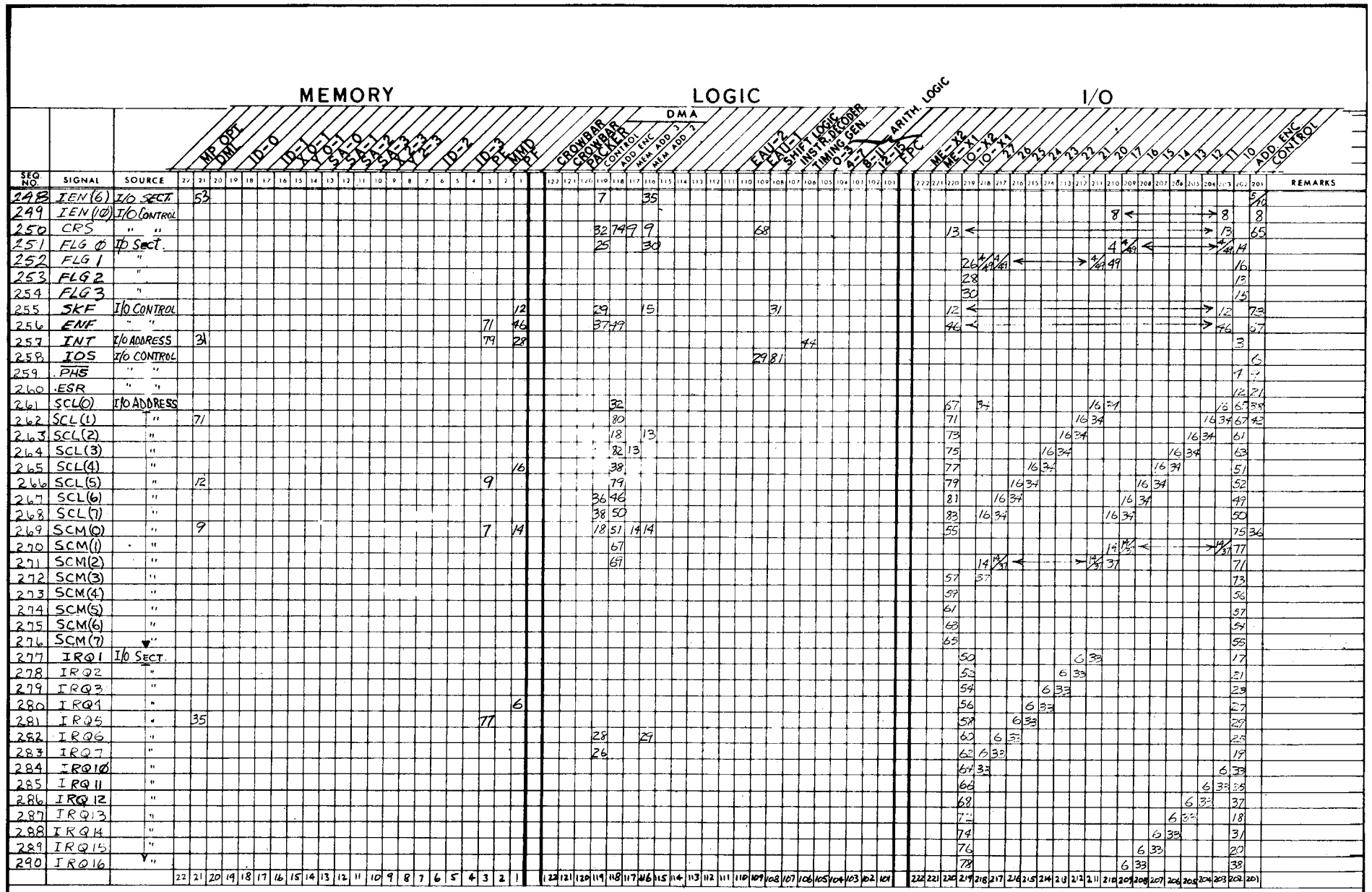
HP 2116B
BACKPLANE WIRE LIST



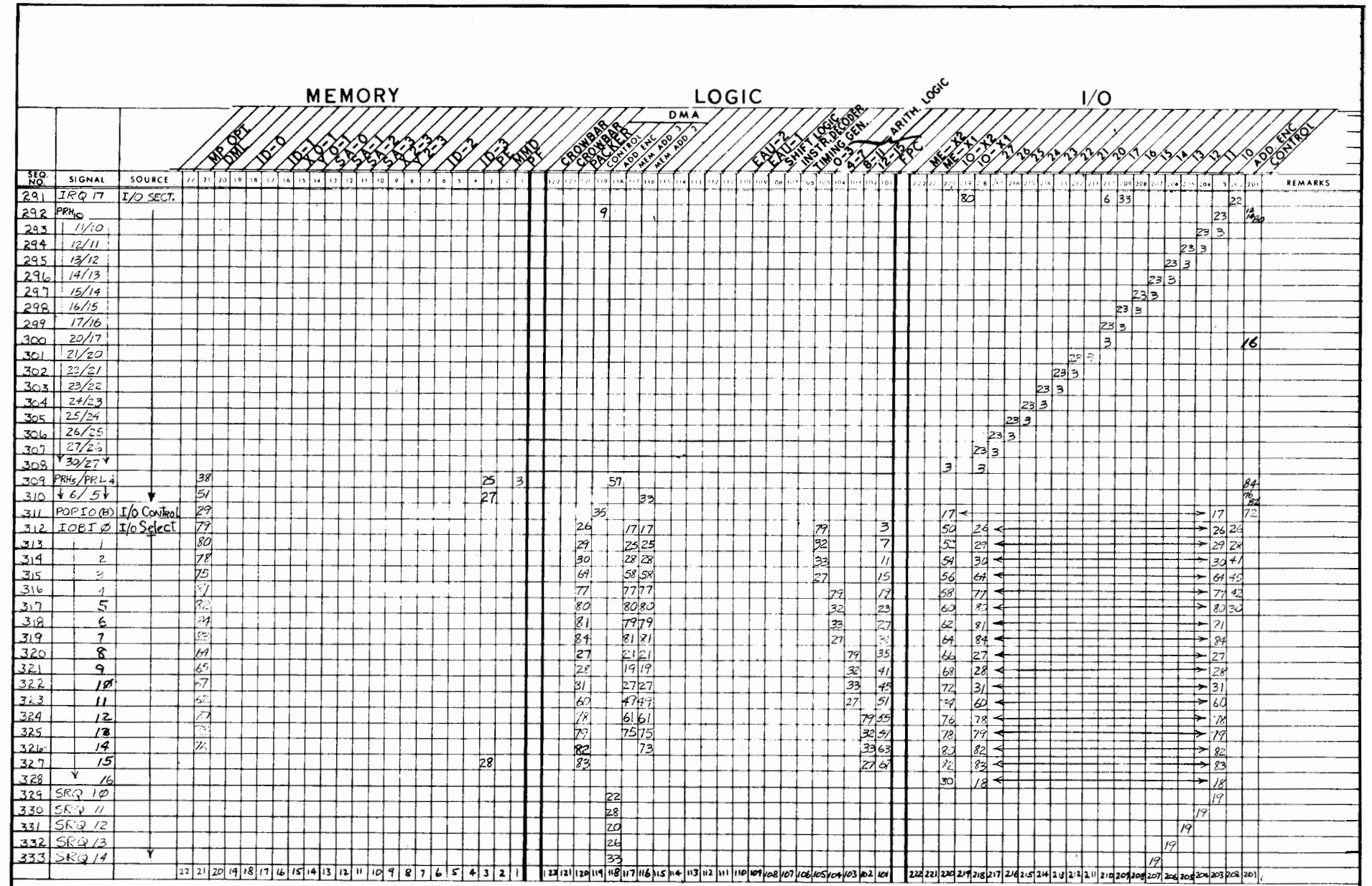
HP 2116B
BACKPLANE WIRE LIST



HP 2116B
BACKPLANE WIRE LIST



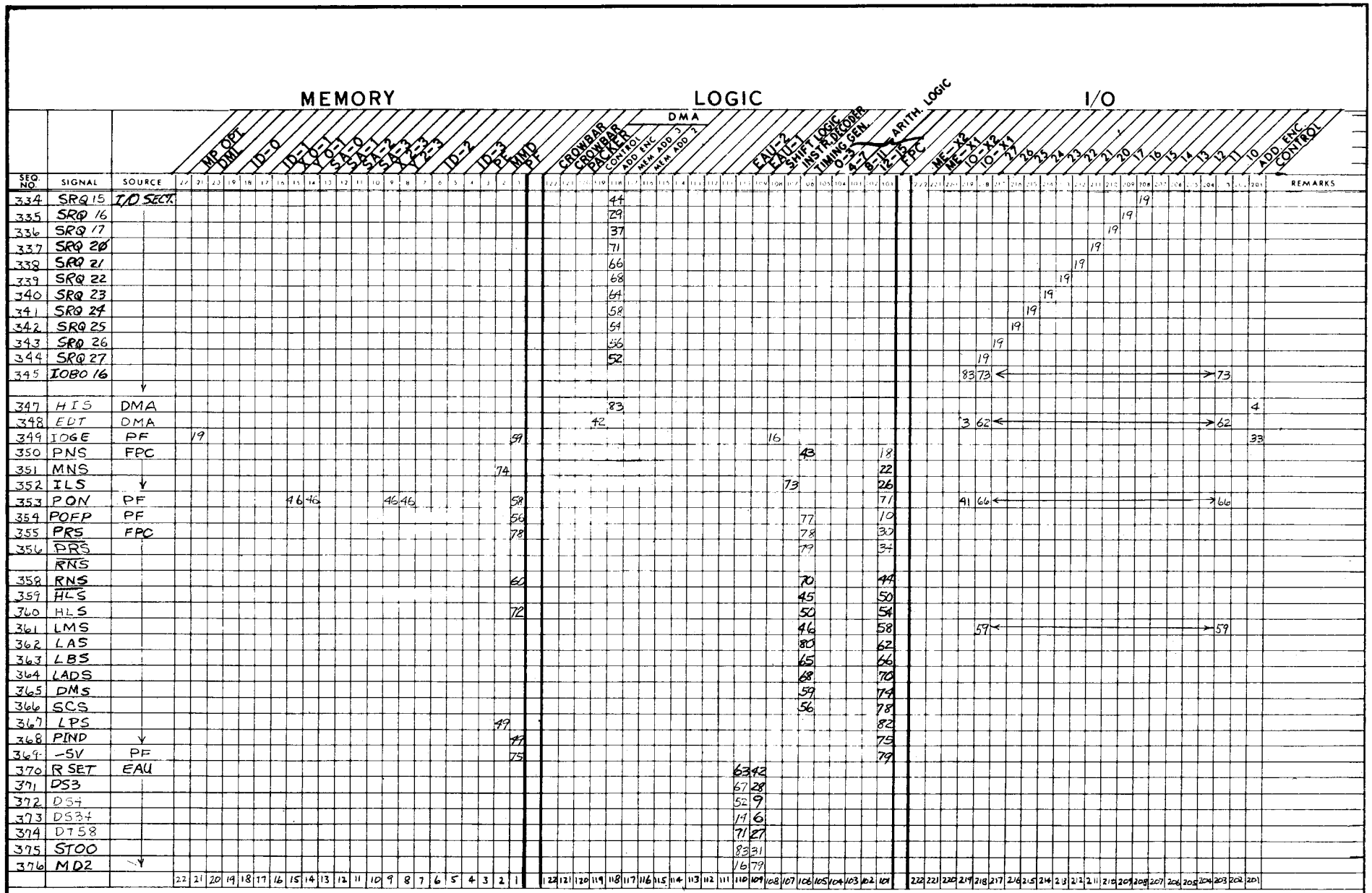
HP 2116B
BACKPLANE WIRE LIST



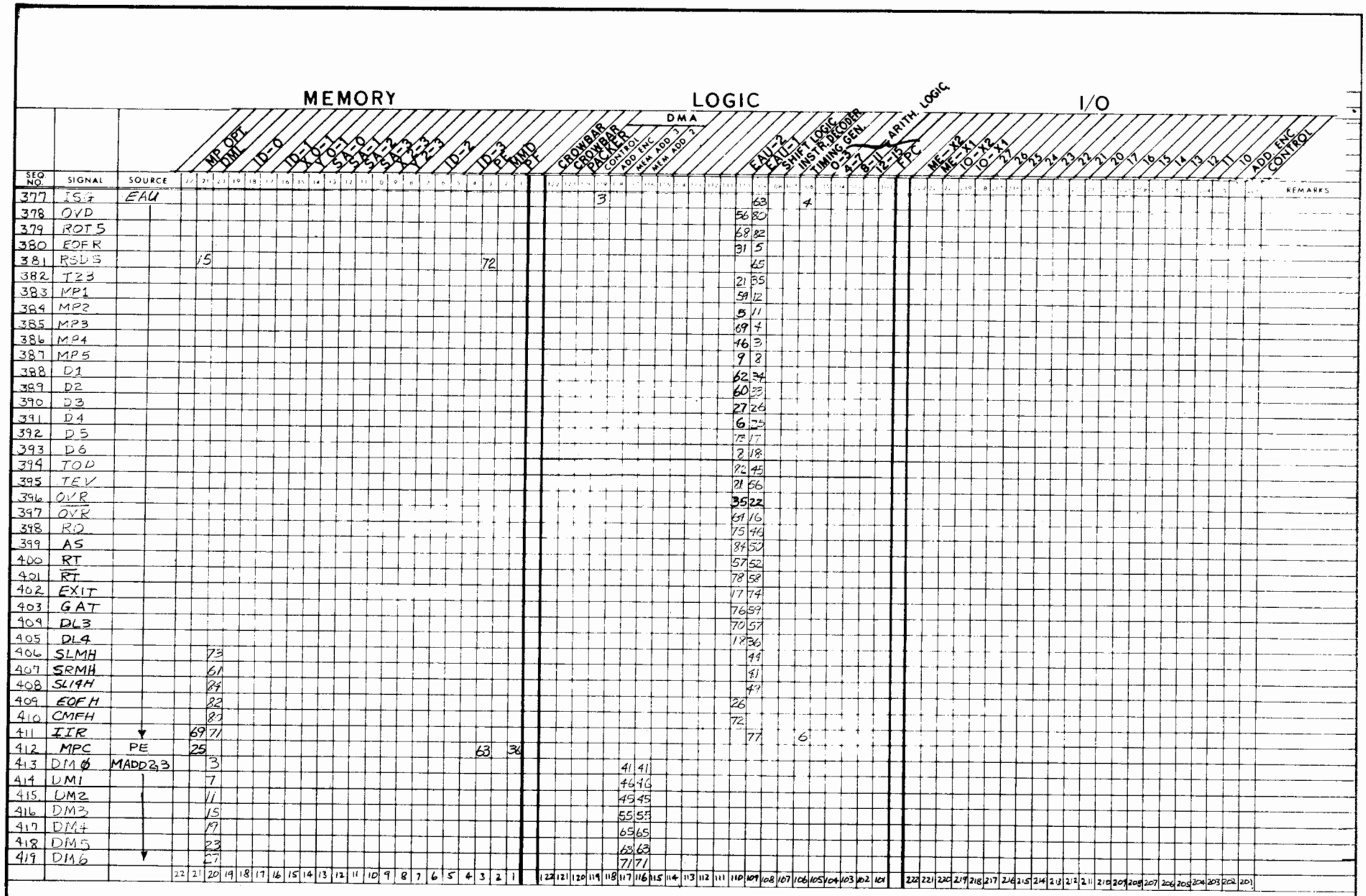
4-9

*PRL (17)

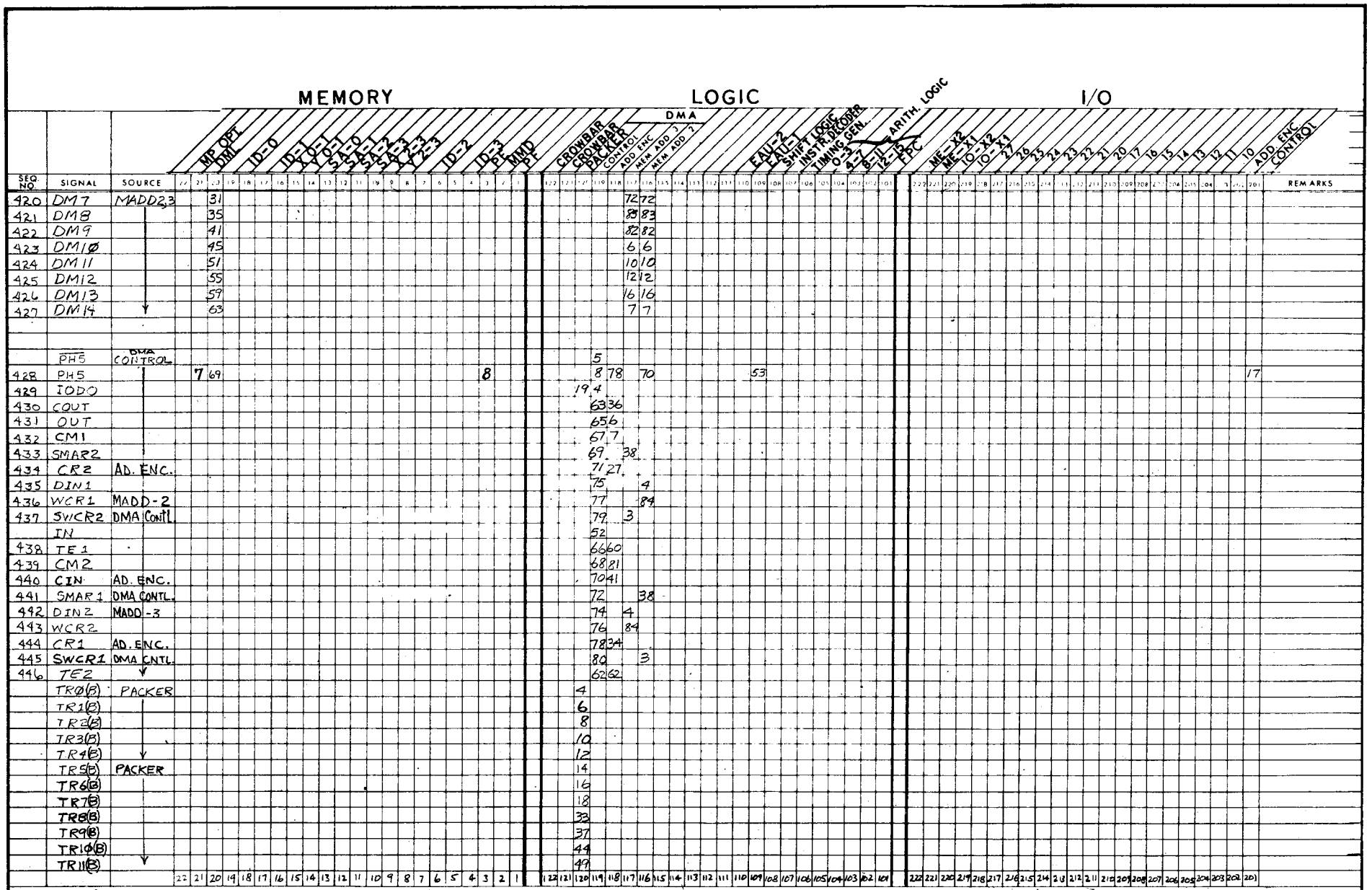
HP 2116B
BACKPLANE WIRE LIST



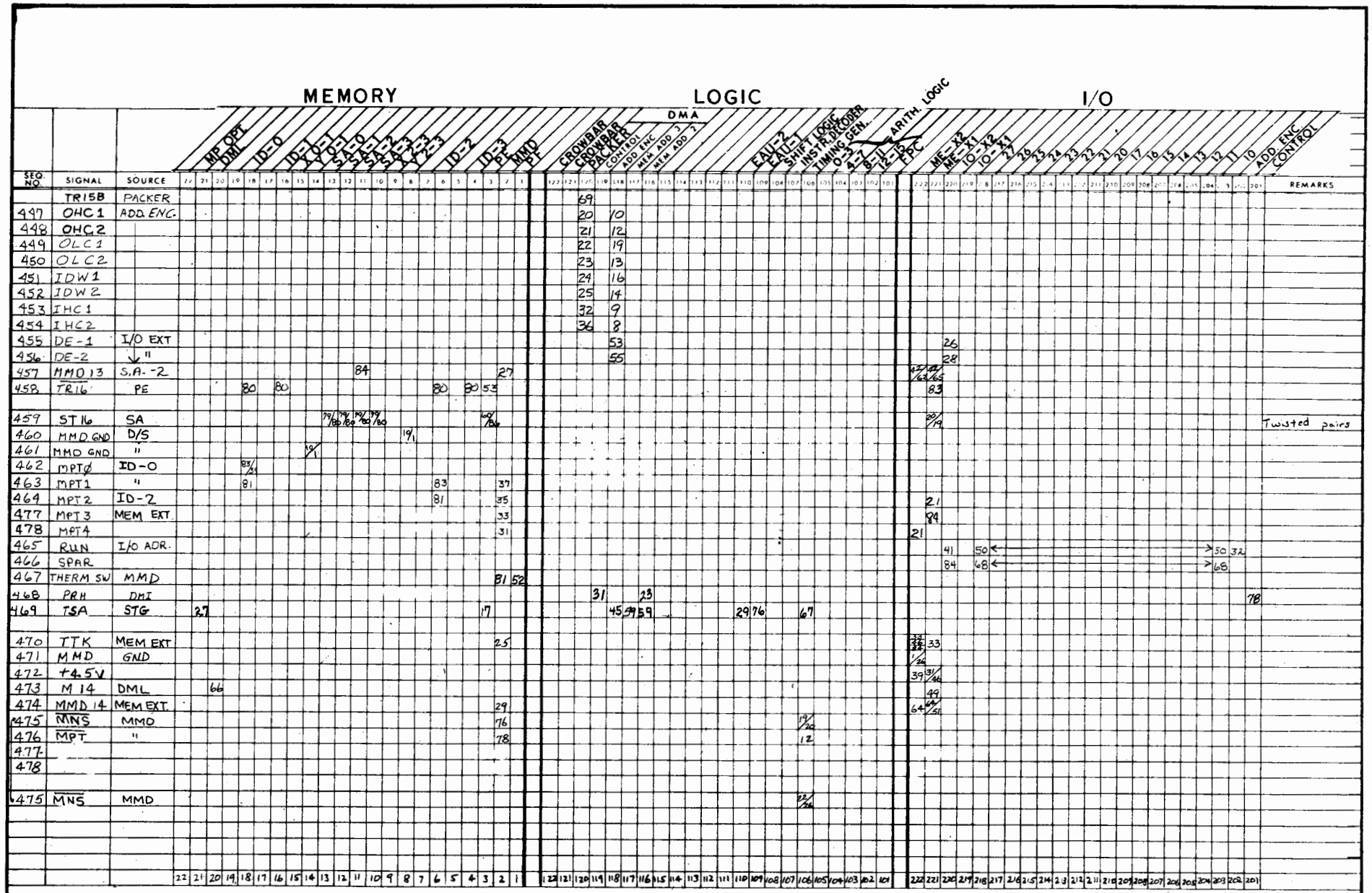
HP 2116B
BACKPLANE WIRE LIST



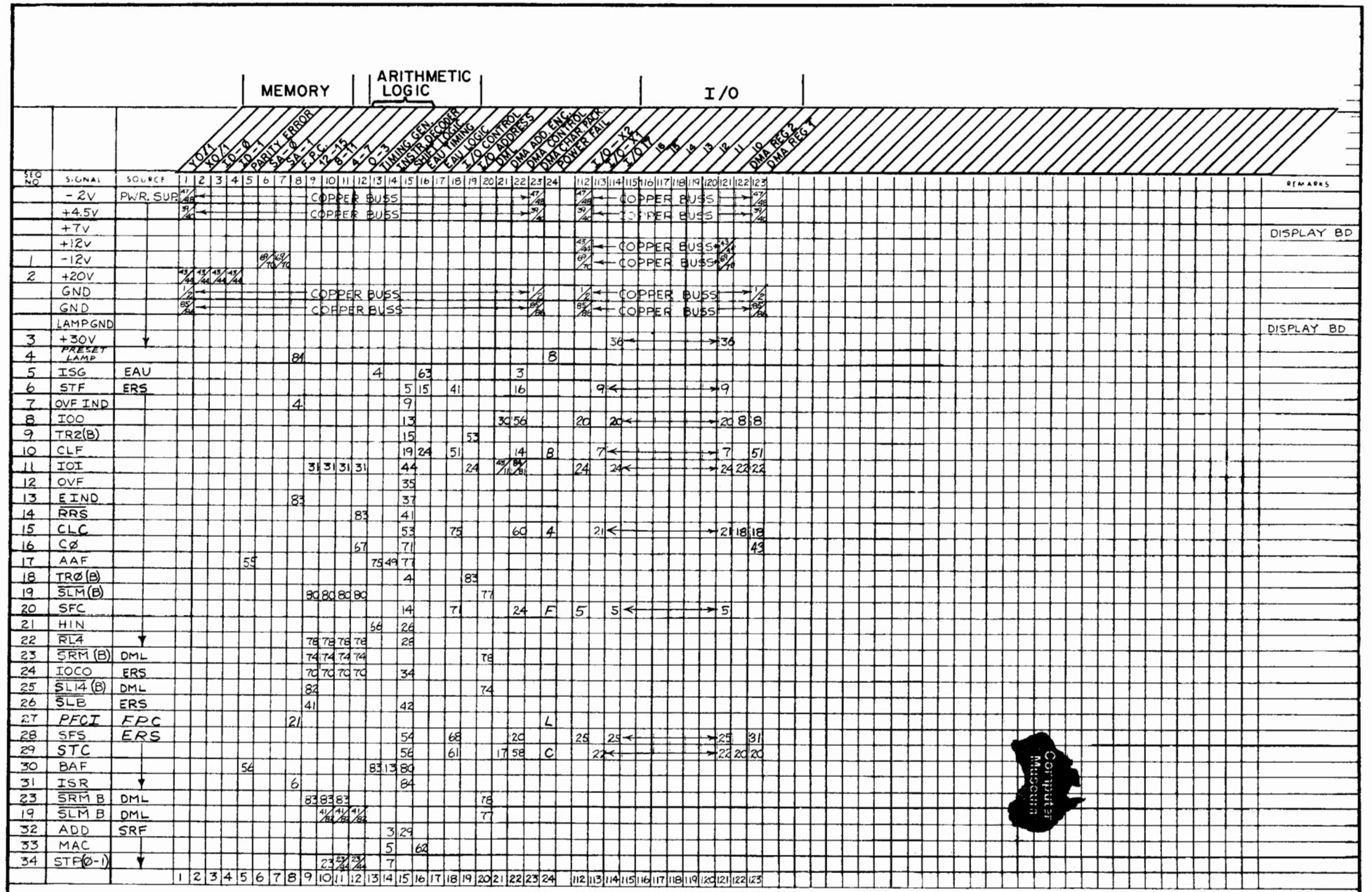
HP 2116B
BACKPLANE WIRE LIST



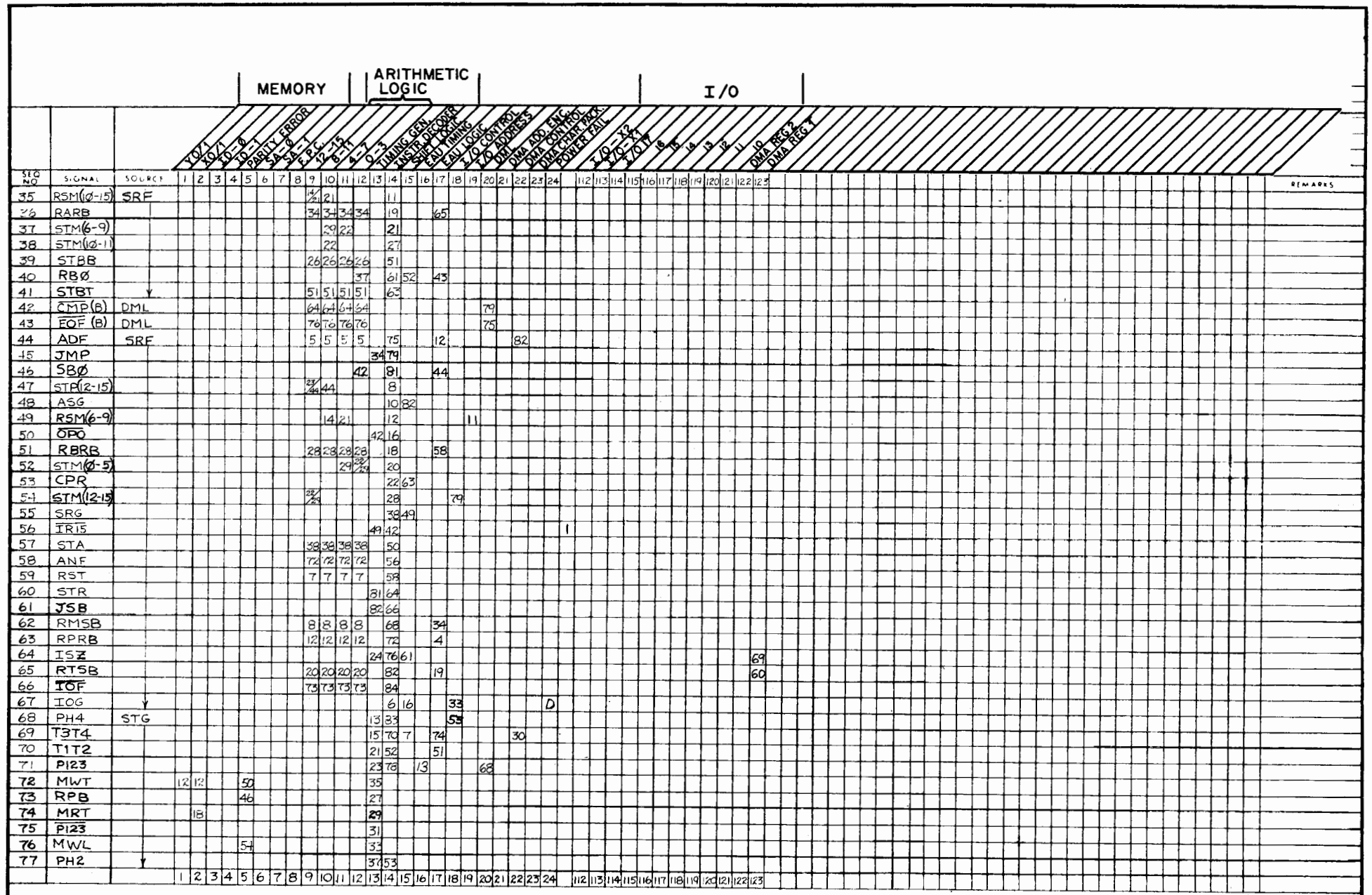
HP 2116B
BACKPLANE WIRE LIST



HP 2116B
BACKPLANE WIRE LIST

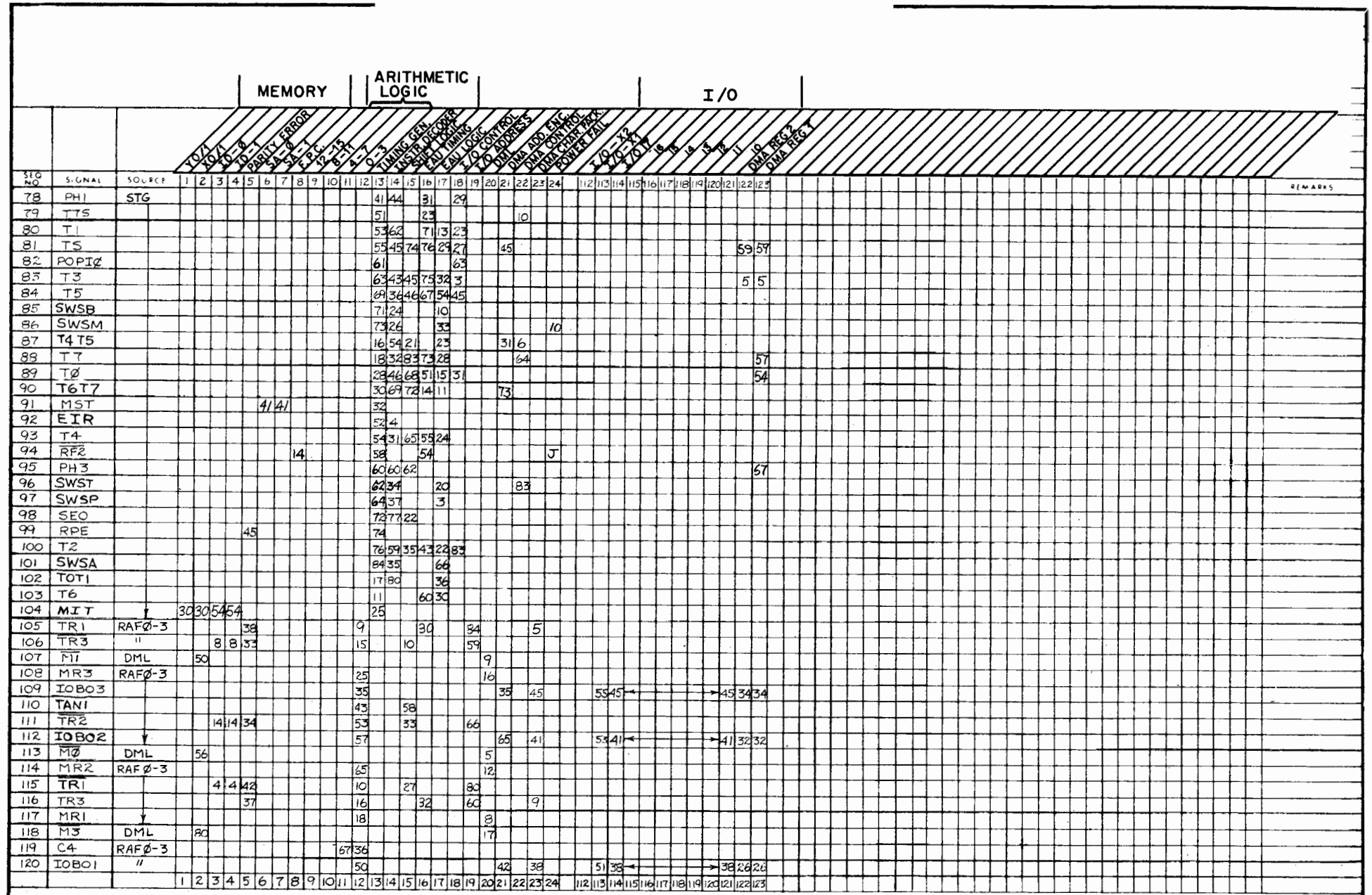


HP 2115A
BACKPLANE WIRE LIST

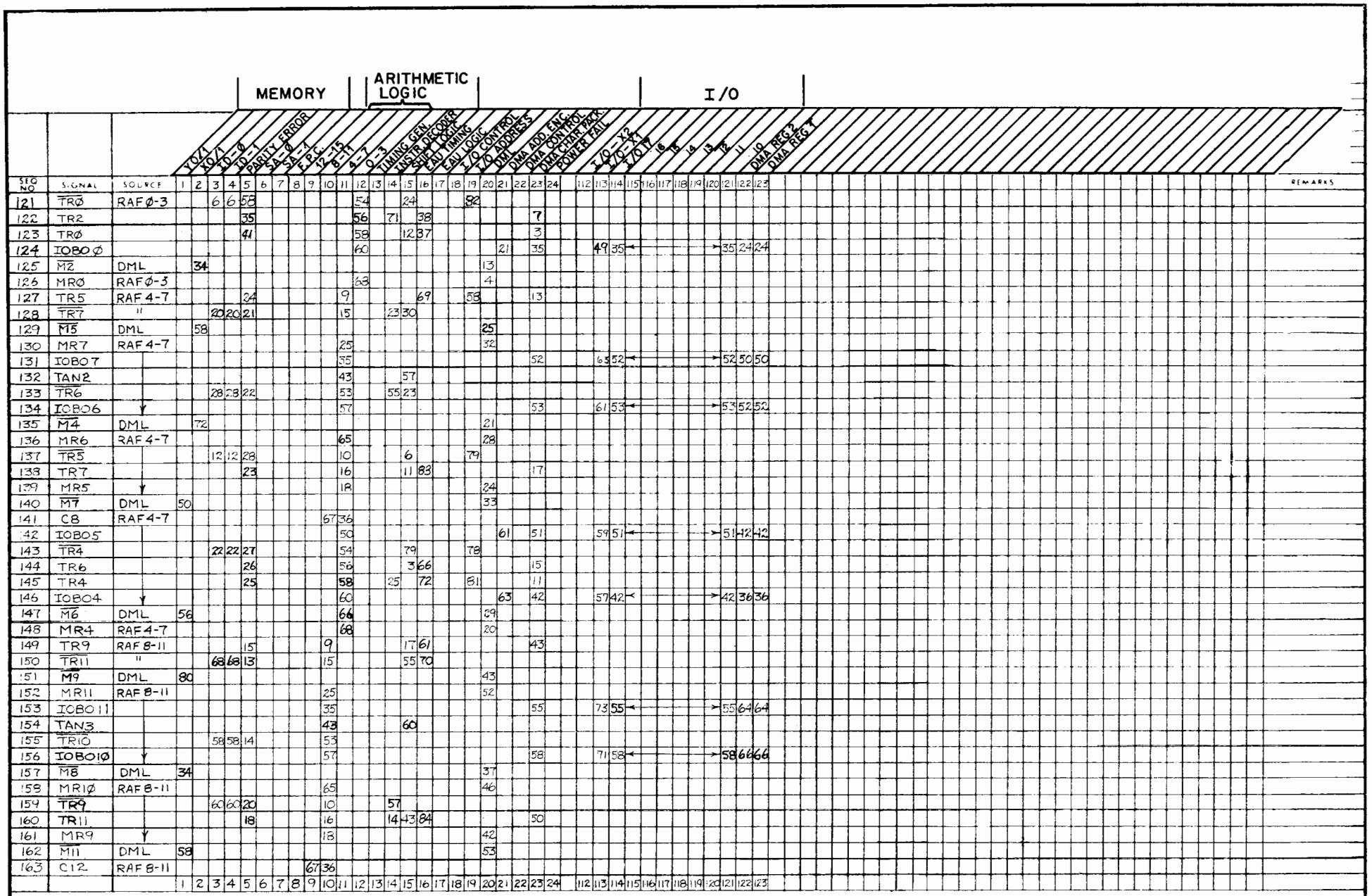


SEG NO	SIGNAL	SOURCE
35	RSM(Ø-15)	SRF
36	RARB	
37	STM(6-9)	
38	STM(Ø-1)	
39	STBB	
40	RBØ	
41	STBT	↓
42	CMP(B)	DML
43	EOF (B)	DML
44	ADF	SRF
45	JMP	
46	SBØ	
47	STP(12-15)	
48	ASG	
49	RSM(6-9)	
50	OPO	
51	RBRB	
52	STM(Ø-5)	
53	CPR	
54	STM(12-15)	
55	SRG	
56	IR15	
57	STA	
58	ANF	
59	RST	
60	STR	
61	JSB	
62	RMSB	
63	RPRB	
64	ISZ	
65	RTSB	
66	IOF	
67	IOG	↓
68	PH4	STG
69	T3T4	↓
70	T1T2	
71	PI23	
72	MWT	
73	RPB	
74	MRT	
75	PI23	
76	MWL	
77	PH2	↓

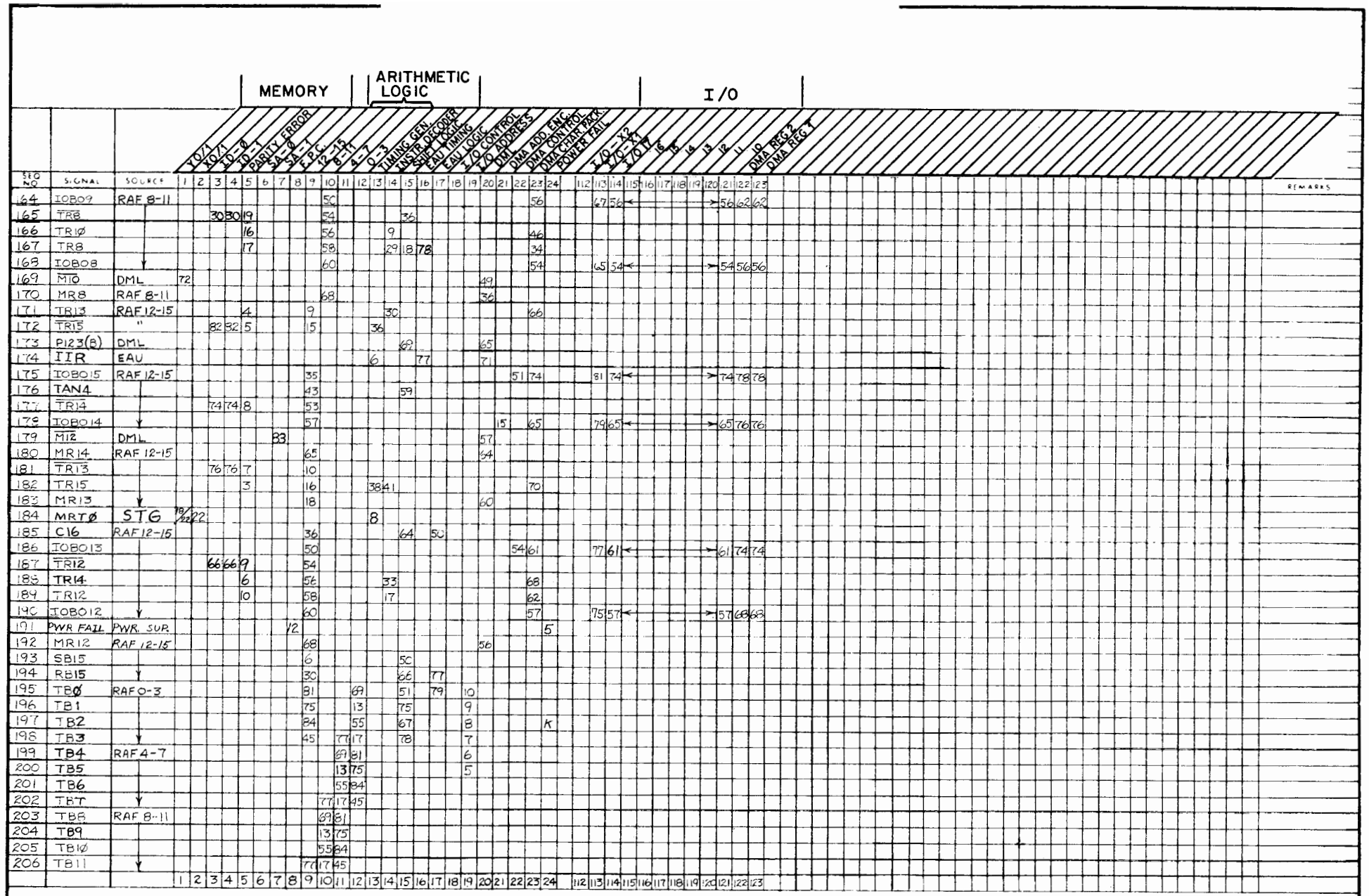
HP 2115A
BACKPLANE WIRE LIST



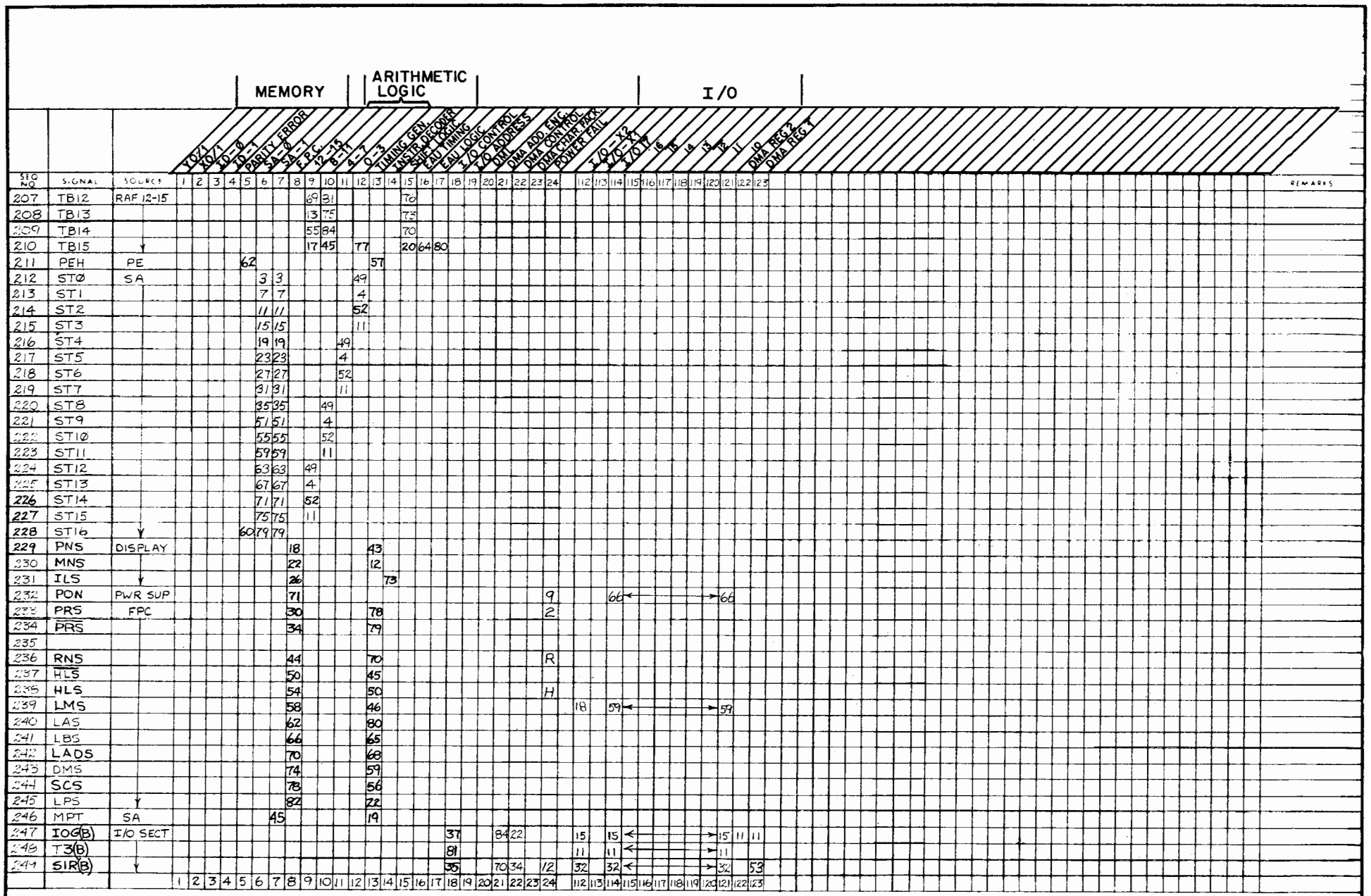
HP 2115A
BACKPLANE WIRE LIST



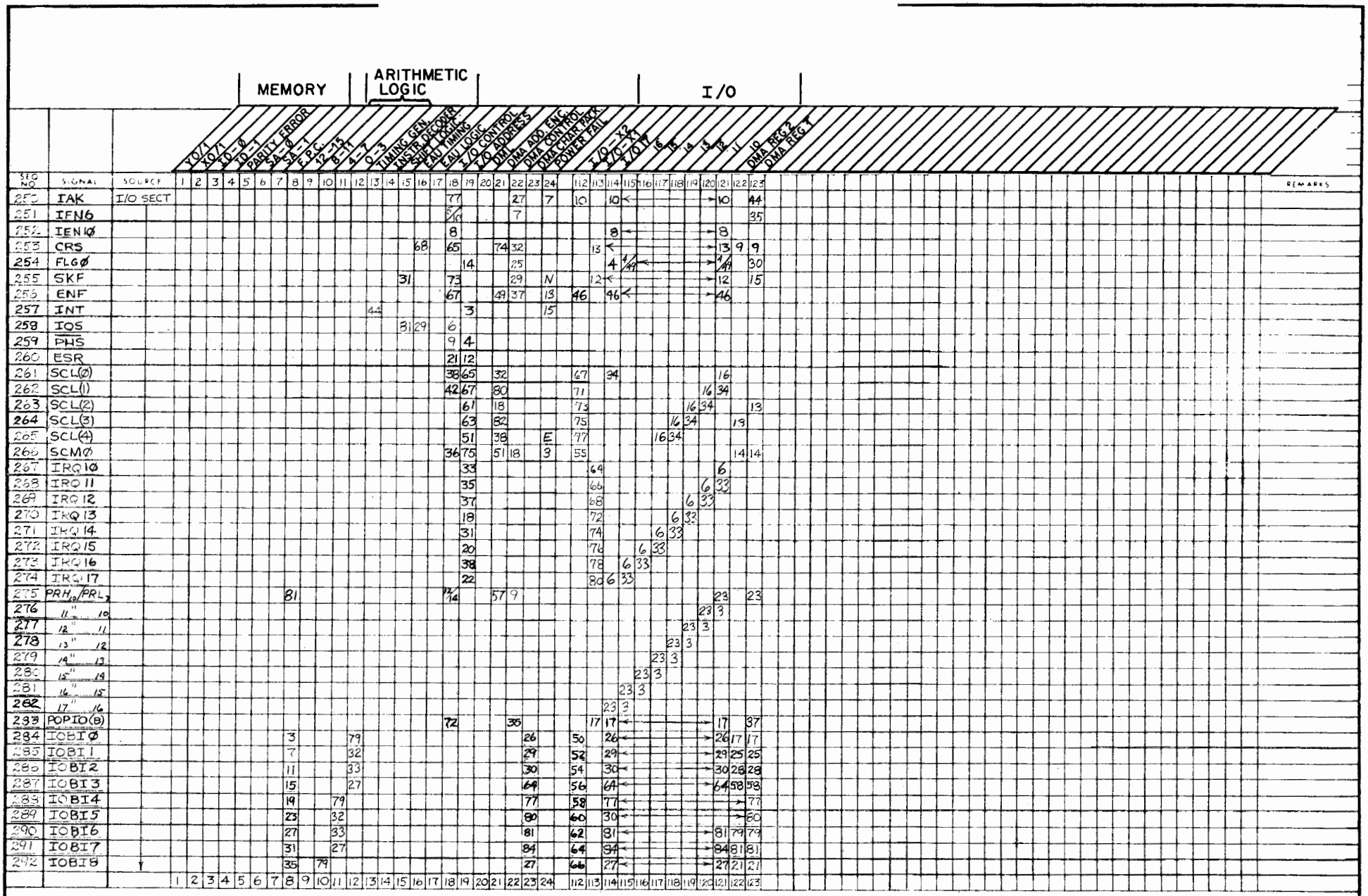
HP 2115A
BACKPLANE WIRE LIST



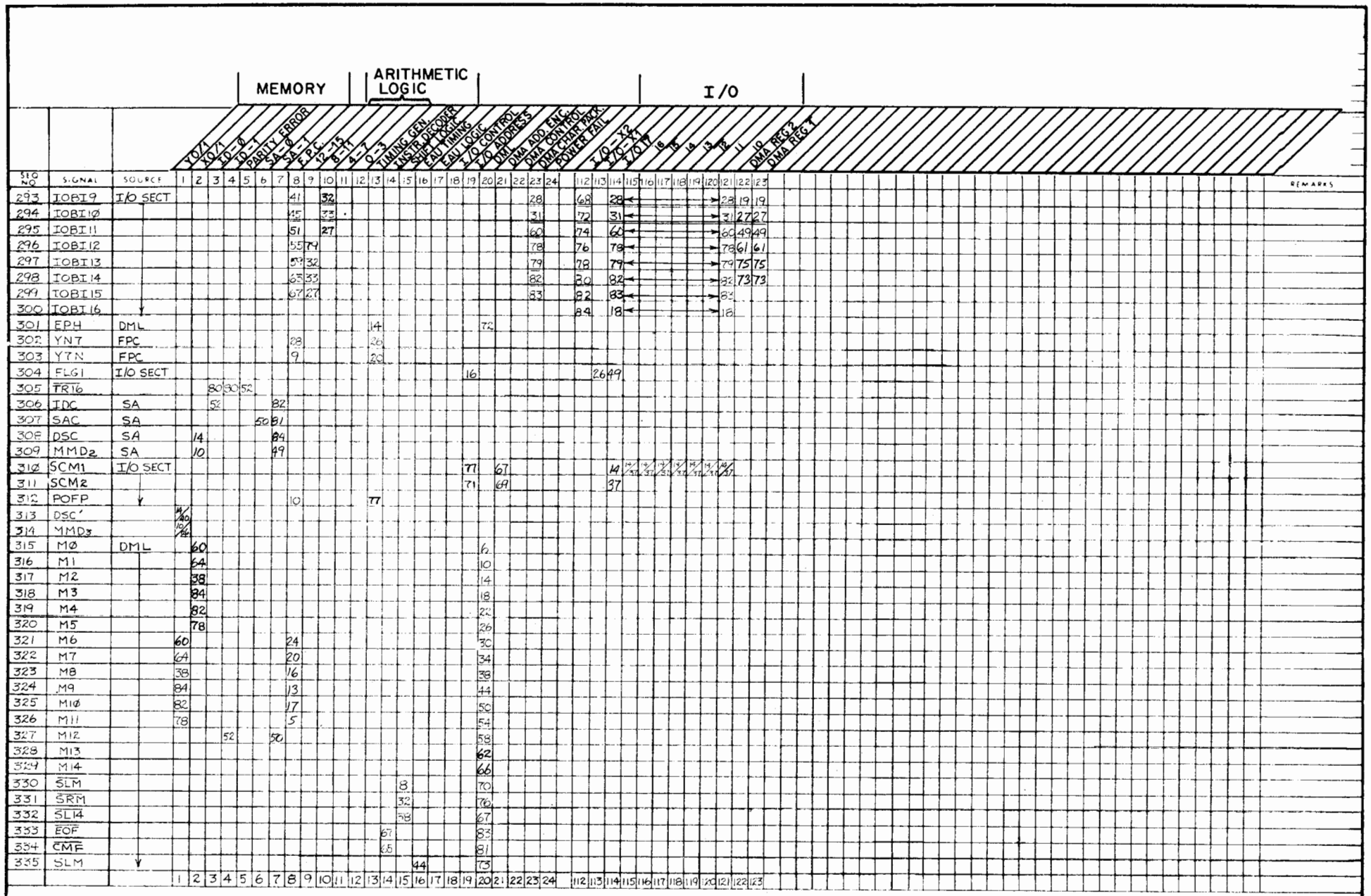
HP 2115A
BACKPLANE WIRE LIST



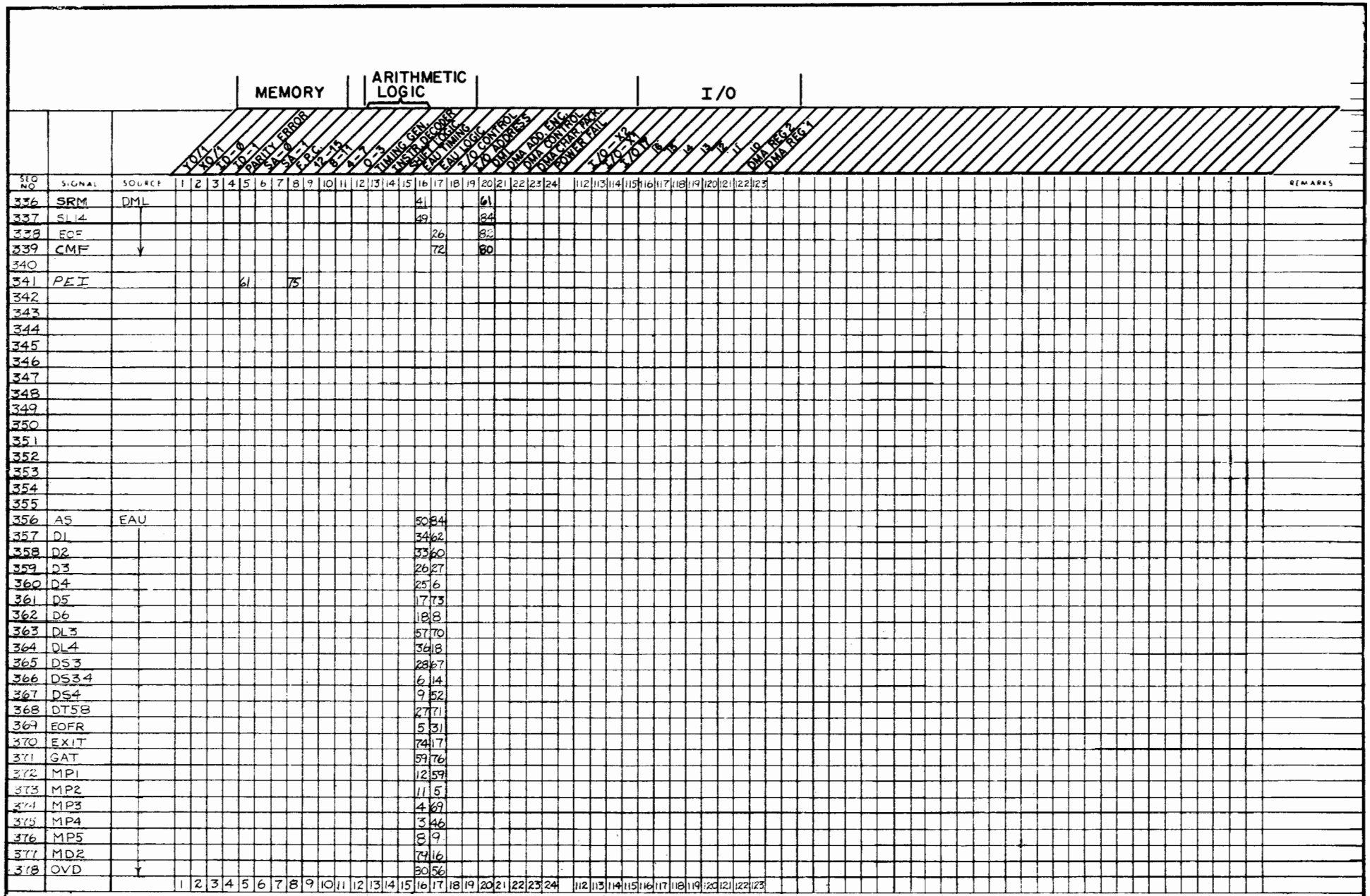
HP 2115A
BACKPLANE WIRE LIST



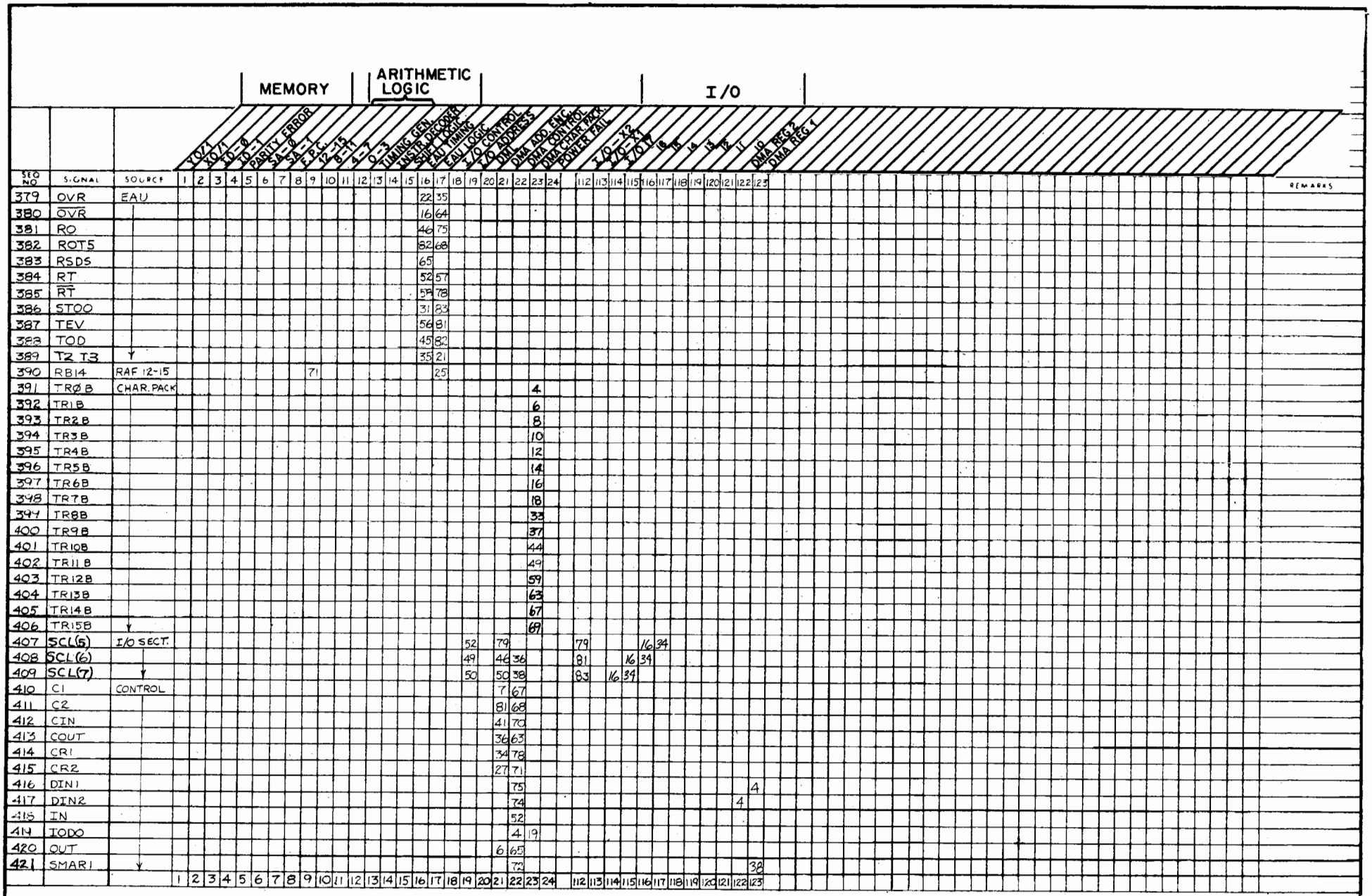
HP 2115A
BACKPLANE WIRE LIST



HP 2115A
BACKPLANE WIRE LIST

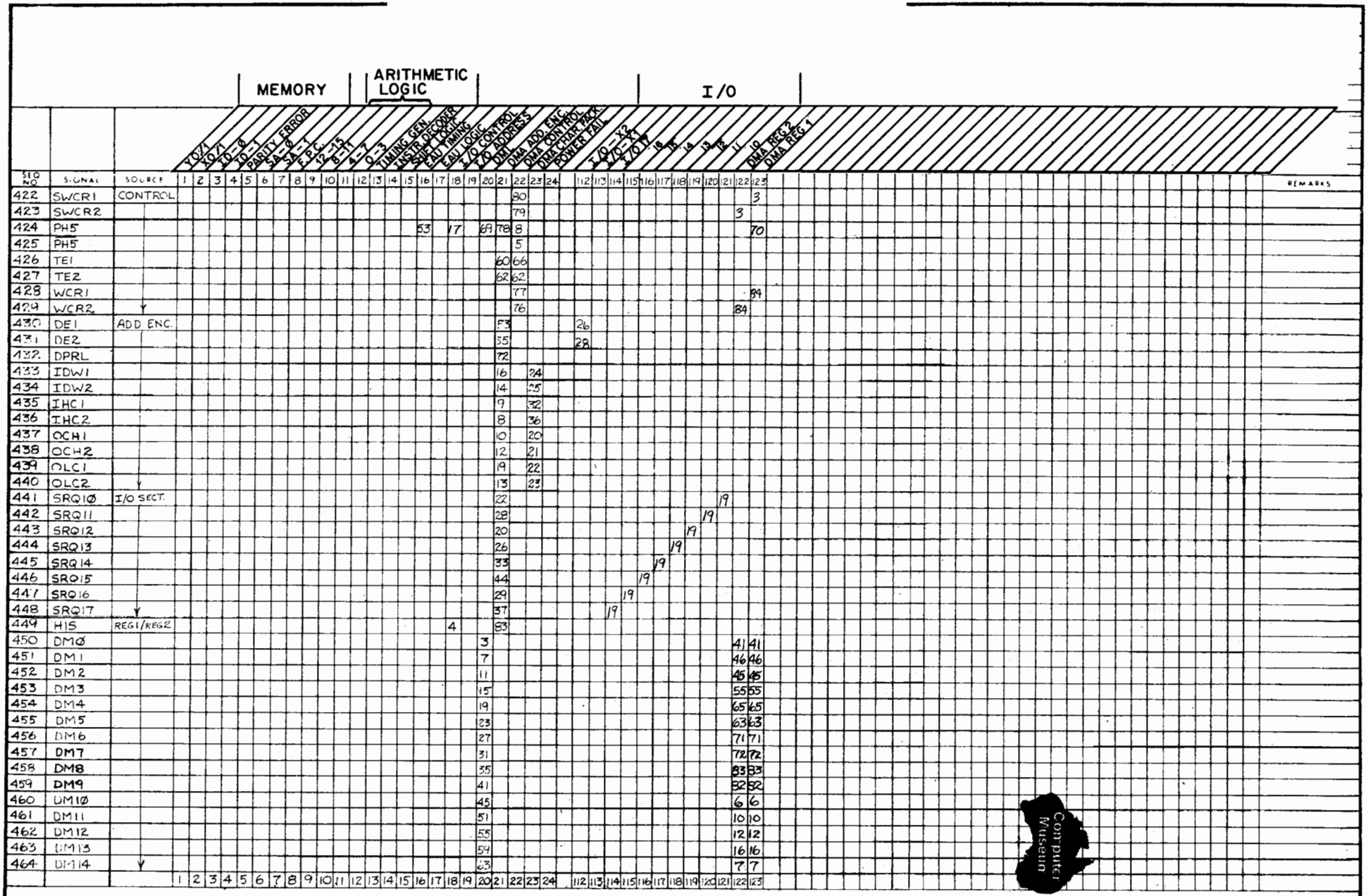


HP 2115A
BACKPLANE WIRE LIST

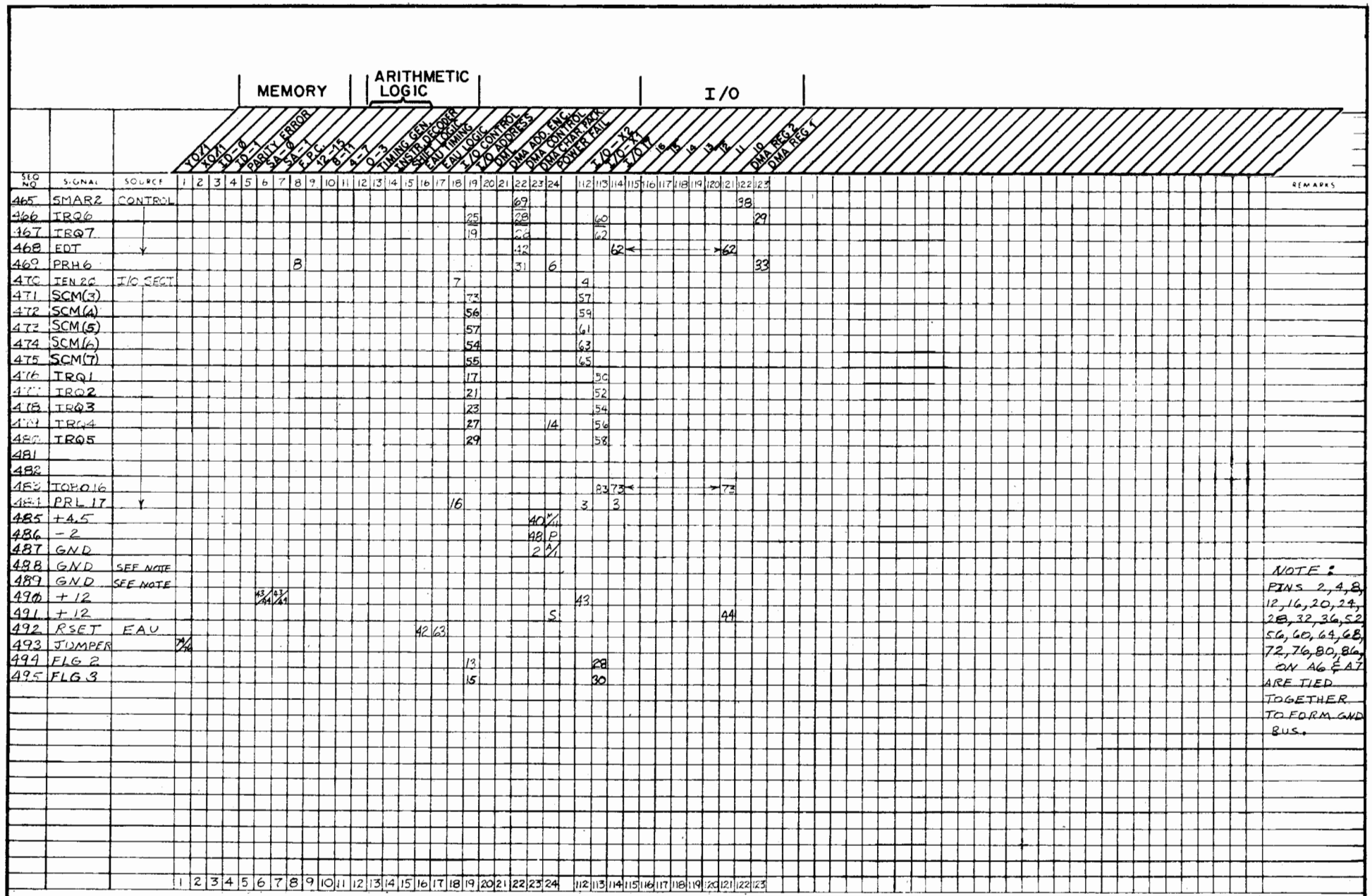


SEQ NO	SIGNAL	SOURCE	REMARKS
379	OVR	EAU	
380	$\overline{OVR}$		
381	RO		
382	ROT5		
383	RSDS		
384	RT		
385	$\overline{RT}$		
386	STOO		
387	TEV		
388	TOD		
389	T2 T3	↓	
390	RB14	RAF 12-15	
391	TRØB	CHAR. PACK	
392	TR1B		
393	TR2B		
394	TR3B		
395	TR4B		
396	TR5B		
397	TR6B		
398	TR7B		
399	TR8B		
400	TR9B		
401	TR10B		
402	TR11B		
403	TR12B		
404	TR13B		
405	TR14B		
406	TR15B	↓	
407	SCL(5)	I/O SECT.	
408	SCL(6)		
409	SCL(7)	↓	
410	CI	CONTROL	
411	C2		
412	CIN		
413	COUT		
414	CR1		
415	CR2		
416	DIN1		
417	DIN2		
418	IN		
419	IODO		
420	OUT		
421	SMAR1	↓	

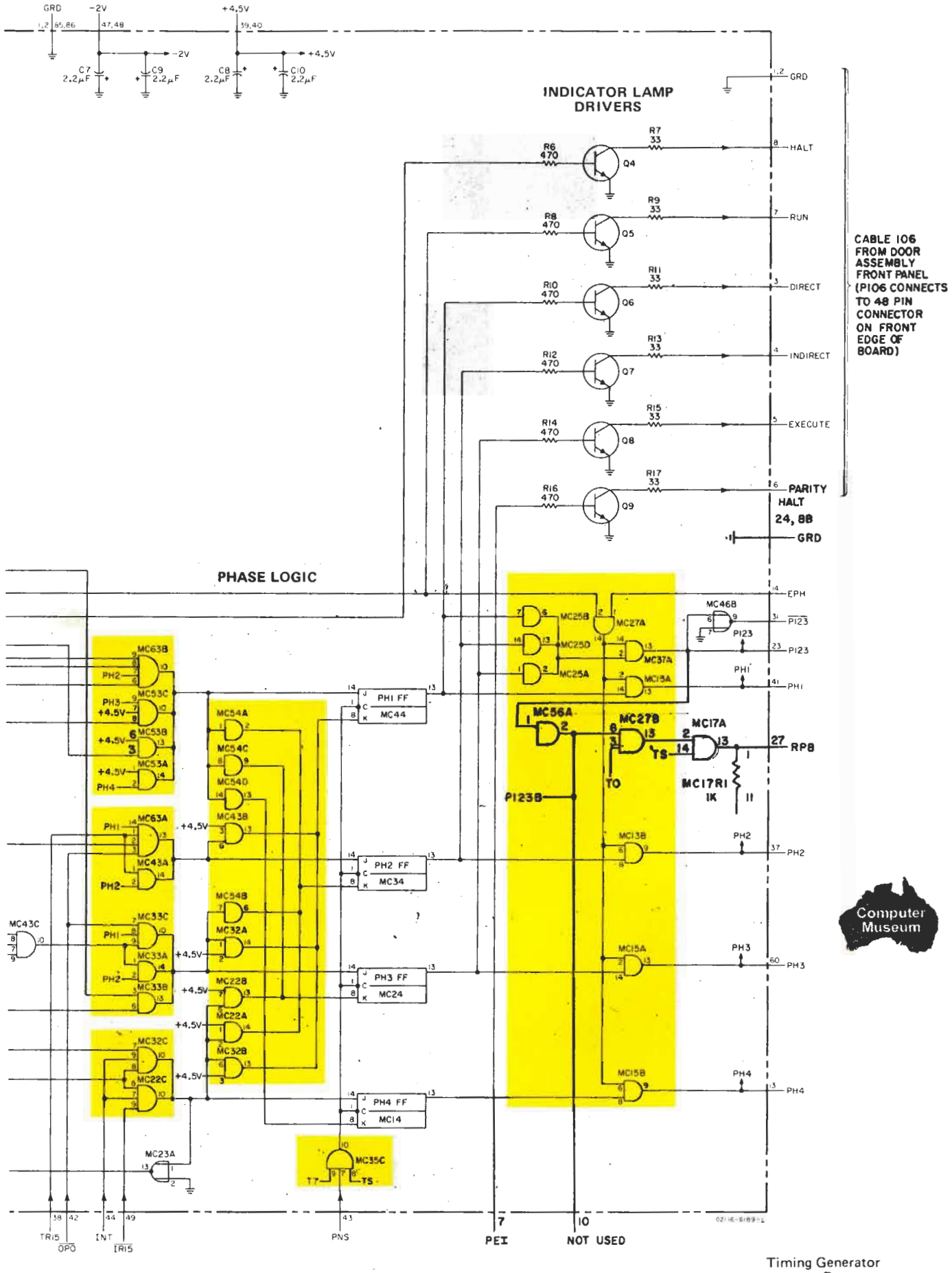
HP 2115A
BACKPLANE WIRE LIST



HP 2115A
BACKPLANE WIRE LIST

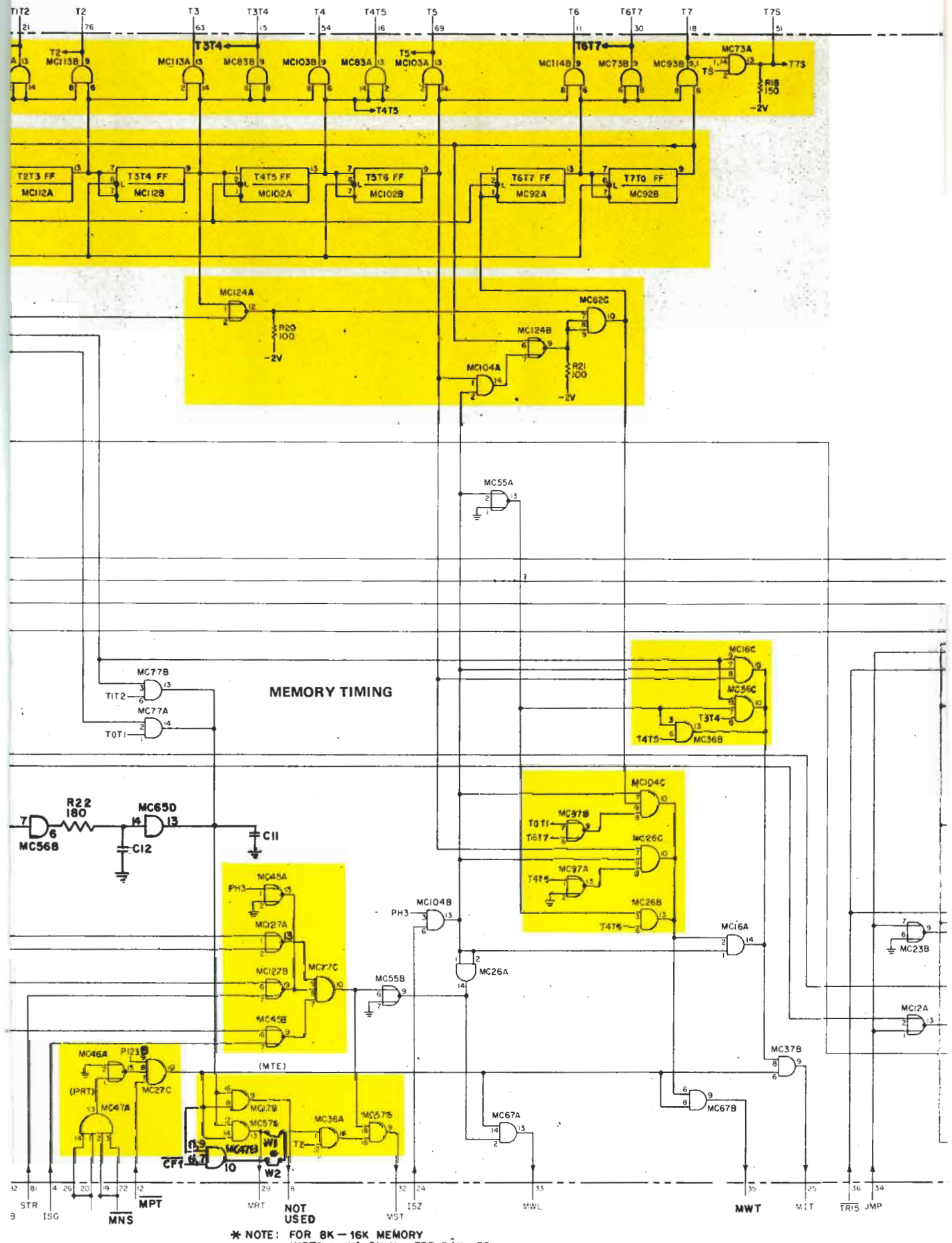


HP 2115A
BACKPLANE WIRE LIST

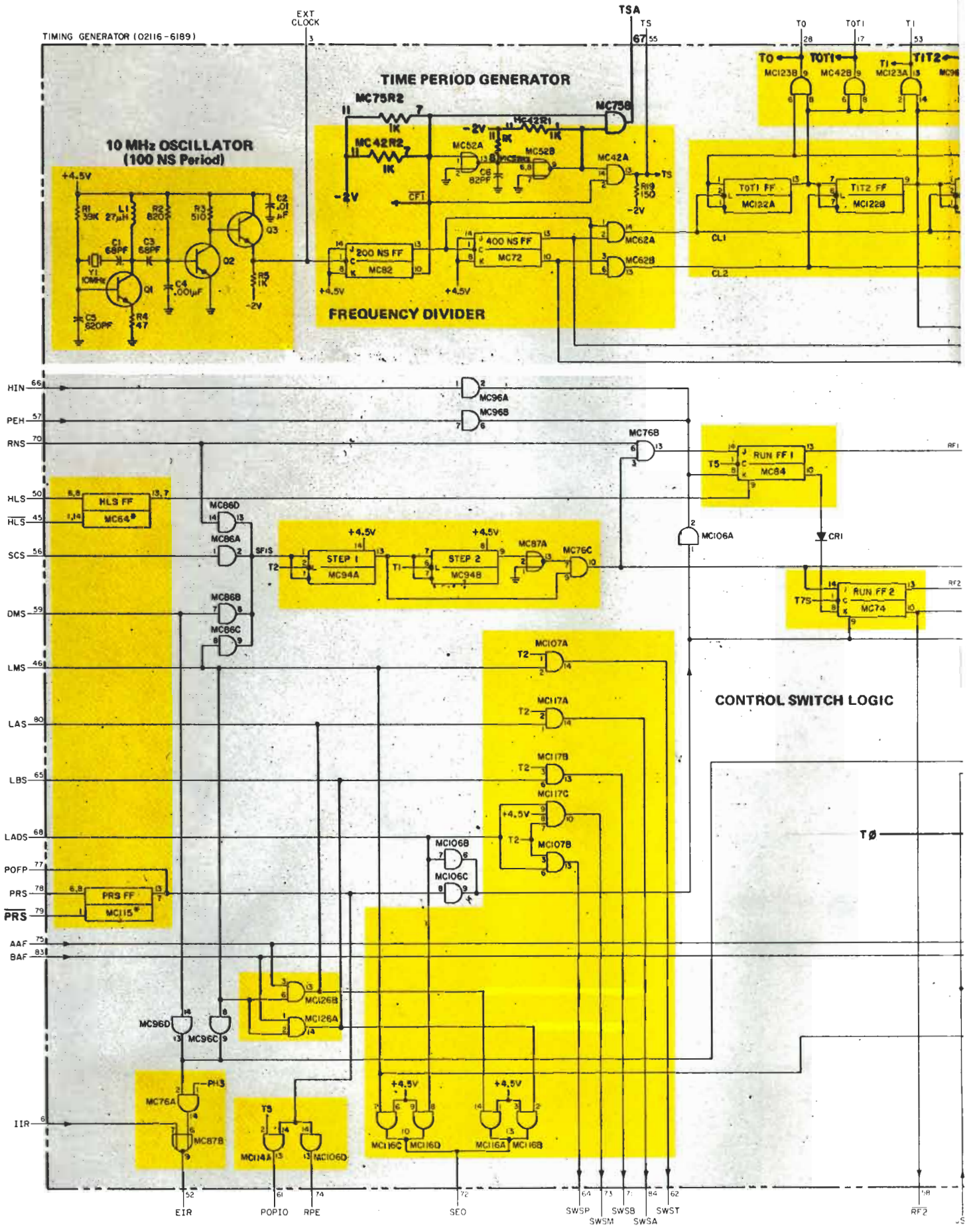


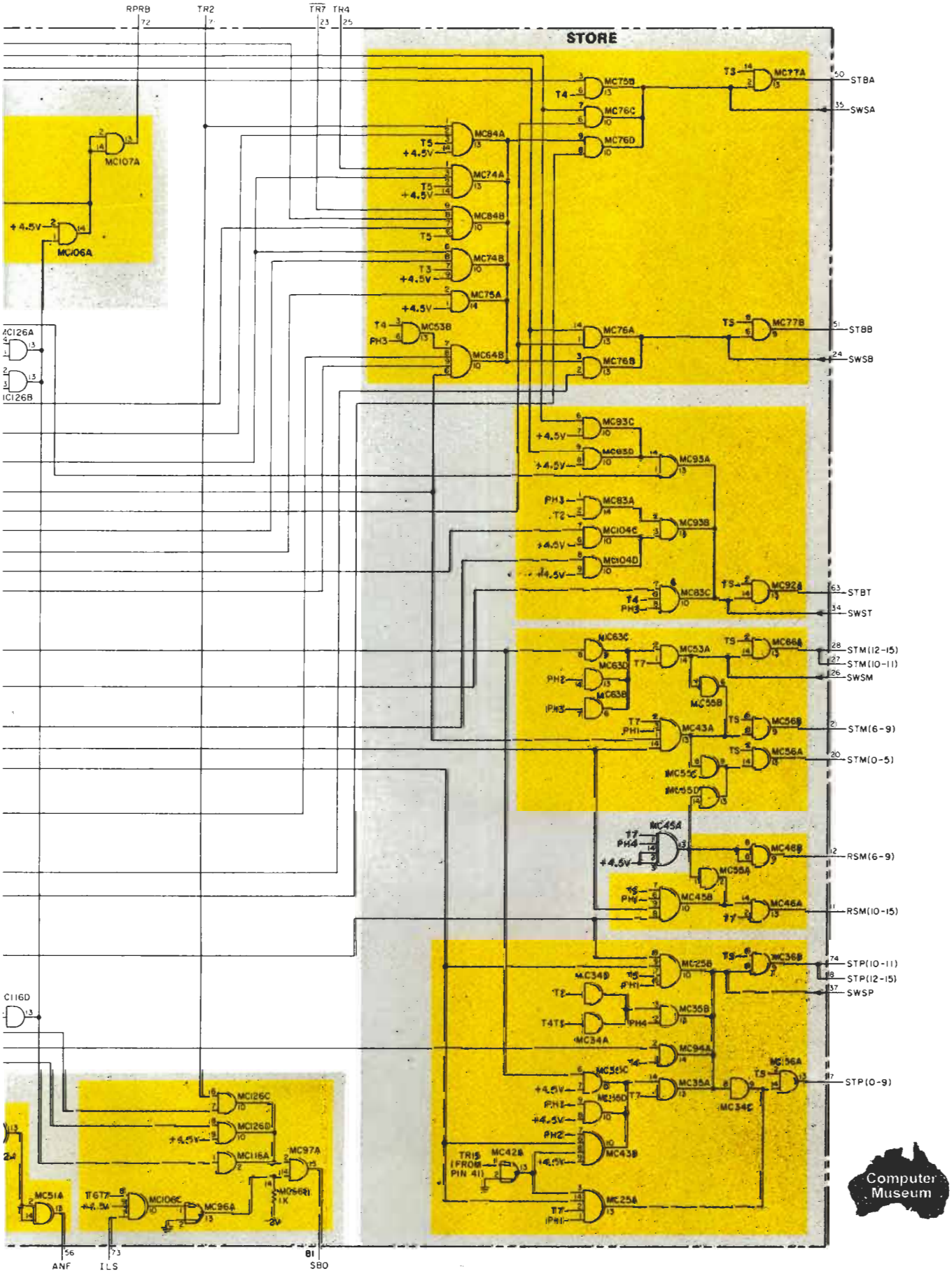
Timing Generator
HP 2116B Computer

FOR TRAINING PURPOSES ONLY

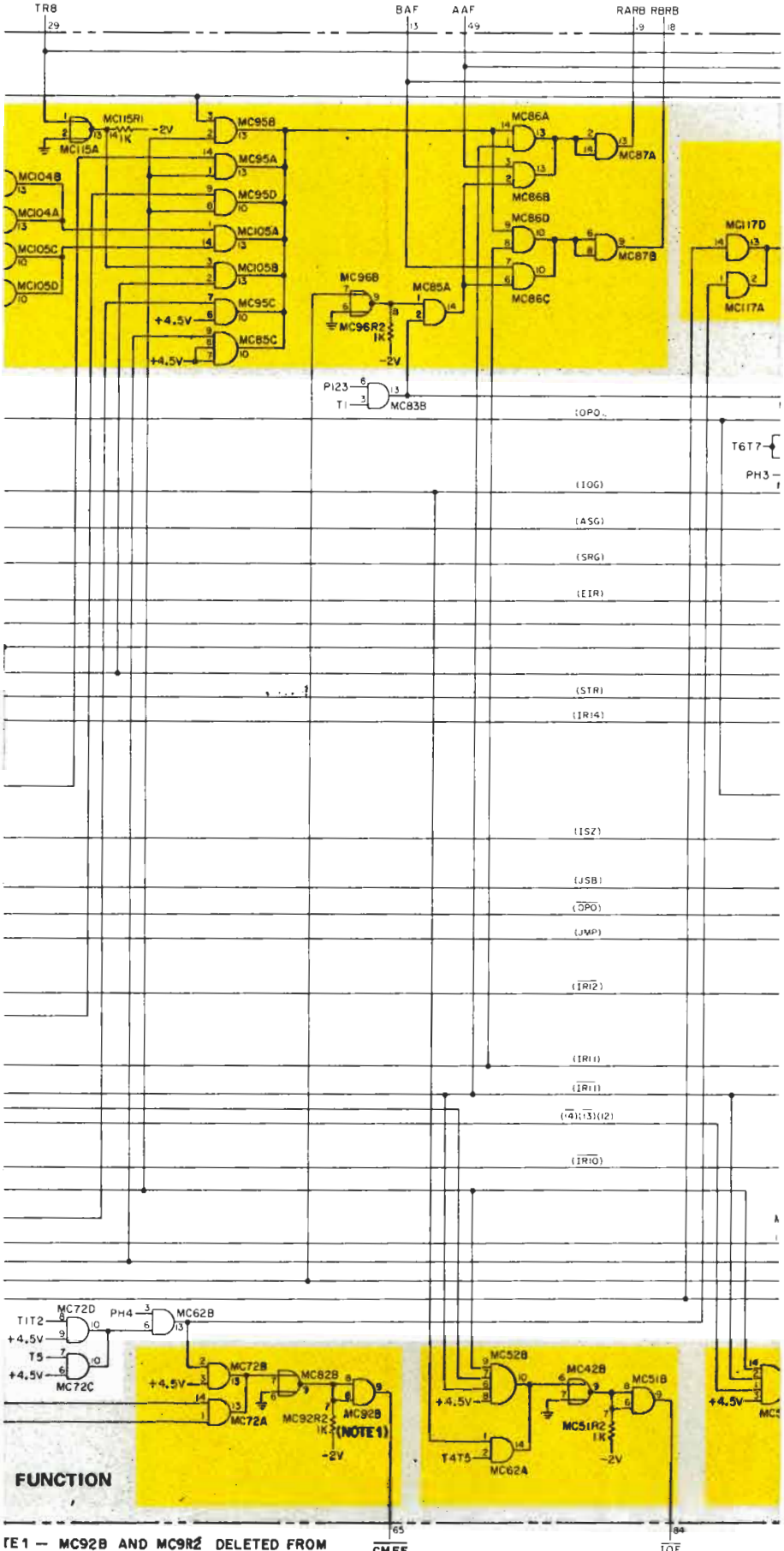


* NOTE: FOR 8K – 16K MEMORY INSTALL W1 ONLY. FOR 24K – 32K MEMORY INSTALL W2 ONLY.

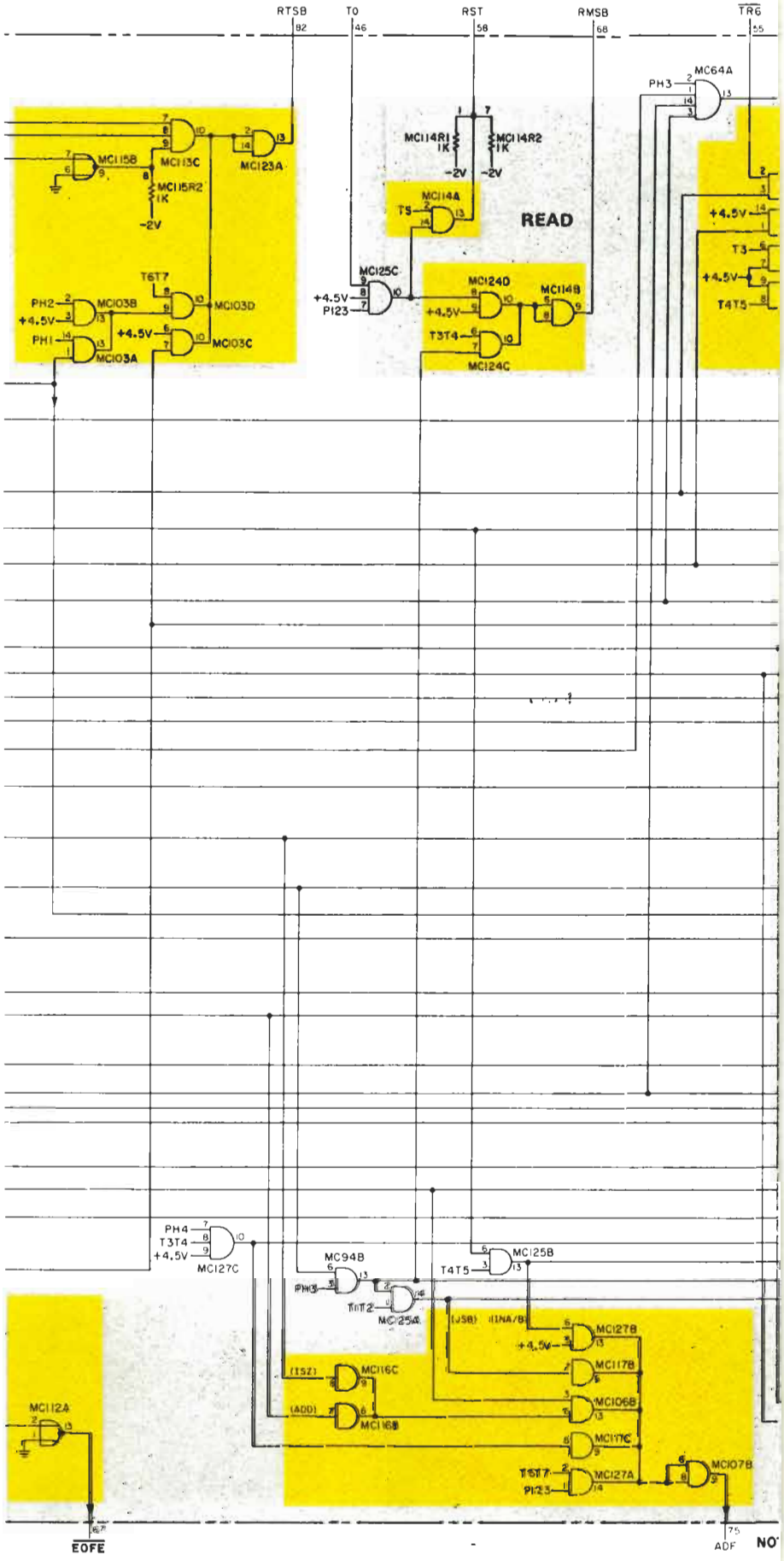

TIMING GENERATOR (02116-6189)
EXT CLOCK
TSA
TS
TO
TOT1
TI
TIT2
TIME PERIOD GENERATOR
10 MHz OSCILLATOR (100 NS Period)
FREQUENCY DIVIDER
200 NS FF
400 NS FF
TOT1 FF
TIT2 FF
RUN FF 1
RUN FF 2
HLS FF
PRS FF
STEP 1
STEP 2
CONTROL SWITCH LOGIC
HIN
PEH
RNS
HLS
SCS
DMS
LMS
LAS
LBS
LADS
POFP
PRS
AAF
BAF
IIR
EIR
POPIO
RPE
SEO
SWSP
SWSM
SWSB
SWSA
SWST
RF1
RF2
TØ

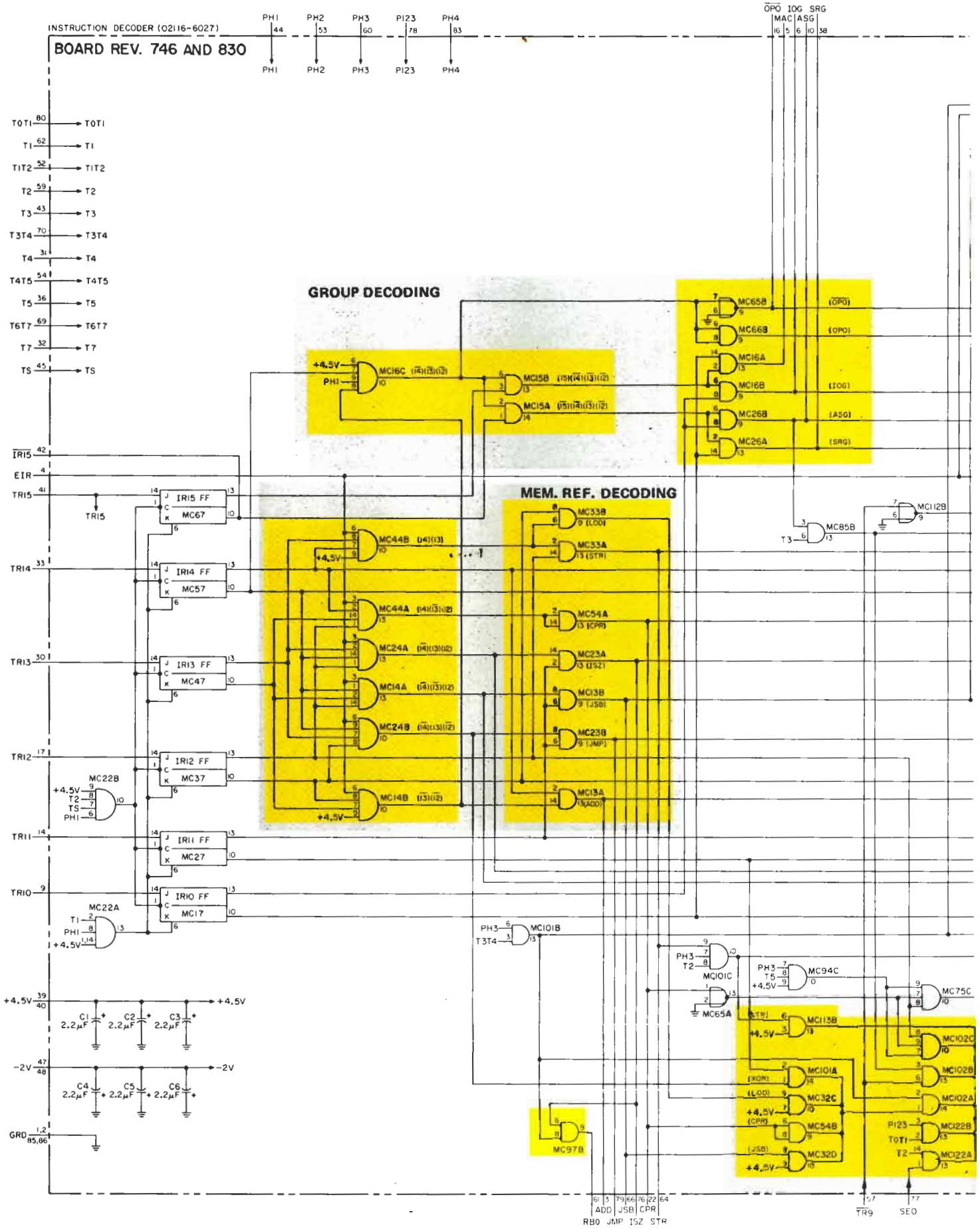


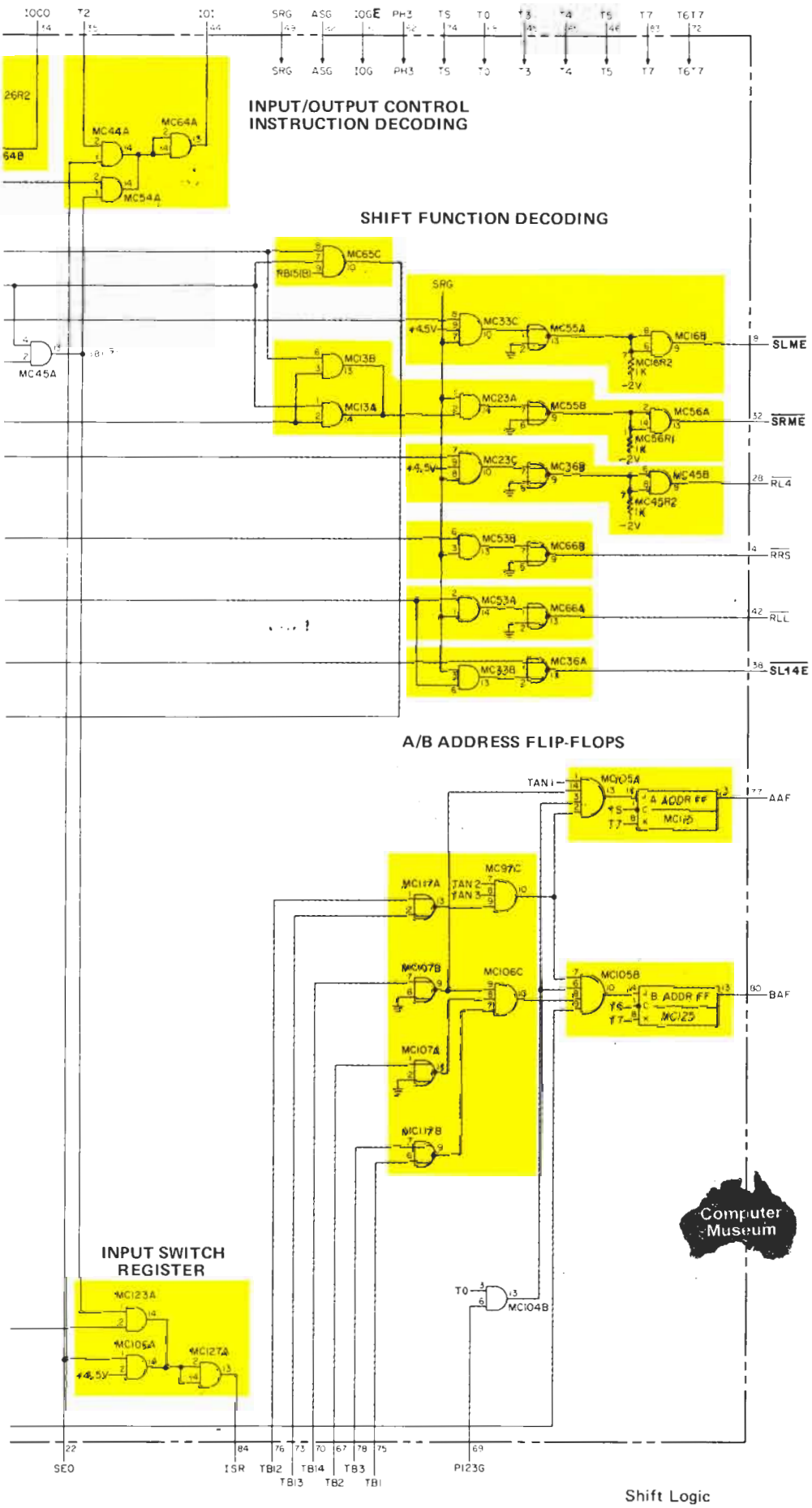
Instruction Decoder
HP 2116B Computer



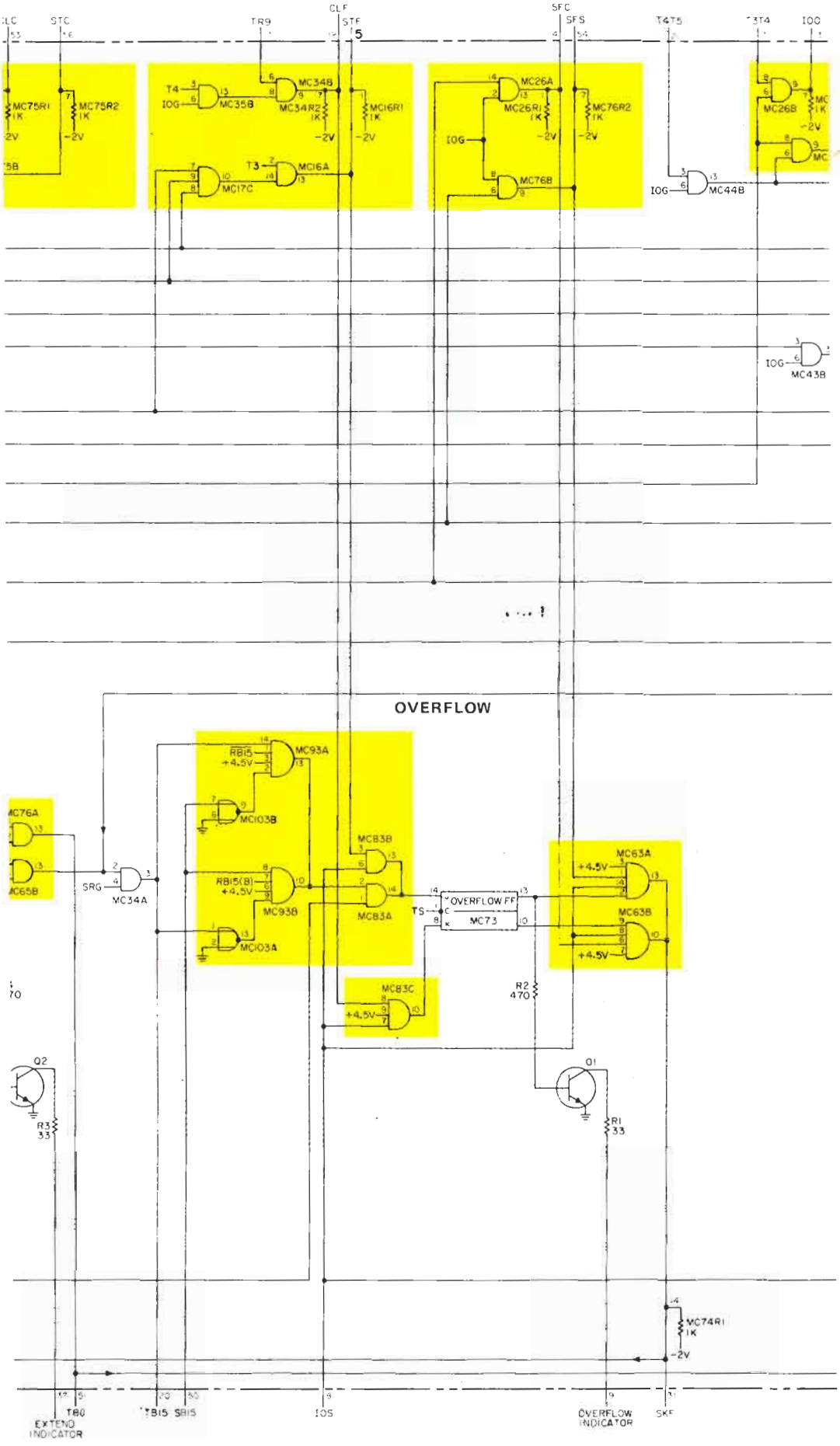
NOTE 1 — MC92B AND MC9R2 DELETED FROM BOARD 830 AND SUBSEQUENT. MC82B PIN 9 CONNECTS DIRECTLY TO PIN 65.

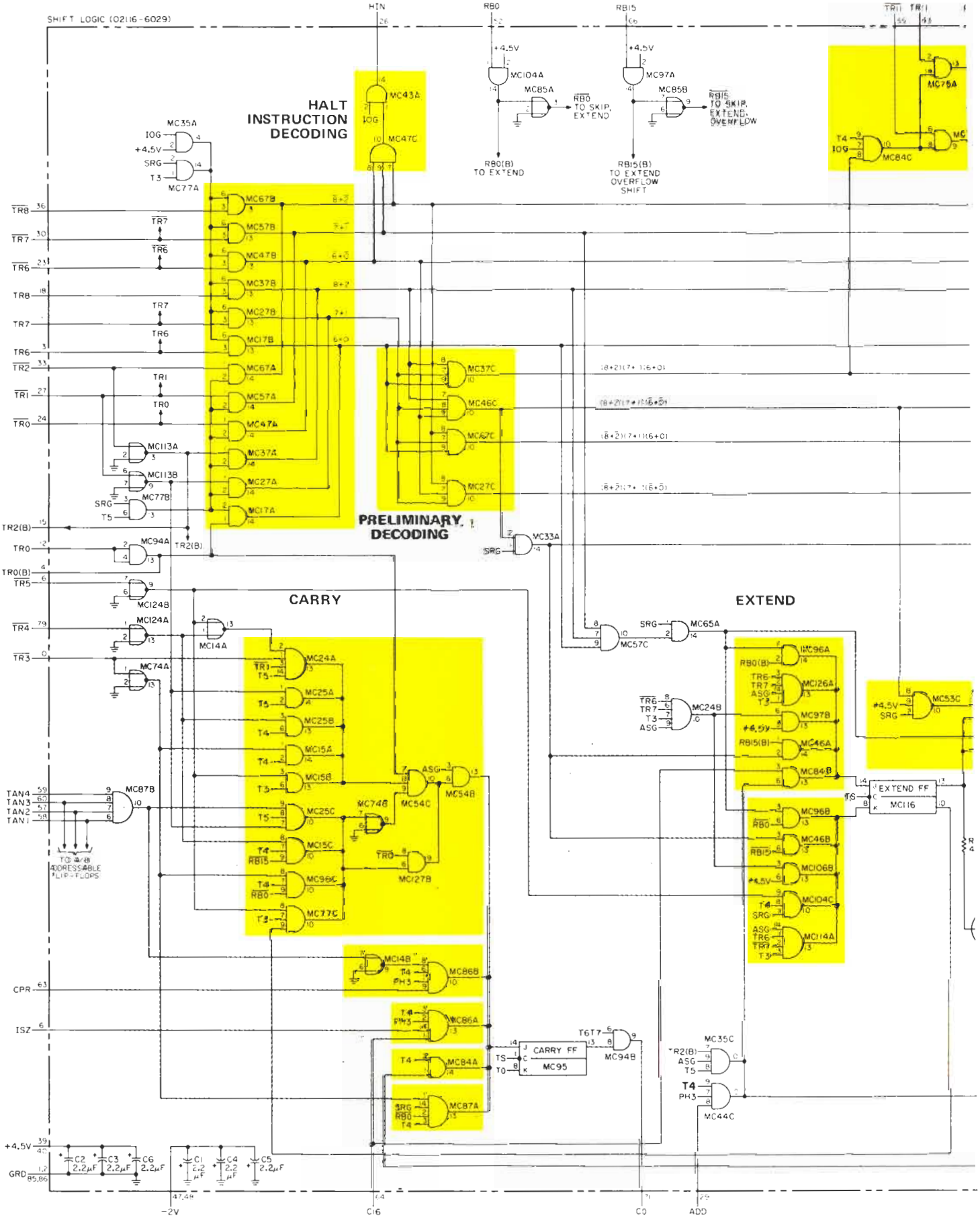

RTSB
82
TO
46
RST
58
RMSB
68
TR6
55
MC64A
PH3
MC114R1
1K
MC114R2
1K
-2V
-2V
MC114A
T5
READ
MC115B
MC113C
MC123A
MC115R2
1K
-2V
T6T7
PH2
MC103B
+4.5V
MC103D
PH1
+4.5V
MC103A
+4.5V
MC103C
MC125C
+4.5V
P123
MC124D
+4.5V
MC114B
T3T4
MC124C
+4.5V
T3
+4.5V
T4T5
PH4
T3T4
+4.5V
MC127C
MC94B
PH3
T1T2
MC125A
MC125B
T4T5
(JSB)
(INA/B)
MC127B
+4.5V
MC117B
MC106B
MC117C
MC116C
(ISZ)
(ADD)
MC116B
MC112A
T5T7
P123
MC127A
MC107B
EOFE
ADF
NO

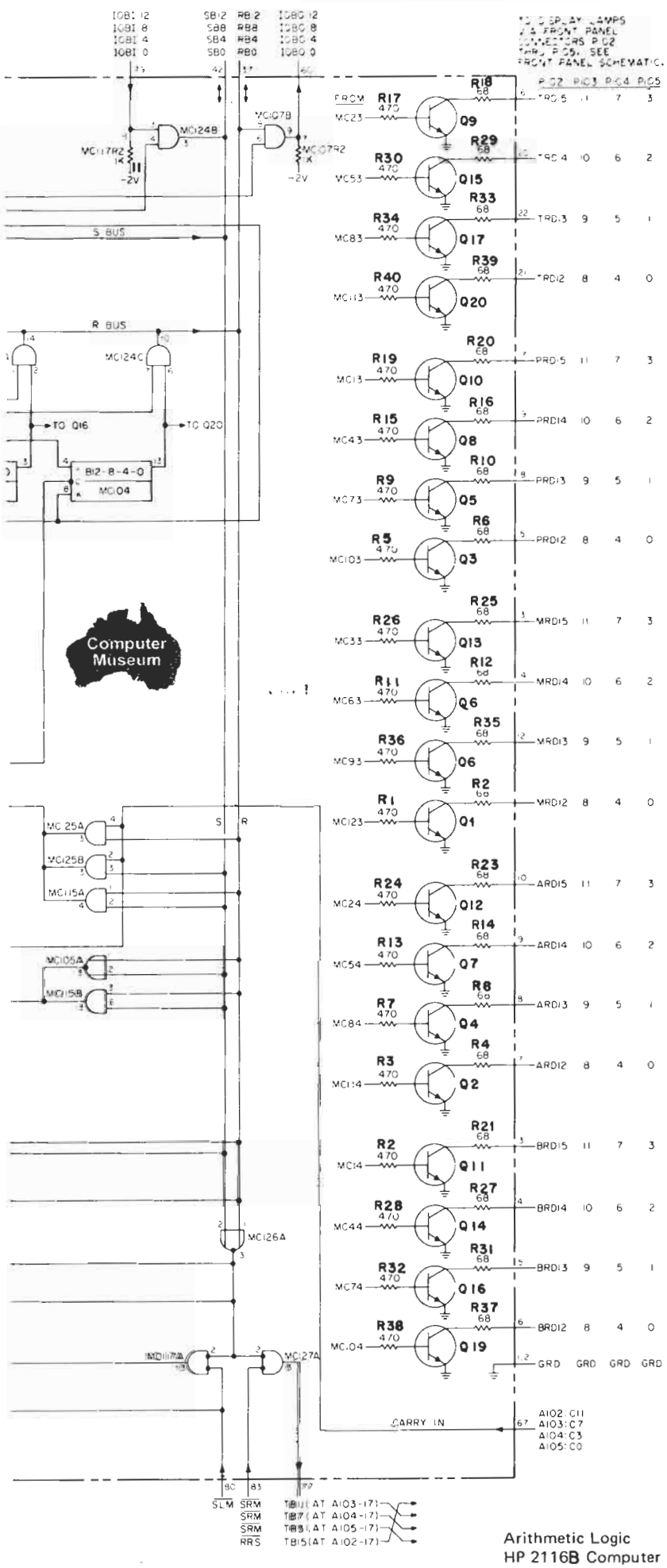

INSTRUCTION DECODER (02116-6027)
BOARD REV. 746 AND 830
PH1 44
PH2 53
PH3 60
PI23 78
PH4 83
OPO IOG SRG
MAC 5 6 ASG 10 38
T0T1 80
T1 62
T1T2 52
T2 59
T3 43
T3T4 70
T4 31
T4T5 54
T5 36
T6T7 69
T7 32
TS 45
GROUP DECODING
MEM. REF. DECODING
IRI5 42
EIR 4
TRI5 41
TRI4 33
TRI3 30
TRI2 17
TRI1 14
TRI0 9
IRI5 FF MC67
IRI4 FF MC57
IRI3 FF MC47
IRI2 FF MC37
IRI1 FF MC27
IRI0 FF MC17
+4.5V 39 40
-2V 47 48
GRD 1,2 85,86
C1 2.2μF
C2 2.2μF
C3 2.2μF
C4 2.2μF
C5 2.2μF
C6 2.2μF
MC16C
MC15B
MC15A
MC65B
MC66B
MC16A
MC16B
MC26B
MC26A
MC44B
MC44A
MC24A
MC14A
MC24B
MC14B
MC22B
MC22A
MC33B
MC33A
MC54A
MC23A
MC13B
MC23B
MC13A
MC85B
MC112B
MC101B
MC101C
MC65A
MC94C
MC75C
MC113B
MC101A
MC32C
MC54B
MC32D
MC102C
MC102B
MC102A
MC122B
MC122A
MC97B
RB0 JMP ISZ STR
ADD JSB CPR
TR9
SEO



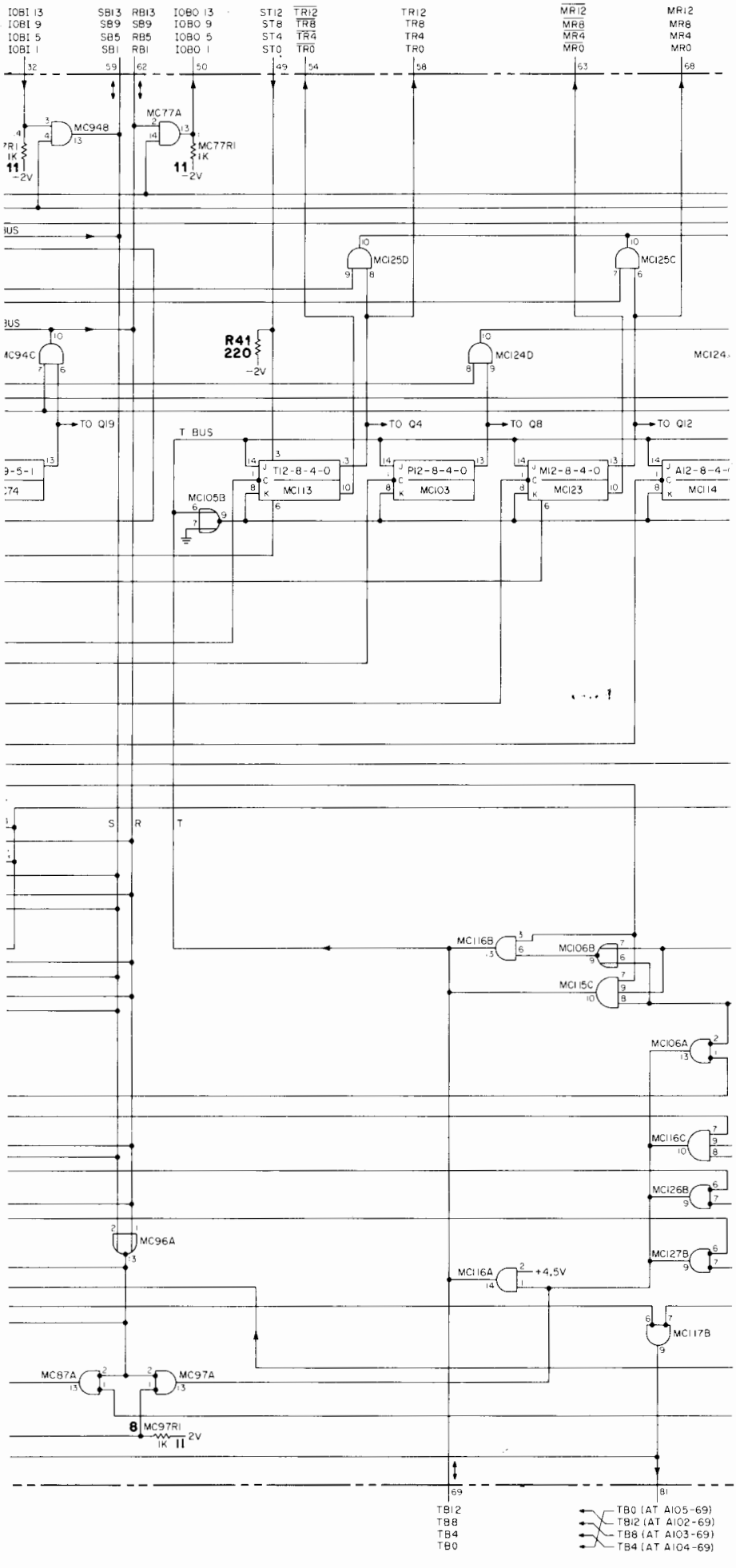
Shift Logic
HP 2116B Computer

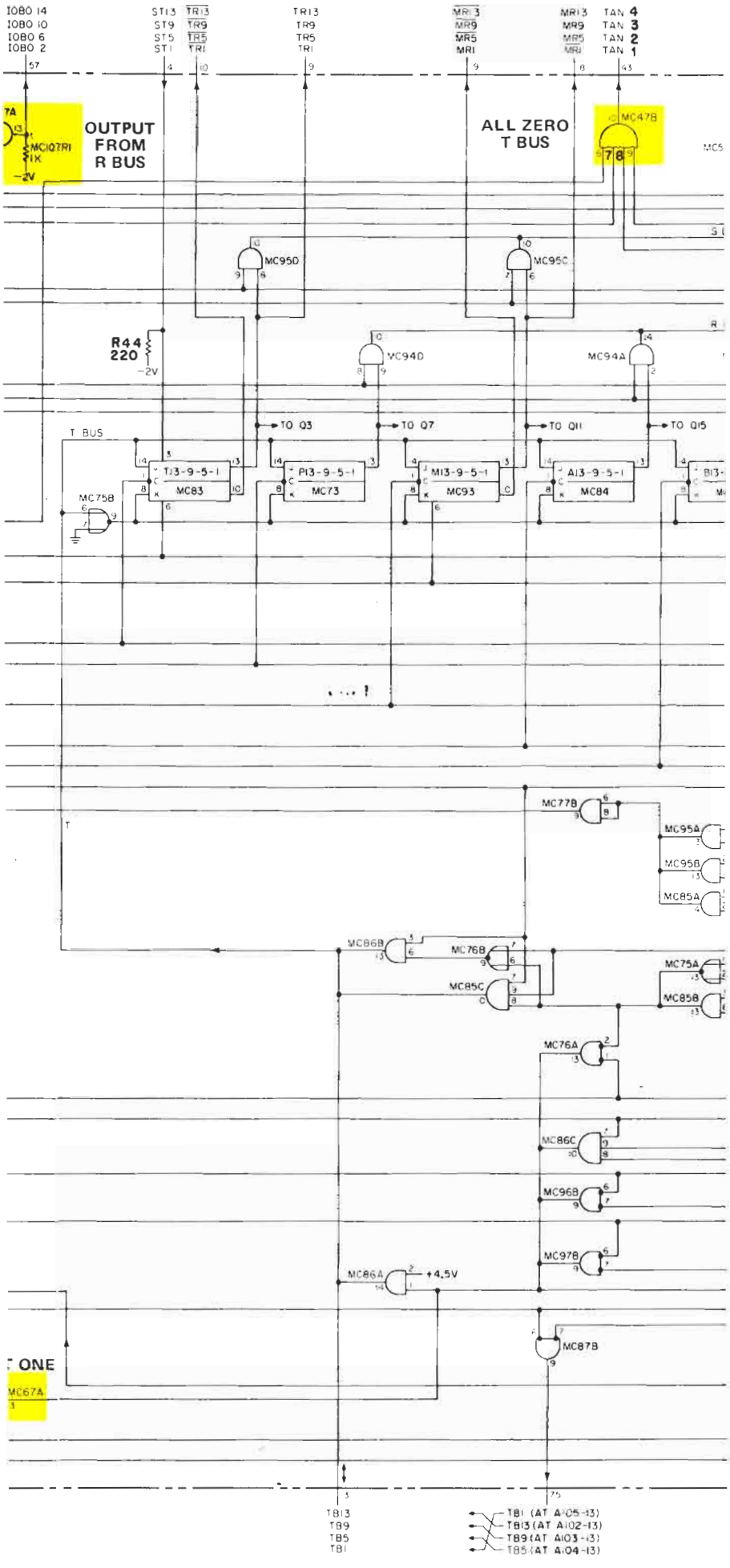

CLF
SFC
STC
TR9
STF
SFS
T4T5
T3T4
IOO
MC75R1 1K
MC75R2 1K
-2V
T4
IOG
MC35B
MC34B
MC34R2 1K
MC16R1 1K
T3
MC17C
MC16A
MC26A
MC26R1 1K
MC76R2 1K
MC76B
MC26B
MC44B
MC43B
OVERFLOW
RB15 +4.5V
MC93A
MC103B
MC83B
MC76A
MC65B
SRG
MC34A
RB15(B) +4.5V
MC93B
MC103A
MC83A
OVERFLOW FF
TS
MC73
MC63A
MC63B
+4.5V
MC83C
R2 470
Q2
Q1
R3 33
R1 33
MC74R1 1K
TB0
EXTEND INDICATOR
TB15
SRIS
IOS
OVERFLOW INDICATOR
SKF

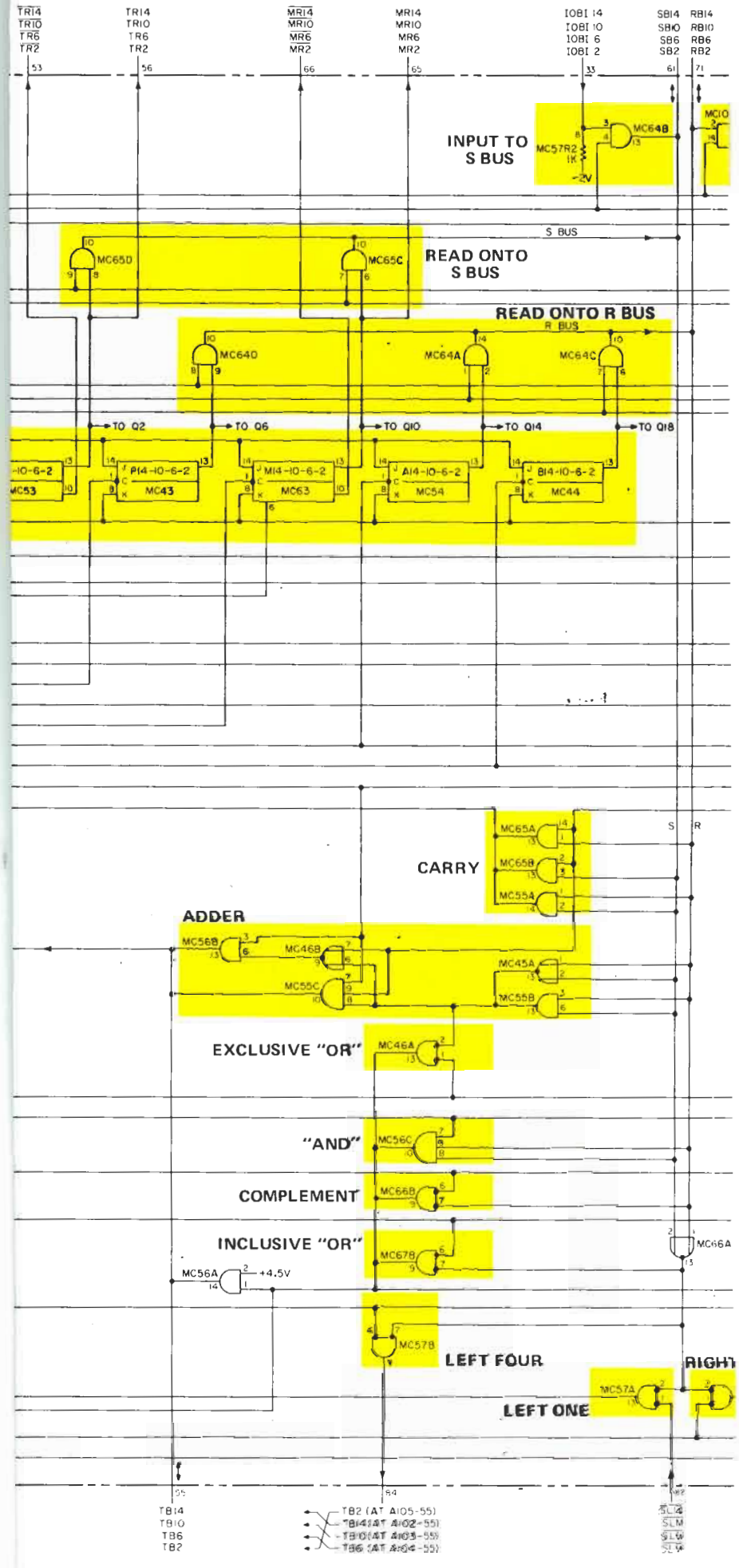

SHIFT LOGIC (02116-6029)
HALT INSTRUCTION DECODING
PRELIMINARY DECODING
CARRY
EXTEND
HIN
RB0
RB15
RB0 TO SKIP, EXTEND
RB15 TO SKIP, EXTEND, OVERFLOW
RB0(B) TO EXTEND
RB15(B) TO EXTEND OVERFLOW SHIFT
CARRY FF MC95
EXTEND FF MC116
TO ADDRESSABLE FLIP-FLOPS
CPR
ISZ
-2V
C16
CO
ADD

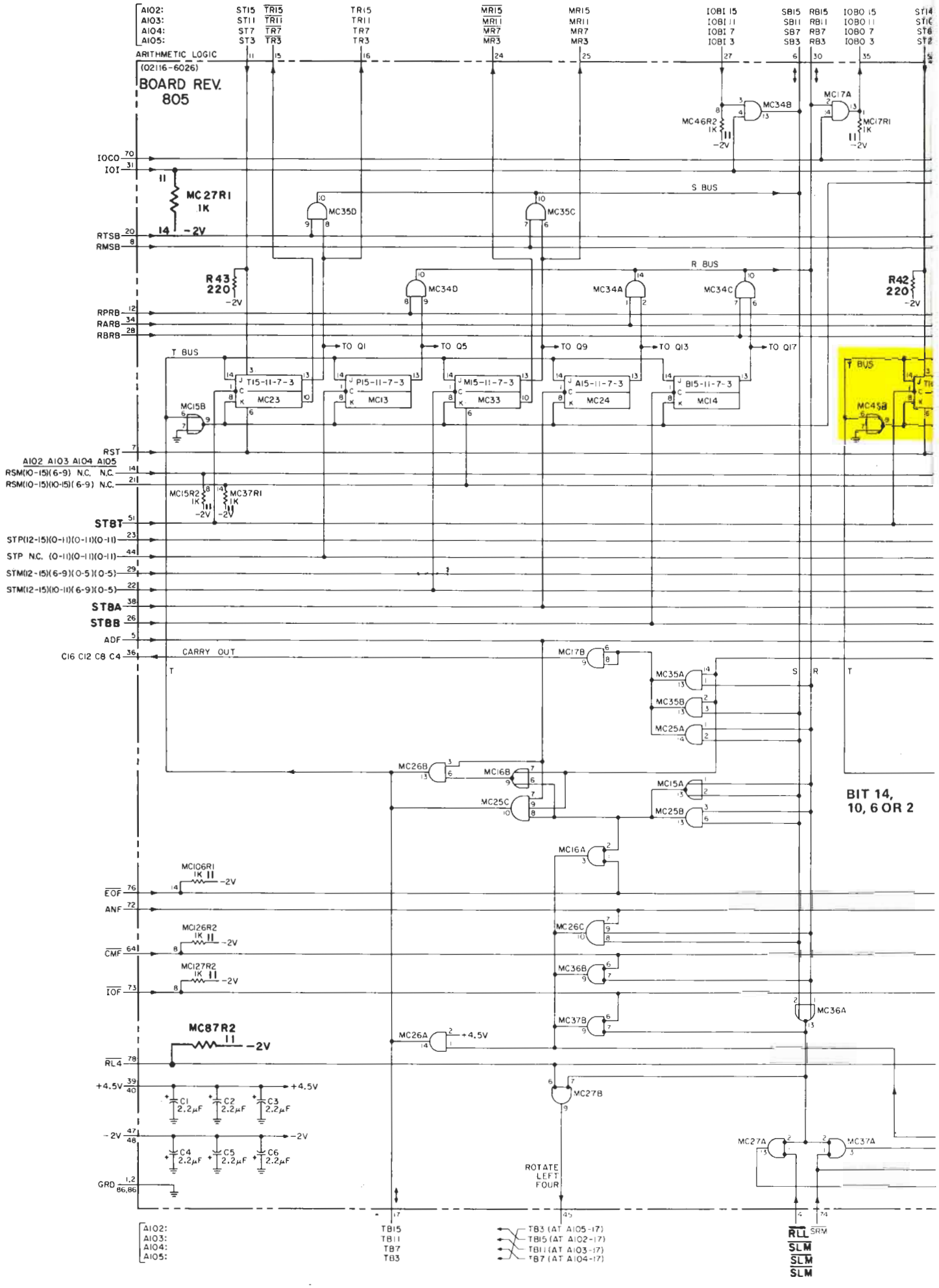


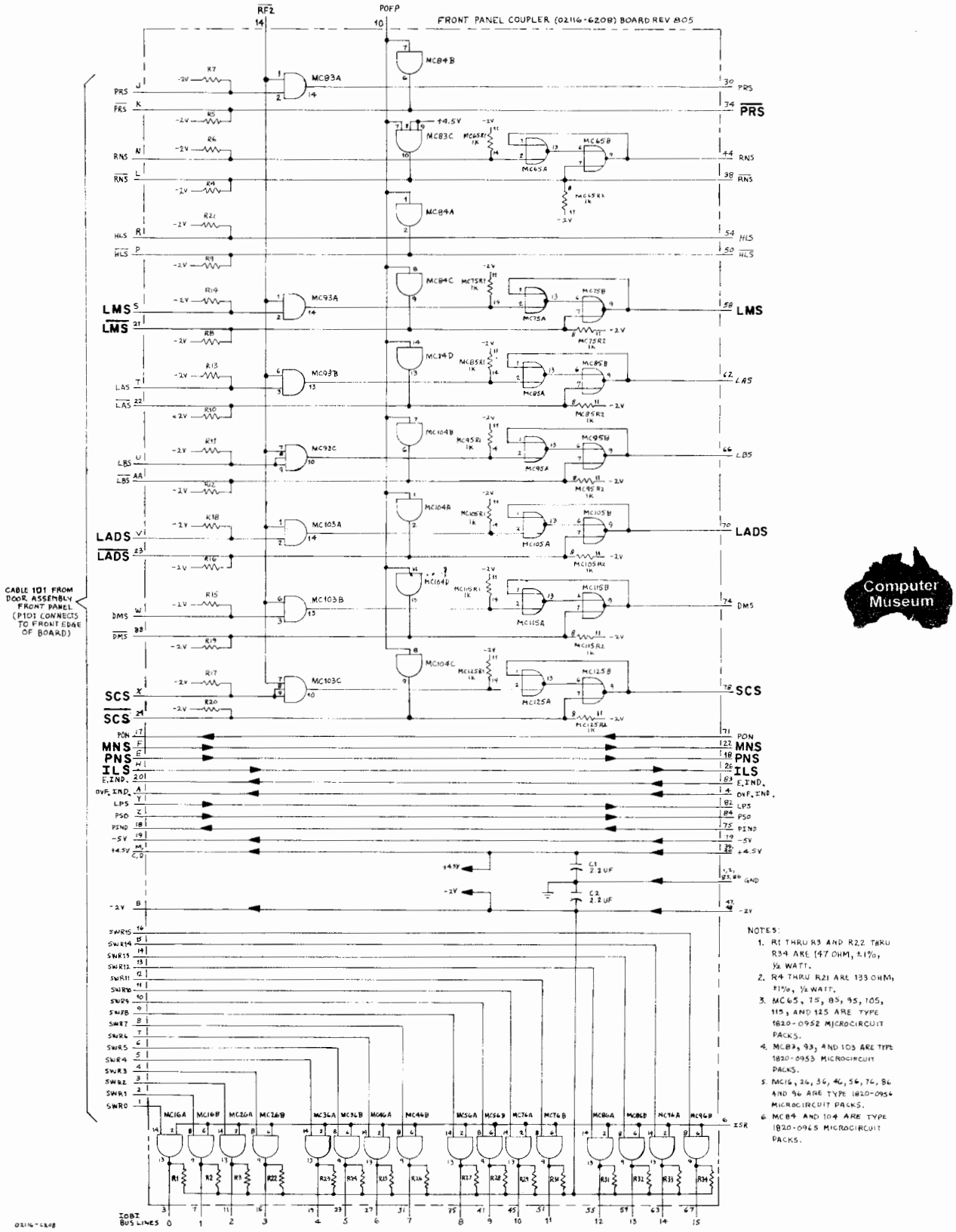
Arithmetic Logic
HP 2116B Computer


IOBI 13
IOBI 9
IOBI 5
IOBI 1
SBI3
SB9
SB5
SBI
RBI3
RB9
RB5
RBI
IOBO 13
IOBO 9
IOBO 5
IOBO 1
ST12
ST8
ST4
ST0
TR12
TR8
TR4
TR0
MR12
MR8
MR4
MR0
MC948
MC77A
MC77RI
1K
11
−2V
MCI25D
MCI25C
MCI24D
R41
220
TO Q19
TO Q4
TO Q8
TO Q12
T BUS
TI2-8-4-0
PI2-8-4-0
MI2-8-4-0
MCI13
MCI03
MCI23
MCI14
MCI05B
S
R
T
MCI16B
MCI06B
MCI15C
MCI06A
MCI16C
MCI26B
MCI27B
MC96A
MCI16A
+4,5V
MCI17B
MC87A
MC97A
MC97RI
2V
TB12
TB8
TB4
TB0
TB0 (AT A105-69)
TB12 (AT A102-69)
TB8 (AT A103-69)
TB4 (AT A104-69)


IOBO 14
IOBO 10
IOBO 6
IOBO 2
ST13 TR13
ST9 TR9
ST5 TR5
ST1 TR1
TR13
TR9
TR5
TR1
MR13
MR9
MR5
MR1
TAN 4
TAN 3
TAN 2
TAN 1
OUTPUT FROM R BUS
MC107R1 1K
-2V
ALL ZERO T BUS
MC47B
MC95D
MC95C
R44 220
-2V
MC94D
MC94A
TO Q3
TO Q7
TO Q11
TO Q15
T BUS
TJ3-9-5-1 MC83
PI3-9-5-1 MC73
MI3-9-5-1 MC93
AI3-9-5-1 MC84
MC75B
MC77B
MC95A
MC95B
MC85A
MC86B
MC76B
MC85C
MC75A
MC85B
MC76A
MC86C
MC96B
MC97B
MC86A
+4.5V
MC87B
ONE
MC67A
TB13
TB9
TB5
TB1
TB1 (AT A105-13)
TB13 (AT A102-13)
TB9 (AT A103-13)
TB5 (AT A104-13)

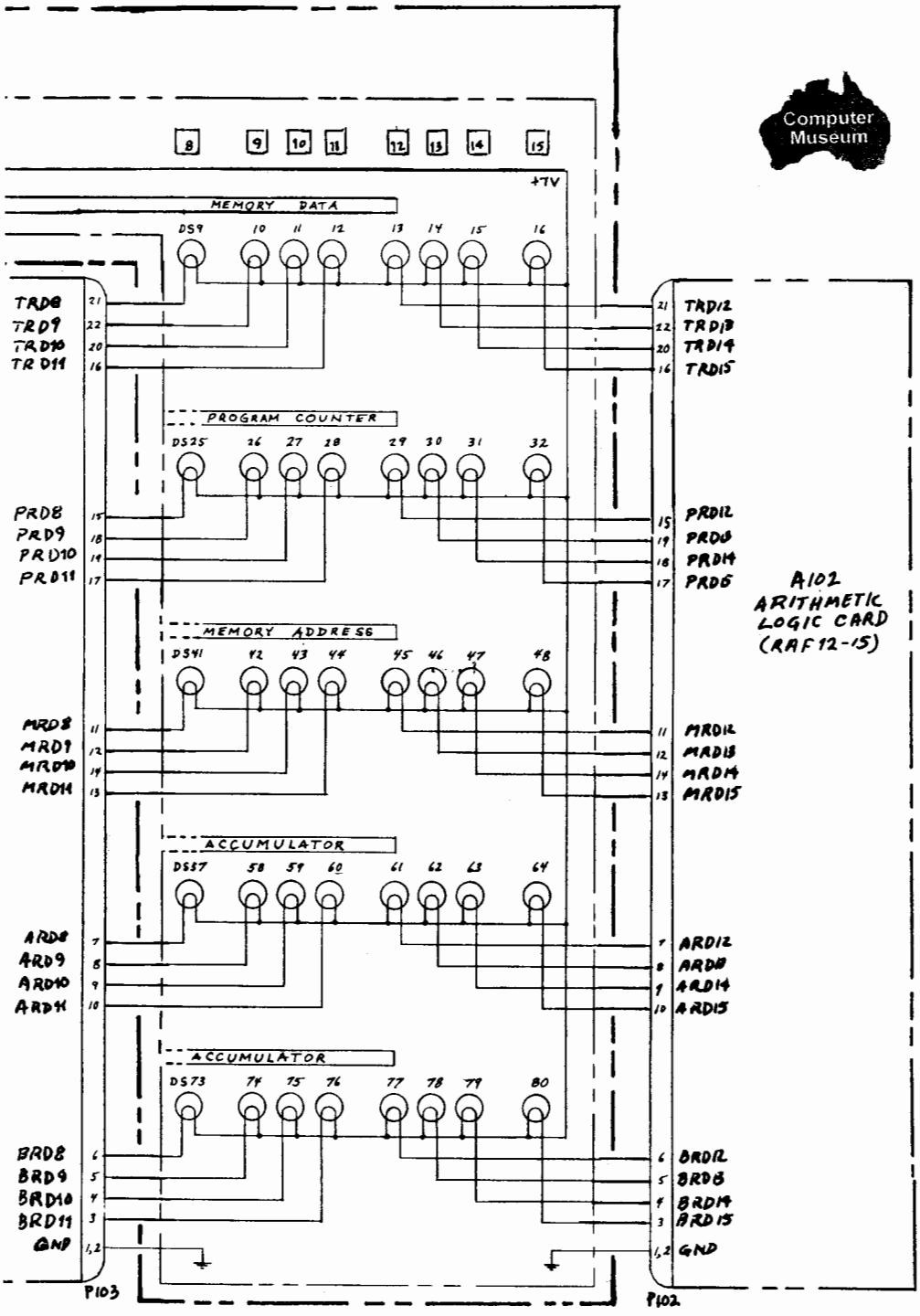

INPUT TO S BUS
READ ONTO S BUS
READ ONTO R BUS
S BUS
R BUS
TO Q2
TO Q6
TO Q10
TO Q14
TO Q18
CARRY
ADDER
EXCLUSIVE "OR"
"AND"
COMPLEMENT
INCLUSIVE "OR"
LEFT FOUR
LEFT ONE
RIGHT
+4.5V


BOARD REV. 805
ARITHMETIC LOGIC (02116-6026)
MC27R1 1K
MC35D
MC35C
MC34B
MC34D
MC34A
MC34C
R43 220
R42 220
MC34B
MC17A
MC17R1 1K
MC46R2 1K
S BUS
R BUS
T BUS
TO Q1
TO Q5
TO Q9
TO Q13
TO Q17
T15-11-7-3 MC23
P15-11-7-3 MC13
M15-11-7-3 MC33
A15-11-7-3 MC24
B15-11-7-3 MC14
MC15B
MC45B
MC15R2 1K
MC37R1 1K
CARRY OUT
MC17B
MC35A
MC35B
MC25A
MC26B
MC16B
MC25C
MC15A
MC25B
MC16A
MC10R1 1K
MC26R2 1K
MC27R2 1K
MC26C
MC36B
MC37B
MC36A
MC87R2
MC26A
+4.5V
MC27B
C1 2.2μF
C2 2.2μF
C3 2.2μF
C4 2.2μF
C5 2.2μF
C6 2.2μF
MC27A
MC37A
ROTATE LEFT FOUR
BIT 14, 10, 6 OR 2
RST
A102 A103 A104 A105
RSM(10-15)(6-9) N.C.
RSM(10-15)(10-15)(6-9) N.C.
ST8T
STP(12-15)(0-11)(0-11)(0-11)
STP N.C. (0-11)(0-11)(0-11)
STM(12-15)(6-9)(0-5)(0-5)
STM(12-15)(10-11)(6-9)(0-5)
ST8A
ST8B
ADF
CI6 CI2 C8 C4
EOF
ANF
CMF
IOF
RL4
GRD
IOCO
IOI
RTSB
RMSB
RPRB
RARB
RBRB
TB15
TB11
TB7
TB3
TB3 (AT A105-17)
TB15 (AT A102-17)
TB11 (AT A103-17)
TB7 (AT A104-17)
RLL
SRM
SLM
SLM
SLM

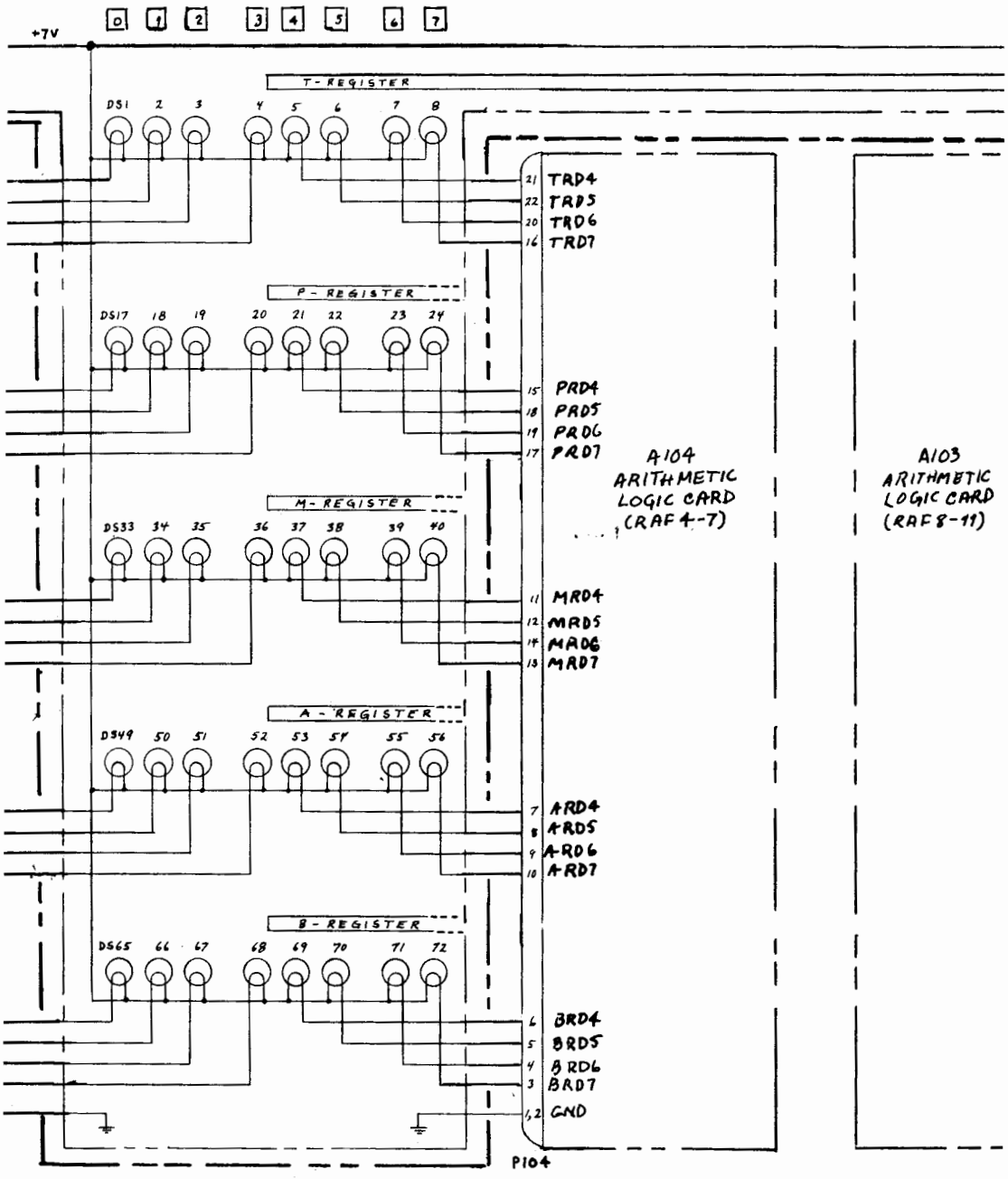


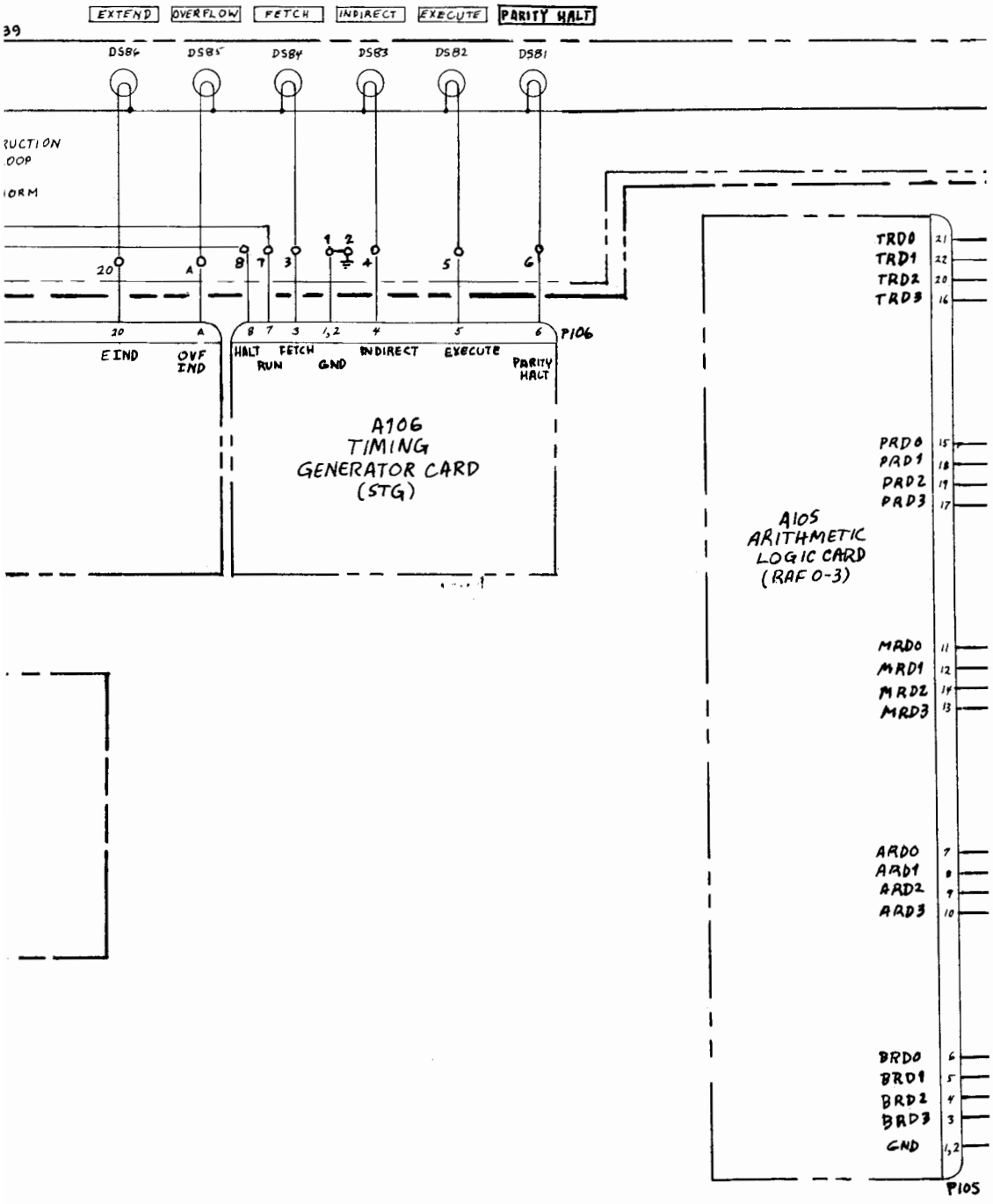
Front Panel Coupler Card (02116-6208), Logic Diagram

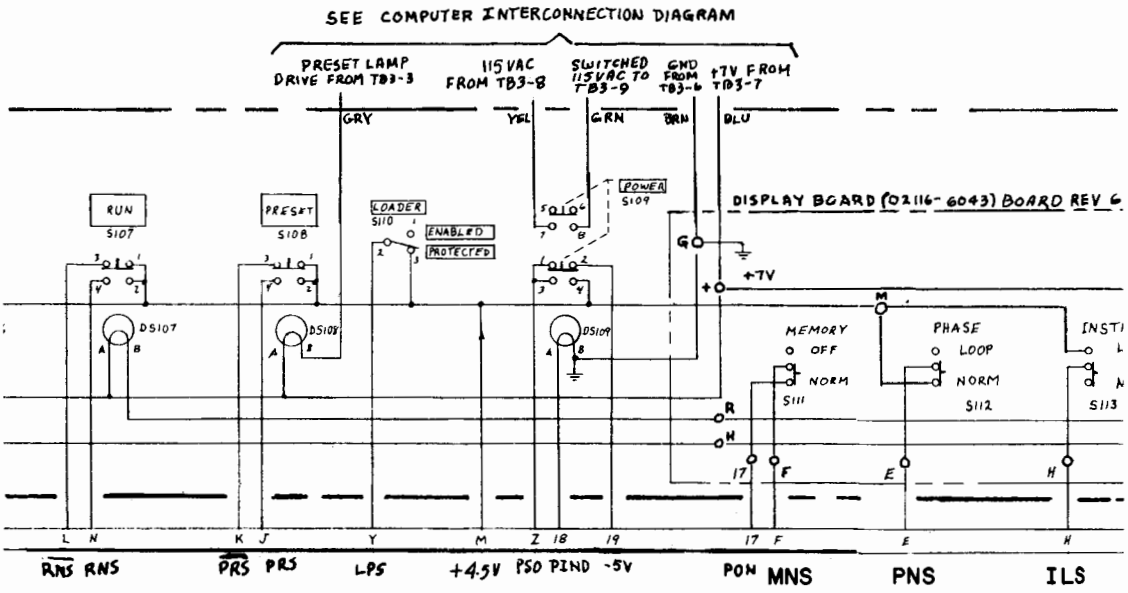
FOR TRAINING PURPOSES ONLY
HP 2116B



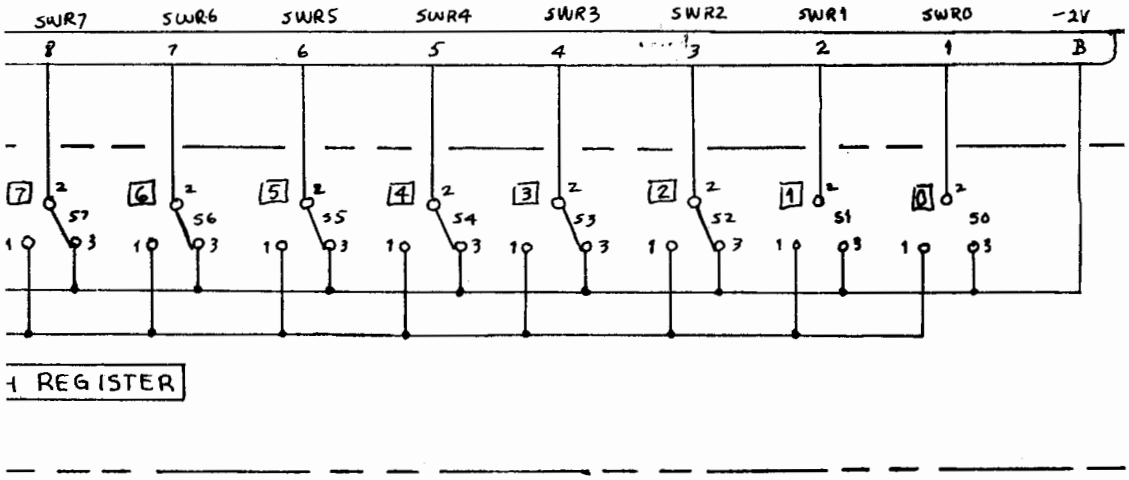
Door Assembly (02116-6287), Schematic and Interconnection Diagram


+7V
0 1 2 3 4 5 6 7
T-REGISTER
DS1 2 3 4 5 6 7 8
21 TRD4
22 TRD5
20 TRD6
16 TRD7
P-REGISTER
DS17 18 19 20 21 22 23 24
15 PRD4
18 PRD5
19 PRD6
17 PRD7
M-REGISTER
DS33 34 35 36 37 38 39 40
11 MRD4
12 MRD5
14 MRD6
13 MRD7
A-REGISTER
DS49 50 51 52 53 54 55 56
7 ARD4
8 ARD5
9 ARD6
10 ARD7
B-REGISTER
DS65 66 67 68 69 70 71 72
6 BRD4
5 BRD5
4 BRD6
3 BRD7
1,2 GND
P104
A104
ARITHMETIC
LOGIC CARD
(RAF 4-7)
A103
ARITHMETIC
LOGIC CARD
(RAF 8-11)


EXTEND
OVERFLOW
FETCH
INDIRECT
EXECUTE
PARITY HALT
39
DS86
DS85
DS84
DS83
DS82
DS81
RUCTION
OOP
IORM
20
A
8
7
3
1 2
4
5
6
20
A
8 7 3 1,2 4 5 6
P106
EIND
OVF IND
HALT RUN
FETCH
GND
INDIRECT
EXECUTE
PARITY HALT
A106
TIMING
GENERATOR CARD
(STG)
A105
ARITHMETIC
LOGIC CARD
(RAF 0-3)
TRD0 21
TRD1 22
TRD2 20
TRD3 16
PRD0 15
PRD1 18
PRD2 19
PRD3 17
MRD0 11
MRD1 12
MRD2 14
MRD3 13
ARD0 7
ARD1 8
ARD2 9
ARD3 10
BRD0 6
BRD1 5
BRD2 4
BRD3 3
GND 1,2
P105

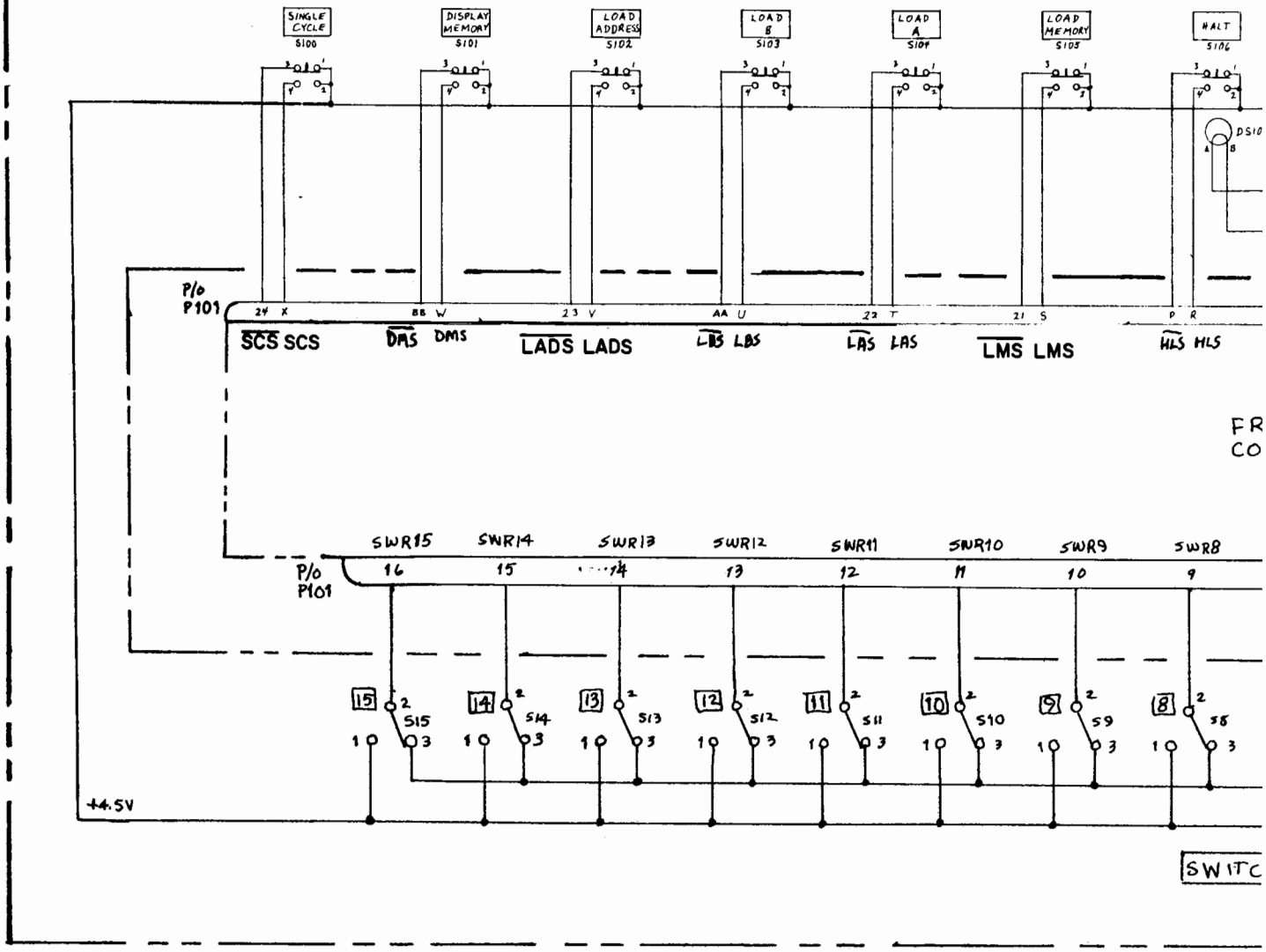


A101
ONT PANEL
UPLER CARD
(FPC)

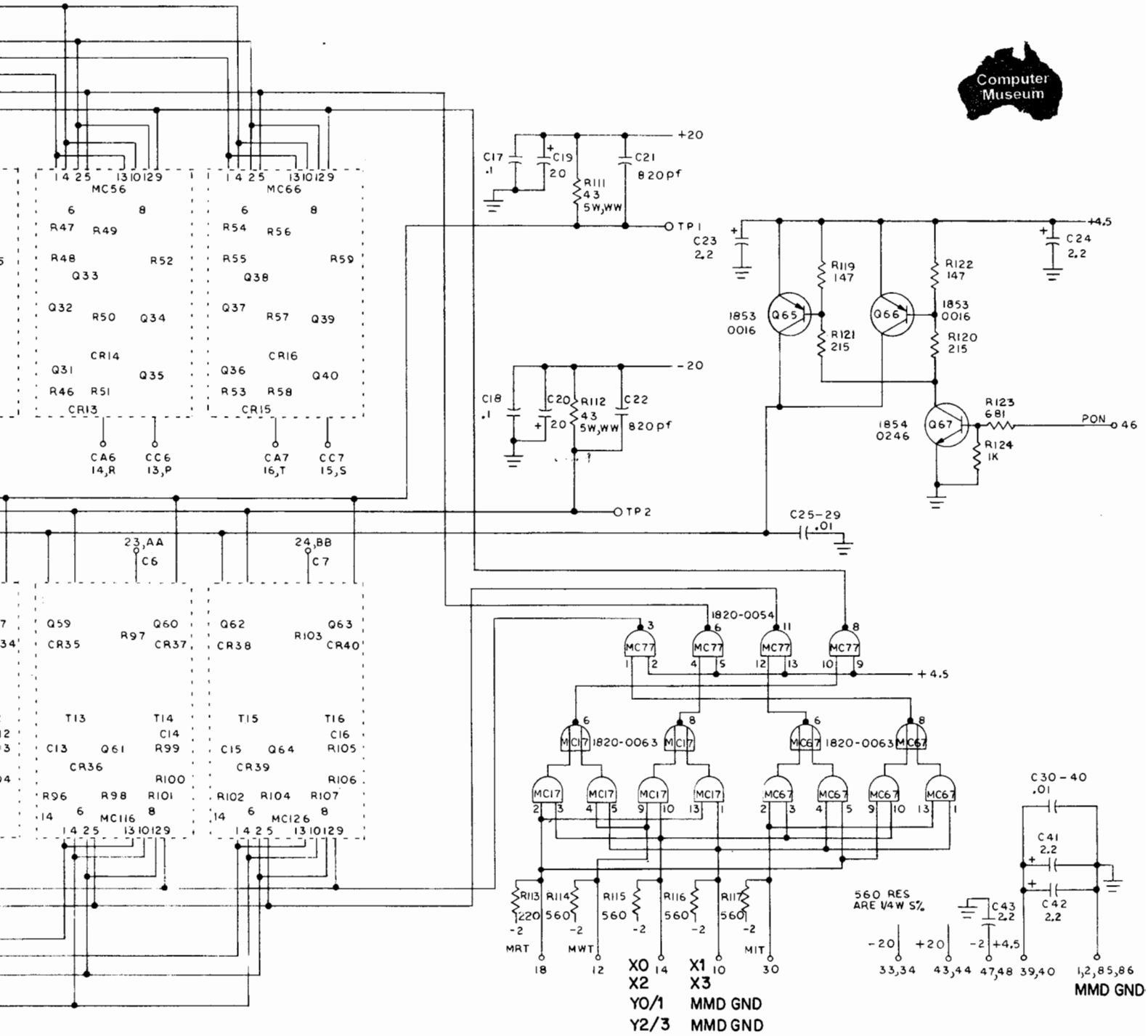


REGISTER

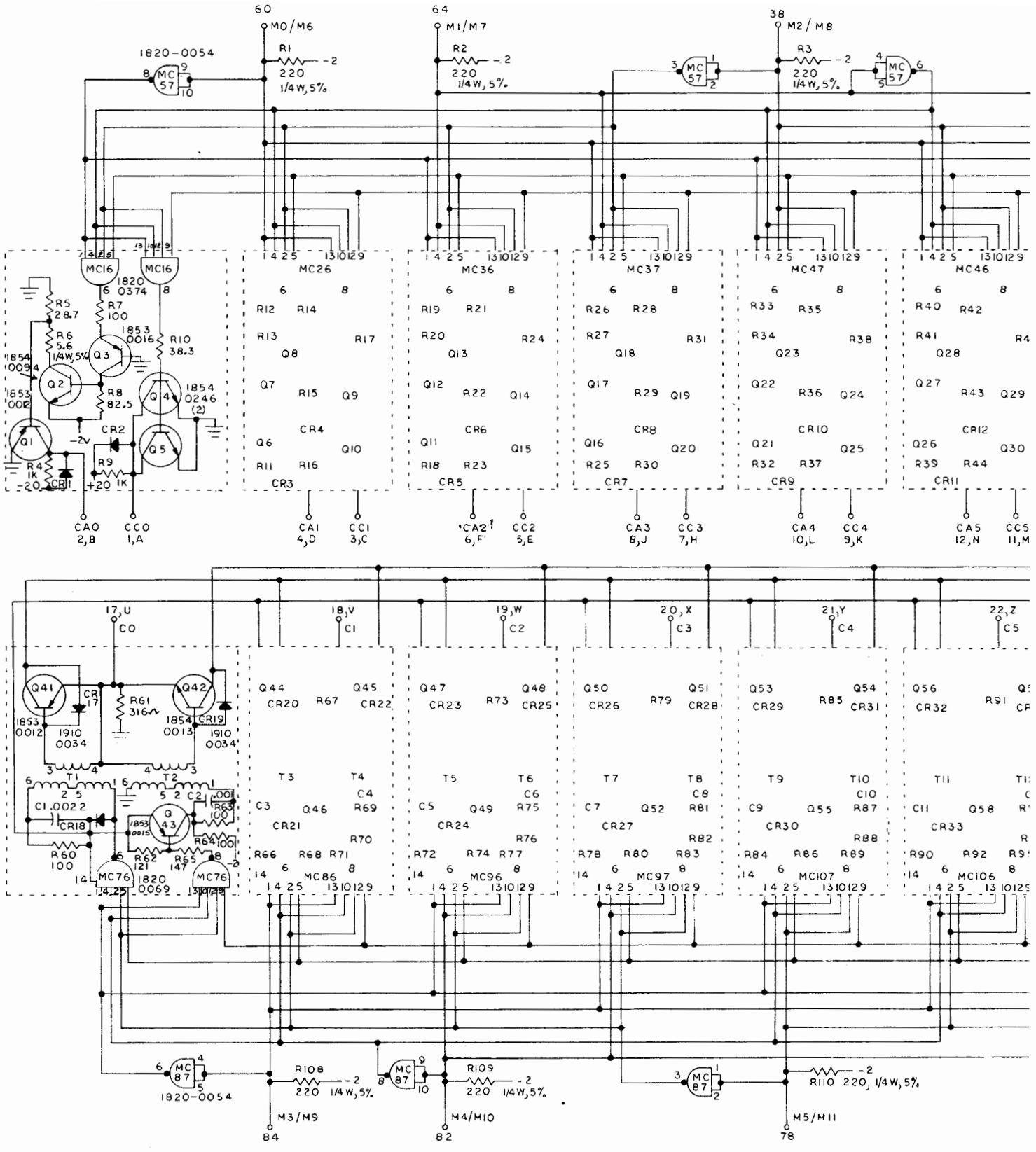
DOOR ASSEMBLY 02116-6287



02116-9150B
02116-6208
02116-6043A

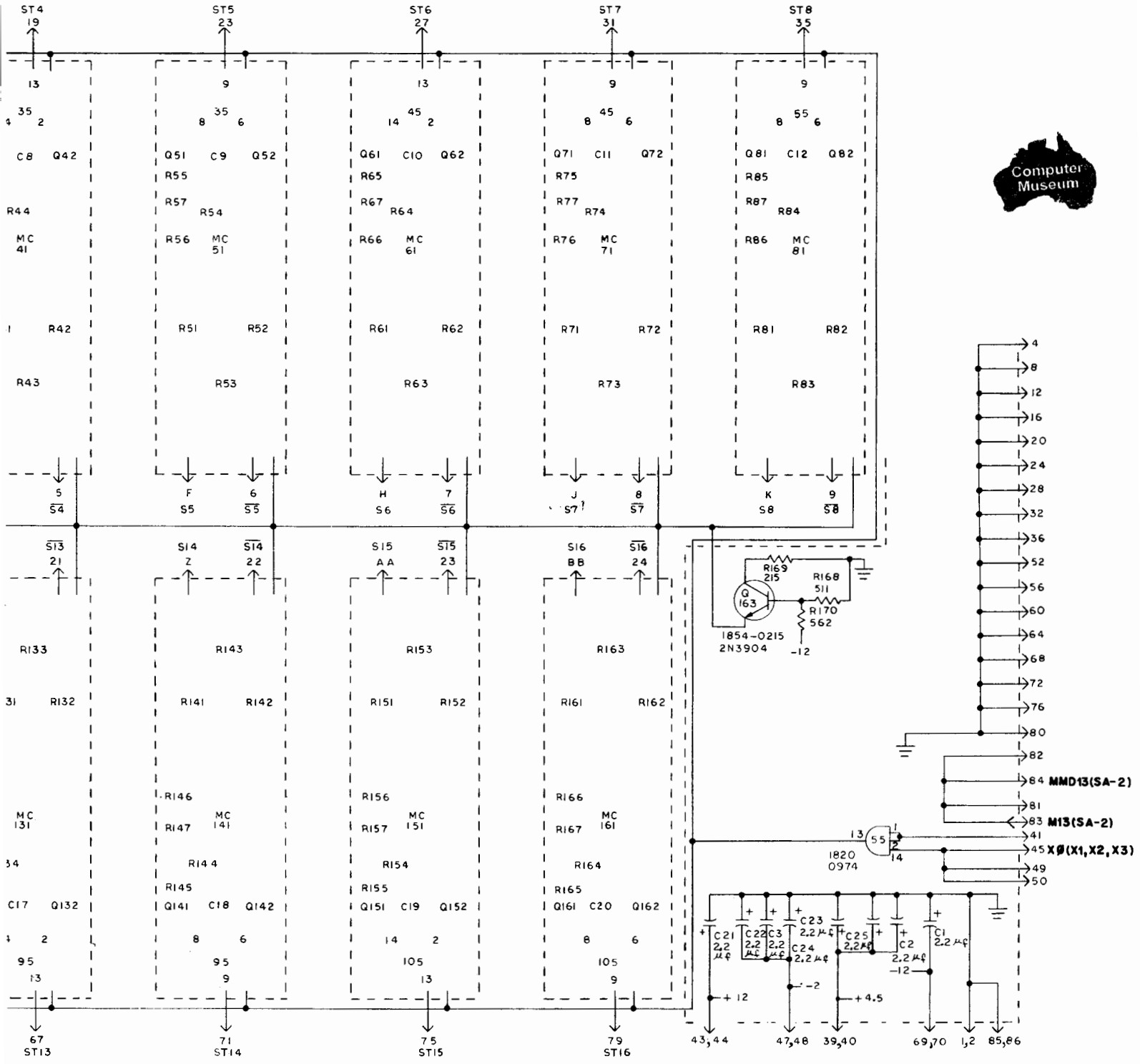


Driver Switch Card (02116-6266), Logic Diagram



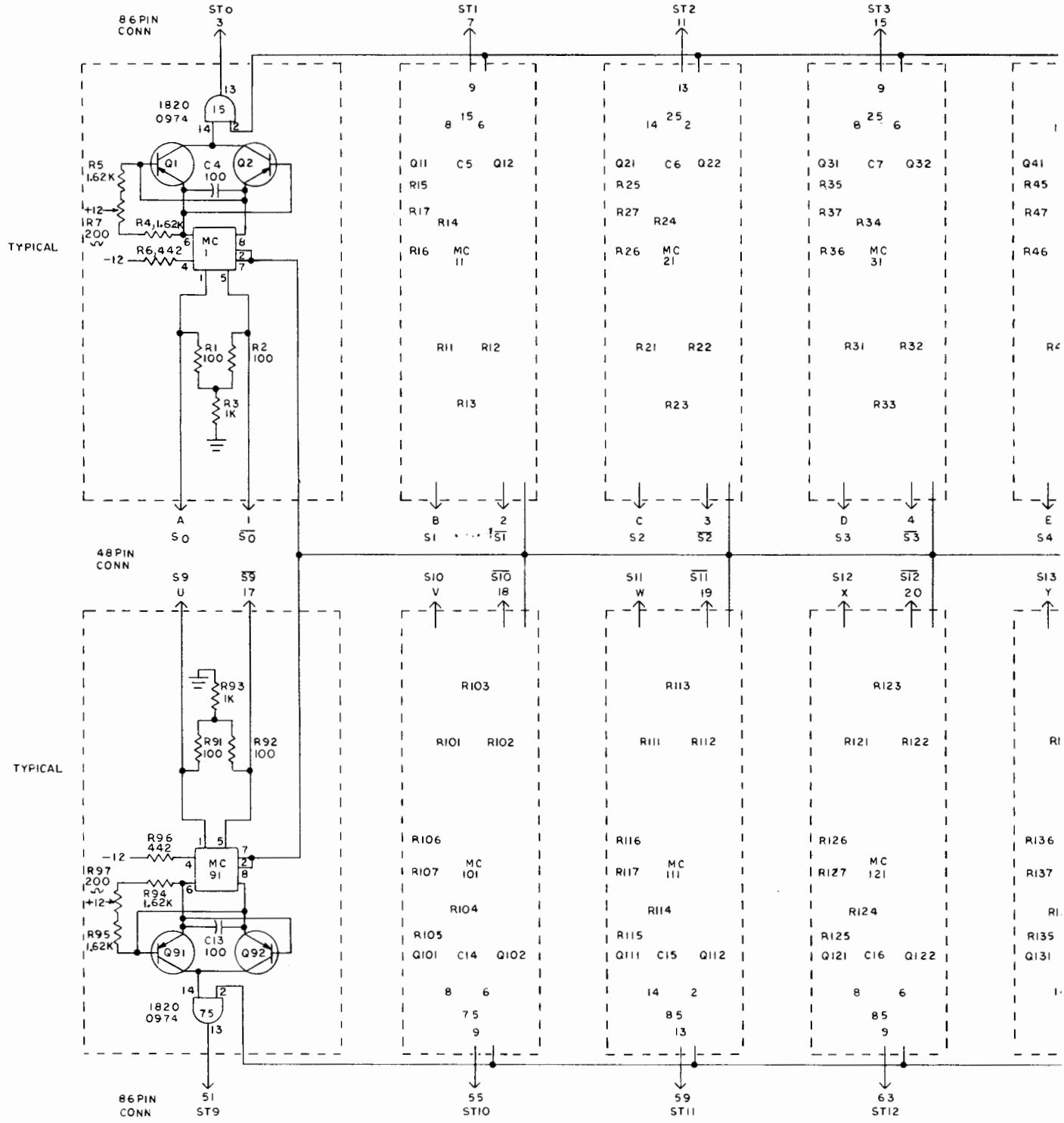
NOTE

UNLESS OTHERWISE NOTED
ALL DIODES 1901-0040
ALL TRANSFORMERS 662849
CAPACITANCE IN MICRO FARADS
RESISTORS 1/8W 1%
BOARD REV B17



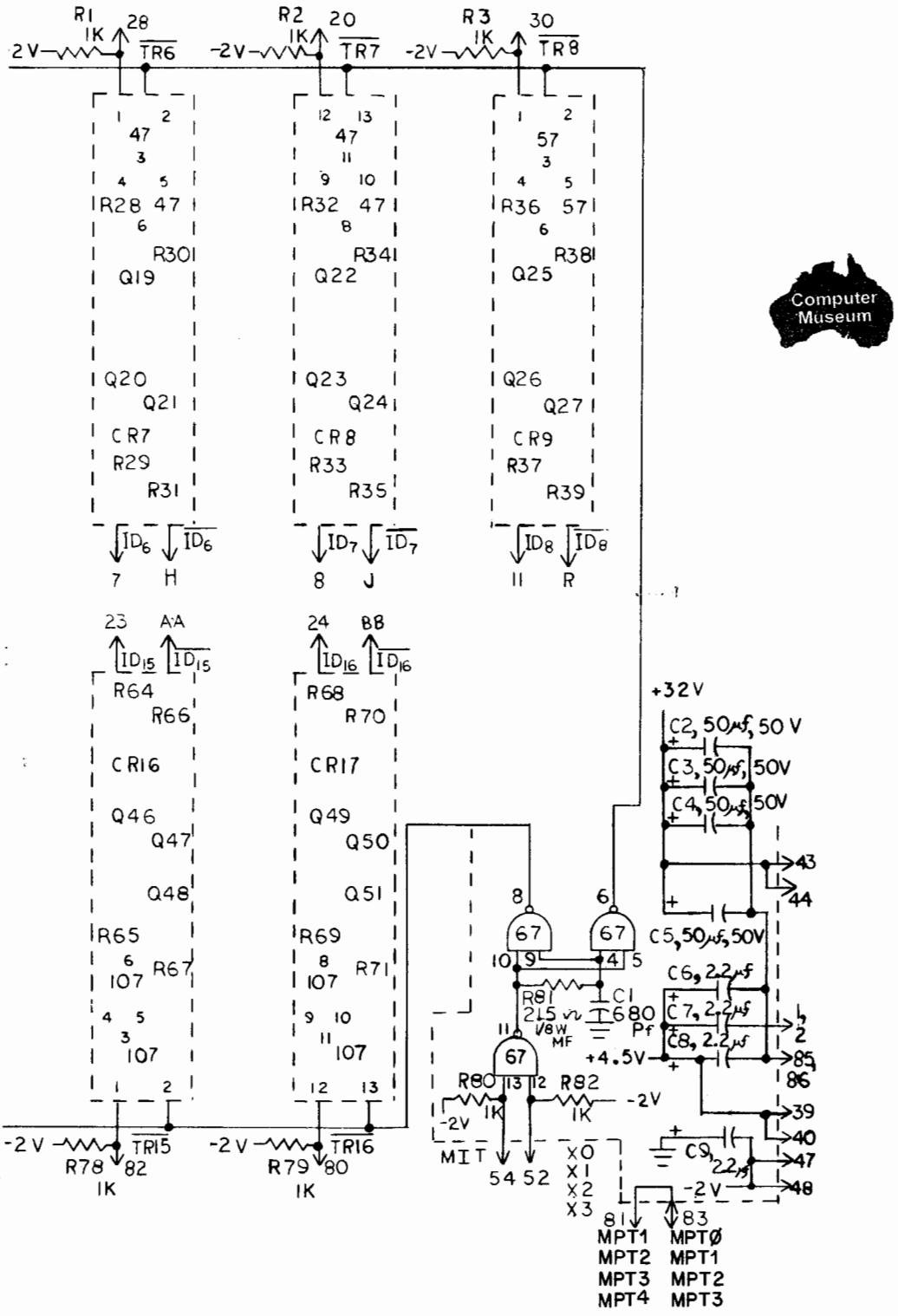
Sense Amplifier Card (02115-6001), Logic Diagram

FOR TRAINING PURPOSES ONLY
HP 2116B



NOTE
UNLESS OTHERWISE NOTED
ALL INTEGRATED CKTS ARE 1820-0306
ALL TRANSISTORS ARE 1853-0036
ALL RESISTORS 1/8W 1% MF
BOARD REV. 744

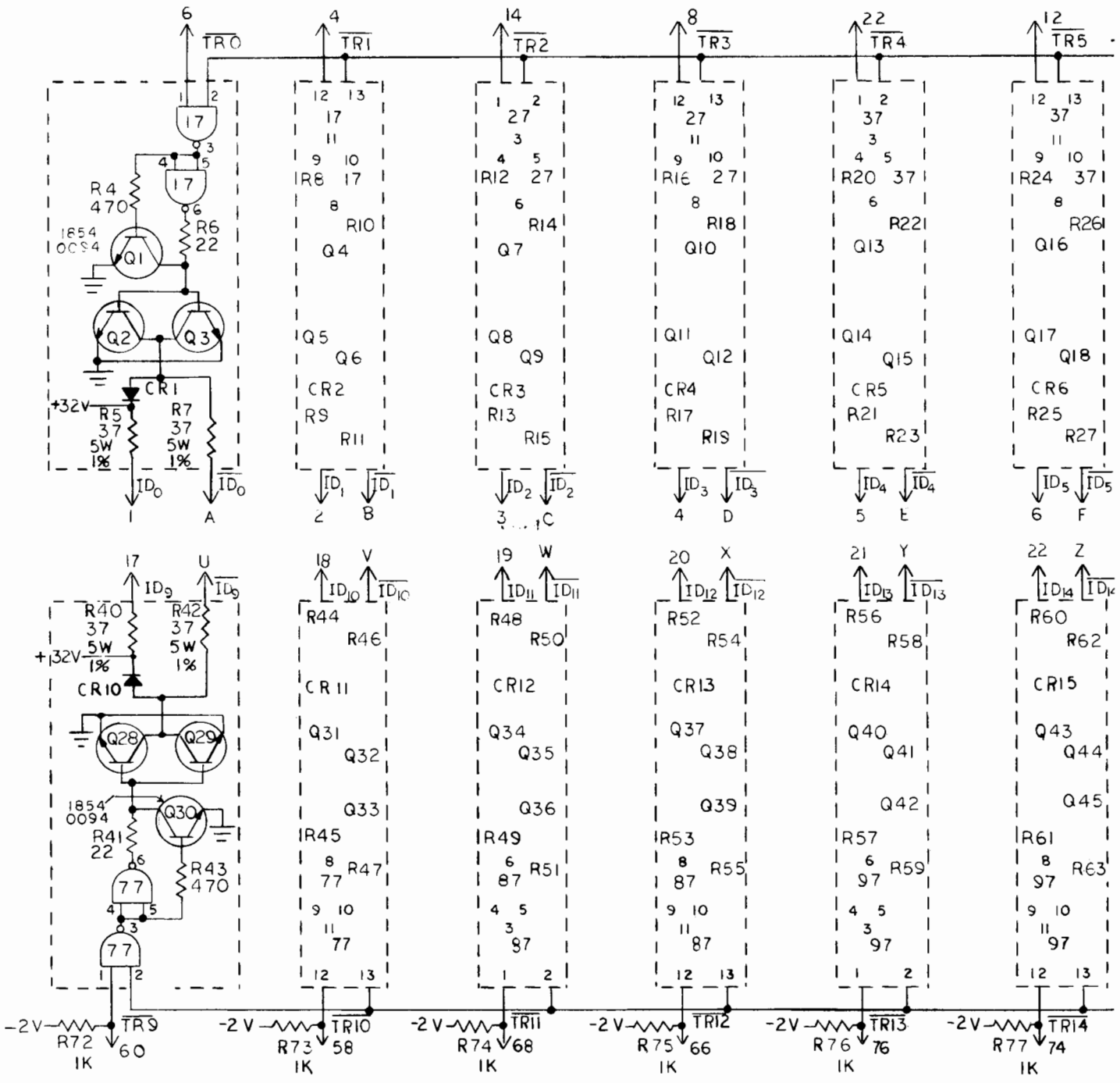
(15) REF DES (MC15)



Computer Museum

Inhibit Driver Card (02116-6265), Logic Diagram

FOR TRAINING PURPOSES ONLY
HP-2116B



NOTE:

UNLESS OTHERWISE NOTED;

ALL RESISTANCE IN OHMS

ALL RESISTORS 1/4 W ± 5%

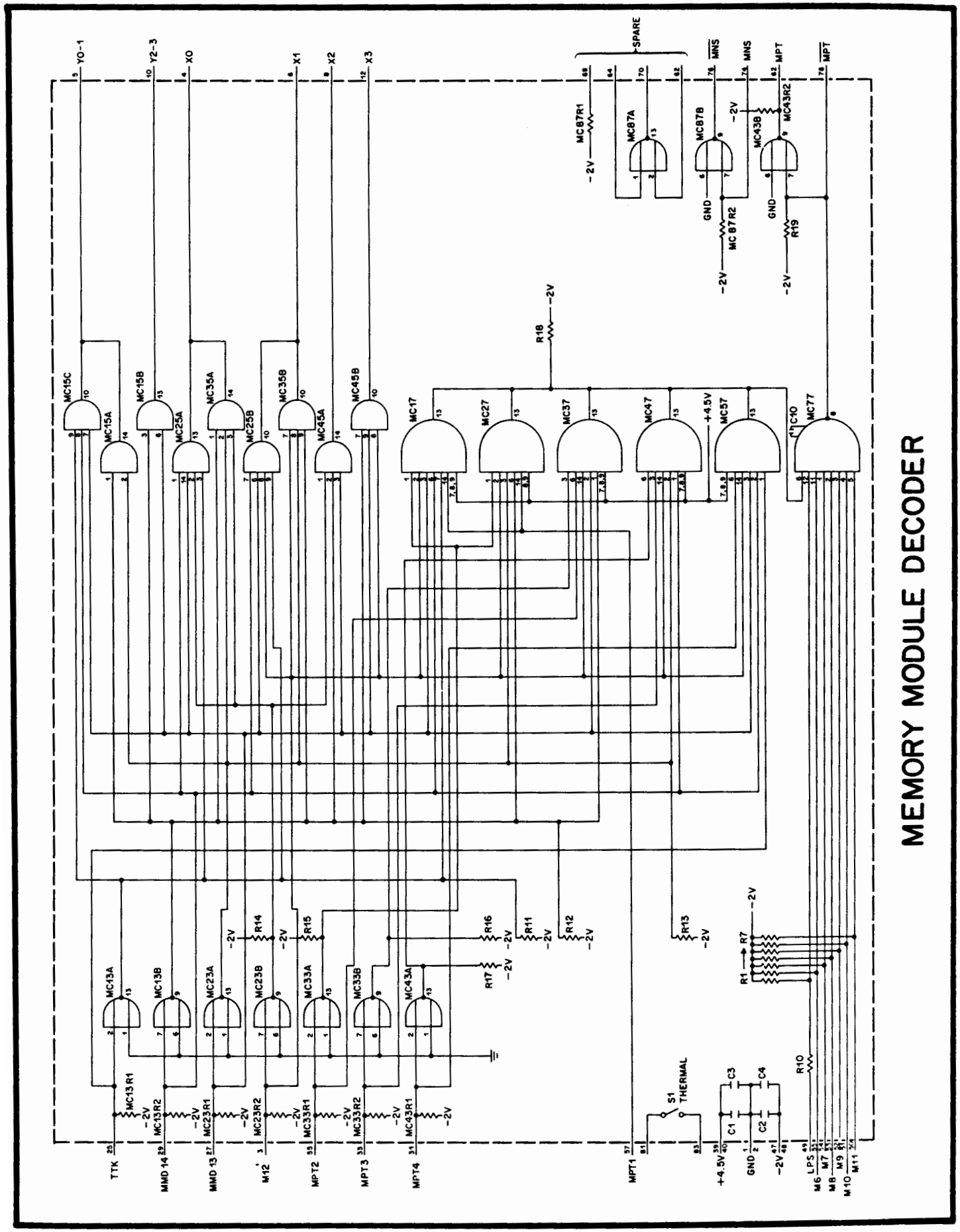
ALL CAPACITANCE IN MICROFARADS

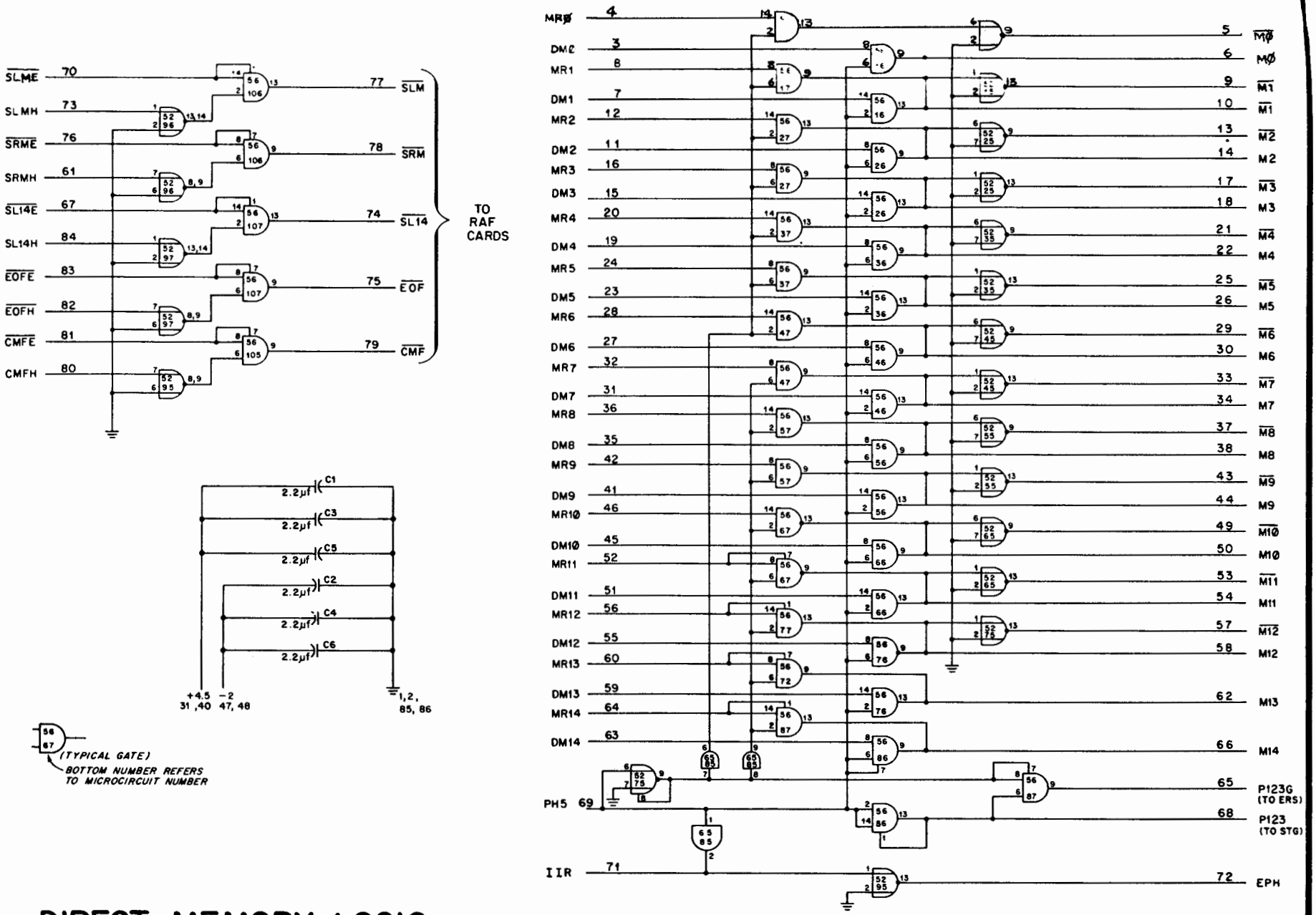
ALL TRANSISTORS 2N3642

ALL MC'S 1820-0127

ALL DIODES 1901-0050

BOARD REV 819





DIRECT MEMORY LOGIC

FIG. 4-16

Voltages

mory 16K
- 3.4V
- 5.6V
-12.4V
+35.5V
+23.3V
-22.6
-36.4
-84.5
+105
+56.4

Memory Supply Regulator A302, Typical Circuit Voltages (See Note 5)

Test Point Description		DC Voltage Measurement
Q50	Emitter	- 8.3V
	Base	- 9.0V
	Collector	-14.0V
Q51	Emitter	- 8.3V
	Base	- 9.0V
Q52	Emitter	-13.1V
Q53	Base	-11.5V
Q54A	Emitter	- 0.7V
	Base	0.0V
	Collector	+24.5V
Q55	Emitter	+23.5V
Q56	Base	+21.7V
Q57	Emitter	+ 0.7V
	Base	0.0V
	Collector	-25.2V
Q58	Emitter	+ 0.7V
Q59	Emitter	-24.4V
Q60	Base	-21.4V
Q61A	Emitter	- 0.7V
	Base	0.0V
	Collector	+34.0V
Q63	Emitter	+32.6V
Q64	Base	+30.6V
A302-1 (+22V Temp Sense)		- 7.9V
A302-13 (+32V Temp Sense)		- 7.9V

Logic Supply Regulator A301, Typical Circuit Voltages (See Note 5)

Test Point Description		DC Voltage Measurement
Q30	Base	+ 4.5V
Q31	Base	+ 4.5V
Q32	Emitter	- 1.2V
Q33	Base	+ 0.1V
	Collector	- 2.3V
Q35	Base	0.0V
Q37	Emitter	- 3.3V
Q38	Base	- 1.9V
	Collector	- 4.4V
Q39	Base	+ 0.7V
Q41	Emitter	+12.7V
Q42	Base	+11.3V
	Collector	+14.0V

NOTES:

1. Capacitor values are in microfarads.
2. See "Overall Computer Interconnection and Schematic Diagram" for connections to the Card Cage Assembly and Door Assembly.
3. Jumper "A" must be removed when external power control connector J2 is used.
4. For operation with 230 VAC power source, remove both jumpers from transformer terminals 1, 2, 3, and 4 and reconnect both jumpers between terminals 2 and 3.
5. Voltages specified are typical and mea sured under the following conditions:

   a. 115 VAC, 60 CPS main power input;

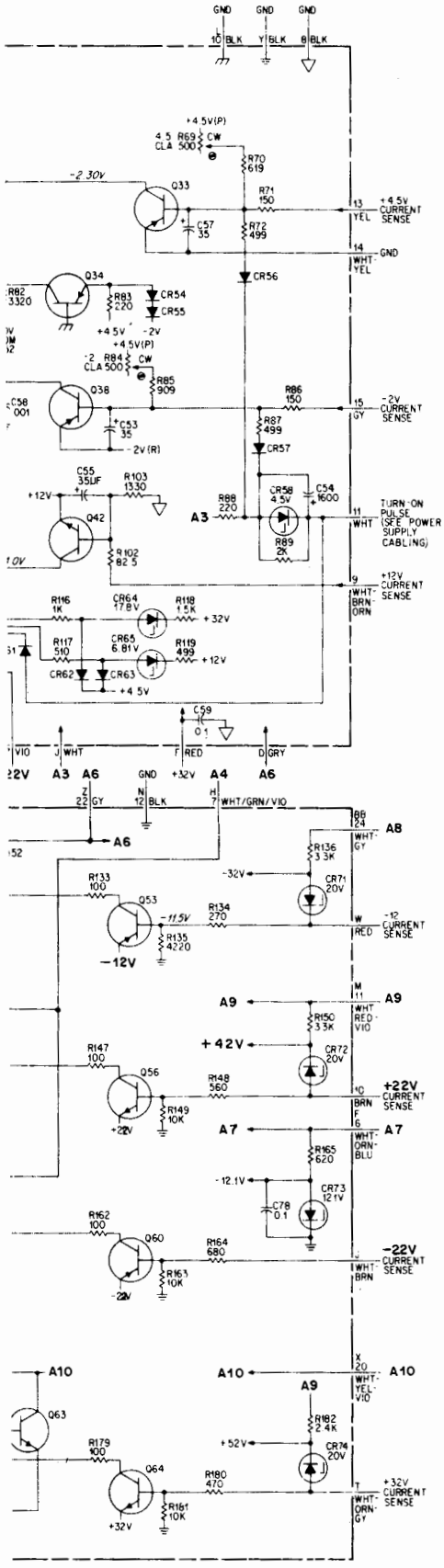
   b. All cards removed from the I/O slots except A201, A202, and slot containing Resistance Load Card 02116-6047;

   c. Computer in HALT mode;

   d. Minimum warm-up period of 30-minutes prior to taking measurements;

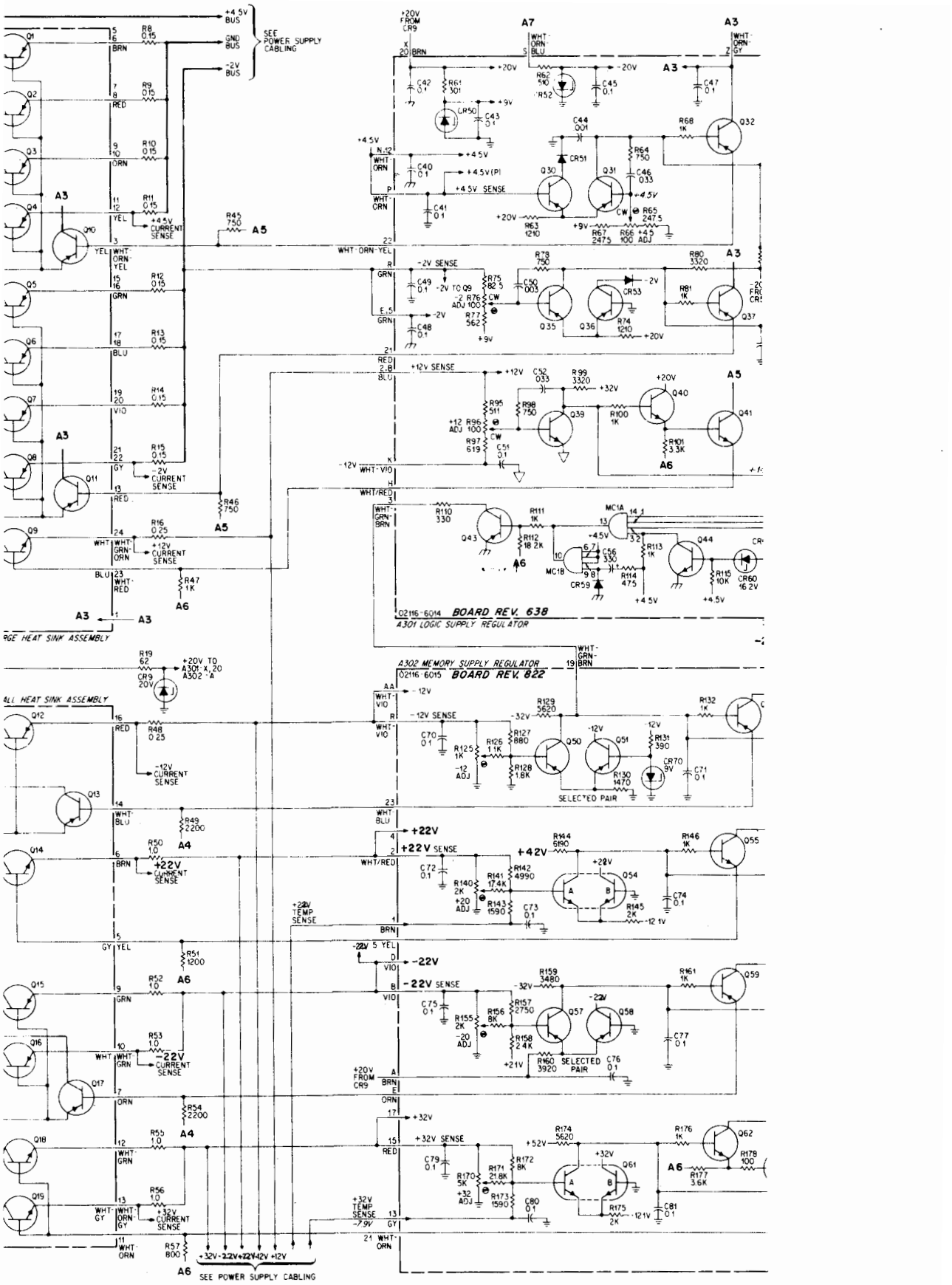
   e. Supply voltages set to +32V, +22.8V, -22.8V, +12V, -12V, +4.5V and -2V (all voltages ±1%) as measured at test jacks on Crowbar Assembly 02116-6284 (A121).

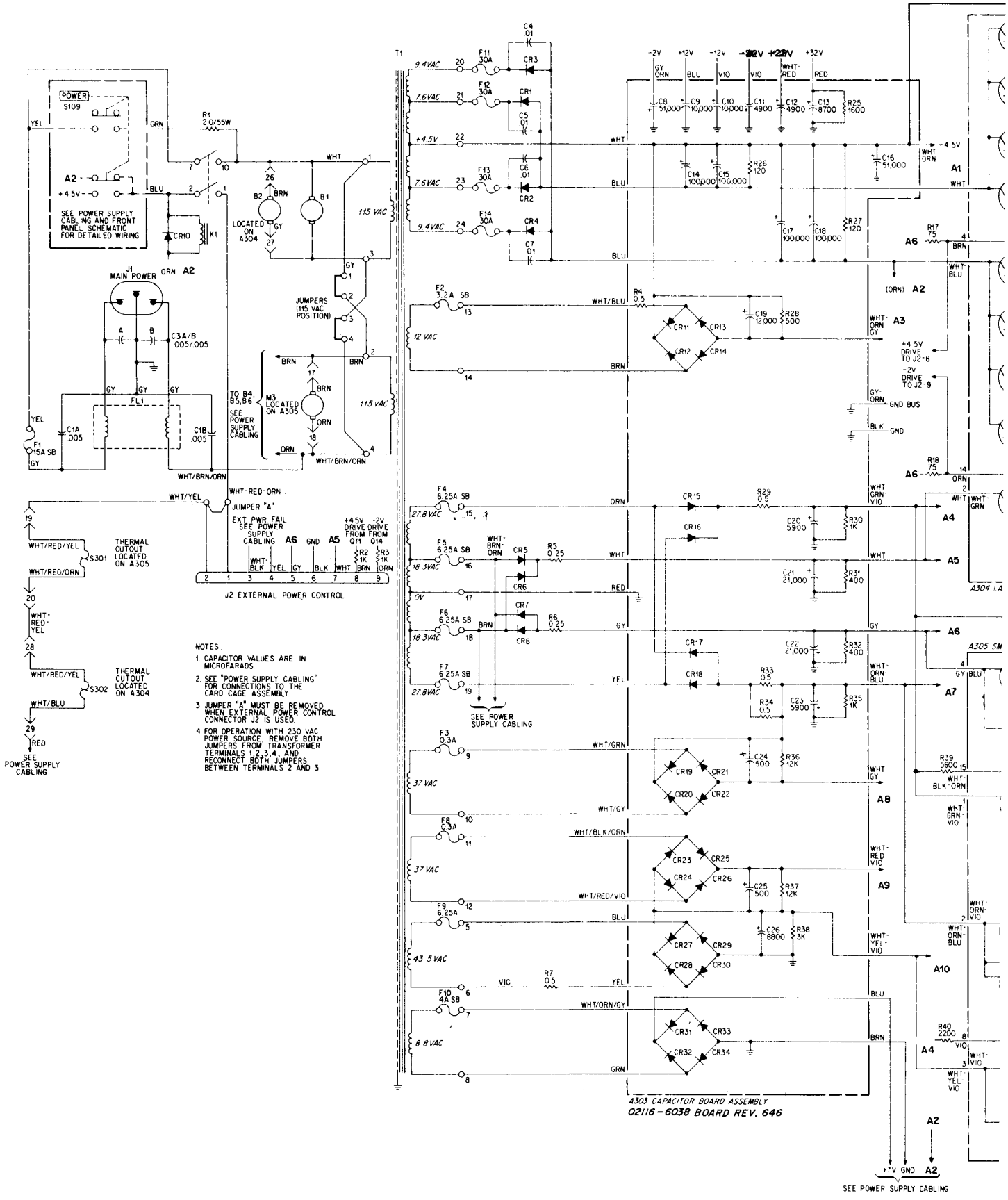
Power Supply Assembly (02116-6124), Schematic Diagram



Capacitor Board A303, Typical Raw DC
(See Note 5)

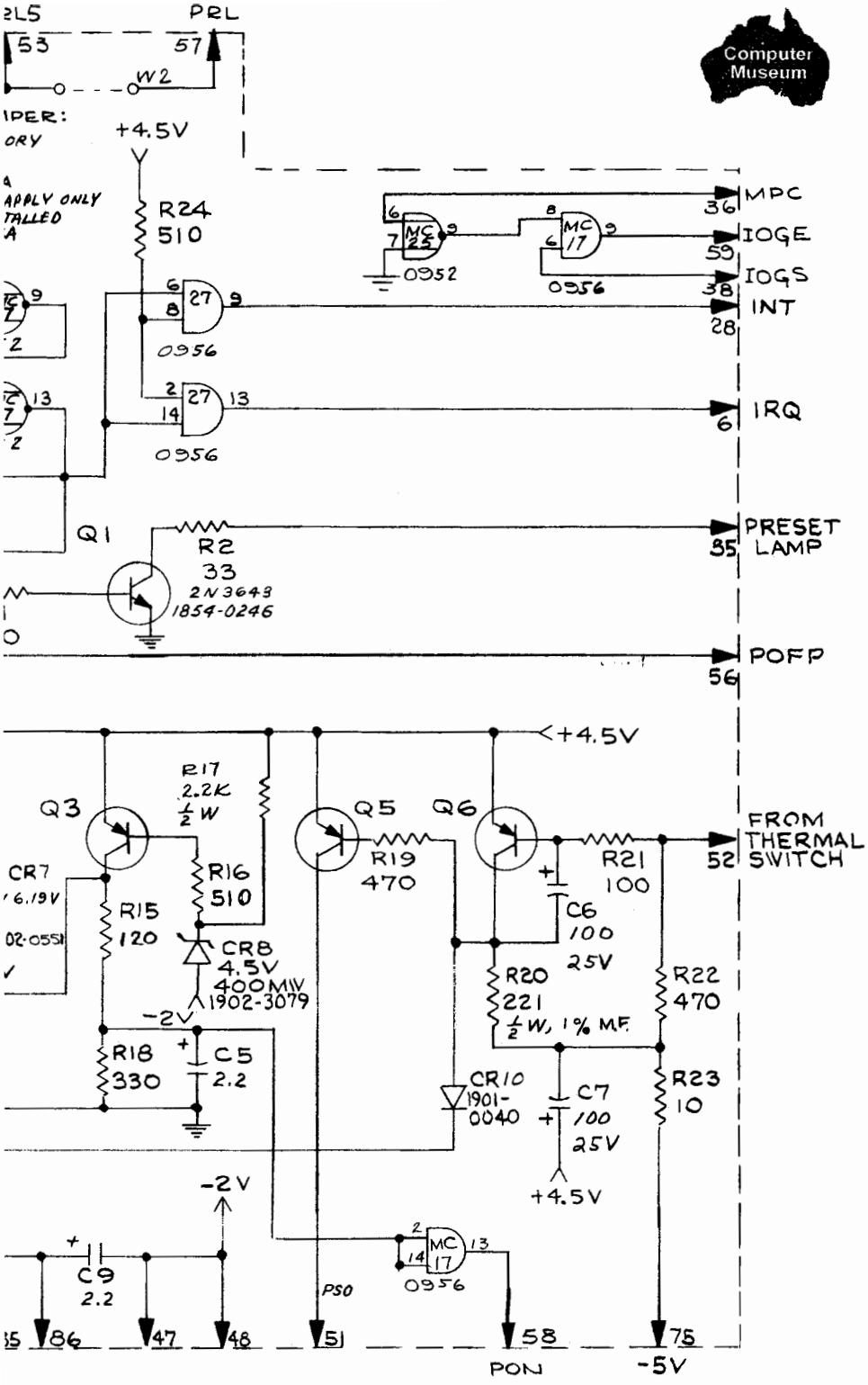
Test Point	Source Identification	Me 8K
A1	A303R26 (White Lead) to Collectors of A304Q1 thru A304Q4	- 3.9V
A2	A303R27 (Orange Lead) to Collector of A304Q5 and CR10	- 6.0V
A3	A303R28 (White-Orange-Gray Lead) to A304-1 and A301-2	-12.9V
A4	A303R30 (White-Green-Violet Lead) to A305-1, -15, A302-7, -H, R19, R44, R54	+36.9V
A5	A303R31 (White Lead) to A304-2, A301-J, R45, R46, and J2-7	+22.4V
A6	A303R32 (Gray Lead) to A305-4, A301-D, A302-2, -22, R47, R57, junction of R52 and R53, and J2-5	-23.8
A7	A303R35 (White-Orange-Blue Lead) to A305-2, A301-8, and A302-6	-37.2
A8	A303R36 (White-Gray Lead) to A302-24, -BB	-86.9
A9	A303R37 (White-Red-Violet Lead) to A302-11, -M	+107
A10	A303R38 (White-Yellow-Violet Lead) to A305-3 and A302-20, -X	+58.0


+4.5V BUS
GND BUS
-2V BUS
SEE POWER SUPPLY CABLING
+20V FROM CR9
A7
A3
A5
A6
+4.5V CURRENT SENSE
-2V CURRENT SENSE
+12V CURRENT SENSE
-12V CURRENT SENSE
+22V CURRENT SENSE
-22V CURRENT SENSE
+32V CURRENT SENSE
-2V SENSE
+12V SENSE
+4.5V SENSE
-12V SENSE
+22V SENSE
-22V SENSE
+32V SENSE
02116-6014 BOARD REV. 638
4301 LOGIC SUPPLY REGULATOR
A302 MEMORY SUPPLY REGULATOR
02116-6015 BOARD REV. 822
SELECTED PAIR
+22V TEMP SENSE
+32V TEMP SENSE
SEE POWER SUPPLY CABLING

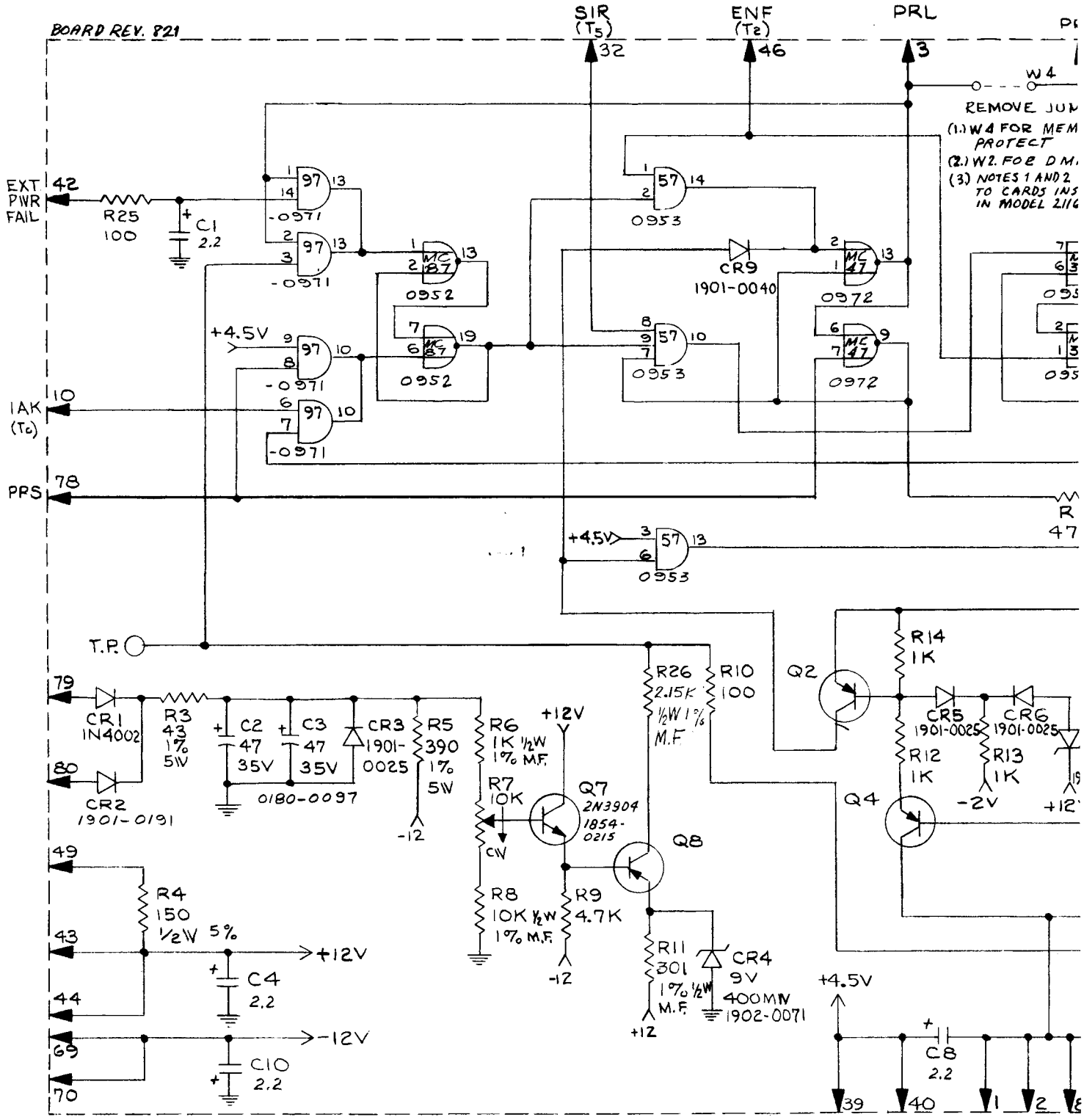


NOTES:

1. CAPACITOR VALUES ARE IN MICROFARADS.
2. SEE "POWER SUPPLY CABLING" FOR CONNECTIONS TO THE CARD CAGE ASSEMBLY.
3. JUMPER "A" MUST BE REMOVED WHEN EXTERNAL POWER CONTROL CONNECTOR J2 IS USED.
4. FOR OPERATION WITH 230 VAC POWER SOURCE, REMOVE BOTH JUMPERS FROM TRANSFORMER TERMINALS 1,2,3,4, AND RECONNECT BOTH JUMPERS BETWEEN TERMINALS 2 AND 3.



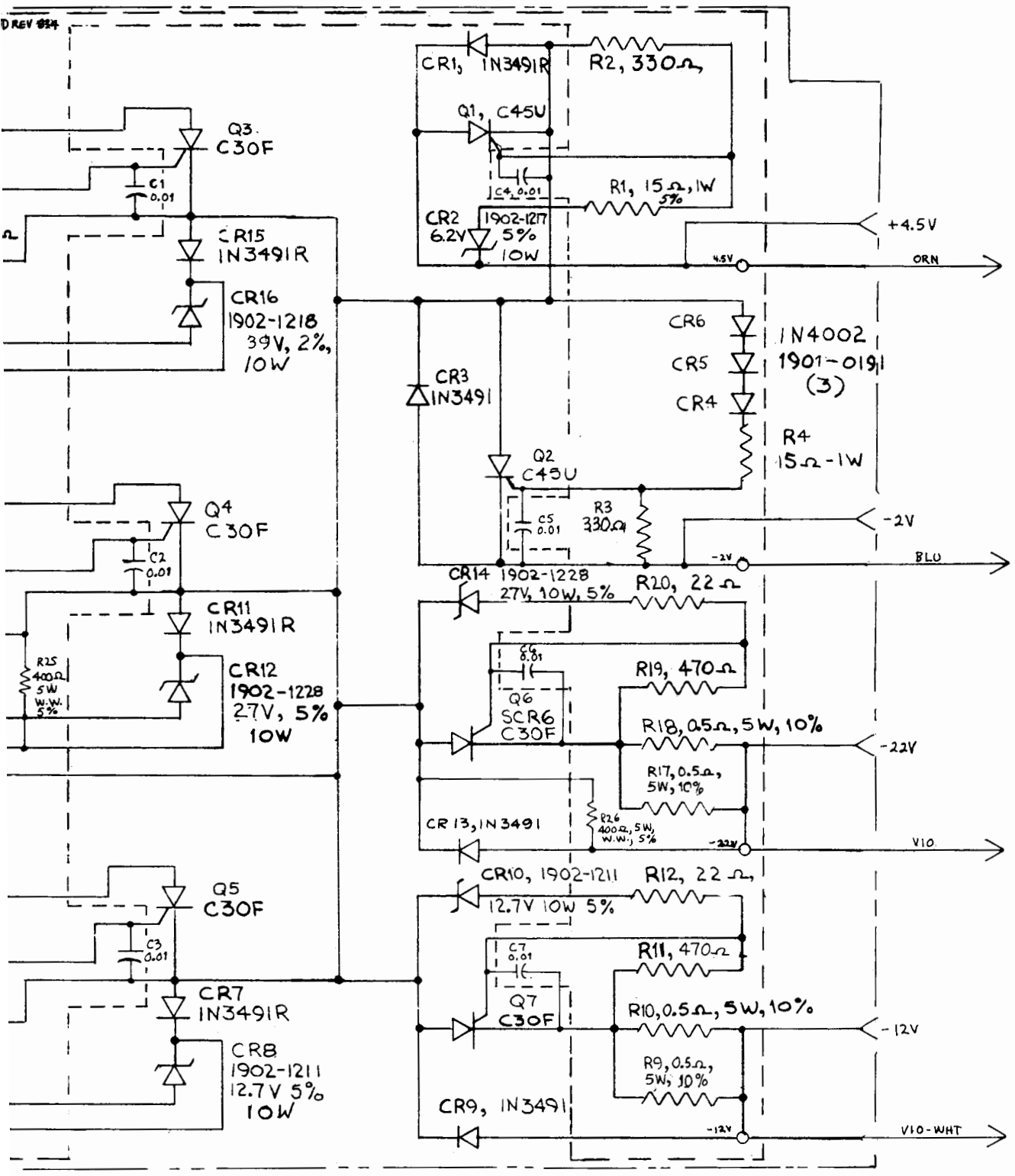
Power Fail Interrupt
Card (02116-6175), Logic Diagram



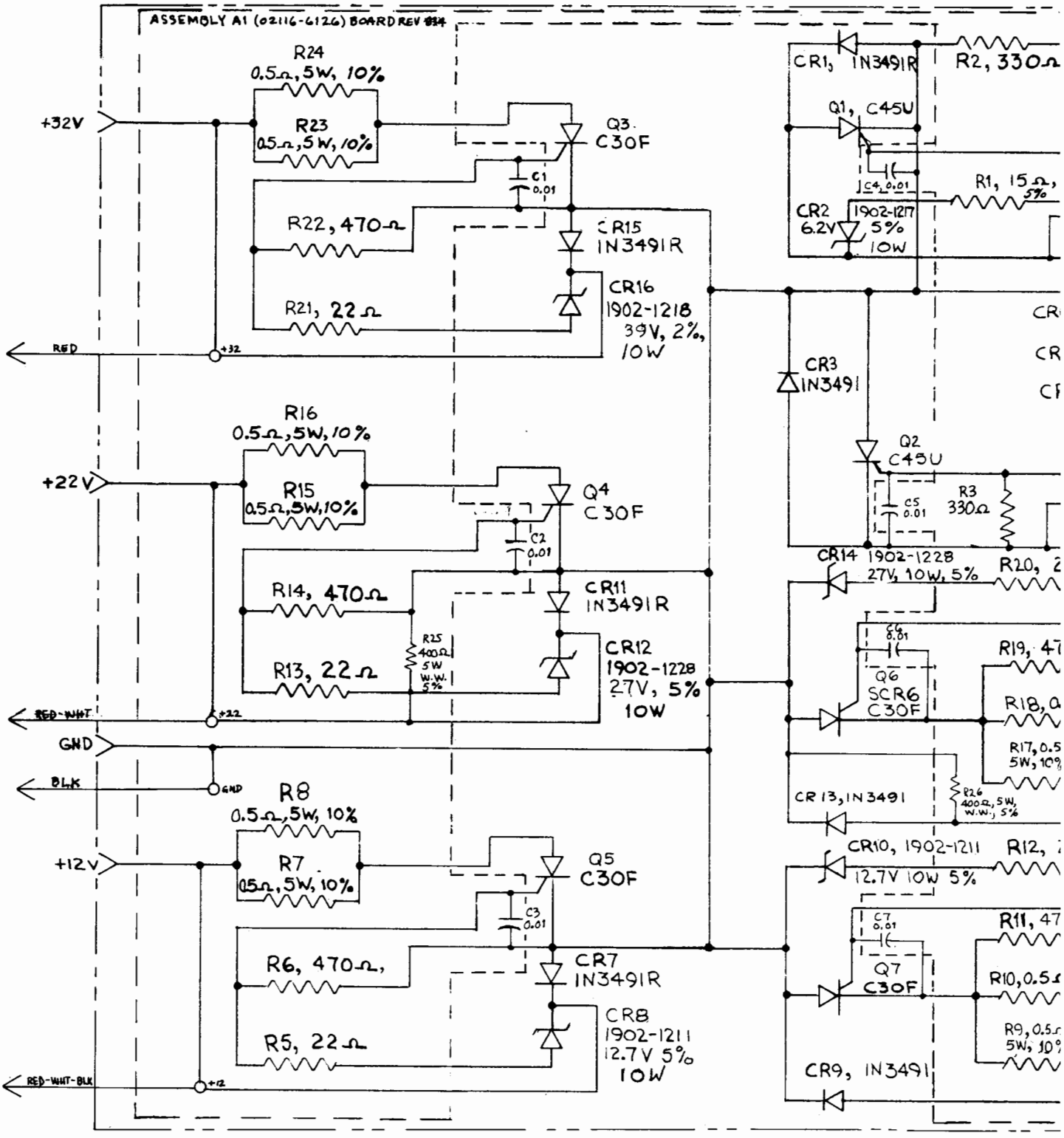
NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR
   VALUES GIVEN IN OHMS
   TOLERANCE ± 5%
   1/4 WATT
2. ALL CAPACITOR
   VALUES GIVEN IN MICROFARADS
3. ALL TRANSISTORS ARE 2N3906 (1853-0036)

ALL MC-PACKS PRECEDED BY 1820-

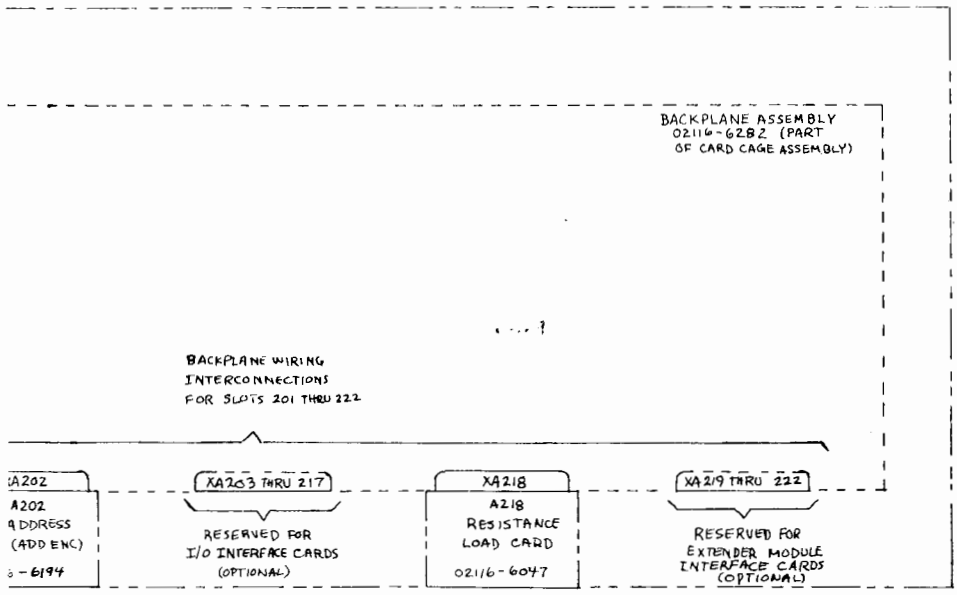


Overvoltage Protection Assembly (02116-6284), Schematic Diagram

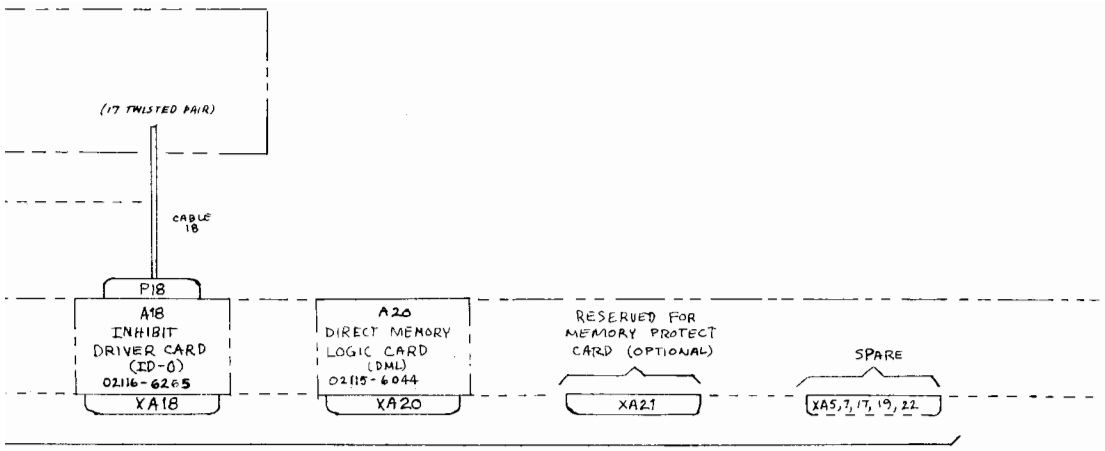


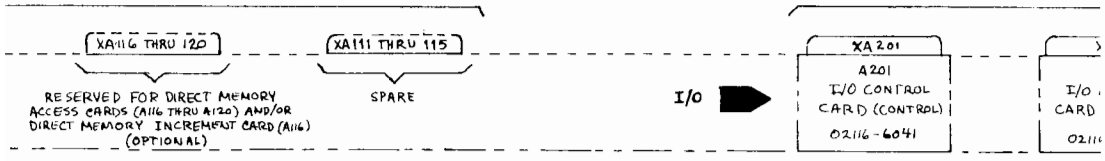
NOTE:
UNLESS NOTED
ALL RESISTORS 1/2W 5% Comp
ALL CAPACITORS 0.01 MFD, 100 WVDC,
-20 +80%, DISC CERAMIC. PART
NO. 0150-0093

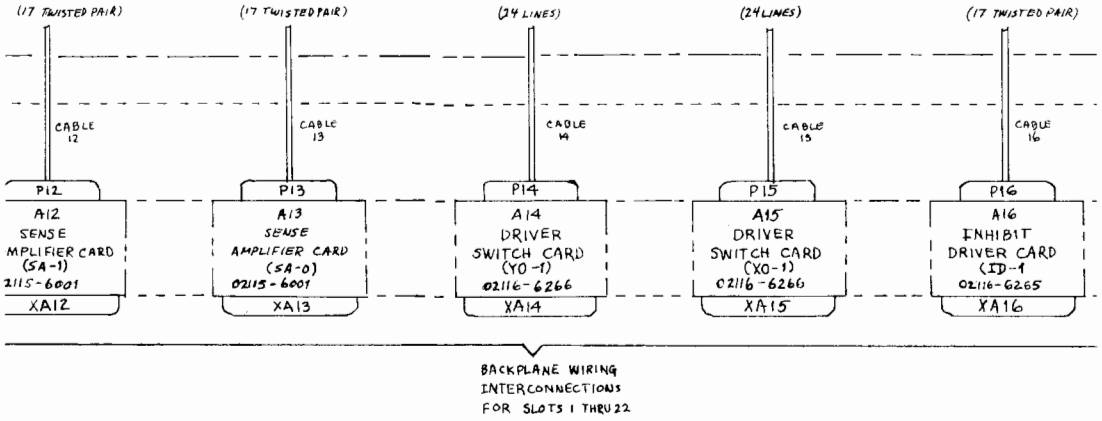
Assembly (

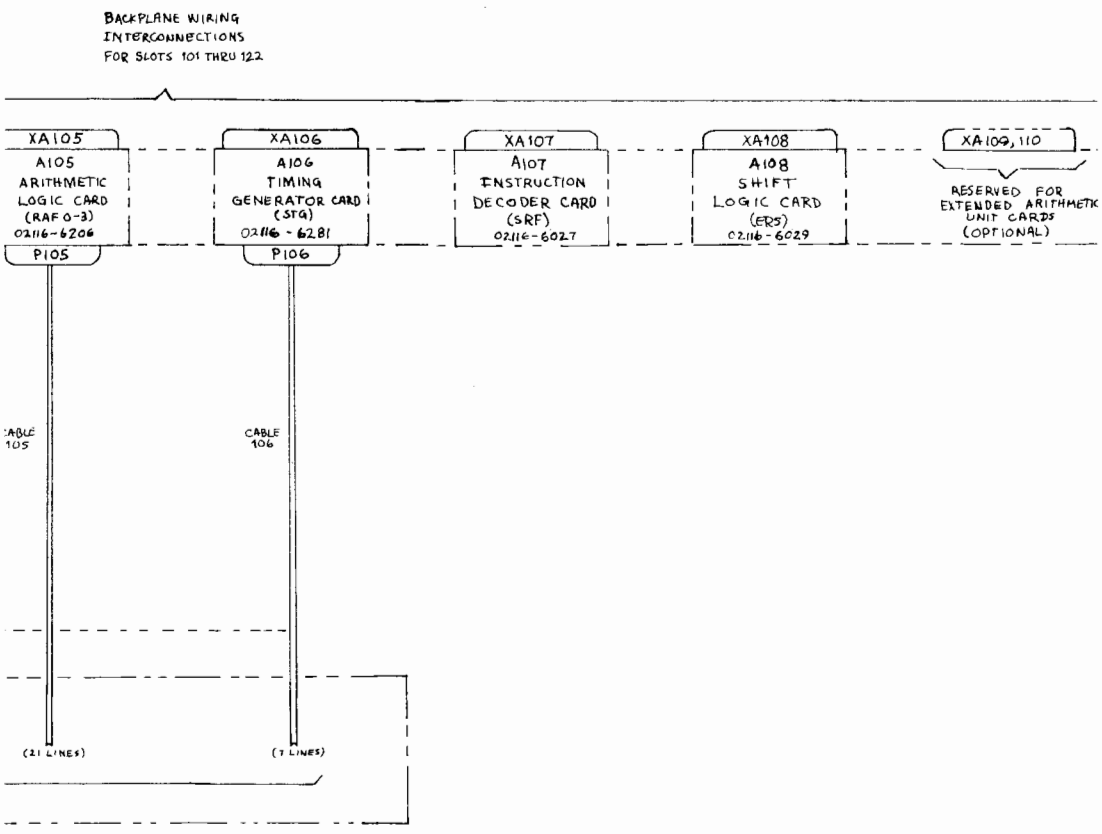


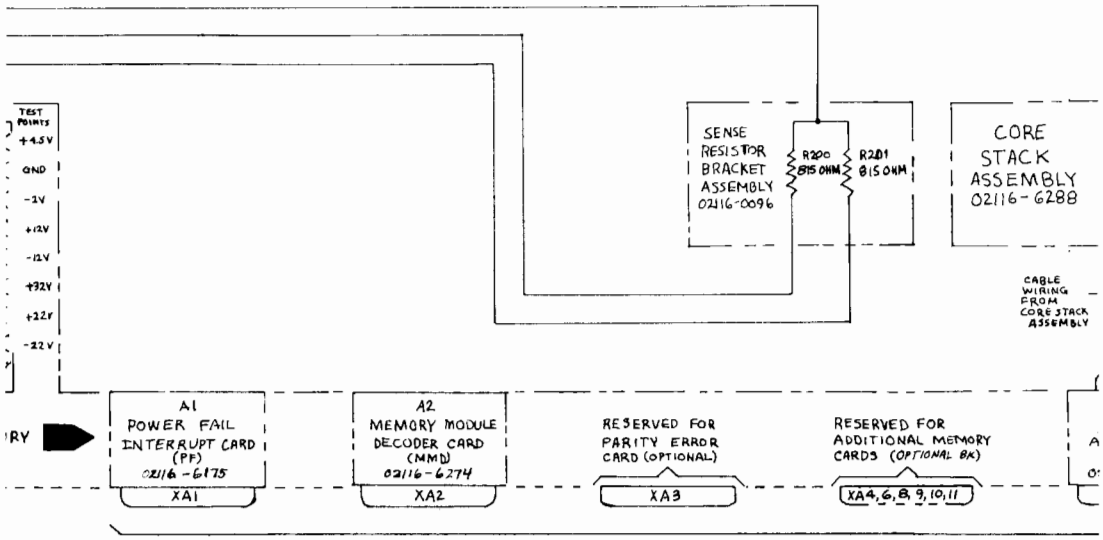
Model HP 2116B Computer, Overall Interconnection Diagram

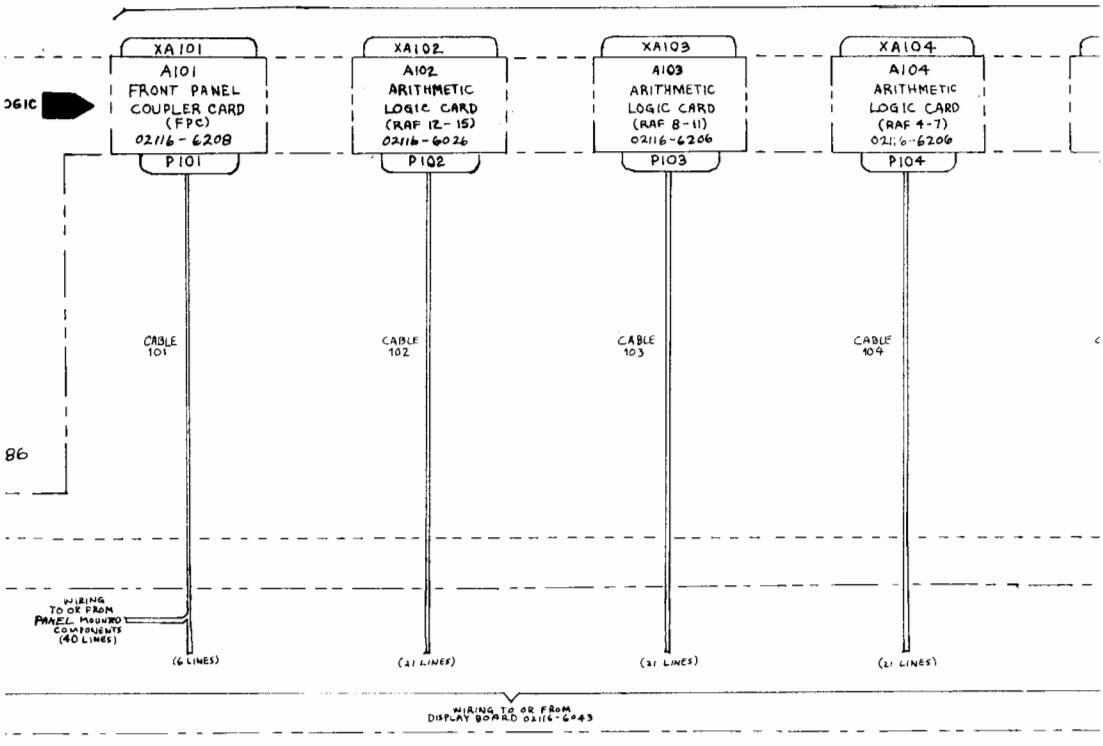

(17 TWISTED PAIR)
CABLE 1B
P18
A18
INHIBIT
DRIVER CARD
(ID-0)
02116-6265
XA18
A20
DIRECT MEMORY
LOGIC CARD
(DML)
02115-6044
XA20
RESERVED FOR
MEMORY PROTECT
CARD (OPTIONAL)
XA21
SPARE
XA5, 7, 17, 19, 22

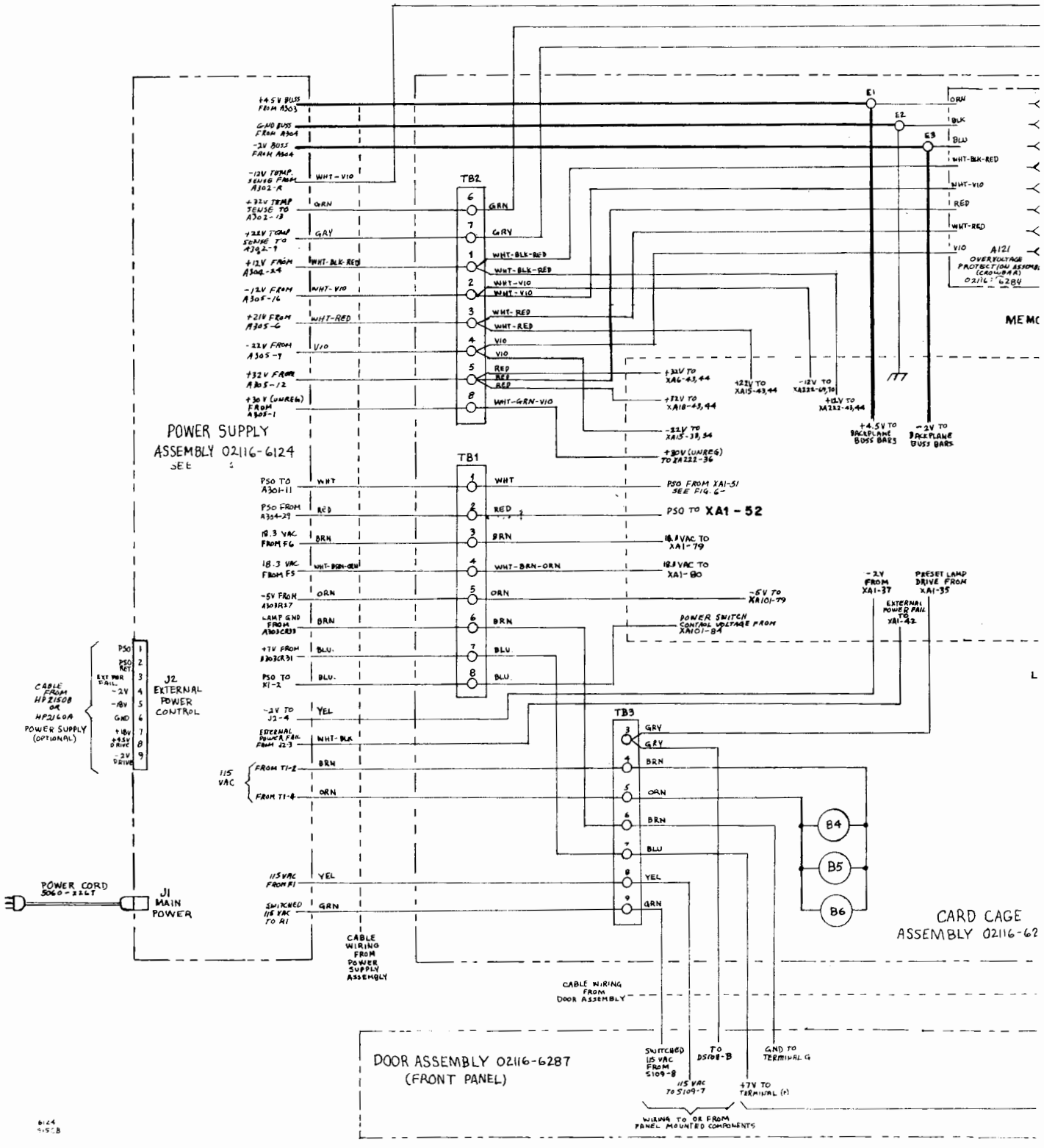

XA116 THRU 120
RESERVED FOR DIRECT MEMORY
ACCESS CARDS (A116 THRU A120) AND/OR
DIRECT MEMORY INCREMENT CARD (A116)
(OPTIONAL)
XA111 THRU 115
SPARE
I/O
XA201
A201
I/O CONTROL
CARD (CONTROL)
02116-6041

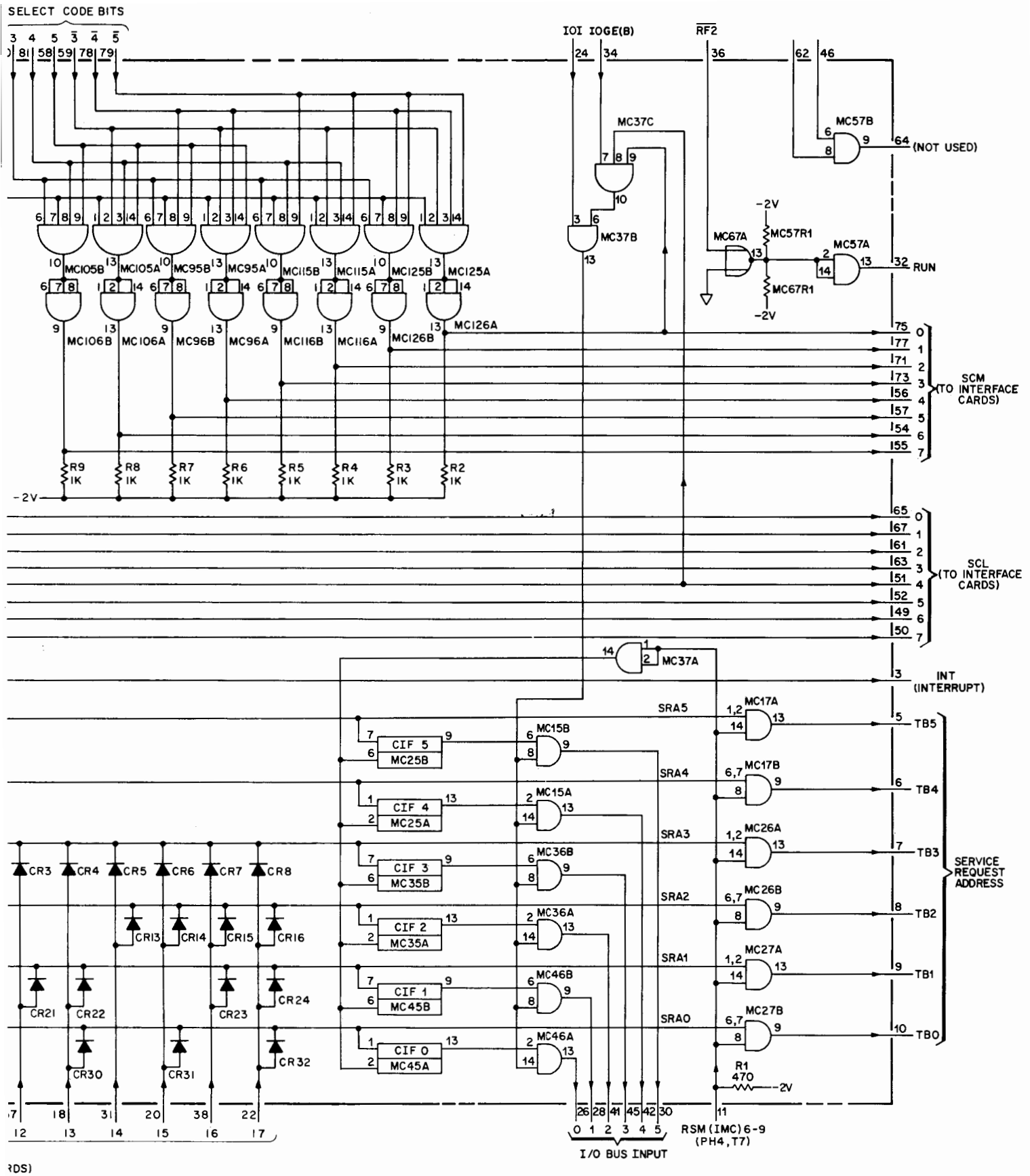

(17 TWISTED PAIR)
(17 TWISTED PAIR)
(24 LINES)
(24 LINES)
(17 TWISTED PAIR)
CABLE 12
CABLE 13
CABLE 14
CABLE 15
CABLE 16
P12
P13
P14
P15
P16
A12 SENSE AMPLIFIER CARD (SA-1) 2115-6001
A13 SENSE AMPLIFIER CARD (SA-0) 02115-6001
A14 DRIVER SWITCH CARD (YO-1) 02116-6266
A15 DRIVER SWITCH CARD (XO-1) 02116-6266
A16 INHIBIT DRIVER CARD (ID-1 02116-6265
XA12
XA13
XA14
XA15
XA16
BACKPLANE WIRING INTERCONNECTIONS FOR SLOTS 1 THRU 22


BACKPLANE WIRING INTERCONNECTIONS FOR SLOTS 101 THRU 122
XA105
XA106
XA107
XA108
XA109, 110
A105 ARITHMETIC LOGIC CARD (RAF 0-3) 02116-6206
A106 TIMING GENERATOR CARD (STG) 02116-6281
A107 INSTRUCTION DECODER CARD (SRF) 02116-6027
A108 SHIFT LOGIC CARD (ERS) 02116-6029
RESERVED FOR EXTENDED ARITHMETIC UNIT CARDS (OPTIONAL)
P105
P106
CABLE 105
CABLE 106
(21 LINES)
(7 LINES)

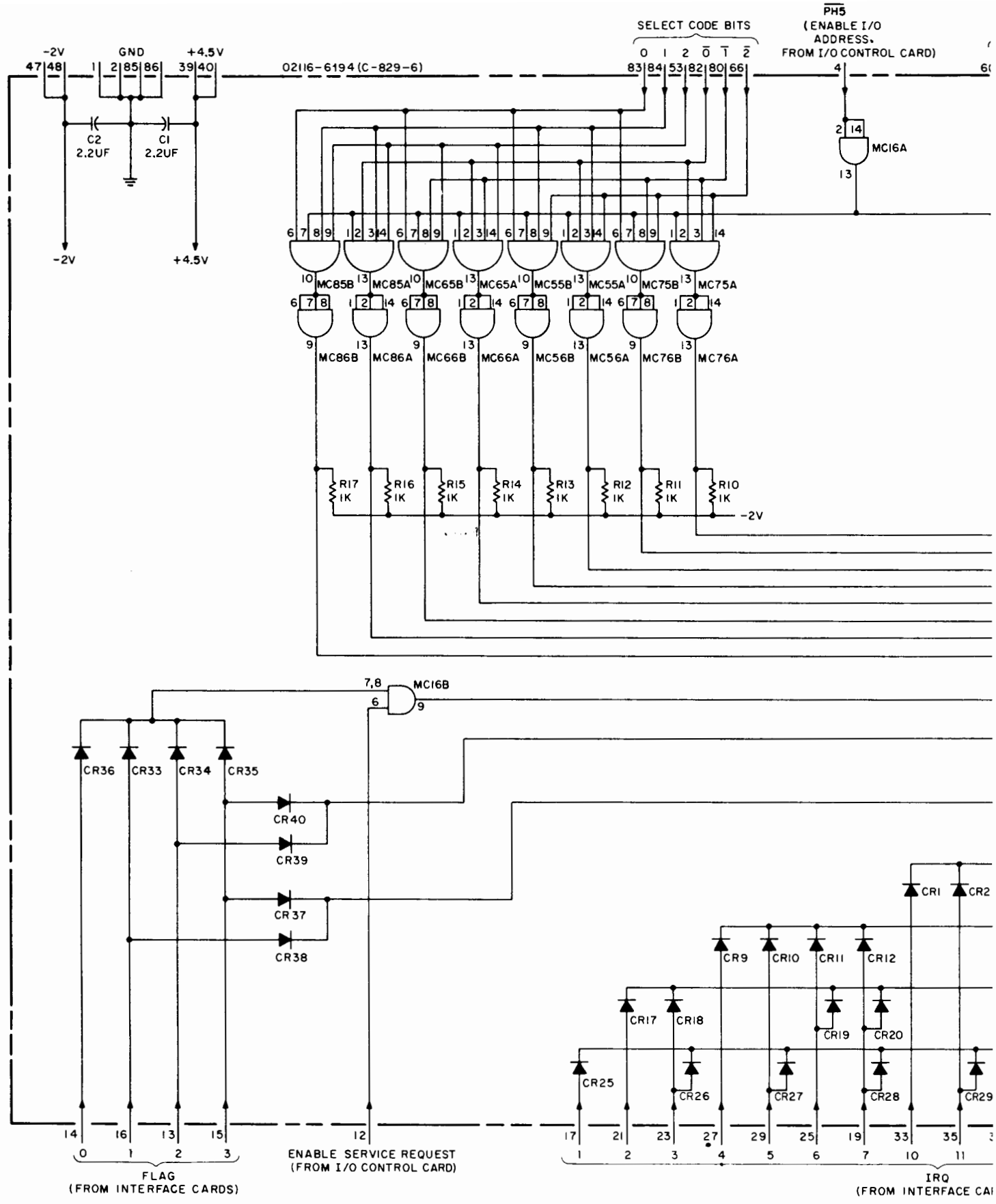

TEST POINTS
+4.5V
GND
-2V
+12V
-12V
+32V
+22V
-22V
SENSE RESISTOR BRACKET ASSEMBLY 02116-0096
R200 815 OHM
R201 815 OHM
CORE STACK ASSEMBLY 02116-6288
CABLE WIRING FROM CORE STACK ASSEMBLY
A1 POWER FAIL INTERRUPT CARD (PF) 02116-6175
XA1
A2 MEMORY MODULE DECODER CARD (MMD) 02116-6274
XA2
RESERVED FOR PARITY ERROR CARD (OPTIONAL)
XA3
RESERVED FOR ADDITIONAL MEMORY CARDS (OPTIONAL 8K)
XA4,6,8,9,10,11


XA101
A101 FRONT PANEL COUPLER CARD (FPC) 02116-6208
P101
XA102
A102 ARITHMETIC LOGIC CARD (RAF 12-15) 02116-6026
P102
XA103
A103 ARITHMETIC LOGIC CARD (RAF 8-11) 02116-6206
P103
XA104
A104 ARITHMETIC LOGIC CARD (RAF 4-7) 02116-6206
P104
CABLE 101
CABLE 102
CABLE 103
CABLE 104
WIRING TO OR FROM PANEL MOUNTED COMPONENTS (40 LINES)
(6 LINES)
(21 LINES)
(21 LINES)
(21 LINES)
WIRING TO OR FROM DISPLAY BOARD 02116-6043


POWER SUPPLY ASSEMBLY 02116-6124
SEE
TB2
TB1
TB3
J2 EXTERNAL POWER CONTROL
J1 MAIN POWER
POWER CORD 5060-2224
CABLE FROM HP2150B OR HP2160A POWER SUPPLY (OPTIONAL)
CABLE WIRING FROM POWER SUPPLY ASSEMBLY
CABLE WIRING FROM DOOR ASSEMBLY
DOOR ASSEMBLY 02116-6287 (FRONT PANEL)
CARD CAGE ASSEMBLY 02116-62
WIRING TO OR FROM PANEL MOUNTED COMPONENTS
+4.5V BUSS FROM A303
GND BUSS FROM A304
-2V BUSS FROM A304
-12V TEMP. SENSE FROM A302-A
+32V TEMP SENSE TO A302-13
+32V TEMP SENSE TO A302-9
+12V FROM A304-24
-12V FROM A305-16
+24V FROM A305-6
-32V FROM A305-9
+32V FROM A305-12
+30V (UNREG) FROM A305-1
PSO TO A301-11
PSO FROM A304-29
18.3 VAC FROM F6
18.3 VAC FROM F5
-5V FROM A303R27
LAMP GND FROM A303CR33
+7V FROM A303CR31
PSO TO K1-2
-2V TO J2-4
EXTERNAL POWER FAIL FROM 22-3
115 VAC FROM T1-2
FROM T1-4
115VAC FROM F1
SWITCHED 115 VAC FROM A1
+32V TO XA6-43,44
+12V TO XA15-43,44
-12V TO XA22-69,70
+12V TO XA22-43,44
-32V TO XA15-38,54
+30V (UNREG) TO XA222-36
+4.5V TO BACKPLANE BUSS BARS
-2V TO BACKPLANE BUSS BARS
PSO FROM XA1-51 SEE FIG. 6-
PSO TO XA1-52
18.3 VAC TO XA1-79
18.3 VAC TO XA1-80
-5V TO XA101-79
POWER SWITCH CONTROL VOLTAGE FROM XA101-84
-2V FROM XA1-37
PRESET LAMP DRIVE FROM XA1-35
EXTERNAL POWER FAIL TO XA1-42
SWITCHED 115 VAC FROM S109-8
115 VAC TO S109-7
TO DS108-B
GND TO TERMINAL G
+7V TO TERMINAL (+)
B4
B5
B6
A121 OVERVOLTAGE PROTECTION ASSEMBLY (CROWBAR) 02116-6284
E1
E2
E3
6124 9-5-78

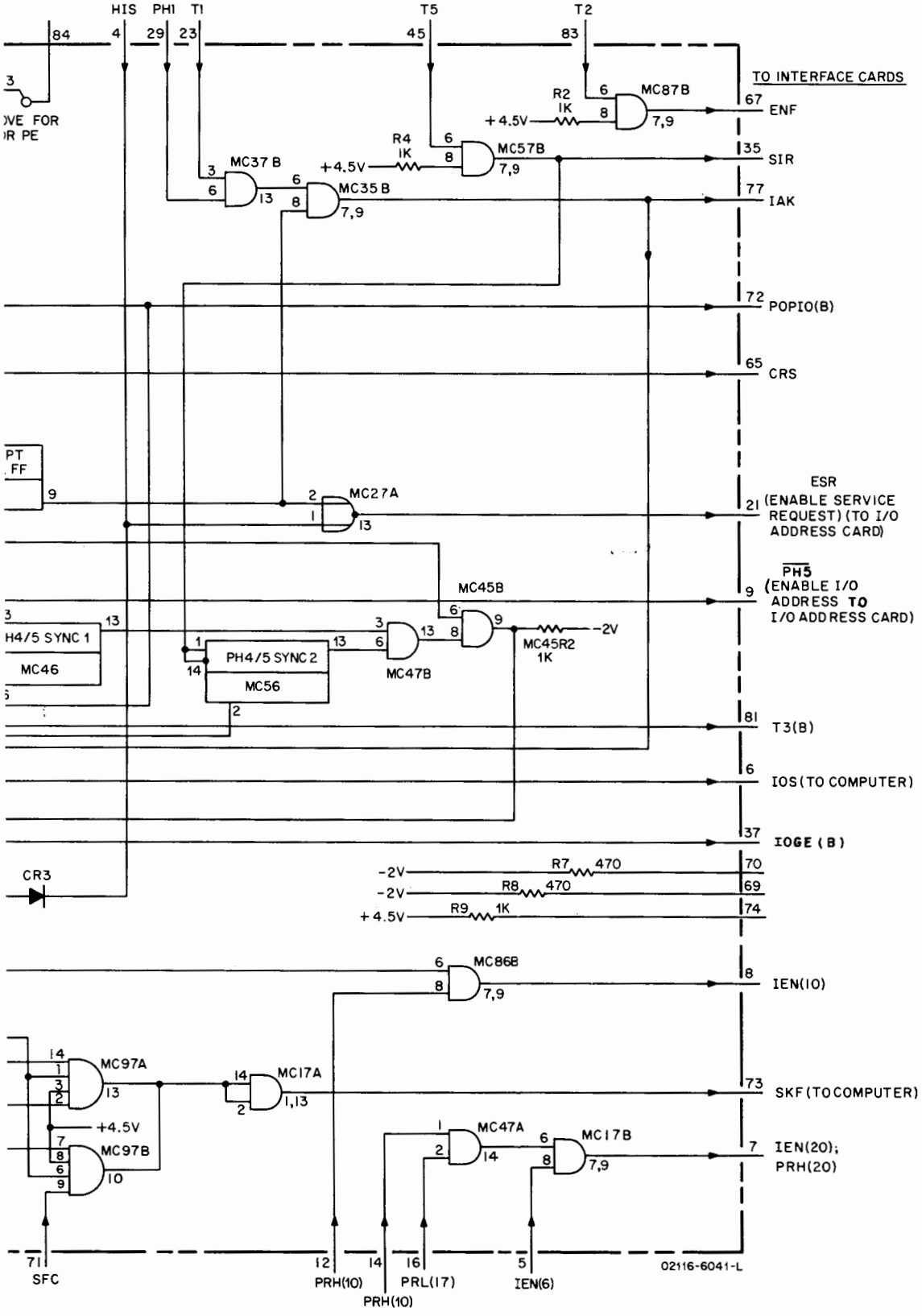


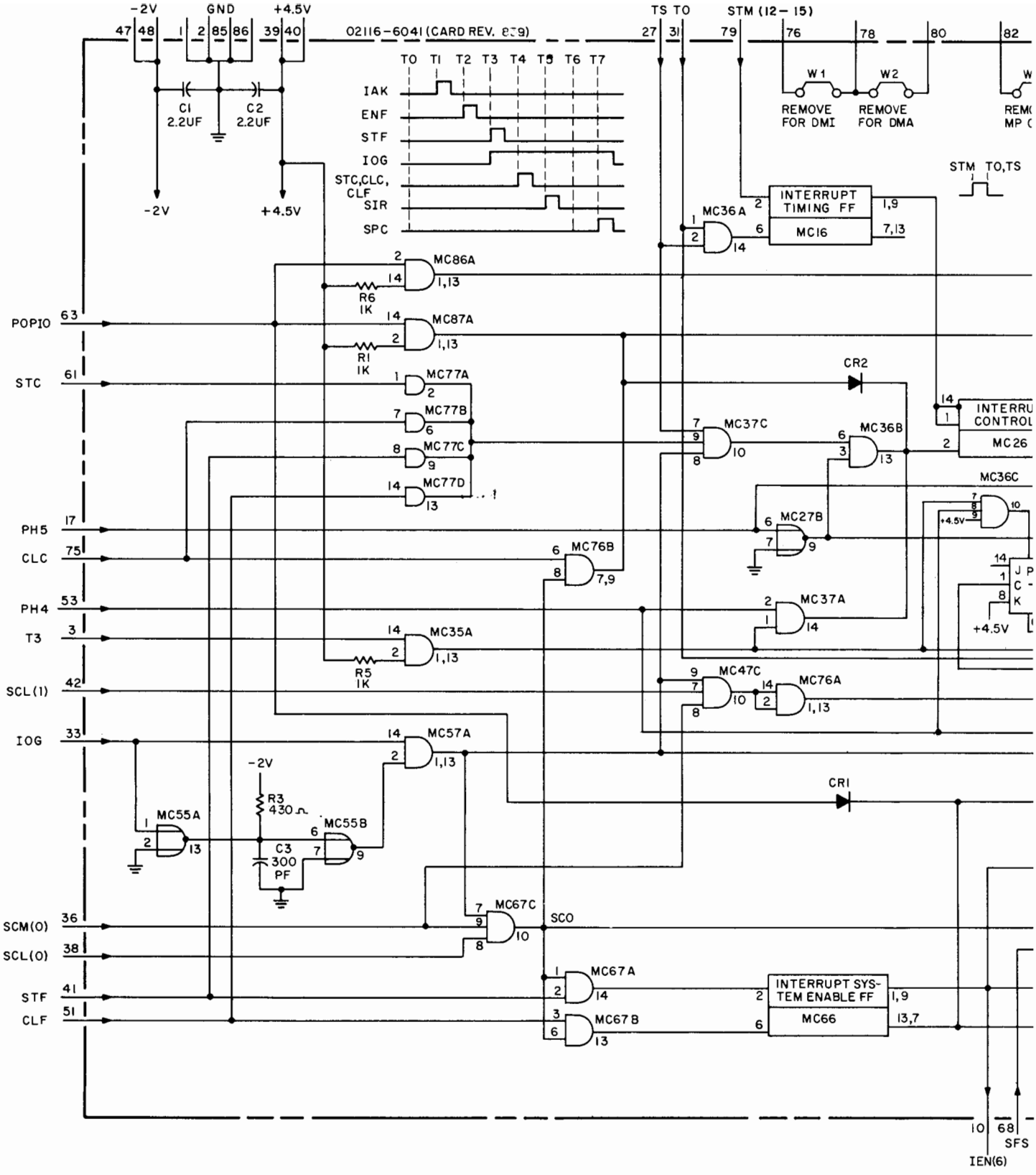
I/O Address Card



NOTE:

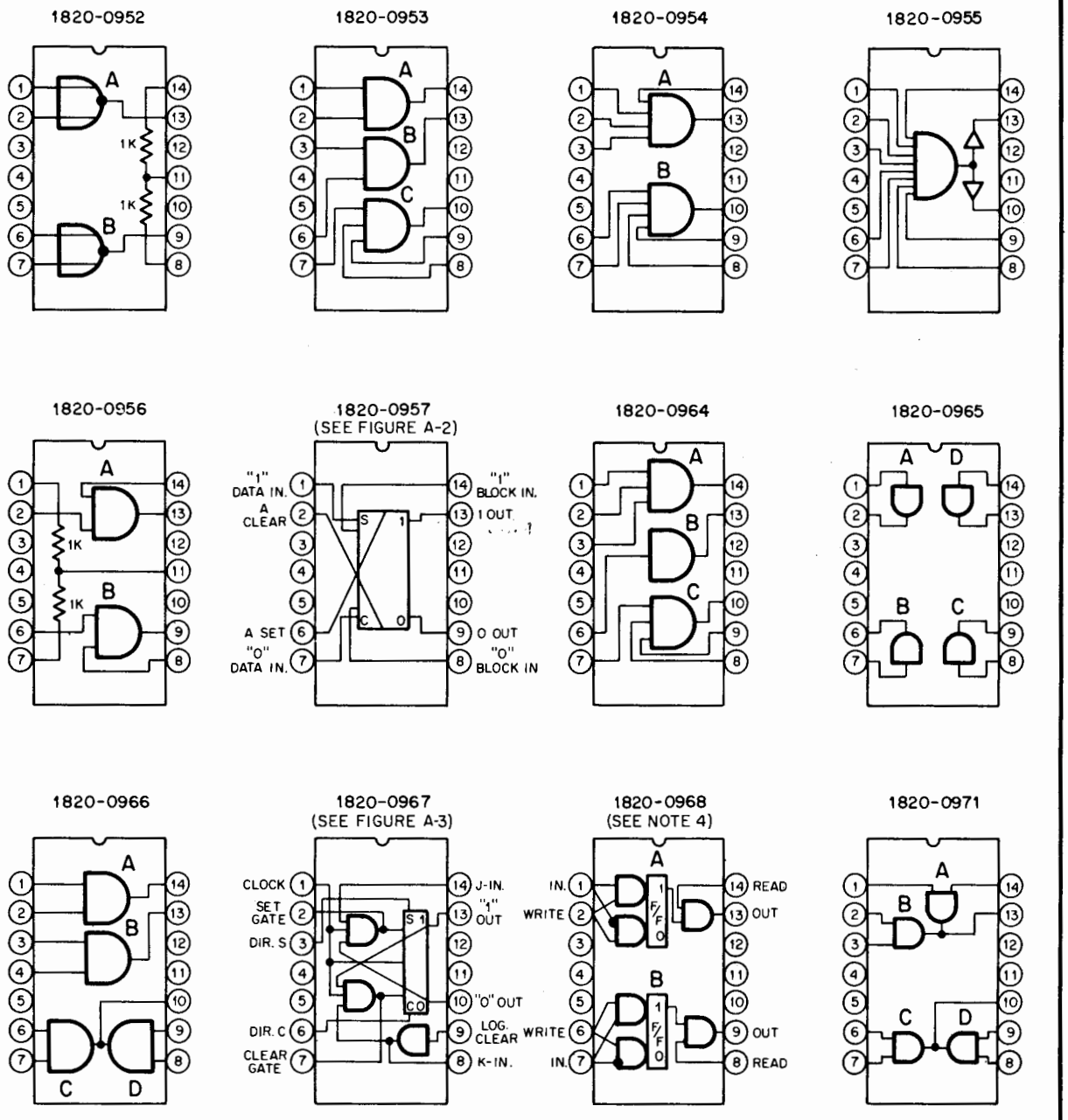
1. ALL LOGIC IS POSITIVE-TRUE.





NOTES:

1. ALL LOGIC IS POSITIVE-TRUE.
2. THE TIMING CHART DOES NOT RELATE SIGNALS TO THE MACHINE PHASE IN WHICH THEY OCCUR.

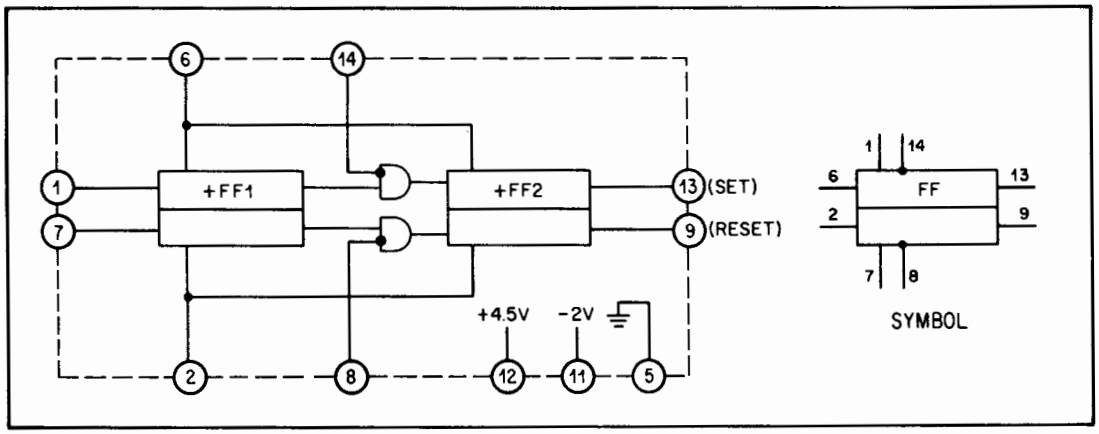


NOTES:

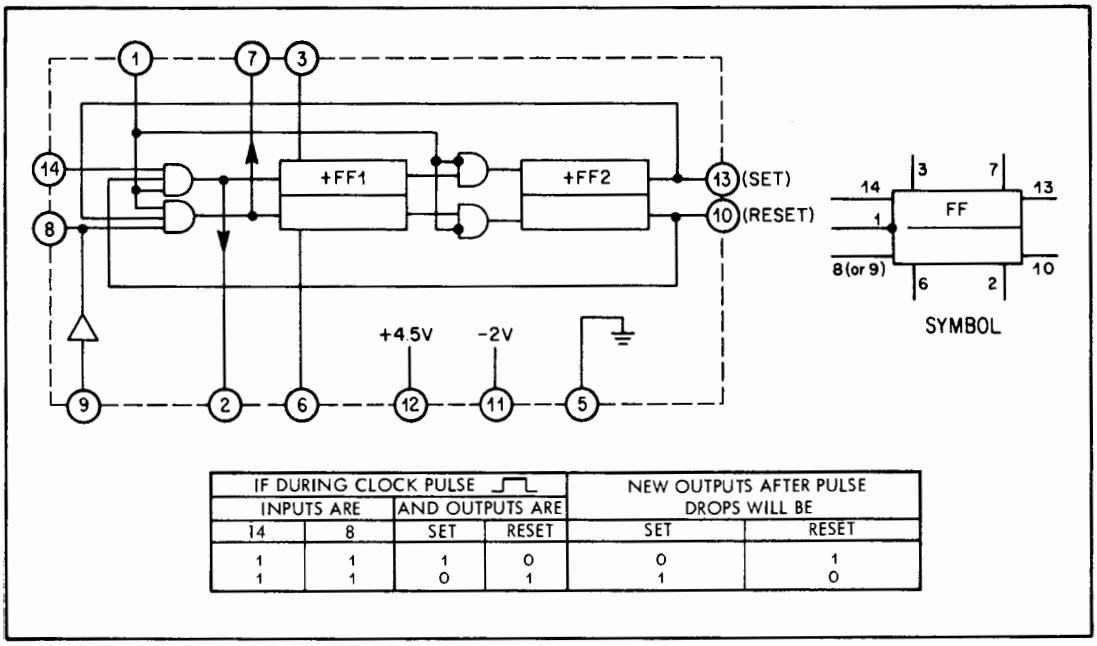
1. PIN 5 ON ALL MICROCIRCUIT PACKAGES IS GROUND.
2. PIN 11 ON ALL MICROCIRCUIT PACKAGES IS −2V ± 5%.
3. PIN 12 ON ALL MICROCIRCUIT PACKAGES IS +4.5V ± 5%.
4. PINS 8 AND 14 OF 1820-0968 ARE CONNECTED TO +4.5V. UNLESS OTHERWISE INDICATED ON A LOGIC DIAGRAM USING THE MICROCIRCUIT PACKAGE.

Logic Diagrams for Microcircuit Packages, Top View

FOR TRAINING PURPOSES ONLY
HP2116B

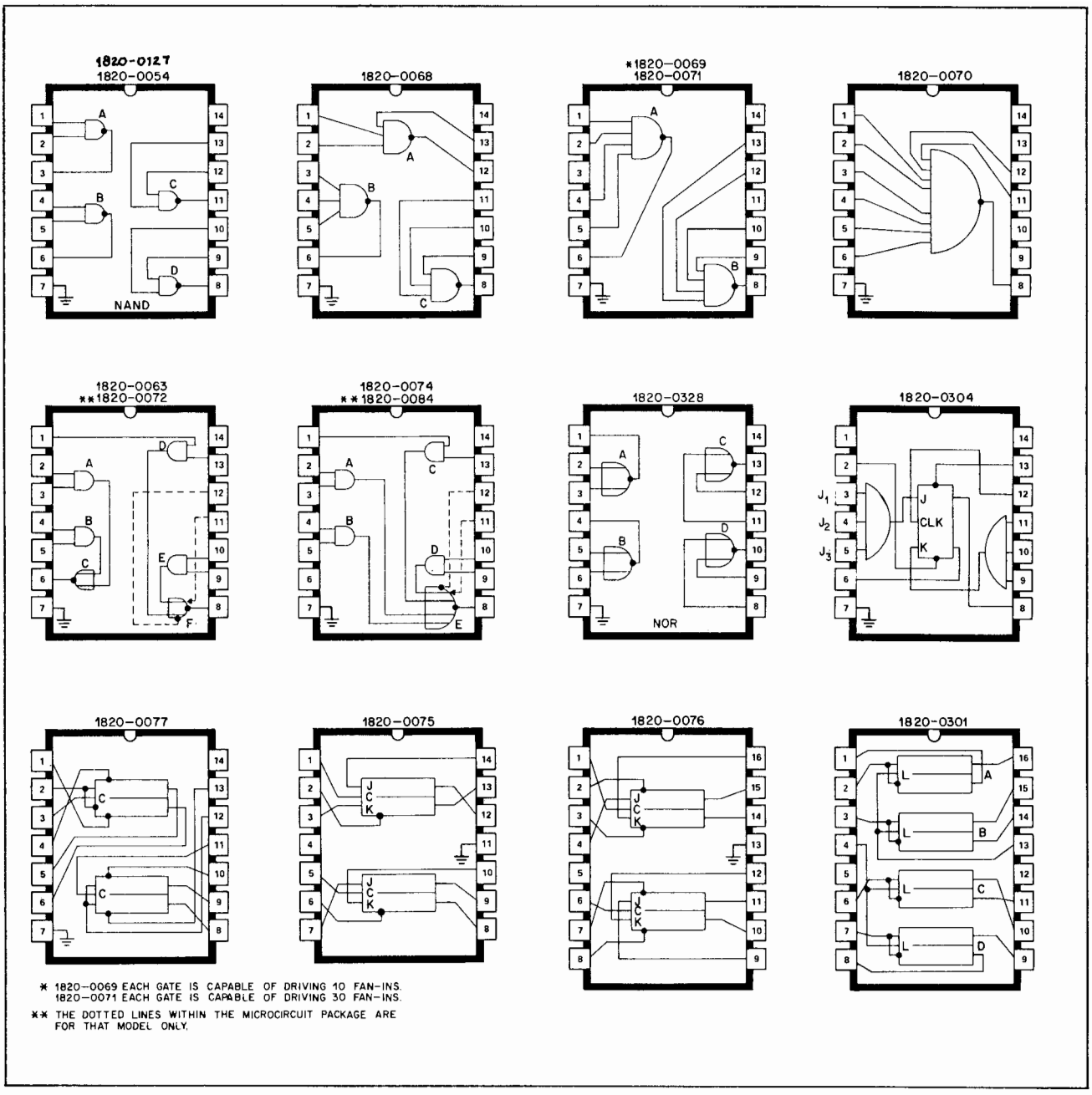


Simplified Logic Diagram of 1820-0957 Microcircuit Package



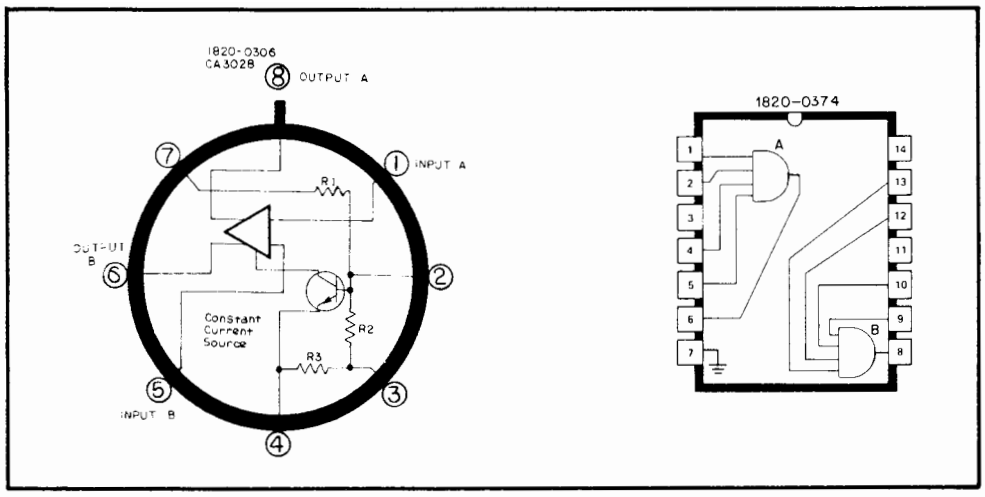
IF DURING CLOCK PULSE ⎍ INPUTS ARE		AND OUTPUTS ARE		NEW OUTPUTS AFTER PULSE DROPS WILL BE	
14	8	SET	RESET	SET	RESET
1	1	1	0	0	1
1	1	0	1	1	0

Simplified Logic Diagram of 1820-0967 Microcircuit Package

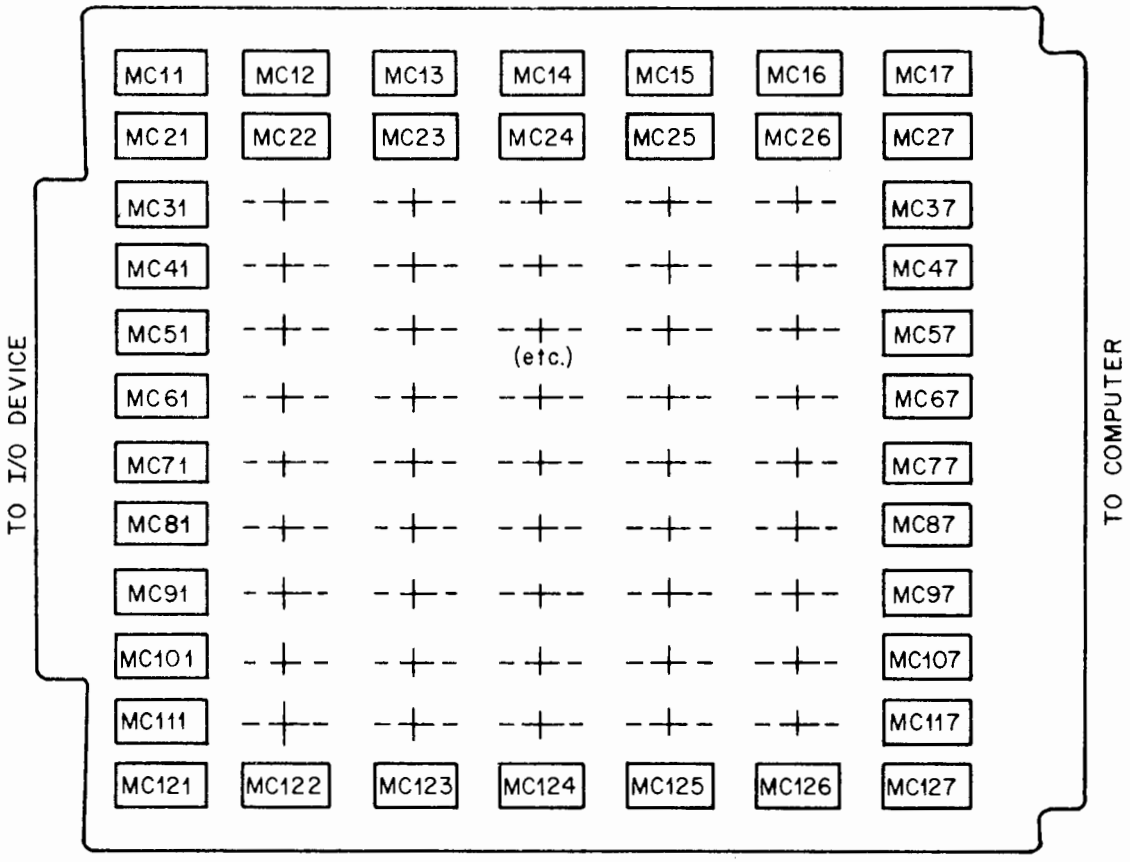


Logic Diagram for Microcircuit Packages, Top View

FOR TRAINING PURPOSES ONLY
HP 2116B

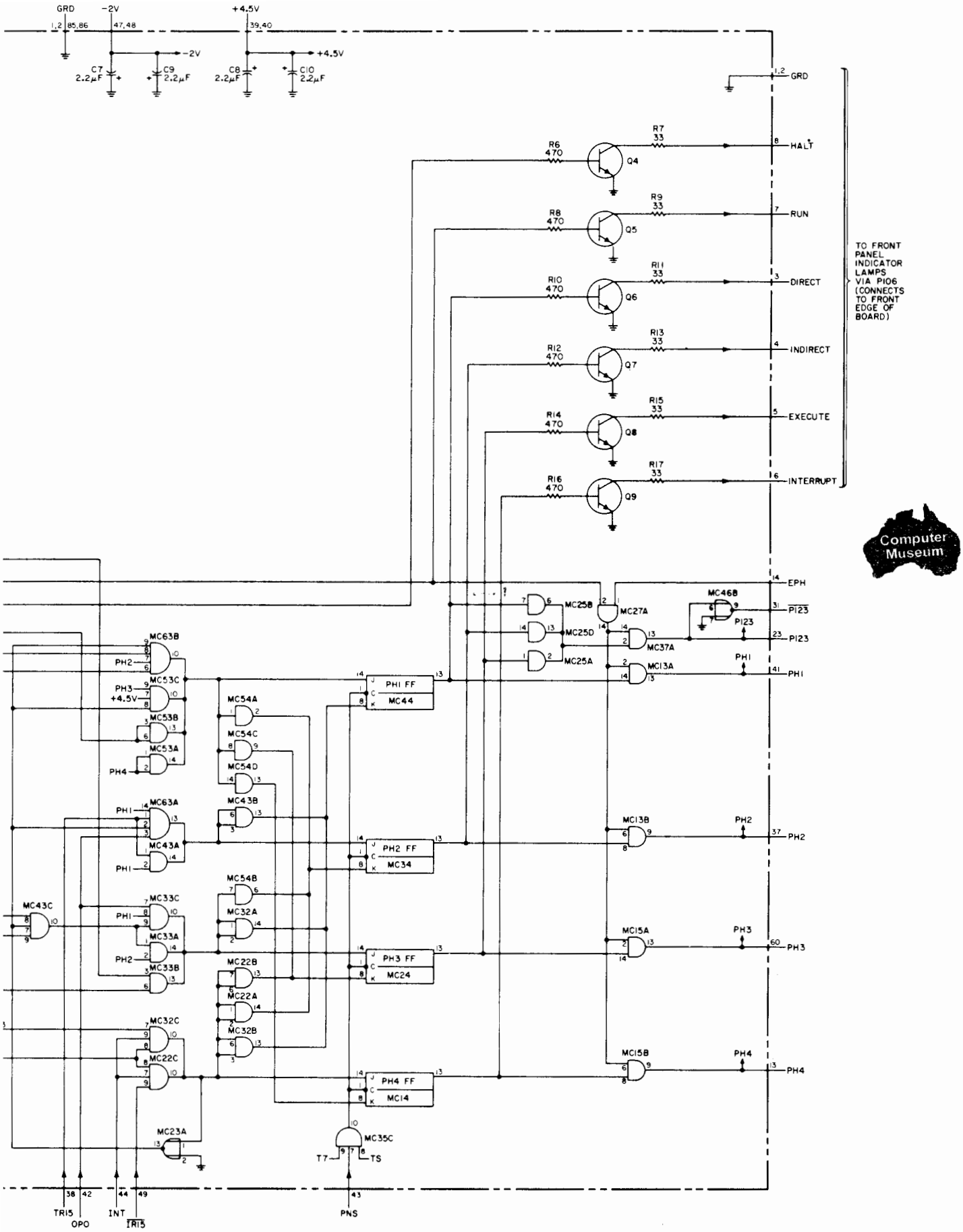


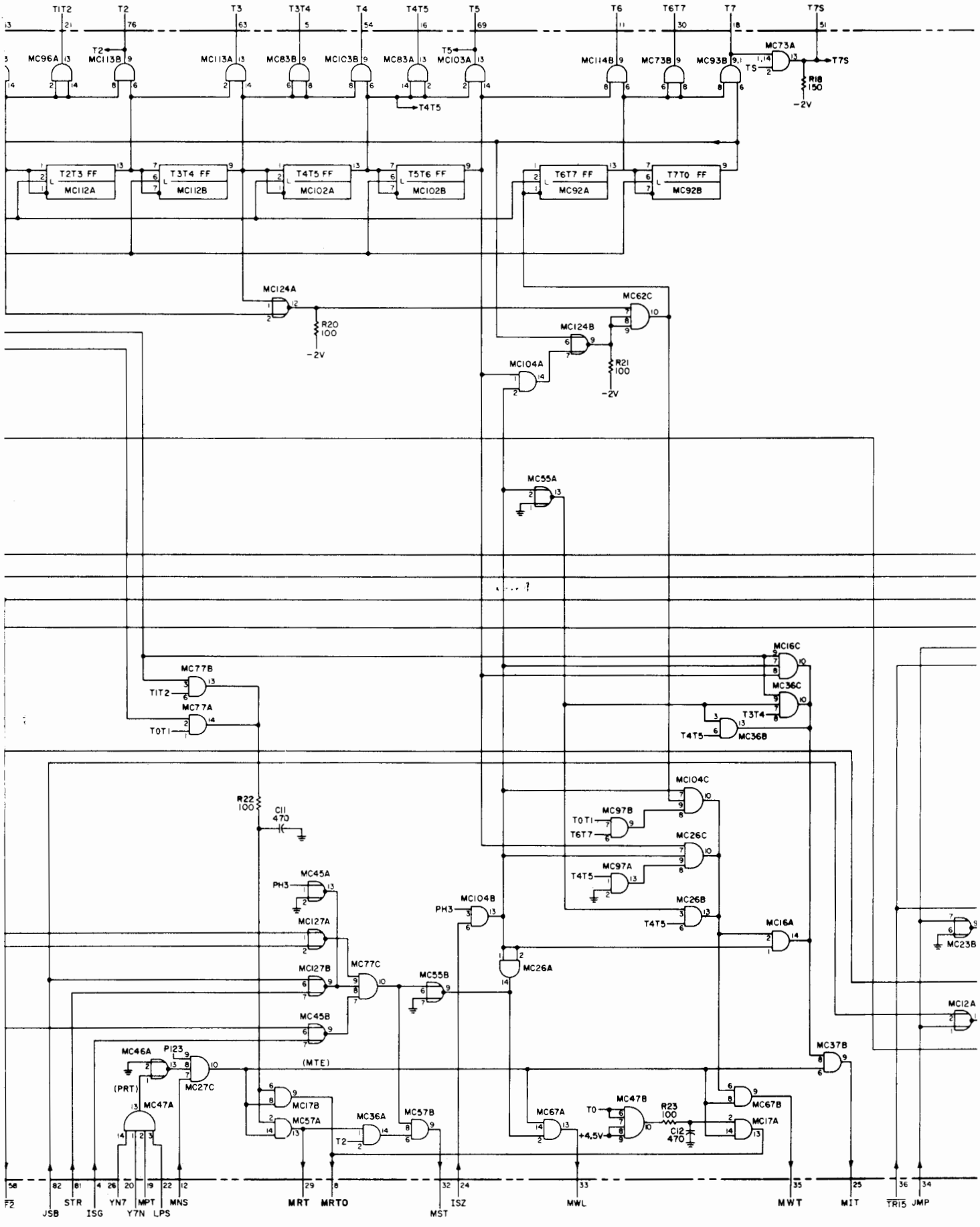
Logic Diagram for Microcircuit Packages 1820-0306 and 1820-0374

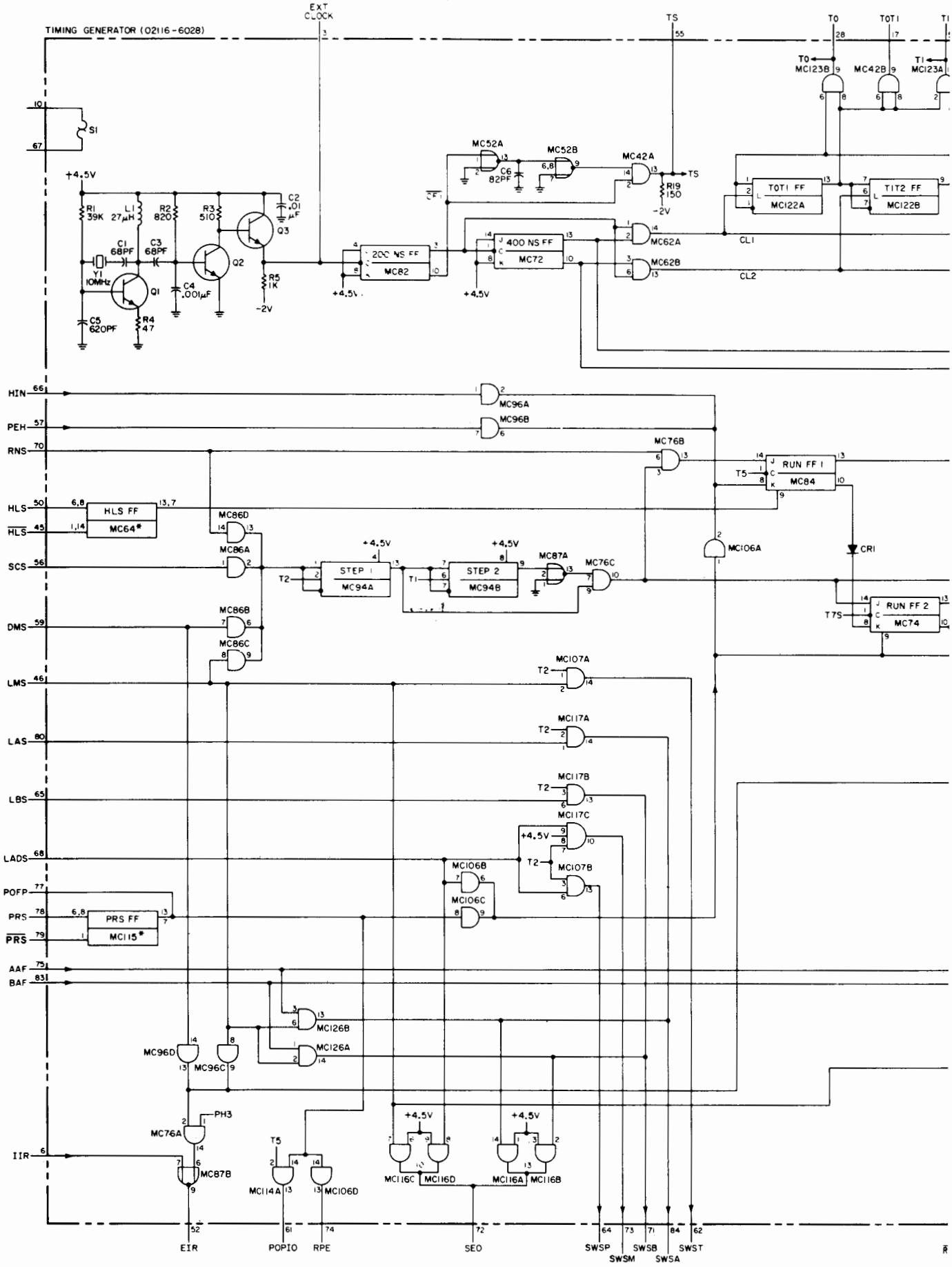


NOTE: A Microcircuit Package always assumes the reference designation assigned to its location on the card as illustrated in this figure.

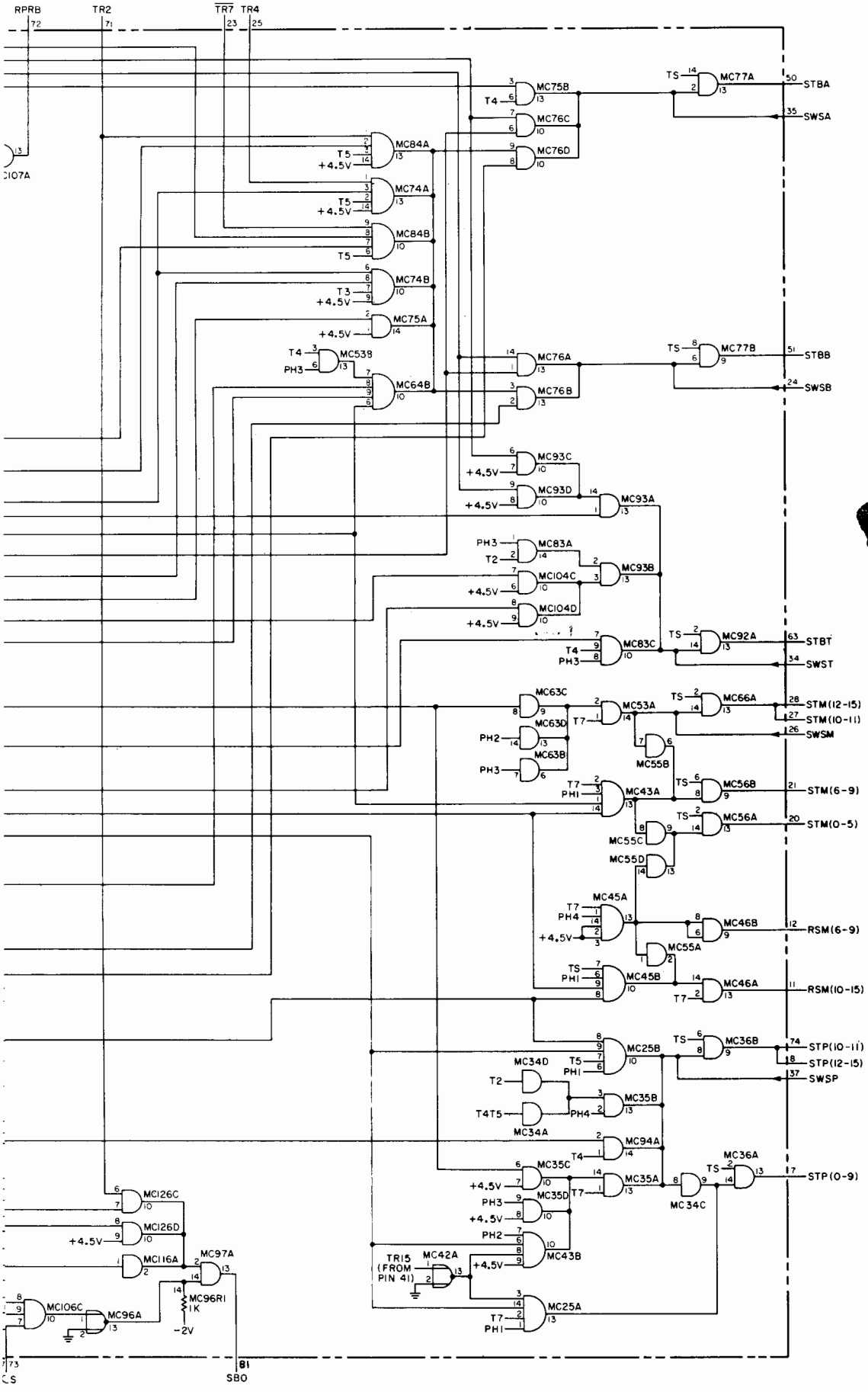
Microcircuit Package Locations




T1T2
T2
T3
T3T4
T4
T4T5
T5
T6
T6T7
T7
T7S
MC96A
MC113B
MC113A
MC83B
MC103B
MC83A
MC103A
MC114B
MC73B
MC93B
MC73A
T2
T5
T4T5
T7S
R18
150
-2V
T2T3 FF
MC112A
T3T4 FF
MC112B
T4T5 FF
MC102A
T5T6 FF
MC102B
T6T7 FF
MC92A
T7T0 FF
MC92B
MC124A
R20
100
-2V
MC62C
MC124B
R21
100
-2V
MC104A
MC55A
MC16C
MC36C
T3T4
T4T5
MC36B
MC77B
T1T2
MC77A
T0T1
R22
100
C11
470
MC104C
MC97B
T0T1
T6T7
MC26C
MC97A
T4T5
MC26B
T4T5
MC16A
MC23B
MC45A
PH3
MC104B
PH3
MC127A
MC127B
MC77C
MC55B
MC26A
MC45B
MC12A
MC37B
MC46A
P123
(MTE)
(PRT)
MC27C
MC47A
MC67B
MC17B
MC57A
MC36A
MC57B
MC67A
T0
MC47B
R23
100
C12
470
+4.5V
MC17A
T2
F2
JSB
STR
ISG
YN7
Y7N
MPT
LPS
MNS
MRT
MRTO
MST
ISZ
MWL
MWT
MIT
TRIS
JMP

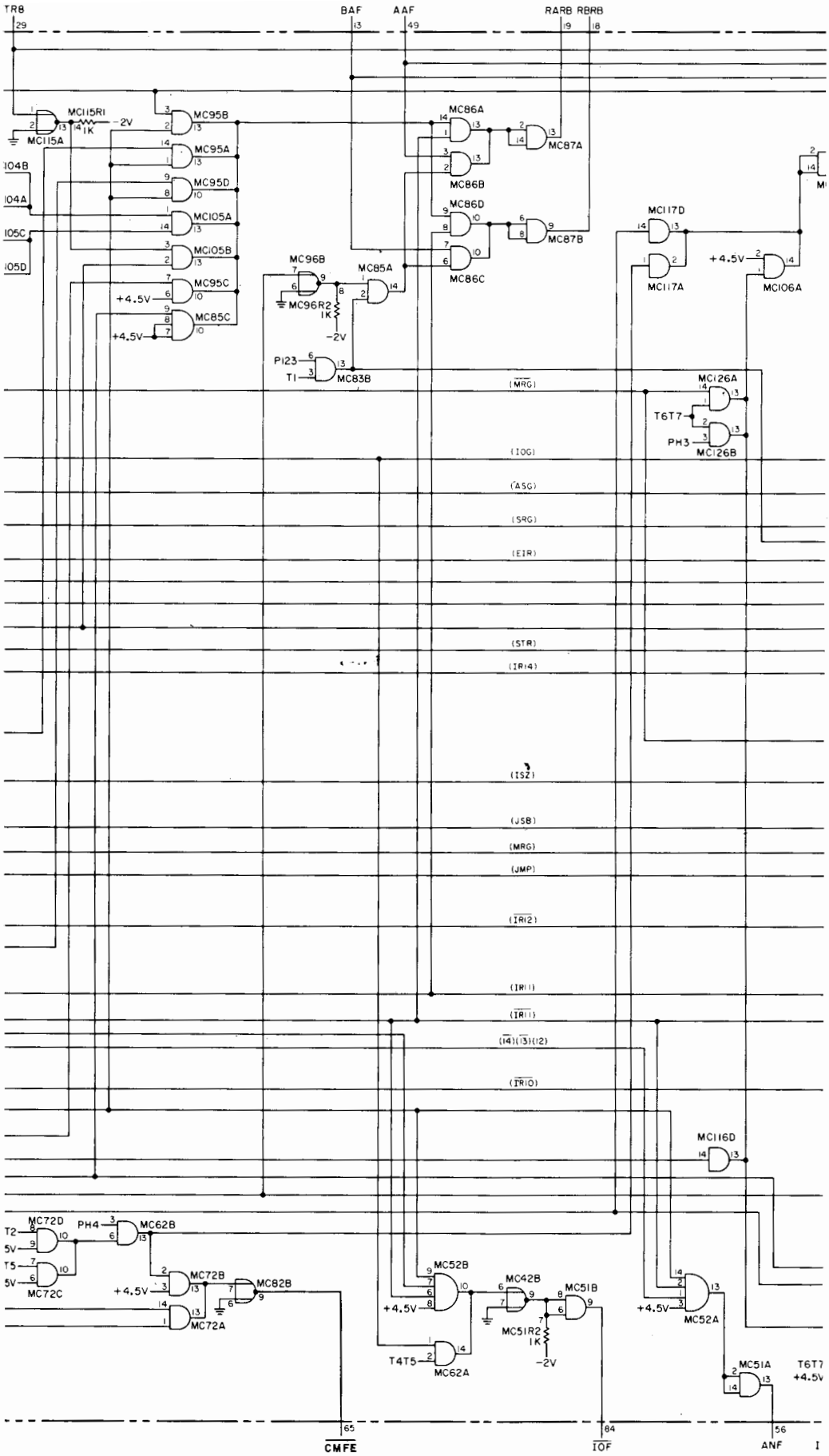


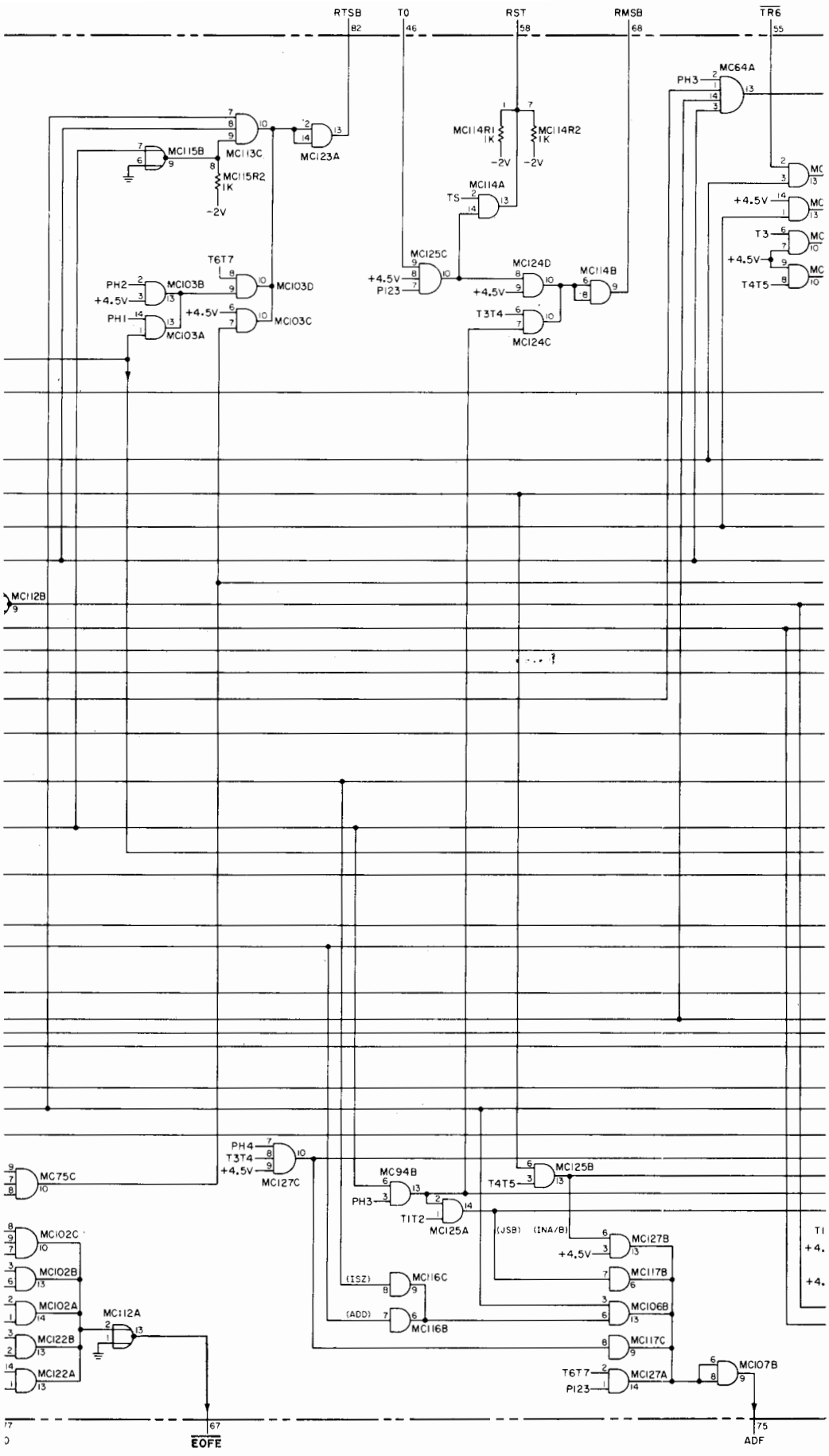
CHANGE	REFERENCE	REVISION/PREFIX

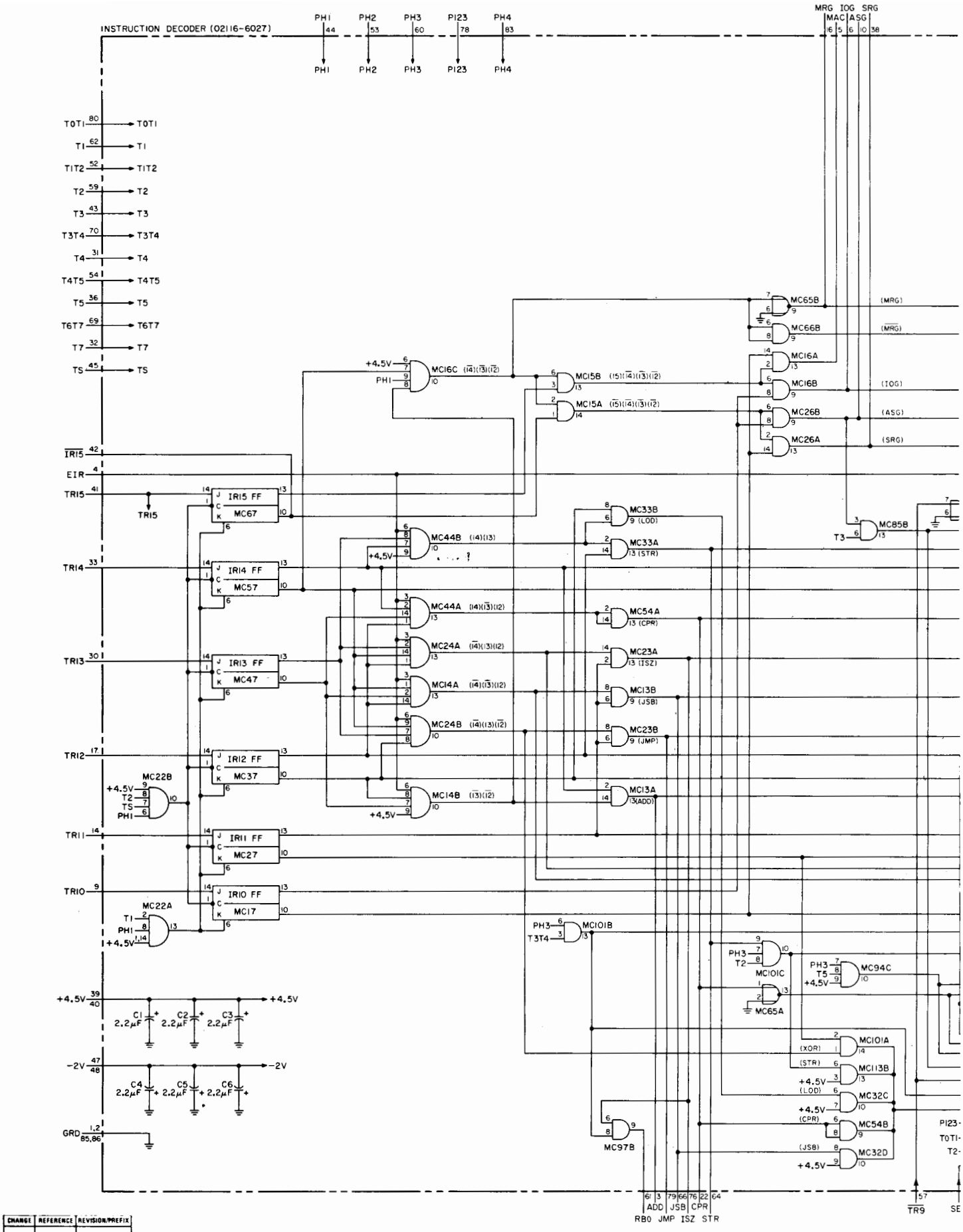


Instruction Decoder
HP 2115A

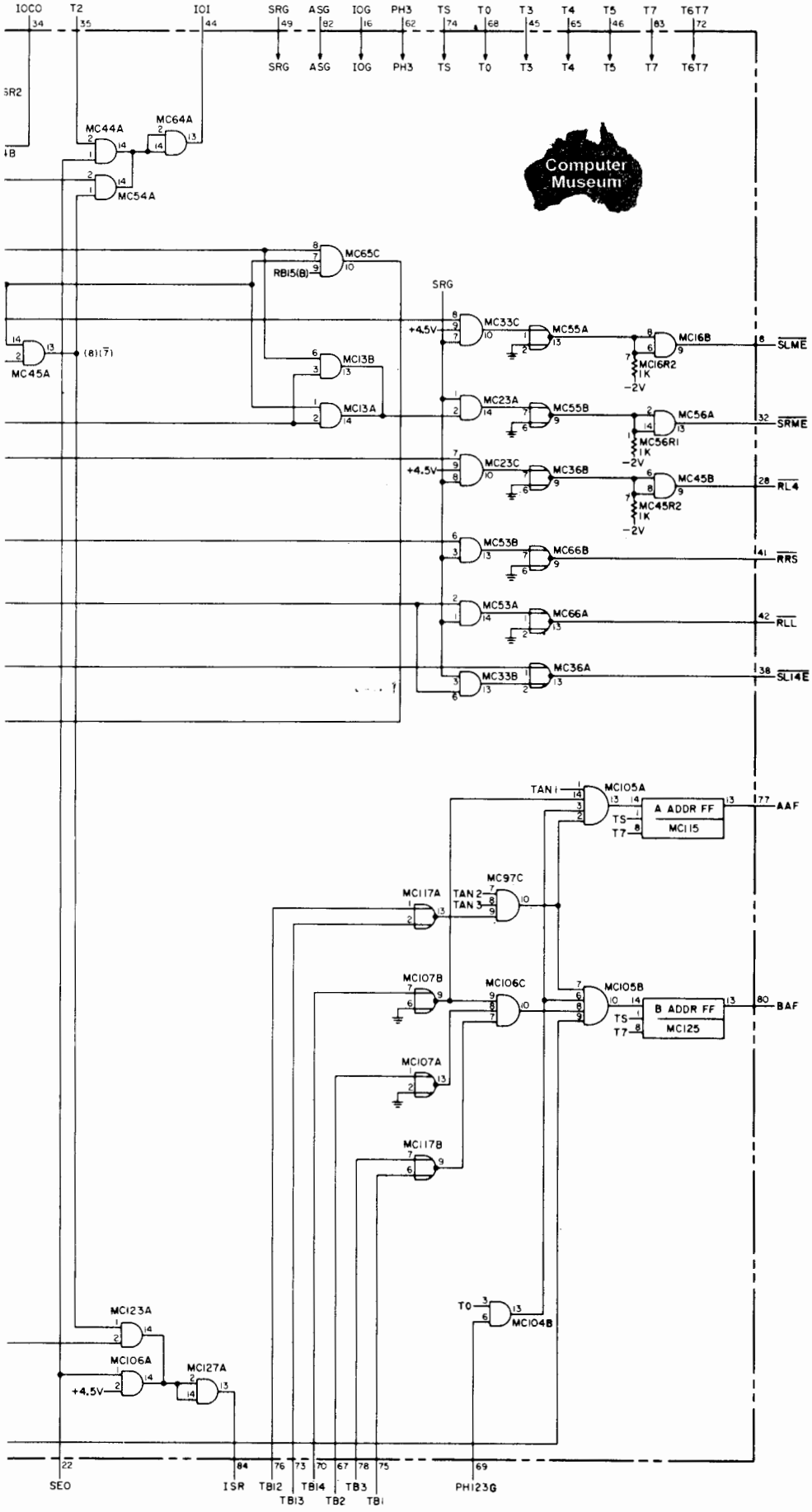
FOR TRAINING PURPOSES ONLY


TR8
29
BAF
13
AAF
49
RARB
19
RBRB
18
MC115A
MC115R1
1K
-2V
MC95B
MC95A
MC95D
MC105A
MC105B
MC95C
MC85C
+4.5V
+4.5V
104B
104A
105C
105D
MC86A
MC86B
MC87A
MC86D
MC86C
MC87B
MC96B
MC96R2
1K
-2V
MC85A
P123
T1
MC83B
MC117D
MC117A
+4.5V
MC106A
(MRG)
MC126A
T6T7
PH3
MC126B
(IOG)
(ASG)
(SRG)
(EIR)
(STR)
(IR14)
(ISZ)
(JSB)
(MRG)
(JMP)
(IR12)
(IR11)
(IR11)
(14)(13)(12)
(IR10)
MC116D
T2
5V
T5
5V
MC72D
MC72C
PH4
MC62B
MC72B
+4.5V
MC72A
MC82B
MC52B
+4.5V
T4T5
MC62A
MC42B
MC51B
MC51R2
1K
-2V
+4.5V
MC52A
MC51A
T6T7
+4.5V
65
CMFE
64
IOF
56
ANF
I


RTSB
82
T0
46
RST
58
RMSB
68
TR6
55
MC64A
PH3
MC114R1
1K
MC114R2
1K
-2V
-2V
MC114A
TS
MC115B
MC113C
MC115R2
1K
-2V
MC123A
T6T7
PH2
MC103B
+4.5V
MC103D
PH1
+4.5V
MC103A
MC103C
MC125C
+4.5V
P123
MC124D
+4.5V
T3T4
MC124C
MC114B
+4.5V
T3
+4.5V
T4T5
MC112B
9
PH4
T3T4
+4.5V
MC127C
MC75C
MC94B
PH3
T1T2
MC125A
T4T5
MC125B
(JSB)
(INA/B)
MC127B
+4.5V
MC117B
MC102C
MC102B
MC102A
MC122B
MC122A
MC112A
(ISZ)
MC116C
(ADD)
MC116B
MC106B
MC117C
T6T7
P123
MC127A
MC107B
77
0
67
EOFE
75
ADF

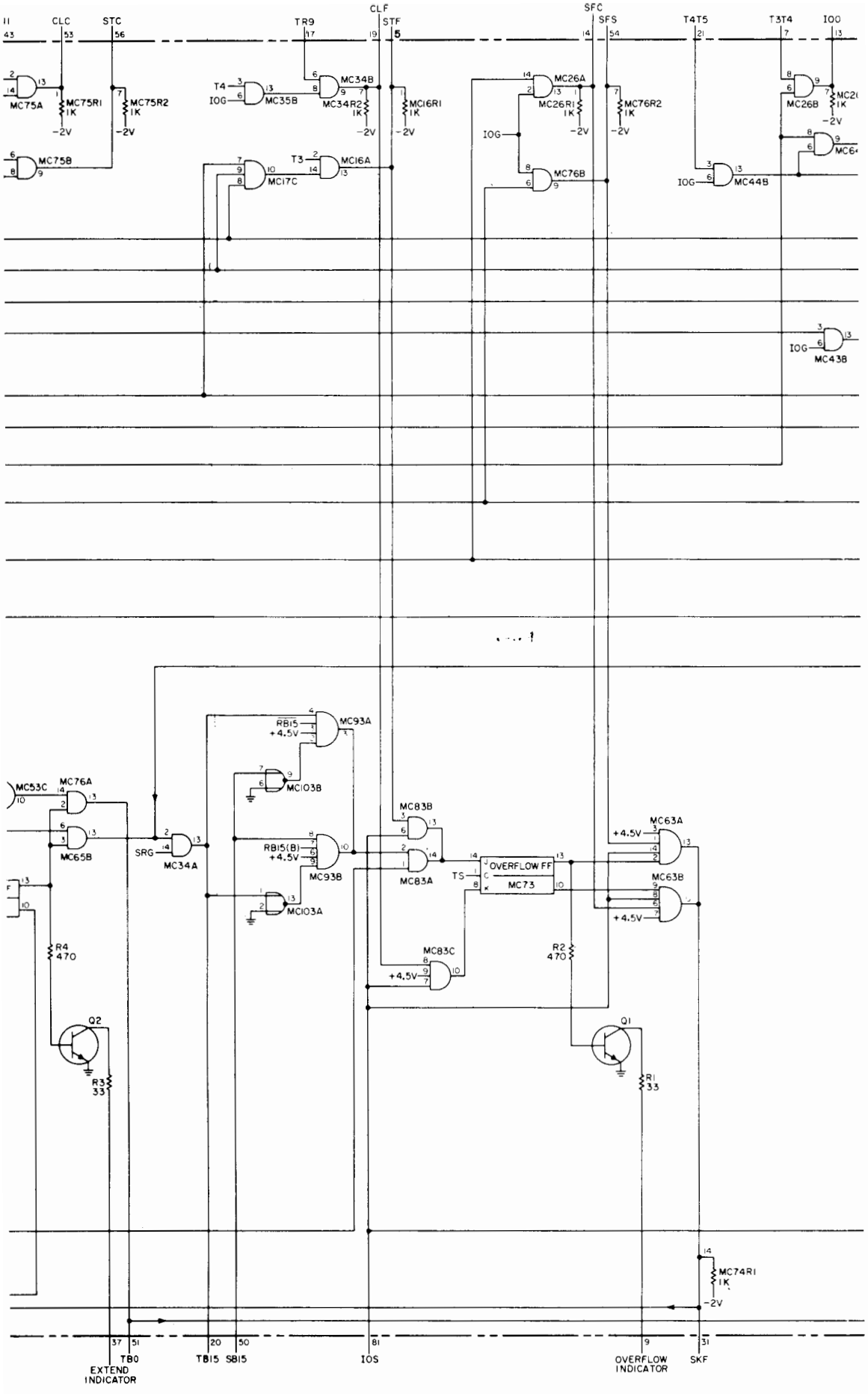


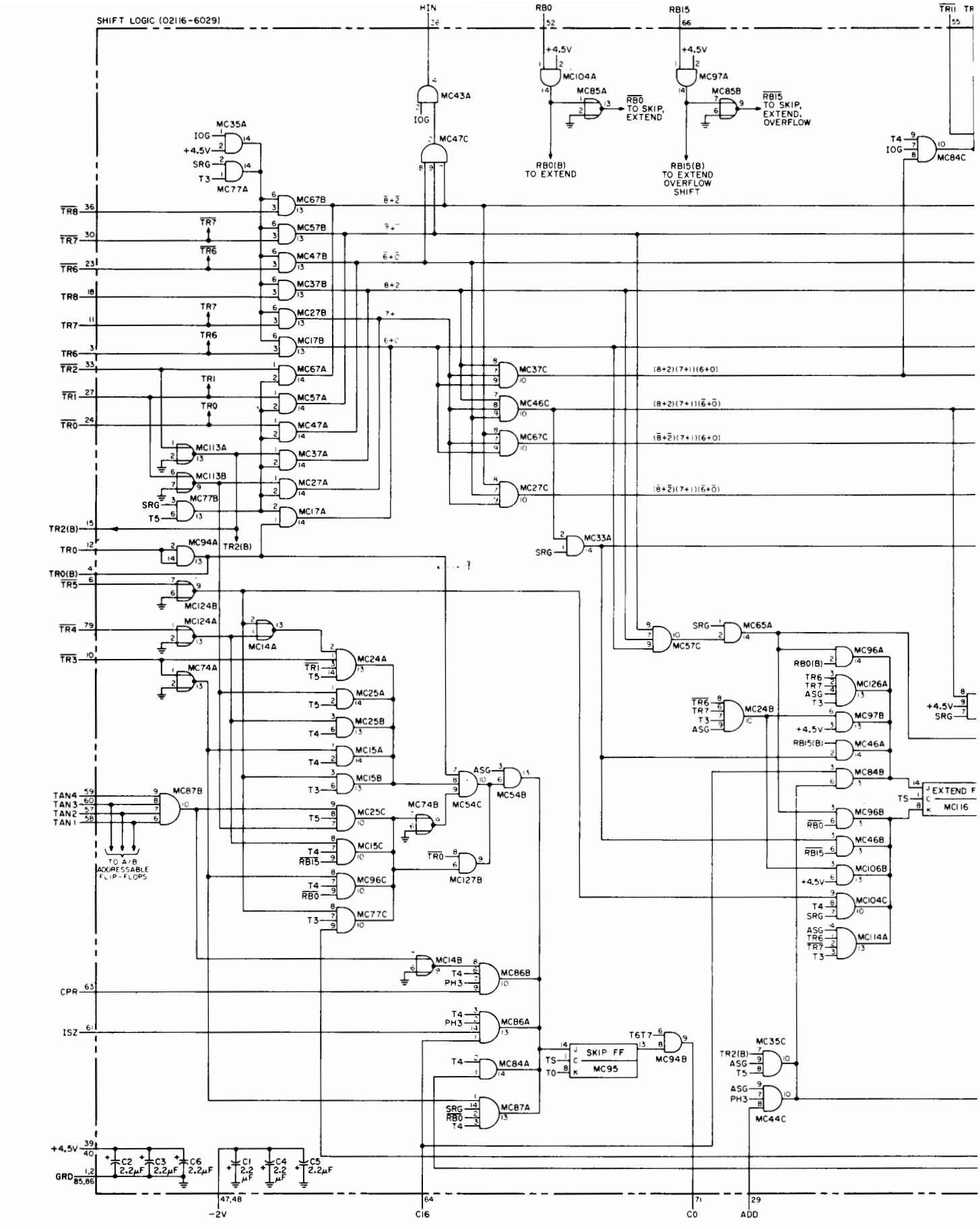
CHANGE	REFERENCE	REVISION/PREFIX



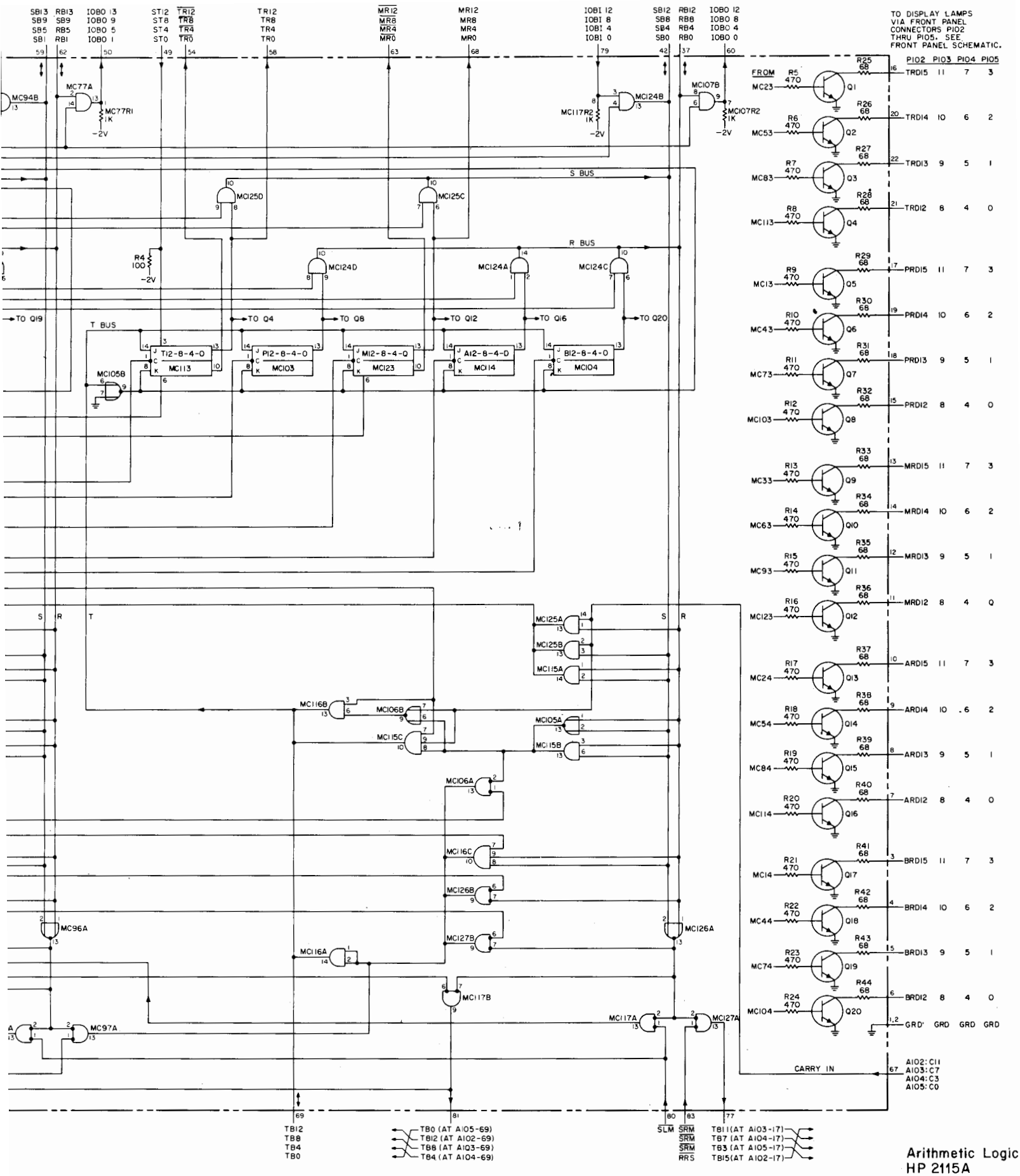
Shift Logic
HP 2115A

FOR TRAINING PURPOSES ONLY


CLC
STC
CLF
STF
SFC
SFS
T4T5
T3T4
IOO
TR9
MC75A
MC75R1 1K
MC75R2 1K
MC75B
MC34B
MC34R2 1K
MC35B
MC16R1 1K
MC17C
MC16A
MC26A
MC26R1 1K
MC76R2 1K
MC76B
MC44B
MC26B
MC43B
-2V
IOG
T4
T3
RB15 +4.5V
MC93A
MC103B
MC83B
MC83A
MC83C
MC53C
MC76A
MC65B
SRG
MC34A
RB15(B) +4.5V
MC93B
MC103A
OVERFLOW FF
MC73
TS
MC63A
MC63B
+4.5V
R4 470
R2 470
R3 33
R1 33
Q2
Q1
MC74R1 1K
TB0
EXTEND INDICATOR
TB15
SB15
IOS
OVERFLOW INDICATOR
SKF

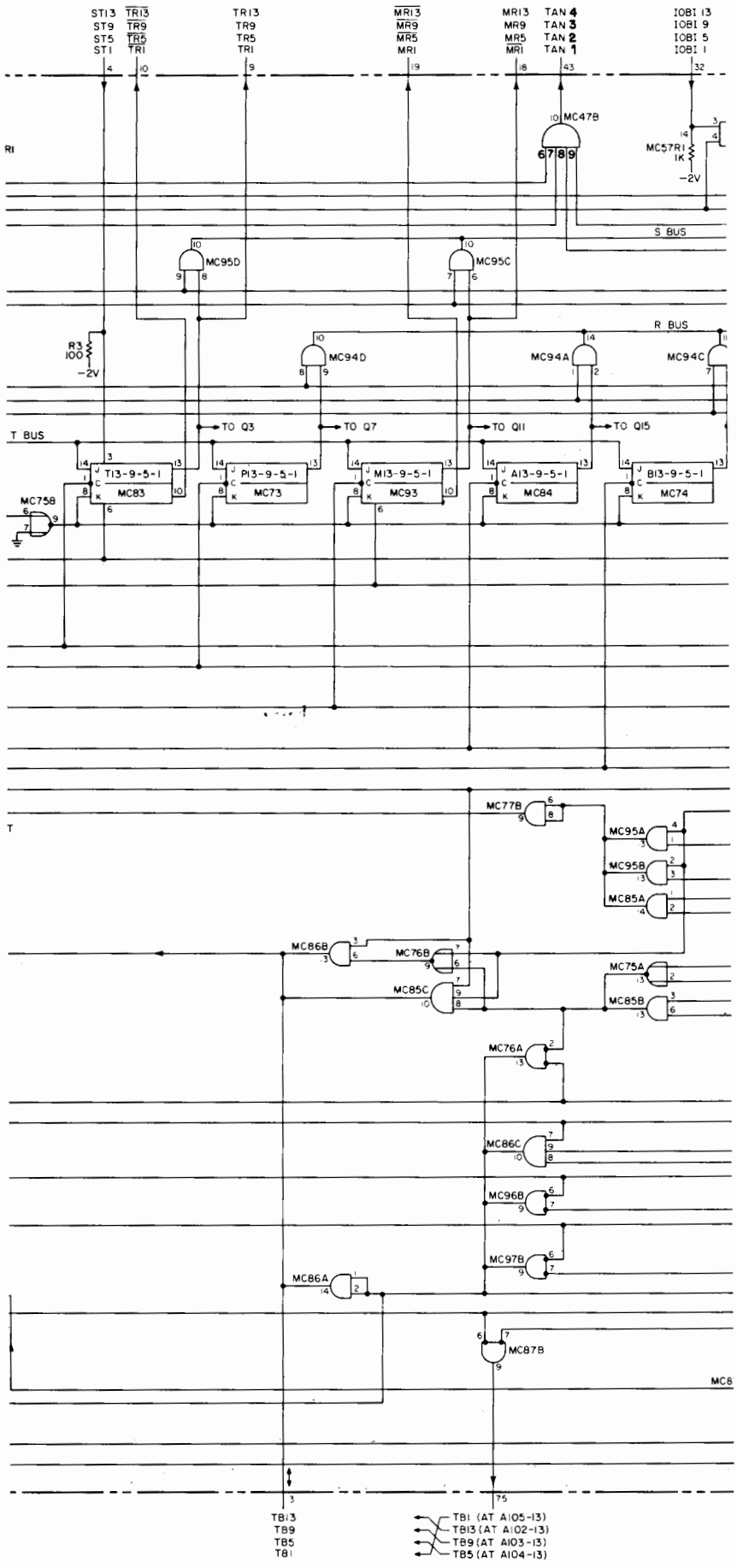


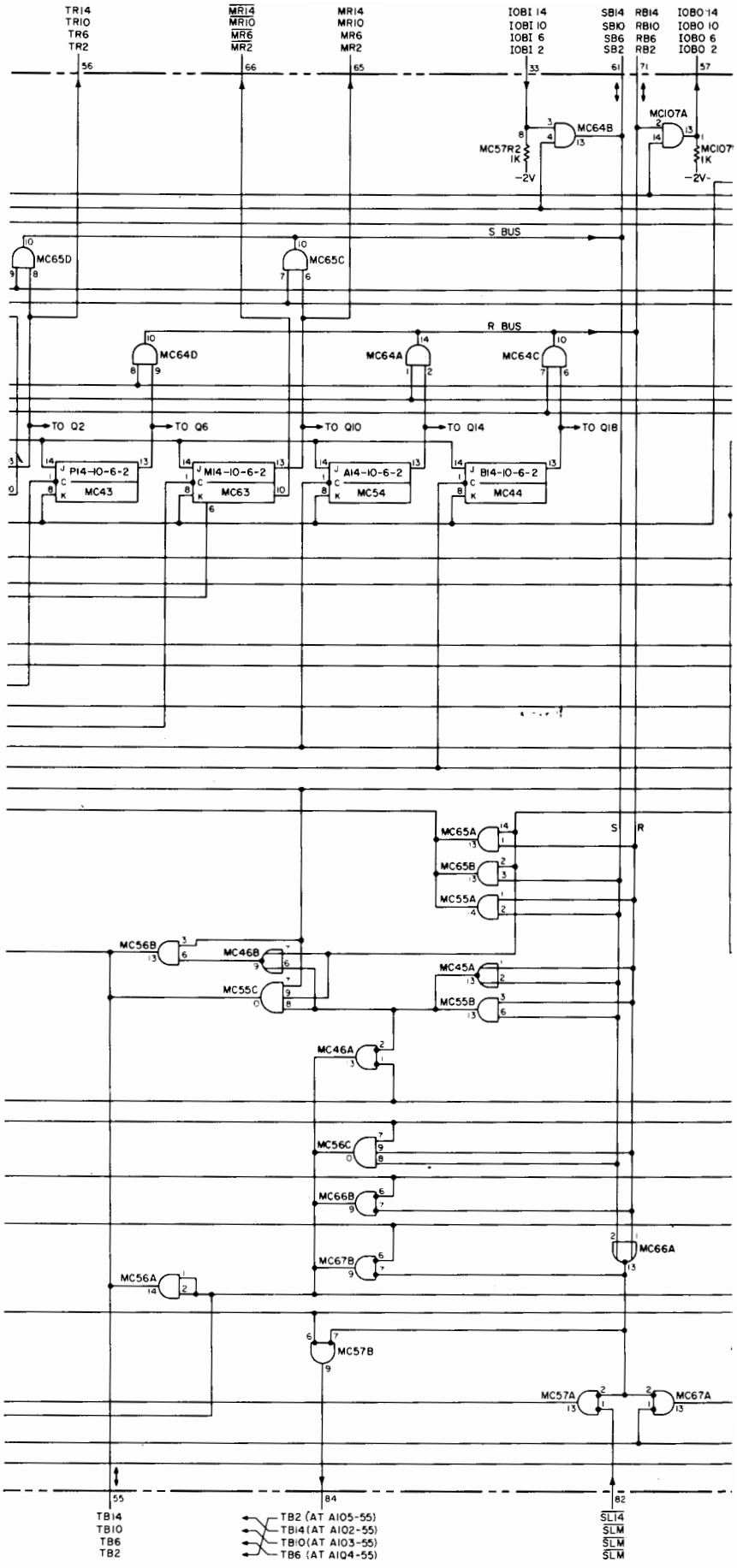
CHANGE	REFERENCE	REVISION/PREFIX

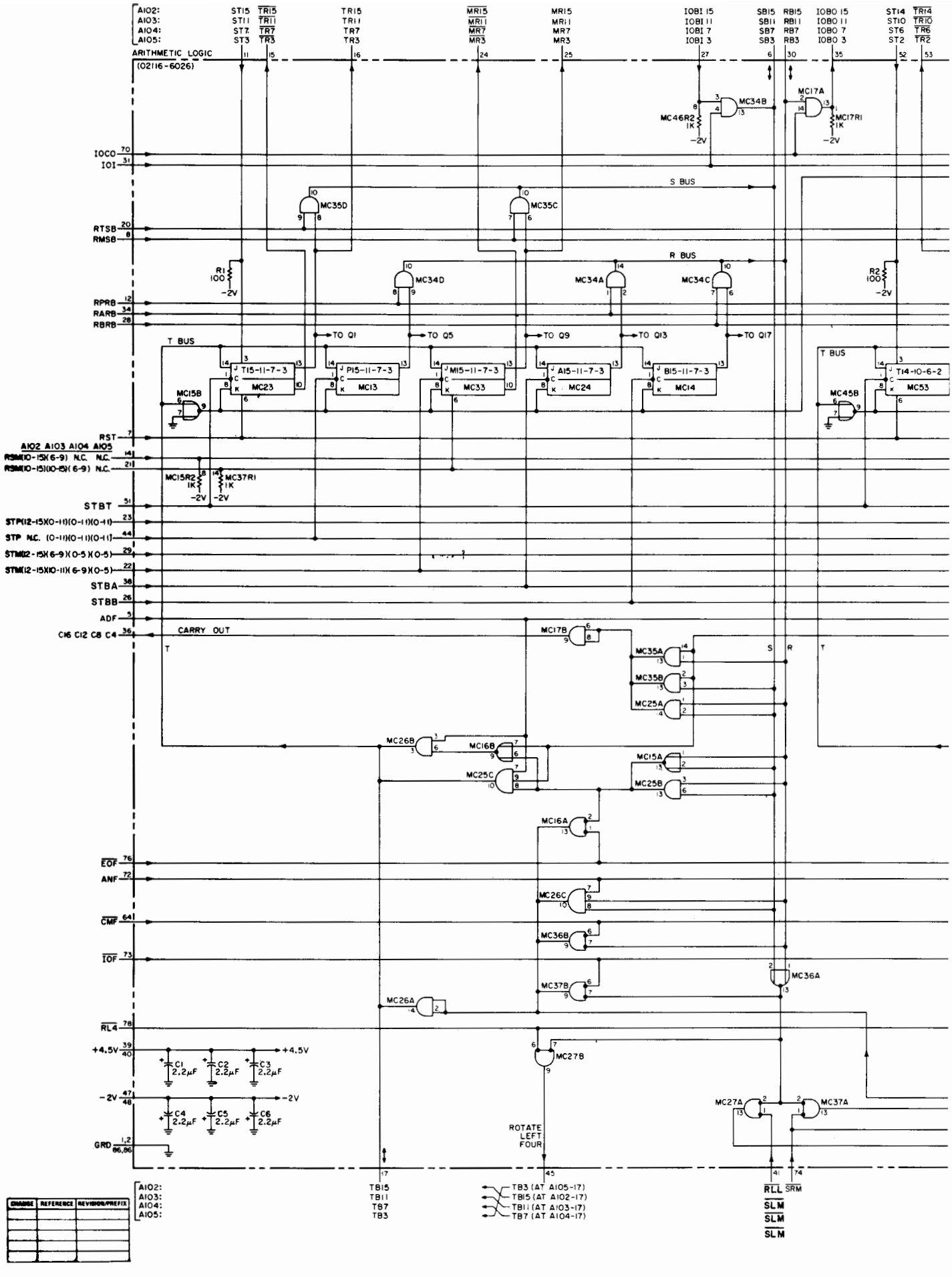


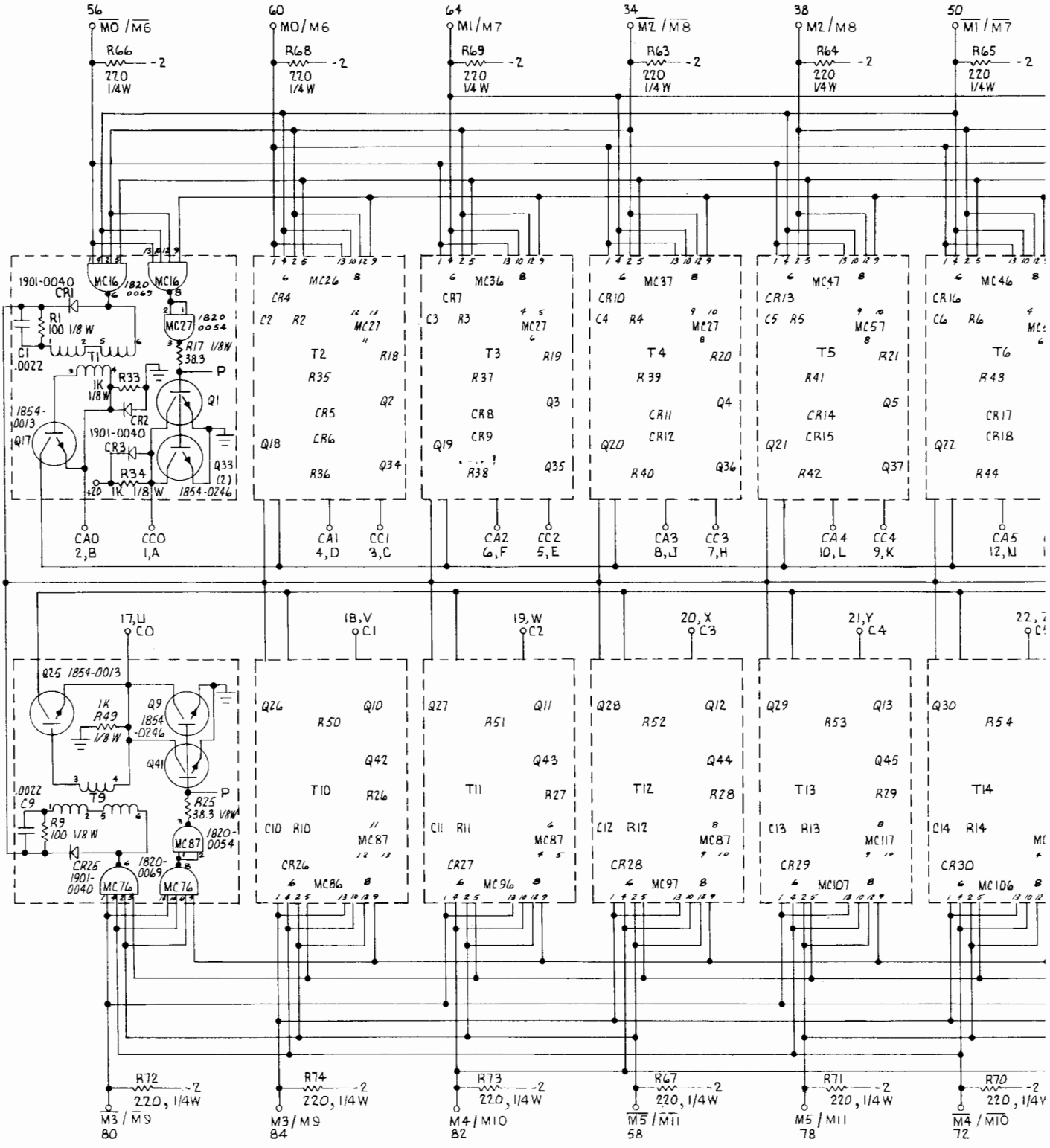
Arithmetic Logic
HP 2115A

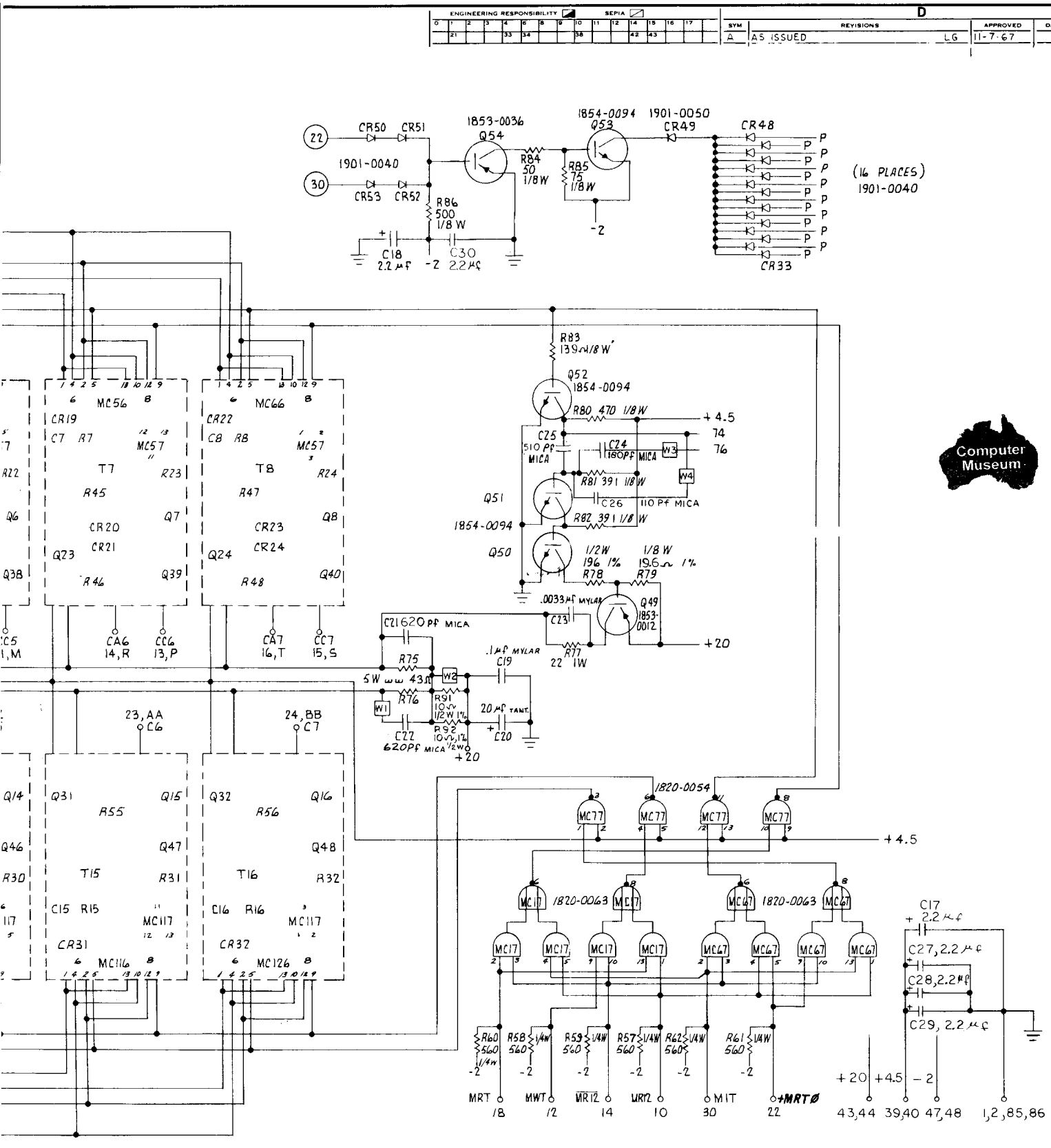
FOR TRAINING PURPOSES ONLY


ST13 TR13
ST9 TR9
ST5 TR5
ST1 TR1
TR13
TR9
TR5
TR1
MR13
MR9
MR5
MR1
TAN 4
TAN 3
TAN 2
TAN 1
IOBI 13
IOBI 9
IOBI 5
IOBI 1
MC47B
6 7 8 9
MC57R1
1K
−2V
RI
S BUS
MC95D
MC95C
R BUS
R3
100
−2V
MC94D
MC94A
MC94C
T BUS
TO Q3
TO Q7
TO Q11
TO Q15
T13-9-5-1
MC83
P13-9-5-1
MC73
M13-9-5-1
MC93
A13-9-5-1
MC84
B13-9-5-1
MC74
MC75B
T
MC77B
MC95A
MC95B
MC85A
MC86B
MC76B
MC85C
MC75A
MC85B
MC76A
MC86C
MC96B
MC97B
MC86A
MC87B
MC8
TB13
TB9
TB5
TB1
TB1 (AT A105-13)
TB13 (AT A102-13)
TB9 (AT A103-13)
TB5 (AT A104-13)


TR14
TR10
TR6
TR2
56
MR14
MR10
MR6
MR2
66
MR14
MR10
MR6
MR2
65
IOBI 14
IOBI 10
IOBI 6
IOBI 2
33
SBI4
SBI0
SB6
SB2
61
RBI4
RBI0
RB6
RB2
71
IOBO 14
IOBO 10
IOBO 6
IOBO 2
57
MC64B
MC57R2
1K
-2V
MC107A
MC107
1K
-2V
S BUS
MC65D
MC65C
R BUS
MC64D
MC64A
MC64C
TO Q2
TO Q6
TO Q10
TO Q14
TO Q18
P14-10-6-2
MC43
M14-10-6-2
MC63
A14-10-6-2
MC54
B14-10-6-2
MC44
MC65A
MC65B
MC55A
S
R
MC56B
MC46B
MC55C
MC45A
MC55B
MC46A
MC56C
MC66B
MC67B
MC66A
MC56A
MC57B
MC57A
MC67A
55
84
82
TB14
TB10
TB6
TB2
TB2 (AT A105-55)
TBI4 (AT A102-55)
TBI0 (AT A103-55)
TB6 (AT A104-55)
SLI4
SLM
SLM
SLM


ARITHMETIC LOGIC
(02116-6026)
S BUS
R BUS
T BUS
CARRY OUT
ROTATE LEFT FOUR
MC34B
MC17A
MC17R1 1K
MC46R2 1K
MC35D
MC35C
MC34D
MC34A
MC34C
R1 100
R2 100
-2V
TO Q1
TO Q5
TO Q9
TO Q13
TO Q17
MC23
MC13
MC33
MC24
MC14
MC53
MC15B
MC45B
MC15R2 1K
MC37R1 1K
MC17B
MC35A
MC35B
MC25A
MC26B
MC16B
MC25C
MC15A
MC25B
MC16A
MC26C
MC36B
MC37B
MC36A
MC26A
MC27B
MC27A
MC37A
C1 2.2μF
C2 2.2μF
C3 2.2μF
C4 2.2μF
C5 2.2μF
C6 2.2μF
+4.5V
-2V
GRD
IOCO
IOI
RTSB
RMSB
RPRB
RARB
RBRB
RST
STBT
STBA
STBB
ADF
C16 C12 C8 C4
EOF
ANF
CMF
IOF
RL4
A102 A103 A104 A105
TB15
TB11
TB7
TB3
TB3 (AT A105-17)
TB15 (AT A102-17)
TB11 (AT A103-17)
TB7 (AT A104-17)
RLL
SLM
SRM


56
M0 / M6
R66
220
1/4W
60
M0 / M6
R68
220
1/4W
64
M1 / M7
R69
220
1/4W
34
M2 / M8
R63
220
1/4W
38
M2 / M8
R64
220
1/4W
50
M1 / M7
R65
220
1/4W
1901-0040
CR1
MC16
1820 0069
MC27
1820 0054
R1
100 1/8W
C1
.0022
T1
R17 1/8W
38.3
P
R33
1K
1/8W
Q1
1854-0013
Q17
CR2
1901-0040
CR3
Q2
Q33 (2)
R34
1K 1/8W
1854-0246
CA0
2,B
CC0
1,A
CA1
4,D
CC1
3,C
CA2
6,F
CC2
5,E
CA3
8,J
CC3
7,H
CA4
10,L
CC4
9,K
CA5
12,M
17,U
C0
18,V
C1
19,W
C2
20,X
C3
21,Y
C4
Q25 1854-0013
1K
R49
1/8W
Q9
1854-0246
Q41
.0022
C9
T9
R9
100 1/8W
R25
38.3 1/8W
MC87
1820-0054
CR25
1901-0040
MC76
1820-0069
R72
220, 1/4W
M3 / M9
80
R74
220, 1/4W
M3 / M9
84
R73
220, 1/4W
M4 / M10
82
R67
220, 1/4W
M5 / M11
58
R71
220, 1/4W
M5 / M11
78
R70
220, 1/4W
M4 / M10
72

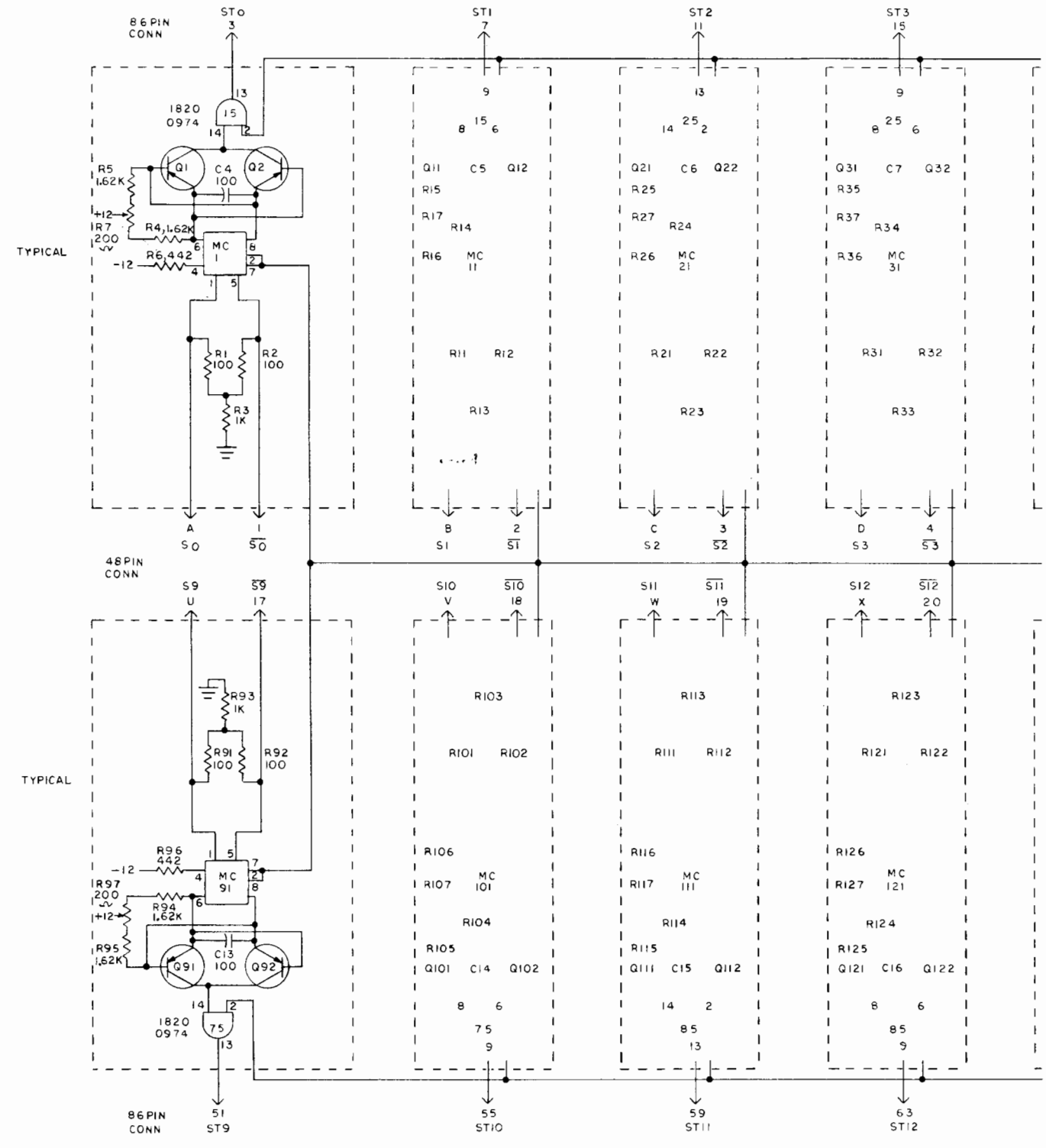


NOTE:
TRANSFORMERS - 11EHA

Driver Switch
HP 2115A

FOR TRAINING PURPOSES ONLY

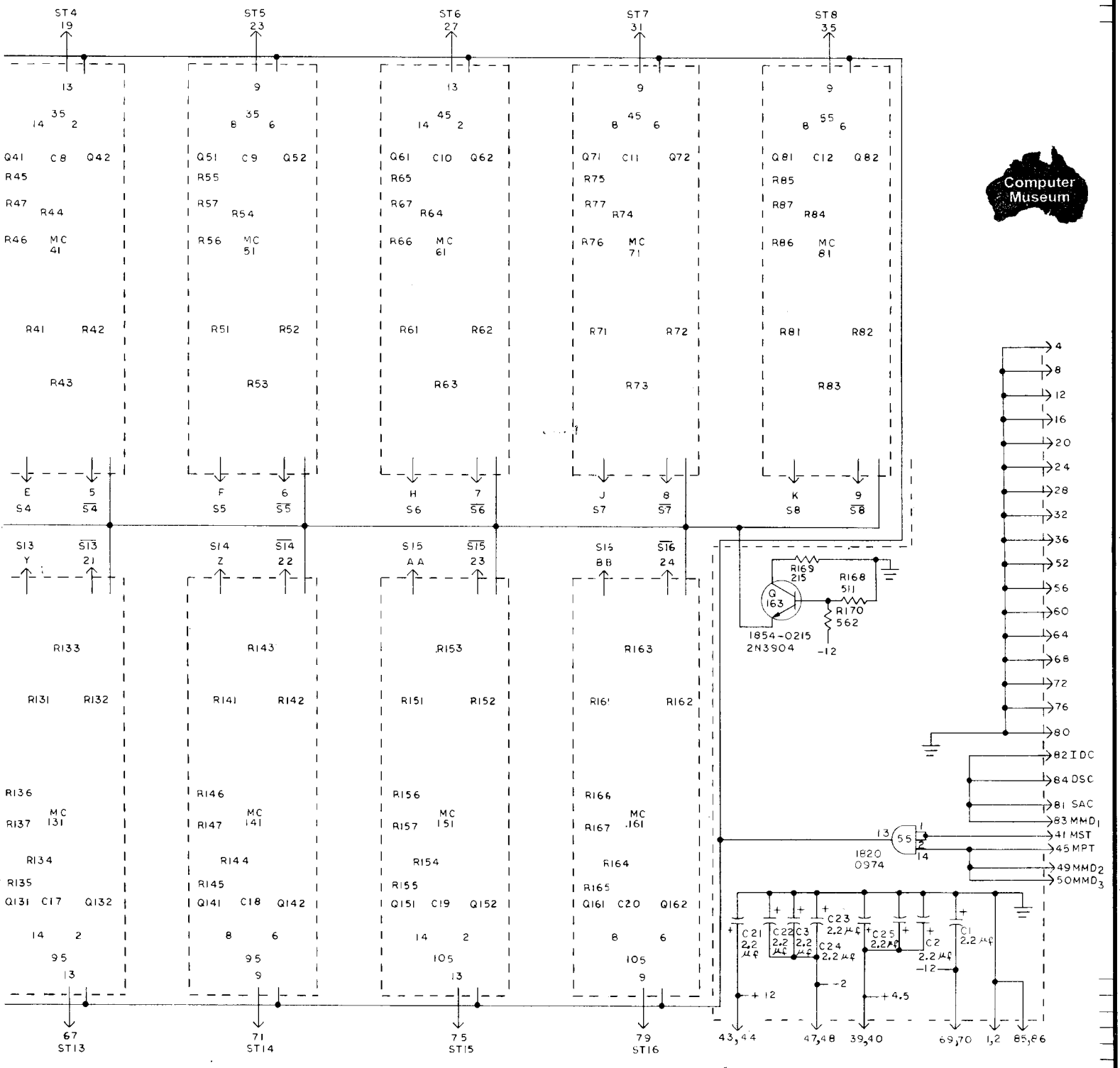
SHEET OF



NOTE
UNLESS OTHERWISE NOTED
ALL INTEGRATED CKTS ARE 1820-0306
ALL TRANSISTORS ARE 1853-0036
ALL RESISTORS 1/8W 1% MF

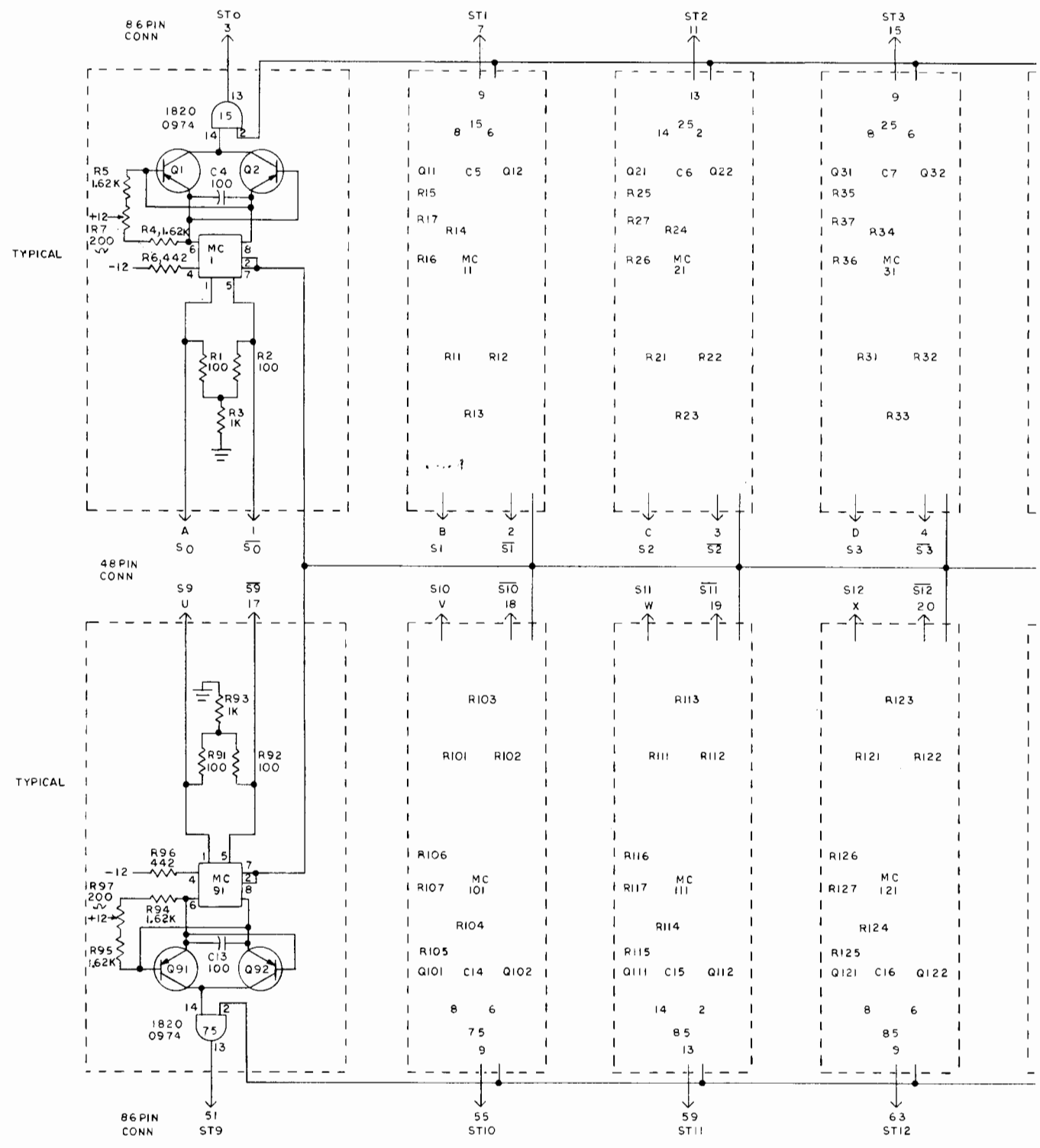
(15) REF DES (MC15)

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A B	REVISED PIN CONN LE ADDED C4-25, Q3, 17 EMITTER RES. R167-169 REVISED PIN CONN LG	6-13-67 9-12-67	
C	ADDED 17 VARIABLE RES LG AND MRT CIRCUIT	10-13-67	
D	REMOVED MRT CIRCUIT LG	10-31-67	



Sense Amplifier
HP 2115A

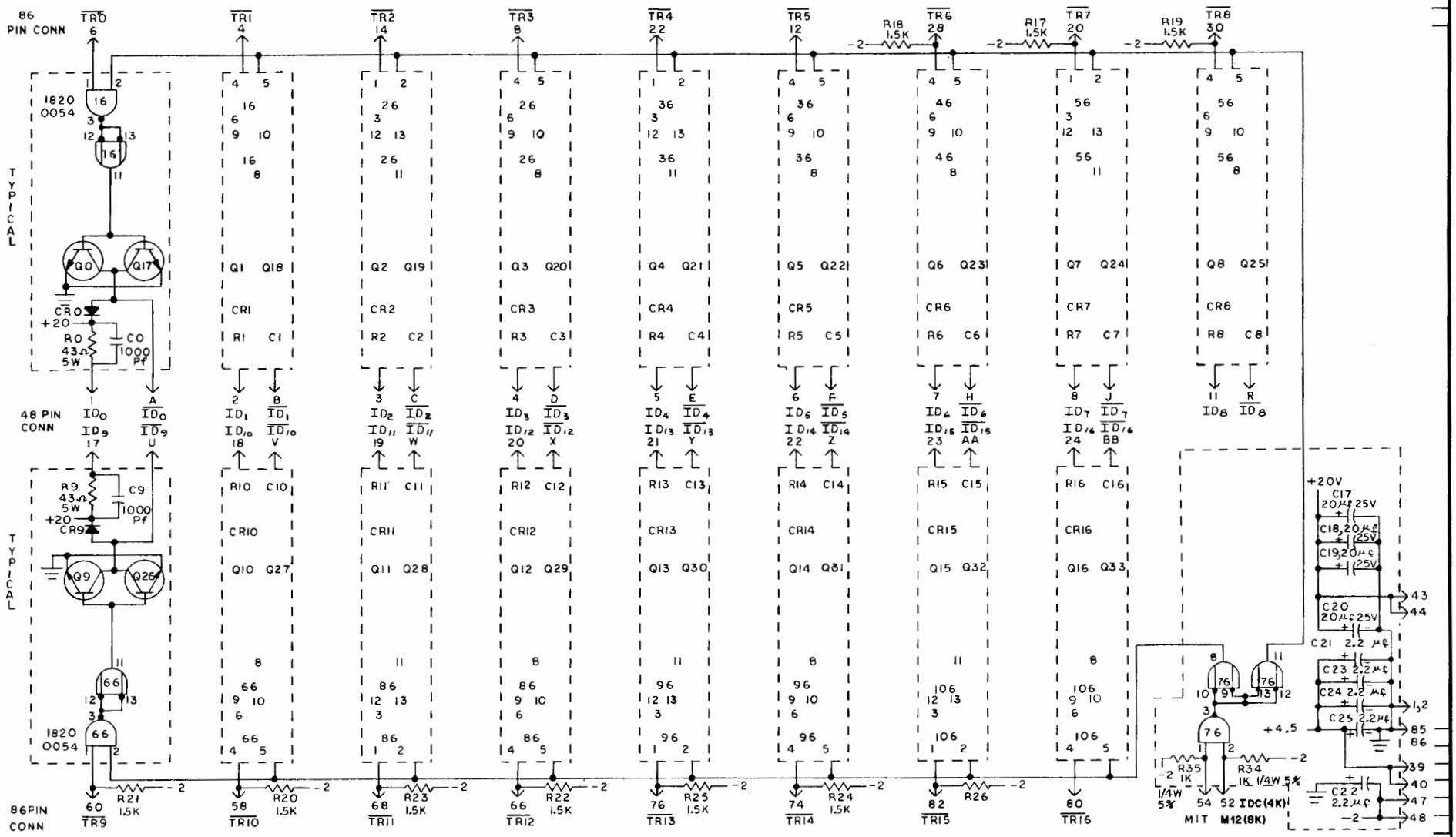
FOR TRAINING PURPOSES ONLY



NOTE
UNLESS OTHERWISE NOTED
ALL INTEGRATED CKTS ARE 1820-0306
ALL TRANSISTORS ARE 1853-0036
ALL RESISTORS 1/8W 1% MF

(15) REF DES (MC15)

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	ADDED CO-22, Q17-33, CHG PACK NOS	8-17-67	
B	ADDED C23-25, DELETED R17-33 LG	10-10-67	
C	R17-26 LG	12-5-67	

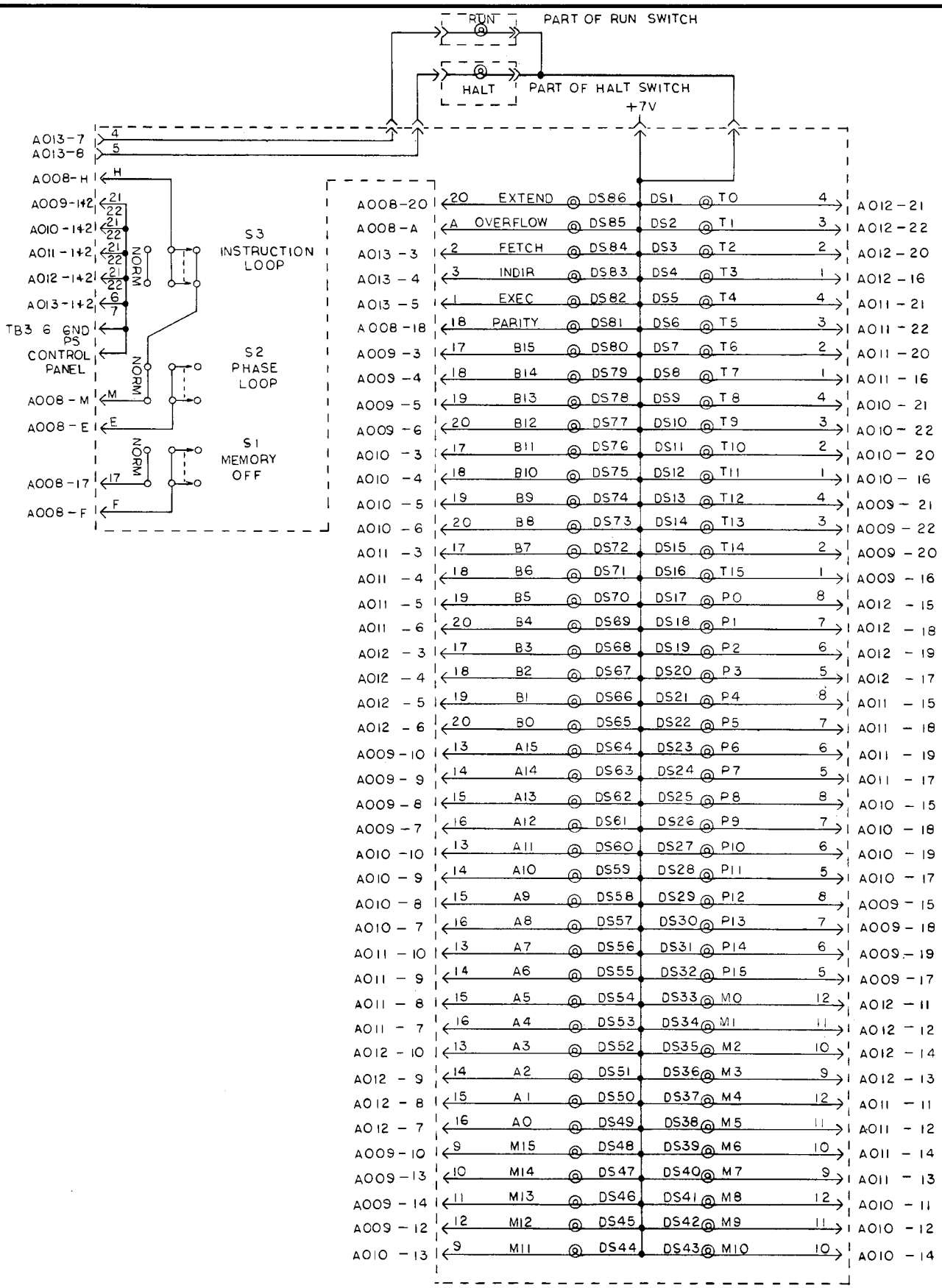


NOTE
UNLESS OTHERWISE NOTED
ALL DIODES 1901-0050
ALL TRANSISTORS 2N3643
ALL RESISTORS 1/4W 5%

24 LOCATION (MC 24)

Inhibit Driver
HP 2115A

FOR TRAINING PURPOSES ONLY



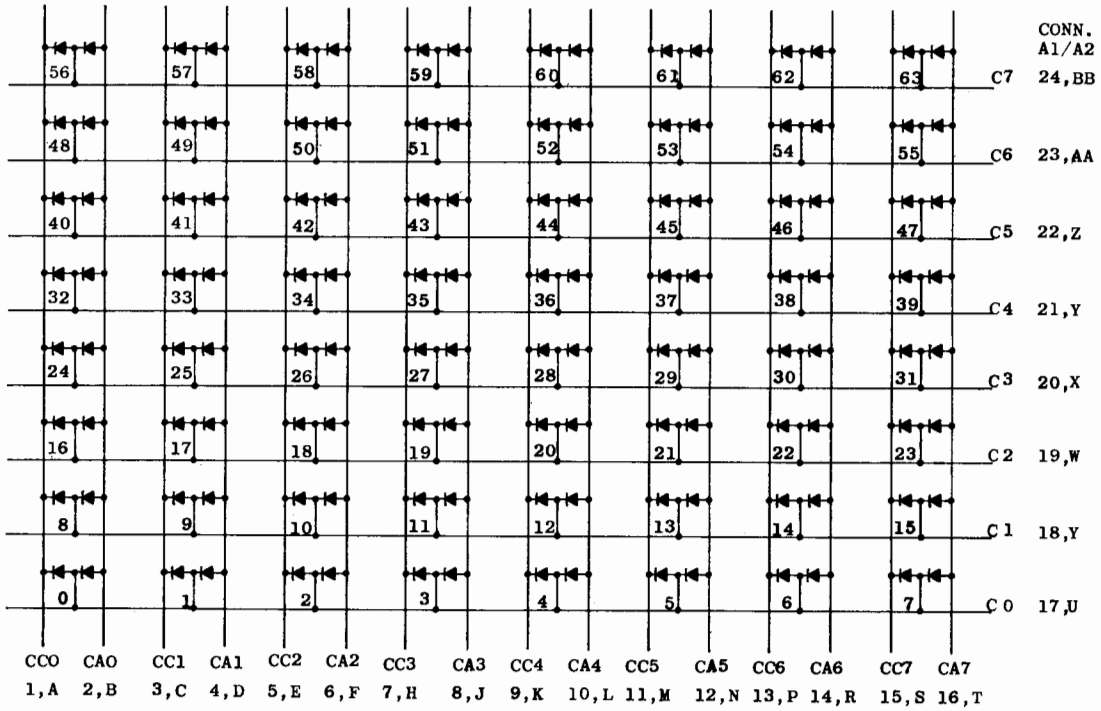
Display Board And
Run Halt Lamps
HP 2115A

FOR TRAINING PURPOSES ONLY

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

COMMON ANODE FOR WRITE

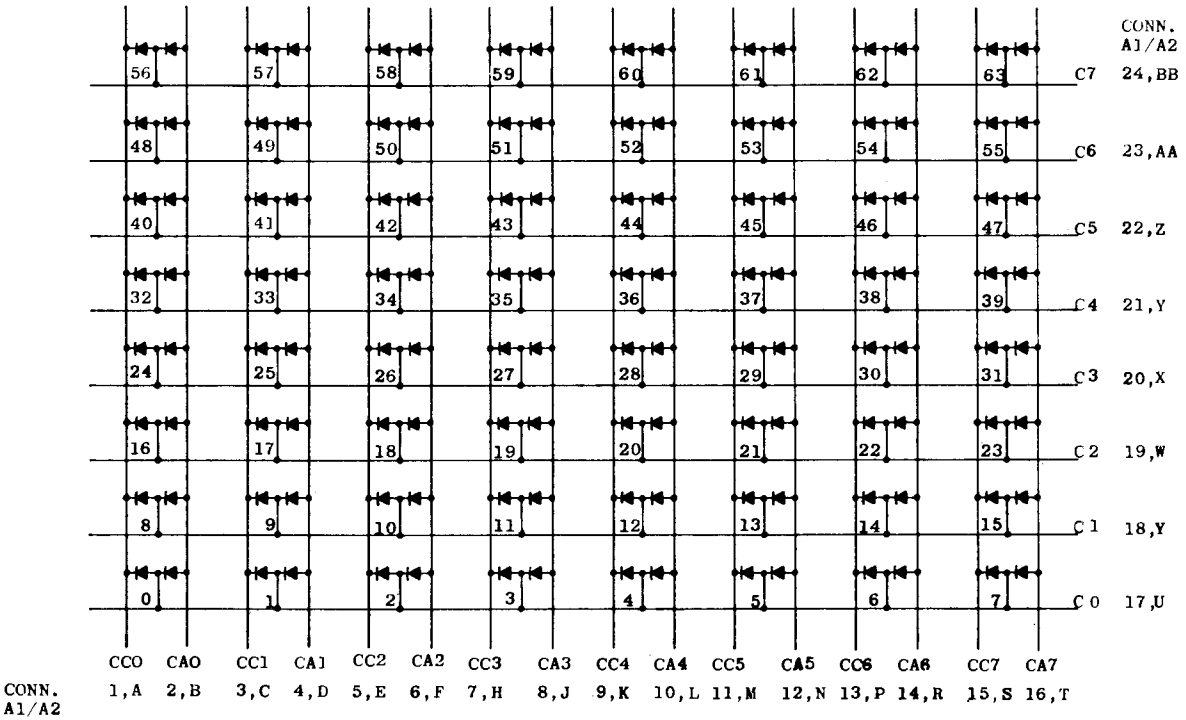
COMMON CATHODE FOR READ



Wiring Info
HP 2115A

FOR TRAINING PURPOSES ONLY

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



NOTE:

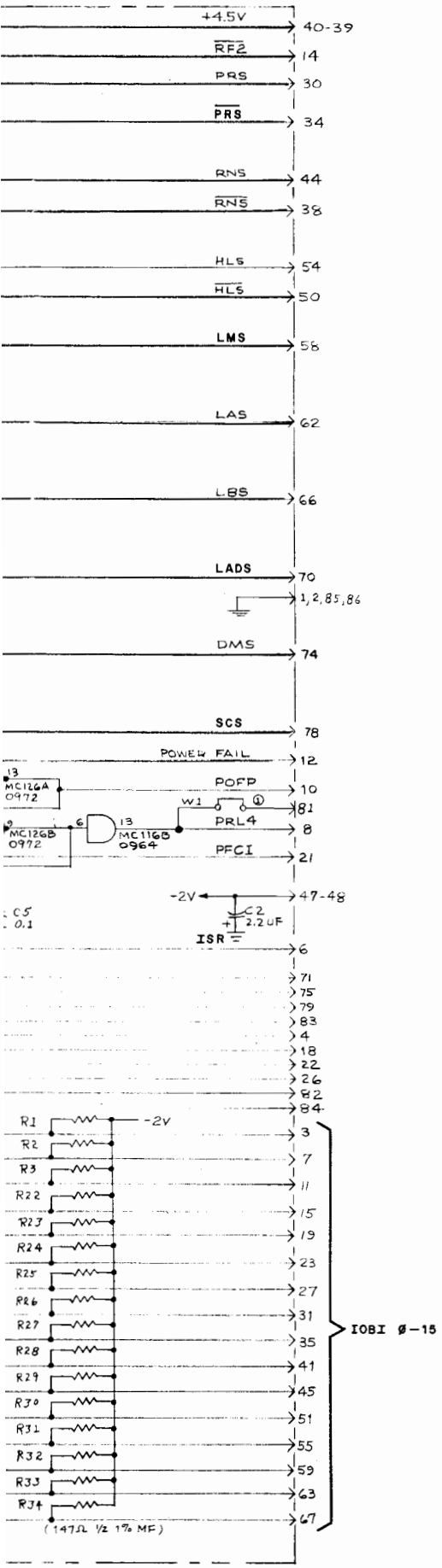
CURRENT DIRECTION ASSIGNMENTS

	MODULE 0 X and Y COORDINATES	MODULE 1 X COORDINATE
COMMON ANODE	WRITE	READ
COMMON CATHODE	READ	WRITE
DIGIT ASSIGNMENTS	A3 - INHIBIT A6 - SENSE	A4 - INHIBIT A7 - SENSE

Wiring Info
HP 2115A

FOR TRAINING PURPOSES ONLY

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	AS PER L. CORRELL CORRECTIONS	1-2-68	JC

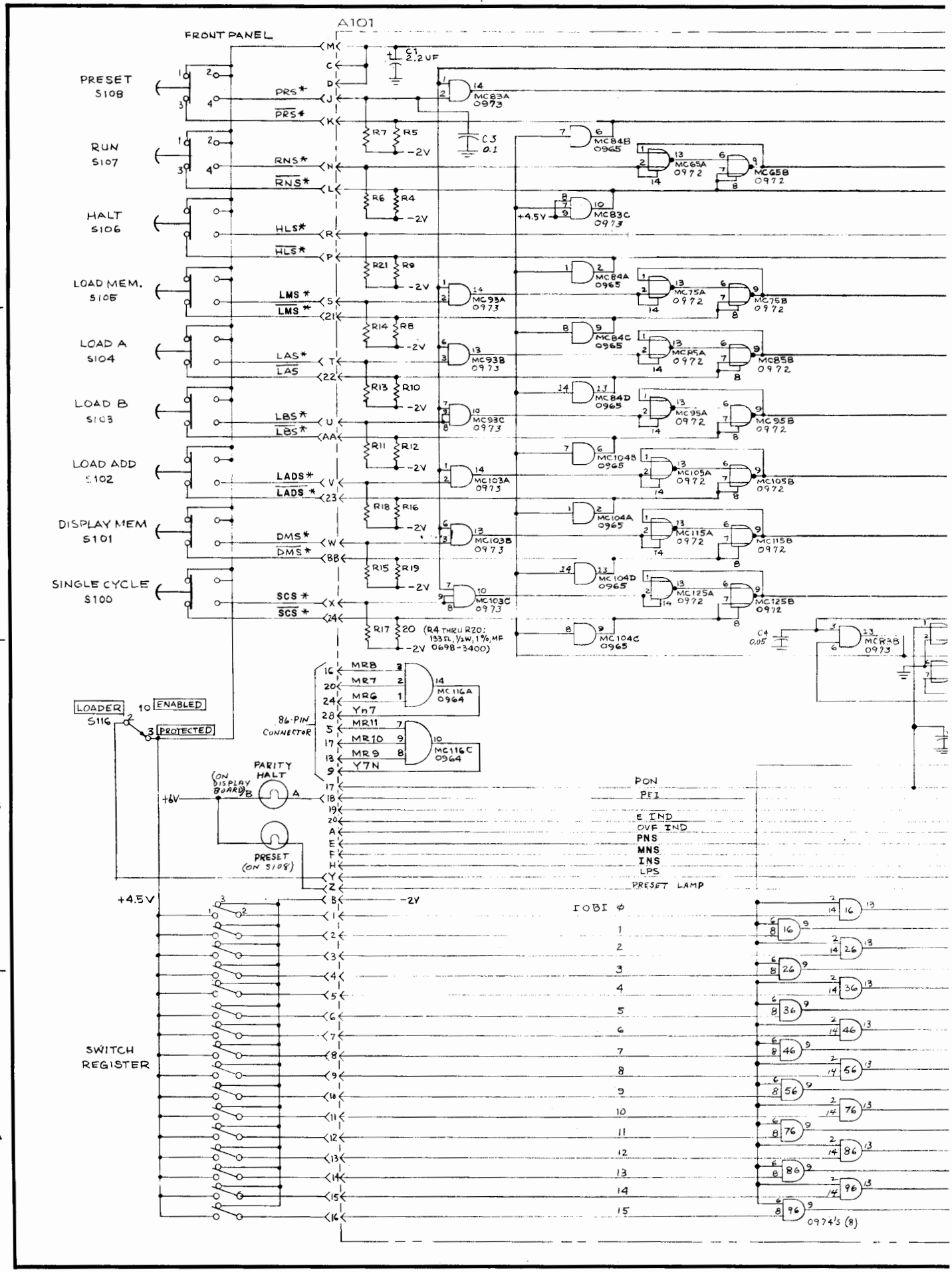


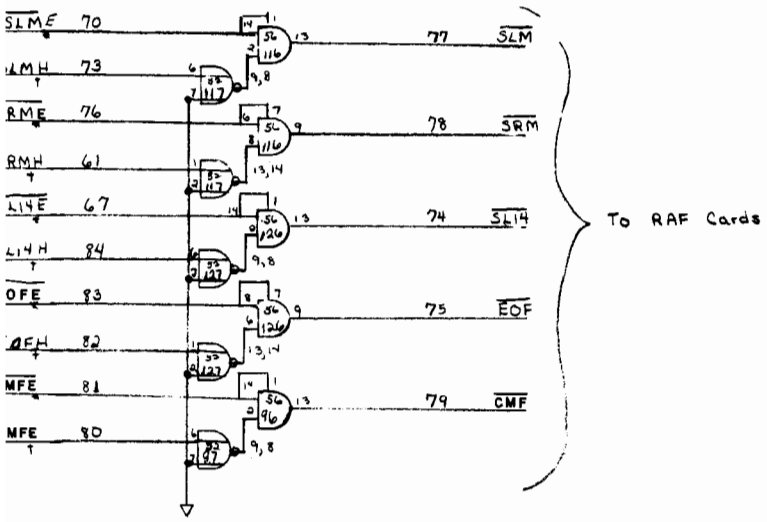
NOTES

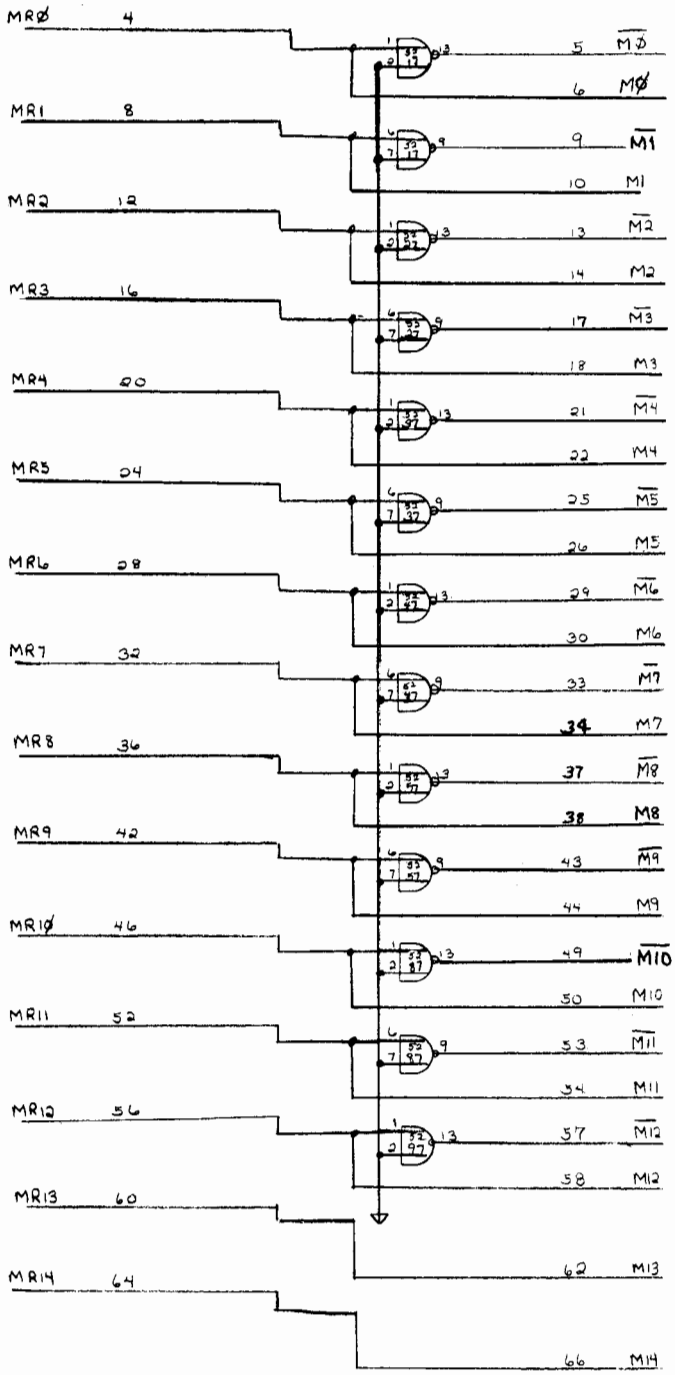
① REMOVE W1 FOR DMA.

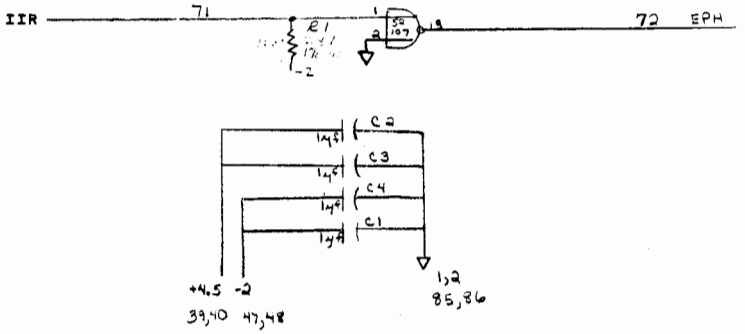
Front Panel
Coupler Schematic
HP 2115A

FOR TRAINING PURPOSES ONLY


A101
FRONT PANEL
PRESET S108
RUN S107
HALT S106
LOAD MEM. S105
LOAD A S104
LOAD B S103
LOAD ADD S102
DISPLAY MEM S101
SINGLE CYCLE S100
PRS*
RNS*
HLS*
LMS*
LAS*
LBS*
LADS*
DMS*
SCS*
C1 2.2 UF
C3 0.1
C4 0.05
R17 20 (R4 THRU R20: 133Ω, ½W, 1%, MF 0698-3400)
-2V
+4.5V
+6V
MC83A 0973
MC84B 0965
MC65A 0972
MC65B 0972
MC83C 0973
MC84A 0965
MC75A 0972
MC75B 0972
MC93A 0973
MC84C 0965
MC85A 0972
MC85B 0972
MC93B 0973
MC84D 0965
MC95A 0972
MC95B 0972
MC93C 0973
MC104B 0965
MC105A 0972
MC105B 0972
MC103A 0973
MC104A 0965
MC115A 0972
MC115B 0972
MC103B 0973
MC104D 0965
MC125A 0972
MC125B 0972
MC103C 0973
MC104C 0965
MCR3B 0973
MRB
MR7
MR6
Yn7
MR11
MR10
MR9
Y7N
MC116A 0964
MC116C 0964
86-PIN CONNECTOR
LOADER S116
ENABLED
PROTECTED
PARITY HALT
(ON DISPLAY BOARD)
PRESET (ON S108)
SWITCH REGISTER
PON
PEI
E IND
OVF IND
PNS
MNS
INS
LPS
PRESET LAMP
IOBI Φ
0974's (8)







Memory Logic
HP 2115A
FOR TRAINING PURPOSES ONLY

Laboratory Project # 1

Lesson: Logic Control and Timing

Objective: To give the student practice in using the Logic Equations and Backplane Wire List.

Problem: Find the source of the RBRB control function. Find and list the source and distribution of all logic signals required to generate RBRB when the B-Register is addressed as memory location ØØØØØ1.

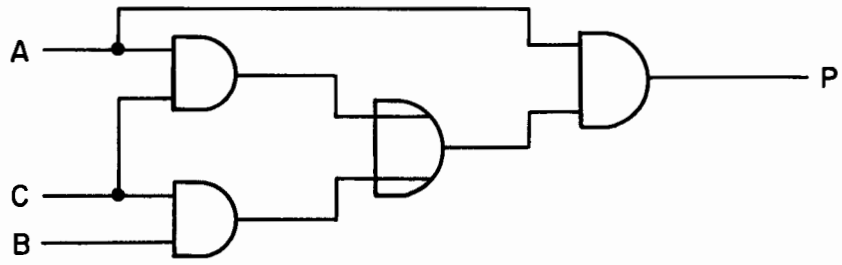
Laboratory Project # 2

Lesson: Logic Control and Timing

Objective: To give the student practice in using Truth Tables and Boolean expressions.

Problem:

1. Write the Boolean expression for the circuit below:



2. Reduce the equation obtained in step 1 and construct the circuit for the new equation.

3. Construct a Truth Table for the circuits derived in steps 1 and 2.

Laboratory Project #3

Lesson: System Timing and Control

Objective: To ensure that the student is knowledgeable of the time relationship of certain control signals.

Problem: Draw a timing chart consisting of actual waveforms observed when viewing the following signals, (FETCH phase only):

a. MRT
b. MWT
c. MST
d. MRT
e. RST
f. RMSB

Procedure:

1. Store the instruction LDA ØØØ1ØØ in memory location ØØØ1ØØ.
2. Load address ØØØ1ØØ into P & M Registers.
3. Depress PRESET and set the PHASE switch to LOOP.
4. Depress RUN.
5. Adjust the oscilloscope such that one time period equals one centimeter, i.e. TØ = 1 cm.

Laboratory Project #4

Lesson: Memory

Objective: To give the student experience in making the sense amplifier adjustment.

Problem: Properly adjust the sense amplifier circuits.

Procedure:

1. Open the front cover from the HP 2116B Computer.
2. With POWER off, disconnect the core stack connector from the Sense Amplifier board SA-0. Remove the board from the slot and install an Extender Board in its place. Then plug the Sense Amplifier board into the Extender, and reconnect the core stack to the Sense Amplifier using an Extender Cable. Switch POWER on.
3. Set SWITCH REGISTER to 000000 and press LOAD MEMORY, LOAD ADDRESS, LOAD A and LOAD B.
4. Set SWITCH REGISTER to 070000 and press LOAD A; then press SINGLE CYCLE once.
5. Set PHASE switch to LOOP (rear of front panel).
6. Set SWITCH REGISTER to 177777 and press LOAD A.
7. Press RUN.

   The Computer will run continuously with all T-Register lights on, indicating that 177777 is being stored in all memory locations.
8. Connect oscilloscope synchronization input to the test point on the Timing Generator Board.
9. Consecutively connect the oscilloscope vertical input to the collectors of the output transistor pairs (Q1/Q2, Q11/Q12, Q21/Q22, etc. through Q161/162) and adjust the corresponding balance adjustment (R7, R17, R27, etc. through R167) for the cleanest possible pulse. Use only the first displayed pulse for observation; disregard succeeding pulses. See Figure 2 for correct and incorrect waveforms.

10. Press HALT. Switch POWER off. Remove the Extender Board and Cable, install the Sense Amplifier board in its normal position, and set PHASE switch to NORM.

11. If the Computer has an 8K memory, repeat steps b through k using the other Sense Amplifier Board, SA-1.

12. Disconnect oscilloscope leads, and replace Computer cover.

Laboratory Project #5

Lesson: Input/Output System

Objective: To teach the student how to analyze I/O system failures and how to troubleshoot the I/O system.

Problem: While executing the accompanying program, the operator found the computer "hung" in a loop. He halted the computer and reinstated his program. The computer then read one character and "hung" in the same loop again.

SAMPLE PROGRAM FOR LABORATORY EXERCISE 5

Set B = Ø

Set A = Ø

Set 5ØØ = Ø

Set 6ØØ = 1Ø

Set 6Ø1 = Ø

Set 1Ø = Ø161ØØ (JSB to 1ØØ)

MAIN PROGRAM
STARTING ADDRESS = 3ØØ

3ØØ = 1Ø21ØØ (STF ØØ)

3Ø1 = 1Ø371Ø (STF, CLF 1Ø)

3Ø2 = Ø465ØØ (ADB 5ØØ)

3Ø3 = Ø46ØØ1 (ADB Ø1(B))

3Ø4 = Ø726ØØ (STA 6ØØ)

3Ø5 = Ø366Ø1 (ISZ 6Ø1)

3Ø6 = Ø263Ø2 (JMP 3Ø2)

3Ø7 = Ø263Ø2 (JMP 3Ø2)

INTERRUPT SUB-ROUTINE
STARTING ADDRESS = 1ØØ

1ØØ = RETURN ADDRESS

1Ø1 = 1Ø251Ø (LIA 1Ø)

1Ø2 = 1Ø371Ø (STC, CLF 1Ø)

1Ø3 = 1261ØØ (JMP, I 1ØØ)

STUDY ASSIGNMENTS

Section 1: Answer questions on pages 1-16, 1-22, and 1-45.

Read pages 2-1 through 2-66

Section 2: Answer questions on pages 2-3, 2-4, 2-23, 2-24, 2-40, 2-21, 2-58, 2-59, 2-64 and 2-66.

Read pages 3-1 through 3-26.

Section 3: Answer questions on pages 3-7, 3-8, and 3-26.

Read pages 4-1 through 4-36.

Section 4: Answer questions on page 4-36.

Read pages 5-1 through 5-42.

Section 5: Answer questions on pages 5-30, 5-35 and 5-38.

Read pages 6-1 through 6-43.

Section 6: Answer questions on pages 6-8, 6-7, 6-19, 6-21, 6-41 and 6-43.

Read pages 7-1 through 7-16.

HEWLETT PACKARD

11000 WOLFE ROAD, CUPERTINO, CALIFORNIA 95014, TELEPHONE 408 257-7000, TWX 910-338-0221
EUROPE: 1217 MEYRIN-GENEVA, SWITZERLAND • CABLE "HEWPACKSA" TEL. (022) 41.54.00

Printed in U.S.A. 3/69