SERVICE MANUAL

9895A Flexible Disc Memory

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Recording Specifications

HP Double Density Format

Encoding:	Modified modified frequency modulated
Rotational Speed:	360 RPM, ±2.0 (±7.2 RPM)

Bit Density @ 360 RPM:

Track No.	Head 0 Single/Double-Sided	Head 1 Double-Sided Only
0	3651 BPI*	3736 BPI
38	4702	4845
76	6536	6816

* BPI – Bits Per Inch

Track Density:	48 tracks per inch
Tracks Per Surface:	77
Surfaces Per Disc:	2

IBM Single Density Format

Encoding:	Frequency modulated
Rotational Speed:	360 RPM, ±1 (±3.6 RPM)
Bit Density @ 360 RPM:	3268 BPI, track 76, head 0
Track Density:	48 tracks per inch (approx. 19 tracks per cm)
Tracks Per Surface:	77
Surfaces Per Disc:	1

Capacity

HP Double Density Format

Bytes/Sector:	256
Sectors/Track:	30
Tracks:	154 on two surfaces
Bytes/Disc (Formatted):	1.18 megabytes (154 tracks)

IBM Single Density Format

Bytes/Sector:	128
Sectors/Track:	26
Tracks:	77 (head 0 only)
Bytes/Disc (Formatted):	256 kilobytes

Access Time

Track-to-Track Seek:	3 ms/track, plus 20 μs settling
Maximum Track-to-Track Seek (76 Tracks):	248 ms
Average Track-to-Track Seek:	96 ms
Maximum Rotational Latency:	167 ms
Average Rotational Latency:	83 ms
Maximum Data Access Time (Seek Plus Latency):	415 ms
Average Data Access Time:	179 ms
Head Load Time:	40 ms

Data Transfer Rate

Read Burst Transfer Rate:	190 kilobytes/second
Write Burst Transfer Rate:	190 kilobytes/second
HP Format Average Transfer Rate:	25.6 kilobytes/second[1]
IBM Format Average Transfer Rate:	11.1 kilobytes/second[2]

Environmental Specifications

Operating Limits

Temperature:	10°C to 40°C (50°F to 104°F)
Relative Humidity:	20% to 80% with maximum wet bulb temperature not to exceed (non-condensing) 25.5°C (77.9°F)
Altitude:	0 to 4572 M (0 to 15,000 feet)

Non-Operating Limits (Storage and Transit)

Temperature:	−40°C to 60°C (−40°F to 140°F)
Altitude:	−304.8 to 15240 M (−1,000 to 50,000 feet)

Alignment Limits

Radial Alignment:	±0.001 inch (.025 mm) of track center at track 38 for both head 0 and head 1

1 Interleave parameter dependent – best case every other sector.

2 Interleave parameter dependent – best case every other sector. If sectors are not staggered, then only one sector per revolution can be transferred in buffered mode – 768 bytes/second.

Power Requirements

100, 120, 220, 240 volts ac, ±10%
2.5 amps max at 120 volts
50/60 Hz, ±2.0%

Media Life

Revolutions:	>3,000,000 on any track, heads loaded
Insertions:	>30,000

Head Life

More than 15,000 hours of operation with use of HP approved media.

Dimensions

Height:	192 mm (7.6 inches)
Depth:	575 mm (22.6 inches)
Width:	483 mm (19.0 inches)

Weight

	9895A	9895A Option 10
Net:	26.8 kg (59 lbs)	20.9 kg (46 lbs)
Shipping:	31.8 kg (70 lbs)	25.9 kg (57 lbs)
Heat Dissipation:	295 W	
Recommended Attitude:	Horizontal	

Safety Considerations

General

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

Safety Symbols

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Safety Earth Ground

This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

Before Applying Power

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the main power source.

Servicing

Any servicing, adjustment, maintenance or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc) are to be used for replacement.

Chapter 1
General Information

Introduction

This chapter contains a general description of the 9895A Flexible Disc Memory and a description of the recording formats which can be used.

General Description

The 9895A Flexible Disc Memory is a random access storage system employing a flexible magnetic medium. It consists of a controller printed circuit module, two drive modules, a power supply and the chassis and cover package. The 9895A can be ordered in various optional configurations, which delete the controller, one drive or the controller and one drive.

The controller module accepts and interprets commands over the Hewlett-Packard Interface Bus (HP-IB), controls the interface to the drive electronics module, retrieves and stores data from the drive electronics module, and returns disc drive and disc operation status information to the host mainframe.

Each drive module contains all the mechanical parts for physically handling the disc. These include the drive spindle and motor, the read/write and erase heads, write protect and single-sided disc sensors, door open/closed sensor, door lock and various guides. Each drive module also contains all driver, positioning, loading and interface electronics needed by the mechanical parts. The electronics are located on a printed circuit board mounted on the bottom of the drive module.

The power supply module contains rectifiers, filters and regulators to provide +24 volts, +12 volts, +5 volts and −12 volts to the various electronic modules.

An internal transformer provides stepped down voltages to the power supply and 120 Vac to the spindle motors.

The flexible magnetic medium used in the 9895A is called a flexible disc. The flexible disc is 20 centimeters (7.9 inches) in diameter and has a 3.8 centimeter (1.5 inch) hole for alignment on the spindle of the disc drive. The disc is enclosed in a protective Polyvinylchloride (PVC) jacket with a slot for head access to the recording surface. Both sides of the flexible disc are used for data storage.

The recording head in the drive module is positioned by a mechanism that includes a stepper motor, capstan and taut metal band. The mechanism operates in an open loop configuration, that is, there is no positive feedback to determine the actual position of the head. The head assembly has two read/write heads, one for each side of the flexible disc. When the heads are loaded, both contact the medium. The heads are automatically unloaded one and a half seconds after the last command is received.

The controller module contains a Micro CPU Chip (Z80), a processor-to-HP-IB Interface (PHI) Chip, Read-Only Memory (ROM), Random Access Memory (RAM) and the associated logic circuits necessary to provide an interface between up to four disc drive assemblies and the HP-IB interface channel. The Z80 handles data and commands directly at the byte level.

The controller module also contains an extensive self-test capability. Self-test functions include various combinations of read/write operations on numerous tracks. All self-test functions may be initialized by manual switching or HP-IB command except a pre-formatted read-only test, which is switch-initiated only. The controller module performs a subset of the self-test each time power is applied. This subset does not include reading from or writing to a disc. Self-test results are available as a four-bit binary word displayed on an LED array mounted on the controller module or as two bytes of status information which can be read by the host system.

The 9895A will read and write the HP standard flexible disc format as used on the HP 9885 Flexible Disc Drive, on either single-sided or double-sided discs. The 9895A will also read and write the IBM 128 bytes per sector standard data interchange format (IBM 3740) on a single-sided disc. When a formatted disc is loaded into the disc drive, the controller module will determine which format is being used and whether the disc is single- or double-sided. Format and disc type are both reported as status information. When a disc is re-formatted, the controller module performs defective track labeling and sparing as well as track re-formatting.

Data transfers are buffered on a sector-to-sector basis. This allows devices connected to the flexible disc memory to access data at any rate up to the maximum burst rate.

A modular replacement philosophy has been implemented in the flexible disc memory to minimize on-site repair time. Troubleshooting the flexible disc memory is simplified by its self-test diagnostics.

Service Support Package

Tools and parts needed for effective support of the 9895A are organized into two Service Support Packages. The Product Support Package (part number 09895-67100) contains tools, and the Field Service Inventory (part number 09895-67197) contains parts and assemblies. The contents of the PSP are listed in Table 1-1 and the contents of the FSI are listed in Table 1-2, although both inventories are subject to change as experience indicates that a different inventory would be more effective. The PSP and FSI may be ordered together under part number 09895-67190.

Table 1-1. PSP Contents

Description	HP Part Number	Quantity
Service Manual	09895-90030	1
Pozidriv	8710-0900	1
Diagnostic Tape Cartridge	98041-90010	1
Status Display Board	09895-66506	1
Alignment Disc	9164-0111	1
Blank Discs	9164-0144	1 pkg

Table 1-2. FSI Contents

Exchange Assemblies:

Description	HP Part Number New	HP Part Number Rebuilt
Controller Board	09895-66500	09895-69500
Disc Drive	09895-67914	09895-69914

Other Parts or Assemblies:

Description	HP Part Number	Quantity
Power Module	09895-67910	1
Switch, Main Power	3101-0417	1
Cable Assembly, Drive AC	8120-2930	1
Board, Back Plane	09895-66501	1
Cable Assembly, Transformer to Power Module	8120-2926	1
Cable Assembly, Internal HP-IB	09895-61608	1
Fuse, Internal	2110-0383	1
Fan	3160-0311	1
Belt, Motor	0950-0475	5
Switch, Door-Closed	0950-0476	2
Detector, Write Protect	1535-4090	1
LED, Door Button	0950-0477	5
Clip, Push-In	0950-0478	1
Latch, Door	0950-0479	1
Spring, Door	0950-0472	1
Pin, Hinge (Short)	0950-0480	4
Pin, Hinge (Long)	0950-0481	4
Pin (Door Front)	0950-0482	4
Pin, Hitch	0950-0500	4
Button, Door	0950-0483	1
Detector, Track 0	0950-0489	1
Load Plate	0950-0473	2
Detector, Index	0950-0499	1
Ejector Assembly	0950-0474	1

Options

The following options are available with the 9895A.

Option 001 – 50 Hz Operation

This option enables the drive to operate on a 50 Hz line frequency. It is installed at the factory if the unit is going to an area which utilizes 50 Hz power. The unit can easily be changed in the field from one frequency to the other.

Option 002 – Rack Mount

This option enables the unit to be mounted in a standard 19-inch rack mount cabinet. It is usually installed at the factory, although a rack mount field installation kit (09895-88022) is available.

Option 010 – Single Drive Master

This option deletes one drive from the unit.

Option 011 – Single Drive Slave

This option deletes one drive and the controller from the unit.

Option 012 – Double Drive Slave

This option deletes the controller from the unit.

Equipment Supplied

The following equipment is supplied with the unit and should be checked for upon delivery.

Item	HP Part Number	9895A	Opt 10	Opt 11	Opt 12
Master-to-Slave Cable (1M)	09895-61606	0	0	1	1
Power Cord	Depends on Installation Region	1	1	1	1
User's Manual	09895-90000	1	1	1	1
Disc Protector Card	09895-90010	2	1	1	2
Blank Disc	9164-0144	1	1	1	1

Accessories Available

Item	
Drive Accessory[1] To upgrade a one drive unit to a two drive unit. Order Option 001 for 50 Hz operation. Order Option 101 for installation by HP.	98952A
Control Board Assembly[1] To upgrade a slave to a standard unit. Order Option 101 for installation by HP.	98951A
Rack Mount Kit	09895-88022
Package of 10 Double-Sided, Double Density Flexible Discs	92195A
HP-IB Interface Cable (2M)	8120-2718

[1] To ensure proper operating performance, these kits should be installed by a Hewlett-Packard Customer Engineer.

Installation

This section provides information for installing a 9895A Dual Disc Memory and putting it into operation.

The 9895A Disc Memory may contain either one or two drives, depending on purchaser preference. It may also control one or two other drives in another 9895A (Option 011 or 012). It is connected to a controlling mainframe by means of an HP Interface Bus (HP-IB) System. It is connected to other 9895A's by means of a cable furnished with Option 011 and 012 units (part number 09895-61606). The disc memory is controlled by a standard set of commands (see Appendix A), utilizing HP-IB timing and protocol. Many HP computers provide a high-level language subsystem to control a disc memory. Methods for controlling the disc memory are contained in the computer's programming or subsystem reference manual. If a high-level disc control language is not available with your mainframe, refer to the disc memory command set description in the appendix. Contact the local HP Sales and Service office for assistance.

Please follow these instructions carefully, as a mistake made in the installation can cause impaired operation.

Power Requirements

The 9895A can operate on line voltages of 100, 120, 220 or 240 Vac (±10%). The line frequency must be within 2.0% of 50 or 60 Hz. The voltage selector switches on the rear panel must be set to the nominal ac line voltage for the area it is operating in. Figure 1-1 shows the setting of the voltage selector switches for the various line voltages.

NOTE

Option 001 must be installed in the 9895 when operating on a line frequency of 50 Hz. Option 001 requires internal modification.

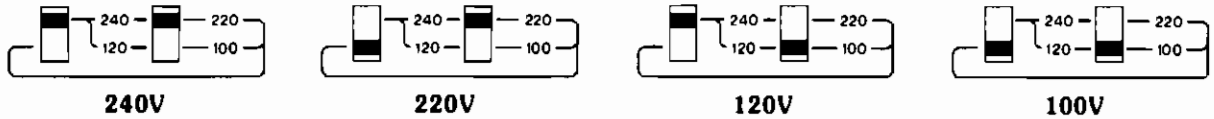


Figure 1-1. Line Voltage Selector Switches

Fuses

A different fuse is required for each of the two voltage ranges of 100-120 and 220-240 Vac. Table 1-3 gives the correct fuse ratings and part numbers.

Table 1-3. Fuses

Voltage Range	Fuse Rating	HP Part Number
100 – 120	3 Amp Normal Blow	2110-0003
220 – 240	2.0 Amp Normal Blow	2110-0002

Addressing

The address of each individual drive is composed of two parts, the bus address and the drive or unit number. Each of these parts is set on a different switch in a different location, using a different set of rules. Since it is essential that this address be set correctly, these will be covered in detail.

Bus Address

The various devices on an HP-IB channel are differentiated by the bus address portion of the address. The 9895A must use a bus address between 0 and 7. The bus address select switch is located on the front of the controller board (see Figure 1-2). Removing the front cover provides access to the switch. Note that although as many as four drives may be controlled by one controller board, they all have the same bus address. If several controller boards are connected to an HP-IB, each must have a different bus address. If you change the bus address, change the number on the front panel, also.

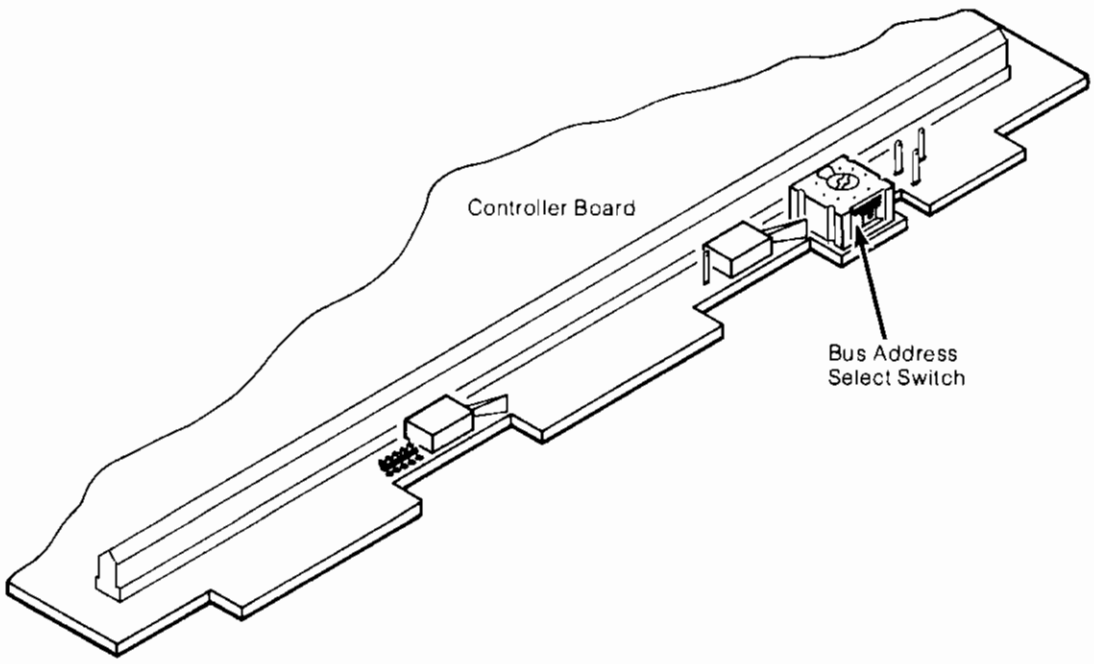
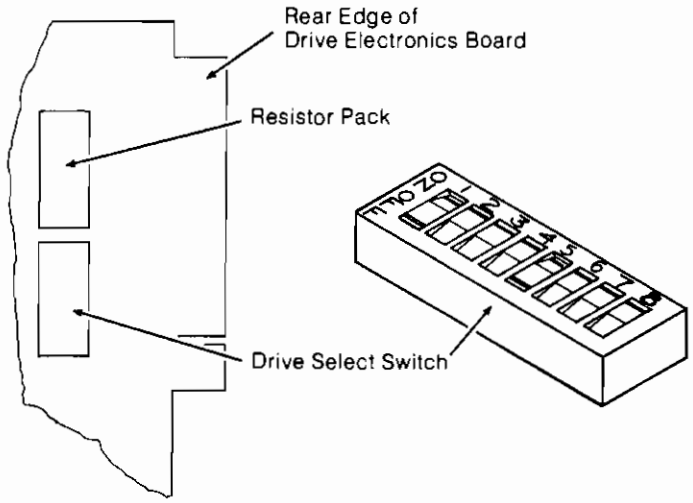


Figure 1-2. Bus Address Selector Switch

Drive or Unit Number

The drives connected to a controller board are differentiated by their drive number. The drive number must be between 0 and 3. The factory sets 9895A drives to 0 and 1, and 9895A Option 011 or 012 to 2 and 3. The drive number can be found on the front cover, beneath the disc insertion opening. If this number must be changed (to eliminate conflicts or other reason), follow this procedure.

1. Remove front, top and bottom covers (see disassembly procedures in Chapter 3).
2. Place the unit on it's top.
3. Remove the controller board.
4. Remove the four screws holding the drive into the chassis.
5. Slide the drive forward to clear the aluminum plate covering the back portion.
6. Locate the eight segment drive select switch on the rear of the drive electronics board mounted on the underside of the drive module (see Figure 1-3).
7. Set the switch segments according to the following diagram.



Select Code	Segments 1	2	3	4	5	6	7	8
3	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
1	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
0	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON

Figure 1-3. Setting the Drive Number

8. If you changed the drive number, be sure to change the number on the front of the drive.
9. Re-assemble the unit.

Self-Test

During installation you may wish to check the electrical performance of the drive. The drive can be checked with or without a disc installed. To conduct the self-test, follow this procedure:

1. Remove the front cover of the 9895A, thereby exposing two toggle switches and an LED display on the front edge of the controller (see Figure 1-4).
2. Press and release the right-hand toggle switch. The LED's should now start blinking, indicating that the self-test routine has begun.
3. The routine should terminate with only the right-most LED lit. Any other result indicates a failure. Try running the self-test several times to verify pass or failure. This self-test verifies operation of:

    a. HP-IB interface chip (PHI),
    b. Read-only memory,
    c. Z80 processor,
    d. Random access memory,
    e. Serializer/deserializer,
    f. Encoder,
    g. Decoder,
    h. Stepping circuit and mechanism,
    i. Rotational timing (if disc installed).

If the drive fails self-test, turn to the troubleshooting section of Chapter 3.

A more elaborate test, the read/write self-test, is run using the following procedure:

1. Install a write enabled, formatted, scratch disc in each drive.
2. Press and hold the left-hand switch.
3. While holding the left-hand switch, press and release the right-hand switch.
4. Release the left-hand switch. Read/write self-test should now start.

This routine writes on the disc and then reads back, comparing what it read with what it wrote. It checks the read/write circuitry and the CRC generator/checker, as well as everything checked by the previous routine.

A final check, the read-only self-test, may be run using the following procedure:

1. Install a formatted scratch disc in all drives.
2. Press and hold the right-hand switch.

This routine compares the location of a sector with where the controller thinks it should be. It starts on the outermost track and increments inward at about two tracks per second. If the sectors are located differently than the controller thinks they should be, the routine will halt on an error. Continue the test until it is apparent that it is running correctly (several seconds).

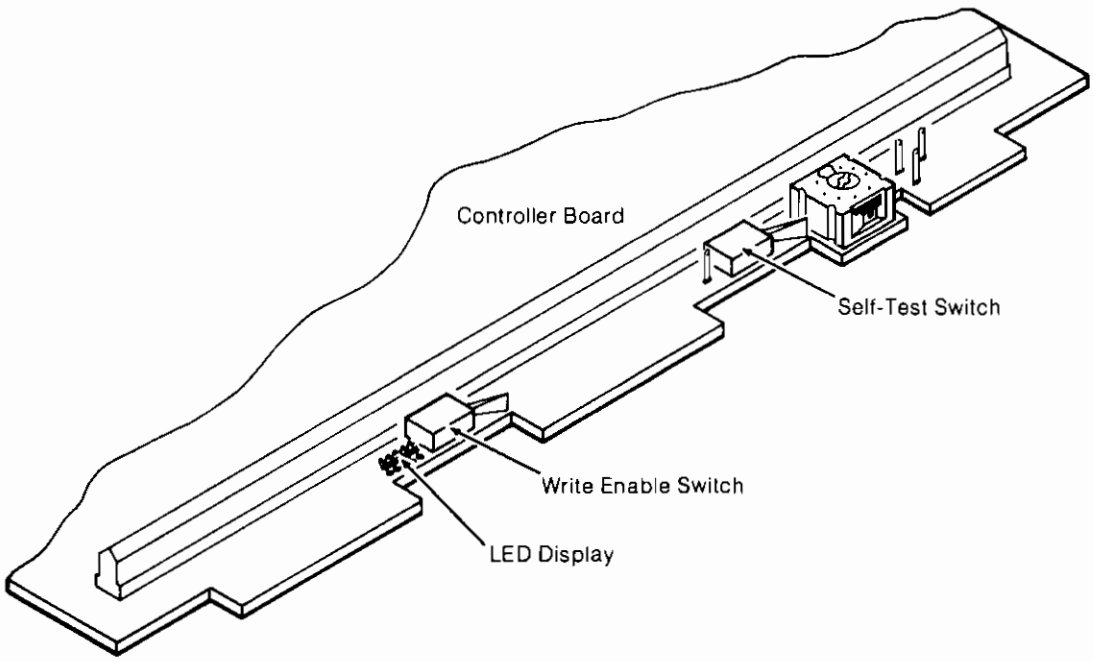


Figure 1-4. Self-Test Functions

9895A Installation Procedure

To install a 9895A, follow this procedure:

1. Unpack the 9895A and account for all furnished equipment.
2. Check the voltage selection switches on the rear panel (see Figure 1-1). If the setting is incorrect, change it to the correct voltage.
3. Ensure that the fuse in the rear panel is the correct rating (see Table 1-3).
4. Set the bus address select switch on the front of the controller board on the master unit.
5. Connect the ac power cord to the power input connector on the back of the unit (see Figure 1-5) and to an appropriate ac power source.
6. Turn the 9895A on and run the exercises described in the Self-Test section.
7. Turn to the section for the appropriate mainframe.

HP 9835A/B, HP 9845B/C

8. Install the appropriate ROM in the mainframe ROM drawer (see Table 1-4).
9. If connecting the 9895A to an existing HP-IB bus, plug one end of the 8120-2718 cable into the socket on the rear panel of the 9895A and the other end into the socket on a nearby mass storage device (see Figure 1-5).

   If connecting directly to a mainframe, set the select code on the interface body and plug it into the socket on the rear panel of the mainframe. Then plug the other end into the socket on the rear panel of the 9895A (see Figure 1-5).

   If connecting a slave unit, use the 9895-61606 cable to connect the slave to the master (see Figure 1-5).
10. Turn the mainframe and all peripherals on. All peripherals connected to a bus should be turned on for the system to operate properly.
11. Install the System Exerciser Cartridge in the mainframe.
12. Select the 9895A exerciser from the menu and load it.
13. Install an initialized scratch disc in all drives. Close the doors.
14. Allow the Exerciser to run. It will repeat for all drives.
15. Blank discs can now be initialized on the drives.

HP 300, HP 3000

8. Plug one end of the 8120-2718 cable into the socket on the rear panel of the 9895A (see Figure 1-5). Plug the other end into the General Interface Controller (Part Number 31262-60001).

1000 – M.E.F.

8. Install the DVA 32 Driver ROM and the 12992H Loader ROM in the mainframe.
9. Plug the 12821A Interface into the mainframe, then plug one end of the 59310-60002 cable into the interface, and the other end into the socket on the rear panel of the 9895A.

   If connecting a slave unit, use the 9895-61606 cable to connect the slave to the master (see Figure 1-5).
10. Turn the mainframe and all peripherals on. All peripherals connected to a mainframe should be connected for the system to operate properly.

Table 1-4. ROM/Driver and HP-IB Interface Guide

HP System	ROM/Driver	Interface
9835A/B	98331B	98034A
9845B/C	98413A	98034A
HP 1000-10	DD.30	12009A
HP 1000-20, 40, 45	DVA 32	12821A
HP 300, 3000	None Needed	General Interface Controller

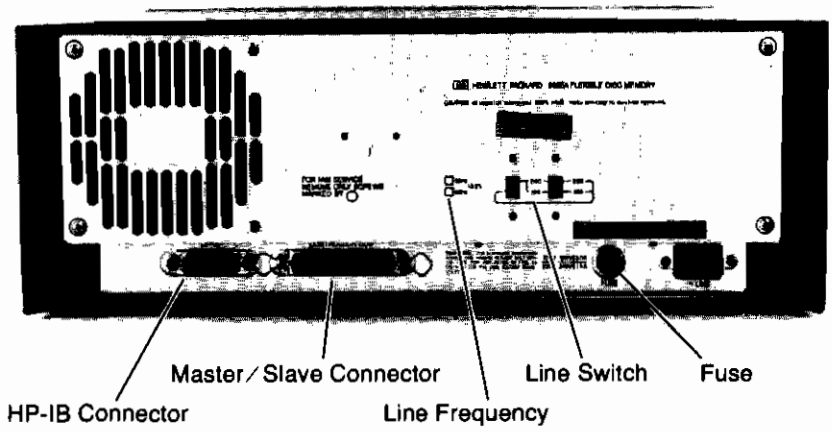


Figure 1-5. 9895A Rear Panel

Flexible Disc Use

Introduction

This section contains flexible disc loading instructions, disc handling precautions and details of the disc write protect capability.

Disc Loading

Figure 1-6 shows the proper method of loading the disc into the disc drive. To load a disc, proceed as follows:

NOTE
Disc loading/unloading should be done with disc drive power on and the drive spindle rotating.

1. Open the door on the front of the drive by pressing in on the door latch.
2. Insert the disc into the drive, with the label on the disc facing up, as shown in Figure 1-6.
3. Press the handle down until it locks in place.

Disc Handling Precautions

The disc is enclosed in a plastic jacket which is lined with a wiping material that cleans the disc of foreign matter. When not in use, the disc should always be stored in its protective envelope and returned to the box. To ensure error-free disc drive operation, the following additional precautions should be observed:

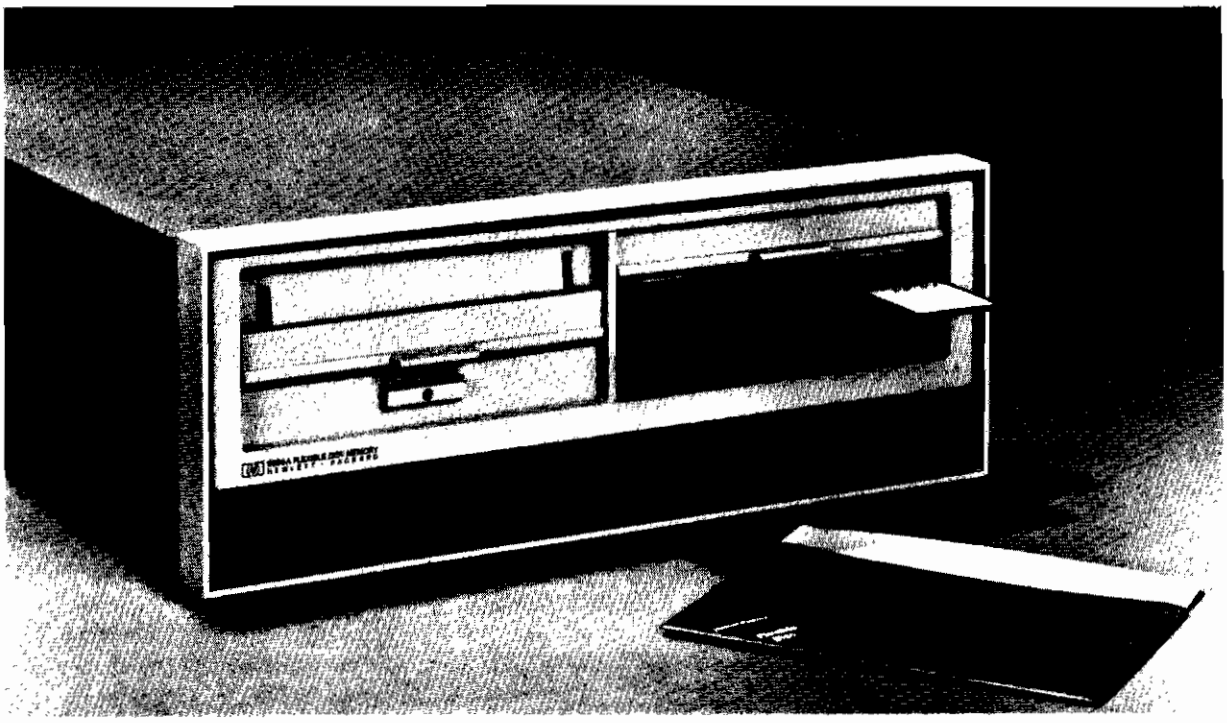


Figure 1-6. Loading a Disc

1. Use only HP-approved discs. Use of any others can result in damage to the drive mechanism, high maintenance costs and data loss.
2. Return the disc to its storage envelope and replace in the box whenever it is removed from the disc drive.
3. Replace storage envelopes when they become worn, cracked or distorted.
4. Do not touch or attempt to clean the surface of the disc. Abrasions may cause the loss of stored data.
5. Do not write on the plastic jacket of the disc with a lead pencil or ballpoint pen. Use a felt-tip pen and write only on the label.
6. Do not expose the disc to extremes of temperature or humidity.
7. Keep the discs away from magnetic fields and ferromagnetic materials that may become magnetized. Strong magnetic fields can destroy the data recorded on a disc.

Write Protect

The disc has the capability of being write protected. This feature prevents the accidental erasure of data recorded on the disc. The write protect feature is enabled when the write protect notch on the cover of the disc is uncovered (see Figure 1-7). When the notch is covered, writing is allowed on the disc.

The write protect notch may be covered by placing a tab over the notch on the top side of the disc jacket and then folding the tab over the edge to cover the notch on the bottom side. The installation of the tab is shown in Figure 1-7. The notch must be covered with an opaque material, as it is sensed optically.

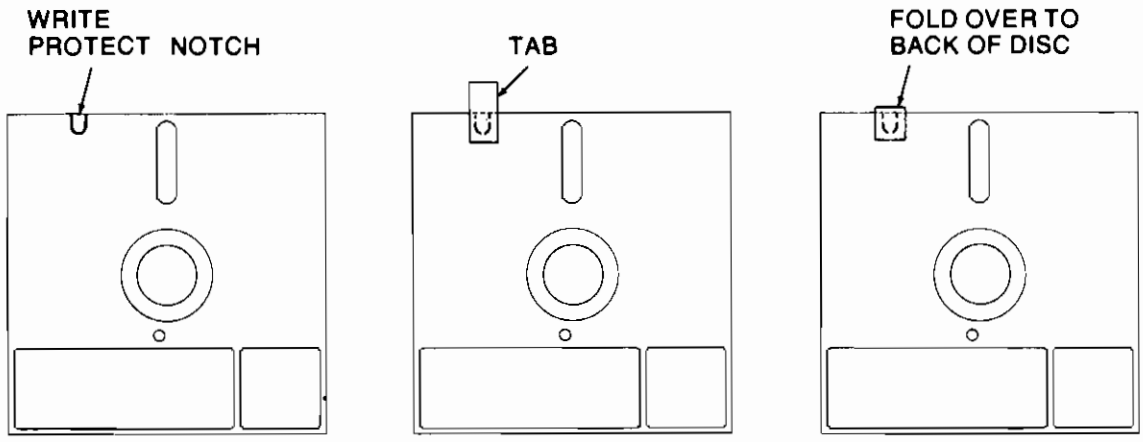


Figure 1-7. Write Enable Method

Operator Controls

There are no operator controls on the 9895A Disc Memory.

Reset Caused by Line Voltage Reduction

If the 9895A experiences a momentary line voltage reduction, or sag, it may lose data bits during a transfer while appearing to operate properly. In order to prevent this situation, the 9895A will go into a Reset mode if a sag of roughly 30% from nominal for about half a second occurs. This warns the operator that data bits may have been lost, so that this condition can be checked for and remedied immediately. There are two ways of recovering from the Reset condition. The power switch may be turned off and then turned back on, or the reset switch on the controller board may be pressed (it is the right-hand switch on the front edge of the controller board).

Chapter 2
Theory of Operation

Introduction

This chapter contains the 9895A theory of operation and block diagrams. The 9895A can be broken down into a controller module, a drive module and a power supply. The controller is described first, then the drive, followed by the power supply.

Controller Module Theory of Operation

Introduction

This section provides a functional description of the controller, part number 09895-66500.

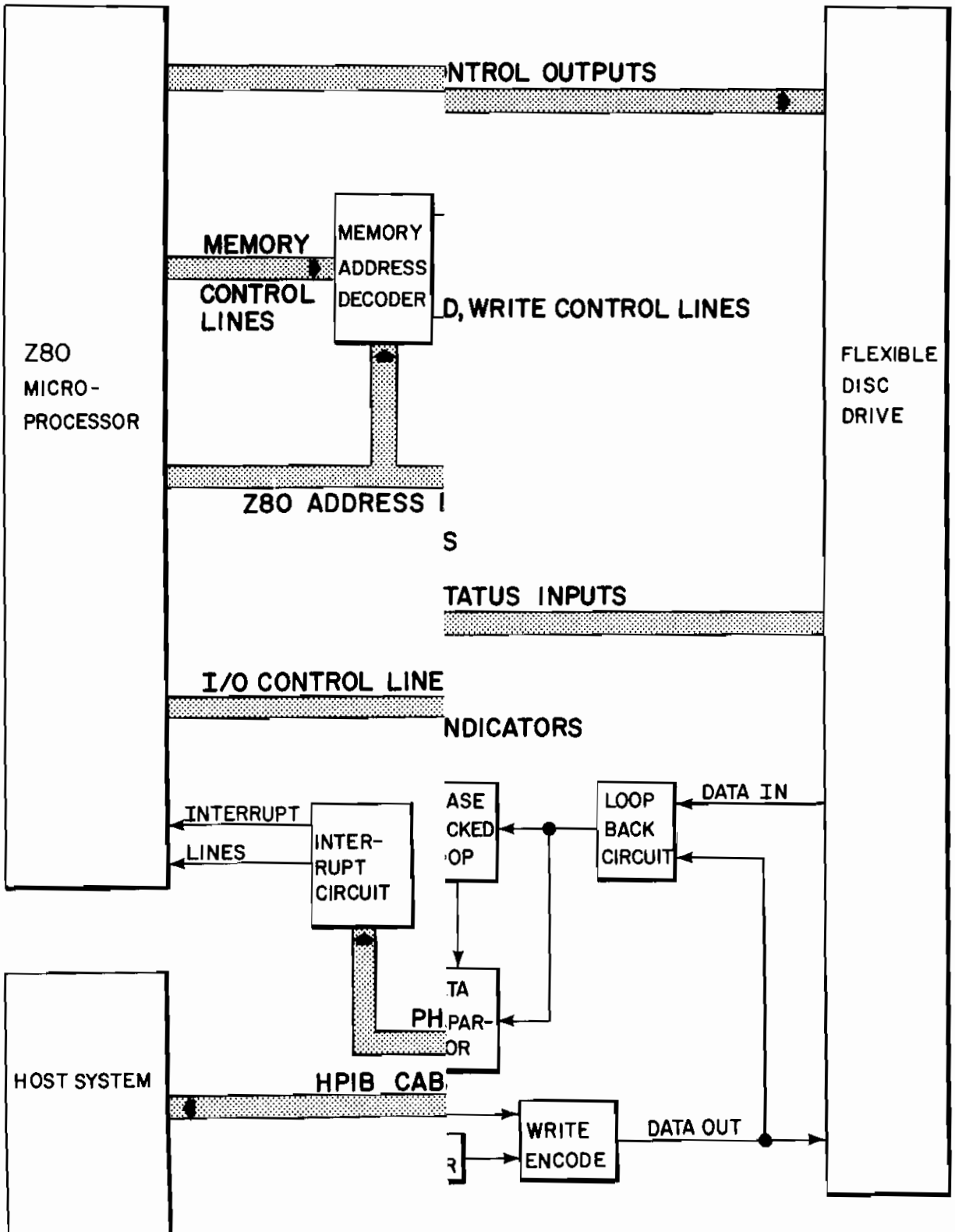
General Description

The controller module provides an interface between a Hewlett-Packard Interface Bus (HP-IB) channel and up to four disc drives. Commands are accepted from the HP-IB channel and interpreted to provide the proper operating sequences for the selected disc drive. This includes:

- Providing control and timing signals,
- Sending data to the disc drive,
- Receiving data from the disc drive,
- Handling all input/output communication with the drive channel.

The controller provides control signals to the drive and receives the resulting status information.

If an error occurs, or when a disc is removed or inserted into a disc drive, the controller requests attention from the HP-IB. It also generates and decodes error detection bits which are recorded with the data. In addition to these normal operations, self-tests are performed on the controller and the disc drives.


Z80
MICRO-
PROCESSOR
MEMORY
CONTROL
LINES
MEMORY
ADDRESS
DECODER
D, WRITE CONTROL LINES
Z80 ADDRESS I
S
TATUS INPUTS
I/O CONTROL LINE
NDICATORS
INTERRUPT
LINES
INTER-
RUPT
CIRCUIT
ASE
CKED
OP
LOOP
BACK
CIRCUIT
DATA IN
TA
PH PAR-
OR
HOST SYSTEM
HPIB CAB
WRITE
ENCODE
DATA OUT
FLEXIBLE
DISC
DRIVE

Controller Interface to HP-IB (PHI Chip)

The PHI chip provides a high-speed interface to the HP-IB via PHI/HP-IB converters for the host system and the Z80. The PHI appears to the Z80 as a bank of eight addressable registers. All interaction with the HP-IB is performed by reading from or writing to these registers. In addition, the PHI chip provides buffering for in-bound and out-bound data through two 8-byte, first-in, first-out buffers (FIFO's) which can be accessed by the host processor. The lines provided by the PHI chip for interfacing to the Z80 include:

- An 8-bit-wide data bus,
- Three register select lines for selecting the eight registers,
- A data direction line for specifying either reading or writing of the selected register,
- Two handshake lines to coordinate data transfer,
- An interrupt line to alert the host processor to selected events.

Four, quad instrumentation bus transceivers are used with the PHI chip for interfacing with the HP-IB. Two transceivers are assigned for 8-bit data transfer between the HP-IB and the PHI chip, and two are used for HP-IB commands and handshakes.

Processor and Memory

The processor on the controller is a Z80A microprocessor. It is a single chip, 4 MHz, 8-bit microprocessor. The Z80A executes the programs stored in four, 2048 x 8-bit Programmable Read Only Memory (PROM) chips or one, 8192 x 8-bit Read Only Memory (ROM) chip to perform the controller functions. Also available are two, 1024 x 4-bit Random Access Memory (RAM) chips for stack operations, scratchpad memory, and buffering the data sent to and from the disc drive.

The Z80A microprocessor is constantly monitoring the PHI chip for in-bound commands from the HP-IB. If it receives a command, the Z80A will execute the necessary programs from ROM to implement the command. On completion, the Z80A goes back to monitoring the PHI chip for a command.

The Z80A communicates with the PHI chip and several registers on the controller via its I/O ports. The PHI chip's registers are assigned I/O ports 10_{16} through 17_{16}, and the controller registers are assigned I/O ports 60_{16} through 67_{16}.

The controller registers contain:

- Status information from the disc drives,
- Control signals sent to the disc drives,
- Status of switches and error indicators on the controller,
- Control signals to enable read, write, and error detection electronics on the controller, the serializer/deserializer (SERDES) registers, and the self-test LED display.

Read Operation

When the Z80A receives a command from the HP-IB to read a sector from the disc, it selects the specified drive, enables the drive to read, and enables the read electronics on the controller. The disc drive begins sending a pulse stream which represents the flux transitions on the disc. The phase locked loop synchronizes to the clock bits recorded with the data to generate a bit clock. The pulse stream is then clocked into the data separator circuit which separates the pulses into clock bits and data bits according to the recording format of the disc. The serial clock and data bits are then shifted into the SERDES shift registers and presented to the Z80A as two 8-bit parallel bytes. The Z80A then reads the I/O ports corresponding to the SERDES registers and stores the data in a RAM buffer. When an entire sector has been read and is stored in the RAM buffer, the Z80A transfers the buffer to the host system via the HP-IB.

Write Operation

When the Z80A receives a write command from the HP-IB, it fills the RAM buffer with a sector of data from the HP-IB. It then enables the write electronics and writes eight bits of parallel data and eight bits of parallel clock to the SERDES. The SERDES changes the parallel clock and data bytes to serial bit streams which are input to the write encoder. The write encoder combines the clock and data bits into a single pulse stream according to the recording format of the disc. This pulse stream, which represents the flux transitions to be stored on the disc, is then sent to the disc drive.

Error Detection

Several types of errors are detected by electronics on the controller. These are CRC error, overrun error and margin error.

The Cyclic Redundancy Check (CRC) is two, 8-bit data bytes that are written on the disc with every sector. As the serial data is sent to the write encoder, it also goes to a CRC chip which computes the CRC for the data stream. After the last data byte is written on the disc, the two CRC bytes are written. When a sector is read back, the separated serial data, including the two CRC bytes, are again input to the CRC chip. The CRC bytes are computed such that when the data field and its CRC are input to the CRC chip, the chip can detect an error in the bit stream. After reading the data field, the Z80A checks a bit in the controller status register to see if a CRC error occurred. If so, the error is reported to the host system via HP-IB.

An overrun error occurs if the Z80A is not sending or receiving data fast enough to keep up with the bits coming off the disc. This is detected by a logic circuit on the controller. At the conclusion of the read or write operation, the Z80A checks a bit in the controller status register to see if an overrun occurred, and notifies the host system accordingly.

A margin error occurs when a clock or data bit occurs too close to the edge of the clock or data window of the bit stream. This does not indicate that the data was read incorrectly, but only that the controller may not be able to read the sector in the future if the bits shift any further within the window. This error is checked by the Z80A following a read operation and reported to the host system only if the host system requests a verify or read verify operation.

Seek Operation

Before reading or writing a sector of data, the controller must position the read/write head of the disc drive over the desired sector. To do this, the controller sends signals to the disc drive to step the head to the desired track. The controller then begins to read the disc. Track and sector information is stored as a preamble to each sector, and the disc is formatted in a manner to allow the controller to detect the beginning of a preamble. On finding a preamble, the Z80A first checks that the track number is correct. If not, it will continue to step the head until the correct track is found. The sector number is then compared. If correct, the Z80A waits for the mark to indicate the beginning of the data field and then begin reading or writing the data field. If incorrect, it passes over this sector and looks for the next until it finds the desired sector. If it can't find the sector after two revolutions of the disc, an error condition is indicated to the host system.

Drive Theory of Operation

Introduction

This section provides a general description of the drive module, part number 09895-69430. Since this module is still being modified, this description will only cover those areas common to all versions.

General Description

The basic function of the drive is to indicate to the controller when it is ready to operate, and respond to the commands of the controller to:

- Receive and generate control signals,
- Position the read/write heads to selected tracks,
- Read or write data on the disc when selected.

Signals received and transmitted by the drive are shown in Table 2-1. Some signals received by the drive are gated with drive select so that no stepping, reading or writing can be performed on an unselected drive. Also, some signals generated within the drive are gated with drive select so that they can't be transmitted from an unselected drive.

Table 2-1. Control, Status and Data Lines Between the Controller and Drive Electronics

Signal	Mnemonic	Function
		Control Signals
Drive Select	DRV0–3	Identifies disc drive with which controller desires to communicate.
Head Load	HEADLOAD	Loads the heads and locks the door on the unit identified by Drive Select.
Head Select	HEADSEL	Selects head 1 when active, head 0 otherwise.
Low Current	LOWCURR	Reduces write current on inner tracks to decrease bit shift.
Move In	MOVEIN	Causes heads to move toward center of disc when active during a Step command. Heads move away from center when active during a Step command.
Step	STEP	Causes heads to move in direction specified by MOVEIN.
Write Enable	WRITDRV	Places disc drive in write mode when active.
		Status Signals
Disc Change	DISCHNG	Asserted when the selected drive is either not ready (due to no disc) or has a new disc inserted.
Disc Two-Sided	TWO-SIDE	Asserted when disc is found to be two-sided.
Index	INDEX	Asserted when index hole in disc passes photodetector.
Ready	READY	Asserted when a disc in the selected drive has rotated for at least two revolutions.
Track Zero	TRACK0	Asserted when heads are positioned at track zero.
Write Protect	WRPROT	Asserted when disc in selected drive is write protected.
		Data Lines
Read Data	RDATA	Carries read data to the controller from the drive.
Write Data	WDATA	Carries write data to the drive from the controller.

During the write operation, the selected drive must have head-load, head select, write enable and write data signals. During the read operation, the selected drive will perform a head load. The write enable line remaining high implies a read operation. Under these conditions the drive will transfer read data to the controller. Controller step and direction commands are received initiating a track-seek operation on a selected drive. The selected drive transmits a track 00 signal to the controller whenever the read/write heads are at track 00.

Positioning the carriage-mounted read/write heads is accomplished by a band-driven stepper motor. Each step command from the user system increments the stepper motor which, in turn, moves the band. The band increments the read/write heads one track for each step command.

A read or write operation begins by placing the read/write heads in contact with the disc with a Head-Load command at the desired track. To write on the disc, write enable is sent by the controller to condition the write logic. The write current then in the head reverses polarity synchronous with the high-to-low transitions of the write-data pulses from the controller. The current reversals cause magnetic flux reversals on the desired disc track. Erasure of previously recorded data is simultaneously accomplished during the writing operation in addition to a delayed tunnel erase which ensures disc interchangeability.

To read from the disc, magnetized bits in the format of the pre-recorded data are sensed by the read/write heads. This signal is amplified, digitized and transmitted to the controller.

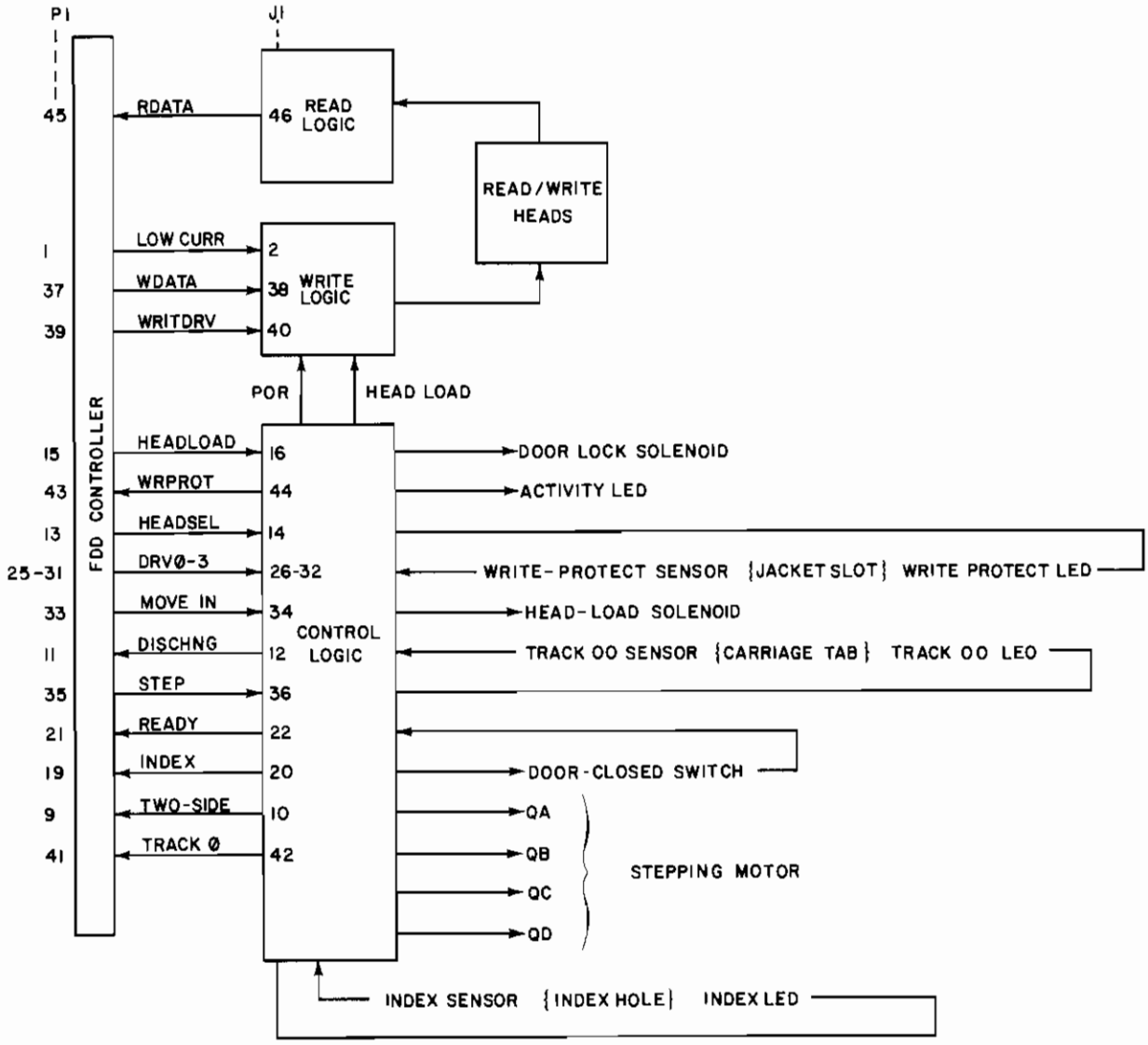


Figure 2-2. Drive Block Diagram

Power Supply Theory of Operation

Introduction

This section provides a general description of the power supply, which includes the power module, part number 09895-67910, and the associated ac input circuitry mounted on the chassis and fan compartment.

General Description

Ac power enters through fuse A3F1 and is switched by S1, the front panel power switch. It passes through S2 and S3, the voltage selection switches, into the proper windings of transformer T1. T1 has three secondary windings.

One secondary winding supplies rectifier CR10 through fuses A1F1 and A1F2. CR10 supplies unregulated +12 volts and −12 volts. The +12 volt line is regulated to +5 volts by U1, an LM723 voltage regulator, which functions by changing the bias on Q1, a Darlington pass regulator. U1 receives inputs from the current limiter (U2 pin 1), regulated +5V line and regulated +12V line (see next paragraph). U2 senses the voltage across R4. As the current through R4 increases, the voltage across it increases. When it reaches a predetermined threshold, pin 1 changes rapidly from zero to +12 volts, turning VOUT of U1 off, which turns Q1 off. +5V enters the inverting input of U1 and +12 volts biases CR7, a 4.99 volt precision zener diode at the non-inverting input. Note that in this configuration there will be no +5 volts until the +12 volt line is up. CR4 and CR5 form a crowbar. CR5 conducts when the potential across it reaches 6.19 volts, turning on CR4 which blows fuses F1 and/or F2, or current limits the +5 volt supply. U2 and U3 produce the PON signal. U3 produces a power-up signal when the potential on pin 2 reaches 4.75 volts (which occurs after a time delay to charge C12).

Another secondary winding supplies rectifier CR1 through fuse F3. CR1 supplies unregulated +24 volts. U4 is a +12 volt regulator. CR8 and CR9 form a crowbar. When the potential on CR9 exceeds 14.7 volts, it conducts, turning CR8 on, which shorts the +24 volt line to ground, blowing fuse F3. Note that the crowbar operates from the +12 volt line, but affects the +24 volt line. CR2 and CR3 are negative voltage protection.

The third secondary winding provides 120 Vac for the fan motor and the drive motors.

Functional Characteristics and Communication Protocol

Introduction

This section describes the recording formats used in the HP disc memory and the HP disc command set.

Recording Formats

The HP disc drive supports both the HP Standard Disc Format (hereafter referred to as the HP Format) and the IBM (IBM 3740) Standard Data Interchange Format (hereafter referred to as the IBM Format). Format similarities and differences are described in the following paragraphs.

Format Similarities

The following features are common to both the IBM Format and the HP Format.

Media. A double-sided disc is used as the recording medium. The disc is composed of recording material and is enclosed in a square plastic jacket. An index hole in the disc is used to provide a rotational position reference. The disc drive will also accept a single-sided disc. Single-sided discs must be used for the IBM Format mode of operation.

Tracks. There are 77 physical tracks on each side of the disc, with a spacing of 0.0208 inch between track centers (48 tracks per inch). The outermost track is Track 0 and the innermost track is Track 76.

Recording. Information is stored on the disc as a series of magnetic flux reversals. Since a single head is used to read from and write on each side of the disc, a self-clocking code must be used to store the information.

The portion of the disc or the duration of the time used to store a single bit is referred to as a bit cell. The first part of the bit cell is called the clock window and the remainder of the bit cell is called the data window. A flux reversal in the clock window is called a clock transition and a flux reversal in the data window is called a data transition. A bit cell that contains a data transition stores a 1 and a bit cell with no data transition stores a 0.

Track Format. Each track is divided into sectors, as shown in Figure 2-3. The data contained in one sector is the smallest amount of information that can be written at a time. The disc is soft-sectored, that is, there is no hardware indication of where each sector starts. Instead, the beginning of each sector is indicated by information recorded on the disc.

In order to allow soft-sectoring, each sector is divided into two fields. First, there is an ID field which contains information to identify the sector. Next, there is a data field which contains the actual data. The ID field is written only when the disc is formatted, never during actual operation. Thus, an ID field serves as a fixed marker for the beginning of each sector. The entire data field is re-written each time a write operation occurs to the sector.

The makeup of the ID and data fields is similar. Both fields start with a series of sync-up bytes. These bytes end with a long string of identical bits. During a read, the bit string allows the controller's decoder circuitry time to synchronize itself with the data on the disc. Next comes an address mark byte, which indicates that the beginning of an ID or data field has been found. The data stored in this byte indicates which type of field it is part of. In order that no other byte can be mistaken for an address mark, the address mark byte contains an abnormal pattern of clock transitions. The first bit of an address mark is the opposite type from the last bit of a sync-up field. This feature simplifies detection of address marks.

Following the address marks comes a series of information bytes. In an ID field, these bytes indicate the logical track, head and sector address. In a data field, these bytes are the data being stored in the sector.

At the end of each field are two Cyclic Redundancy Check (CRC) bytes. These bytes allow the detection of most errors that occur in the storage and recovery of information from the disc.

There are gaps between each field on a track. The gaps allow for variations in disc rotational speed. The sectors are logically numbered consecutively. However, the sectors may occur in any physical order around the track. This allows the sectors to be staggered to optimize system performance.

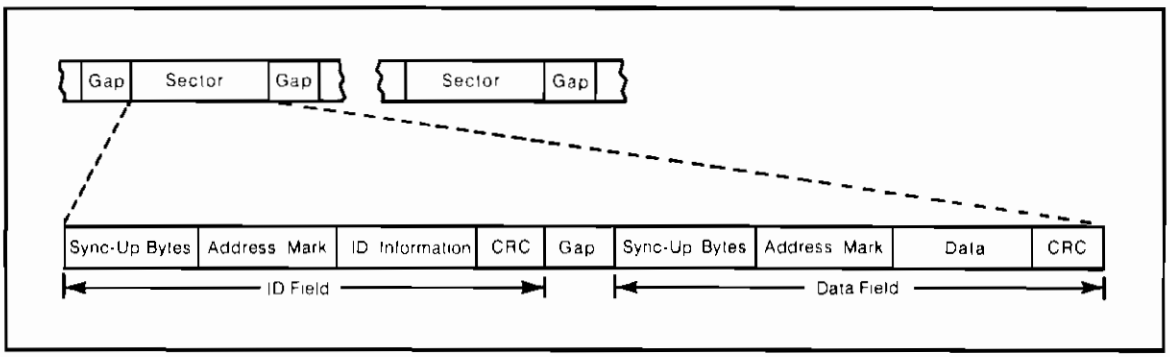


Figure 2-3. Track Format

Track Numbering. Each track has a physical address as previously described. There is also a logical track address associated with each good track. The logical track address is written in the ID field of each sector on the track. If a disc has no bad tracks, the logical address of a track is the same as the physical address.

A disc with N bad tracks can be made to look like a 77 − N track disc with no bad tracks. To do this, the logical track address stored in the ID field of each sector of every bad track is set to !FF. Tracks of this type are known as invisible tracks. All visible tracks are then sequentially assigned logical track numbers. Logical Track 0 is the outermost good track, not necessarily physical Track 0.

Format Differences

Table 2-3 summarizes the principal differences between the IBM Format and the HP Format. Details of these differences are provided in the following paragraphs.

Coding. The IBM Format uses a single-density encoding scheme known as frequency modulation (FM). The rules for FM coding are as follows:

- A 0 bit cell has no data transition.
- A 1 bit cell has a data transition.
- Every bit cell has a clock transition.

The minimum distance between transitions is one-half the bit cell, that is, the distance from a clock transition to a data transition.

Table 2-3. Format Differences

Feature	HP Format	IBM Format
Usable Physical Tracks	0 − 76	0 − 76
Sectors Per Track	30	26
Sector Numbering	0 − 29	1 − 26
Bytes Per Sector	256	128
Data Order	LS Byte First LS Bit First	MS Byte First MS Bit First
Coding	MMFM	FM
Precompensation Required	Yes	No
Sync-Up Bytes	Four Bytes of !00 And Four Bytes of !FF	Six Bytes of !00
Address Marks	Extra Clock Transitions	Missing Clock Transitions
CRC Includes Address Mark	No	Yes

The HP Format uses a double-density encoding scheme known as Modified Modified Frequency Modulation (MMFM). The rules for MMFM coding are as follows:

- A 0 bit cell has no data transition.
- A 1 bit cell has a data transition.
- A 0 bit cell has a clock transition if there is no transition in the preceding bit cell.
- A 1 bit cell never has a clock transition.

For the same recording density (flux transitions per inch), there are twice as many data transitions in MMFM coding as in FM coding.

Precompensation. Transitions which are written close together tend to appear shifted apart when they are read back. This effect is known as bit shift. Due to its large bit cell, the IBM Format is not affected by bit shift. However, because of the smaller bit cell used in the HP Format, bit shift is noticeable. To compensate for bit shift, certain MMFM transitions are written closer together. This action is called precompensation. The actual precompensation used on a transition is dependent upon the pattern being recorded.

Address Marks. There are four types of HP address marks. All are unique in that they include a bit cell with an extra clock transition. The HP address mark byte is not included in CRC generation. Address mark is abbreviated AM.

Name	Data Pattern	Clock Pattern	Where Found
ID AM	!70	!0E	ID Field
Defective Track AM	!F0	!0E	ID Field
Data AM	!50	!0E	Data Field
ECC Data AM	!D0	!0E	Data Field

At the command set level, a clear D bit indicates an ID AM in the ID field, and a set D bit indicates a defective track AM in the ID field.

There are four types of IBM Format address marks. All are unique in that they include bit cells which contain no clock transition. The IBM address mark byte is included in CRC generation.

Name	Data Pattern	Clock Pattern	Where Found
Index AM	!FC	!D7	At Index Hole
ID AM	!FE	!C7	ID Field
Data AM	!FB	!C7	Data Field
Deleted Data AM	!F8	!C7	Data Field

! = Hexadecimal

At the command set level, a clear D bit indicates a data AM in the data field and a set D bit indicates a deleted data AM in the data field.

Presently, all data fields contain a data AM. If error correcting code (ECC) bytes are added to the data field in the future, an ECC data AM will be used, allowing interchange between ECC and non-ECC systems.

Track Format. Detailed track formats for the HP Format and IBM Format are shown in Figures 2-4 and 2-5, respectively.

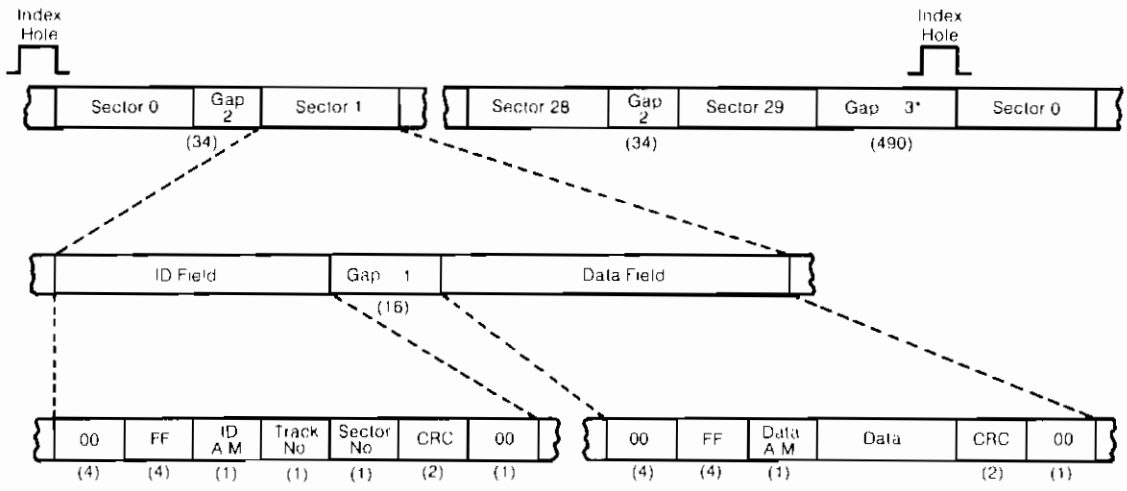
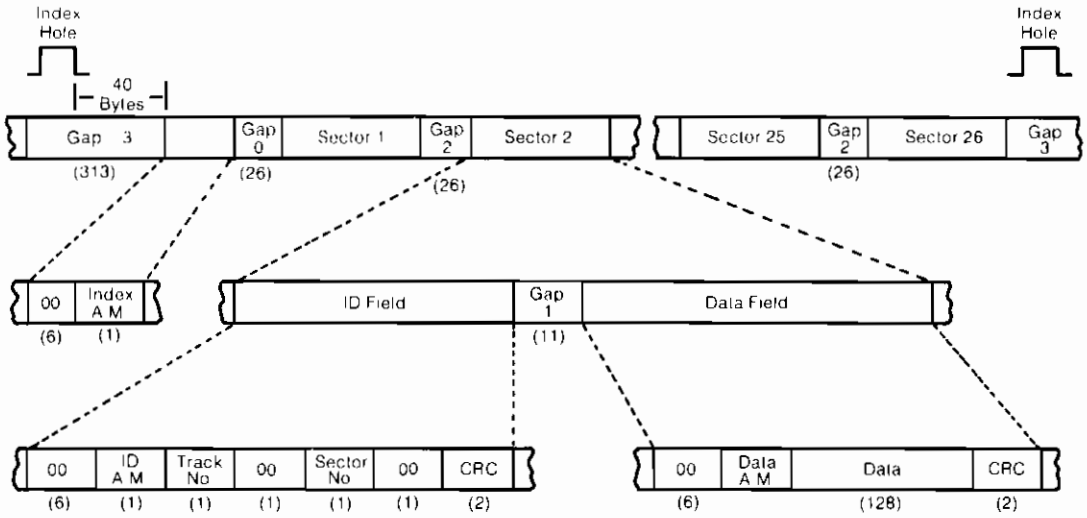


Figure 2-4. Hewlett-Packard Standard Sector Recording Format



(X) = Number of Bytes

Gap	Length (Bytes)	Hex Value
0	26	FF
1	11	FF
2	26	FF
3	313 (Approx.)	FF

Figure 2-5. IBM Standard Sector Recording Format

Chapter 3
Maintenance

Introduction

This section contains recommended service procedures and a list of equipment and special tools needed for the procedures. It also contains disassembly and re-assembly instructions.

WARNING

TO AVOID PERSONNEL INJURY AND/OR DAMAGE TO EQUIPMENT, OBSERVE ALL WARNINGS AND CAUTIONS STATED IN THIS PUBLICATION AND AS DETAILED BELOW.

USE EXTREME CAUTION WHEN WORKING ON THE DISC DRIVE WITH POWER APPLIED. HAZARDOUS VOLTAGES ARE PRESENT INSIDE THE DISC DRIVE WHENEVER IT IS CONNECTED TO AN ACTIVE AC POWER SOURCE.

DO NOT ATTEMPT TO REMOVE OR CHANGE PRINTED CIRCUIT ASSEMBLIES OR INTERCONNECTING CABLES WITHOUT FIRST REMOVING POWER FROM THE DISC DRIVE.

CAUTION

NEVER ALLOW THE HEADS TO TOUCH EACH OTHER. WHENEVER THE HEADS ARE DETACHED FROM THE HEAD LOAD PLATE, PLACE A PIECE OF CLEAN LENS TISSUE BETWEEN THEM TO PREVENT THEM FROM TOUCHING.

THE READ/WRITE HEADS ARE FACTORY ALIGNED WITH A FOUR-TRACK OFFSET BETWEEN THE HEADS. LOOSENING THE HEAD-MOUNTING SCREW WILL DESTROY THIS OFFSET AND NECESSITATE THE RETURN OF THE DISC DRIVE FOR RE-ALIGNMENT.

DO NOT LUBRICATE THE DISC DRIVE – OIL WILL CAUSE DUST AND DIRT TO ACCUMULATE.

DO NOT TOUCH THE HEADS OR ATTEMPT TO CLEAN THEM.

Standard Test Equipment

An oscilloscope (HP 1707B oscilloscope or equivalent) is the only piece of standard test equipment required to service the disc drive. The oscilloscope is used primarily to check the alignment of various components in the disc drive and for troubleshooting.

Special Tools

Table 3-1 lists the special tools required to service the disc drive.

Table 3-1. Special Service Tools

Tool	HP Part Number
Diagnostic Tape	98041-90010
Status Display Board	09895-66506
Alignment Disc	9164-0111

WARNING

THE INFORMATION GIVEN IN THIS SECTION IS FOR TRAINED SERVICE PERSONNEL ONLY. TO AVOID POTENTIALLY SERIOUS ELECTRICAL SHOCK, DO NOT PROCEED FURTHER IN THIS SECTION UNLESS QUALIFIED TO DO SO.

Disassembly Procedures

Introduction

This section provides detailed disassembly and reassembly procedures for those assemblies which are field replaceable.

Adjustments and/or checks must be performed following the replacement of certain items in the unit. A list of required procedures is furnished as the last step in each disassembly procedure.

The disassembly procedures are presented in a manner such that assemblies which block access to other assemblies are listed first.

Cover Panels

Front cover is removed by pulling outward on lower outside corners of disc insertion openings.

Remove the top cover by placing the unit on a broad, flat object (such as a book), so that the feet are off the surface. Remove the four recessed screws (two per side) on the exposed front panel, and the two screws in the lower corners of the back of the unit. Then slide the cover back and off of the unit.

Bottom cover is attached by five screws which are exposed when the top cover is removed.

Controller Module

1. Remove power from unit.
2. Remove front cover panel.
3. Remove the connector retaining bracket on lower right side of unit.
4. Remove connector on right side of controller module.
5. Rotate the two board extractors and then remove the controller board.

CAUTION

TO PREVENT POSSIBLE DAMAGE TO THE CONTROLLER BOARD DURING REMOVAL OR REINSTALLATION, CARE MUST BE TAKEN TO INSURE THAT THE BOARD REMAINS IN ITS GUIDE TRACKS.

If the controller board is loose in the guides, perform the following steps to adjust the controller board guide:

1. Remove the drive assemblies.
2. Set the 9895A on its side or rear surface.
3. Make sure that the controller board is completely seated in the connectors.
4. Loosen the guide screws and press on the guide so that it fits firmly against the side of the controller board.

5. Tighten the guide screws.

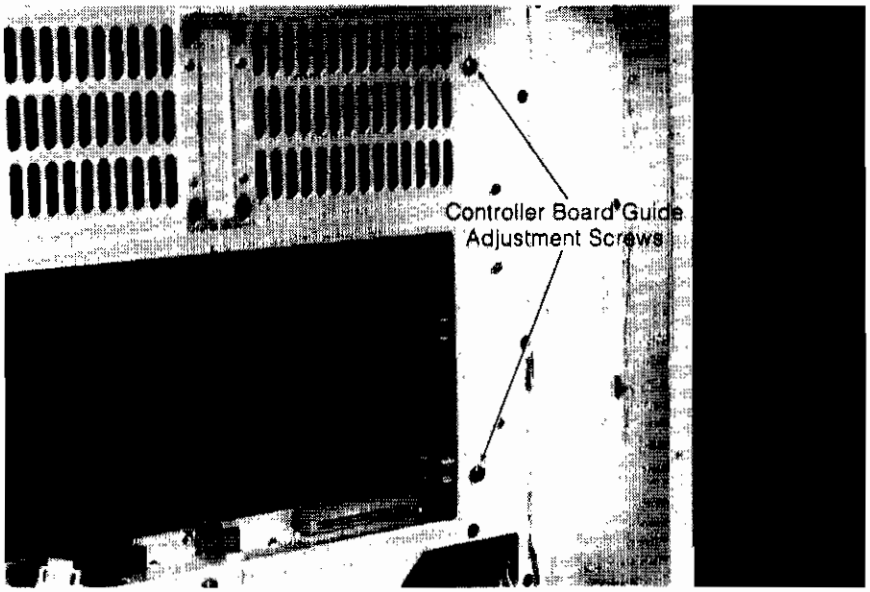


Figure 3-1. Controller Board Guide Adjustment

The controller module is installed by reversing this procedure. Make sure that all connectors are seated firmly.

Drive Module

The drive mechanics module is removed by the following method:

1. Remove power from unit.
2. Remove top, bottom and front covers.
3. Remove controller board.
4. Remove two screws fastening drive to side of chassis, and two screws fastening drive to bottom of chassis.
5. Remove ac connector and dc connector.
6. Slide drive forward, while loosening rear edge connector.
7. Remove drive through front of unit.

The drive module is installed by reversing this procedure. Make sure that the two longer screws go in the bottom and the two shorter screws go in the side.

Fan Compartment

The fan compartment can be removed by the following procedure:

1. Remove power from the unit.
2. Loosen four screws at corners of compartment; back them out about 1 inch.

3. Pull compartment away from mainframe, then reach inside to unplug the main power cord and the fan power cord.

The fan compartment can be installed by reversing this procedure.

Power Module

The power module is removed by the following method:

1. Remove the top cover and fan compartment.
2. Remove two connectors on front of power module.
3. Remove four screws fastening module to rear of unit.

The power module is installed by reversing this procedure. Make sure that all connectors are seated firmly.

Drive Electronics Board

NOTE
Changing the drive electronics board is not a recommended procedure. If it is defective, the entire drive module should be exchanged. This procedure is included for reference, only.

1. Remove drive module.
2. Disconnect harnesses from connectors on printed circuit board.
3. Remove screw from printed circuit board adjacent to connector J1.
4. Remove board by detaching it from the four push-in clips.
5. To replace printed circuit board, push clips through printed circuit board.
6. Replace screw adjacent to connector J1.
7. Re-connect harnesses.
8. Set dipswitch S1, if applicable.
9. Make sure that jumpers are configured properly (jumpers are listed in the appendix).
10. Perform Burst-to-Index check and adjust as necessary.

Drive Motor Assembly

NOTE
Changing the drive motor assembly is not a recommended procedure. If it is defective, the entire drive module should be exchanged. This procedure is included for reference, only.

1. Perform removal procedure for drive board.
2. Loosen screws securing drive motor capacitor.
3. Remove ground screw and cable clamps.
4. Remove ac connector from bracket.
5. Remove spindle drive belt.
6. Remove three nuts securing drive motor.
7. Remove drive motor assembly (drive motor, capacitor and ac connector).
8. To replace drive motor assembly, perform, in reverse order, steps 7 through 1.

Front Plate

The front plate is removed by the following method:

1. Remove the four screws fastening the top cover to the front plate.
2. Remove the six screws fastening the front plate to the chassis.
3. Pull the front plate forward and to the left.

Maintenance

Introduction

This section contains the troubleshooting and corrective maintenance information required to maintain correct operation of the 9895A. No preventive maintenance is required.

Troubleshooting

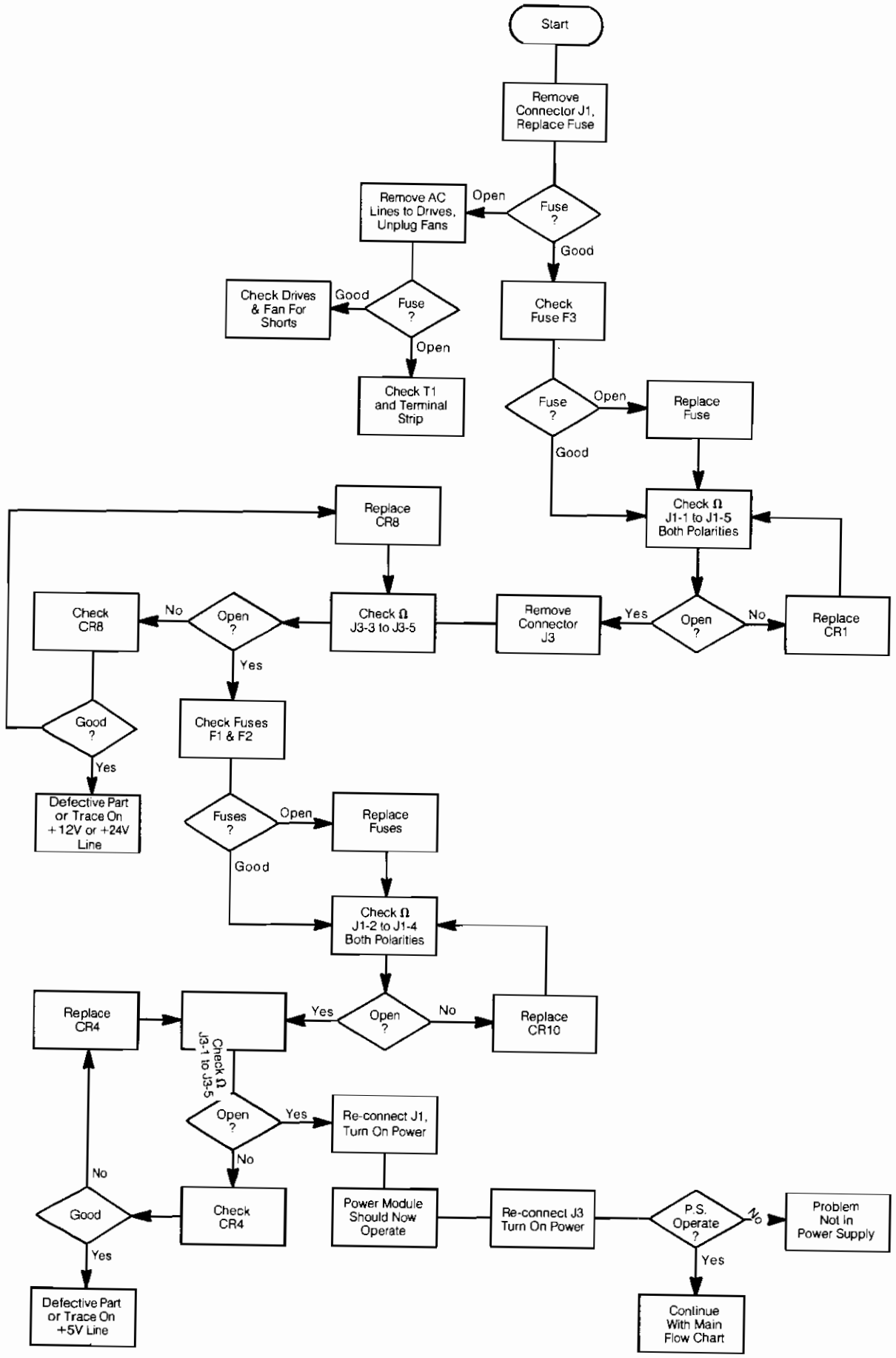
Nearly all of the working parts of the 9895A are mounted on modules which are furnished in the Service Kit as exchange items. Thus, the basic troubleshooting scheme consists of isolating problems to a specific module by common sense techniques, and then exchanging the module. If this is not a practical method, several other approaches are provided.

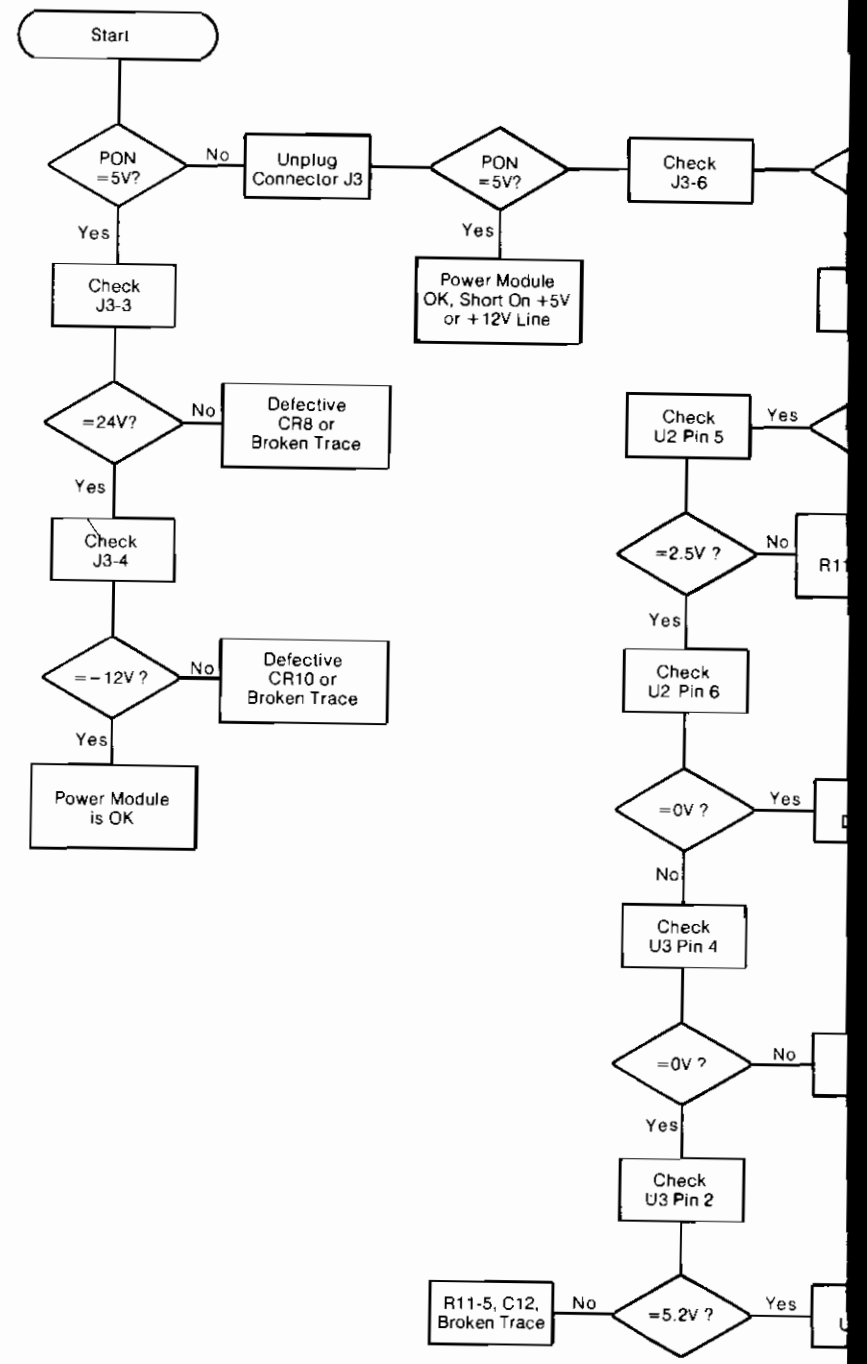
Schematics. Full schematics are provided for all electronics except the drive module. The drive module is still evolving so a final version is not yet available. The schematics are provided in a separate packet for ease of use.

Status Display Board Diagnosis. The 09895-66506 Status Display Board may be used to obtain a large amount of information about the operation of the controller and drive modules. Procedures for use are detailed in Chapter 4. The Status Display Board is included in the 09895-67100 Service Support Package.

Error Messages. Appendix B contains a list of error messages for systems consisting of a 9895A and certain mainframes.

Power Supply Flowcharts. The power supply, which consists of the power module (09895-67910) and chassis-mounted ac input circuit, is quite easy to troubleshoot if circumstances require. Problems can be narrowed down quickly by checking the fuses and by noting which supply voltages are missing. Two flowcharts have been provided in order to facilitate this process. A short chart diagnoses problems in units with open line fuses. A


Start
Remove Connector J1, Replace Fuse
Fuse ?
Open
Good
Remove AC Lines to Drives, Unplug Fans
Fuse ?
Good
Open
Check Drives & Fan For Shorts
Check T1 and Terminal Strip
Check Fuse F3
Fuse ?
Open
Good
Replace Fuse
Check Ω J1-1 to J1-5 Both Polarities
Replace CR8
Check CR8
Open ?
No
Yes
Check Ω J3-3 to J3-5
Remove Connector J3
Open ?
Yes
No
Replace CR1
Good ?
Yes
Defective Part or Trace On +12V or +24V Line
Check Fuses F1 & F2
Fuses ?
Open
Good
Replace Fuses
Check Ω J1-2 to J1-4 Both Polarities
Replace CR4
Check Ω J3-1 to J3-5
Open ?
Yes
No
Re-connect J1, Turn On Power
Open ?
Yes
No
Replace CR10
Good
No
Yes
Check CR4
Power Module Should Now Operate
Re-connect J3 Turn On Power
P.S. Operate ?
No
Yes
Problem Not in Power Supply
Defective Part or Trace On +5V Line
Continue With Main Flow Chart


Start
PON =5V?
No
Unplug Connector J3
PON =5V?
Check J3-6
Yes
Power Module OK, Short On +5V or +12V Line
Yes
Check J3-3
=24V?
No
Defective CR8 or Broken Trace
Yes
Check J3-4
=−12V ?
No
Defective CR10 or Broken Trace
Yes
Power Module is OK
Check U2 Pin 5
Yes
=2.5V ?
No
Yes
Check U2 Pin 6
=0V ?
Yes
No
Check U3 Pin 4
=0V ?
No
Yes
Check U3 Pin 2
R11-5, C12, Broken Trace
No
=5.2V ?
Yes

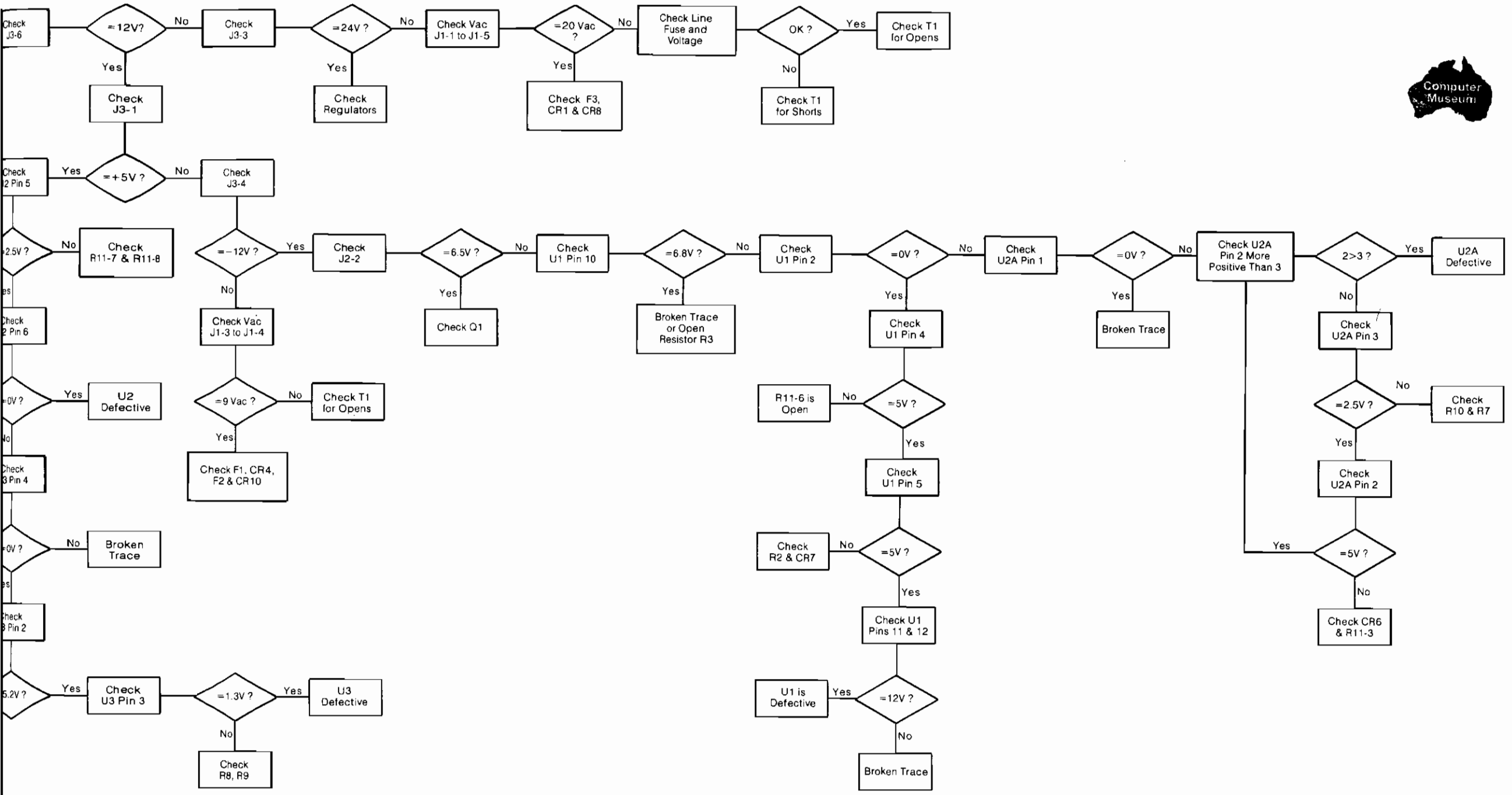


Figure 3-2. 9895A Power Supply Troubleshooting Charts

longer flowchart details how to troubleshoot a partially functioning module, and how to verify correct operation.

The quickest way to check the power module is to measure the voltage of the PON signal (J3-2) while connected to the load. If it is +5 Vdc, the module is probably functioning properly. Just check the +24 Vdc line (J3-3) and the −12 Vdc line (J3-4) to verify proper operation. If PON is low, disconnect J3 and re-check PON. If it is now +5 Vdc, there is an external short on either the +5V line or the +12V line. If PON is still low, refer to the flowcharts.

The module may be operated with the load removed, thereby making it easy to determine whether a problem is in the module or in the load. Note that the module may operate differently when unloaded, due to the current limiting action of R4-U2, and that the supply voltages may be slightly higher when unloaded.

DC Voltage and Signal Check of Drive Module

1. Input dc power should be +5 Vdc ±5% at pin 5 of the dc connector (pin 6 is +5V return), and +24V ±10% at pin 1 (pin 2 is +24V return).
2. Various detector functions can be checked by observing the dc level at the board connector. Table 3-2 contains a list of these functions and the point to check for the signal.

Table 3-2. Detector Functions

Function	Connector, Pin 2 Wire Color
Write Protect	J5-12 Red
Track 0	J6-3 Red
Index (Single-Sided)	J6-5 Black
Index (Double-Sided)	J6-6 Purple
Door Closed	J5-2 Yellow

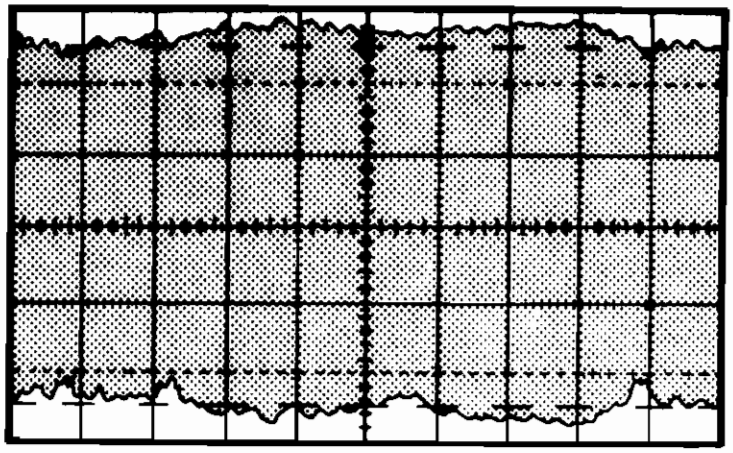
3. Certain functions used in the adjustment procedures have built-in test points. These functions are listed in Table 3-3.

Table 3-3. Adjustment Test Points

Function	Test Point
Differentiated Analog	1
Read Data (Differential)	2
Analog Read Data	3
Differential	4
Ground	15

SCOPE SETTINGS:

200mv/cm
20ms/cm



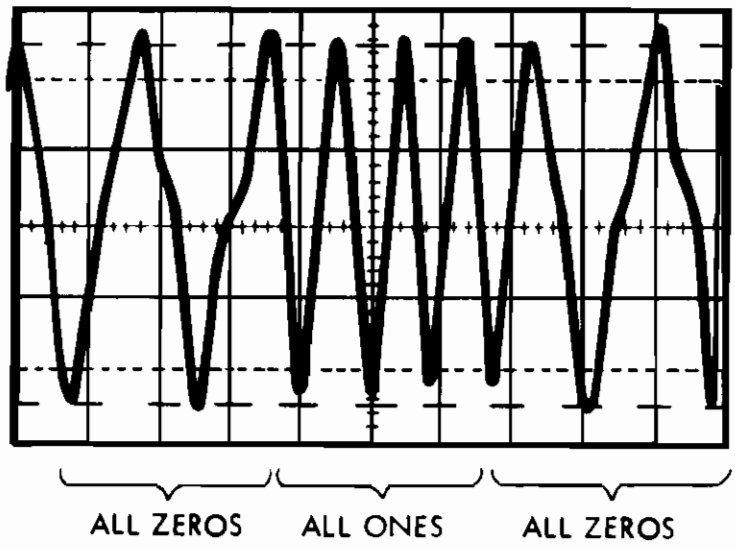
TP3 AND TP4

APPROX. AMPLITUDE RANGE,
INNER TO OUTER TRACKS:
100mv - 1100mv ALL ONES
300mv - 1200mv ALL ZEROS

Figure 3-3. Differential Read Signal for Entire Track

SCOPE SETTING:

200mv/cm
10us/cm



TP3 AND TP4

Figure 3-4. Differential Read Signal for Portion of Outer Track

Corrective Maintenance Procedures

There are no corrective maintenance procedures for the power module or the controller, except replacement. There are a number of corrective adjustments for the drive module. This section contains these adjustments. They are listed in Table 3-4.

Table 3-4. Adjustment Reference List

Index-to-Burst Check and Adjustment

Alignment disc (9164-0111) is used to perform this procedure.

1. Disassemble the 9895 and set it up as shown in Figure 3-5.

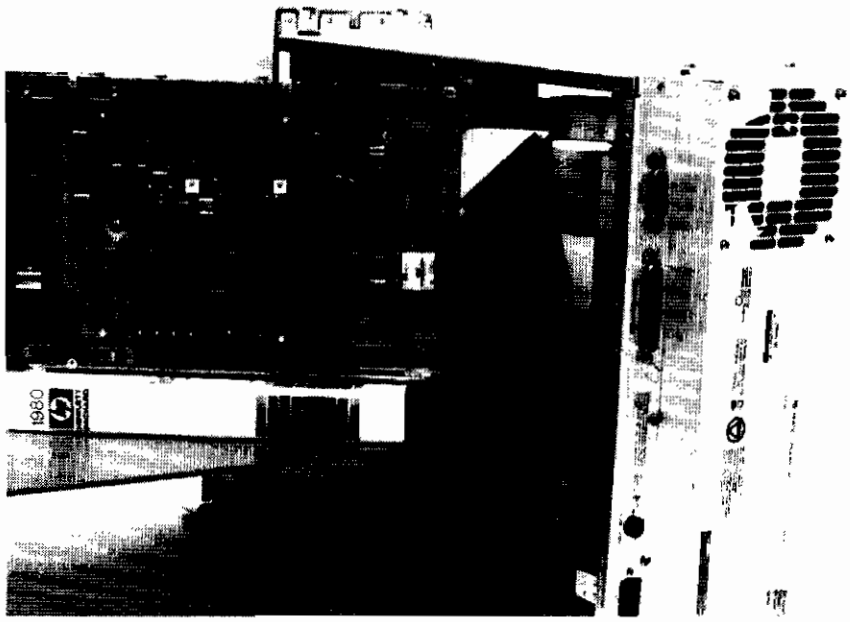


Figure 3-5. Alignment/Adjustment Test Setup

2. Precondition the alignment disc by allowing it to reach room temperature for one hour.
3. Install the alignment disc.

CAUTION

THE ALIGNMENT DISC IS FOR READ ONLY. EXTREME CAUTION SHOULD BE USED TO ASSURE THIS DISC IS NOT WRITTEN ON.

---

4. Seek to Track 0, then seek to Track 1 and Read on Head 0. (No data is recorded on Track 1.)
5. Connect Channel 2 of scope to TP3 (inverted) on the drive board, Channel 1 to TP4 of the drive board and the External Trigger Input to U20-8. Set up the scope as follows: (Refer to Figure 3-5)

Channel 1	2 Volt/Division ac - connect to TP3 (inverted)
Channel 2	0.1 Volt/Division ac - connect to TP4
GND Lead	Connect to TP15
Vertical Mode to:	Add
Slope (Sync) to:	Positive
Trigger Source to:	External - U20-8
Trigger Coupling to:	Low Frequency (High Frequency Reject)
Trigger Mode to:	Normal
Time Base to:	50 μSeconds/Division

6. The time from Index pulse to write-splice bit should be 200 μSeconds, ±100 μSeconds (refer to Figure 3-6). To adjust the write Index-to-Burst time, loosen the single-sided sensor setscrew holding the (single-sided-sensor) phototransistor located on the bottom of the chassis toward the front of the unit (Figure 3-5). Using the adjustment tab protruding through the casting, move the phototransistor until the specification is met. Tighten the setscrew while observing the scope signal. Verify that the adjustment did not change.
7. All scope settings are to remain as defined in the original setup in Step 4, but it may be necessary to slightly adjust the sync. Seek to Track 0 then seek to Track 1 and perform a read. While observing the signal on the scope, remove and re-insert the disc three times.

   After each insertion, verify that the change in the time from Index to write splice is less than 50 μSeconds.

   Repeat Steps 2 through 6 using Alignment Disc for the two-sided sensor adjustment tab and its associated setscrew, as required. (Head 1)

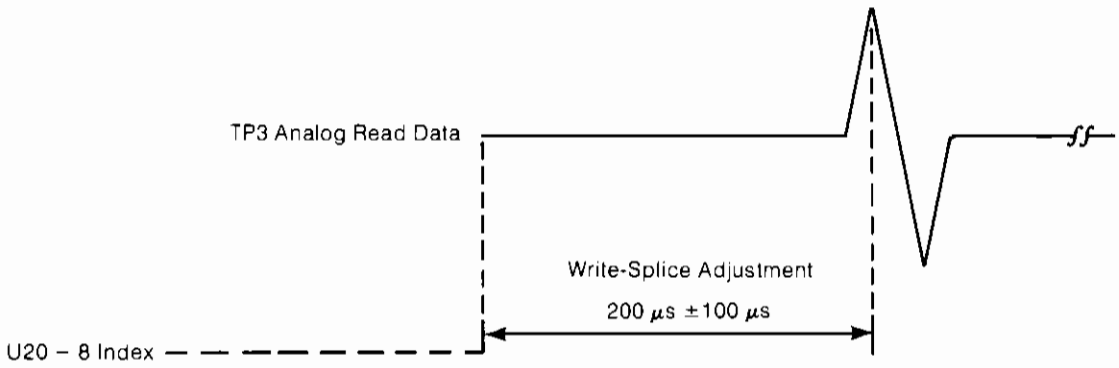


Figure 3-6. Index Pulse to Write-Splice Bit Timing

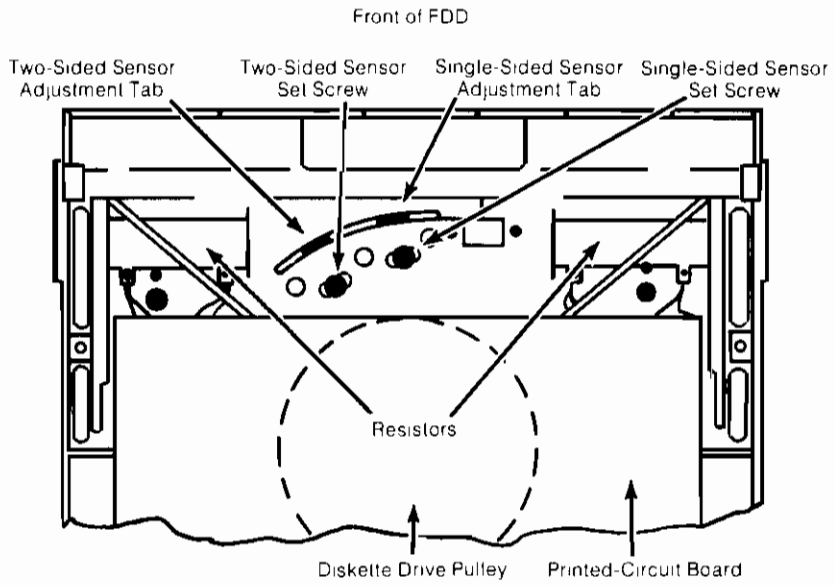


Figure 3-7. Single- and Two-Sided Sensor Adjustment Means

Radial Alignment

CAUTION

RADIAL ALIGNMENT IS NOT A RECOMMENDED PROCEDURE. IF THE RADIAL ALIGNMENT IS INCORRECT, THE ENTIRE DRIVE MODULE SHOULD BE EXCHANGED. THIS PROCEDURE IS INCLUDED FOR REFERENCE, ONLY.

The purpose of the radial alignment procedure is to establish a standard adjustment among all drives, in order to ensure interchangeability of media between all drives. It is important, therefore, that the radial alignment performed in the field follow as closely as possible the factory alignment procedure.

The factory alignment procedure compensates for temperature and humidity. It is desirable that the procedure be performed at or as close as possible to normal living conditions.

1. Precondition the alignment disc by exposing it to room temperature for one hour.
2. Install the alignment disc.

CAUTION
THE ALIGNMENT DISC HAS SPECIAL ALIGNMENT DATA RECORDED ON IT. EXTREME CAUTION SHOULD BE EXERCISED TO PREVENT THIS DISC FROM BEING WRITTEN ON.

3. Set up the scope as follows:

Channel 1:	.1 Volts/Division ac
Channel 2:	.1 Volts/Division ac (inverted)
Vertical Mode:	Add
Slope (Sync):	Negative
Trigger Source:	External
Trigger Coupling:	Low Frequency (High Frequency Reject)
Trigger Mode:	Normal
Time Base:	20 ms/Division

4. Connect the scope as follows:

Channel 1 to TP3
Channel 2 to TP4
External Sync to Index at U20 Pin 8

Refer to Figure 3-8 for locations.

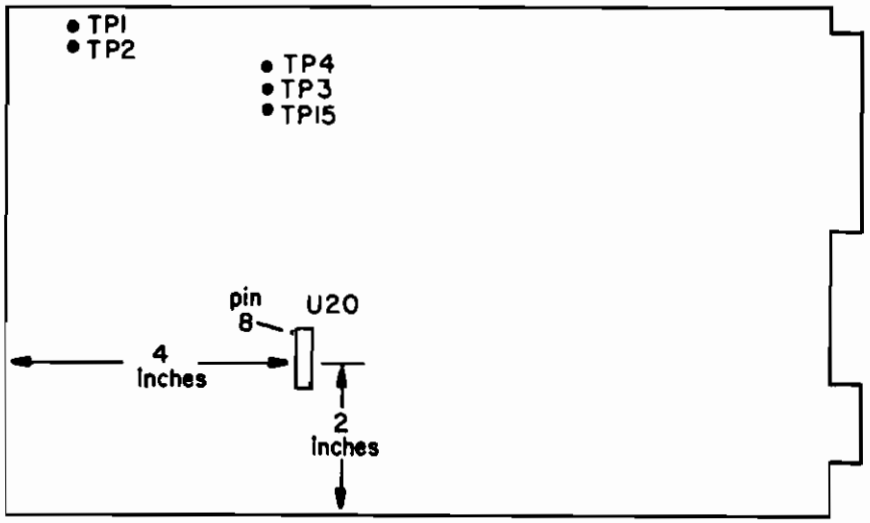


Figure 3-8. Drive Electronics Board Layout Diagram

NOTE

The scope trace after the trigger level is adjusted for repetitive trace should display an envelope of data "Cateyes" consisting of two lobes (refer to Figure 3-9).

5. Locate the traces so that the ground references are at the same position, then switch both channels to .02 volts/division ac.
6. Move the traces until both lobes are completely visible, and the ground references are at the same position.
7. Seek to Track 0. A program for manipulating the drive is on the 98041 Disc Diagnostic Tape. To use the program, follow this procedure:

    a. SCRATCHA Execute
    b. LOAD BIN "HIPxxx" Execute

       where xxx refers to mainframe model number (35A, etc)
    c. GET "DISCO" Execute
    d. RUN
    e. Answer questions on screen.
    f. Make menu choice ALIGN Continue
    g. Follow instructions on screen.

8. Seek to Track 38.
9. a. Measure ratio of smaller lobe to larger lobe for Head 0.
    b. Record lobe ratio as a percentage. If the larger lobe is on the left, use a minus sign.
    c. Measure lobe ratio for Head 1.
    d. Record this datum, using a minus sign if larger lobe is on the left.
10. Calculate head-to-head alignment error in this manner:

    a. Invert the head 0 lobe ratio (to invert subtract from 100. For example 60 inverted is 40; −10 inverted is −90)
    b. invert the head 1 lobe ratio.
    c. Average these two numbers. This figure is the head-to-head alignment error (to average, add together and divide by two).

11. Seek to Track 76.
12. Seek to Track 38.
13.

    a. Measure ratio of smaller lobe to larger lobe for Head 0.
    b. Record the lobe ratio as a percentage, using a minus sign if the larger lobe is on the left.

14. Calculate hysteresis error in this manner:

    a. Invert the head 0 seek from track 0 lobe ratio (10a = 14a)
    b. Invert the head 0 seek from track 76 lobe ratio.
    c. Average these two numbers. This figure is the hysteresis error.

15. Calculate the desired lobe ratio in this manner:

    a. Average the head-to-head alignment error and the hysteresis error.
    b. If this number is zero, the heads are aligned and the procedure may be terminated.
    c. Algebraically subtract any non-zero result from the head 0 seek from track 0 lobe ratio inverse (to algebraically subtract, change the sign of the first number and add to the second number).
    d. Invert this number. This is the desired lobe ratio for head 0 after a seek from track 0.

16. Seek to Track 0.
17. Seek to Track 38.
18. Loosen the two stepper motor adapter mounting screws and slowly rotate the stepper motor to adjust the amplitude until the desired lobe ratio is achieved (refer to Figure 3-9 and 3-10). Small increments of motion can be easily achieved by placing the blade of a screwdriver against the adapter main wall, and then tapping lightly on the side of the screwdriver handle.
19. Tighten the stepper motor adapter screws. Seek to Track 0, then seek to Track 38.
20. Verify the adjustment. If not correct, repeat steps 18 and 19 until it is correct.
21. Perform the Track 0 adjustment.

CAUTION

DO NOT TOUCH THE EDGE OF THE HEAD POSITIONING BAND WITH A METAL OBJECT. DUE TO THE HARDNESS OF THE STEEL, IT WILL NICK EASILY, AND EVENTUALLY BREAK.

DO NOT TAP AGAINST THE MOTOR. TAP AGAINST THE MOTOR ADAPTOR ONLY.

RADIAL ALIGNMENT WORKSHEET

Head-to-Head Alignment Error

9b. Head 0 seek from Track 0 lobe ratio.	SIGN	
9d. Head 1 seek from Track 0 lobe ratio.	SIGN	
10a. 100 minus absolute value of 9b.		
10b. 100 minus absolute value of 9d.		
10c. If signs are opposite, 10a + 10b, If signs are the same, 10a − 10b.	SIGN	

Hysteresis Error

9b. Head 0 seek from Track 0 lobe ratio.	SIGN	
13b. Head 0 seek from Track 76 lobe ratio.	SIGN	
10a. 100 minus absolute value of 9b.		
14a. 100 minus absolute value of 13b.		
14b. If signs are opposite, 10a + 14a, if signs are the same, 10a − 14a.	SIGN	

Desired Lobe Ratio

10c. Head-to-head alignment error.	SIGN	
14b. Hysteresis error.	SIGN	
15a. Total error, 10c + 14b.	SIGN	
15b. 15a divided by two.	SIGN	
15c. 100 plus 15b.	SIGN	

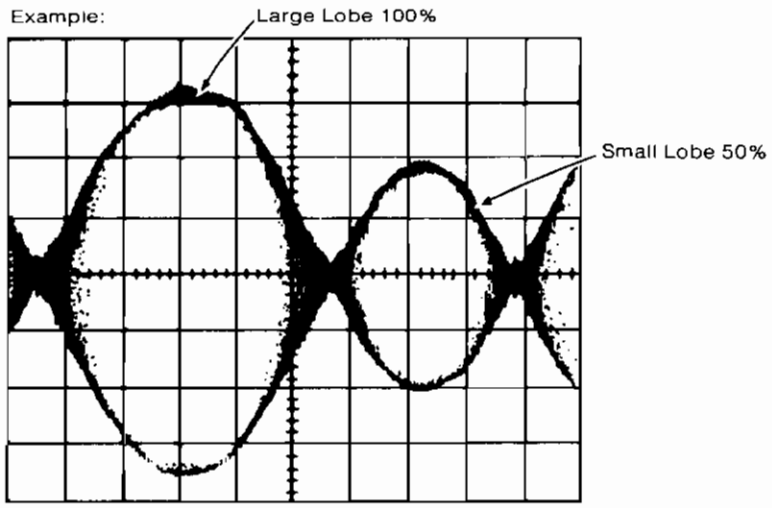


Figure 3-9. Head-Alignment Amplitude

Door-Closed Switch Adjustment

Close the door and check that it is latched. Turn the setscrew clockwise until the switch makes contact; then turn the setscrew an additional one and a half turns. Open and close the door several times while observing the door-closed signal. The door-closed signal may be observed on the terminals on the switch.

Track 0 Optical Sensor Adjustment

Adjust the Track 0 optical sensor for the output in Figure 3-11 while the drive alternately seeks at 3 μSeconds, ±0.1 μSeconds per step between Track 0 and Track 3.

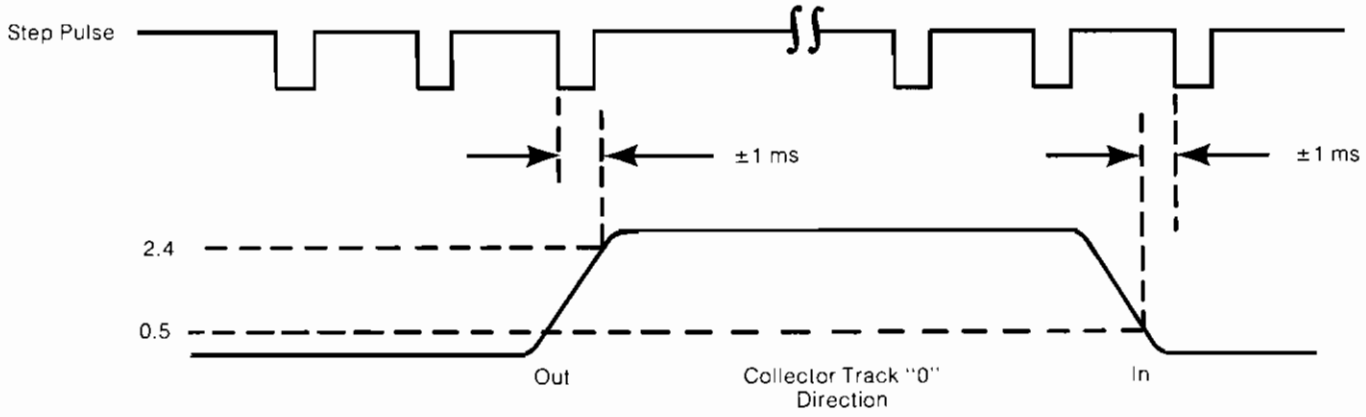


Figure 3-10. Track 0 Optical Sensor Output

Disc Ejector

Insert a disc fully and note a clicking noise as the ejector engages a pin on the door.

While observing the ejector, latch and latch block (Figure 3-12 through the ½ inch hole in the sidewall) close the door. Note that closing the door moved the ejector further to the rear, allowing the latch to rotate counterclockwise until the tip drops over the step in the latch block.

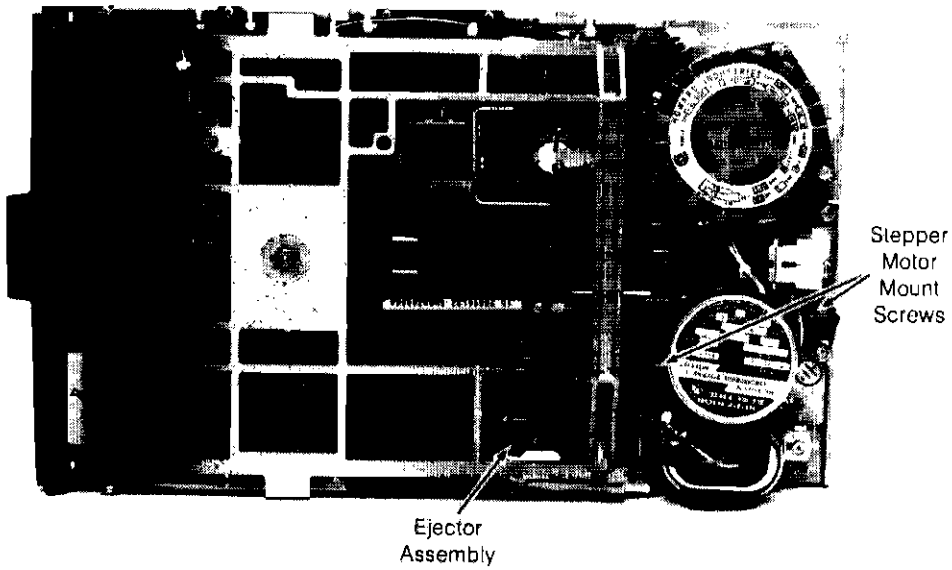


Figure 3-11. Stepper Motor Mount Screws and Ejector Assembly

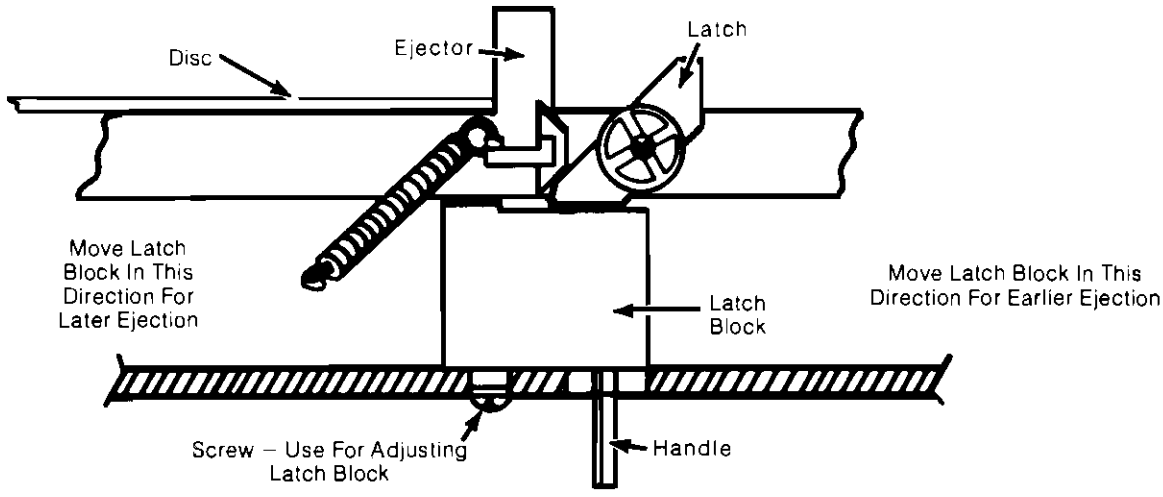


Figure 3-12. Ejector, Latch and Latch Block

With the door closed, adjust the latch block (Figure 3-12) so the tip of the latch is directly below the rear edge of the ejector.

Check by opening the door slowly and observing the door position when the disc is ejected. To avoid damage, it is to be ejected when the door is ¼ inch maximum from the fully opened position. If further adjustment is required, move the latch block as indicated by the arrows and instruction in Figure 3-12.

Cycle the door several times and observe that the disc ejection is within the ¼ inch maximum described above.

Disc-Load-Pad Adjustment

1. Install a disc.
2. Close the door and load the heads by seeking to a track.
3. Loosen solenoid mounting screws.
4. Move solenoid down on bracket to obtain a clearance of 0.010 to 0.015 inch between the load plate and the lift extension of the upper-head arm at the location of minimum clearance. Move the carriage through its full travel manually to determine the location of minimum clearance.

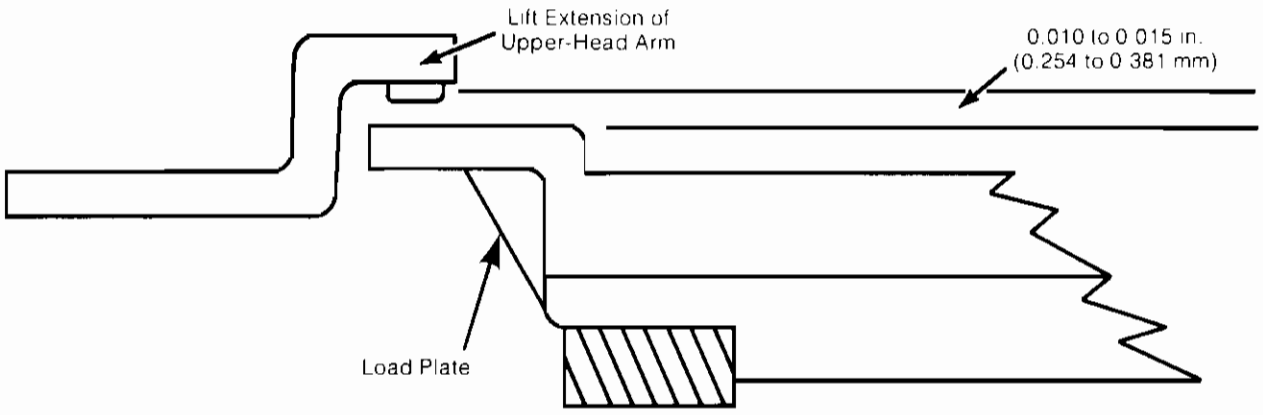


Figure 3-13. Load-Pad Adjustment

Head-Unload Clearance

Adjust setscrew on door for 0.100 inch to 0.125 inch clearance (Figure 3-14) between flyer pads with head-load solenoid de-energized and door closed.

CAUTION

MEASURE THIS DISTANCE BY EYE ONLY. DO NOT USE A GAUGE.

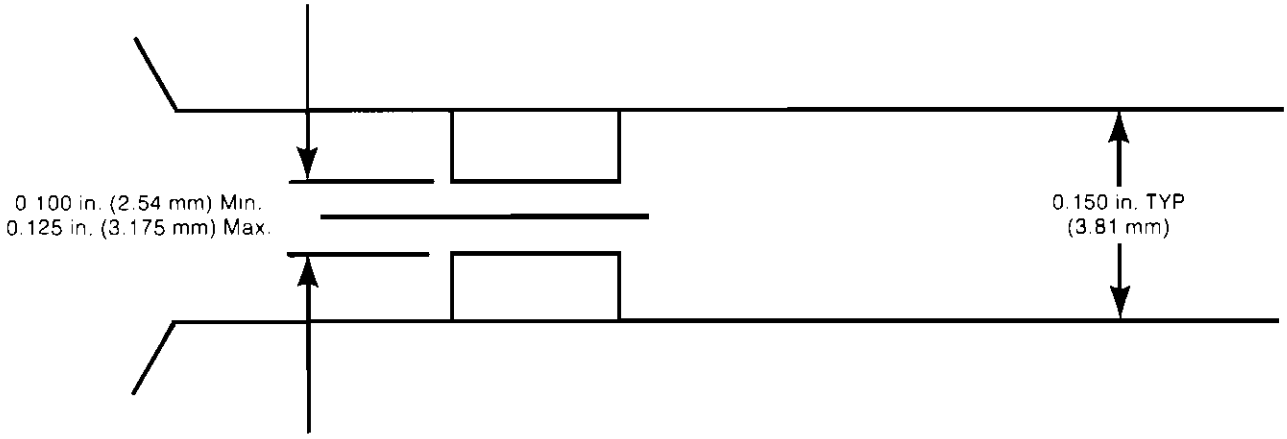


Figure 3-14. Head-Unload Clearance

Line Frequency Conversion Procedure

This procedure is to be used to convert the unit from 60 Hz operation to 50 Hz operation, or vice versa. This is accomplished by reversing the dual-diameter reversible pulley on the spindle-motor shaft using the following steps:

1. Remove ac power.
2. Remove printed circuit board assembly.
3. Remove the belt from the spindle-motor pulley (accessible from the underside of unit).
4. Loosen setscrew and remove pulley.
5. Reverse pulley and replace on motor shaft.
6. Position pulley allowing clearance of 0.039 inch, ±0.010 inch between shoulder of motor mounting screws and pulley (Figure 3-15).
7. Tighten down setscrew.
8. Replace belt and printed circuit board.

CAUTION
IT IS IMPORTANT THAT THE NEW OPERATING FREQUENCY BE MARKED ON THE UNIT'S RATING NAMEPLATE.

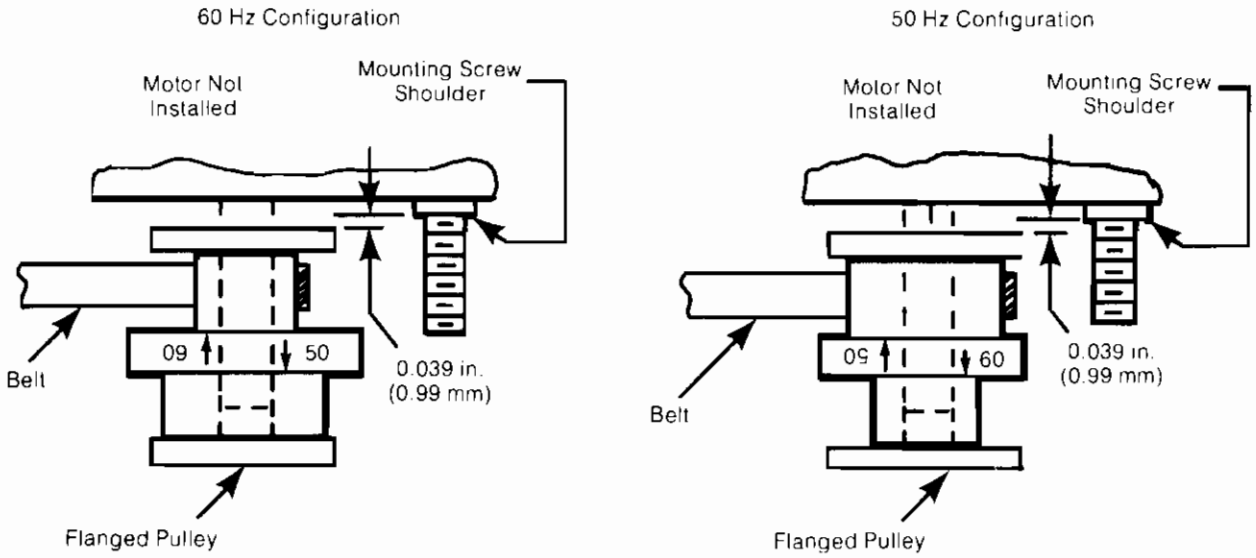


Figure 3-15. Drive-Pulley Reversal

System Exerciser

A 9895 exerciser is being added to the exerciser tapes for desktop mainframes which can utilize the 9895. To run the exerciser, refer to the mainframe exerciser operation manual. Be sure that each drive has an initialized scratch disc in it, as the exerciser includes write instructions.

Diagnostic Routines

Two diagnostic routines have been written for the 9895, DISCO and DISKEY. They are recorded on the 98041 Disc Diagnostic Tape, starting with revision D. Instructions for use are written in a file named "HELP!". To obtain "HELP!", follow this procedure:

Load the 98041 Disc Diagnostic into a tape drive.
Type GET "HELP!", press EXECUTE
and LIST for a printer
or EDIT for a CRT display.

PROM to ROM Controller Board Re-configuration

The controller board (09895-66500) was originally built using four PROM chips (1816-1237). These four PROMs are to be replaced by one ROM (1818-1391) in late 1980. PROM boards can be converted to ROM boards in the field by using this procedure:

1. Locate and remove the four PROM chips. They are located in positions U10 to U13.
2. Install the ROM in location U12.

3. Locate jumper terminal 1. It is adjacent to pin 40 of the Z80A (U14).
4. Configure the jumpers according to the following diagram:

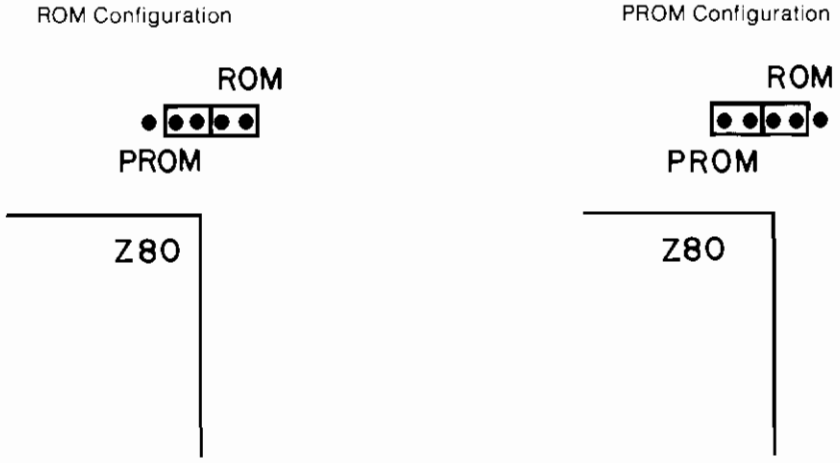


Figure 3-16. ROM/PROM Jumper Terminal Configuration

CAUTION
THERE IS AN UNUSED IC LOCATION AT U9. THIS LOCATION IS NOT TO BE USED FOR ANY COMPONENT.

Chapter 4
Status Display Board Diagnosis

Introduction

This chapter contains information pertaining to the diagnosis of problems using the 09895-66506 Status Display Board.

General Description of Diagnosis Method

The 9895 Controller contains 2 kbytes of code dedicated to a self-exercise of the drive system to verify its correct operation. The self-exercise is designed to halt at any failure. Fortunately, status of the self-test can be monitored as 15 bits of data. Ten bits indicate which test and subtest are being performed, and the other five contain miscellaneous information such as format being used (see Table 4-1 for complete list of bit functions). When a halt occurs, the ten bits may be read as an error code, and the problem narrowed down to a smaller area. The next few sections detail how to initiate the self-exercise, how to use the Status Display Board to obtain the error code and how to translate the error code into a specific problem area.

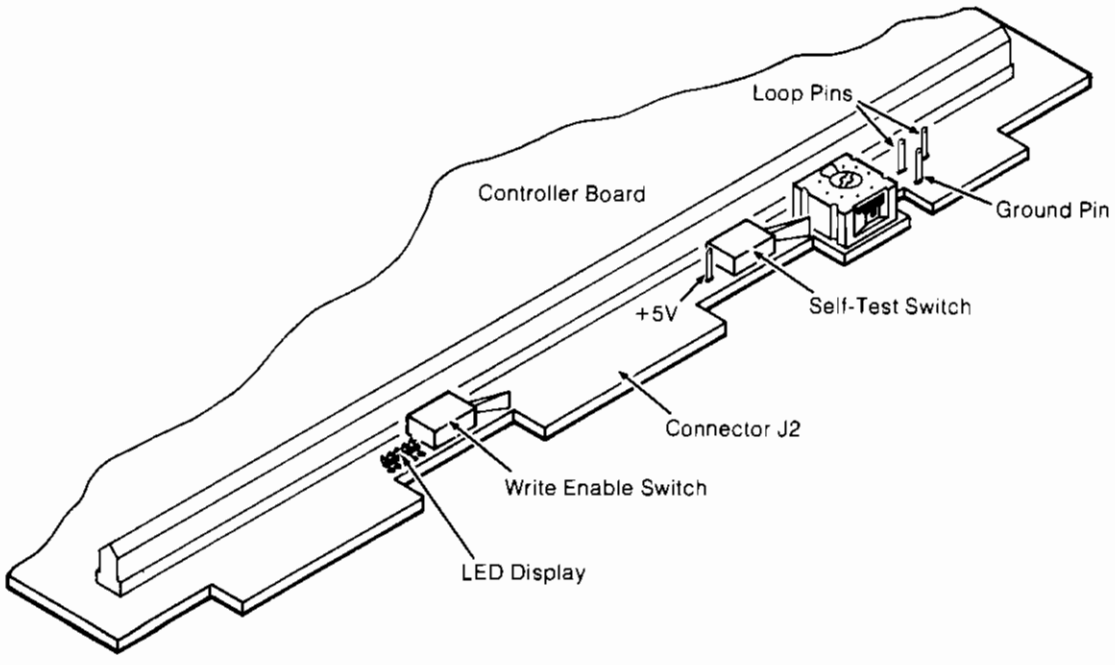


Figure 4-1. Self-Test Functions

Self-Test Initiation

The basic self-test may be initiated in any of three ways:

1. By turning the power on,
2. From the host system by means of the disc memory command set,
3. By pressing the self-test switch.

Turning the disc drive on automatically initiates the start-up sequence which includes self-test. Note that the basic self-test doesn't contain any read or write functions; therefore, a disc need not be installed in any drive.

Using the command set from the controller is by far the best way to initiate self-test, since the command set can also be used to display the results on any chosen medium.

In order to allow the disc drive to be self-tested without being connected to other devices, self-test input/output hardware was added to the front of the controller board. Figure 4-1 is a drawing of this area. The self-test switch is pressed to start the self-test routine. The read/write self-test switch is used to enable the read/write functions detailed in the next section. The loop pins are used to enable the repeat function detailed in the next section. The right-most LED indicates that the controller is busy doing self-test. The four left-most LED's display the number of the test being run. If the routine halts on any test, the LED display may be read as an error code (see Table 4-2).

Test Selection

There are three classes of tests selectable in the manually-invoked self-test. They are:

1. Default self-test,
2. Read-only self-test,
3. Write/read self-test.

Default Self-Test

The default self-test is selected by momentarily depressing the self-test switch.

Loop Pins	Self-Test Switch	Function
Open	Released	Perform standard self-test only and then go on-line. If soft error occurs, pause 20 seconds before going on-line.
Closed	Released	Perform standard self-test repetitively. If soft error occurs, pause 20 seconds before repeating.

Read-Only Self-Test

The read-only self-test is selected by pressing and holding the self-test switch.

Loop Pins	Self-Test Switch	Function
Open	Held	Perform read-only test on incrementing tracks with .5 second delay between increments. If error occurs, wait for release of self-test switch before going on-line.
Closed	Held	Perform read-only test on incrementing tracks with no wait between increments. If error occurs, pause .2 second before repeating failed test.

Write/Read Self-Test

Write/read self-test is selected by holding the write enable switch in while pressing the self-test switch. If the write enable switch is held in during execution of the test, the read after write is performed with reduced margins.

Loop Pins	Self-Test Switch	Function
Open	Released	Perform write/read test on track 0 and then go on-line. If error occurs, pause 20 seconds before going on-line.
Open	Held	Perform write/read test on incrementing tracks with .5 second delay between increments. If error occurs, wait for release of self-test switch before going on-line.
Closed	Released	Perform write/read test on incrementing tracks with no wait between increments. If error occurs, pause 20 seconds before continuing test.
Closed	Held	Perform write/read test on incrementing tracks with no wait between increments. If error occurs, pause .2 second before repeating failed test.

Using the Status Display Board for Failure Analysis

Although the four digits displayed on the LEDs can narrow the problem down to a small area, there is much more information available. It can be read by the controller using the disc memory command set. It is also available at connector J2 (see Figure 4-1). The module is designed to fit on this connector and present this information as an LED display. To use the module, follow this procedure:

1. With the power turned off, remove all interconnecting cables from the 9895A.
2. Pull the front cover off.
3. Locate connector J2 (Figure 4-1). Slide the module onto this connector, component side up.
4. Hook the +5V clip onto the +5V pin. If the +5V pin is missing, +5V is available at the top of the LED display.
5. Turn power on. The start-up sequence includes the basic self-test.
6. After the self-test has finished running (that is, the LED pattern has stopped changing), press and release the self-test switch.
7. The basic self-test should now occur. When it has finished running, put an initialized scratch disc in each drive and close the doors.
8. Pressing and releasing the read/write enable switch and hold it in until after pressing the self-test switch. The basic self-test with read/write should now occur.
9. To make self-test repeat, short the loop pins together.

Self-test information can be read directly from the LED's, using the methods presented in the next section.

Obtaining Test Results From LED Display

The two pieces of information which we are interested in are the four-bit test number and the five-bit subtest number. The test number appears as four red LED's labeled TEST. The MSB is toward the 9895A. The subtest number appears as five green LED's labeled SUB-TEST. These two numbers are listed in Table 4-2, along with the meaning of the code. Note that only nine of ten error code bits are used. The tenth digit is always zero, as can be seen by using the controller and command set, which present all ten bits.

Table 4-1. LED Display

ERR	Turns on when error is detected.
HEAD	Off for head 0, on for head 1.
UNIT	Unit number of drive being tested (in binary).
HPFMT	Off for IBM format, on for HP format.
TEST	Indicates number of test being performed.
SUBTEST	Indicates number of subtest being performed.
DONE	Indicates board is functioning. Test has completed if only this LED is on.
UNIT 0 ERR	Counts number of errors found in drive unit 0.
UNIT 1 ERR	Counts number of errors found in drive unit 1.

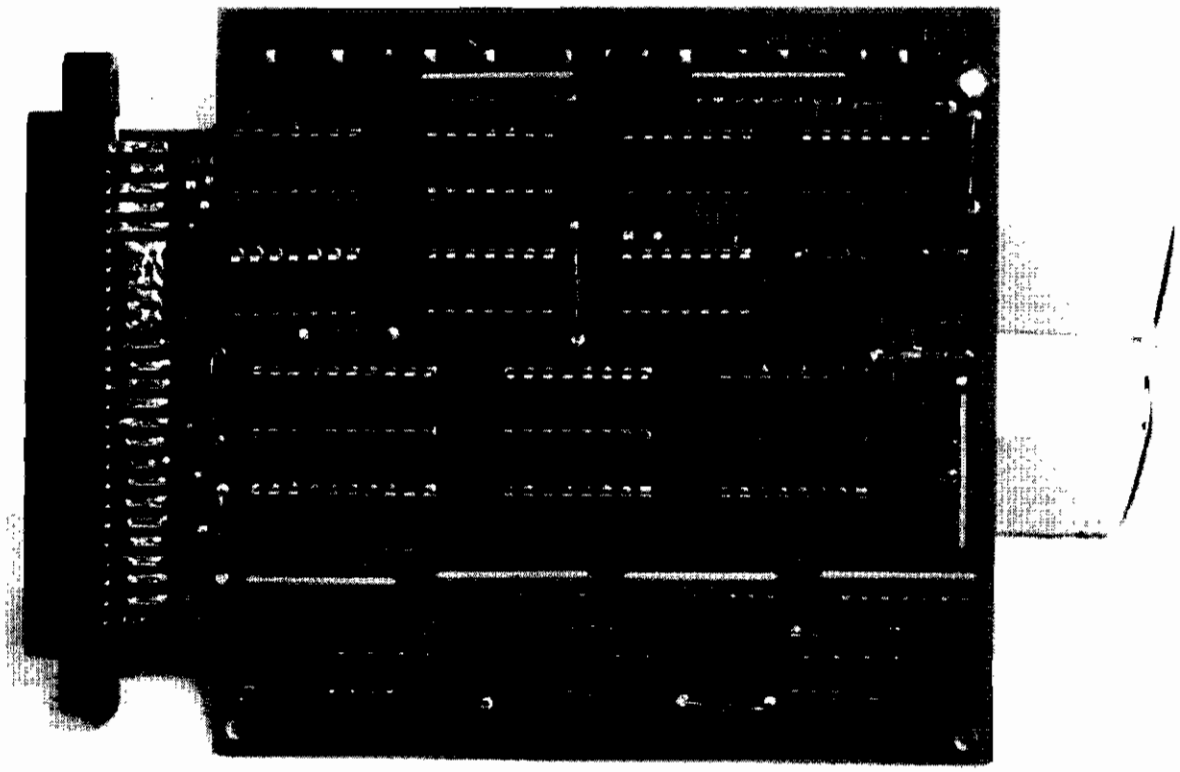


Figure 4-2. 09895-66506 Status Display Board

Error Rate Testing With the Status Display Board

The Status Display Board can be used for error rate testing of up to two drives at a time. It counts the number of passes of the selected self-test, and counts errors separately for each drive. This is the procedure:

1. Attach a jumper between the loop pins.
2. Put a disc with no defective tracks in each drive, and close the door.
3. Turn the power on.
4. Press the write enable switch and hold it in while pressing the self-test switch. Hold the self-test switch in with an insulated clip. The write/read test will now run continuously.
5. The HP bit error rate standard is no more than one error in 10^9 bits. 7862 passes are the equivalent of 10^9 bits. A drive would pass if it has no more than five errors in 39,308 passes. A problem arises in that the pass counter only counts to 9999 and then re-sets. This problem may be circumvented in one of two ways. Put the system into operation and allow it to run for an hour or two. If errors have accumulated, the drive is defective. To prove that a drive is good, determine the length of time the system takes to make a countable number of passes, say 3,000 or 10,000 and then calculate how long 39,308 would take. Allow the system to run for that length of time, and stop when the counter reads 9308. If no more than five errors have accumulated on a drive, it is a good drive.
6. Note that the self-test routine cannot determine whether a track is good or bad, but attempts to write on every track. If errors appear to occur at the same point on the disc, there is probably a defective track at that point.

Table 4-2. Error Codes

Test Number	Subtest Number	Error Explanation	Possible Failure
0001	00000	ROM Checksum Test: This test sums the contents of the ROM and compares it to the checksum value stored in the ROM.	ROM Data or Address Bus
0101	00000	Indicates a failure in the upper four bits (U36).	
0110	00000	Indicates a failure in the lower four bits (U35).	
0111	00000	PHI Test: This test exercises the internal operations of the PHI chip (U34).	PHI Chip
1000		Time-Out Bit Test: These subtests measure the pulse of the time-out one-shot (U68) and test for re-triggerability.	Time-Out One-Shot One-Shot Reset Circuit
	00000	Time-out is high when it should be low.	I/O port read circuit
	00001	Time-out is low when it should be high.	
		Overrun Bit Test: These subtests verify functioning of the overrun circuit - ability to reset the overrun bit and ability of circuit to detect an overrun condition.	Overrun circuit Reset to overrun Write enable circuit Write clock I/O port read circuit
	00010	Overrun is high when it should be low.	
	00011	Overrun is low when it should be high.	
1001		IBM Data Loop Test: These subtests exercise the data loop in IBM format mode. A pattern is written to the clock and data registers; it loops through the serializer, write encoder, data separator and deserializer, and is read back from the clock and data registers.	Clock or data register I/O port real circuit Serializer/deserializer Write encoder circuit Data separator circuit IBM format select
	00000	Error in data byte read.	
	00001	Error in clock byte read.	
	00010 00011	HP Data Loop Test: Exactly the same as the IBM Data Loop Test except that it runs in HP format mode.	Same as IBM Data Loop except HP format select vice IBM format select.
		Address Mark Test: These subtests check the address mark detect circuit.	
	00100	Address mark detect is on when it should be off.	Address mark detect circuit
	00101	Address mark detect is off when it should be on.	
		Margin Error Test: These subtests check the margin error detect circuit.	Margin error detect circuit.
1010		CRC Test: This test exercises the cyclic redundancy check generator. It tests ability to detect a CRC error and to generate the correct CRC for a specific data pattern.	CRC chip CRC enable I/O port read enable

Table 4-2. Error Codes (cont.)

Test Number	Subtest Number	Error Explanation	Possible Failure
	00000	CRC ERR is off when it should be on.	
	000001	Wrong CRC bytes were generated.	
	00010	CRC ERR is on when it should be off.	
1011		Re-calibrate/Seek Test: This test attempts to select each drive, re-calibrate the drive, step in to track 76 and step out to track 0.	Drive select signals Control signals Track 0 signal I/O port read circuit I/O port write circuit
	00100	Track 0 indicator came on while stepping in to track 76.	
	00101	Track 0 indicator came on when not expected while stepping out to track 0.	
	00110	Track 0 indicator did not come on when it should have.	
	00111	No drives were found attached to the controller, or a drive failed to re-calibrate.	
1100		Rotational Timing Test: This test measures the time for revolution of the disc and compares it to the specification.	Index signal Ac line frequency Spindle motor
	00000	No index mark was found.	
	00001	Disc is spinning too fast.	
	00010	Disc is spinning too slow.	
1101		Write Test: This test formats a track in both HP and IBM formats and reads back what was written.	Most failures are caused by problems with the phase locked loop circuit or the WDATA or RDATA interface between the controller and the drive.
	00000	Drive went not ready during format.	
	00001	No disc in the drive.	
	00010	Disc is write-protected.	
1110		Read Test: This test reads a track on the disc. It may be a part of the write/read test or it may be a read-only test, depending on switch settings.	Same as write test.
		Subtests common to both write/read and read-only tests.	
	00000	Drive went not ready.	
	00001	Head, track or format information written in the ID field is incorrect.	
	00010	No ID fields were found.	
	00011	Current sector was not found.	
	00100	Data mark for the desired sector was not found.	
	00101	CRC error occurred.	
	00110	Overrun error occurred.	
		Subtests in write/read test only.	
	00111	Data read back not the same as what was written.	

Table 4-2. Error Codes (cont.)

Test Number	Subtest Number	Error Explanation	Possible Failure
	01000	Margin error occurred.	
		Subtests in read-only test only.	
	10000	Drive went not ready while seeking to the desired track.	
	10001	Unknown format.	
	10010	Seek to desired track failed.	
	10011	No disc in the drive.	
1111		Processor Test: This test exercises the operations of the processor.	
	00001	Problem with the internal functions of the processor - branching, register arithmetic and logic functions.	Processor ROM Data or Address Bus
	00010	Problem with functions which access the RAM- read and write of RAM, stack operations and indexed and indirect addressing of RAM.	Processor ROM RAM Data or Address Bus

Chapter 5
Replaceable Parts

Introduction

This chapter contains a listing of all parts and assemblies which normally might require replacement or exchange. Table 5-1 contains a list of Exchange assemblies, more frequently needed electronic parts, drive module mechanical parts and some miscellaneous parts such as covers, cables, etc.

Table 5-1. Replaceable Parts

Reference Designator	CD	hp Part No.	TQ	Description
				Exchange Assemblies
A1	4	09895-69500		Controller Board, Rebuilt 09895-66500
A2	4	09895-69914		Drive Module, Rebuilt 09895-67914
				Electronic Parts
A1U1	8	1820-1287	1	IC: 7437
A1U16	0	1810-0315	1	Delay Line
A1U18	8	1820-1112	1	IC: 7474
A1U14	3	1820-2298	1	IC: Z80A
A1U34	1	1820-2147	1	IC: PHI
A4F1	0	2110-0003	1	3 Amp Fuse (For 100 & 120 Volt Operation)
A4F1	8	2110-0043	1	1.5 Amp Fuse
A4Q1	9	1854-0669	1	XSTR, 2N6057
A4S1	2	3101-0417	1	Switch, Rocker
A4T1	8	9100-2639	1	Transformer, Power
A3	6	09895-67910	1	Power Module
C1	0	0180-2682	2	C-F: 1000µf; 50V
C2	6	0180-2208	1	C-F: 220µf; 10V
C3	0	0180-2682		C-F: 1000µf; 50V
C4	6	0160-4298	1	C-F: 4700Pf; 250V
C5	5	0180-1746	1	C-F: 15µf; 20V
C7	2	0180-1735	1	C-F: 0.22µf; 35V
C8	0	0160-4557	4	C-F: 0 1µf; 50V
C10,C11	5	0180-0540	2	C-F: 400; 30V
C12	8	0180-0197	1	C-F: 2.2µf; 20V
C13	0	0160-3335	2	C-F: 470Pf; 100V
C14	8	0180-2606	1	C-F: 180µf; 40V
C15	0	0160-3335		C-F: 470Pf; 100V
C16-C18	0	0160-4557		C-F: 0.1µf 50V
CR1	5	1906-0052	2	Diode: Breakdown
CR2,CR3	3	1901-0708	2	Diode: Power Rectifier
CR4	8	1884-0293	2	Diode: SCR
CR5	2	1902-0049	1	Diode: Zener; 6.19V
CR6	1	1901-0040	2	Diode: Switching
CR7	1	1902-3092	1	Diode. Zener; 4.99V
CR8	8	1884-0293		Diode: SCR
CR9	6	1902-3203	1	Diode: Zener; 10.5V
CR10	5	1906-0052		Diode: Breakdown
CR11	1	1901-0040		Diode: Switching
F1-F3	0	2110-0342	3	Fuse: 8A; 250V
J2	6	1251-4781	1	Connector: 3 Pin; Male
J3	9	1251-3819	1	Connector: 6 Pin; Male
R1	6	0757-0316	2	R-F: 42.2Ω; 1%, .125W
R2	2	0698-3445	1	R-F: 348Ω; 1%; .125W
R3	0	0757-0401	1	R-F: 100Ω; 1%; .124W
R4	1	0811-1826	1	R-F: 0.05Ω; 10%; 3W
R5	3	0761-0041	1	R-F: 56Ω; 5%; 1W
R6	6	0757-0316		R-F: 42.2Ω; 1%; .125W
R7	3	0757-0470	1	R-F: 162K; 1%; .125W
R8	5	0698-3266	1	R-F: 237; 1%; .125W
R9	2	0698-8825	1	R-F: 681K; 1%; .125W
R10	9	0757-0442	1	R-F: 10K; 1%; .125W
R11	1	1810-0316	1	Resistor Pack: 10K; 2%; .218W
U1	0	1826-0049	1	IC: Regulator; 723
U2	1	1826-0412	1	IC: Comparator; LM393
U3	5	1826-0408	1	IC: Power Sensor; 8212
U4	9	1826-0147	1	IC: 7812

Reference Designator	CD	hp Part No.	TQ	Description
				Drive Mechanical Parts
	8	0950-0475	1	Belt, Motor
	9	0950-0476	1	Switch, Door-Closed
	2	1535-4090	1	Detector, Write Protect
	0	0950-0477	1	LED, Door Button
	4	0950-0489	1	Detector, Track 0
	1	0950-0478	1	Clip, Push-In
	6	0950-0473	1	Load Plate
	6	0950-0499	1	Detector, Index
	2	0950-0479	1	Latch, Door
	5	0950-0472	1	Spring, Door
	5	0950-0480	1	Pin, Hinge (Short)
	6	0950-0481	1	Pin, Hinge (Long)
	7	0950-0482	2	Pin (Door Front)
	7	0950-0474	1	Ejector Assembly
	0	0950-0500	2	Pin, Hitch
	8	0950-0483	1	Button, Door
				Miscellaneous Parts
	6	09895-04102	1	Bottom Cover
	9	09895-60602	1	Top Cover
	0	09895-40001	1	Front Panel
	2	09895-00601	1	Fan Compartment
	9	3160-0311	1	Fan
	3	8120-2930	1	Cable Assembly, Drive AC
	9	09895-66501	1	Cable Assembly, Drive DC
	7	8120-2926	1	Cable Assembly, Transformer to Power Module
	7	09895-61608	1	HP-IB Internal Bus
	4	09895-90000	1	User's Manual
	6	09895-90010	1	Disc Care Guide
	5	8120-2718	1	HP-IB Interface Cable
	5	09895-61606	1	Master-to-Slave Cable
	2	7120-6966	1	Labels; Drive and Address

Appendix A

HP 9895A Disc Memory Command Set

Introduction

The following description of the HP 9895A Flexible Disc Memory command set is HP-IB rather than CPU oriented. It is given in terms of operations (mainly bytes sent) over the HP-IB. Since this level is common to any interface to the 9895A, it is machine independent.

A basic knowledge of the HP-IB operation including primary commands, secondary commands, and parallel poll operation is assumed. An HP publication "Condensed Description of the Hewlett-Packard Interface Bus", Part No. 59401-90030, is available for background information. HP-IB is an implementation of IEEE Standard #488-1978.

Bus Controller	As used in the manual, is the current HP-IB controller in charge of the HP-IB.
Controller	The 9895A disc controller hardware or firmware.
Unit	One of up to four drives connected to the controller.
Flexible Disc, Disc or Diskette	The coated mylar media used to record data on by the 9895A.
HP Format	The double-density, single- or double-sided, HP standard recording format.
IBM Format	The single-sided IBM standard recording format.
Physical Track Number	The track number relative to the outer-most track on the disc.
Logical Track Number	The track number recorded on the disc at a physical track. Logical track numbers may or may not be the same as the physical track number.
Head	One of the two sets of read, write and erase elements used to record data in the unit.
Track	The area defined by a cylinder and head address.
Cylinder	The recording area accessible by the two heads without moving the head actuator.
Sector	The smallest block of data that can be read or written from the disc.
Host System	The system which contains the bus controller.

Command Compatibility

The 9895A belongs to a set of command compatible HP-IB interface discs. All of these discs meet the "HP-300 Compatible HP-IB" standards. In addition, the same sequence of HP-IB operations can be used to transfer data to and from any of these discs.

There are some subtle differences between HP-300 Compatible HP-IB and IEEE Standard #488-1978.

1. An identify code sequence by the host to determine what class of devices and which device is connected, is not supported by IEEE #488-1978.
2. Disc read and write operations cannot be suspended and then resumed; i.e., an Untalk or Unlisten command terminates command operation. This is not consistent with IEEE #488-1978.

Since the capacity and organization of a flexible disc is different from other HP-IB compatible discs, the allowable range of certain parameters is also different from the other discs.

Certain commands used in formatting a disc or for diagnostic purposes are unique to the 9895A. Similarly, certain commands supported by other discs are not supported by the 9895A. An unrecognized command causes an error to be set, but has no detrimental effect on controller operation.

Command Sequences

Much of the 9895A command set shown in this section is made up from two basic types of HP-IB sequences.

To send information (commands or data) to the 9895A, the bus controller addresses it to listen, and then sends a secondary command byte followed by a series of information bytes. The last information byte sent must be tagged with an EOI. Finally, the bus controller sends an Unlisten command, and the sequence is complete.

To receive information (status or data) from the 9895A, the bus controller addresses it to talk, and then sends a secondary command byte. At this point the device sends back a series of information bytes. In some cases the last information byte will be tagged with an EOI. In cases where the last information byte is not tagged with an EOI, an additional byte tagged with an EOI is made available. The extra byte may be used to detect that a byte was dropped on the HP-IB, or it can be used to determine the end of a transfer without maintaining a byte count. Finally, the bus controller issues an Untalk and the sequence is complete.

Sequences other than the ones shown may, in some cases, work; but there is no guarantee that they will be compatible with other HP-IB discs or with future HP disc memories.

The controller only operates on a single command at any given time; i.e., overlapped operations on multiple drives are not possible.

Parallel Poll Response

Parallel poll is used as an additional means of communication between the 9895A and the bus controller. If the 9895A is ready to accept the next part of a command sequence, it will respond to the parallel poll conducted by the bus controller.

After accepting most secondary command bytes, the 9895A disables the parallel poll response. This indicates that the device is busy processing the current part of the command sequence. The actual disabling of parallel poll response may occur up to 100 microseconds after the secondary is accepted by the 9895A. Thus, if the 9895A has parallel poll enabled, and the bus controller is fast enough to send a command sequence and then conduct a parallel poll before the 9895A has disabled the poll, the bus controller would see the wrong parallel poll response. To solve this problem, an intentional delay can be introduced, or a DSJ command (this disables parallel poll) can be issued before other commands.

The exception to the parallel poll response interlock concerns the Clear commands. The DSJ command, unlike the Clear commands, may not be a valid or recognized command in all states of the controller. Thus, the controller may reject or not even see the DSJ command and not disable the parallel poll response. If the bus controller had expected the DSJ to lower the parallel poll in the case where the controller can not accept the DSJ, the bus controller would see the wrong parallel poll after the Clear command.

Cylinder and Track Numbering

Starting from the outer cylinder, cylinders are numbered sequentially from 0 to 76. These numbers are also the physical track addresses. A track is the intersection of a cylinder and a head. There is also a logical track address associated with each good track. If a disc has no bad tracks, the logical address of a track is the same as the physical address.

A disc with bad tracks can be made to look like a slightly smaller disc with no bad tracks. To do this, the bad tracks are specially marked to indicate that they have no logical address. A track marked in this way is referred to as an invisible track. The remaining good tracks are sequentially assigned logical track numbers. Logical track 0 is the outer-most good track (it may or may not be physical track 0).

During normal operations, the user need be concerned only with logical addresses. The 9895A controller will take care of finding the proper physical address.

Target Addressing

Each unit has a target address associated with it. This is the logical address of the next sector which will be accessed by a Data Transfer command or return for an address request. This sector is referred to as the target sector. It is uniquely determined by a target cylinder address, a target head address and a target sector address.

Following a power up or a Clear command, the target address will be set to cylinder 0, head 0 and sector 0 for HP format and 1 for IBM format.

A Seek command sets the target address to the cylinder, head and sector indicated in the command sequence.

During a data transfer, the target address is automatically updated so the successive logical sectors can be read without issuing a seek to each sector. This includes updates which cross track or cylinder bounds. The 9895A is always in cylinder mode; that is, the head address will be incremented before the cylinder address.

If a data transfer terminates abnormally, the target address is left pointing at the sector which caused the termination.

The D Bit

Each sector has a flag called the D bit. It is used to indicate that a track is defective (which is different than invisible). The D bit can be set or cleared using the Initialize command. A set D bit affects the Read, Write and Format commands and is indicated in the returned status.

The Format command is used to convert all tracks flagged with the D bit into invisible tracks.

HP and IBM Formats

The 9895A can work with discs which use either the HP single- or double-sided formats or the single-sided IBM format. After a disc is inserted in a unit, the first status request for that unit will cause the controller to determine which format is present. This information is available as part of the returned status.

Many details of operation vary slightly for the two formats. These include the allowable range of target address, the updating of target addresses and the effect of the D bit. These differences will be noted in the appropriate command descriptions.

Loading of the Recording Heads

Control of the position of the heads is done by the controller. Any command received correctly that needs to read or write the disc will load the heads for its operation. In addition, the controller will keep the heads loaded for approximately 2 seconds after the command completes the operation in anticipation of a subsequent command. In multiple drive configurations, the time the heads remain loaded on inactive drives can increase from 2 seconds to approximately 10 seconds, as a function of the operation in progress on some active drive, the interleave of the disc in the active drive and the frequency of the command from the host system. If the host system should malfunction, and leave the controller in a state expecting to receive or send data, the controller will abort the operation in approximately 60 seconds and proceed to its idle loop where the heads could be unloaded. The host system has the ability to lock the access door on any/all of the drives to prevent unwarranted access to the discs; in this case, the doors will not be unlocked if the above error condition should occur.

Holdoffs

The 9895A will not execute most operations when it enters either of the two states described below. It is very important to know these states and the commands that will remove the holdoffs.

1. DSJ = 2 or Power On State

   This state is entered after:

   a. The 9895A is powered up.
   b. After the execution of the Initiate Self-Test command.

   As long as DSJ = 2, a value unique to this state, the commands listed below will not be executed. There are, however, three commands which may be executed either to change the DSJ or override its holdoff. These commands are:

   a. The DSJ command,
   b. The Clear commands,
   c. The Cold Load Read command.

   For both DSJ and Clear, the DSJ value becomes 0, the cold load read will override the holdoff and set the DSJ according to the outcome of the read.

   The only way for the bus controller to realize that the device was in the Power On state is by sending the DSJ command (which clears the state).

   The purpose of this holdoff state is to withhold all operations that may occur during normal usage until the bus controller can become aware that the power has been interrupted.

   The following is a list of the commands not executed while in the DSJ = 2 state:

   a. All Read commands
   b. All Write commands
   c. Verify
   d. Initialize
   e. Format
   f. Seek
   g. End
   h. Request status
   i. Request disc address commands

   The 9895A will, however, respond to a Talk command from the above group by sending one byte (of value 1) tagged with an EOI. Also, all data bytes sent to the 9895A as part of the commands listed above will be accepted but ignored. These actions will cause the 9895A not to hang (timeout) the HP-IB until the bus controller is aware of the holdoff.

2. First Status State

   This state is entered for a particular drive after:

   a. A disc is inserted in the drive during normal operation,
   b. The 9895A is powered up with a disc in the drive,
   c. The 9895A is issued an Initiate Self-Test command, with a disc in the drive.

   When this state is entered, a flag in the status 2 word for the drive(s) affected is set. All operations requiring access to the newly inserted disc are disabled until the status of the drive is requested or the Cold Load Read command is issued.

   The holdoff ensures that the HP-IB controller is aware that the disc is a newly inserted one before it is actually accessed. In addition, the first request of status for that drive will cause the device to find out the format of the newly-inserted disc, thereby enabling proper use of the disc.

   Commands not executed while first status is set are:

   a. Read commands
   b. Write commands
   c. Verify
   d. Initialize
   e. Format
   f. Seek

   It should be noted that after a power-on has occurred or after the execution of the Initiate Self-Test command, the DSJ is set to 2 and the first status bit is set for any drive containing a disc. Thus, both holdoffs, DSJ and first status, will be in effect.

   Therefore, to enable access to a disc, two command sequences may be used. They are:

   a. A DSJ or Clear followed by a Status command,
   b. A Cold Load Read command.

Command Execution Checks

In addition to the above holdoffs, the controller will verify other conditions before a particular operation is permitted to execute.

1. Correct number of command bytes.

   Obviously, the correct command syntax must be received, or else an I/O program error is defined by the controller.

2. DSJ = 1 and status 1 <> I/O program error
   DSJ = 1 and status 1 <> illegal opcode

   The above condition exists when the most recent command terminated with an error. The following commands are disabled when this condition exists until the host system requests status and hence is aware of the status of that last operation:

   a. Read commands,
   b. Write commands,
   c. Door lock/unlock.

3. Disc format.

   Most commands that operate on the disc will verify that the format is either HP or IBM. If an unknown disc is in the requested drive, these operations will abort with a status 2 error. The commands are:

   a. Seek,
   b. Read commands,
   c. Write commands,
   d. Initialize command.

4. Obviously, the disc must not be write protected when any command that needs to write information on the disc is given. The commands that make this check are:

   a. Write commands,
   b. Initialize command,
   c. Format command.

Commands

The details of the 9895A HP-IB command set are given in this section. The following conventions are used:

| |	Byte sent between the bus controller and the 9895A.
P P D	Parallel poll disabled.
P P E	Parallel poll enabled.
ADDR	The 9895A's current HP-IB device address.
P	HP-IB parity bit.
ATN	HP-IB bus control signal; this signal indicates that a command is present on the bus.
EOI	End or identify; this signal specifies that the present data byte is the last of the sequence or, if ATN is concurrently asserted, then a parallel poll is being conducted by the bus controller.
UUUU or UNIT	Unit number (0 <= UUUU <= 3).
Stat 1	Status one word: Most significant byte is S1; Least significant byte is unit number.
Stat 2	Status two word.

The bit numbering notation for words is as follows:

15 14 13 12	**11 10 9 8**	**7 6 5 4**	**3 2 1 0**
X X X X	X X X X	X X X X	X X X X

All command sequences are verified for validity when received. This involves testing the secondary command, the command number and the number of data bytes in the command sequence for correctness. An I/O program error is defined whenever there is a problem with a command sequence.

Table A-1. Command Table

	Primary	Secondary	Key[1]	Opcode	Key[2]	# Bytes
Identify	U	ADDRS		—		—
DSJ	T	!10	P	—		1
Read Self-Test	T	!1F	—	—		2
Read Loopback	T	!1E	^	—		1 to 256
Request Status	L	!08	H	!03	C	2
Request Status	L	!0A	J	!03	C	2
Req (Logical) Address	L	!0A	J	!14	T	2
Req (Logical) Address	L	!08	H	!14	T	2
Req (Physical) Address	L	!0C	L	!14	T	2
Send Status or Address	T	!08	H	—		4
Universal Clear	U	—		—		—
Selected Device Clear	L	—		—		—
HP-300 Clear	L	!10	P	—		1
Initiate Self-Test	L	!1F	—	—		2
Write Loopback	L	!1E	^	—		1 to 256
Download Controller	L	!0F	O	—		1 to 256
Door Lock	L	!0C	L	!19	Y	2
Door Unlock	L	!0C	L	!1A	Z	2
HP-IB CRC	T/L	!11	Q	—		—
Seek	L	!08	H	!02	B	6
End	L	!08	H	!15	U	2
Buffered Read	L	!0A	J	!05	E	2
Unbuffered Read	L	!08	H	!05	E	2
Verify	L	!08	H	!07	G	4
Buffered Read Verify	L	!0B	K	!05	E	2
Unbuffered Read Verify	L	!0C	L	!05	E	2
Cold Load Read	L	!08	H	!00	@	2
ID Triggered Read	L	!0B	K	!06	F	2
Send Data	T	!00	@	—		—
Buffered Write	L	!09	I	!08	H	2
Unbuffered Write	L	!08	H	!08	H	2
Initialize	L	!08	H	!0B	K	2
Format	L	!0C	L	!18	X	4
Receive Data	L	!00	@	—		—

[1] To generate the command Secondary, hold the Control key down while pressing the listed key.

[2] To generate the command Opcode, hold the Control key down while pressing the listed key.

Command Table

! – Hexadecimal Number
T – Talk Primary
L – Listen Primary
U – Universal Primary

Sense Commands

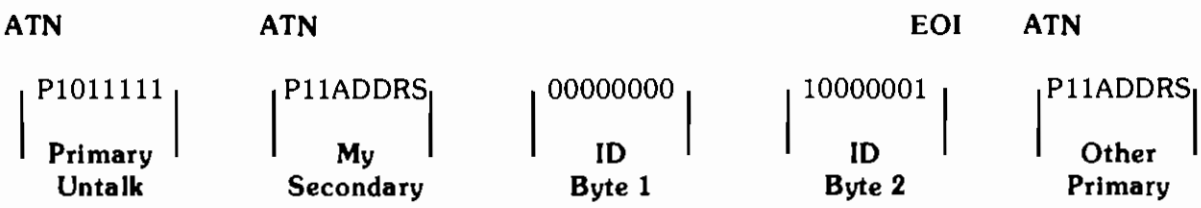
Identify

Type: Sense.

Purpose: The 9895A will return a code unique to the disc subsystem to allow for auto-configuration of systems.

Description: Upon the reception of the untalk primary followed by the secondary corresponding to the 9895A's current HP-IB address, the 9895A's PHI will respond by sending the ID bytes of 0 and 81 hex, the second byte being tagged with an EOI. These two bytes will continue to be sent until another command is transmitted on the bus.

HP-IB Sequence:



DSJ

Type: Sense.

Purpose: The 9895A returns a byte indicating if the last operation completed normally or abnormally, or if the power to the 9895A has just been restored, or if a parity error has been detected on the HP-IB. The DSJ command also provides a way to disable the 9895A's parallel poll response.

Description: After accepting the DSJ secondary, the 9895A disables its parallel poll response (usually within 100 microseconds) and returns a byte (the DSJ byte) reflecting the status of the controller.

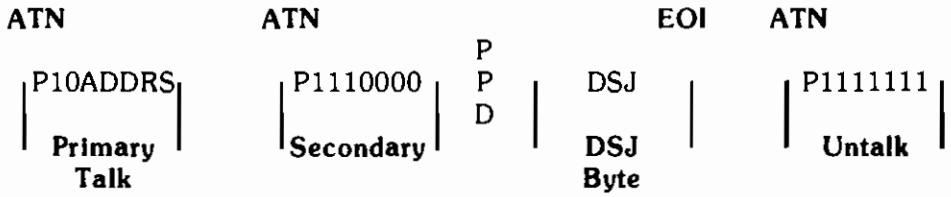
DSJ = 0 – The 9895A completed its last operation normally.

DSJ = 1 – The 9895A aborted its last operation abnormally. Status will indicate the current error.

DSJ = 2 – The 9895A has just completed a power up sequence and is in the DSJ = 2 holdoff state.

DSJ = 3 – A parity error has occurred on the HP-IB. Repeat the request to receive the pre-parity error DSJ.

HP-IB Sequence:



Status (Upon Command Completion): No errors.

S1 – Unchanged
Stat 2 – Unchanged
DSJ – For DSJ = 0 or DSJ = 1 unchanged
– For DSJ = 2 then 0
– For DSJ = 3 then previous DSJ

Parallel Poll: Parallel poll is disabled after the reception of the secondary and is not re-enabled after the completion of the command.

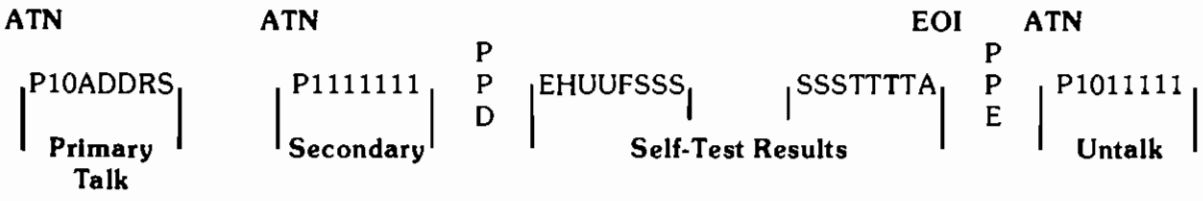
Read Self-Test Results

Type: Sense.

Purpose: The 9895A returns the results of the last self-test it has performed. This is useful after the Initiate Self-Test command or after the 9895A has been powered on (it performs a self-test at power on).

Description: After receiving the self-test secondary, the 9895A makes two bytes of the self-test results available. The second byte will be tagged with an EOI.

HP-IB Sequence:



Where:
- E – Error bit. If on, then an error has occurred.
- H – Head number. Indicates which head the read or write test failed on.
- UU – Unit number. Indicates which unit was selected when the error occurred.
- F – Format of operation. Indicates if the controller was in IBM (0) or HP (1) operation at the time of failure.
- SSSSSS – Subtest number. Number of the failing subtest.
- TTTT – Test number. Number of the failing test.
- A – "*" LED. Indicates state of the "*" LED.

NOTE

See page 4-7 for an explanation of self-test results.

Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – Unchanged

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

Read Loopback Record

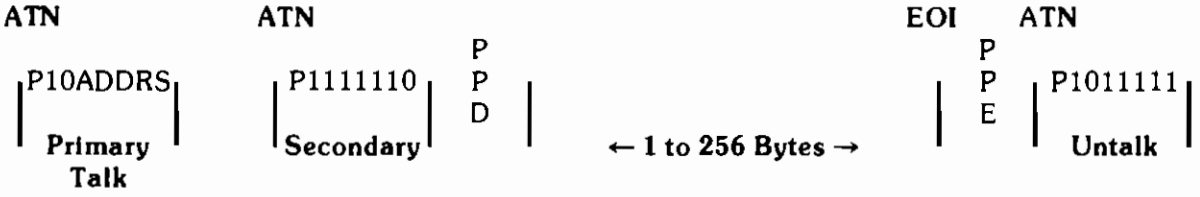
Type: Sense.

Purpose: The 9895A sends up to 256 bytes (see Write Loopback Record) from its internal data buffer over the HP-IB. This is used by diagnostics to test the HP-IB data path.

Description: Upon accepting the loopback secondary, the 9895A sends the bytes stored in its internal buffer. The most significant byte of the first word is transferred first. The 256th byte will be tagged with an EOI and the transfer terminated. If fewer than 256 bytes are requested, the device will realize that the transfer is complete when:

1. The 9895A has been untalked,
2. It accepts another byte from the HP-IB.

HP-IB Sequence:



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – Unchanged

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

Request Status

Type: Sense.

Purpose: The device returns four bytes of status information. These status bytes indicate how the last attempted operation completed, which unit was involved and the current status of the unit specified.

Description: After receiving the Request Status command, parallel poll response is disabled. If the unit's first status bit is set, the 9895A attempts to determine the type and format of the current disc (this may take up to 10 seconds). After the status operation has completed, the parallel poll response is re-enabled.

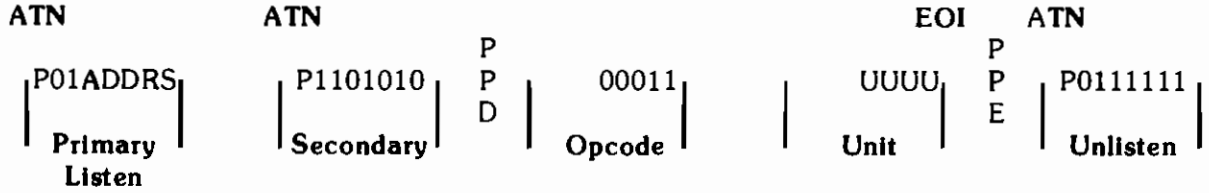
NOTE

There is also an unbuffered status request which uses a different secondary whose operation is identical.

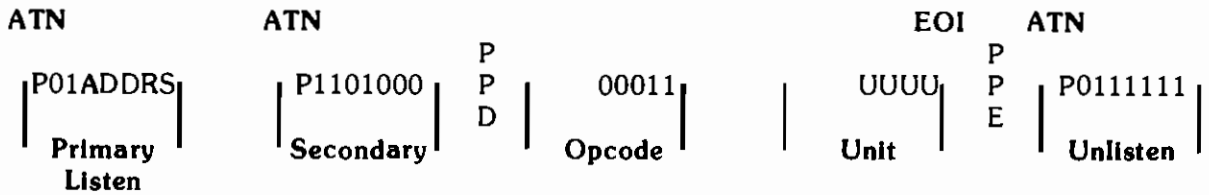
After the send status secondary, the 9895A sends four bytes of status information. The first two bytes (known as Stat 1) includes information about the last operation which the device performed. The Stat 1 unit field indicates which drive was involved in the operation. The D bit is set if a D bit was encountered during the operation.

HP-IB Sequence:

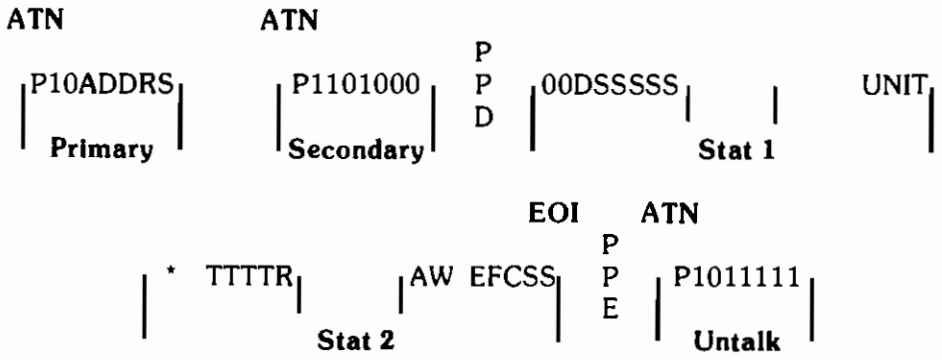
Request Status (Buffered)



Request Status (Unbuffered)



Receive Status



Where:

	Bit Number	Description
	Stat 1	(From previous operation)
D	13	D Bit
SSSSS	12-8	S1 (see following table)
UNIT	3-0	Unit Number
	Stat 2	(From current operation)
*	15	Set if one or more starred bits are set.
TTTT	12-9	Disc Type
R	8	Reserved
A	7	Drive Attention
W	6	Disc is Write Protected
E	4	*Drive Fault
F	3	First Status Bit
C	2	*Seek Check
SS	1, 0	*Drive Ready Status

S1 Binary (Decimal)	Meaning
00000 (0)	Normal completion. The operations completed without error, or the controller has just been cleared or powered up.
00001 (1)	Illegal opcode. The last command contained an opcode which is not recognized by the 9895A.
00111 (7)	Cylinder compare error. The target cylinder has one or more sectors in which the track number does not correspond with the track number of the remainder of the sectors. The controller will automatically re-try the read/write operation once if this is encountered.
01000 (8)	Uncorrectable data error. The disc read or verify operation was terminated because a CRC error was detected in the data field. The data is still transmitted for the bad sector.

S1 Binary (Decimal)	Meaning
01001 (9)	Sector compare error. The target sector cannot be found in the current track. Up to two passes of the track are made before this status is set. In this case, a CRC error exists in the preamble of the requested sector, or the subsequent data field cannot be found.
01010 (10)	I/O program error. This error is defined when: 1. An illegal secondary is received. 2. An improper number of data bytes are received. This status can only be set if the previous S1 was zero.
10001 (17)	Defective track or sector. During an HP write, read, read verify or verify, a set D bit was encountered.
10010 (18)	Re-tryable hardware error. An internal hardware timing error occurred during a data transfer or seek. The operation should be re-tried.
10011 (19)	Stat 2 error. Some condition in Stat 2 prevented the drive-related operation from completing normally. These conditions include: 1. Specified unit is between 0 and 3, but that drive is not connected to the controller. 2. There is no disc in the drive. 3. A hardware problem is detected in the drive. 4. The disc is unformatted or has an unknown format. 5. The disc is write protected (error only during a disc write operation). 6. The selected drive's first status bit is set. 7. IBM format requested on a double-sided disc. 8. ID triggered read attempted on an IBM disc.
10111 (23)	Unit unavailable. A command included a request for a unit number greater than 3.
11111 (31)	Drive attention. The indicated drive is requesting attention because: 1. A seek completed normally. 2. A Seek command failed due to: a. Drive fault, b. Out of bounds target cylinder or sector, c. The controller cannot find the target address. 3. Following an End command, a change in drive status was detected, including: a. Inserting a disc, b. Removing a disc.

Stat 2	Bit #	Meaning
*	15	Stat 2 error. This bit is set if one or more of the following bits are set in stat 2: 1. Drive fault, 2. Seek check, 3. Any drive not ready error. (See code 10011 in S1 table for list of possible causes.)
TTTT	12-9	Disc type. These four bits indicate the type and format of the disc currently present in the selected drive as follows: 0000 – Empty drive 0001 – Blank or unknown format, single-sided 0010 – HP format, single-sided 0101 – Blank or unknown format, double-sided 0110 – HP format, double-sided 1000 – IBM format, single-sided
A	7	Attention. This bit is set when a seek completes (successfully or unsuccessfully), or following an End command when stat 2 changes. It is cleared after the status is read.
W	6	Write protected. The disc in the selected drive has the write protect notch present.
E	4	Drive fault. This bit is set after the following occurs: 1. Drive goes not ready after End command, 2. Drive goes not ready during data transfer, 3. Hardware failure. Drive fault is cleared after the status is read.
F	3	First status bit. This bit is set when a disc is present in the selected drive after: 1. Power on, 2. The door is closed, 3. Self-test completion. First status is cleared after the status is read.
C	2	Seek check. This bit is set when a seek fails for one or more of the following reasons: 1. An out-of-bounds target sector was specified, 2. An attempt was made to access a non-existent physical track, 3. The seek algorithm could not find the target logical track.

Stat 2	Bit #	Meaning
		The seek check bit is cleared after the status is read.
SS	1, 0	Drive (not) ready. These two bits indicate the state of the selected drive as follows: 00 – Drive ready 01 – Undefined 10 – No drive connected to controller (this condition is established at power on and will not change if a new drive is added while the controller is operating normally) 11 – No disc in drive
Status:		No errors. S1 – 0 Stat 2 – Bits A, E, F and C are cleared DSJ – 0
Parallel Poll:		If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command. An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes.

Request (Logical) Disc Address

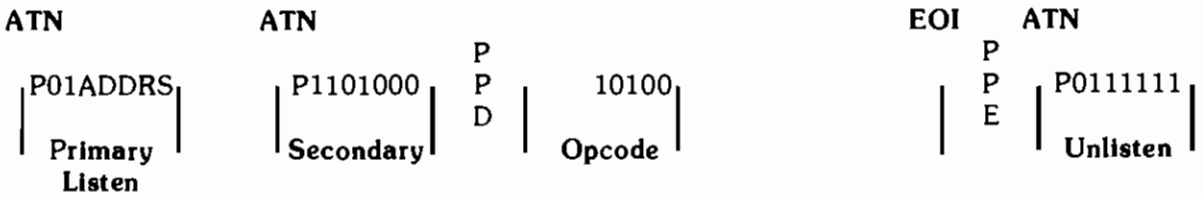
Type: Sense.

Purpose: The 9895A returns bytes indicating the current target address. This command is used to determine the address of the offending sector after a data error has occurred.

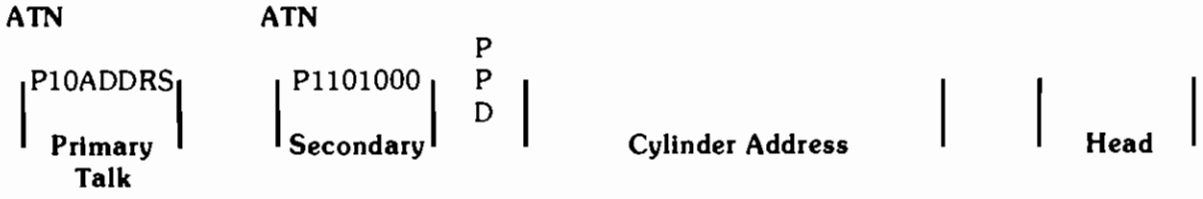
Description: Following reception of the appropriate command sequence, the 9895A returns four bytes indicating the current target sector. This includes two bytes of target cylinder address, one byte of target head address and one byte of target sector address.

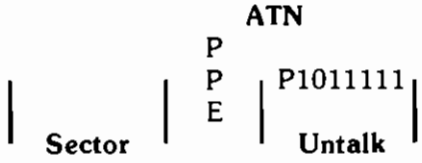
HP-IB Sequence:

Request (Logical) Disc Address



Send Address Command





Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes. However, this request is not necessary for normal operations.

Request (Physical) Disc Address

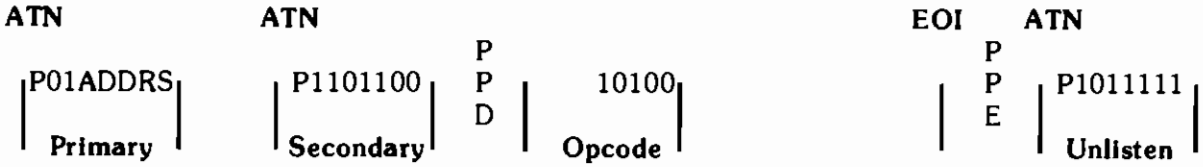
Type: Sense.

Purpose: The 9895A returns bytes indicating the physical cylinder on which the head actuator is positioned. This is useful for calculating the number of invisible tracks between the outer-most track and the current track. This is done by subtracting the physical cylinder address from the target cylinder address.

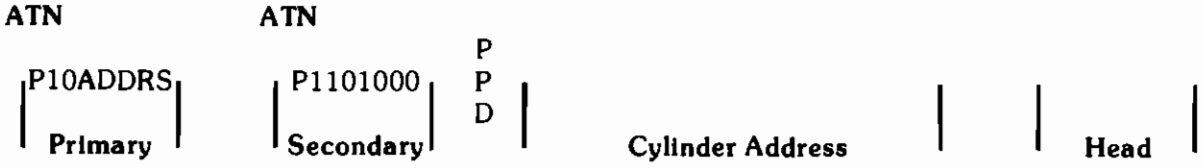
Description: After receiving the request (physical), the 9895A returns two bytes containing the physical cylinder address, one byte containing the head address and one byte of zeros.

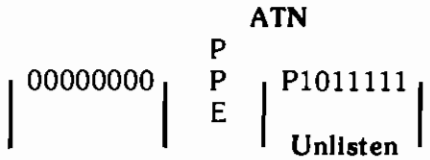
HP-IB Sequence:

Request (Physical) Disc Address



Send Address





Status: See Request (Logical) Address.

Parallel Poll: See Request (Logical) Address.

Control Commands

Universal or Selected Device Clear

Type: Control.

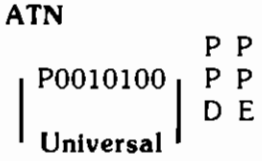
Purpose: A clear places the 9895A in a known state. Thus, it is useful when initializing a system on power up or after a host system crash. The clear also allows a power up DSJ of 2 to be cleared by sending a single byte. Since a clear updates the device's HP-IB address, it is useful if the system is being re-configured.

Description: Upon reception of either a universal or selected device Clear command, the 9895A stops handshaking with the HP-IB, parallel poll response is disabled and the following are performed:

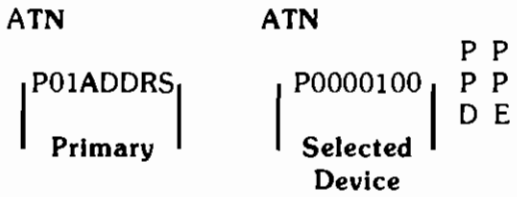
1. The PHI is reset,
2. HP-IB is updated from the device address on the controller board,
3. Stat 1 is cleared,
4. Stat 2 is updated appropriately,
5. DSJ set to 0,
6. All drives are re-calibrated to physical track 0,
7. The target address is set to cylinder 0, head 0, sector 0/1 for HP/IBM format,
8. Disable HP-IB parity checking.

HP-IB Sequence:

Universal Device Clear



Selected Device Clear



Status: No errors.

S1 – 0
Stat 2 – All bits cleared, then bits E and SS are set, if appropriate.
DSJ – 0

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Clear

Type: Control.

Purpose: This command gives the user the capability to place the 9895A controller in a known state and to programatically enable or disable the HP-IB parity check logic.

Description: After reception of the HP-300 clear secondary, the data byte and the device clear, the controller sets or clears the HP-IB parity enable in the PHI.

HP-IB Sequence:

HP-300 Device Clear

ATN	ATN		EOI	ATN		ATN
P01ADDRS	P1110000	P P D	X	P0000100	P P E	P0111111
Primary Listen	**Secondary Device Clear**		**Control Byte**	**Selected Device Clear**		**Unlisten**

Where: X – HP-IB parity check bit:
0 – Disable parity check,
1 – Enable parity check.

Status: No errors.

S1 – 0
Stat 2 – All bits cleared, then E and SS set, if appropriate.
DSJ – 0

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Initiate Self-Test

Type: Control.

Purpose: This command gives the user the capability to remotely initiate the 9895A self-test. The self-test results may then be read back using the Read Self-Test Results command. Self-test takes approximately 7 seconds to complete.

Description: Two bytes are sent following the self-test secondary and contain the following information:

The first byte contains the cylinder to be tested and is only pertinent if the W bit is set in the second byte of the command. The W bit is interpreted as follows:

0 – No write/read test performed,
1 – The write/read test is performed on the designated cylinder.

If the write/read test is selected, a double-sided disc is required and all data on both sides of the selected cylinder will be lost.

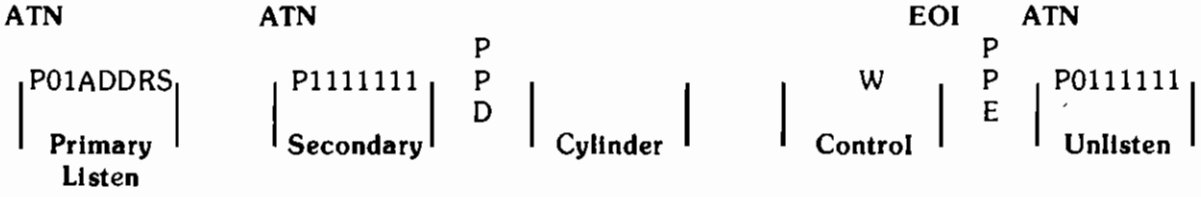
After the execution of the self-test, the controller will be in the same state as a power on condition would leave it.

NOTE

The self-test write test will re-format the selected test cylinder. This re-formatting will destroy data on the selected cylinder and change the sector interleave and offset so that it may no longer be optimal for the host system. After the write test is performed, the disc should be re-formatted by the Format command.

HP-IB Sequence:

Initiate Self-Test



Status: No errors.

S1 – 0
Stat 2 – Cleared, the bits E, F, C and * set, if appropriate.
DSJ – 2

Illegal cylinder number.

S1 – Drive attention
Stat2 – Bit C and * are set.

DSJ – 1

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally. If additional commands are sent before the controller is ready and while self-test is in progress, they will be lost.

Write Loopback Record

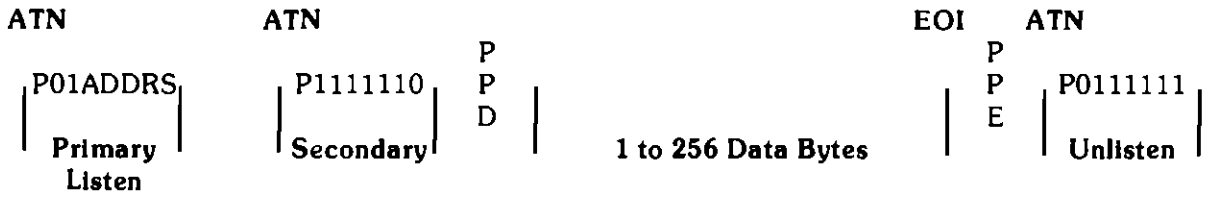
Type: Control.

Purpose: The 9895A stores up to 256 bytes in its internal buffer. A diagnostic could use the command, along with the read loopback record, to test the operation of the HP-IB link.

Description: After receiving the write loopback record secondary, the controller will store up to 256 bytes in the internal buffers. If less than 256 bytes are sent, the last byte must be tagged with an EOI.

HP-IB Sequence:

Write Loopback Record



Status: No errors.

S1 – Unchanged
Stat 2 – Unchanged
DSJ – Unchanged

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

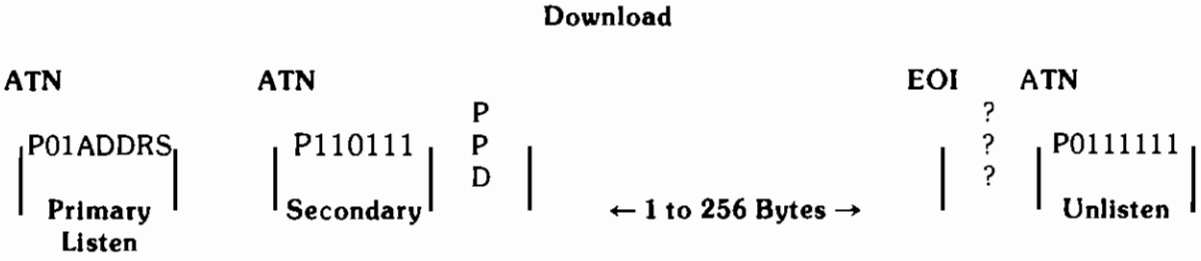
Download

Type: Control.

Purpose: This command allows the downloading and execution of MCC or Z80 code into the controller's internal RAM memory. It is intended for diagnostic purposes only, and as such should be used with care.

Description: After receiving the download secondary, up to 256 bytes are stored in the controller's RAM memory. Following the reception of the last byte, the code will be executed starting at the first byte if the controller processor is an MCC, or starting at the third byte if the controller processor is a Z80.

HP-IB Sequence:



NOTE

Updating of status and the operation of parallel poll is dependent upon downloaded code.

Seek

Type: Control.

Purpose: The Seek command updates a unit's target address and moves the head actuator to the new target cylinder. A seek usually precedes a data transfer operation or a series of consecutive data transfers.

It is important to note that the 9895A controller is totally dedicated to the selected drive during any drive-related operation (e.g., the Seek command). This disallows any overlapped seek operation between multiple drives.

Description: The device receives 6 bytes, including the seek opcode, the unit number, and the target cylinder, head and sector address. Checks are made to assure that the specified drive is available, that the entire command has been received and that the new target address lies within the following bounds:

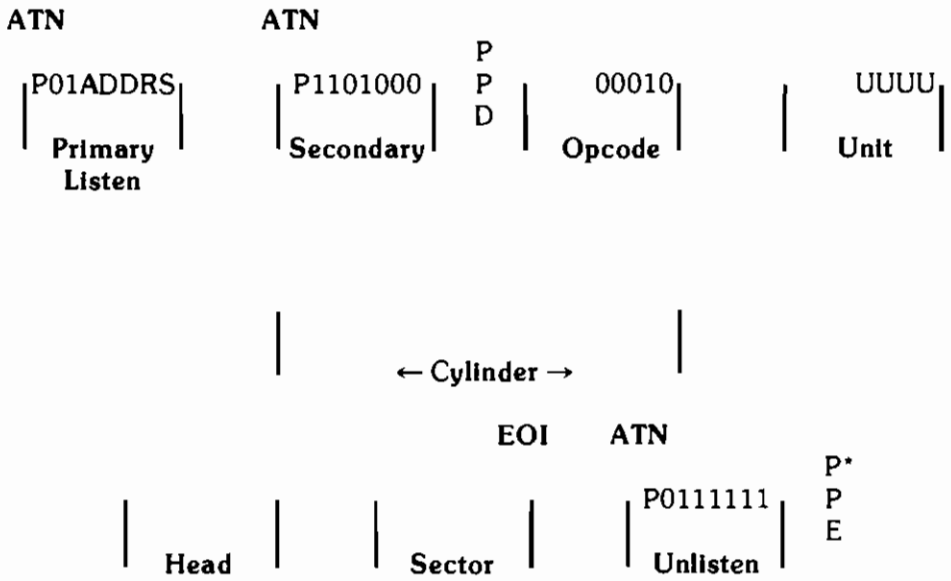
	HP		IBM
	Single	**Double**	**Single**
Cylinder address:	0 <= C <= 76	0 <= C <= 76	0 <= C <= 76
Head address:	H = 0	0 <= H <= 1	H = 0
Sector address:	0 <= S <= 29	0 <= S <= 29	1 <= S <= 26

If any of these tests fail, the status is updated and the Seek command is aborted with a "Seek Check" indication.

The following algorithm is used to locate a logical target track during the seek operation:

1. Determine if present logical track is the same as that requested. If they are, then seek is complete. Otherwise, proceed with step 2.
2. Read current cylinder location from disc.
3. If current address is not the location expected, then do physical seek to cylinder 0.
4. Estimate the direction and number of steps to the target cylinder.
5. Step actuator to target and read current head position.
6. If not at target cylinder address, repeat steps 3 and 4 until target found or re-try exhausted.

HP-IB Sequence:



* On seek completion.

Status:

Successful seek.

S1 – Drive attention
Stat 2 – Bit A set (drive attention)
DSJ – 0

Unsuccessful seek.

1. Illegal seek parameter, target track not found, off end of disc.

S1 – Drive attention
Stat 2 – Bits A and C set (see check)
DSJ – 1

2. Drive not ready during seek, track 0 indicator not found when expected.

S1 – Drive attention
Stat 2 – Bits A and E set (drive fault)
DSJ – 1

No disc, disc not ready, first status bit holdoff, disc not formatted, unknown format.

S1 – Status 2 error
Stat 2 – Unchanged
DSJ – 1

Parallel Poll:

The parallel poll response is re-enabled after the operation is completed, normally or abnormally. Normal completion occurs when the target cylinder is reached.

End

Type: Control.

Purpose: The End command serves a dual purpose as follows:

1. It causes the 9895A to cease responding to a parallel poll and puts the controller and drives in a "Stand By" state, and,
2. In case of a status change in any of the drives, the 9895A immediately re-activates its parallel poll response which can serve as a pseudo-interrupt facility to the bus controller.

Description: The End command should be issued after a series of commands to a single unit have been completed. The following is performed by the 9895A upon reception of an End command:

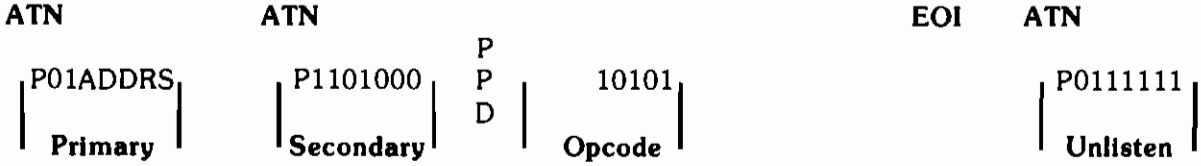
1. S1 – 0
   Stat 2 – Unchanged
   DSJ – 0
2. Disable parallel poll response.
3. Wait for change in drive status.

The 9895A will continue to check the status of all drives and will, at the same time, remain ready to execute any new HP-IB command. However, if no new command has been issued to the 9895A, and the state of a drive changes since the last time status was requested, the following is performed by the device:

1. Disc removed
   S1 – Drive attention
   Stat 2 – Bit A
   DSJ – 1
2. Disc inserted
   S1 – Drive attention
   Stat 2 – Bits A and F set (first status)
   DSJ – 1
3. Parallel poll is enabled on the HP-IB.

HP-IB Sequence:

End Command



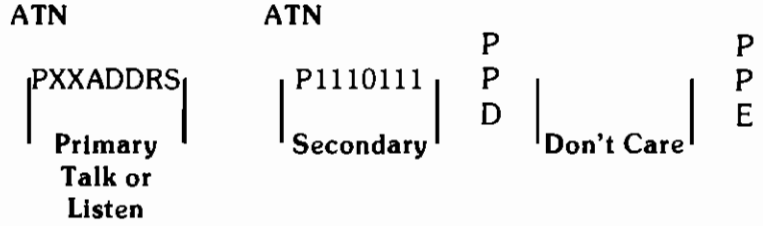
HP-IB CRC Secondary

Type: Control.

Purpose: The HP-IB CRC secondary is part of the 9895A command set to be compatible with future HP-IB devices which use the CRC data tests of the future HP-IB control chips. The 9895A will ignore this command; that is, not set I/O program error when it is received.

Description: The 9895A can be addressed to talk or listen. If addressed to listen, any number of data bytes may be sent; if addressed to talk, an EOI will be sent over the HP-IB.

HP-IB Sequence:



Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Door Lock

Type: Control.

Purpose: This command will lock the disc access door on the selected drive.

NOTE

Normal operation of the 9895A will lock the access door whenever a drive is selected for an operation.

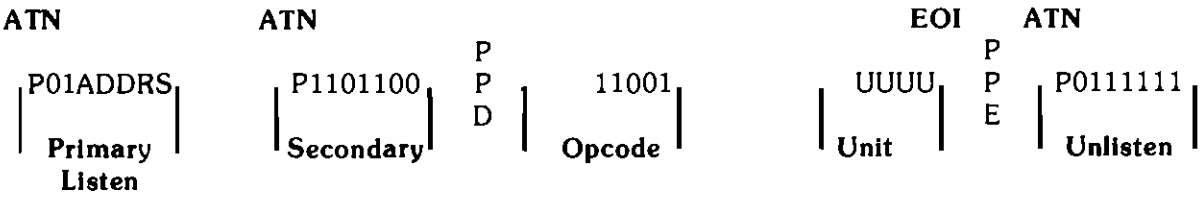
When the door is locked, the heads are also loaded. The heads loaded position represents the maximum wear condition for the disc.

Description: After sending the secondary, the opcode and the unit number, the 9895A will issue a command to the selected drive to lock the door. The door will remain locked and the heads loaded until one of the following conditions occur:

1. A Door Unlock command,
2. A Clear command,
3. An Initiate Self-Test command.

HP-IB Sequence:

Door Lock Request



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Door Unlock

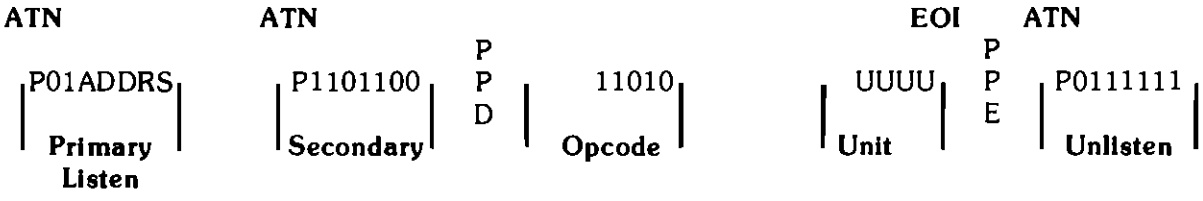
Type: Control.

Purpose: This command is used to unlock the disc access door. It is useful after the Door Lock command is given (see Door Lock).

Description: After the reception of the secondary, opcode and unit number, the 9895A will issue a command to the selected drive to unlock the access door. This command has no effect if the door was not previously locked.

HP-IB Sequence:

Door Unlock



Status: (See Door Lock)

Disc Read Commands

Buffered Read

Type: Disc read.

Purpose: Data is transferred through an internal buffer in 9895A before being sent to the HP-IB. This allows HP-IB data transfers to be asynchronous with the disc, and to vary from an arbitrarily low rate to about 190K bytes per second. The maximum number of bytes to be transferred in a buffered read is 256 (1 sector); the read request must be repeated for each additional sector transferred.

Description: Following reception of the Read command, parallel poll response is disabled and the status of the specified unit is checked. If the unit can be accessed, then the current cylinder number is read and compared with the target cylinder address. If they differ, a seek to the target cylinder is performed. This may occur if the actuator has slipped or if an auto-increment to the next cylinder is required.

If an HP format disc is being used, then the target sector's 256 bytes are read into the controller's buffer. If the read completes successfully, then the target address is incremented by one sector. If the sector is not found, a CRC error is indicated, or a D bit is encountered, the target address is not incremented.

If an IBM disc is present, then the target sector's 128 bytes are read into the controller's buffer. If the read completes successfully, then the target address is incremented by one. If the target sector is not found, a CRC error is indicated, or the D bit is encountered, then the target address is not incremented.

After the data has been buffered into the controller, the parallel poll response is re-enabled, indicating that the device has data ready to transmit. The bus controller should request the data by issuing the "Send Data" secondary. Upon receiving the secondary, the 9895A again disables parallel poll.

If the read was terminated before data was loaded into the buffer (i.e., any error except CRC or D bit on), the device will respond by sending an EOI tagged byte and enabling parallel poll response.

If there was no error, the sector's worth of data is made available. The bus controller can take any number of bytes up to a sector's length. If more than one sector is requested, the 9895A will send a byte tagged with an EOI. The number of bytes taken has no effect on the updating of the target address.

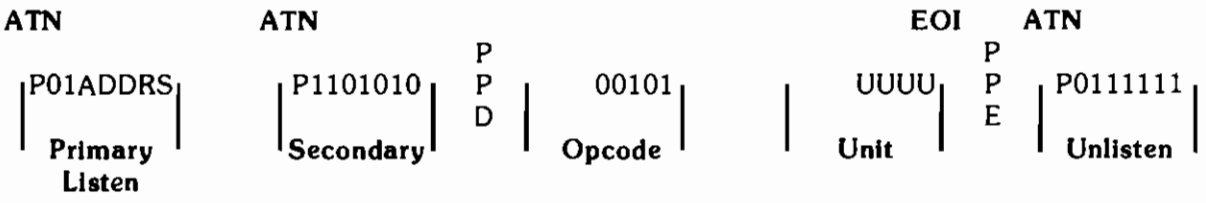
If the D bit or CRC error occurs, the corresponding data may be invalid.

Parallel poll response will be enabled after sending the last byte, sending another secondary to the 9895A or by untalking the 9895A.

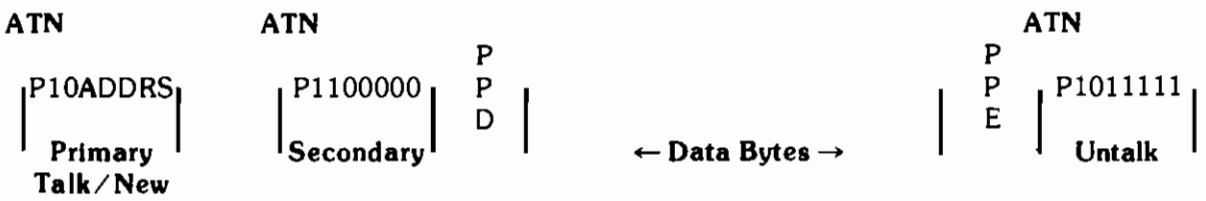
If more than one sector is to be transferred, then any number of buffered reads can be used in succession. If an error is encountered, all following reads will be held off due to a bad DSJ, so there is no chance of an error in the middle of a long read going unreported. However, error detection will be hastened if a DSJ is used after each read.

HP-IB Sequence:

Buffered Read Request



Send Data Request



Status:

No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful read.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution:

1. Unit 0 <= U <= 3
2. DSJ <> 2
3. Disc present and ready
4. Not first status
5. Stat 1 = Normal completion,
   I/O program error, or,
   Illegal opcode error.
6. Disc format is HP or IBM.

Parallel Poll:

The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes. However, this request is not necessary for normal operations.

Unbuffered Read

Type:

Disc read.

Purpose:

The unbuffered read allows more than one sector to be transferred from the disc to the bus controller using a single command.

Description:

Following reception of the Read command, parallel poll response is disabled and the status of the selected unit is checked. If the unit can be accessed (requirements for execution), the internal buffer is filled with a sector of data from the disc, just as in the buffered read. Now the 9895A waits for the Send Data command, then begins sending data to the bus controller. When all the bytes from the sector have been sent, the 9895A then reads the next sector into the internal buffer and sends it to the bus controller. This process continues until a termination condition is reached:

If the unit becomes unavailable, or a sector cannot be found when the buffer is empty, or if a CRC error or D bit is encountered, the sector in the buffer is sent followed by an EOI.

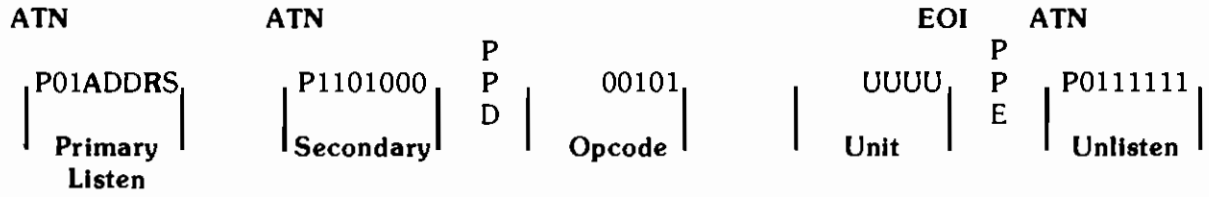
If at any time during the operation the device notices that it has been untalked or that the bus controller has sent a byte, the process is stopped.

Following any of the above terminations, status is updated and parallel poll response is re-enabled. If there was an error in reading the data from the disc, the target address is left pointing to the sector in which the error occurred. Otherwise, the target address points to the sector following the last sector read from the disc. Occurrence of the error will cause a dummy byte tagged with EOI to be transmitted to the host system, thereby terminating the read process.

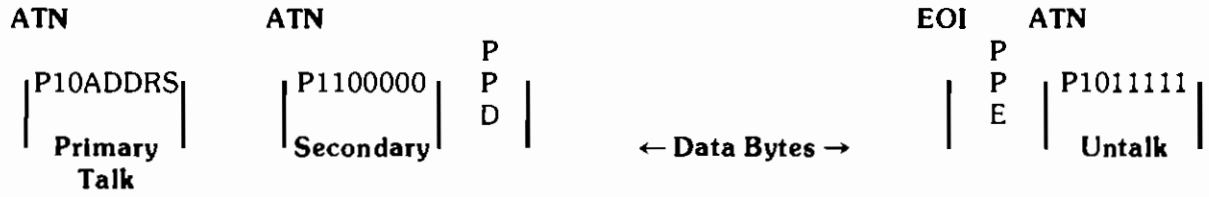
As has been seen, the unbuffered read actually uses the internal buffer to store the data. However, the protocol used is unbuffered in that the parallel poll response is not used to indicate when data is available. Thus, there is a pause in data flow to the HP-IB each time the buffer is re-filled from the disc. This pause occurs at the beginning of the read and after every sector has been transferred. Depending on when the read is started and the sector interleaving, this pause may be up to 160 milliseconds long.

HP-IB Sequence:

Unbuffered Read Request



Send Data Request



Status:

No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful read.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirement for Execution: See Buffered Read.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

Verify

Type: Disc read.

Purpose: The Verify command is a read with reduced margins which does not transfer data to the HP-IB. This is useful for performing a surface analysis of the disc or checking the integrity of the data on the disc.

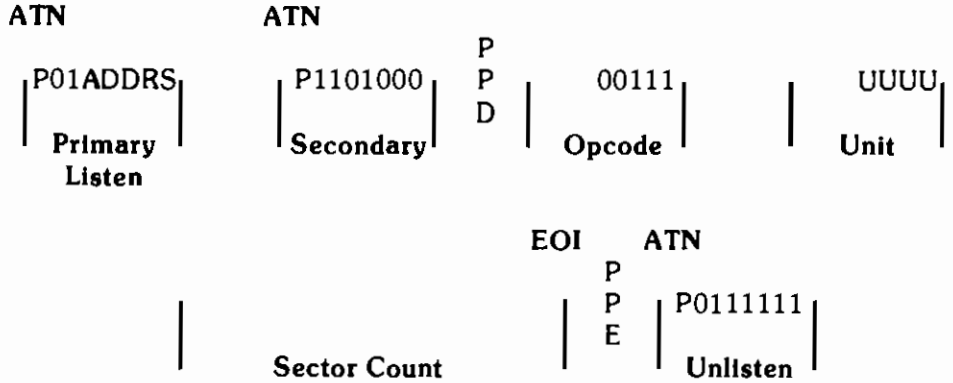
Description: As with other read commands, parallel poll is disabled, the availability of the unit is checked, and the target sector is sought. Starting with the target sector, consecutive sectors are read using reduced margins until any of the following occurs:

1. Unable to begin verify operation,
2. Sector count given in the command expires,
3. A seek or read error occurs,
4. A sector marked defective is detected,
5. The end of the disc is reached.

Parallel poll response is re-enabled upon completion of the verify. If an error was detected, the target address points to the sector in which the error occurred. Otherwise, the target address points to the sector following the last sector read.

HP-IB Sequence:

Verify Request



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Verify error.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution:

1. 0 <= Unit <= 3
2. DSJ <> 2
3. Disc present and ready
4. Not first status bit
5. Sector count >= 0
6. Disc of known format.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Buffered Read Verify

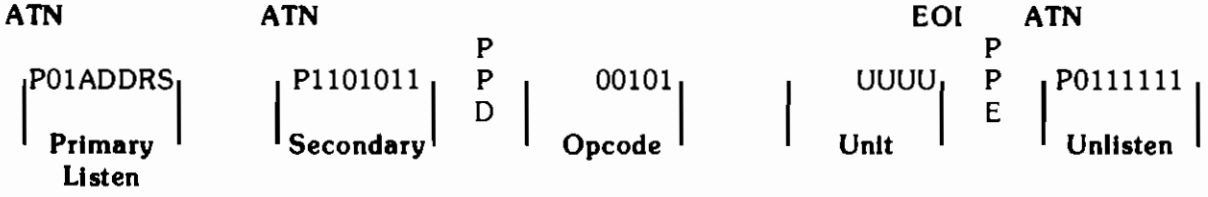
Type: Disc read.

Purpose: The buffered read verify is identical to the Buffered Read command except that the margins for good data are reduced. This command gives a high confidence that the data on the disc is recoverable.

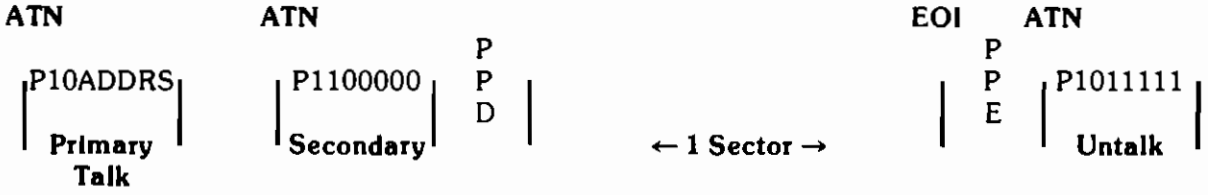
Description: See Buffered Read.

HP-IB Sequence:

Request Buffered Read Verify



Send Data



Status: See Buffered Read.

Requirements for Execution: See Buffered Read.

Unbuffered Read Verify

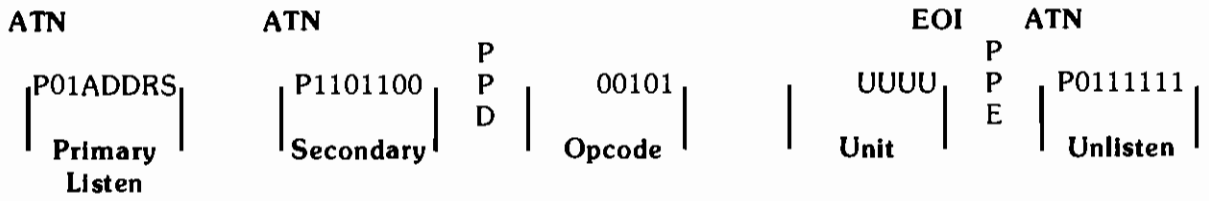
Type: Disc read.

Purpose: The unbuffered ready verify is identical to the Unbuffered Read command except that the margins for good data are reduced. This command gives a high confidence that the data on the disc is recoverable.

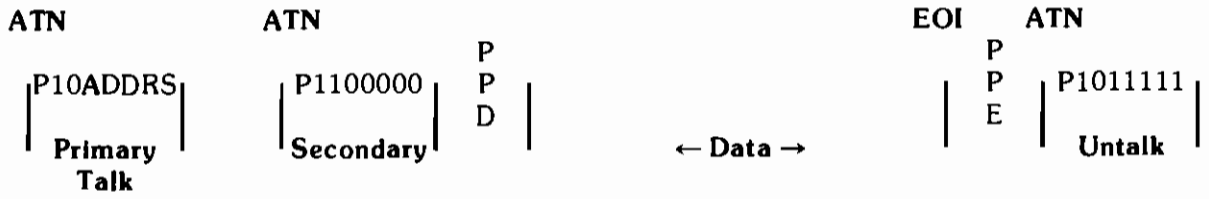
Description: See Unbuffered Read.

HP-IB Sequence:

Request Unbuffered Read Verify



Send Data



Status: See Unbuffered Read.

Requirements for Execution: See Unbuffered Read.

Cold Load Read

Type: Disc read.

Purpose: The cold load read is a command to read from unit 0, cylinder 0 at a specified head and sector address. This command consists of a seek to cylinder 0 followed by a read operation starting at the specified head and sector. Consecutive sectors are read until the bus controller stops the read.

Description: Following reception of the Read command, parallel poll is disabled, the DSJ cleared and the first status bit checked. If first status is set, the format of the disc is determined and the first status bit cleared. If the unit can be accessed, the 9895A performs a seek to cylinder 0, reads the specified sector into the internal buffer, then asserts parallel poll waiting for the send data secondary. After the send data secondary is received, parallel poll is disabled and the buffered sector is sent to the bus controller. When the sector has been sent, the controller fills the buffer with the next sector from the disc and then sends it to the bus controller. This process is repeated until one of the terminating conditions occurs:

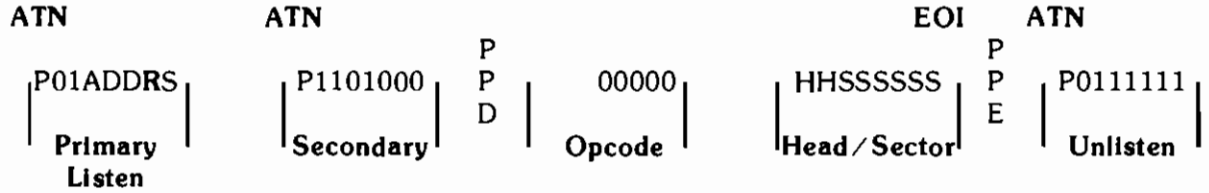
1. If the unit becomes unavailable or a sector cannot be found when the buffer is empty, a byte tagged with EOI is sent.
2. If a CRC error or D bit is encountered, the sector is sent followed by a byte tagged with an EOI.
3. If at any time during the operation the device notices that it has been untalked or that the bus controller has sent a byte, the transfer will be stopped.

Following any of the above terminations, status is updated and parallel poll response is re-enabled. If there was an error in reading data from the disc, the target address is left pointing to the sector in which the error occurred. Otherwise, the target sector points to the sector following the last sector read from the disc.

The cold load read uses unbuffered HP-IB protocol, although all sector transfers take place through the buffer. Thus, there is a pause in data flow to the HP-IB each time the buffer is re-filled from the disc. This pause occurs at the beginning of the read and after every sector is transferred. Depending on when the read is started and the staggering of the sectors (see the Format command), this inter-sector pause may be up to 160 milliseconds long.

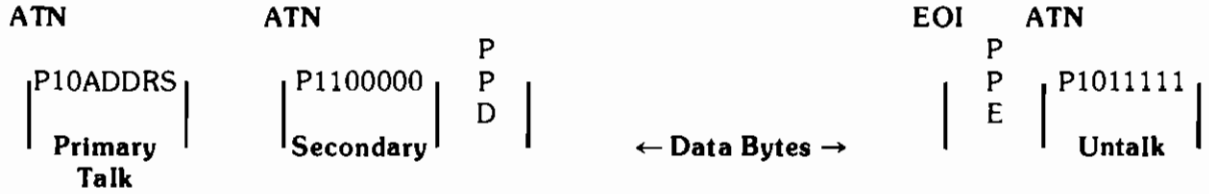
HP-IB Sequence:

Cold Load Read Request



Where: HH – Head address
SSSSSS – Sector address

Send Data



Status: No errors.

S1 – 0
Stat 2 – Type field updated.
DSJ – 0

Unsuccessful read.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 0

Requirements for Execution:

1. Unit available,
2. Disc ready,
3. Disc of known format,
4. Valid head and sector number.

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

ID Triggered Read

Type: Disc read.

Purpose: ID triggered read is used to read a sector of which the ID field cannot be found or read correctly. As an example, if the status from a read indicates that the target address sector is not found, the ID triggered read would be used to locate and trigger off of the previous sector's ID field to read the target sector. The host processor must be aware of the sector interleaving to request the correct sector to trigger from (see Format).

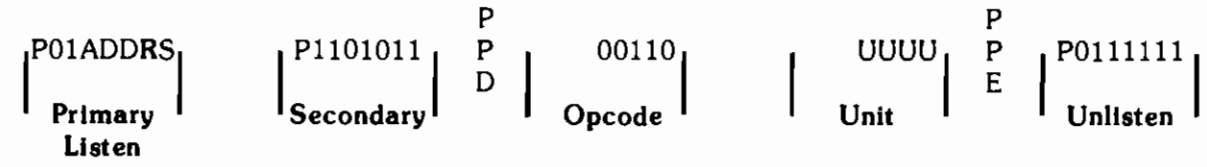
NOTE

ID triggered read is only supported for HP format and uses buffered protocol.

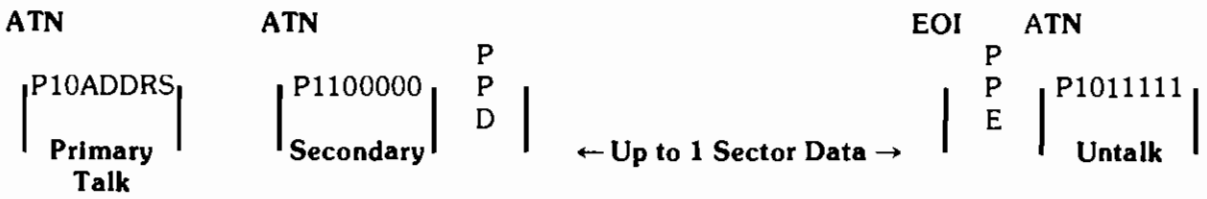
Description:

HP-IB Sequence:

Request ID Triggered Read



Send Data



Status: See Buffered Read.

Requirements for Execution: Disc must be in HP format. See Buffered Read.

Disc Write Commands

Buffered Write

Type: Disc write.

Purpose: The disc controller takes data transmitted on the HP-IB and stores it in an internal buffer before writing it on the disc. This buffering allows the host system to transmit asynchronously from an arbitrarily slow rate to about 190K bytes per second. The maximum HP-IB data rate is faster than the data rate to the disc, thus less time is used to transfer one sector over the HP-IB than it takes to write that sector. During the remaining time the HP-IB is free to be used by other devices on the bus.

Description: Following reception of the Write command, parallel poll response is disabled, status of the specified unit is checked and the parallel poll response is re-enabled.

At this time the bus controller should send the receive data secondary followed by up to one sector of data bytes. After seeing the receive data secondary, the 9895A will disable parallel poll response and begin placing data bytes in its buffer. The 9895A will stop accepting bytes after:

1. It receives a byte tagged with an EOI,
2. It has accepted one sector.

NOTE

If less than one sector is sent, the sector will be filled with data in the buffer from previous operations.

After the buffer has been accepted by the controller, the current address is checked with the target address. If they differ, a seek to the target cylinder is performed. This may occur if the actuator has slipped or if an auto-increment to the next cylinder is required.

If an HP format disc is being used, the 9895A attempts to write the 256 bytes in the buffer to the target sector. If the write completes successfully, the target address is incremented by one sector. If the target sector cannot be found or a D bit is encountered, the sector is not written and the target track is not incremented.

If an IBM format disc is being used, only 128 bytes from the buffer are written to the disc. If the write completes successfully, the target address is incremented by one sector. If the target sector is not found, the sector is not written and the target address not updated.

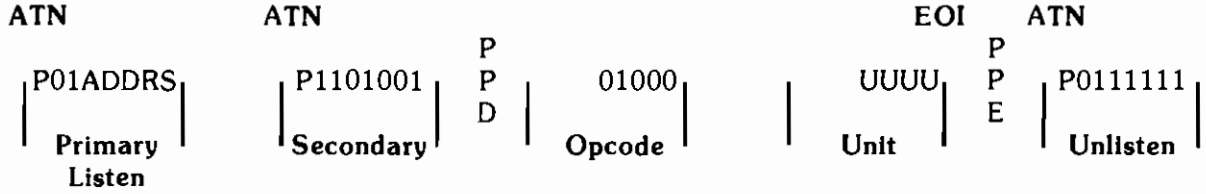
NOTE
In IBM format, writing to a sector which has the D bit on clears the D bit.

Parallel poll is re-enabled after the write completes or aborts.

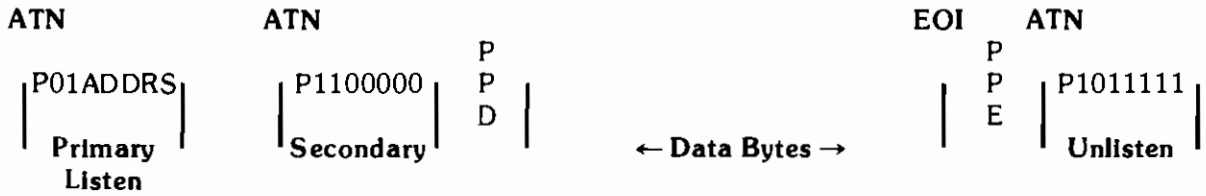
If more than one sector is to be written, any number of write commands can be used in succession. The 9895A will update the target address automatically. A write will fail if it follows another write which failed, so there is no chance of an error in the middle of a long transfer going unreported. However, error detection will be quickened if a DSJ is used after each write sequence is completed.

HP-IB Sequence:

Buffered Write Request



Receive Data



Status:

No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful write.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution:

1. 2 data bytes in command
2. 0 <= Unit <= 3
3. DSJ <> 2
4. Disc present and ready
5. First status bit not set
6. Stat 1 = Normal completion,
   I/O program error or illegal opcode error
7. Disc not write protected

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Unbuffered Write

Type: Disc write.

Purpose: The unbuffered write allows more than one sector to be transferred from the bus controller to the disc using a single HP-IB command sequence. Due to the inability to share the HP-IB during the transfer, the unbuffered write is not the preferred mode when HP-IB performance is desired.

Description: Following reception of the Write command, parallel poll response is disabled and status of the specified unit is checked. The 9895A now waits for the receive data secondary and then fills its internal buffer with one sector from the bus controller. When the buffer is full, the 9895A searches for the target sector and writes the buffer to it. When the buffer has been emptied, the 9895A accepts another sector from the HP-IB and in turn writes it to the next sector of the disc. This process continues until a byte tagged with an EOI is received or an error occurs. The buffer containing the byte tagged with the EOI is written to the disc before the write completes.

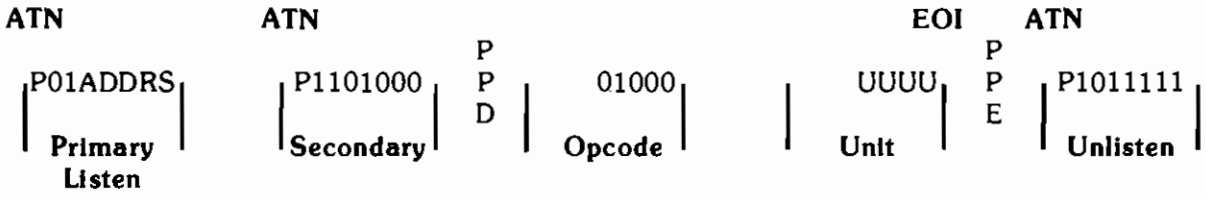
If an error occurs (i.e., drive goes not ready, an HP format D bit is encountered, the sector can't be found, etc.), writing to the disc will stop, but the 9895A will continue accepting bytes until an EOI tagged byte is received.

If an error occurs, the target address will point to the sector in which it occurred. Otherwise, the target address will point to the sector following the last sector written. When writing has been completed, parallel poll response will be re-enabled.

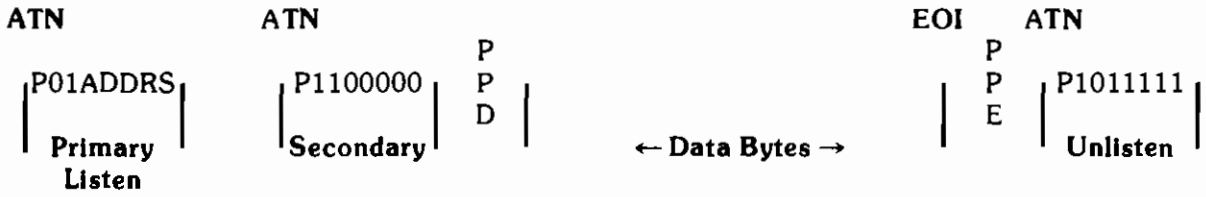
As in the unbuffered read, unbuffered write actually uses the internal buffer of the controller. However, the protocol used is unbuffered in that parallel poll is not used to indicate when data may be sent to the 9895A. Like unbuffered read, there is a pause in the data flow to the 9895A each time the buffer is written to the disc. The pause occurs after each sector is transferred. Depending on when the write starts and the staggering of the sectors (see the Format command), this pause may be up to 160 milliseconds long.

HP-IB Sequence:

Unbuffered Write Request



Receive Data



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful write.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution: See Buffered Write Command.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Initialize

Type: Disc write.

Purpose: The Initialize command is used to set or re-set D bits. It is similar to the buffered write with the following exception:

1. For HP format discs, all D bits on the target track will be set or re-set before the target sector is written.
2. For IBM format discs, the D bits of the target sector are set or re-set as the sector is written.

The Initialize command is especially useful when used with the Format command to make invisible tracks.

Description: Following reception of the Initialize command, parallel poll is disabled and the status of the selected unit is checked.

If an HP format disc is present, the entire target track is re-formatted, with the D bit in all sectors set or re-set according to the D bit specified in the opcode byte of the command. This re-formatting has several results:

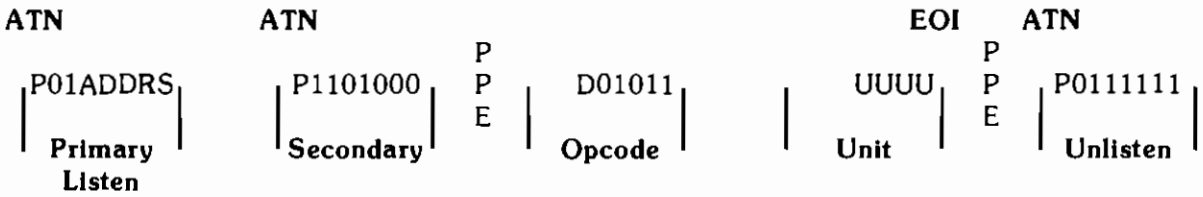
1. All data on the target track is lost,
2. The sector interleave of the track is changed to 2 (every other sector),
3. The spiral offset of the target track may no longer be optimal.

If an IBM format disc is present, the D bit is set or re-set according to the D bit specified in the opcode data byte as each sector is written. The initialization of an IBM sector does not affect the format or data of the remaining sectors of the target track, as does an HP format.

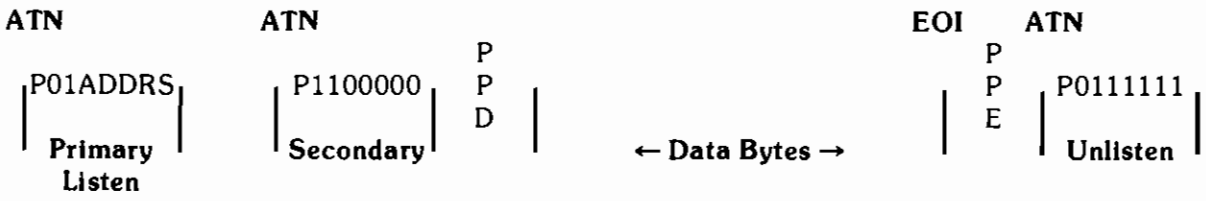
After the initialize request is sent, the command accepts and writes data in a manner identical to the Buffered Write command.

HP-IB Sequence:

Initialize Request



Receive Data



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution: See Buffered Write requirement.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Format

Type: Disc write.

Purpose: The Format command is a part of the sequence of commands which changes a disc which is unformatted or has the wrong format into a disc with a usable format. The 9895A supports three types of formats: HP double density, single- or double-sided and single-sided standard IBM format disc. The formatting operation also can make tracks marked with the D bit into invisible tracks.

The format sequence was designed to allow the disc controller to do as much of the work of formatting as possible, but still allow the host system to set its own criteria for:

1. Format type,
2. Bad track detection,
3. Sector interleave,
4. Spiral offset,
5. Format data byte.

Description: After receiving the Format command, parallel poll is disabled and the status of the specified unit is checked. If the unit can be used, the disc is formatted according to the type, old format override, interleave and selected data byte.

If the disc is of a different format than the Format command requests or the override old format bit is set, the entire disc will be formatted without invisible tracks.

If the disc is the same type as that requested by the Format command and the override old format bit is not set, 9895A will attempt to read from each track before it is formatted and make that track invisible if:

1. The track is already invisible,
2. A sector with a D bit set is found,
3. The track has no readable sectors.

NOTE

The 9895A looks at the D bit of a random sector to decide whether or not to make that track invisible. HP format requires that the D bit of all the sectors be set so there is no problem. But, IBM format allows a mixture of set and cleared D bits on one track. Therefore, before formatting an IBM disc, all D bits on a good track should be cleared and all D bits on a bad track set.

If the type parameter is set to 2, the disc will be given HP format. Double-sided discs will automatically be formatted on both sides, and single-sided disc only on head 0. If the type parameter is set to 8, the disc will be formatted IBM. Double-sided discs are not supported in IBM format. Single-sided discs will be formatted on head 0 only (IBM standard). Other values of type will cause an I/O program error.

The interleave parameter determines the order in which the sectors occur on a track. Data transfers which use the internal buffer on the 9895A, or host systems that accept data slower than the disc rate, operate more efficiently if the ordering of the sectors is non-sequential. Non-sequential sectors ordering allows for sectors to be arranged on the disc by logical use instead of by physical location.

In general, the interleave parameter indicates the number of disc revolutions required to send or receive one track's worth of data. For example, an interleave value of 5 would indicate that the sectors would be arranged on the disc in a manner that would require five revolutions to read one track.

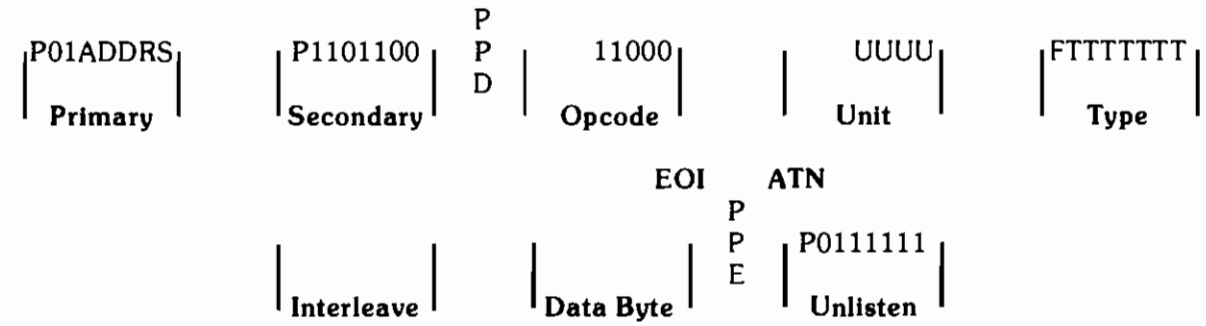
NOTE

An interleave parameter value of 2 (two revolutions per track) generates the sector sequence with the minimum time required to transfer one track.

HP format also uses the interleave parameter to determine the inter-track spiral offset. This offset minimizes the effect of track-to-track seeks by physically arranging sector 29 of one track and sector 0 of the next to make the track seek time approximately the same as the rotational latency.

HP-IB Sequence:

Format Request



Where: ADDRS – 9895A HP-IB address
F – Override old format bit
TTTTTTT – Wanted format type
2 – HP
8 – IBM
Interleave – 1 to 29 for HP
– 1 to 25 for IBM

Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful.

S1 – Error
Stat 2 – Bits A, F and C set, if appropriate.
DSJ – 1

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Appendix B
Error Messages

9845/9895 System

Error	Description
50	File number less than 1 or greater than 10.
51	File not currently assigned. Execute an ASSIGN statement for the file, or check the accuracy of the file number used.
52	Improper mass storage unit specifier. Check the values of the select code, unit code and controller address.
53	Improper file name. A file name can have 1 – 6 characters and can't contain a colon, quote mark, NULL or CHR$(255).
54	Duplicate file name. Choose another name or PURGE the old one.
55	Directory overflow. There is a maximum number of files that a mass storage medium can hold. A file will have to be removed to add another.
56	File name is undefined. Check the spelling.
57	Mass Storage ROM is missing. Check to see that the ROM is installed properly.
58	Improper file type. Use LOAD for PROG files, ASSIGN and GET on DATA files and LOADKEY for KEYS files.
59	Physical or logical end-of-file found. Attempting to READ# or PRINT# past the end of the file. Compare the data list to the file size.
60	Physical or logical end-of-record found in random mode. Compare the data list to the record size.
61	Defined record size is too small for data item. You can either PURGE and RE-CREATE the file with longer records or re-group the data being recorded.
62	File is protected or wrong protect code specified. Check to see that the protect code is included and spelled properly.
63	The number of physical records is greater than 32 767. That's the limit; use something smaller.
64	Medium overflow (out of user storage space). A file can't be set up because there isn't enough space. Use another medium or purge unwanted files.
65	Incorrect data type. You can't use GET on a DATA file that doesn't contain a program. Use TYP to find out what kind of data the computer is trying to be read.

Error	Description
66	Excessive rejected tracks during a mass storage initialization. The medium can't be initialized. If the medium is a flexible disk, use a different one. If the medium is a hard disc, call your HP Sales and Service Office for assistance, to determine whether there has been a hardware failure.
67	Mass storage parameter less than or equal to 0. Check values of variables. Record numbers, record lengths and number of defined records must be positive numbers.
68	Invalid line number in GET or LINK operation. Check line numbers. May be trying to LINK to file that doesn't contain a program.
69	Format switch on the disc off. Turn it on.
70	Not a disc interface. Check mass storage unit specifier.
71	Disc interface power off. Turn it on.
72	Incorrect controller address, controller power off, or disc time out. Check mass storage unit specifier; make sure controller is on.
73	Incorrect device type in mass storage unit specifier.
74	Drive missing or power off.
75	Disc system error, type I[1].
76	Incorrect unit code in mass storage unit specifier.
77	Disc system error, type II[1].
78	Unused.
79	Unused.
80	Cartridge out or door open. Also check to see if interface is connected properly.
81	Mass storage device failure. Possible power failure.
82	Mass storage device not present. Check mass storage unit specifier.
83	Write protected. Check the write-protection device on the medium or drive.
84	Record not found. There is a bad spot on the medium.
85	mass storage medium is not initialized.
86	Not a compatible tape cartridge.
87	Record address error; information can't be read. Hardware failure. Check for a dirty read head.
88	Read data error. Hardware failure. Check for a dirty read head.
89	Check read error.
90	Mass storage system error.

[1] See the Mass Storage Techniques Manual.

Appendix C
Accessory Installation Guide

RACK MOUNT INSTALLATION
KIT 09895-88022

WARNING

LIVE VOLTAGES ARE EXPOSED INSIDE FLEXIBLE DISC MEMORY. DISCONNECT POWER BEFORE BEGINNING INSTALLATION. ALSO, UNIT WEIGHS BETWEEN 45 AND 60 POUNDS (20 AND 27 KG). BE CAREFUL WHEN LIFTING.

CAUTION

DON'T PLACE THE UNIT ON THE FRONT SURFACE, AS THE DOOR HANDLES EXTEND BEYOND THE FRAME.

CAUTION

FLEXIBLE DISC MEMORY CANNOT BE SUPPORTED BY FRONT PANEL ONLY. THE RACK MOUNT INSTALLATION MUST HAVE SIDE SUPPORT RAILS.

---

1. Remove power and interface cables from rear panel connectors.
2. Open the drive doors and pull at points A and B (as shown in Figure C-1) to remove the front panel.
3. Place the unit on a broad, flat object (such as a book), so that the feet are off the surface.
4. Remove the four recessed screws (two per side) on the exposed front panel as shown in Figure C-2. Keep the screws and washers for mounting into the rack.
5. Remove the cover-securing screw in each of the lower corners on the rear of the unit.
6. Slide the cover back and off of the unit.
7. Install the top plate, being careful to slide the front edge of the top plate into the slot in the front panel bezel. Secure the top plate with the four screws provided. Install the two screws removed in step #5 into the same holes from which they were removed.
8. Install side rails into rack and secure. For HP 29400B Series racks order Accessory #12679B. Do not use slide brackets for mounting.
9. Place the unit in the rack and secure it to the rack using the screws and washers removed in step #4 into the same recessed holes shown in Figure C-2. Again, do not support the unit by the front panel only. The rack must have a shelf or side rails.
10. Snap in the front panel.

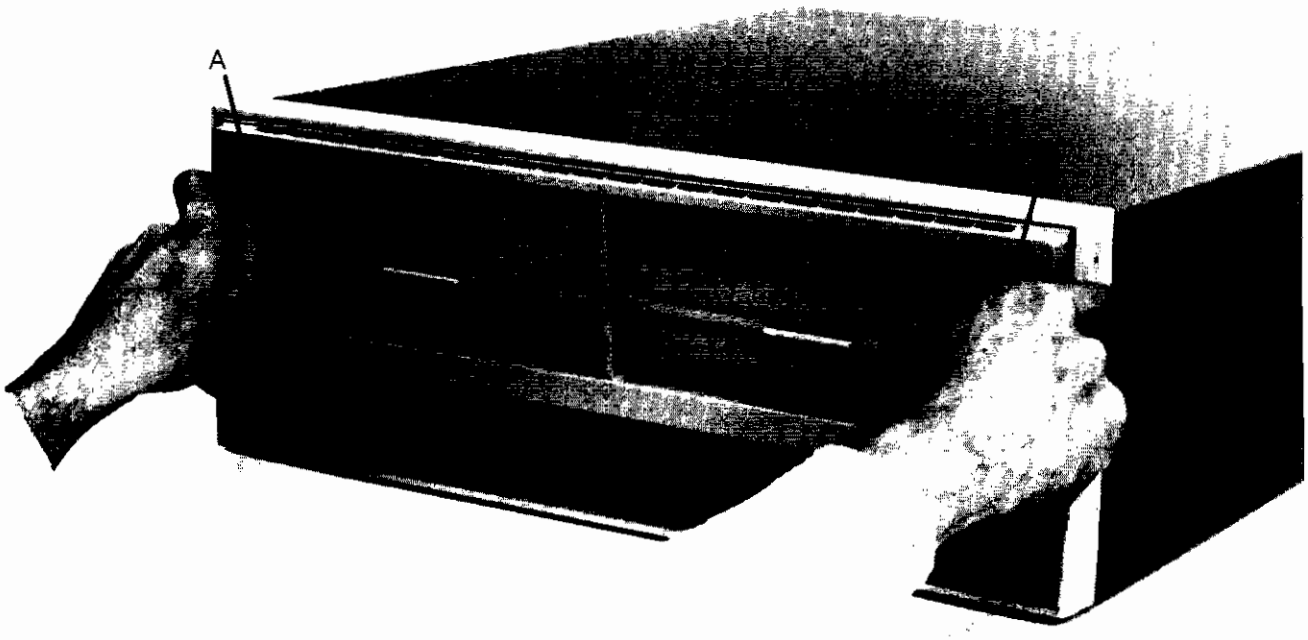


Figure C-1. Removing Front Panel

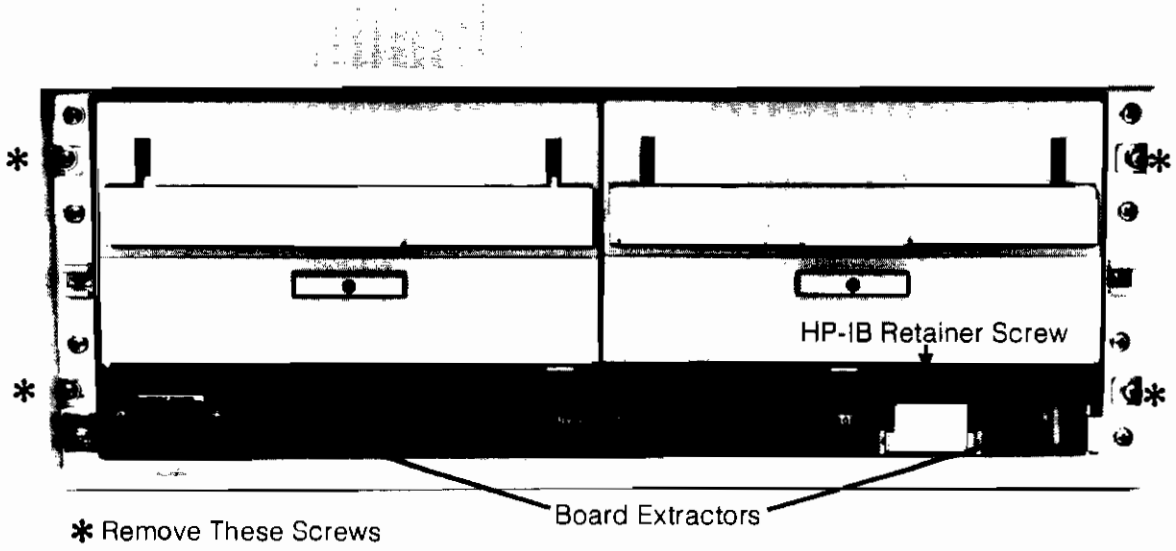


Figure C-2. Front Panel Removed

CONTROLLER INSTALLATION KIT 98951A

WARNING

LIVE VOLTAGES ARE EXPOSED INSIDE FLEXIBLE DISC MEMORY. DISCONNECT POWER BEFORE BEGINNING INSTALLATION. ALSO, UNIT WEIGHS BETWEEN 45 AND 60 POUNDS (20 AND 27 KG). BE CAREFUL WHEN LIFTING.

1. Remove power and interface cables from rear panel connectors.
2. Open the drive doors and pull at points A and B (as shown in Figure C-1) to remove the front panel.
3. Remove the screw securing the HP-IB connector retainer hanging below the right drive (see Figure C-3).
4. Free the end of the flat, gray HP-IB cable behind the retainer and bring it out the front of the slot right under the drive.
5. Slide the controller board into the unit from the front, component side up. Be sure the flat, gray cable stays above the controller board with the connector out the front of the unit.
6. Point the board extractors (see Figure C-2), located at the front corners of the controller board, straight out and then push the controller board as far into the unit as possible. Push the extractors flat into the controller board, thus seating the controller board the rest of the way into the unit.
7. Attach the connector on the gray, flat cable onto the edge connector on the right front side of the controller board (J3).
8. Install the retainer for the HP-IB connector just attached, as shown below in Figure C-3.

WARNING

THE 9895A DOES NOT CONTAIN OPERATOR SERVICEABLE PARTS. IF THE FOLLOWING OPERATION VERIFICATION TESTS DO NOT EXECUTE PROPERLY, REFER TROUBLESHOOTING ACTIVITIES TO SERVICE-TRAINED PERSONNEL.

9. Re-connect the power cord to the unit.
10. Switch the disc memory on and press the self-test switch (see Figure C-4). Upon completion of the test, the LED display should have only the right-most LED on (under the * of the ABCD* label). Any other final LED display pattern indicates that the test has failed.
11. If the above test failed, repeat the test by pressing and releasing the self-test switch. Should the test repeatedly fail, refer to the troubleshooting procedures in Chapter 3.

CAUTION
THE FOLLOWING TEST WILL WRITE OVER AND DESTROY ANY DATA ON THE DISC. USE ONLY BLANK, INITIALIZED DISCS TO PERFORM THE TEST.

12. Insert an initialized, write enabled, scratch disc into the drive(s) and close the door(s). Refer to Figure C-4 for the following steps.
13. Push the write self-test enable switch and hold it in while pressing the self-test switch. Release both switches. This test will successfully end in the same manner as the test in step 10. If it does not, try repeating it in the same manner. Should it again fail, replace the disc(s) and test again. If the test still repeatedly fails, refer to the troubleshooting procedures in Chapter 3.
14. With successful completion of the above tests, power down the unit. Connect the HP-IB interface cable, re-insert the front panel, and the unit is ready for use.

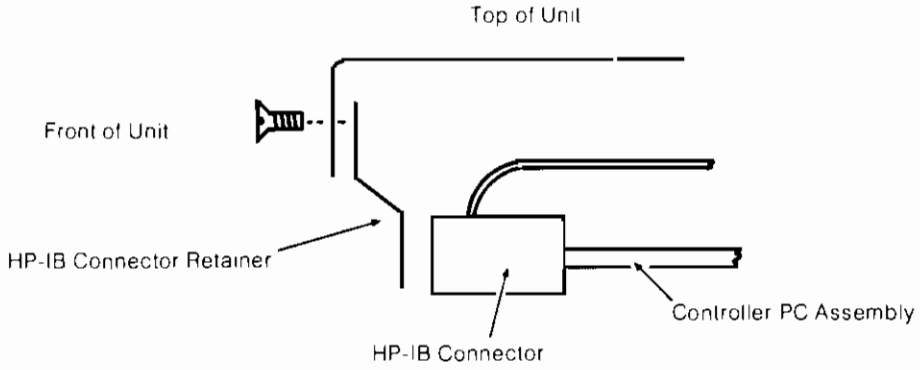


Figure C-3. HP-IB Retainer

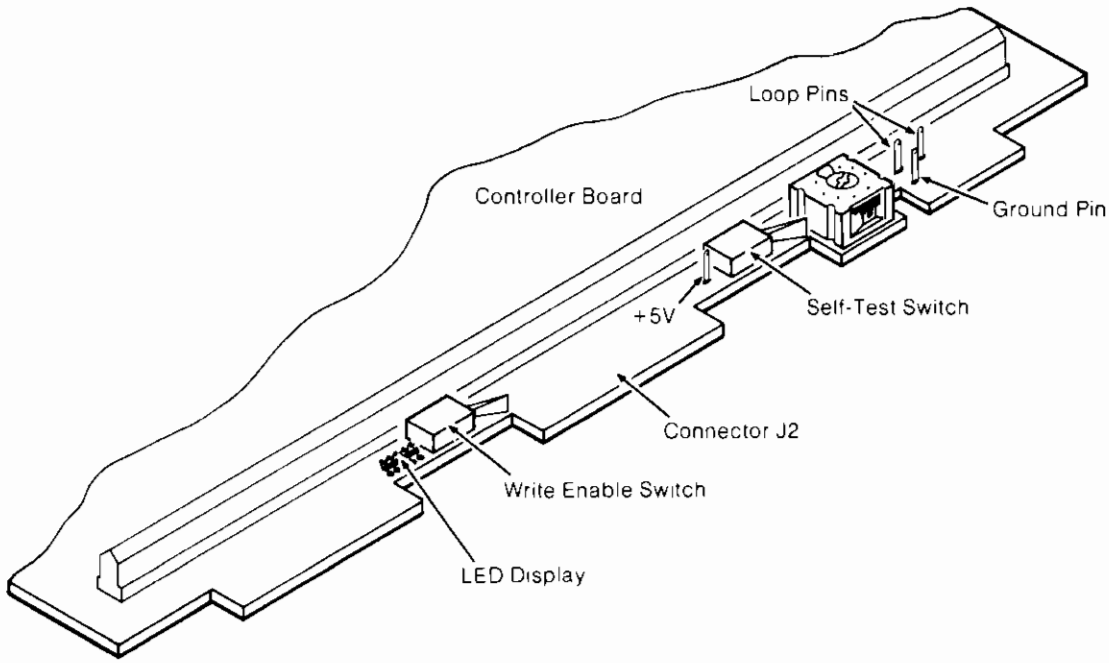


Figure C-4. Self-Test Controls

ACCESSORY DRIVE INSTALLATION KIT 98952A

WARNING

LIVE VOLTAGES ARE EXPOSED INSIDE FLEXIBLE DISC MEMORY. DISCONNECT POWER BEFORE BEGINNING INSTALLATION. ALSO, UNIT WEIGHS BETWEEN 45 AND 60 POUNDS (20 AND 27 KG). BE CAREFUL WHEN LIFTING.

CAUTION

DON'T PLACE THE UNIT ON THE FRONT SURFACE, AS THE DOOR HANDLES EXTEND BEYOND THE FRAME.

1. Check the drive number on the new drive. The drive number must be different from that of all other drives connected to the controller. Use the chart in Figure 1-3 of Chapter 1 to check the drive number.
2. Remove power and interface cables from rear panel connectors.
3. Open the drive doors and pull at points A and B (as shown in Figure C-1) to remove the front panel.
4. Place the unit on a broad, flat object so that the feet are off the surface.
5. Remove the four recessed screws (two per side) on the exposed front panel as shown in Figure C-2.
6. Remove the two screws in the lower corners of the rear of the unit.
7. Slide the cover back and off of the unit.
8. Lay the unit on its left side, bottom towards you, with the empty right drive position on the top.
9. Remove the bottom cover from the unit.
10. For Option 11 units (without controller), go to step 13. Remove the HP-IB connector retainer under the right drive position (see Figure C-5).
11. Remove the HP-IB connector from the controller board behind the retainer just removed.
12. Remove the controller board by pulling out on the board extractor (see Figure C-2) at each front corner of the controller board.
13. Remove the two screws securing the blank panel and slide it out of the unit. Retain the two screws and one washer for use with the new drive.
14. Identify the connector end of the following cables (look at the left drive and Figures C-5 and C-6 to clarify the following cable locations):

    a. Large, flat cable to attach to rear edge of the drive electronics board.
    b. Dc connector to attach to rear of drive.
    c. Ac connector to attach to rear of drive.

15. Slide drive into unit from the front. While drive is still protruding about 1 inch, attach the flat cable connector at J3 (see Figure C-5).
16. Slide the drive in the rest of the way.
17. Re-install the two screws removed in step 10, with washers, in the side of the unit.

CAUTION

MAKE SURE THE SCREW IN THE SLOTTED HOLE HAS A WASHER ON IT.

---

18. Install the two furnished half-inch screws, with washers, in the bottom (see Figure C-5).

CAUTION

MAKE SURE THAT THE FURNISHED HALF-INCH SCREWS GO IN THE BOTTOM, AND THE THREE-EIGHTHS-INCH SCREWS REMOVED IN STEP 13 GO IN THE SIDE. REVERSING THESE SCREWS WILL CAUSE IMPAIRED PERFORMANCE AND DAMAGE TO THE DRIVE.

---

19. Attach the ac and dc connectors at the rear of the drive (see Figure C-6).
20. For Option 11 units, go to step 25.
21. Slide the controller board into the unit from the front, component side up. Be sure the flat, gray cable stays above the controller board with the connector out the front of the unit.
22. Point the board extractor (see Figure C-2), at either front corner of the controller board, straight out and then push the controller board as far into the unit as possible. Push the extractors flat against the controller board, thus seating the controller board the rest of the way into the unit.
23. Attach the connector on the gray, flat cable onto the edge connector on the right, front side of the controller board.
24. Install the retainer for the HP-IB connector just attached, as shown in Figure C-5.
25. Replace the bottom cover onto the unit.
26. Place the unit on a broad, flat object and slide the cover onto the unit.
27. Secure the case to the unit with the screws previously removed from each of the lower, rear corners of the unit.
28. Re-install the screws previously removed from the front panel recessed positions (see Figure C-2).
29. Re-connect the power cord to the unit.
30. For Option 11 units (without controller), connect the unit to the 9895A via the slave cable (09895-61606). Remove the front panel of the 9895A and conduct the following steps on the 9895A to check out the 9895 Option 11.

31. Switch the disc memory on and press the self-test switch (see Figure C-4). Upon completion of the test, the LED display should have only the right-most LED on (under the * of the ABCD* label). Any other final LED display pattern indicates that the test has failed.
32. If the above test failed, repeat the test by pressing and releasing the self-test switch. Should the test repeatedly fail, refer to the troubleshooting procedures in Chapter 3.

CAUTION
THE FOLLOWING TEST WILL WRITE OVER AND DESTROY ANY DATA ON THE DISC. USE ONLY BLANK, INITIALIZED DISCS TO PERFORM THE TEST.

33. Insert an initialized, write enabled, scratch disc into the drive(s) and close the door(s). Refer to Figure C-4 for the following steps.
34. Push the write self-test enable switch and hold it in while pressing the self-test switch. Release both switches. This test will successfully end in the same manner as the test in step 29. If it does not, try repeating it in the same manner. Should it again fail, replace the disc(s) and test again. If the test still repeatedly fails, refer to the troubleshooting procedures in Chapter 3.
35. With successful completion of the above tests, power down the unit. Re-connect the HP-IB interface cable, re-insert the front panel insert, and the unit is ready for use.

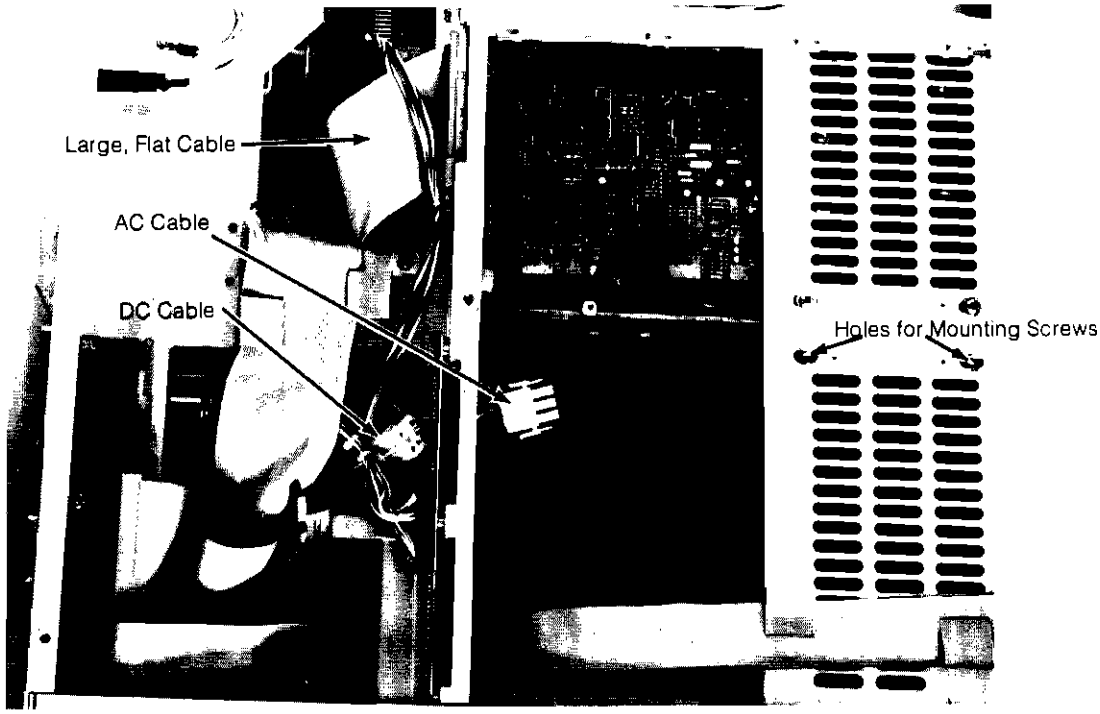


Figure C-5. Bottom View of Drive Location

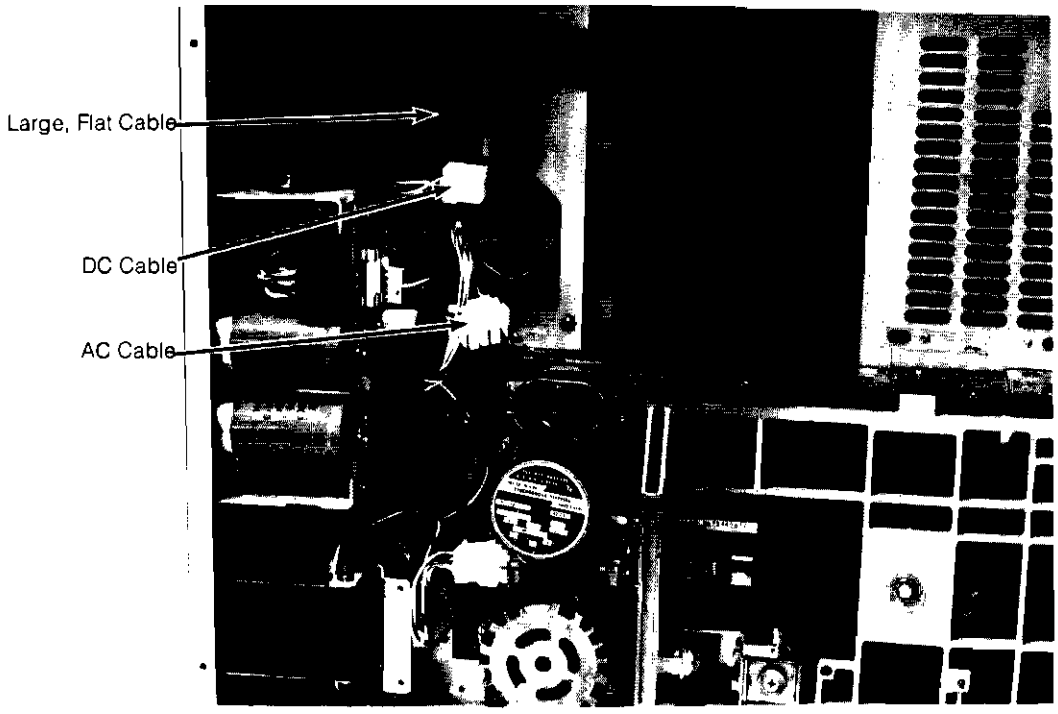


Figure C-6. Top View of Drive Location

KIT CONTENTS

Rack Mount Kit (9895-88022)

Quantity	Part Number	Description
1	09895-04102	Top Cover
4	2360-0192	Screw
4	2510-0107	Screw
1	09895-90035	Accessory Installation Guide

Controller Kit (98951A)

Quantity	Part Number	Description
1	09895-66500	Control Board Assembly
1	8120-2718	HP-IB Cable
1	09895-90035	Accessory Installation Guide

Accessory Drive Kit (98952A)

Quantity	Part Number	Description
1	0950-0430	Drive Assembly
2	2510-0049	Half-Inch Screw
3	3050-0071	Washer
1	09895-90035	Accessory Installation guide

Appendix D

Drive Jumper Configuration Chart

The jumper configuration on the drive electronics printed circuit board are to be as follows:

Jumpered	Open
A	B
D	C
DC	DR
DD	E
DL	FS
HO	HS
I	NP
IU	OS
NS	S
R	S1
RI	S3
RR	Y
SS	Z
S2	
TS	
WP	
X	
2S	

Some versions of the drive electronics board will not have some of these jumpers.

Appendix E
In-Use LED Pattern List

When the controller is operating under the control of a mainframe, the LED display will indicate what function the controller is performing. The following list of LED patterns and controller functions is included as an aid in troubleshooting.

LED Pattern	The controller is:
00010	waiting for a command and monitoring drive status.
00100	sending data to host system.
00110	receiving data from host system.
01000	determining status and format from requested unit.
01010	loading heads on a drive.
01100	waiting for a secondary HP-IB command.
01110	formatting a track.
10000	waiting for a command; last operation completed without error. DSJ = 0.
10010	waiting for a command; last operation completed with error. DSJ = 1.
10100	waiting for a command; power-on holdoff is active. DSJ = 2.
10110	waiting for a command; parity error was enabled and detected on last command. DSJ = 3.
11000	executing VERIFY command.
11010	moving the heads one track.
11100	writing a sector.
11110	reading a sector.

Note that if the right-hand LED is lit, the controller is not operating under the control of a mainframe. Refer to Table 4-2 for a list of error codes.

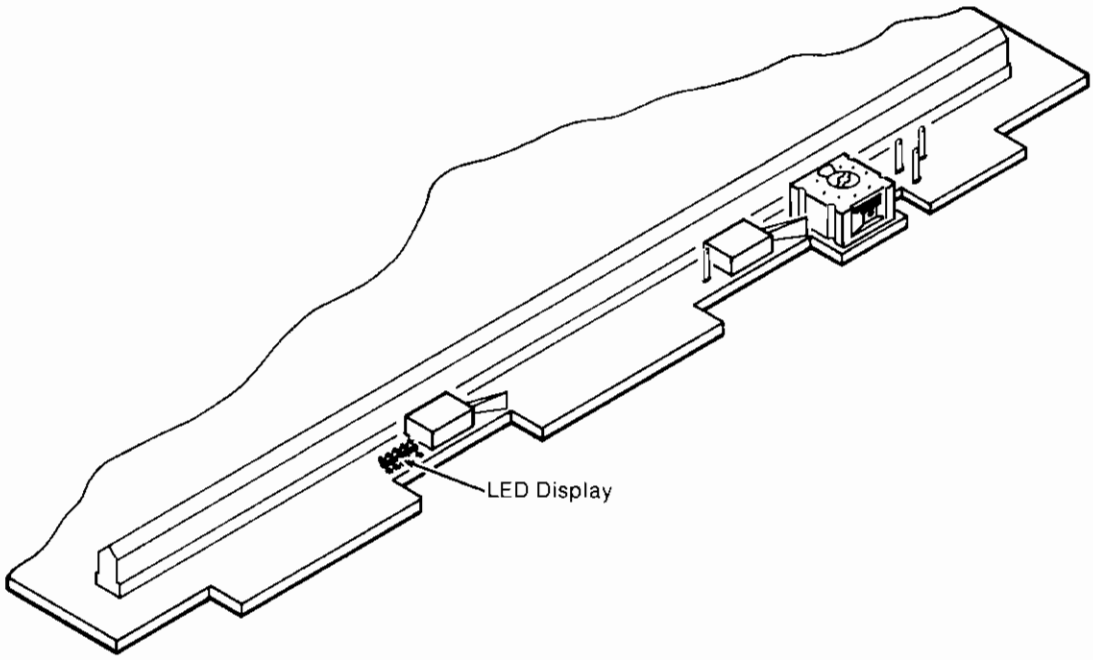


Figure E-1. LED Location

P/O A1 09895-66500 CONTROLLER BOARD

J2

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

+5V 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

R10-10 4.7K R11-9 4.7K R10-9 4.7K R11-8 4.7K R10-8 4.7K R11-7 4.7K R10-7 4.7K R11-6 4.7K R10-6 4.7K R11-5 4.7K R10-5 4.7K R11-4 4.7K R10-4 4.7K R11-3 4.7K R10-3 4.7K R11-2 4.7K

J3

ATN 6 — U26 A: B_A 3, D_A 2, SR_A 1 — 38 ATN
SRQ 8 — U26 B: B_B 5, D_B 6, SR_B 7, E_AB 4 — 44 CIC
U15D: 8 → 9 — 39 SRQ

REN 17 — U26 C: B_C 11, D_C 10, SR_C 9 — 42 REN
IFC 10 — U26 D: B_D 13, D_D 14, SR_D 15, E_CD 12 — 43 IFC

NDAC 12 — U8 A: B_A 3, D_A 2, SR_A 1 — 41 DAC
NRFD 14 — U8 B: B_B 5, D_B 6, SR_B 7, E_AB 11 — 40 RFD
U15C: 6 → 5 — 46 DAV/EOI ENABLE

U34

A13 22
A14 21
A15 20

D8 27
D9 28
D10 29
D11 30
D12 31
D13 32
D14 33
D15 34

D1 26
DMAREQ 14 NC
+12V 12 +12V
+5/+12V 24 +5V
+5V 48
TRIG 37 NC

U13: 01–08 → A0–A7; CE1 20; A8 23, A9 22, A10 21, CE2 19, CE3 18

U12: 01–08 → A0–A7; CE1 20; A8 23, A9 22, A10 21, CE2 19, CE3 18

U11: 01–08 → A0–A7; CE1 20; A8 23, A9 22, A10 21, CE2 19, CE3 18

U10: 01–08 → A0–A7; CE1 20; A8 23, A9 22, A10 21, CE2 19, CE3 18

14 I/01
13 I/02
12 I/03
11 I/04

CS 8

+5V — R15-5 1.0K

NOT

ENABLE

EOI 18 — U8 — 3 EOI
DAV 16 — U8 — 2 DAV
U8 — 45 HSE
U8 — 47 DIO ENABLE

DIO1 26 — U7 — 11 OIO1
DIO2 24 — U7 — 10 DIO2

DIO3 22 — U7 — 9 DIO3
DIO4 20 — U7 — 8 DIO4

DIO5 25 — U25 — 7 DIO5
DIO6 23 — U25 — 6 DIO6

+12V
C9 .01
DELAY
R13 17.8K
RTL
SYSCOM
GND

DIO7 21 — U25 — 5 DIO7
DIO8 19 — U25 — 4 DIO8

GND 3 5 7 9 11 13 15

TRIG 37 NC

U11 — A4 A5 A6 A7 A8 A9 A10 CE3 CE2 CE1
U10 — A4 A5 A6 A7 A8 A9 A10 CE3 CE2 CE1

+5V
R15-7 1.0K
U50A — A12

U49B

+5V
R15-4 1.0K
U55 — PS J CK K CLR Q

IDEND 18 NC
IOGO 19
WRITE 16
CS 23
PON 15

U54B
U51B
U53C
U52B

INT 17

+5V
C17 0.1
C18 0.1
C19 0.1
C14 0.1
U82
Y1
U81F
U81E

4 2 1,5 3

D0 D1 D2 D3 D4 D5 D6 D7

J2

+5V 48 R9-2 4.7K
+5V 47 R9-3 4.7K
+5V 46 R9-4 4.7K
+5V 45 R9-5 4.7K
+5V 44 R9-6 4.7K
+5V 43 R9-7 4.7K
+5V 43 R9-8 4.7K
+5V 42 R9-9 4.7K
+5V 41

A15 30 +5V R11-2 4.7K

D0 D1 D2 D3 D4 D5 D6 D7 ②

A0 A1 A2 A3 A4 ②

U36
U35
I/O1 I/O2 I/O3 I/O4
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
CS WE

U50D R15-5 1.0K A11

U9
NOT USED

PROM ROM
E D C B A

U38
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13
P/O U39
NOTE 1

+5V R19 10K
NC BUSACK BUSREQ

U14

+5V R7 4.7K C5 .01
U68 Q CLR NC
+5V R14-2 4.7K
U53A U53D
RESET
R9-10 4.7K PONRES (2,3) PROGRES ②
WR R12-4 4.7K WR ②
WAIT R12-5 4.7K WAIT ③
HALT R12-3 4.7K
NMI R12-8 4.7K
IORQ R11-3 4.7K IORQ ②
M1 R12-9 4.7K M1 ②
U15F U15B
P/O U39

J4 35 POP
J2 3 PONRES
8 WR
9 WAIT
13 HALT
6 NMI
10 IORQ
4 M1

U9
NOT USED

R15-8
1.0K
+5V

U50B

A13

U49B

U53B

U54C

U37
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
IN/OUT ENABLE

U52C

U81B

R14-7
4.7K
+5V

A12
A13
A14
A15

NOTE 1

A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7

P/O U39

IORQ
MI
RD
RFSH
MREQ
INT
CLK GND +5V

C45
.47
+5V

R11-3
R12-9
R12-10
R12-6
R12-2
R12-7
4.7K
+5V

IORQ
MI
RD
RFSH
MREQ
INT

U49A

U54A

U15E

A14
A13

2

U81E

U79
S G

8or4
HIDEN

C47
33pf
R29
220
R31
22
R30
1.2K
Q1B
U15A
SWB1
SWB2

R15-2
1.0K
R14-8
4.7K
R14-4
4.7K
PS
CK U80
J K Q Q̄
CLR

U52D

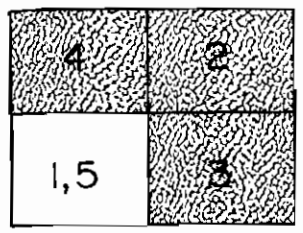
8MHZ

4MHZ

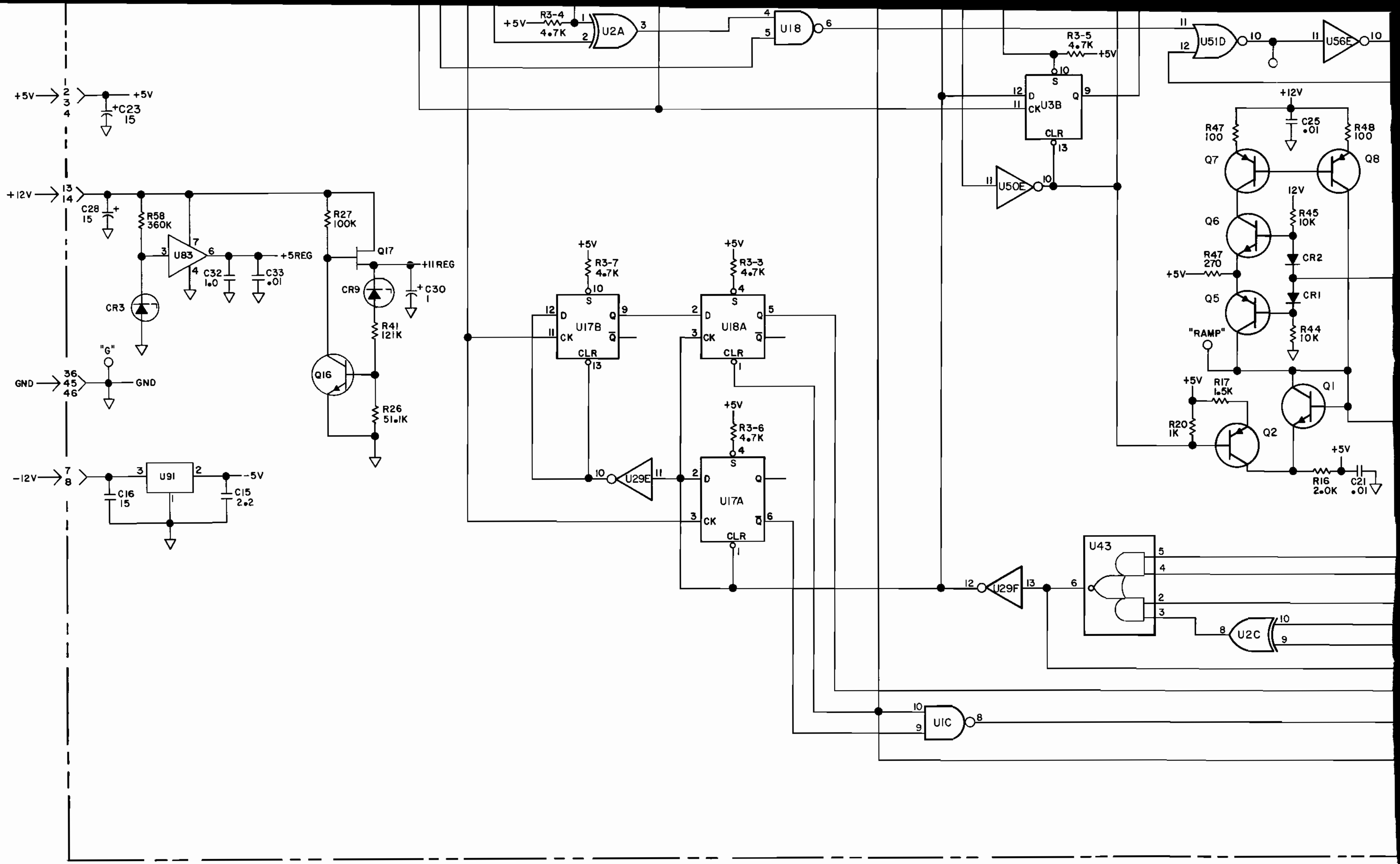
09895-J-75019
ORG

NOTES:

1. U15B & U15F ADDED AT DATE CODE 2038
2. U54A WAS CONNECTED TO U39 PIN 3 PRIOR TO DATE CODE 2038

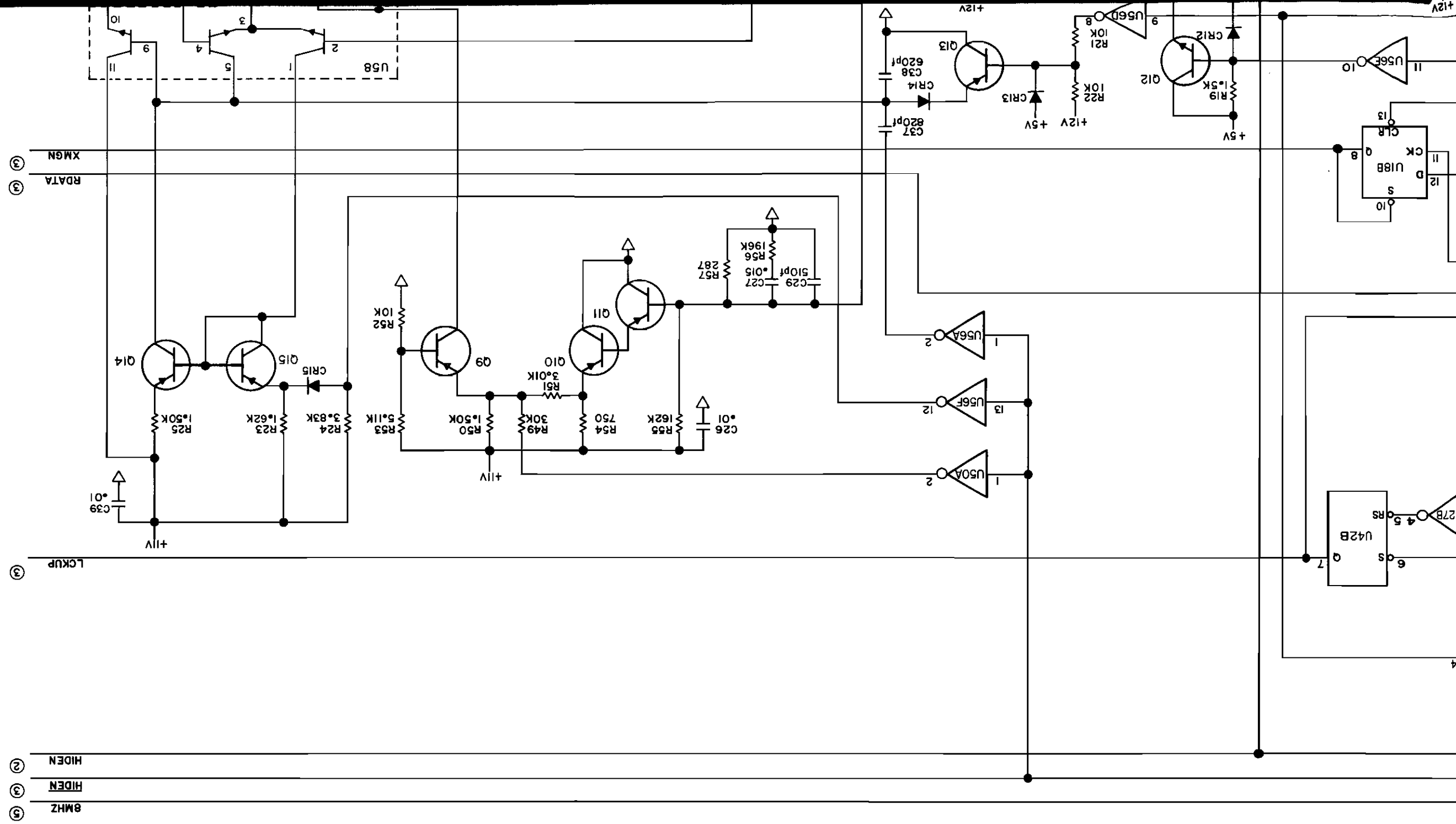


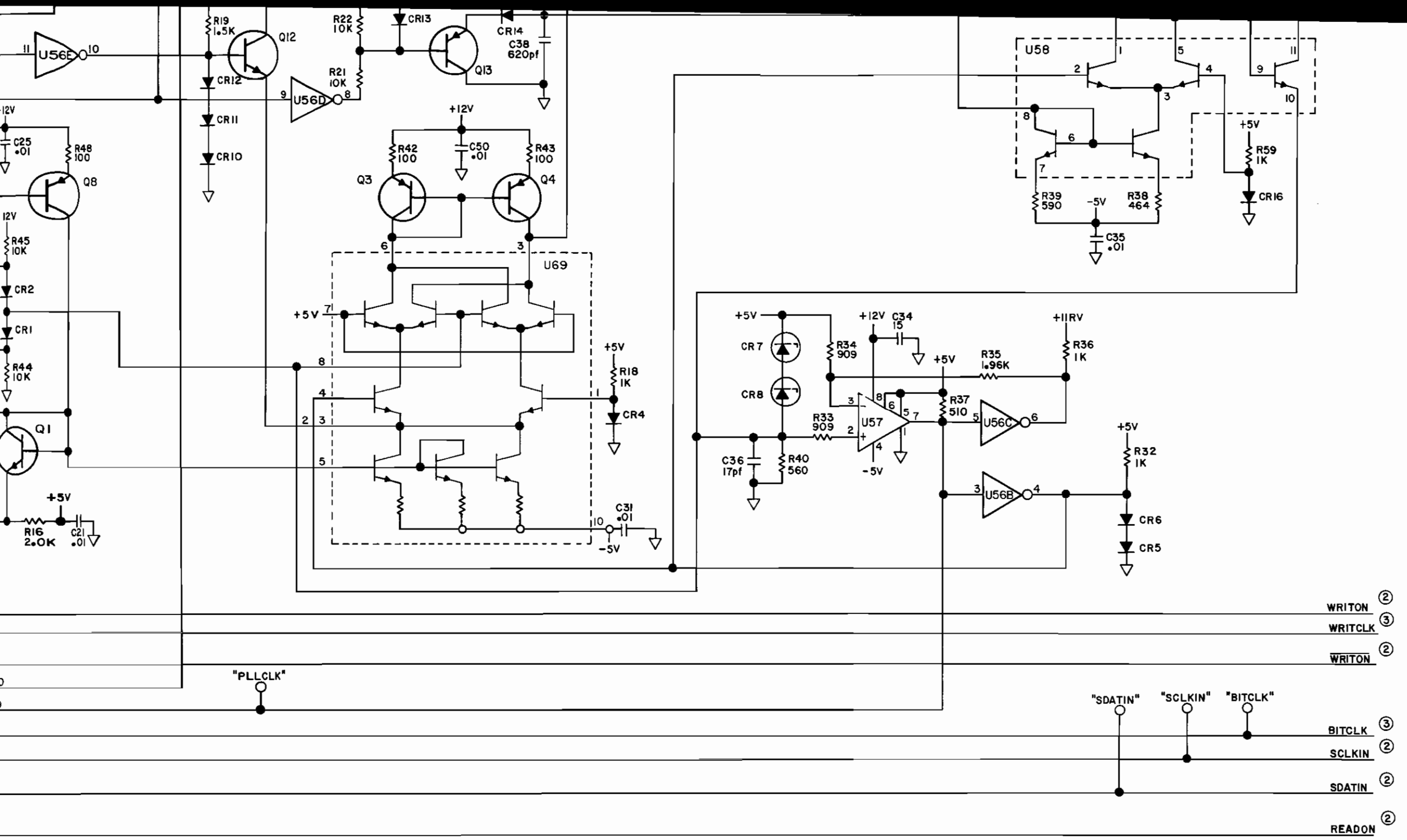
U62
U63
U43
U75B
U42A
U42B
U73B
U28
U27C
U27B
U27F
U16
U2B
U2A
U1D
U1B
U3A
U2D
U18B
U51D
U56E
R4-6 4.7K
R4-7 4.7K
R9-4 4.7K
R3-2 4.7K
R3-4 4.7K
R3-5 4.7K
R2 422
+5V
NC



09895-J-75019 1of4

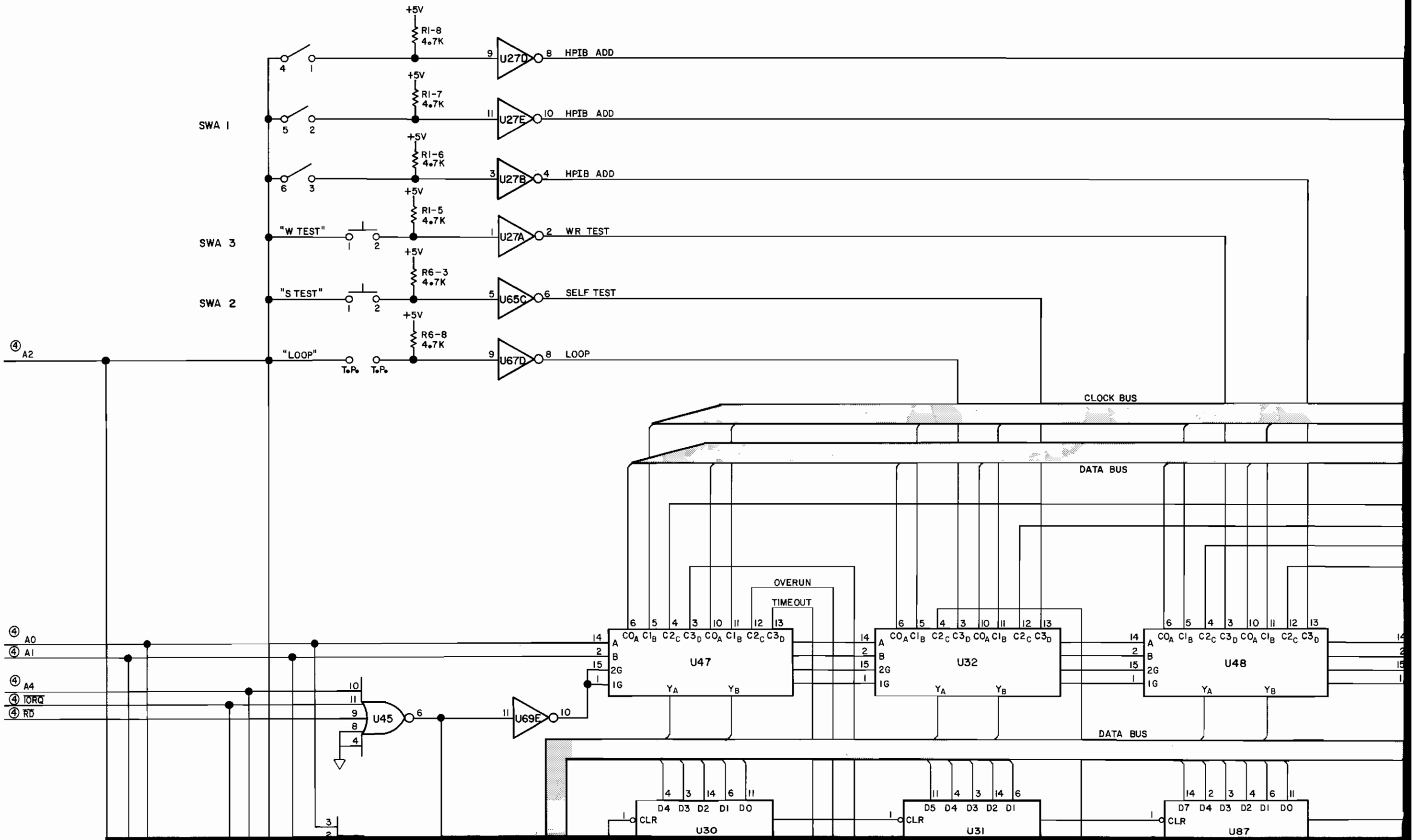
ORG.

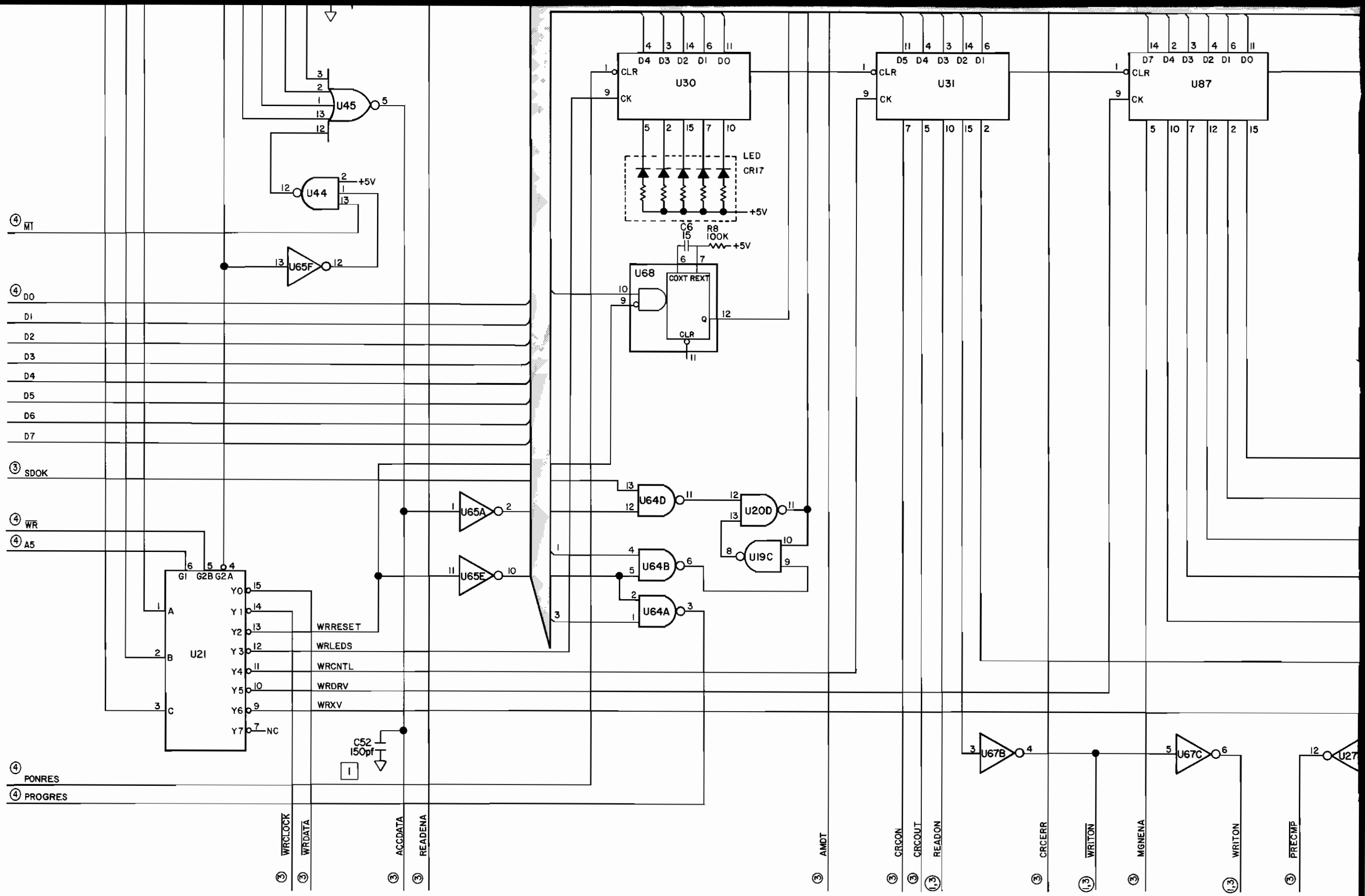

8MHZ
HIDEN
HIDEN
LCKUP
RDATA
XMGN
+12V
+5V
+11V
U58
U56A
U56B
U56E
U56F
U50A
U42B
U18B
Q12
Q13
Q14
Q15
Q9
Q10
Q11
CR12
CR13
CR14
CR15
R19 1.5K
R21 10K
R22 10K
R23 1.62K
R24 3.83K
R25 1.50K
R50 1.50K
R51 3.01K
R52 10K
R53 5.11K
R54 750
R55 162K
R56 196K
R57 287
C26 .01
C27 .015
C29 510pf
C37 820pf
C38 620pf
C39 .01

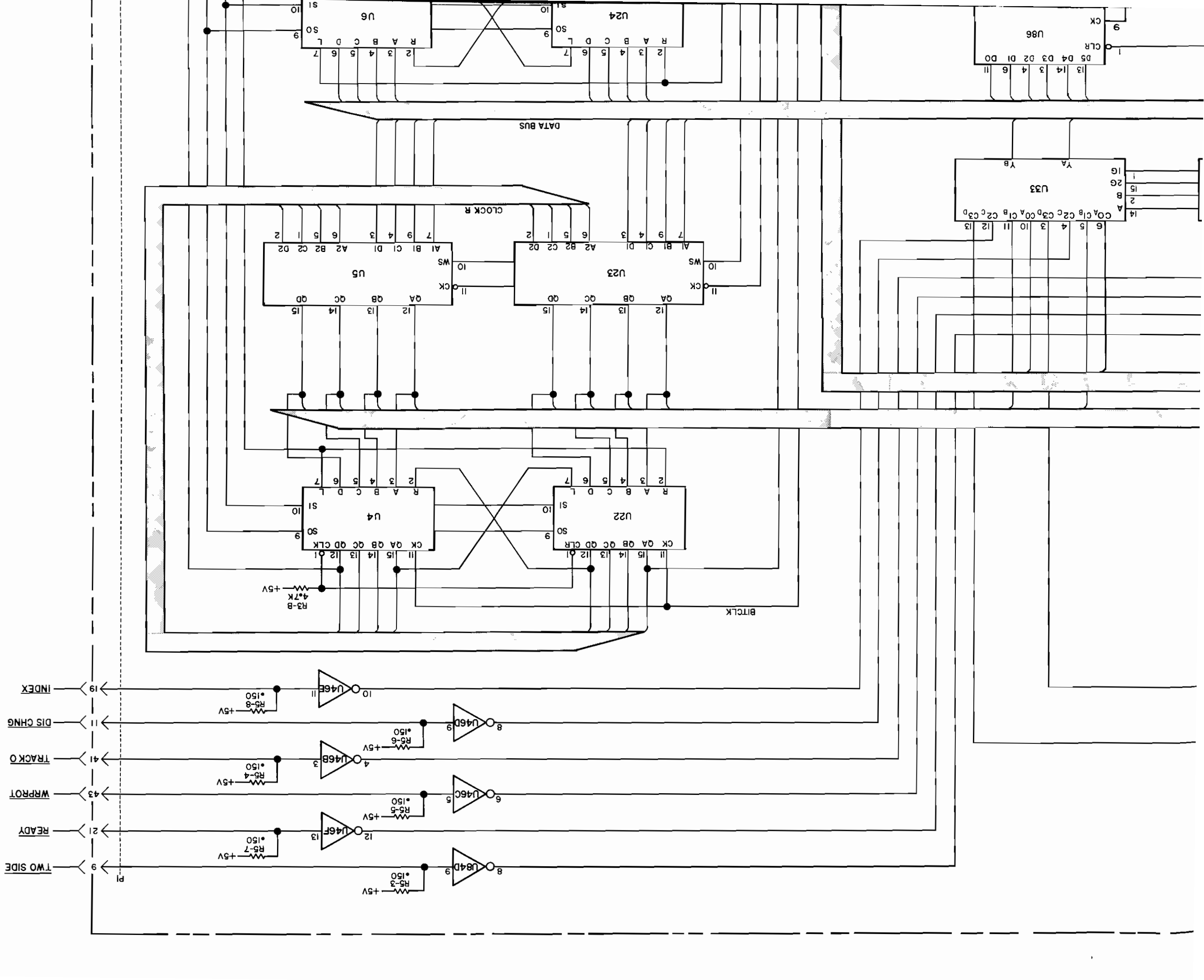

U56E
R19 1.5K
Q12
CR12
CR11
CR10
U56D
R22 10K
R21 10K
CR13
CR14
C38 620pf
Q13
+12V
C25 .01
R48 100
Q8
R45 10K
CR2
CR1
R44 10K
Q1
+5V
R16 2.0K
C21 .01
R42 100
C50 .01
R43 100
Q3
Q4
U69
+5V
R18 1K
CR4
C31 .01
-5V
U58
R39 590
-5V
R38 464
C35 .01
+5V
R59 1K
CR16
CR7
CR8
C36 17pf
R40 560
R33 909
U57
R34 909
+12V
C34 15
+5V
R35 1.96K
+11RV
R36 1K
R37 510
U56C
U56B
+5V
R32 1K
CR6
CR5
WRITON
WRITCLK
WRITON
"PLLCLK"
"SDATIN"
"SCLKIN"
"BITCLK"
BITCLK
SCLKIN
SDATIN
READON

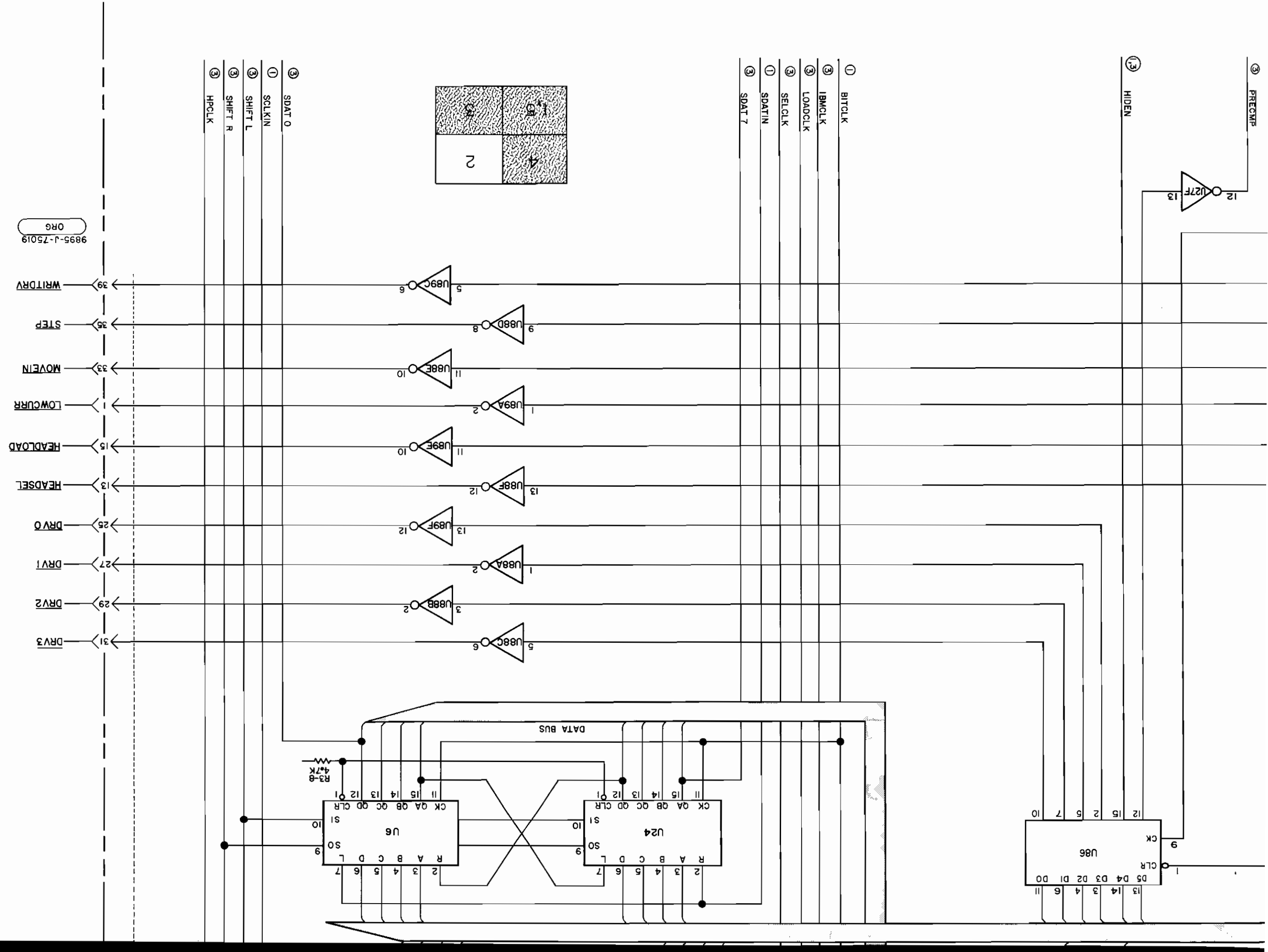
NOTES:

[1] C52 ADDED AT DATE CODE 2039




U45
U44
+5V
U65F
④ MT
④ D0
D1
D2
D3
D4
D5
D6
D7
③ SDOK
④ WR
④ A5
U21
G1 G2B G2A
A
B
C
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
NC
WRRESET
WRLEDS
WRCNTL
WRDRV
WRXV
C52
150pf
④ PONRES
④ PROGRES
U65A
U65E
U30
U31
U87
D4 D3 D2 D1 D0
D5 D4 D3 D2 D1
D7 D4 D3 D2 D1 D0
CLR
CK
LED
CR17
C6
15
R8
100K
U68
COXT REXT
Q
U64D
U64B
U64A
U20D
U19C
U67B
U67C
WRCLOCK
WRDATA
ACGDATA
READENA
AMDT
CRCON
CRCOUT
READON
CRCERR
WRITON
MGNENA
WRITON
PRECMP


DATA BUS
CLOCK R
BITCLK
U86
U24
U6
U33
U23
U5
U22
U4
U46B
U46D
U46B
U46C
U46F
UB4D
R3-B
4.7K
+5V
R5-8
R5-6
R5-4
R5-5
R5-7
R5-3
.150
INDEX
DIS CHNG
TRACK O
WRPROT
READY
TWO SIDE
P1


9895-J-75019
ORG
PRECMP
HIDEN
BITCLK
IBMCLK
LOADCLK
SELCLK
SDATIN
SDAT 7
SDAT 0
SCLKIN
SHIFT L
SHIFT R
HPCLK
WRITDRV
STEP
MOVEIN
LOWCURR
HEADLOAD
HEADSEL
DRV0
DRV1
DRV2
DRV3
U27F
U89C
U89D
U88E
U89A
U89E
U88F
U89F
U88A
U88B
U88C
U86
U6
U24
DATA BUS
R3-8
4.7K

A4

220
240
100
120

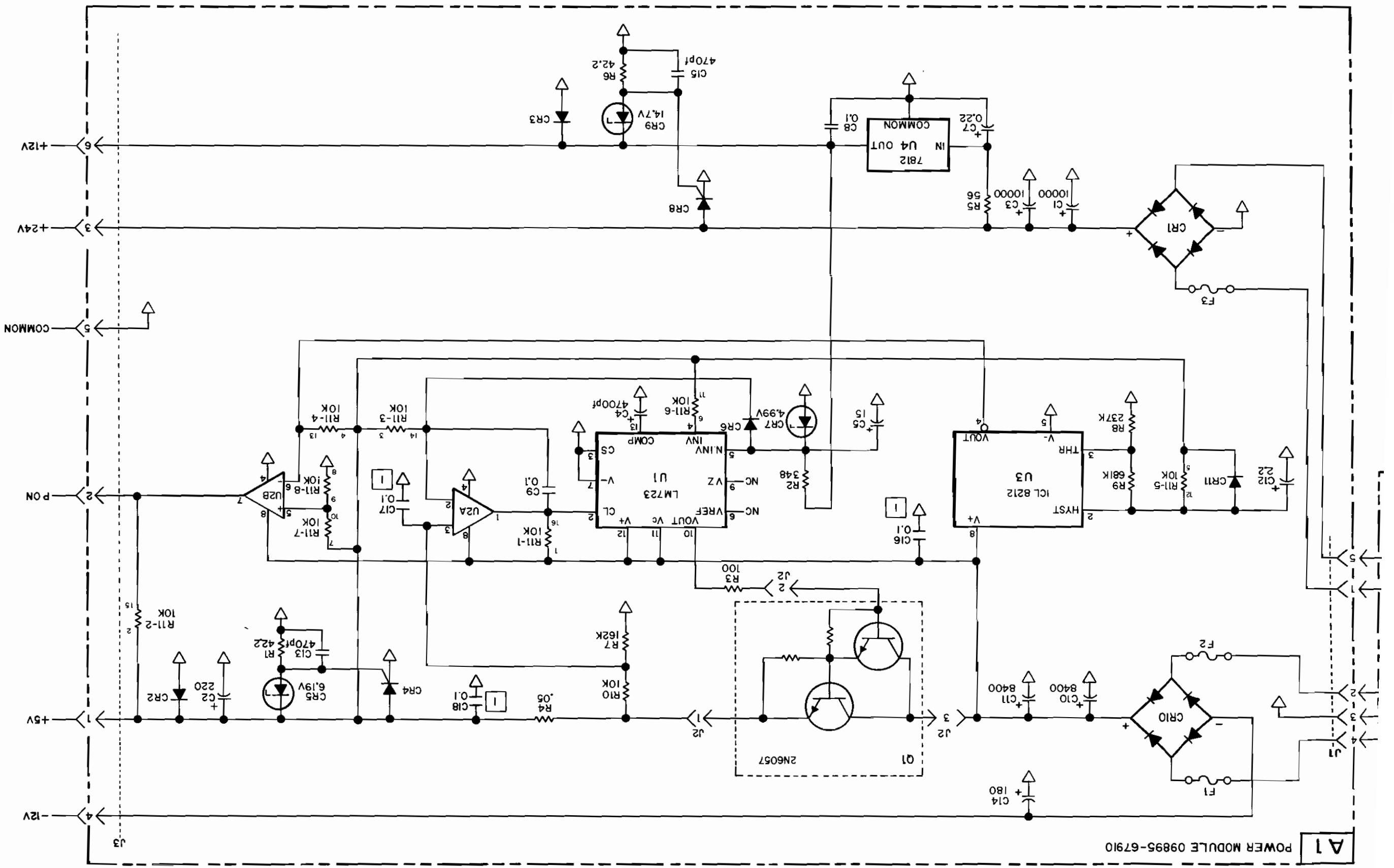
T1
J1
F1
S1
S2
S3
P/O T1
FL1
M1
M2
FAN

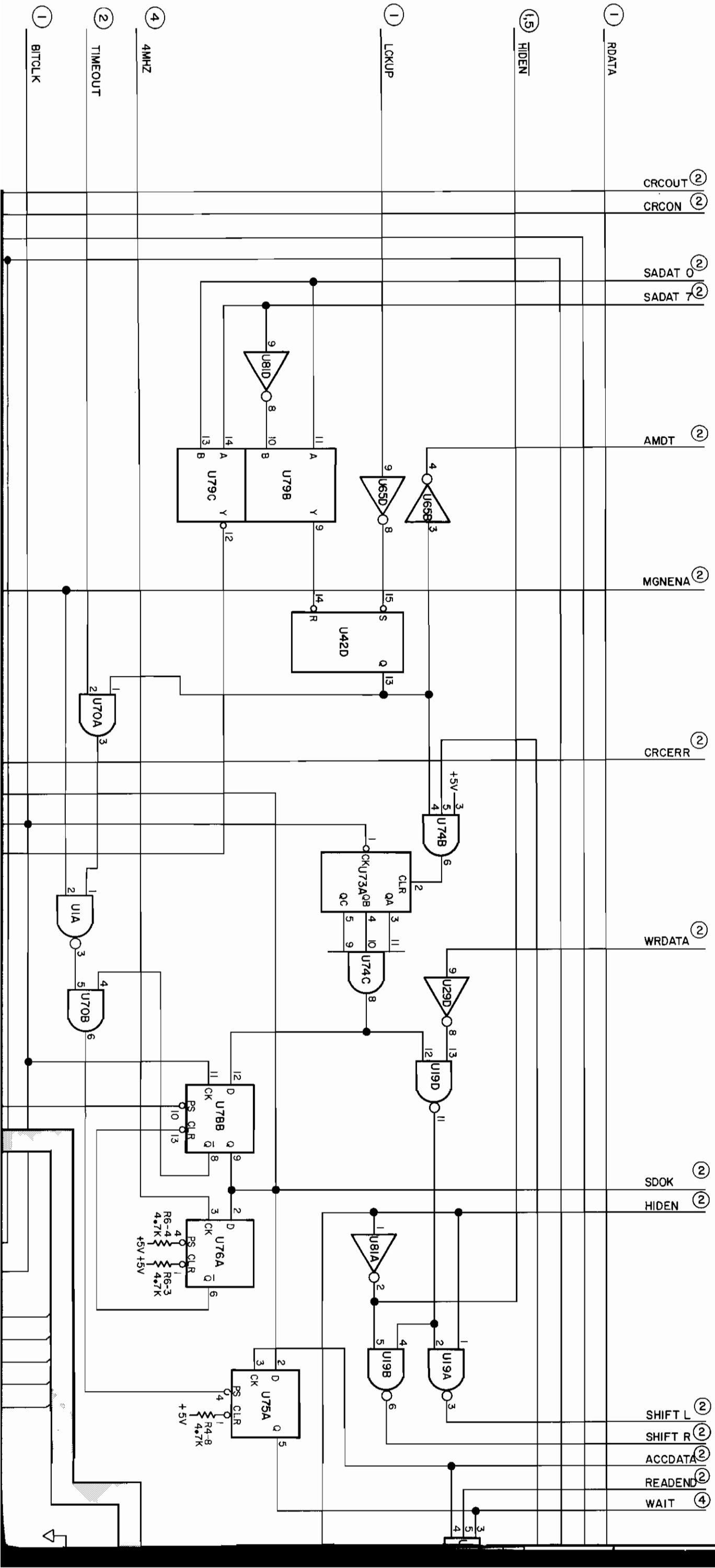
NOTES:

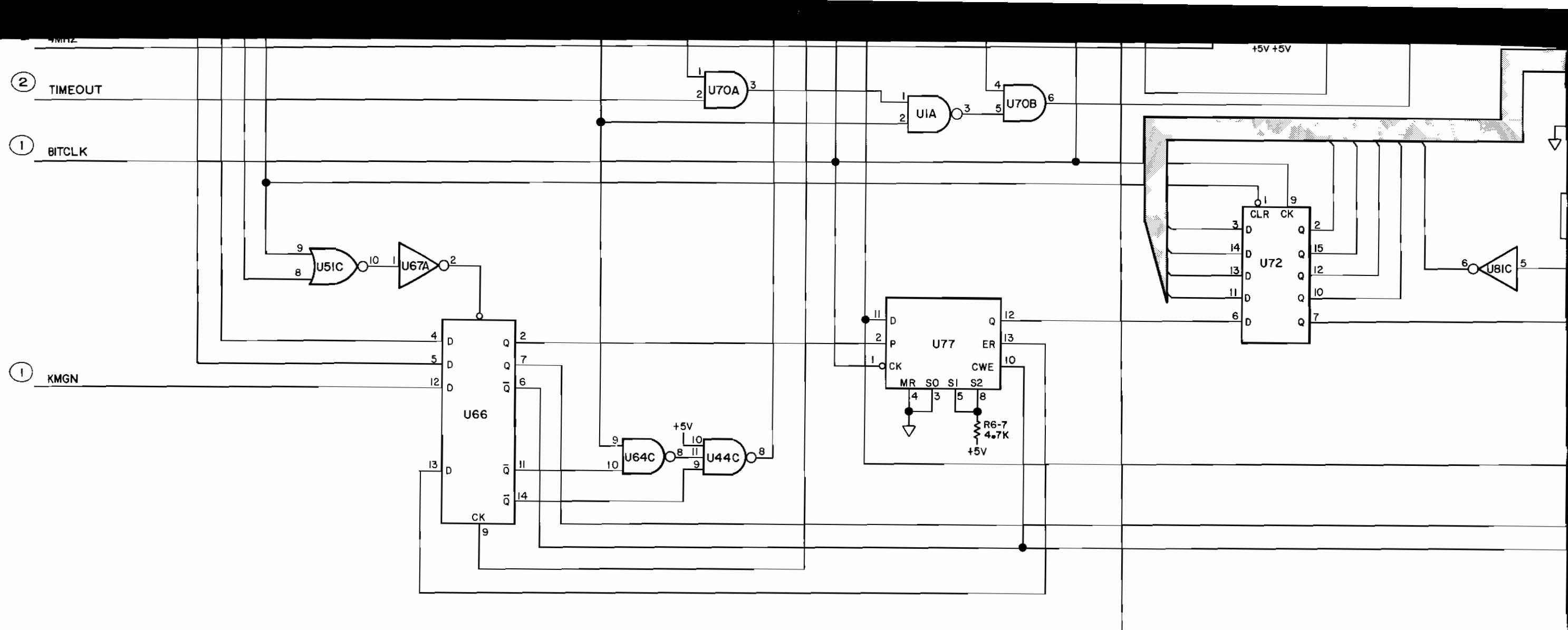
[1] C16, C17, C18 EFFECTIVE ON REV. B BOARDS

A1 POWER MODULE 09895-67910

F1
F2
CR10
C14 180
C10 8400
C11 8400
Q1 2N6057
J2
R10 10K
R4 .05
C18 0.1
R7 162K
R3 100
C16 0.1
R11-1 10K
C17 0.1
C9 0.1
U2A
R11-3 10K
C12 2.2
CR11
R11-5 10K
R9 681K
R8 237K
ICL 8212 U3
HYST
THR
V+
V-
VOUT
R2 348
C5 15
CR7 4.99V
CR6
R11-6 10K
C4 4700pf
LM723 U1
VOUT
Vc
V+
VREF
VZ
N.INV
INV
COMP
CL
CS
F3
CR1
C1 10000
C3 10000
R5 56
7812 U4
IN
OUT
COMMON
C7 0.22
C8 0.1
CR8
CR9 14.7V
CR3
C15 470pf
R6 42.2


A1
POWER MODULE 09895-67910
+12V
+24V
COMMON
P ON
-12V
+5V
J3
J1
J2
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
F1
F2
F3
U1
LM723
U2A
U2B
U3
ICL 8212
U4
7812
Q1
2N6057
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11-1
R11-2
R11-3
R11-4
R11-5
R11-6
R11-7
R11-8


BITCLK
TIMEOUT
4MHZ
LCKUP
HIDEN
RDATA
CRCOUT
CRCON
SADAT 0
SADAT 7
AMDT
MGNENA
CRCERR
WRDATA
SDOK
HIDEN
SHIFT L
SHIFT R
ACCDATA
READEND
WAIT
U79C
U79B
U65D
U65B
U42D
U70A
U74B
U1A
U73A
U74C
U70B
U29D
U19D
U78B
U81A
U19B
U19A
U76A
U75A
R6-4 4.7K
R6-3 4.7K
R4-8 4.7K
+5V

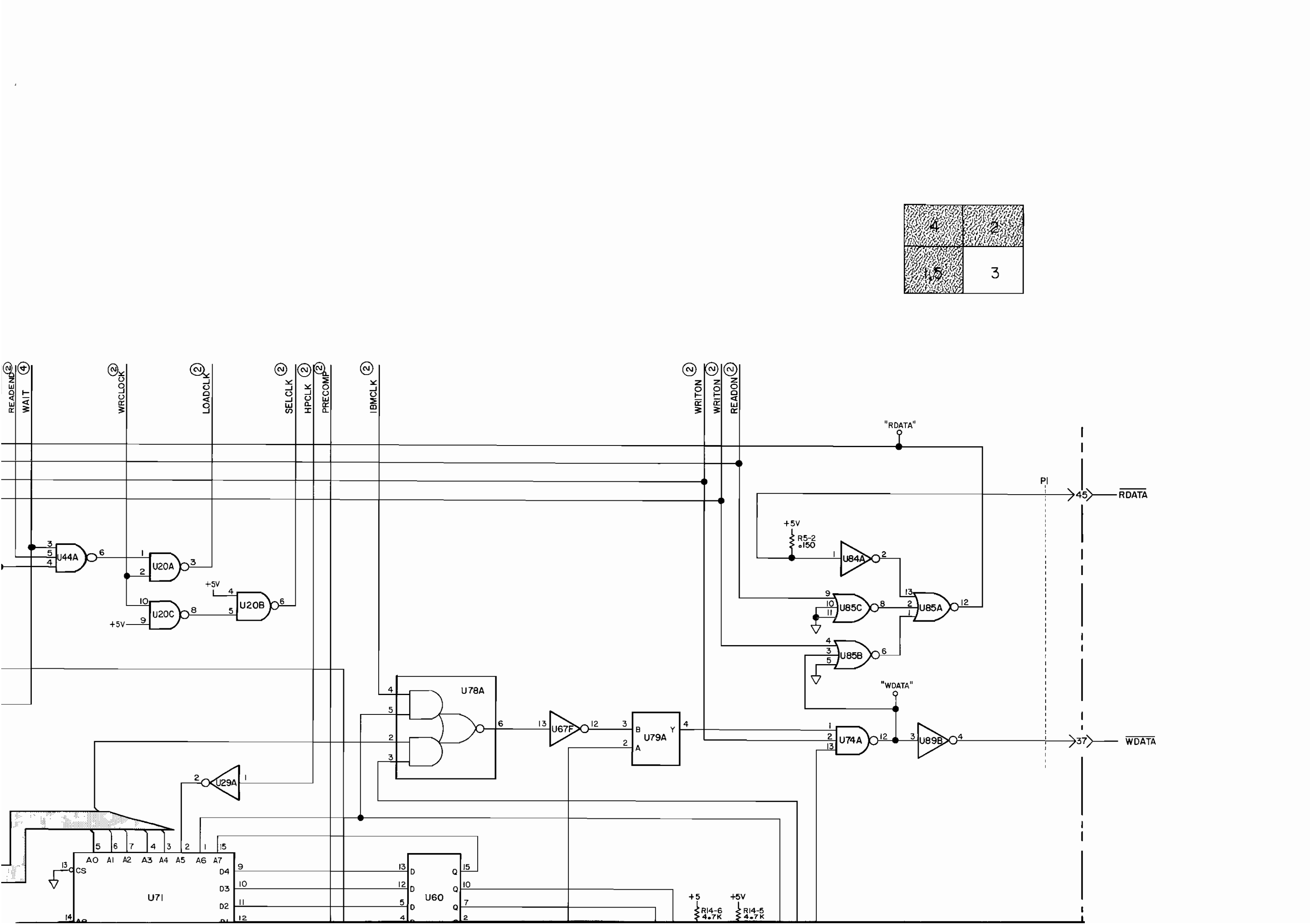


4 B or 4

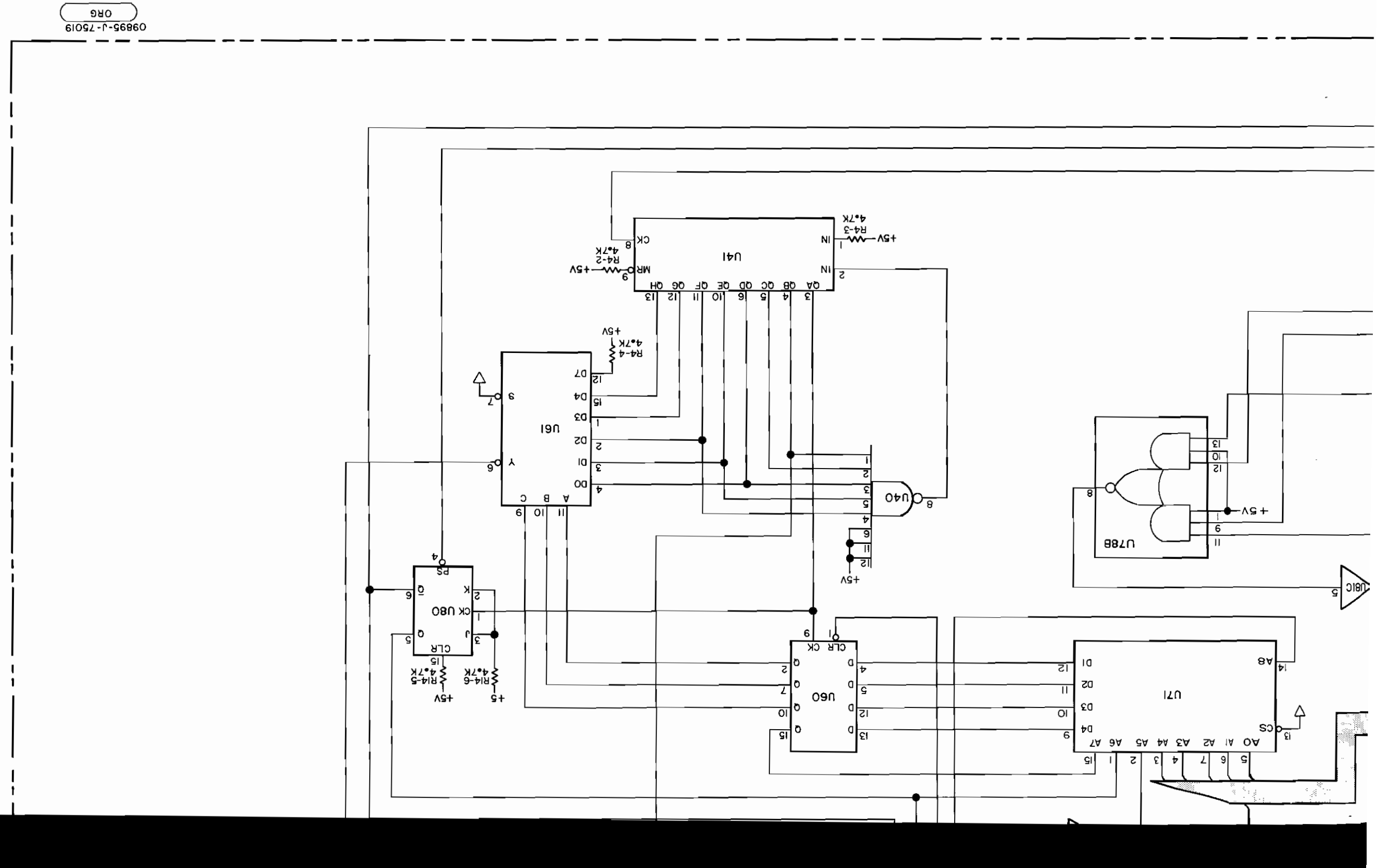
4 PONRES

1 WRTCLK

09895-66500 SHEET#3


4
2
15
3
READEND
WAIT
WRCLOCK
LOADCLK
SELCLK
HPCLK
PRECOMP
IBMCLK
WRITON
WRITON
READON
"RDATA"
P1
45
RDATA
+5V
R5-2
.150
U84A
U85C
U85A
U85B
U44A
U20A
U20C
U20B
"WDATA"
U74A
U89B
37
WDATA
U78A
U67F
U79A
U29A
U71
U60
A0 A1 A2 A3 A4 A5 A6 A7
CS
D4
D3
D2
D
Q
+5
+5V
R14-6
4.7K
R14-5
4.7K

09B95-J-75019
ORG



09895-66506 FLEXIBLE DISC CONTROLLER SELF TEST MONITOR

+5V
C1-C6
.01

J1

D7 41
D6 42
D5 43
D4 44
D3 45
D2 46
D1 47
D0 48

2
11
31
32
33
34
GND 35
36
37
38
39
40
49

RESET 3

A0 15
A1 16
A5 20
A2 17
WR 8
IORQ 10

U6

3 D
4 D
7 D
8 D
13 D
14 D
17 D
18 D
CLR 1
CLK 11

Q 2
Q 5
Q 6
Q 9
Q 12
Q 15
Q 16
Q 19

U9

3 D
4 D
7 D
8 D
13 D
14 D
17 D
18 D
CLR 1
CLK 11

Q 2
Q 5
Q 6
Q 9
Q 12
Q 15
Q 16
Q 19

U14D 9 8

U16B 11 10 9 8

U17B 4 11 10 9 8

6 11 U15E 10

U15A 1 2

U17A 12 13 1 2 3

5 9 U15D 8

6 U15C 5

13 U15F 12

13 11 9 13 11 1 9 5 5 3

14 11 1 15 2 6 5 7 4 3 10 12 13

+5V

U16A

U16C

U15C

U15B

U13A

U13F

U13E

U13D

U13B

CR15 R9-4 "ERROR"

CR14 R9-8 "HEAD"

CR13 R9-7 "UNIT"

CR12 R9-6

CR11 R9-5 "HPFMT"

U11F

U11E

U12D

U12F

U12E

U12A

U11D

U13C

U12C

U12B

CR6 R8-6

CR5 R8-5

CR4 R8-4

CR3 R8-3

CR2 R8-2

CR10 R9-3

CR9 R9-2 "TEST"

CR8 R8-8

CR7 R8-7

CR1 R7 "DONE"

"SUB TEST"

U8

U7

Reset

LE

CLK

D C B A

a b c d e f g

R5 R1 R5 R5 R1 R5 R6

U10

"UNIT 0 ERROR"

U4

Reset

LE

CLK

D C

a b c d e f g

R1 R1 R2 R2 R2 R2 R3

U2

1990-0558

"UNIT 1 ERROR"

U5

R3 R4 R3 R4 R3 R4 R4

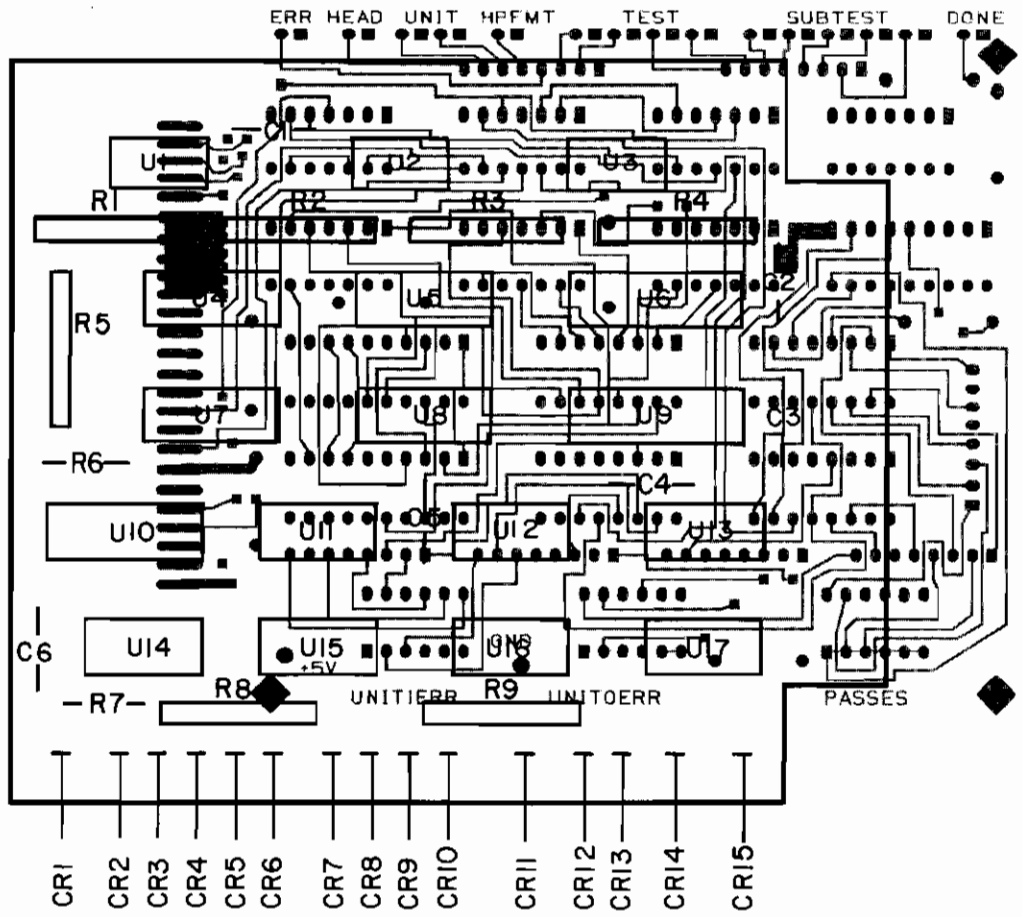
U3

1990-0558

"PASSES"

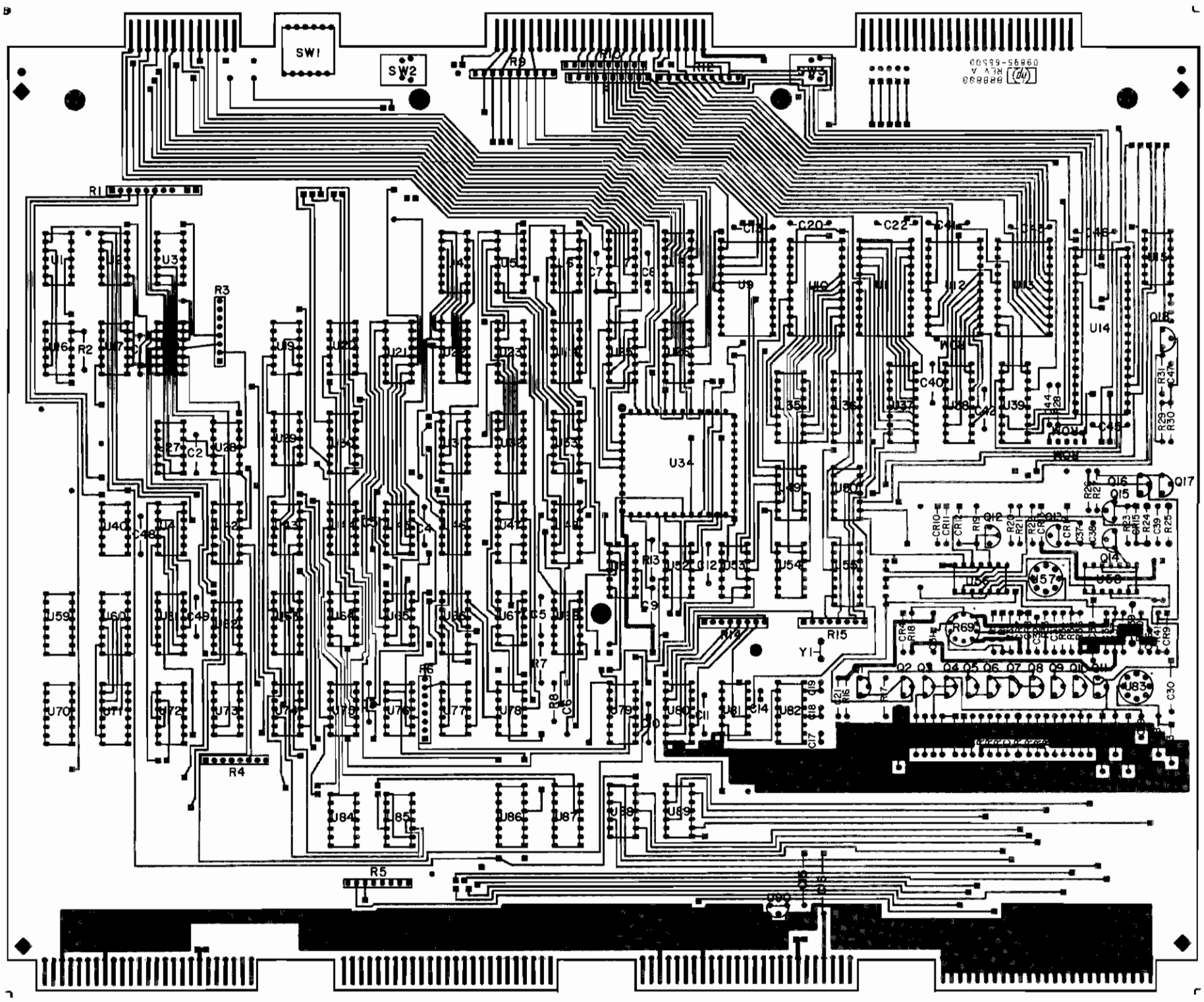
U1

1990-0558



COMPONENT SIDE

Status Display Board

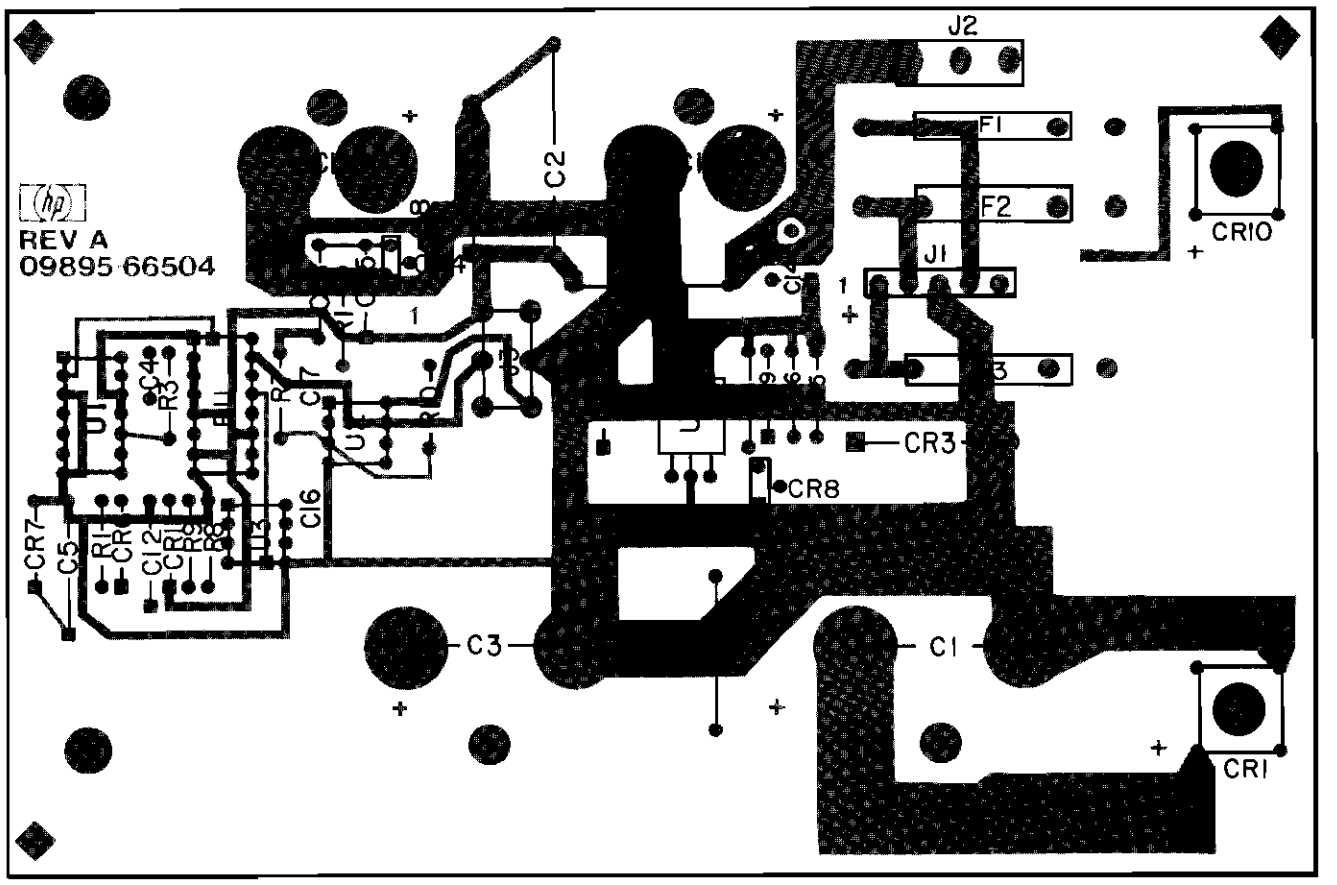


1	$\overline{RD}$
3	$\overline{RES}$
5	$\overline{INT}$
7	$\overline{RFS}$
9	$\overline{WA}$
11	GND
13	$\overline{HAL}$
15	AO
17	A2
19	A4
21	A6
23	A8
25	AIO
27	AI2
29	AI4
31	GND
33	GND
35	GND
37	GND
39	GND
41	D7
43	D5
45	D3
47	DI
49	GND

COMPONENT SIDE

A0

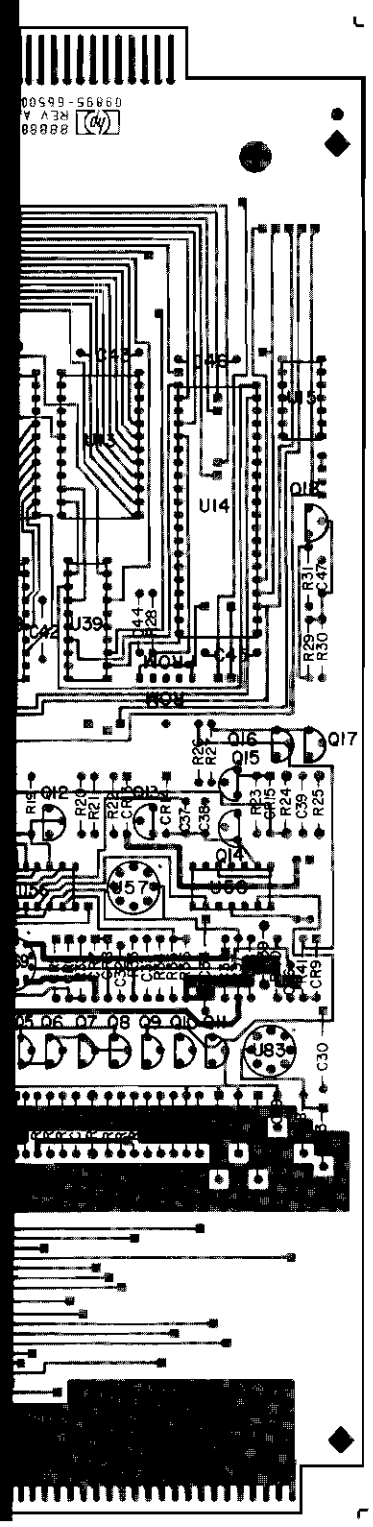
-hp- Part No. 09895-66500 Rev A



COMPONENT SIDE

A4

-hp- Part No. 09895-66504 Rev A



Controller Board Edge Connector Pin Assignments

J2 CONNECTOR
Z80 PROCESSOR
BUS

1	$\overline{RD}$	2	GND
3	$\overline{RESET}$	4	$\overline{MI}$
5	$\overline{INT}$	6	$\overline{NMI}$
7	$\overline{RFSH}$	8	$\overline{WR}$
9	$\overline{WAIT}$	10	$\overline{IORQ}$
11	GND	12	$\overline{MREQ}$
13	$\overline{HALT}$	14	GND
15	A0	16	A1
17	A2	18	A3
19	A4	20	A5
21	A6	22	A7
23	A8	24	A9
25	A10	26	A11
27	A12	28	A13
29	A14	30	A15
31	GND	32	GND
33	GND	34	GND
35	GND	36	GND
37	GND	38	GND
39	GND	40	GND
41	D7	42	D6
43	D5	44	D4
45	D3	46	D2
47	D1	48	D0
49	GND	50	4MHZ

P1 CONNECTOR
CONTROLLER TO
DRIVE BUS

1	LOW CURR
3	N.C.
5	N.C.
7	N.C.
9	TWO-SIDE
11	DISC CHNG
13	HEAD SEL
15	HEAD LOAD
17	N.C.
19	INDEX
21	READY
23	N.C.
25	DRV 0
27	DRV 1
29	DRV 2
31	DRV 3
33	MOVE IN
35	STEP
37	WDATA
39	WRITDRV
41	TRACK 0
43	WRPROT
45	RDATA
47	N.C.
49	N.C.

2-50 EVEN
GND

J3 CONNECTOR
HPIB BUS

1	N.C.	2	N.C.
3	GND	4	N.C.
5	GND	6	ATN
7	GND	8	SRQ
9	GND	10	IFC
11	GND	12	NDAC
13	GND	14	NRFD
15	GND	16	DAV
17	REN	18	EOI
19	DIO8	20	DIO4
21	DIO7	22	DIO3
23	DIO6	24	DIO2
25	DIO5	26	DIO1

P2 AND P4 POWER
CONNECTORS

1	+5V	2	+5V
3	+5V	4	+5V
7	-12V	8	-12
13	+12V	14	+12
35	POP	36	GND
45	GND	46	GND

ALL OTHER CONNECTORS N.C.
P2-35 IS N.C.