dup in A11

HP 98705 Graphics Processor Hardware Support Manual

HP 9000 Series 300/400/700 Computers

HEWLETT PACKARD

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February 1991 ... First edition

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Warnings, cautions, and notes are used throughout this manual to alert the user to conditions of importance. They are used as follows.

- Warnings contain operating procedures, practices, etc., that if not observed, could result in injury to personnel or loss of life.
- Cautions contain operating procedures, practices, etc., that if not observed, could result in damage to or destruction of equipment.
- Notes contain operating procedures, practices, etc., that will assist the user in accomplishing the job.

Examples:

Warning	**Turn the equipment OFF and disconnect power cords before removing covers.**

Caution	Printed circuit boards are susceptible to damage from electro-static discharge (ESD). Use approved ESD procedures when handling printed circuit boards. Use an Anti-static Workstation.

Note	Hewlett-Packard supports repair of this product only to the assembly level. The fault is diagnosed to the assembly causing the fault. That assembly is then replaced with a new or rebuilt assembly.

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取扱説明書に従って正しい取り扱いをして下さい。

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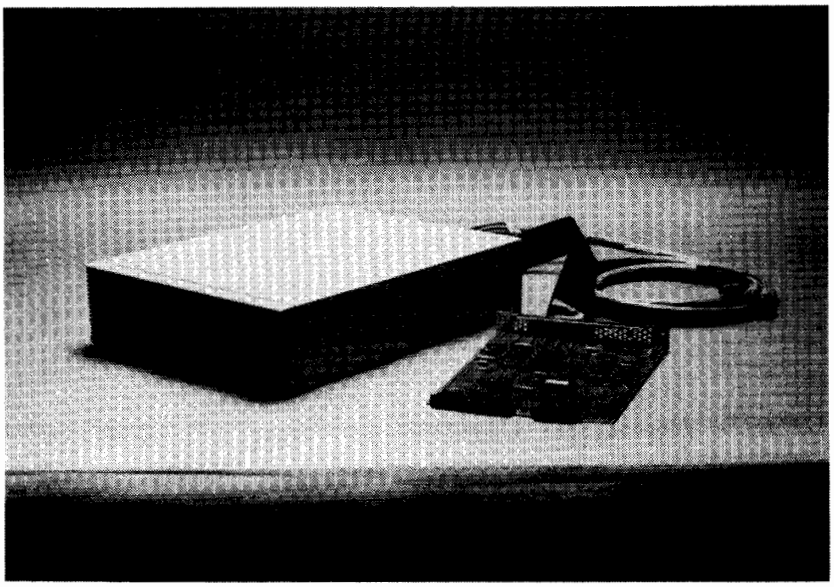


Figure 1-1. HP 98705 Graphics Processor

Introduction

The HP 98705A/B/C Graphics Processors are 3-D solids graphics peripherals for both wire-frame and solids design.

The HP 98705A Graphics Processor consists of:

- A transform engine.
- A scan converter.
- A frame buffer memory of eight planes.
- An 8-bit color map (maps 8-bits into 24-bits).

The HP 98705B has an additional eight planes of frame buffer memory (for double buffering) and a 16-bit Z buffer.

The HP 98705C is the same as the HP 98705A except for a slower transform engine.

The Graphics Processor uses an SGC Graphics Interface Card when used with Series 700 computer, and an HP 98702A DIO II/GAD Interface Card with Series 300 or 400 computers.

A Graphics Address and Data bus (GAD) cable is used to connect either interface to the computer.

The Graphics Processor provides red, green, blue (RGB) output for a 1280 by 1024 high resolution color monitor such as the HP 98754A 19 inch monitor.

Service Support

Hewlett-Packard provides only On-site Repair for the Graphics Processor. A Hewlett-Packard Field Service Engineer will troubleshoot and repair the product, on the customer's site, to the field replaceable unit.

2

Site Preparation and Technical Specifications

Site Preparation

Refer to the *HP 9000 Series 200/300/500 Site Preparation Manual* to assist you in preparing for the installation of the HP 98705A/B/C Graphics Processor.

Wiring

Verify electrical power receptacle wiring and contact retention force for all electrical receptacles supplying power to system devices. If wiring is not correct and safe, do not install equipment until corrected.

Technical Specifications

Power Requirements

Power Line Frequency		47 through 66 Hz
Switch Selected Line Voltage	115	90 through 132 Vac
	230	180 through 240 Vac
Fuse	Non customer replaceable	6 A/250 V
Line Current	90 through 132 Vac	4 Amps
	180 through 240 Vac	2 Amps
Power Consumption		260 Watts maximum
Heat Dissipation		207 kcal/hr (822 BTU/hr)

Environmental

Operating Temperature	0°C to 55°C ambient temperature to 7500 ft.
	0°C to 47°C ambient temperature to 15,000 ft.
Storage Temperature	−40°C to 71°C ambient temperature.
Relative Humidity	Operating—5% to 95% at 40°C ambient temperature.
	Storage—90% at 65°C ambient temperature.
Maximum Operating Altitude	15,000 ft.
Non-operating Altitude	50,000 ft.

Physical

Height	100 mm (3.9 inches).
Width	325 mm (12.8 inches).
Depth	445 mm (17.5 inches).
Weight	8.6 kg (20 lbs).

Regulatory

Canada	CSA 22.2 #220; IEC 950 (EN-60950).
Germany	VDE 0871/6.78 Level B.
Japan	VCCI.
United States of America	FCC A; UL 1950.

3

Installation and Configuration

Introduction

This chapter shows the installation procedure in a picture guide format. This is the same as the *HP 98705A, B, or C Installation* picture guide that is shipped with each product. The picture guide also explains how to turn the system ON and verify that it is working properly.

The picture guide shipped with the product does not have this front page information.

The HP 98705 Graphics Processor has three supported models. Installation is the same for all three models. The three models and their configuration are:

Model HP 98705A:

Transform and Scan Converter	98705-66573
8 Plane Frame Buffer (FB0)	98705-66570
Color Map	98705-66574

Model HP 98705B:

Transform and Scan Converter	98705-66573
16 Plane Frame Buffer (FB0 & FB1)	98705-66571
Color Map	98705-66574
16 Plane Z Buffer	98705-66572

Model HP 98705C:

Transform and Scan Converter	98705-66575
8 Plane Frame Buffer (FB0)	98705-66570
Color Map	98705-66574

Either an SGC or a DIO-II interface card is provided with the Graphics Processor, depending upon which SPU is being used.

Installation

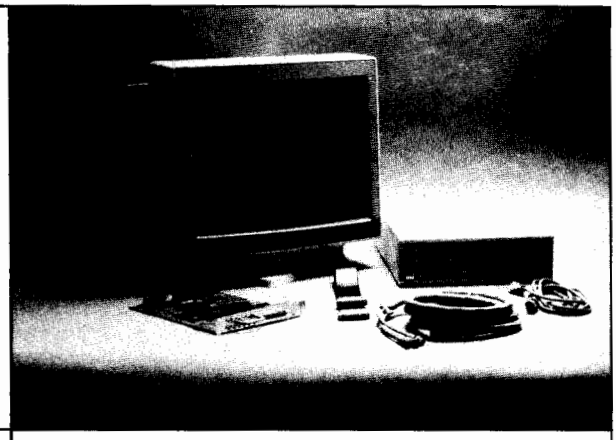
The following picture guide explains how to install the:

- SGC Interface Card (SGC to Graphics Processor for Series 700 SPU's) (98705-66582).
- HP 98702A Interface Card (DIO-II to Graphics Processor for Series 300/400 SPU's).
- HP 98705A, B, or C Graphics Processor.
- HP 98754A Color monitor.

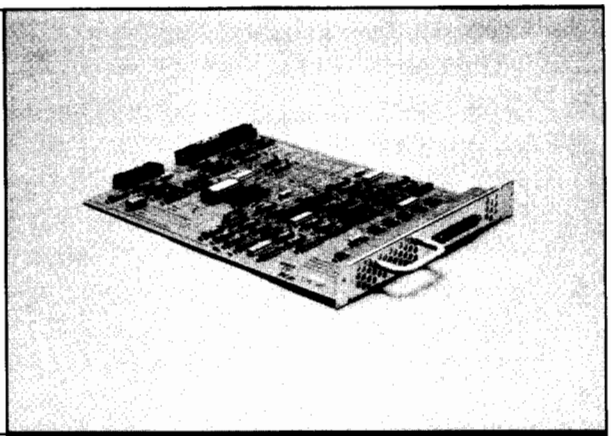
Some pictures show a Series 300 SPU while others show a Series 400; the Series 700 SPU's are not shown, but are similar to the Series 400's.

Caution Electronic components and assemblies can be damaged by static discharge. Do not touch the traces or connector contacts. Leave the interface card in its protective, anti-static container until required for installation.

When installing, removing, or handling printed circuit assemblies, use an anti-static workstation, HP part number 9300-0933.

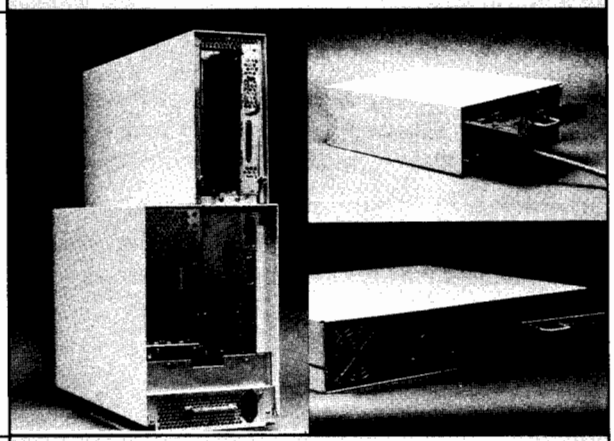
1 Unpack and inventory your HP 98705 Graphics Processor. Note: The monitor is included in the installation process but is not a part of the Graphics Processor product.	
2 Check with your system administrator, or refer to the appropriate computer documentation for the procedure, and turn-off your computer.	

3 Find the SGC Interface Card or the HP 98702A DIO-II Interface Card. **Caution** the SGC and DIO-II cards look alike. Check the silkscreen lettering on the metal cover plate for the correct card. The SGC interface (for Series 700) has the number "98705-66582" near the cable connector, while the DIO-II interface (for Series 300/400) has "98702A" near the HP logo. Also, the SGC card has no configuration switches, while the DIO-II card has a set near the connector.

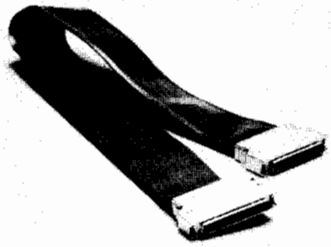


4 Install card into appropriate slot in your computer. Refer to computer's documentation to get inside (or call the nearest HP Sales and Service Center for information).

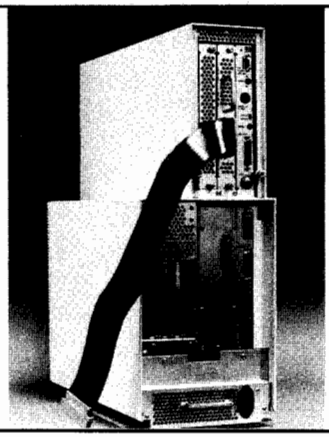
The SGC card has no configuration switches. The DIO-II card's switches have a factory setting to a default address (133-135). If you need a different address, see the section *Series 300/400 System Configuration* after Step 17.



5 Find the Graphics Address and Data (GAD) bus cable.

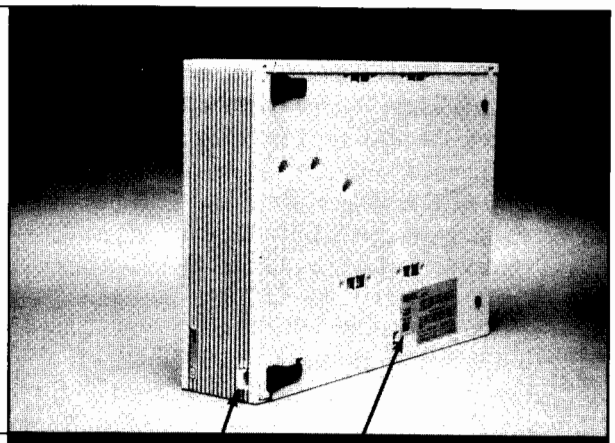


6 Connect the Graphics Address and Data cable to the interface card. Later, the other end will connect to your HP 98705.



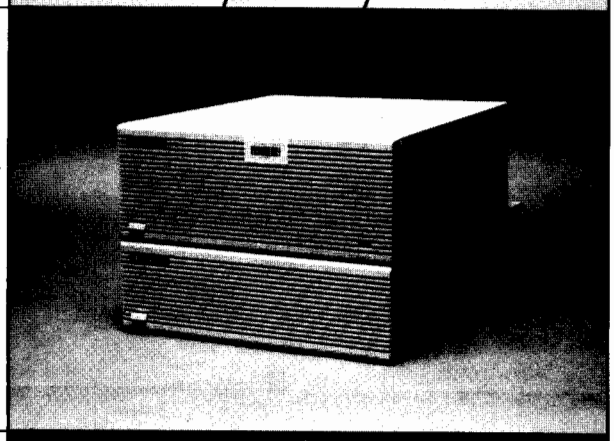
7 Check that the voltage select switch is set for your power source.

Check that the power switch is OFF.

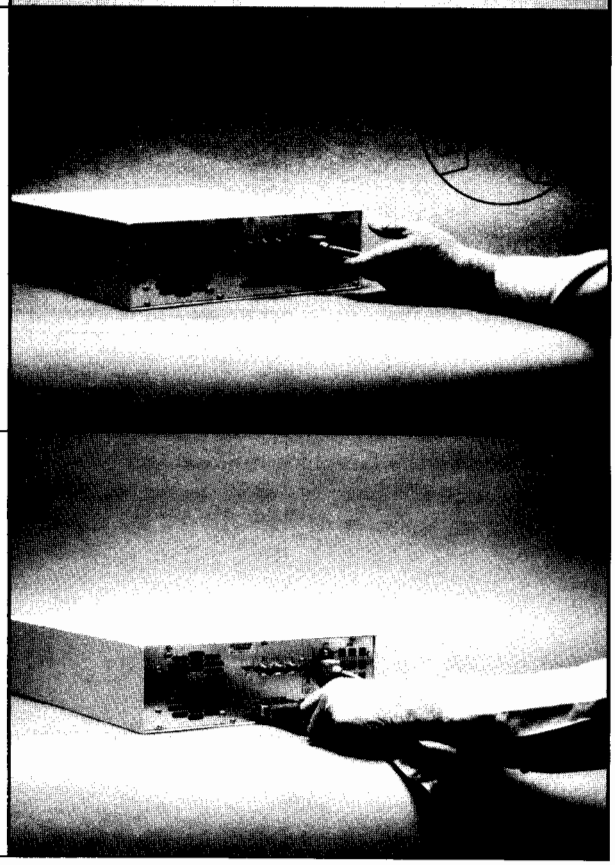


8 Place the HP 98705 near, on, or under your computer (depending on your system configuration). If the Graphics Processor will be attached to a vertically mounted SPU, refer to the instructions provided with the mounting kit.

Ensure that air flow is not restricted at the front or rear of the Graphics Processor.



9 Connect the power cord to your HP 98705 Graphics Processor. Connect the other end to a power outlet.



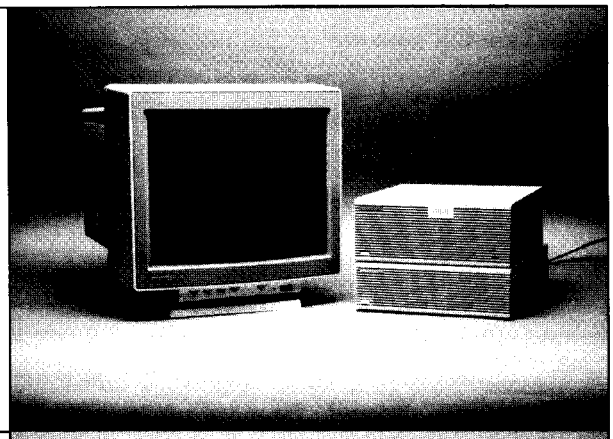
10 Ensure that power is OFF.

Connect the Graphics Address and Data cable to the GRAPHICS BUS connector on the HP 98705.

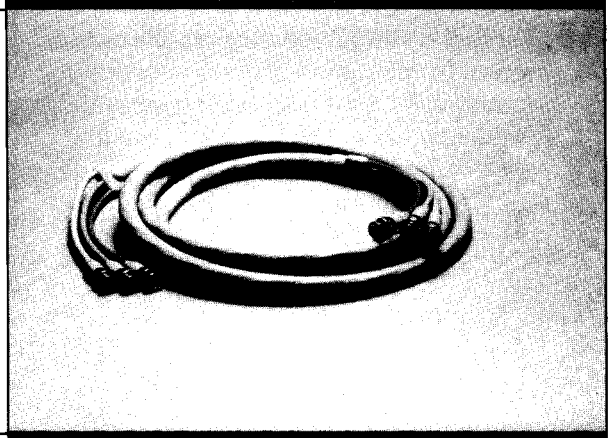
Ensure that the connector locks into position.

11 Unpack the monitor and place it near your computer.

Warning the monitor is heavy. Have someone help you when you unpack and move it.



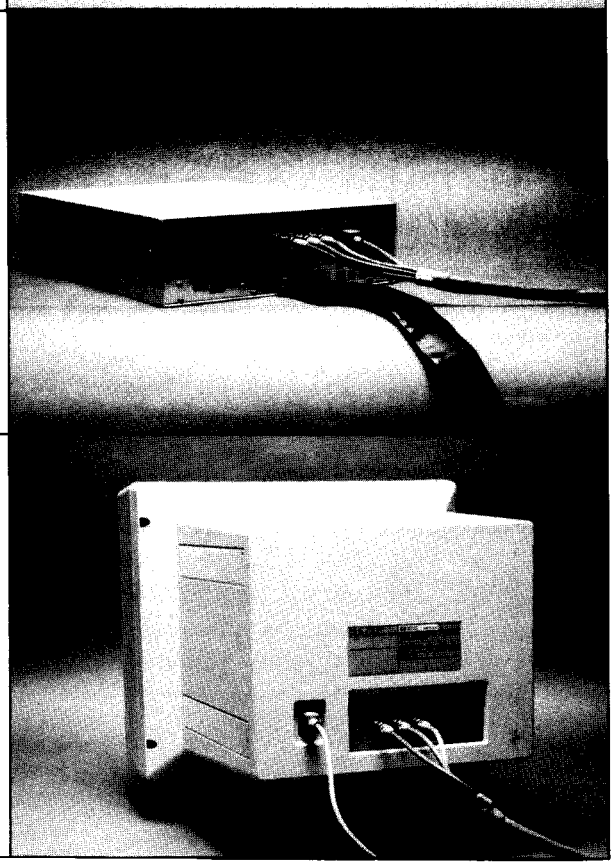
12 Find the RGB cable.



13 Connect one end of the RGB cable to your HP 98705A, B, or C; red to R, green to G, and blue to B.

In like manner, connect the other end of the RGB cable to the monitor.

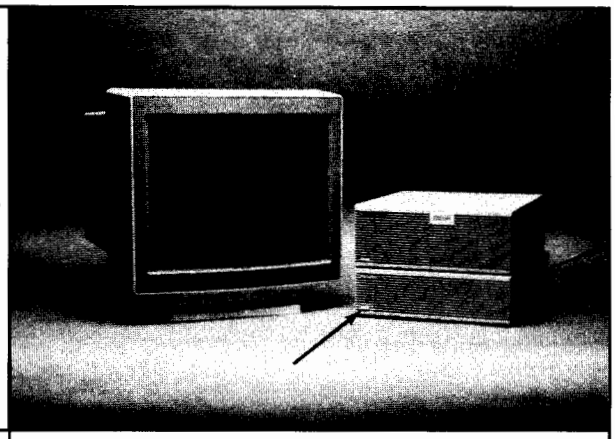
14 Connect the monitor's power cord to it. Connect the other end to a power outlet. Switch the monitor to ON.



15 Turn ON your HP 98705 Graphics Processor.

Turn ON your computer.

Refer to Step 16 if you have a Series 700 SPU, or refer to Step 17 if you have a Series 300 or 400 SPU.



16 For Series 700 SPU's, compare the console screen to this figure. If they compare (minor differences may exist), your installation is successful. If not, continue with *In Case of Trouble*.

```
Copyright 1990
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Processor Dependent Code (PDC) revision 1.0


Console path           = graphics
Keyboard path          = hil
Primary boot path      = scsi.6.0
Alternate boot path    = scsi.5.0


16 MB of memory configured and tested.
Autosearch for boot path enabled.
To override, press any key within 10 seconds.


Boot from primary boot path(Y or N)?>
```

17 For Series 300/400 SPU's,compare the console screen to this figure. If they compare, your installation is successful. If not, continue with *In Case of Trouble*.

Note: This screen is representative of a Model 375 and an HP 98705B installed as the console. Other configurations may have different screen messages.

```
Copyright 1989
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BOOTROM Rev. D
MC68030 Processor
MC68882 Coprocessor
HP-HIL Keyboard
HP-IB
DMA-CO
RAM 16776992 Bytes
HP98644 (RS-232) at 9
HP98625 (HS HP-IB) at 15
HP98643 (LAN) at 21, 080009AAAAAA
CENTRONICS at 23
Bit-Mapped Video at 253



SEARCHING FOR A SYSTEM (Press RETURN To Pause)
RESET To Power-Up
```

Note If you purchased an add on HP 98705 for use with a vertically mounted SPU, two attachment kits were included in the package. Look at the installation instructions provided with each kit and determine which should be used with your system. You can discard the other attachment kit.

In Case of Trouble

If you have problems installing or turning-on your system:

1. Switch the system to OFF.
2. Check the seating of your interface board.
3. Check all cable connections.
4. Check for select code conflicts with other I/O cards if you have a Series 300/400 SPU (DIO-II interface); see *Series 300/400 System Configuration.*
5. Turn ON the system and recheck step 16 if you have a Series 700 SPU, or check step 17 if you have a Series 300 or 400 SPU.

If you still have problems, contact your Hewlett-Packard Sales and Service Office for assistance.

Series 700 System Configuration

Following are some examples of using the mknod entry for the HP-UX Operating System.

For an SPU with only one SGC interface slot, a sample mknod entry would be:

```
/etc/mknod /dev/crt c 12 0x100000
```

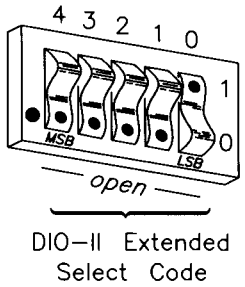
For an SPU with two SGC interface slots, a sample mknod entry for the other slot would be:

```
/etc/mknod /dev/crt c 12 0x000000
```

Refer to the graphics software documentation for your system for more information on device specific needs in software.

Series 300/400 System Configuration

If your Series 300/400 system has a conflict with the interface's select code address, you can change the address. If a second interface is installed with the same select code, one of them will need a new select code switch setting.



Note: If switch is down on the open side, that bit is zero

Figure 3-1. DIO-II Interface Address Switches

The switch configuration shown in Figure 3-1 is the default configuration on the board when it was shipped. It is configured for DIO-II Select Code 133-135.

The interface occupies three consecutive select codes in uncached address space. The first select code provides 4 Mbytes of address space for control. The second two select codes allocate 8 Mbytes of address space for full pixel addressing to the frame buffer.

Each switch position corresponds to four DIO-II select codes. The first select code is not used and is available for users other than the Graphics Processor. The second select code is used for the Graphics Processor's control space, and the last two are used for the Graphics Processor's frame buffer space. Table 3-1 shows the translation between the interface's address switch settings, the DIO-II select code, and the mknod minor numbers for use on an HP-UX system.

The following is an example of using the mknod entry for the HP-UX Operating System. The switch setting shown in Figure 3-1 would have a mknod entry of:

```
/etc/mknod /dev/crt c 12 0x850200
```

Also, the HP-UX kernel must be configured to accept a 12 Mbyte device. Refer to the *Starbase Device Drivers Library* (or an equivalent manual for your system) for recommended kernel configuration.

Refer to the graphics software documentation for your system for more information on device specific needs in software.

Caution If you have "Instant Ignition" (or if you depend on `/dev/crt` to automatically select the console) do not use a select code above 140.

A switch setting of 00000 is not a valid address code. The result will be a failure of the IODC test code to load and run at power-up (all LEDs on the interface will stay ON).

Table 3-1. DIO-II Address Base

DIO-II Select Code	Switch MSB—LSB	mknod Minor Number
133-135	00001	0x850200
137-139	00010	0x890200
141-143	00011	0x8d0200
145-147	00100	0x910200
149-151	00101	0x950200
153-155	00110	0x990200
157-159	00111	0x9d0200
161-163	01000	0xa10200
165-167	01001	0xa50200
169-171	01010	0xa90200
173-175	01011	0xad0200
177-179	01100	0xb10200
181-183	01101	0xb50200
185-187	01110	0xb90200
189-191	01111	0xbd0200
193-195	10000	0xc10200
197-199	10001	0xc50200
201-203	10010	0xc90200
205-207	10011	0xcd0200
209-211	10100	0xd10200
213-215	10101	0xd50200
217-219	10110	0xd90200
221-223	10111	0xdd0200
225-227	11000	0xe10200
229-231	11001	0xe50200
233-235	11010	0xe90200
237-239	11011	0xed0200
241-243	11100	0xf10200
245-247	11101	0xf50200
249-251	11110	0xf90200
253-255	11111	0xfd0200

4

Preventive Maintenance

Cleaning

Before cleaning the HP 98705 Graphics Processor, disconnect the power cord and interconnect cables from the controller. Dampen a clean, soft, lint free cloth with a solution of clean water and mild soap. Wipe the soiled areas, making sure that the cleaning solution does not get inside the Graphics Processor. For cleaning more heavily soiled areas, a 50% solution of clean water and isopropyl alcohol can be used. Then dry with a clean, soft, lint free cloth.

Caution Chemical spray-on cleaners used to clean appliances and other household applications may damage the surface. These and other chemical cleaners should not be used. Clean CRT display screens with clean water only.

5

Functional Description

Introduction

This chapter contains functional descriptions of the printed circuit assemblies in the HP 98705A/B/C Graphics Processor. The Graphics Processors are peripherals that connect to a system computer (SPU) through either an SGC Interface Card (for Series 700 — 98705-66582) or an HP 98702A Interface Card (DIO-II for Series 300/400).

The HP 98705 Graphics Processor has three supported models. The differences are in the combinations of Transform and Scan Converters, and Frame Buffer boards. Also, the HP 98705B will be the only Graphics Processor with a Z Buffer. The three models and their configuration are:

Model HP 98705A:

Transform and Scan Converter	98705-66573
8 Plane Frame Buffer (FB0)	98705-66570
Color Map	98705-66574

Model HP 98705B:

Transform and Scan Converter	98705-66573
16 Plane Frame Buffer (FB0 & FB1)	98705-66571
Color Map	98705-66574
16 Plane Z Buffer	98705-66572

Model HP 98705C:

Transform and Scan Converter	98705-66575
8 Plane Frame Buffer (FB0)	98705-66570
Color Map	98705-66574

Interface Card

The SGC or DIO-II interface card is connected to the appropriate computer bus and communicates with the Graphics Processor over a cable called the Graphics Address and Data (GAD) bus. Information on this bus is received by the Local Graphics Bus (LGB) control circuitry on the Transform and Scan Converter Board.

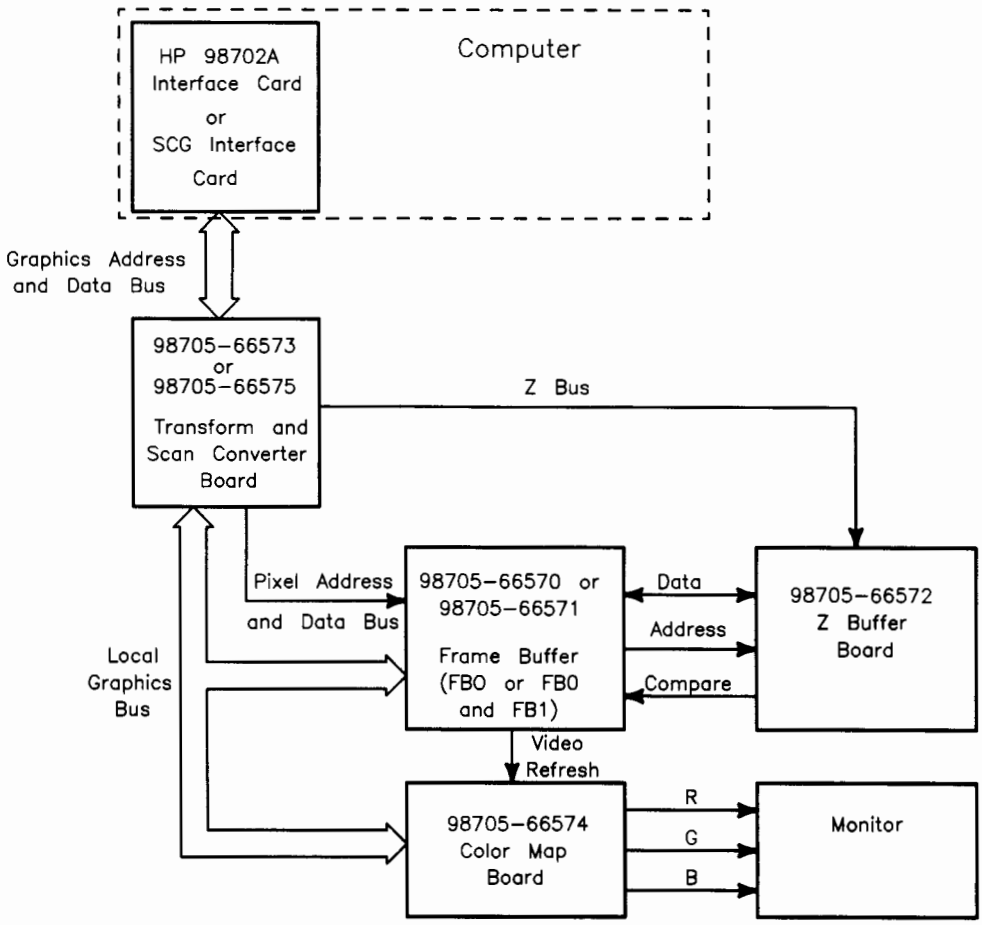


Figure 5-1. HP 98705A/B/C System Block Diagram

Transform and Scan Converter

There are two versions of the Transform and Scan Converter board. One is used with the HP 98705A and B, and a different one is used by the HP 98705C. The Transform and Scan Converter used in the HP 98705C has lower performance due to internal timing circuits.

The Transform and Scan Converter board provides three major functions.

- Local Graphics Bus (LGB) control. This section acts as an interface between the Graphics Address and Data bus, and the Local Graphics Bus.
- Transform engine functions. The main purpose is to receive commands and data from the host, process the commands, and generate programs for scan conversion.

- Scan Conversion functions. This section processes command packets and edge packets from the transform engine into pixel data for the Frame Buffer.

Frame Buffer

The Frame Buffer board has a controller, four overlay planes, and one of two image plane configurations (depending on which board is in the system). The image plane board differences are:

- Frame Buffer—PN 98705-66570 (eight image planes—used in the HP 98705A and C).
- Frame Buffer—PN 98705-66571 (eight double buffered image planes—used in the HP 98705B).

The frame buffer controller is the arbitrator between the scan converter, block mover, host, and refresh circuits. It also controls such things as double buffering, video and dynamic refresh, Z buffer, block moves, and other functions.

Z Buffer

The Z Buffer Board is a storage device for Z depth information. It compares new and old Z values to control the update of frame buffer and Z buffer information. The Z Buffer is only available for the HP 98705B. It is not available for the HP 98705A or C.

Color Map

The Color Map Board provides three mapping functions.

- It maps eight bit color from the image planes into 24 bit red, green, and blue output for the monitor.
- It maps the four bit color from the overlay planes into 24 bit red, green, and blue output for the monitor.
- It maps the two bit color from the cursor generator into 24 bit red, green, and blue output for the monitor.

The output is red, green, blue, and composite sync output to the monitor. The composite sync is on the green coax.

Monitor

This is not considered a part of the Graphics Processor but is the display unit for the output.

Circuit Descriptions

SGC Interface Card (98705-66582)

The Standard Graphics Connection (SGC) interface card is the Series 700 SPU interface to the Graphics Address and Data (GAD) bus of the Graphics Processor.

The interface can function as a slave only; it cannot master the SPUs SGC Bus. Accesses to the interface from the SGC Bus are synchronous. Accesses to the GAD bus from the SGC card are asynchronous. All accesses to modules on the SGC interface take a fixed number of states, but the clock can vary from 15 MHz to 33 MHz. The address and data outputs of the SGC interface modules are multiplexed, and all Graphics Processor outputs are driven directly from the same internal interface bus without isolation buffering.

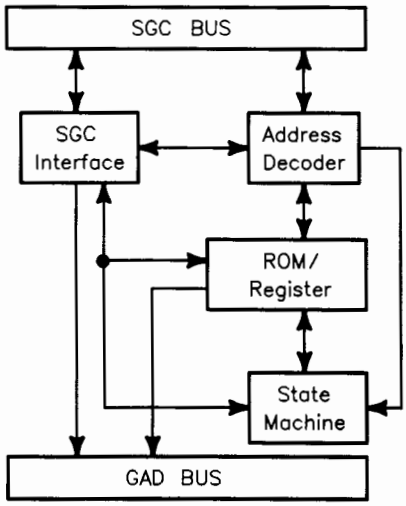


Figure 5-2. SGC Interface Block Diagram

In the SPU, 64 MBytes of address space is dedicated to each SGC slot. The graphics processor and SGC interface are mapped to the lower 32 MBytes of that address space, and are multiply-mapped (repeated) in the upper 32 MBytes. (In the future, this upper 32MBytes may be used for some other purpose.)

Address Decoder

The main function of the Address Decoder block is to determine which addresses on the SGC bus are for the interface slot. The decoder block does this by comparing input SGC bits to six bits that are hardwired on the SPU and detected by the SGC card. This comparison determines whether the message is for the Graphics Processor (without the need of any select switches).

SGC Interface

The SGC Interface block handles the majority of signal interfacing from the SPU to the GAD bus. Signals on the data bus, address bus, plus several other miscellaneous signals, are buffered and latched by the circuitry in this block. Since the SPUs SGC bus is synchronous, the signals on it generally are only valid for a short period around the SGC clock; a buffered version of this SGC clock signal is used throughout the interface board. The clock buffer is also part of the SGC Interface block.

ROM/Register

The ROM/Register block contains all the functionality local to the interface card; it consists of four modules plus their control logic. The modules are: Standard Textual Interface (STI) ROM, Local Control, Test/Status Register, and Timeout.

Functions performed by this block include: latching the decoded (selected) module addresses for the duration of a valid cycle, control of the eight LED's, timeout control (to prevent a timeout on the SGC bus in the event of a graphics processor failure), and access control for the GAD bus.

The Test/Status Register contains the LEDs and their control circuitry.

The (STI) ROM circuitry consists of an input address latch, an output buffer, and the STI ROM.

State Machine

The State Machine block is made up of two state machines. This block controls the entire interface board through states generated by two Programmable Array Logic (PAL) chips. State Machine One monitors and controls the activities related to the SGC bus. This is generally considered the master state machine since it is in control when the interface is idling. State Machine Two monitors and controls the events that relate to the GAD bus.

STI ROM Self Tests

Eight LEDs on the SGC Interface board indicate self-test error messages, and other status information. When all LEDs are off, the self test passed and the Graphics Processor and interface are operational.

The LEDs are numbered from zero thru seven. The first four LEDs (0 thru 3) form a 16 bit counter. They indicate an error condition during the self test procedure.

The next three LEDs (4 thru 6) indicate an interrupt status. They were used during development and are not used for troubleshooting.

The last LED (7) indicates a soft reset of the hardware. This LED was also used during development and is not used for troubleshooting.

When LEDs zero thru three indicate an error during the STI self-test, the LED binary presentation is converted to a decimal number between one and 15. This number is then used to locate the failed component in the following list.

1 `LED_FAILURE` — The self-test could not access the LEDs. Interface board failure.

2 `ROM_READ_FAILURE` — The self-test could not access the ROM. Interface board failure.

3 ROM_CRC_FAILURE — The self-tests had an incorrect ROM CRC. Interface board failure.

4 DCREG_ACCESS_FAILURE — The self-tests could not access the Device Control Register in the scan converter. Transform and Scan Converter board failure.

5 STATUSREG_ACCESS_FAILURE — The self-tests could not access the Status Register in the scan converter. Transform and Scan Converter board failure.

6 CTLREG_ACCESS_FAILURE — The self-tests could not access the Control Register in the scan converter. Transform and Scan Converter board failure.

7 CMAPREG_ACCESS_FAILURE — The self-tests could not access the Color Map Register. Color Map board failure.

8 FB_OR_OV_ACCESS_FAILURE — The self-tests could not access the Frame Buffer or Overlay Register. Frame Buffer board failure.

9 BE_CKT_FAILURE — The self-tests had a failure when Byte Enable was exercised. Interface board failure.

10 CTL_REGS_FAILURE — The self-tests had a failure when exercising the control registers in the Transform and Scan Converter. Transform and Scan Converter board failure.

11 CMAP_REGS_FAILURE — The self-tests had a failure when exercising the color map registers on the Color Map board. Color Map board failure.

12 FB0_PLANE_FAILURE — The self-tests had a failure when exercising Frame Buffer zero. Frame Buffer board failure.

13 FB1_PLANE_FAILURE — The self-tests had a failure when exercising Frame Buffer one. Frame Buffer board failure.

14 OV_PLANE_FAILURE — The self-tests had a failure when exercising the Overlay Plane. Frame Buffer board failure.

15 BLK_MVR_HUNG_FAILURE — The self-tests had a failure when exercising the Block Mover in the Frame Buffer. Frame Buffer board failure.

HP 98702A DIO-II Interface Card

The HP98702A interface is a DIO-II to Graphics Address and Data (GAD) bus cable. The interface provides a means of connecting the Graphics Processor to a Series 300/400 SPU.

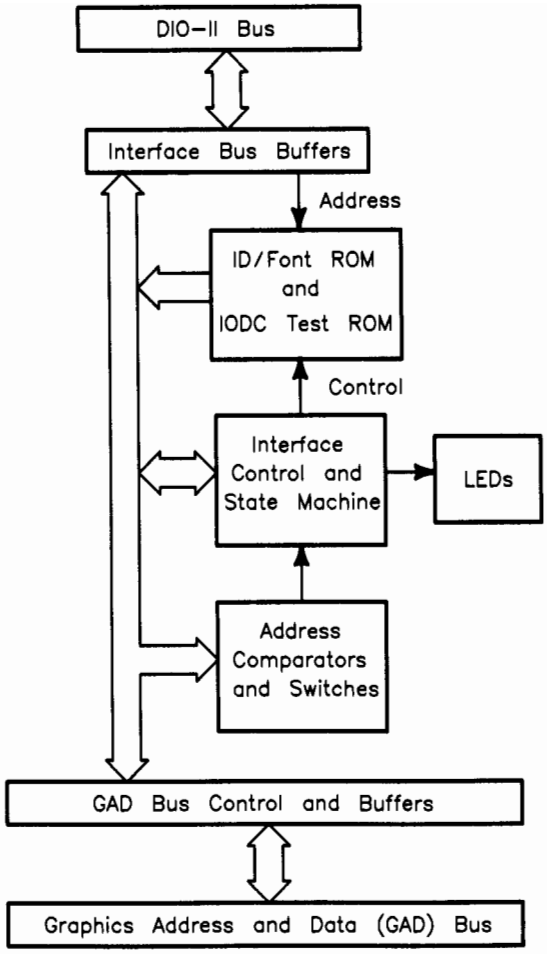


Figure 5-3. HP 98702A Interface Block Diagram

The interface board provides a buffered link between the SPU DIO-II backplane bus and the 32-bit multiplexed Graphics Address and Data (GAD) bus. The interface acts as a slave on the DIO-II bus and as a master controller to the Local Graphics Bus.

Interface Bus Buffers

The DIO data, control, and address bus buffers isolate the DIO-II bus from the interface circuitry.

ID/Font and IODC Test ROMs

The ID/Font ROM contains the Graphics Processor identification (ID) and the default font to be used by the Boot ROM.

The IODC Test ROM contains the test code used by the Boot ROM. The primary goal of the IODC ROM code is to accurately test the hardware used by the Integrated Terminal Emulator (ITE). If the ITE is functioning, then more sophisticated diagnostics can be run to test the entire system.

The device under test may be the system console. If so, a failure in the HP 98705 will not be able to produce an error message on the display. Therefore, an LED display has been made available on the HP 98702 Interface board. All failures are reported twice:

- To the system console.
- To the LEDs on the interface board.

Six of eight LEDs are used to indicate error status. At boot time, the Boot ROM (Rev C1 or later) loads the test code from the IODC ROM. SPU control alternates between the Boot ROM and the test code. During the time test code is in control, all accesses to the Graphics Processor are contained within *try/recover* blocks to guard against unexpected events. Six test modules are called in sequence by the Boot ROM, five of the modules do testing, while the sixth module reports the final status. At the start of testing, the LEDs will all be turned on for a short period of time (If they stay on, ensure that the Interface Address Switches are not all set to zero). During testing, the current module number is always displayed on the interface LEDs. After completion of the "last" module, the LEDs display error conditions found during the tests. In a functional unit, all LEDs are turned OFF.

IODC code attempts to test a limited set of hardware, defined by the ITE. Specific hardware tested includes:

- Interface board, HP 98702A:
  - Data bus to the Frame Buffer Controller.
  - Address path to the overlay planes.
- Frame Buffer Controller:
  - Reads and writes to Frame Buffer overlay planes using bytes, words, and long words.
  - Fast window moves.
  - Slow window moves.
- Color Map board:
  - Color Map driven by the overlay planes.
  - Color Map Controller.
  - Color Map Shadow RAM.
  - Digital to Analog Converters (DACs).

The analog path from the Color Map to the video connector is not tested (this can be tested using the MONITOR TEST button on the back of the unit). If the Color Map can be written to, and correctly read back, then the assumption is made that the analog outputs of the color digital-to-analog converters (DACs) are functioning.

LEDs

Six of the eight LEDs on the interface board are used for error message display. The other two LEDs are not defined. The defined LEDs are the first six when counting from the left (or top if the wider surface of the unit is mounted vertically) and when facing the handle end of the interface board. More than one LED can be lit at any one time. The LEDs have been defined as follows:

1 Interface LED. This LED indicates a problem in the interface board. The interface sends a test to itself and if a reply is not returned, it generates the "HP98702 Interface Failure" error message and lights LED number one.

2 Cable and Transform LED. This LED indicates a failure of the cable or the Transform and Scan Converter board. The error message is: "Cable/HP98705-66573 Error". The message means that the error can be due to the GAD bus cable being bad, the Transform and Scan Converter board being bad (either 98705-66573 or 98705-66575), or a bad HP 98702 Interface board as the third possibility.

3 Transform LED. This error is generated when the test can get to the Transform and Scan Converter board, but the data is incorrect. The generated message is:

"HP98705-66573 Error" (also means a 98705-66575 if installed). In general, this LED is used in conjunction with LED number two and indicates that the GAD bus cable, or the HP 98702A Interface board are not causing LED two to be lit.

4 Frame Buffer LED. This LED is lit when there is an error on the Frame Buffer board. Messages on the console are: "HP98705 FB Memory/Access Error" or "HP98705 FB Block Move Error".

5 Color Map LED. Indicates an error on the color map board. Error messages sent to the console are: "HP98705 Color Map Error", or "HP98705 Color Map R/W Error".

6 Bus LED. Indicates that a Graphics Address Strobe was sent to the Graphics Processor (any of the three boards may answer) and a Data Transfer ACKnowledge signal was not returned. Error messages sent to the console are: "HP98702 Bus Error" or "HP98705 Bus Error". In general, this would indicate a problem in:

- GAD bus cable.
- Power Supply.
- Power Supply Fuse.

Interface Control and State Machine

The interface control registers include reset registers, frame buffer location register, card status and control register.

The State Machine controls read/write cycle timing, and interface register accesses. Arbitration of Local Graphics Bus (LGB) control is managed on the Transform and Scan Converter board.

Address Comparators and Switches

The address comparators and switches determine the Graphics Processor select code.

The interface occupies three consecutive select codes in the SPU's uncached address space. The first select code provides 4 Mbytes of address space for control. The second two select codes allocate 8 Mbytes of address space for full pixel addressing to the frame buffer.

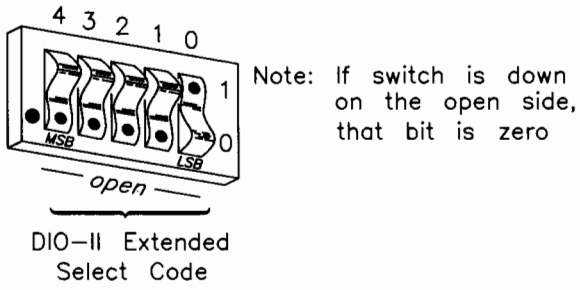


Figure 5-4. DIO-II Interface Address Switches

Each switch position corresponds to four DIO-II select codes. The first select code is not used and is available for other users other than the Graphics Processor. The second select code is used for the Graphics Processor's control space, and the last two are used for the controller's frame buffer space.

See the *Select Code Addresses* section in Chapter 3 for more information about using the switches.

GAD Bus Control and Buffers

The GAD bus Control and Buffers:

- Passes one to four data bytes per read/write cycle between the host computer and the GAD bus.
- Isolates the internal control registers of the interface from the GAD bus.
- Generates GAD bus data strobes.
- Masks select code information.
- Maps DIO-II addresses into Local Graphics Bus address space.

Transform and Scan Converter Board

The Transform and Scan Converter board in your Graphics Processor is one of two configurations. The configuration is determined by the model number of the Graphics Processor. The HP 98705 Models A and B use part number 98705-66573, while the model C uses part number 98705-66575. The difference in the two configurations is in the internal timing circuitry. Otherwise the functional description is the same.

This board description addresses the 98705-66573 used in the HP 98705A and B.

The board consists of three functional subsystems:

1. Local Graphics Bus (LGB) Control.
2. Transform Engine.
3. Scan Converter.

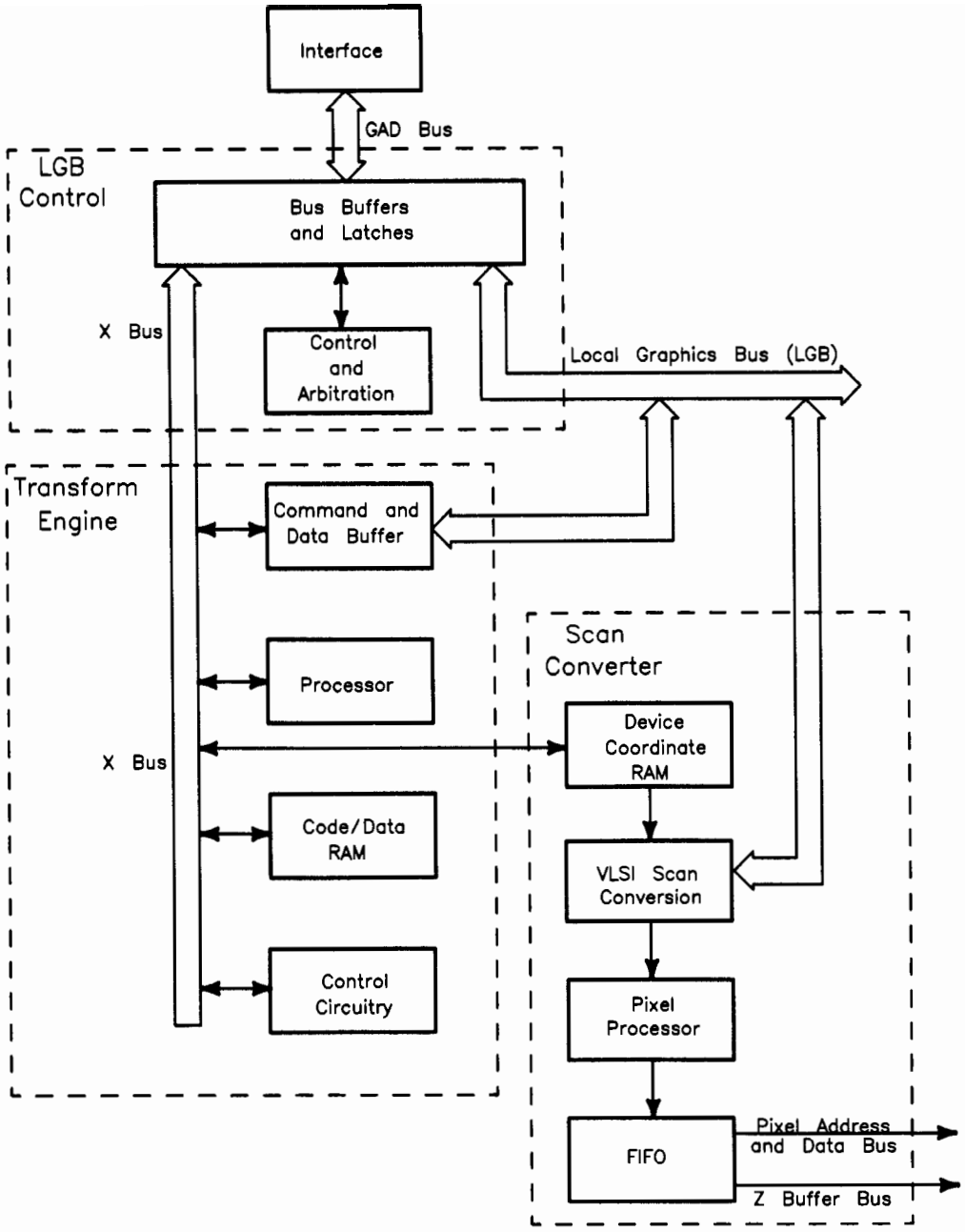


Figure 5-5. Transform and Scan Converter Block Diagram

LGB Control Block

The Local Graphic Bus Control block's primary purpose is to interface the Graphics Address and Data (GAD) bus to the Local Graphics Bus (LGB).

The GAD bus is a 32 bit bus containing multiplexed address and data. The Local Graphics Bus contains 30 separate bits of address and 32 bits of data. The LGB Control block latches the address and data to provide for demultiplexing. The address map of the GAD bus, and the LGB are identical.

A data path (through bus buffers) also provides direct access from the GAD bus to the XBUS for the host computer. A bus arbitrator allows connection to the XBUS by cycle stealing

from the transform engine's processor. This arbitration is transparent to both the host and the transform engine and requires no prior setup. The arbitrator also allows the host to gain control of the XBUS and hold on to it.

The Local Graphics Bus Control block provides (in conjunction with the host interface) LGB arbitration. This allows either the host, via the interface, or the transform engine to be master of the LGB.

There is reset circuitry on the Transform and Scan Converter board that allows reset of the Graphics Processor when; a graphics reset is received from the host, or power is applied to the Graphics Processor.

Transform Engine Block

The Transform Engine has:

- An interface to the LGB.
- Entities that reside on the XBUS.

Although the host has direct access to the entities on the XBUS via the LGB control block, it normally communicates to the Transform Engine through the LGB. The transform engine resides on the XBUS and its main job is to receive commands and data from the host, process the commands, and generate device coordinate data for scan conversion.

The Command and Data Buffer receives the command and data information from the host computer and buffers them in a double buffer. The host can fill one buffer at the same time the transform engine is processing the other.

The transform engine processor is the main computing resource for processing the commands and data in the Command and Data Buffer. It executes code stored in the Code/Data RAM that is downloaded by the host after a reset. Data structures and other values are built and stored in the Code/Data RAM. Floating point hardware is built into the processor and provides high speed computing. The transform engine processor, through arbitration, may also access the LGB for purposes of communicating with the Scan Converter, the Frame Buffer Controller, or the Color Map.

Scan Converter

The Scan Converter's main function is to process device coordinate data and edge packets from the Transform Engine into pixel data.

When transform engine processing is completed, the transform engine processor transfers the results to the Device Coordinate RAM. The Device Coordinate RAM is double buffered to allow the Transform Engine to fill one buffer at the same time the VLSI Scan Converter is emptying the other buffer.

The VLSI Scan Converter accepts vertex and endpoints information and converts the objects described by these vertices and endpoints into pixels. The VLSI Scan Converter then outputs the pixel data (including the XY address, RGB color, and Z depth values) to the Pixel Processor block.

The Pixel Processor accepts pixel data from VLSI Scan Converter and performs pixel clipping, dithering, transparency, and gamma correction. The output goes into the FIFO to buffer the transfer rates to the Frame Buffer.

The First In First Out (FIFO) buffer outputs drive two buses: the Pixel Address and Data bus, and the Z Buffer bus. The Pixel Address and Data bus contains the pixel RGB color and

XY address. It is sent to the Frame Buffer Controller to be written into the Frame Buffer. The Z Buffer bus contains the Z depth which is sent to the Z Buffer.

Frame Buffer

The frame buffer has a 2048 by 1024 resolution. 1280 by 1024 is viewable for storing bitmap images (the remainder of memory is used for offscreen processes such as font storage). It is configured to have four overlay planes, and either eight image planes or 16 image planes (eight planes double buffered). Whether it has eight or 16 planes depends on which board configuration is used.

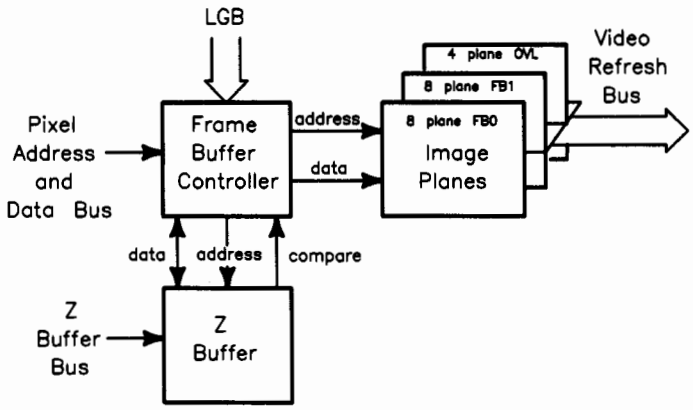


Figure 5-6. Frame Buffer and Z Buffer Block Diagram

Frame Buffer Controller

The frame buffer controller provides access to the frame buffer and its configuration registers. The frame buffer controller is responsible for:

- Frame buffer arbitration (between scan converter, block mover, host, and refresh)
- Frame buffer configuration (fold/full, write enables, replacement rules)
- Video and dynamic refresh
- Block moves
- Repeat pattern control
- Z buffer control
- Overlay buffer control
- Bit-per-pixel transfers

The Frame Buffer Controller also contains the block mover hardware used to move rectangular arrays of pixels from one place in the Frame Buffer to another. Block mover operations consist of regular block moves, fast window moves, block mover repeat pattern fills, and plane-to-plane transfers.

Image Planes

The Graphics Processor supports two image plane configurations: either eight planes (FB0), or eight planes double buffered (FB0 and FB1). When using eight planes double buffered, eight planes are displayed while the other eight planes are being updated.

Accesses into the image planes are made by the Scan Converter (via the Pixel Address and Data bus), Block Mover, or the LGB. LGB accesses may be byte, word, or long word; in bit per pixel, byte per pixel (folded), or long word per pixel (full) format.

The maximum number of color bits per pixel is eight.

Registers in the Frame Buffer Controller control the data format on the LGB, what planes drive the LGB, what planes can be written to, and how they are written to. Registers in the Color Map control what banks are displayed.

Overlay Planes

The Graphics Processor supports four overlay planes whose data can conditionally overlay the contents of the image planes being displayed on the screen.

Accesses to the overlay planes can be made by the Scan Converter, LGB, or the block mover. Access to overlay planes is similar to the way Image Planes are accessed.

Z Buffer

Note the block diagram in Figure 5-5 for the Z Buffer relationship to the Frame Buffer.

The Graphics Processor supports 16 optional Z Buffer planes to store Z depth information for each of the pixels in the frame buffer. The Z Buffer is not double buffered and does not need to be since the values are not viewed and are logically associated with the image planes that are being updated.

Accesses to the Z buffer can be made by the Scan Converter, LGB (via the Frame Buffer Controller), or block mover similar to the way they are made to the image planes. (Bit per pixel accesses into the Z Buffer are not supported.)

Color Map

The color map is the output section of the Graphics Processor. It provides the analog drive for a monitor.

The color map provides three mapping functions:

- It maps the 8-bit color from the image planes into 24-bit red, blue, green (RGB).
- It maps the 4-bit color from the overlay planes into 24-bit RGB.
- It maps the 2-bit cursor generator into 24-bit RGB.

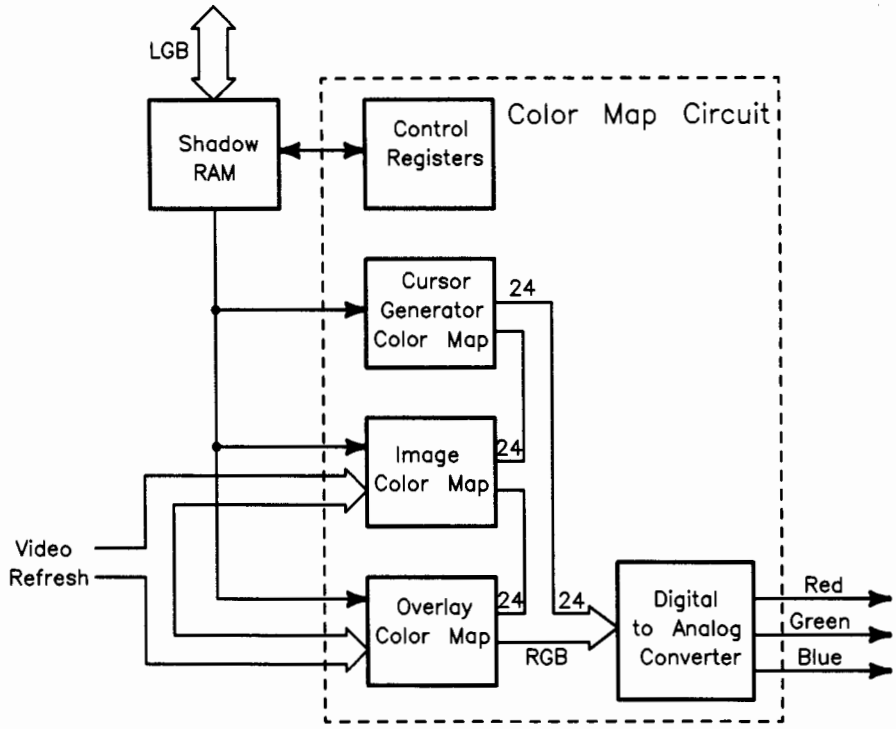


Figure 5-7. Color Map Block Diagram

Shadow RAM

The Shadow RAM acts as a buffer. Data can be written to the Color Map at any time. Therefore, it is stored in the Shadow RAM until the color map circuits are ready for it.

Color Map Circuits

This function is provided by a special purpose VLSI chip.

This chip contains most of the Control Registers, the Cursor Generator Color Map, the Overlay Color Map, and the Image Color Maps.

It receives the image and overlay color data from the video refresh bus. The contents of the control registers, the overlay data, and the cursor generator determine whether image, overlay, or cursor colors are displayed.

The 24 bit color from either the image, overlay, or cursor color map is converted into analog signals by the Digital to Analog Converter for display on the monitor.

The color map circuits generate the horizontal sync and vertical sync signals for the monitor. These are delivered on the Green monitor signal. They also provide vertical blank status for the host and Transform Engine.

The color map circuits do not support PAN and ZOOM, image blending, non-dominant overlays, or rubberband cursors.

Power Supply

The power supply is a switching supply. It develops three voltages for use by the HP 98705 Graphics Processor. Table 5-1 contains the voltages, and Tolerances.

Table 5-1. Voltages

Nominal voltage	Tolerance
+5.1 V	± 3%
+12.0 V	± 5%
− 2.0 V	± 5%

The power supply has one fuse rated at 6 amps and 250 volts. The same fuse is used for both 115 volt or 230 volt input.

Note The voltages listed on the label on the Power Supply voltage select switch may be different than what is on the case. Do not let this confuse you. Use the 115/230 volt figures.

The power supply is replaceable but not field repairable (beyond fuse replacement).

If 230 volts is applied while the voltage select switch is in the 115 volt position, the fuse will blow but the rest of the circuitry is protected.

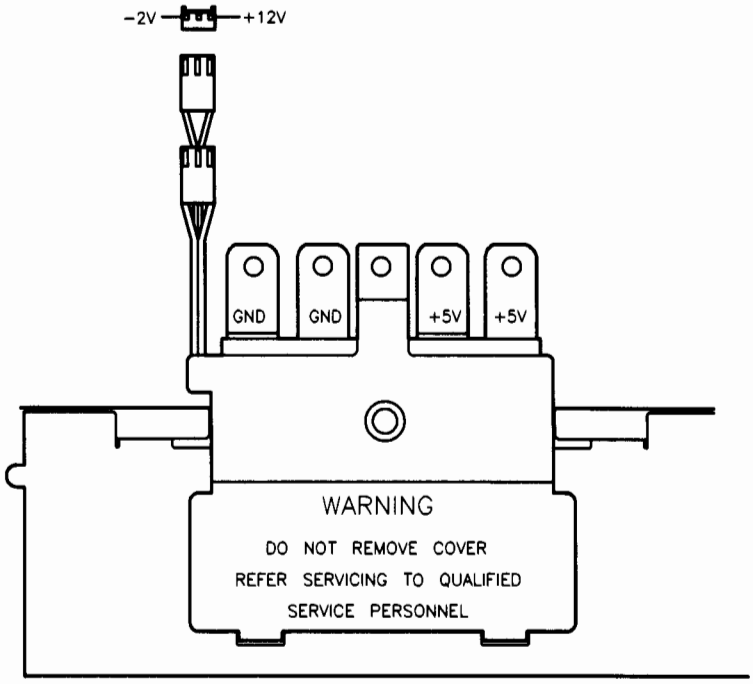


Figure 5-8. Voltage Location on the Power Supply

6

Removal and Replacement

Introduction

This chapter explains how to remove and replace any of the assemblies of the HP 98705A/B/C Graphics Display Controller.

Caution Electronic assemblies in the HP 98705A are susceptible to damage by electro-static discharge.

Be careful how you handle the printed circuit assemblies. Do not touch the traces or the connector pins without using anti-static protection. Electro-static discharge can destroy electronic parts and assemblies. Use an anti-static workstation with a wrist band. The HP part number is 9300-0933.

Required Tools

- T-10 TORX® screwdriver.
- Pozidriv® #2 screwdriver.
- $\frac{9}{16}$ inch deep well socket.

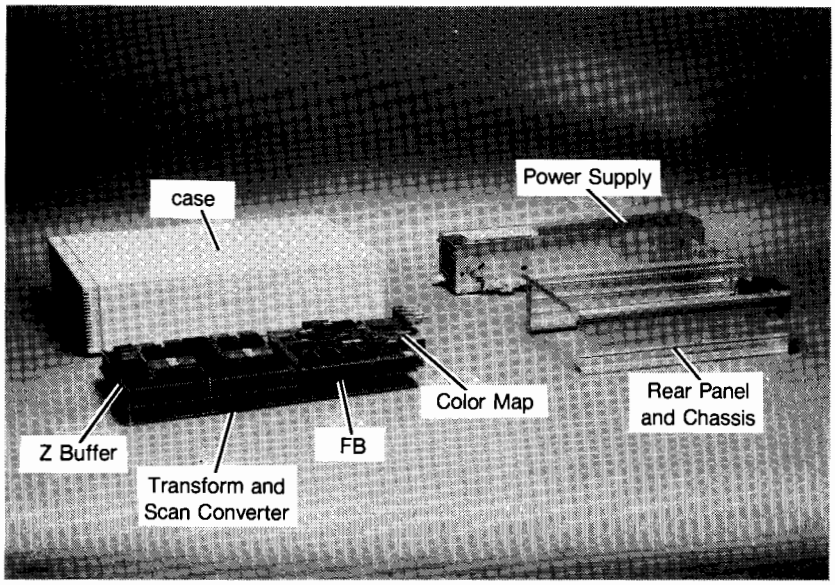


Figure 6-1. HP 98705A/B/C Parts

Cover Removal

All of the assemblies are contained in an extrusion chassis and are attached to the rear panel. Therefore, they are removed from the cover in one complete set.

1. Move power switch to OFF.
2. Disconnect power cable, RGB coax cables, and Graphics Bus cable.
3. Remove 7 TORX screws from the rear panel (Figure 6-2).
4. Slide the chassis and rear panel to the rear and remove the set of assemblies from the cover. It may help to lift on the RGB connectors while sliding the chassis out of the cover.
5. Set the cover aside.

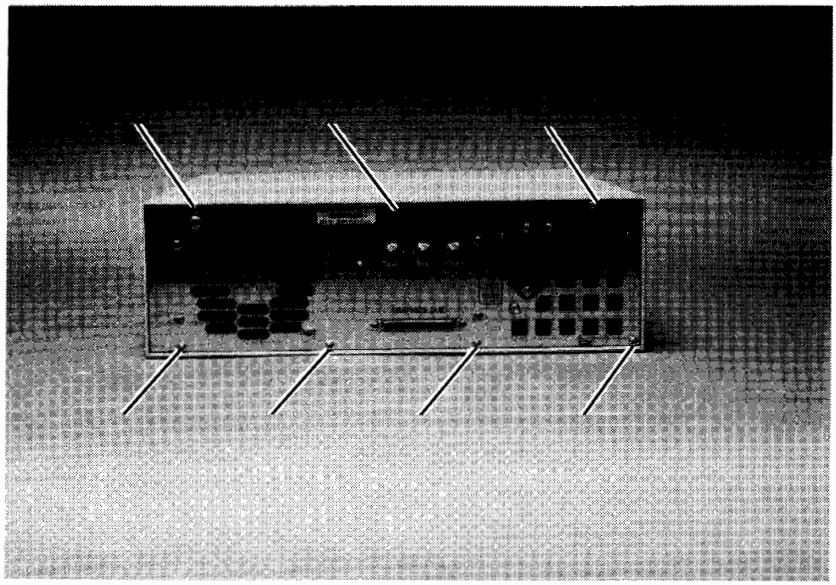


Figure 6-2. Cover Screws

Reverse this procedure to reinstall the cover.

Caution Do not cross thread or over tighten the TORX® screws. The threads in the cover are easily stripped.

Power Supply Removal

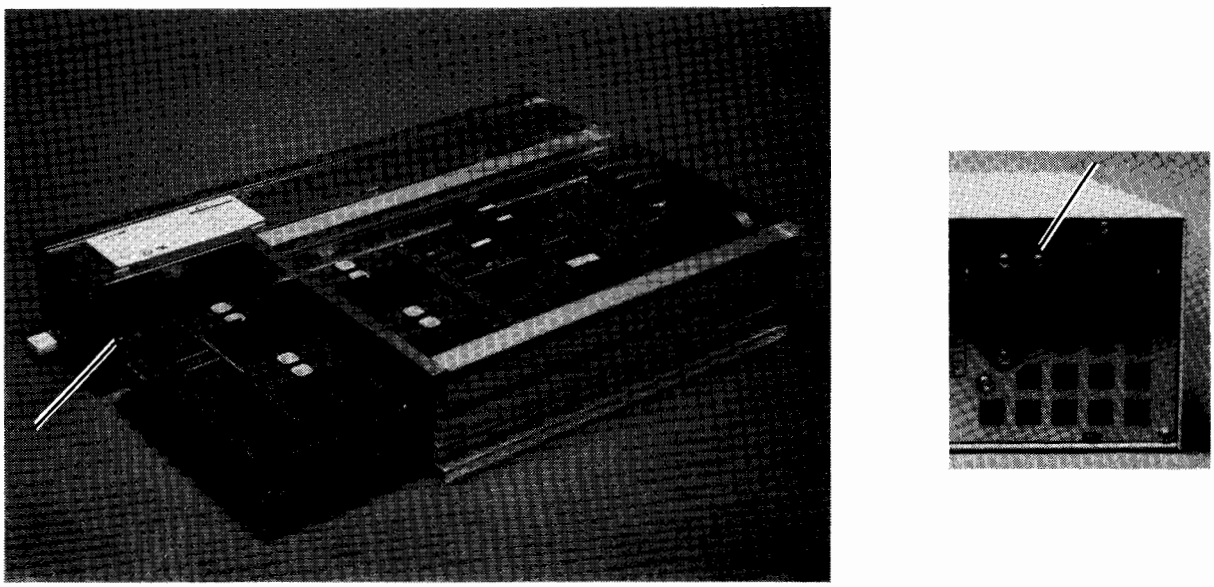


Figure 6-3. Power Supply Removal

1. Remove the cover.
2. Remove four Pozidriv electrical connection screws and one bracket screw on the bottom of the stack near the front of the assembly.
3. Remove the TORX screw that secures the power supply to the rear panel.

Note Note the orientation of the yellow and blue wires on the small connectors between the power supply and the Transform and Scan Converter Assembly, and to the Frame Buffer Assembly. This will make it easier to reassemble.

---

4. Disconnect the two small connectors from the Transform and Scan Buffer Assembly and from the Frame Buffer Assembly.
5. Lift the power supply out of the assembly and set it aside.

Reverse this procedure to reinstall the power supply. Install it mechanically before making the electrical connections.

Caution When reinstalling the Pozidriv #2 screws that make the power connections, be sure the screws are sufficiently tight for good electrical contact. A loose connection could result in intermittent operation.

Printed Circuit Assembly Removal

The PCAs are all held together in the chassis as one assembly. Remove the stack of boards from the chassis before attempting to disassemble individual boards from the stack. For example, to remove the Transform and Scan Converter PCA the stack must be removed from the chassis and the other PCAs must be removed from the stack in order. Note the cautions under *Stack Reassembly*.

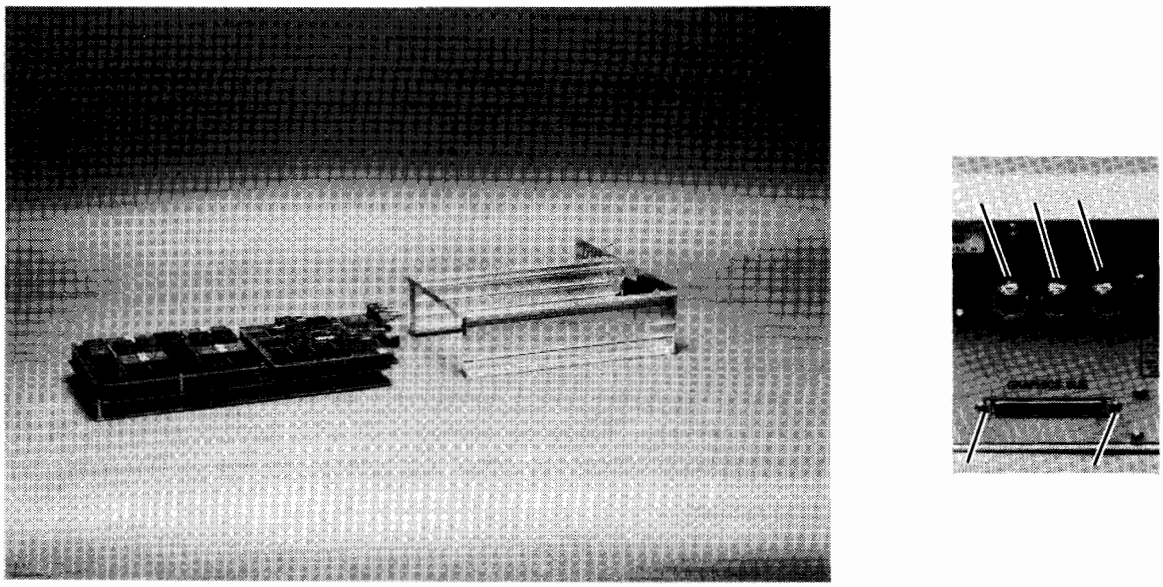


Figure 6-4. Printed Circuit Assembly and Rear Cover/Chassis Removal

Stack Removal.

1. Remove the cover.
2. Remove the power supply.
3. Remove the large nuts and washers from the three video (RGB) connectors.
4. Remove two TORX screws from the graphics bus connector.
5. Slide the entire stack assembly away from the rear panel far enough to remove the small connector that connects the fan to the Frame Buffer Assembly.
6. Slide the entire stack assembly out of the rear panel/chassis assembly.
7. Set the rear panel/chassis assembly aside.

Z Buffer Removal.

1. Remove two TORX screws from the Z Buffer Board.

Caution The PCA connectors have many pins and are very difficult to disconnect. Be careful that you do not bend the board excessively, or bend the pins while loosening the interconnection. Applying pressure to both boards at once, at the connector location, works best. Start at one end of the connection and work towards the other end.

Use anti-static measures to protect the boards.

2. Carefully loosen the interconnect connector and lift the Z Buffer free of the stack.
3. Set it aside in an anti-static bag.

Color Map Removal.

1. Remove two TORX screws from the Color Map board.

Caution The PCA connectors have many pins and are very difficult to disconnect. Be careful that you do not bend the board excessively, or bend the pins while loosening the interconnection. Applying pressure to both boards at once, at the connector location, works best. Start at one end of the connection and work towards the other end.

Use anti-static measures to protect the boards.

2. Loosen the interconnect connectors and lift the Color Map board clear of the stack.
3. Set it aside in an anti-static bag.

Frame Buffer or Transform and Scan Converter Removal.

1. Remove three TORX screws from the Frame Buffer board.

Caution The PCA connectors have many pins and are very difficult to disconnect. Be careful that you do not bend the board excessively, or bend the pins while loosening the interconnection. Applying pressure to both boards at once, at the connector location, works best. Start at one end of the connection and work towards the other end.

Use anti-static measures to protect the boards.

2. Loosen the interconnect connectors and lift the Frame Buffer board clear of the Transform and Scan Converter board.
3. Set it aside in an anti-static bag.

Stack Reassembly.

Caution Ensure the pins are not bent and are properly aligned before pressing the boards together. Support the board with the male connector to avoid excessive bending.

Caution When installing the screws, ensure the spacers are lined up with the holes to avoid cross threading the screws.

1. Reverse the procedures to reassemble the stack and the Graphics Processor.
2. Remember to reconnect the fan to the frame buffer assembly.
3. After reassembly, ensure both fans are operating.

7

Adjustments

Introduction

There are no adjustments for the HP 98705.

8

Troubleshooting and Diagnostics

Introduction

This section contains troubleshooting procedures for repair of the HP 98705 Graphics Processor. The following procedures are provided to help you troubleshoot the Graphics Processor.

- Off-Line Diagnostics.
  - Check for power to the system.
  - Check for HP 98705 output and monitor operation.
  - Check GAD cable for proper connection.
  - Check STI ROM Test LEDs (SGC bus).
  - Check IODC Test LEDs (DIO-II bus).
- On-Line Diagnostics.
  - STI test messages.
  - IODC test messages (if console is available and interface is DIO-II).
  - SAX (Domain).
  - On-line Diagnostics (HP-UX).

When troubles are located, replace the faulty component(s), and confirm correction of the problem.

Note Troubleshooting is to the assembly level only.

Off-line Troubleshooting

Off-line diagnostics are used if nothing is visible on the display.

Question User

Spend some time with the user and discuss the problem:

1. What are the symptoms?
2. Where does the problem appear to be?
3. When did the problem first appear?
4. Is the problem getting better or worse?

Use this information as a starting point in your troubleshooting process.

Warning **Ensure equipment is switched OFF and disconnect power cords before removing any covers.**

Check for Power

Are the fans running? (There are two fans—one for the power supply and one for the stack.)

If fans are running—Power is on the Graphics Processor and +12 volts is getting to the fans.

If fans are not running:

1. Check power cord.
2. Check voltage select switch.
3. Check fuse.
4. Check voltages out of the Power Supply (Figure 8-1). Note that the voltages are marked on the boards next to the power supply connections to the board.
5. If the above checks are okay:
   a. For stack fan—Replace fan or Frame Buffer board.
   b. For Power Supply fan—Replace the Power Supply.

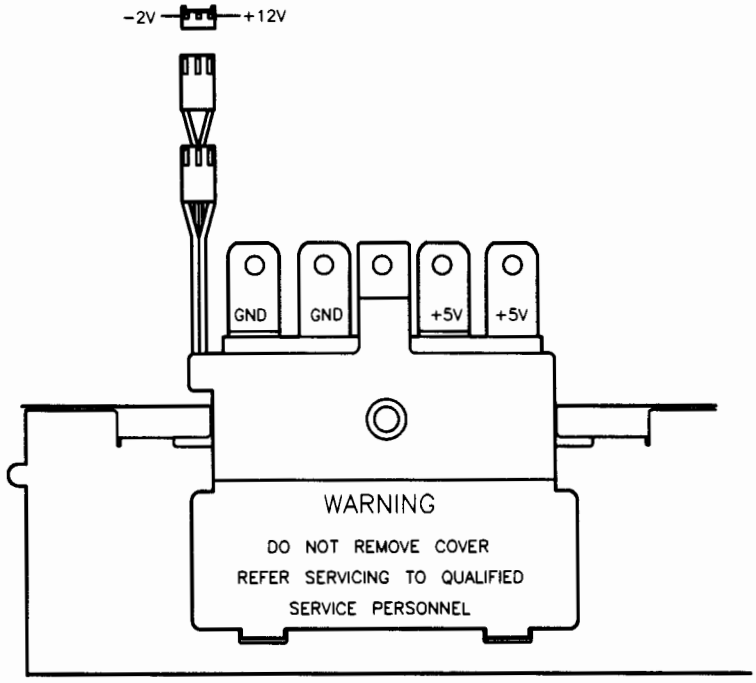


Figure 8-1. Power Supply Output

HP 98705 Output and Monitor Check

Press the MONITOR TEST button on the back of the HP 98705. The monitor should have a white raster while the button is held in. If not:

- Check that the monitor and HP 98705 are powered-up and the RGB cable is connected correctly between the units.
- Suspect the:
  - Monitor.
  - RGB cable.
  - Color Map board.
  - HP 98705 power supply (+5.1 volts).

STI ROM Self-test LEDs (SGC Bus)

Note The Z Buffer is not tested or required for testing. However, it *could* affect other IODC tests. If you suspect this, remove the Z Buffer and repeat the tests.

Caution Ensure disks are powered down when Boot ROM testing the system. This prevents corruption of the operating system or application programs in case of trouble.

I/O testing is done by the Boot ROM accessing code in the STI ROM on the SGC Interface board. The goal of the STI ROM code is to test the Integrated Terminal Emulator (ITE) hardware. If the ITE is functioning, more sophisticated on-line diagnostics can be run.

An LED display is available on the SGC interface board in case the console does not have a display. All STI failures are reported to the LEDs.

Eight LEDs on the SGC Interface board indicate self-test error messages, along with other status information. When all LEDs are off, the self test passed and the Graphics Processor and interface are operational.

The LEDs are numbered from zero thru seven. The first four LEDs (0 thru 3) form a 16 bit counter. They indicate an error condition during the self test procedure. The other LEDs are used for non-troubleshooting purposes (see Chapter 5).

When LEDs zero thru three indicate an error, a two step process determines the failed component; first, the LED binary presentation is converted to a decimal number between one and 15; then the number is used to locate the failed component in the following list.

1 `LED_FAILURE` — The self-test could not access the LEDs. Interface board failure.

2 `ROM_READ_FAILURE` — The self-test could not access the ROM. Interface board failure.

3 `ROM_CRC_FAILURE` — The self-tests had an incorrect ROM CRC. Interface board failure.

4 `DCREG_ACCESS_FAILURE` — The self-tests could not access the Device Control Register in the scan converter. Transform and Scan Converter board failure.

5 `STATUSREG_ACCESS_FAILURE` — The self-tests could not access the Status Register in the scan converter. Transform and Scan Converter board failure.

6 CTLREG_ACCESS_FAILURE — The self-tests could not access the Control Register in the scan converter. Transform and Scan Converter board failure.

7 CMAPREG_ACCESS_FAILURE — The self-tests could not access the Color Map Register. Color Map board failure.

8 FB_OR_OV_ACCESS_FAILURE — The self-tests could not access the Frame Buffer or Overlay Register. Frame Buffer board failure.

9 BE_CKT_FAILURE — The self-tests had a failure when Byte Enable was exercised. Interface board failure.

10 CTL_REGS_FAILURE — The self-tests had a failure when exercising the control registers in the Transform and Scan Converter. Transform and Scan Converter board failure.

11 CMAP_REGS_FAILURE — The self-tests had a failure when exercising the color map registers on the Color Map board. Color Map board failure.

12 FB0_PLANE_FAILURE — The self-tests had a failure when exercising Frame Buffer zero. Frame Buffer board failure.

13 FB1_PLANE_FAILURE — The self-tests had a failure when exercising Frame Buffer one. Frame Buffer board failure.

14 OV_PLANE_FAILURE — The self-tests had a failure when exercising the Overlay Plane. Frame Buffer board failure.

15 BLK_MVR_HUNG_FAILURE — The self-tests had a failure when exercising the Block Mover in the Frame Buffer. Frame Buffer board failure.

IODC Test LEDs (DIO-II Bus)

Note The Z Buffer is not tested or required for testing. However, it *could* affect other IODC tests. If you suspect this, remove the Z Buffer and repeat the tests.

Caution Ensure disks are powered down when Boot ROM testing the system. This prevents corruption of the operating system or application programs in case of trouble.

I/O testing is done by the Boot ROM accessing code in the IODC ROM on the HP 98702A Interface board. The goal of the IODC ROM code is to test the Integrated Terminal Emulator (ITE) hardware. If the ITE is functioning, more sophisticated on-line diagnostics can be run.

An LED display is available on the HP 98702 Interface board in case the console messages can not be displayed. All failures are reported to the LEDs (as well as the system console).

Six of the eight LEDs on the board are used to indicate error status. These are the first six when counting from the left (or top if the wider surface of the unit is mounted vertically) and when facing the handle end of the board.

During testing, the current module number (of six test modules) is displayed on the interface LEDs. After completion of the "last" module, the LEDs display error conditions found during the tests. If all IODC tests pass, all LEDs are OFF.

What Is Tested

IODC code tests a limited set of hardware. Specific hardware tested includes:

- HP 98702A Interface board:
  - Data bus to the Frame Buffer Controller.
  - Address path to the overlay planes.
- Frame Buffer Controller:
  - Reads and writes to Frame Buffer overlay planes using bytes, words, and long words.
  - Fast window moves.
  - Slow window moves.
- Color Map board:
  - Color Map driven by the overlay planes.
  - Color Map Controller.
  - Color Map Shadow RAM.
  - Digital to Analog Converters (DACs).

The analog path from the Color Map to the video connector is not tested. This path can be confirmed using the MONITOR TEST button on the back of the HP 98705.

Domain System. At power up, the ITE tests are run which checks most of the HP 98705 system. However, the window system must be up and running before SAX Diagnostics can be used. Therefore, a "Self Test Subset" is automatically run to ensure the circuitry for the windows system is operational.

If no self test error messages are generated at power up, the SAX program can be run to thoroughly test the Graphics Processor.

Refer to: *Using Domain Diagnostics, Volume 1* Part Number 009329-A02 for information on error messages and the SAX (or GR) diagnostics tests.

LED Definition

A power ON reset signal lights all LEDs. This is the only time all LEDs are lit at once. System resets do not change the LEDs.

Power cycle the SPU and watch the LEDs. If the Boot ROM accesses the Graphics Processor, it will try to load the test code. If the test code cannot be loaded and run, all LEDs will stay ON (such as when the interface address switches are set to the illegal setting of 00000).

While running the test code, the LEDs will flash. Eventually the tests will stop with an error code or test pass indication. The LEDs are defined as follows:

More than one LED can be lit at one time.

Table 8-1. LED Definitions

LED	Label	Comparable Console Message
1	Interface	HP98702 Interface Failure
2	Cable and Transform	Cable/HP98705-66573 Error
3	Transform	HP98705-66573 Error (Also means the 98705-66575 board if used)
4	Frame Buffer	HP98705 FB Memory/Access Error or HP98705 FB Block Move Error
5	Color Map	HP98705 Color Map Error or HP98705 Color Map R/W Error
6	Bus	HP98702 Bus Error or HP98705 Bus Error

1 Interface LED. This LED indicates a problem on the interface board. The interface sends a test to itself and if a reply is not returned, it generates the error message and lights LED number one.

2 Cable and Transform LED. This LED indicates a failure of the Transform and Scan Converter board. The error message means that the error can be due to the GAD bus cable being bad, the Transform and Scan Converter board being bad (either 98705-66573 or 98705-66575), or a bad HP 98702A Interface board as the third possibility.

3 Transform LED. This error is generated when the message can get to the Transform and Scan Converter board, but the data is incorrect. In general, this LED is used in conjunction with LED number two and indicates that the GAD bus cable, or the HP 98702A Interface board are not causing LED two to be lit.

4 Frame Buffer LED. This LED is lit when there is an error on the Frame Buffer board.

5 Color Map LED. Indicates an error on the Color Map board.

6 Bus LED. Indicates that a Graphics Address Strobe (GAS) was sent to the Graphics Processor (any of the three boards may answer) and a Data Transfer ACKnowledge (DTACK) signal was not returned.

On-Line Diagnostics

On-line diagnostics are used to test the graphics functionality of the Graphics Processor. The diagnostics consist of the IODC Error Messages and the use of SAX Diagnostics (for Domain) or On-line Diagnostics (for HP-UX).

STI ROM Error Messages

If console messages are available, they may indicate a console path error. STI error messages will not be displayed on the console screen.

IODC Error Messages

If console messages are available, The IODC tests will be output to the system console. These messages are:

HP98702 Interface Failure	Interface Error Message. This message indicates a problem on the interface board. The interface sends a test to itself and if a reply is not returned, it generates the error message and lights LED number one.
Cable/HP98705-66573 Error	Cable and Transform Error Message. This message indicates a failure of the cable or Transform and Scan Converter board. The message means that the error can be due to the GAD bus cable being bad, the Transform and Scan Converter board being bad (either 98705-66573 or 98705-66575), or a bad HP 98702A Interface as the third possibility. LED two is also lit.
HP98705-66573 Error	Transform Error Message. This error is generated when the test can get to the Transform and Scan Converter board, but the data is incorrect. In general, this message is used in conjunction with *Cable/HP98705-66573 Error* and indicates that the GAD bus cable, or the HP 98702A Interface board is not the problem causing the *Cable/HP98705-66573 Error*. LED three is also lit.
HP98705 FB Memory/Access Error	Frame Buffer Error Message. This message indicates that there is an error on the Frame Buffer board. LED four is also lit.
HP98705 FB Block Move Error	Frame Buffer Error Message. This message indicates that there is an error on the Frame Buffer board. LED four is also lit.
HP98705 Color Map Error	Color Map Error Message. Indicates an error on the color map board. LED five is also lit.
HP98705 Color Map R/W Error	Color Map Error Message. Indicates an error on the color map board. LED five is also lit.
HP98702 Bus Error	Bus Error Message. Indicates that a Graphics Address Strobe was sent to the Graphics Processor (any of the three boards may answer) and a Data Transfer ACKnowledge (DTACK) signal was not returned. LED six is also lit.
HP98705 Bus Error	Bus Error Message. Indicates that a Graphics Address Strobe was sent to the Graphics Processor (any of the three boards may answer) and a Data Transfer ACKnowledge (DTACK) signal was not returned. LED six is also lit.

SAX Diagnostics

Refer to: *Using Domain Diagnostics, Volume 1* Part Number 009329-A02 for information on error messages and the SAX (or GR) diagnostics tests.

On-line Diagnostics

Introduction

The on-line diagnostics provide a means of testing all I/O programs and devices attached to the SPU. This diagnostics system is documented in the *Online Diagnostics Subsystem Manual.*

The 98705A Graphics Subsystem Diagnostic (g98705dg) provides an on-line test for the Graphics Processor. The diagnostic tests all Graphics Processor boards regardless of model configuration.

There are two versions of the diagnostic for the HP 98705A. The HP 9000 Series 700 "converged" on-line diagnostics (DUI version A.02.09) and the Series 300/400 "non-converged" version of the diagnostic (DUI version A.01.05). The "non-converged" diagnostics are used on an SPU running HP-UX software release 7.03 or later (and which supports the on-line diagnostic system).

The "converged" and non-converged diagnostics are slightly different. The differences are:

- The "converged" diagnostics supports the SGC Interface, while the "non-converged" diagnostics supports the DIO-II Interface (HP 98702A).
- Each section of the "converged" diagnostics has its own help message.
- The "converged" diagnostics have a new Section three for the Series 700 Interface test. This section was not used in the "non-converged" diagnostics.
- You do not have to use Single Users Mode (SUM) when using the "converged" diagnostics, as you do with the "non-converged" diagnostics.
- The device file is different for the "converged" diagnostics. The "converged" diagnostic uses a major number of 12, while the "non-converged" diagnostic uses a major number of 10.

  The SGC interface card (used on the Series 700 SPUs) does not have switches. Therefore, a standard **mknod** command is used.

  The minor number for the "non-converged" diagnostics is determined by the switch setting on the interface card.

  Also, if the Series 700 has two slots for the interface card, the minor number requires a different number if the second slot is used (see Chapter 3).

The HP 98705 may be the system console or a graphics peripheral. If possible run the diagnostics from a different terminal than the one being tested. The diagnostic can be run in windows if the unit under test is not in windows.

Hardware Requirements

Before attempting to use the on-line diagnostics on a stand alone system, the system should be capable of passing the STI/IODC tests and displaying a white screen when the MONITOR TEST button on the back of the Graphics Processor is pressed.

Caution This diagnostic destroys all data in the device under test.

The 98705A Graphics Subsystem Diagnostic, g98705dg, tests the graphics interface, and the following minimum set of boards:

- 98705-66570 or 98705-66571 Frame Buffer
- 98705-66573 or 98705-66575 Transform/Scan Converter
- 98705-66574 Color Map

If the Z Buffer is installed, it also will be tested.

While the diagnostic is executing, no input device associated with the HP 98705 under test should be activated (such as, keystrokes, mouse movements, etc).

Help Screens ("Converged" Diagnostics)

A general help screen is available for the On-line Diagnostic after entering the Diagnostic User Interface (DUI). This can be accessed by typing "help g98705dg".

There is a help screen for each section of the HP 98705 Graphics Subsystem Diagnostic. These help screens can be accessed after entering the DUI by entering one of the following commands:

```
help g98705dg sections
```

This help screen gives a quick description of each section diagnostic.

```
help g98705dg section <number>
```

This help screen gives a more detailed description of each section diagnostic.

Help Screens ("Non-converged" Diagnostics)

A help screen is available for the On-line Diagnostic after entering the Diagnostic User Interface (DUI). This may be accessed by typing "help" or a "?".

There are five help screens available in the HP 98705 Graphics Subsystem Diagnostic. These can be accessed after entering the DUI by entering one of the following commands:

```
help g98705dg

help g98705dg sections

help g98705dg parms

help g98705dg commands

run g98705dg dev=/dev/<device_filename> section=1
```

Most of the information in this section of the manual (*Troubleshooting/On-line Diagnostics*) is available in the help screens.

Device File Entries

Before running the HP 98705 Graphics Subsystems Diagnostic (G98705DG), a device file must exist in the operating system. This is entered with a `mknod` command. Once in the operating system, it should not require re-entry (unless it is removed for some reason).

"Converged" Diagnostics. A device file with a major number of 12 must exist in the operating system when using the "converged" diagnostics.

A device file is created by executing the following command:

```
mkdir   /dev/diag

/etc/mknod   /dev/diag/crt16   c   12   0xN00000
```

Where "N" is a either a 1 or 2 depending on which slot is used for the interface board in the Series 700. The board will usually be in slot 1.

"Non-converged" Diagnostics. A device file with a major number of 10 must exist in the operating system when using the "non-converged" diagnostics.

Note A major number of 10 is used ONLY for this `mknod` when executing this diagnostic program. Under normal operating conditions, a major number of 12 is used.

A device file is created by executing the following command:

```
/etc/mknod   /dev/<device_filename>   c   10   0xNNNNc0
```

Where `<device_filename>` is any name you choose that is not the same as any existing device filename.

Where NNNN is a function of the switch setting on the 98702-66501 DIO II/GAD Interface board. Check the switch setting, then find NNNN value in the following table.

Setting	NNNN	Setting	NNNN
00000	——	10000	1040
00001	0140	10001	1140
00010	0240	10010	1240
00011	0340	10011	1340
00100	0440	10100	1440
00101	0540	10101	1540
00110	0640	10110	1640
00111	0740	10111	1740
01000	0840	11000	1840
01001	0940	11001	1940
01010	0a40	11010	1a40
01011	0b40	11011	1b40
01100	0c40	11100	1c40
01101	0d40	11101	1d40
01110	0e40	11110	1e40
01111	0f40	11111	1f40

Note A Setting of 00000 is not allowed.

The default setting on a new card is 00001 (select code 133-135).

Also, it may be necessary to increase some of the HP-UX tunable system parameters due to the size of DIO II mapping for the HP 98705 Graphics Processor. See the section for the HP 98705 in the *Starbase Device Drivers Library* for the minimum values for these tunable parameters.

Running the Diagnostic

You must be superuser (or have a security level which will allow access to the programs) to run the diagnostic programs.

The diagnostic can automatically determine the hardware configuration (or the user can supply the configuration manually). When automatic configuring is selected, the user should verify the reported unit configuration to insure valid test results. Certain hardware failures will prohibit use of automatic configuring. In this case the user should specify the configuration explicitly.

While running the diagnostics, visual patterns will be generated and sent to the screen. These are a product of the tests and are not necessarily for your evaluation.

To start running the diagnostic, enter one of the following commands:

"Converged" diagnostics

```
/usr/diag/bin/DUI
```

"Non-converged" diagnostics

```
/usr/diag/bin/dui
```

This causes the Diagnostic User Interface (DUI) program to begin execution. The following message will be printed on the system console when using the converged diagnostics:

```
THE DIAGNOSTIC MONITOR IS REMOVING PDEV (1.0.0) FROM SYSTEM USE
```

The display will show (depending on whether the "converged" or "non-converged" diagnostic is used):

```
****************************************************************
******                                                    ******
******                ONLINE DIAGNOSTIC SYSTEM            ******
******                                                    ******
****** (C) Copyright Hewlett Packard Co. 1987, 1989, 1990  ******
******                 All Rights Reserved                ******
******                                                    ******
******             DUI version A.02.09                    ******
******        Diagnostic Monitor Version  A.02.18         ******
******                                                    ******
****************************************************************

   Type "HELP" for assistance.

DUI 1>
```

Figure 8-2. "Converged" On-line Message

```
****************************************************************
******                                                    ******
******              ONLINE DIAGNOSTIC SUBSYSTEM           ******
******                                                    ******
******            (C) Hewlett Packard Corporation         ******
******                                                    ******
******                   DUI version A.01.05              ******
******                                                    ******
****************************************************************

DUI 1>
```

Figure 8-3. "Non-converged" On-line Message

The "non-converged" diagnostic MUST be run in single user mode (SUM). To enter single user mode, type:

```
mode sum
```

At this point you can run the diagnostics or call the help messages. To call help messages invoke the commands listed in the *Help Screens* section.

To run the entire diagnostic, execute one of the following commands:

"Converged"

```
run   g98705dg   ldev=/dev/diag/crt16
```

"Non-converged"

```
run   g98705dg   dev=/dev/<device_filename>
```

To run section diagnostics, specify the sections you desire to run. The following are examples of running just one or several sections:

"Converged"

```
run   g98705dg  ldev=/dev/diag/crt16   section=3

run   g98705dg   ldev=/dev/diag/crt16   section=10,11,12
```

"Non-converged"

```
run   g98705dg   dev=/dev/<device_filename>   section=4

run   g98705dg   dev=/dev/<device_filename>   section=10,11,12
```

See the list of sections in the *Diagnostic Section Descriptions* to determine what sections you may want to run.

Assuming you run the entire diagnostic, the following messages will be displayed next:

```
****************************************************************
******                                                    ******
******                      G98705DG                      ******
******                                                    ******
******          (C) Hewlett Packard Corporation           ******
******                Version  A.03(.03 or .04)           ******
******                                                    ******
****************************************************************

Welcome, Today is Tue Apr 20 08:56:19 1990


DUI>
```

Figure 8-4. G98705DG Message

The diagnostic then prompts the user with some questions (typically the default choices are used by pressing the [Return] key).

The "non-converged" diagnostic asks (The "converged" diagnostic automatically finds the answer):

```
Are you running the diagnostic from the 98705A you are testing? (y/n) [y]
```

Then, either of the "converged" or "non-converged" diagnostic will ask:

```
Do you want this program to determine the unit configuration? (y/n) [y]
```

If "y" is chosen, the program will attempt to identify the hardware configuration. If this procedure fails, the diagnostic will return again to the above prompt.

If "n" is chosen for the above question, the program will prompt the user with questions to determine the configuration.

Once the configuration has been determined, the program will show it to the user and ask if you want to continue.

Example:

```
98705-66582 Present  (SGC Interface)
      or
98702-66501 Present  (DIO II Interface)

98705-66573 Present  (Transform Engine and Scan)
98705-66571 Present  (Frame Buffer 0 and 1)
98705-66572 Present  (Z Buffer)
98705-66574 Present  (Color Map)

Do you wish to continue with this unit configuration? (y/n) [y]
```

If you answer "n", the program will return to the questions concerning determining the configuration.

If you answer "y", the program will start executing the diagnostics. The user will be notified when a section is begun, when the section ends, and whether the test passed or failed.

Examples:

```
Begin Section 3

No failures were detected.

End of Section 3


Begin Section 4

No failures were detected.

End of Section 4


Begin Section 10

No failures were detected.

End of Section 10

     .

     .

     .

Begin Section 31


*** ERROR IN SECTION 31
*** ERROR OCCURRED DURING COLOR MAP - FRAME BUFFER 0 TESTING (GS3DERR 98)

End of Section 31
```

At the end of the tests, a table will be printed showing the results of each section, whether the test passed or failed, and whether each board passed or failed each section test. A key to table entries is also provided.

In the following example, note that test sections 1, 2, and 40 are not run. Look at the *Diagnostic Section Descriptions* of these sections and you will see that they are not diagnostic type tests. Also, if the Z Buffer board (or Frame Buffer FB 1) is not in the system configuration, tests related to those boards will not be run.

Also note, that section tests 31 and 33 failed. By looking at the *Diagnostic Section Descriptions* for these sections, and correlating that with the table information, you can determine that the Color Map board or Frame Buffer board are the most probable causes of the failure.

Example:

```
The following table summarizes results of the diagnostic
  sections.  Here is the key to table entries:

  [FFF]   Testing this FRU was a major goal (section FAILED)
  [ppp]   Testing this FRU was a major goal (section PASSED)
  [ F ]   Exercising a portion of this FRU was necessary
            to achieve the section goal (section FAILED)
  [ p ]   Exercising a portion of this FRU was necessary
            to achieve the section goal (section PASSED)
  [ - ]   This FRU was not exercised
```

Result:	FRU Tested:	ITF	TE-SC	FB	Z	CM
Section	3 Passed	ppp	-	-	-	-
Section	4 Passed	ppp	-	-	-	-
Section	10 Passed	p	ppp	-	-	-
Section	11 Passed	p	ppp	-	-	-
Section	12 Passed	p	ppp	-	-	-
Section	20 Passed	p	p	ppp	-	-
Section	21 Passed	p	p	ppp	-	-
Section	22 Passed	p	p	ppp	-	-
Section	23 Passed	p	p	ppp	-	-
Section	24 Passed	p	p	ppp	ppp	-
Section	25 Passed	p	p	ppp	ppp	-
Section	30 Passed	p	p	-	-	ppp
Section	31 FAILED	F	F	FFF	-	FFF
Section	32 Passed	p	p	ppp	-	ppp
Section	33 FAILED	F	F	FFF	-	FFF
Section	39 Passed	p	ppp	ppp	ppp	-

Type "exit" to get out of the diagnostic program.

When leaving the diagnostic and in "converged" diagnostics, the following message will be sent to the system console:

```
THE DIAGNOSTIC MONITOR IS RETURNING PDEV (1.0.0) TO SYSTEM USE
```

Stopping the Diagnostic

If the Break key is pressed while the diagnostic program is running, the program will stop. The test that is currently running will fail, and you will have to press Shift Control Reset (simultaneously) to reset the Graphics Processor and restore the screen to a non-diagnostic presentation.

Diagnostic Section Descriptions

Section 1	Help Information—Used to get information about running the test.
Section 2	Reserved for future use.
Section 3	Series 700 Interface Test (98705-66582 Interface Board).
Section 4	Series 300/400 Interface Test (98702-66501 Interface Board).
Section 10	Transform Engine Test—Tests the Transform Engine for functionality.
Section 11	Scan Converter/Transform Engine Test—Tests the interface between the Transform Engine and the Scan Converter by testing DCRAM from the Transform Engine side. The hardware tested is primarily the 98705-66573 board (Transform/Scan Converter in HP Models 98705A and 98705B).
Section 12	Scan Conversion Logic Test—Tests the LGB and DCRAM Scan Converter registers from the Scan Converter side.
Section 20	Frame Buffer Controller Logic Test—Tests miscellaneous Frame Buffer logic circuitry and control registers.
Section 21	Frame Buffer 0 RAM Test—Tests the 8 planes of RAM on the 8 Plane Frame Buffer board (98705-66570) or the first 8 planes of a 16 Plane Frame Buffer board (98705-66571).
Section 22	Frame Buffer 1 RAM Test—Tests the second 8 planes of RAM on a 16 Plane Frame Buffer board (98705-66571).
Section 23	Overlay RAM Test—Tests the overlay RAM on the Frame Buffer board (either 98705-66570 or 98705-66571).
Section 24	Z Buffer RAM Test—Utilizes the Frame Buffer Controller to test the Z Buffer RAM.
Section 25	Frame Buffer System Test—Tests theFrame Buffer system and its feature set. Includes the Frame Buffer Controller, Frame Buffer and Overlay Planes, and the Z Buffer assembly.
Section 30	Color Map Logic Test—Tests the Color Map logic circuitry and associated control registers.
Section 31	Color Map - Frame Buffer 0 Test—Tests the Color Map data path from Frame Buffer 0.
Section 32	Color Map - Frame Buffer 1 Test—Tests the Color Map data path from Frame Buffer 1.
Section 33	Overlay RAM Test—Tests the Color Map data path from the overlay planes.
Section 39	Transform Engine, Scan Converter, and Frame Buffer Test—Tests the graphics pipe from the Transform Engine, through the Scan Converter, to the Frame Buffer. All available Frame Buffer memory, overlay plane memory, and Z Buffer memory is used.
Section 40	Visual Test—Draws a series of patterns on the monitor. This section does not check the images or report failures. As the name implies, it provides a visual output for the user to observe and verify that the function of the video portion of the Color Map assembly and the monitor are operational.

9

Replaceable Parts

Introduction

This chapter contains lists of replacement parts and exchange assemblies included in the HP 98705 Graphics Display Controller (GDC). Parts are available from Hewlett-Packard Support Materials Organization at this address:

Support Materials Organization (SMO)
Hewlett-Packard Company
8050 Foothills Boulevard
Roseville, California, 95678

Telephone (916) 786-8000

Part numbers in the form 98705-69xxx refer to rebuilt boards that are available on an exchange basis. Part numbers in the form 98705-66xxx, -67xxx, or -68xxx are new boards. Unloaded printed circuit boards are not available.

Replaceable Parts

Table 9-1. Fuse

Fuse	Part Number
Fuse	2110-0056

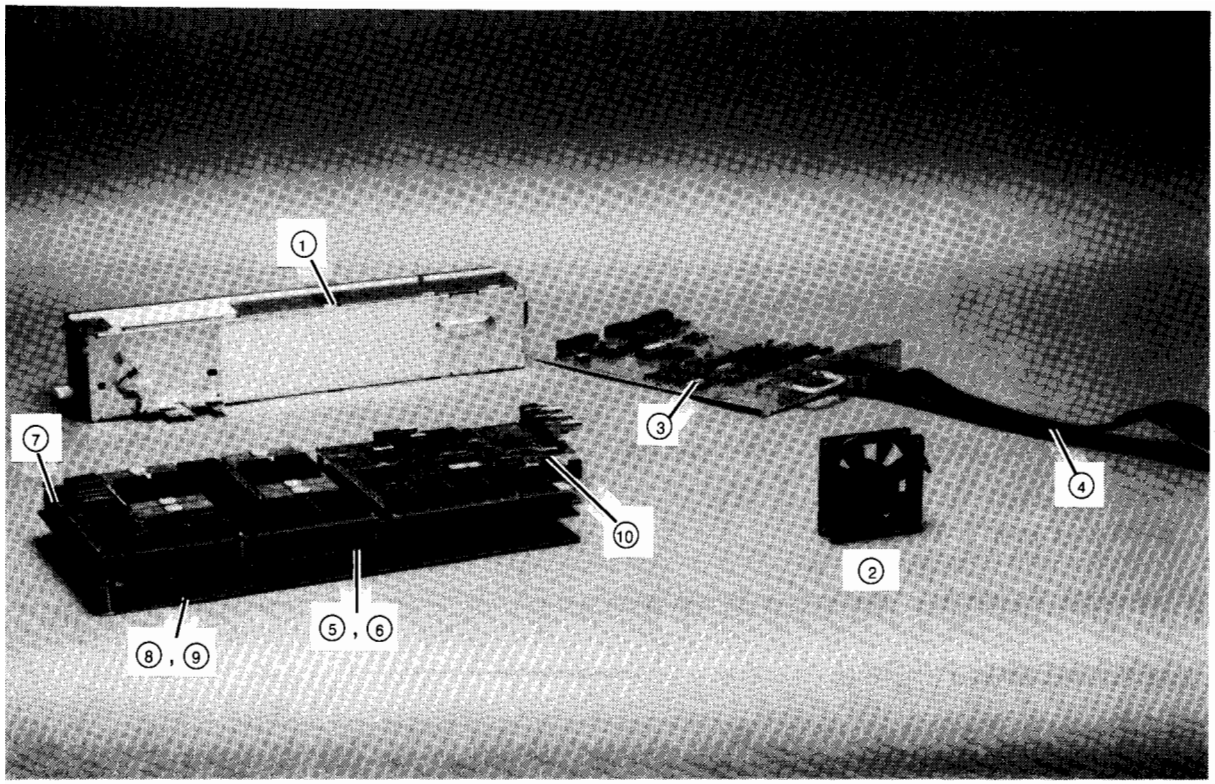


Figure 9-1. HP 98705 Electrical/Electronic Parts

Table 9-2. Electrical/Electronic Parts

Drawing Number	HP Part Number	Description	Exchange
1	0950-2022	Power Supply	
2	3160-0595	Fan	
3	98705-66582	SGC Interface	
	98702-66501	DIO II/GAD Interface	X
4	98702-61601	GAD Cable	
5	98705-66570	Frame Buffer 8 Plane	X
6	98705-66571	Frame Buffer 16 Plane	X
7	98705-66572	Z Buffer	X
8	98705-66573	Transform/Scan Converter—Models A and B	X
9	98705-66575	Transform/Scan Converter—Model C	X
10	98705-66574	Color Map	X

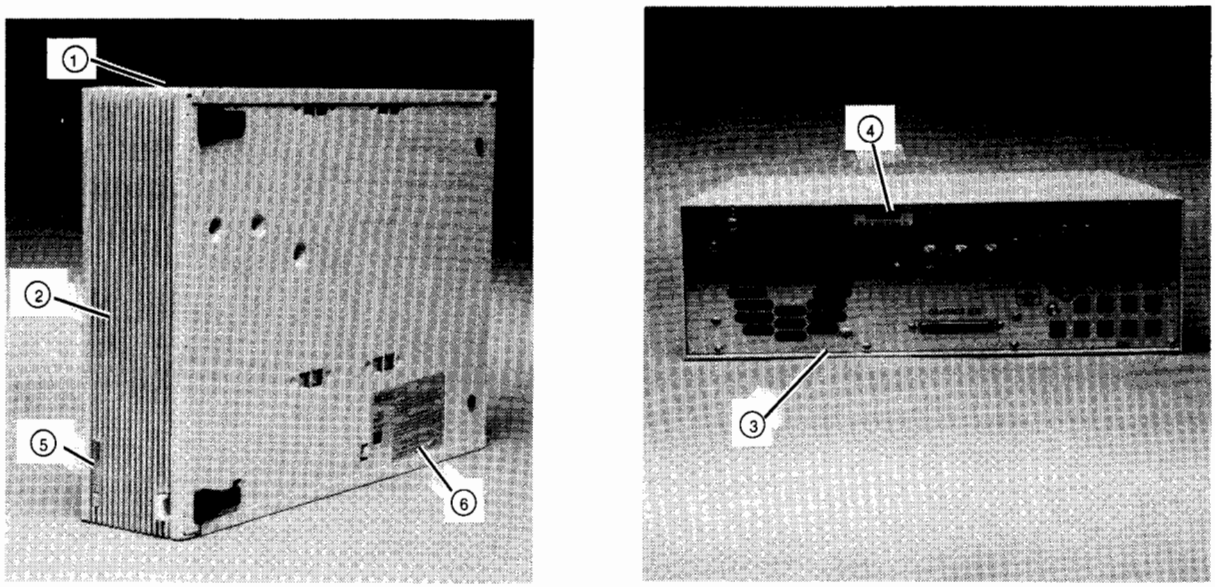


Figure 9-2. HP 98705 Case Parts

Table 9-3. Case Parts

Drawing Number	HP Part Number	Description
1	5001-9046	Case—No Grill
2	98705-40201	Horizontal Grill
	98705-40202	Vertical Grill
3	98705-00101	Rear Panel
4	7121-4733	Label/Serial Plate
5	98705-84001	Label/Name Plate
6	98705-84002	Label/Voltage Select

Note When ordering a new case (or a new grill) the user must order both the grill and the case and put them together. You cannot remove the old grill from the case without damaging both beyond usability.

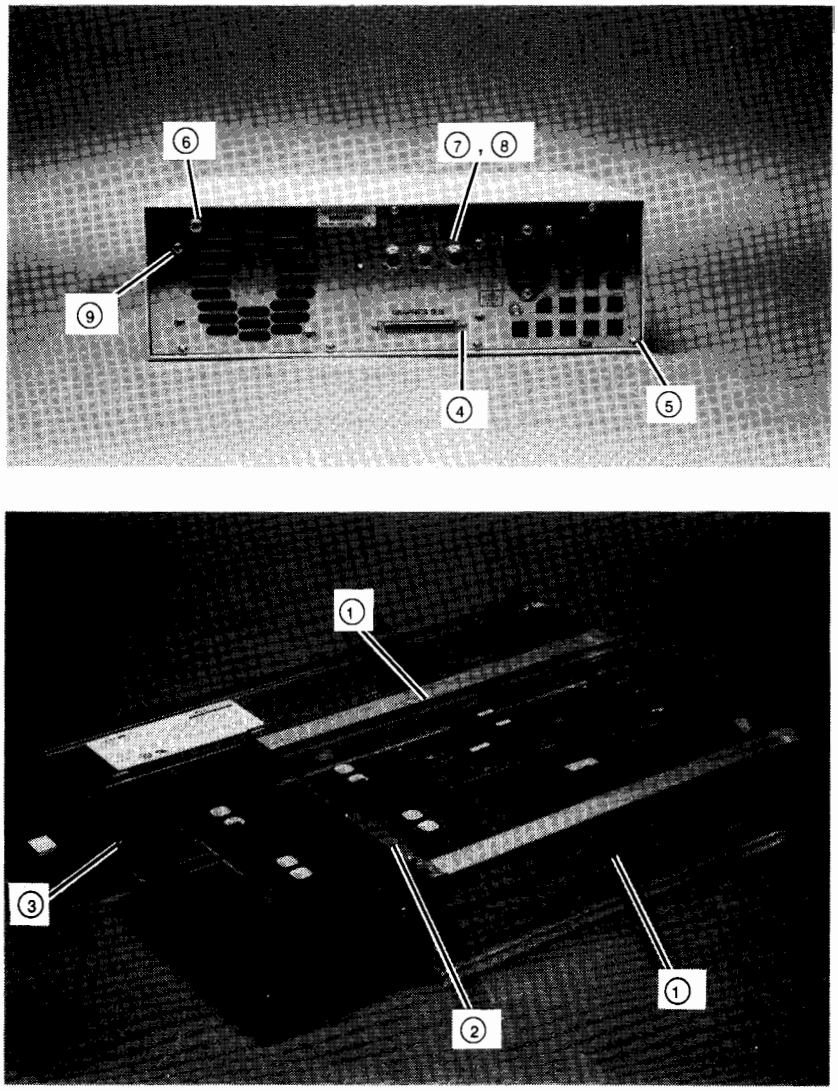


Figure 9-3. HP 98705 Mounting Hardware

Table 9-4. Mounting Hardware

Drawing Number	HP Part Number	Description	Quantity
1	98705-01202	Board Support—Aluminum	2
2	98705-01201	Bracket/Support	1
3	0515-0825	Screw—M 4x7 mm	5
4	0515-1727	Screw—M 2.5x12 mm	2
5	0515-1851	Screw—M 3x5 6mm Lg	7
6	0624-0562	Screw—10-32	2
7	1250-2075	Nut—Hex	3
8	2190-0054	Washer—LK	3
9	0515-0225	Screw—M 3.5x10mm Lg	4

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Reference

Introduction

Use this section to keep reference notes and other reference documents.

Reference Documents

Table 10-1. Graphics Processor Documents

98705-90031	HP 98705A/B/C Hardware Support Manual
98705-90040	HP 98705A/B/C CE Handbook (insert)
98705-90604	HP 98705A/B/C Installation Guide

Table 10-2. Training Materials for CE92-98705A

98705+49A-90002	U.S. Internal Kit
98705+49A-91002	European Internal Kit
98705+49A-90101	Stand-alone Kit (workbook & final)

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Product History

Introduction

Use this section to store changes to system configuration, installation procedures, modifications, and update information applying to your HP 98705A, B, or C systems.

* In early 1991 the SGC interface allowed the HP 98705 Graphics Processor to be connected to the HP 9000 Series 700 computers. The online diagnostic program was also changed to the "converged" diagnostics for the Series 700.

12

Diagrams

Introduction

This section is provided for storage of system maps, network diagrams, and other information that is not stored elsewhere.