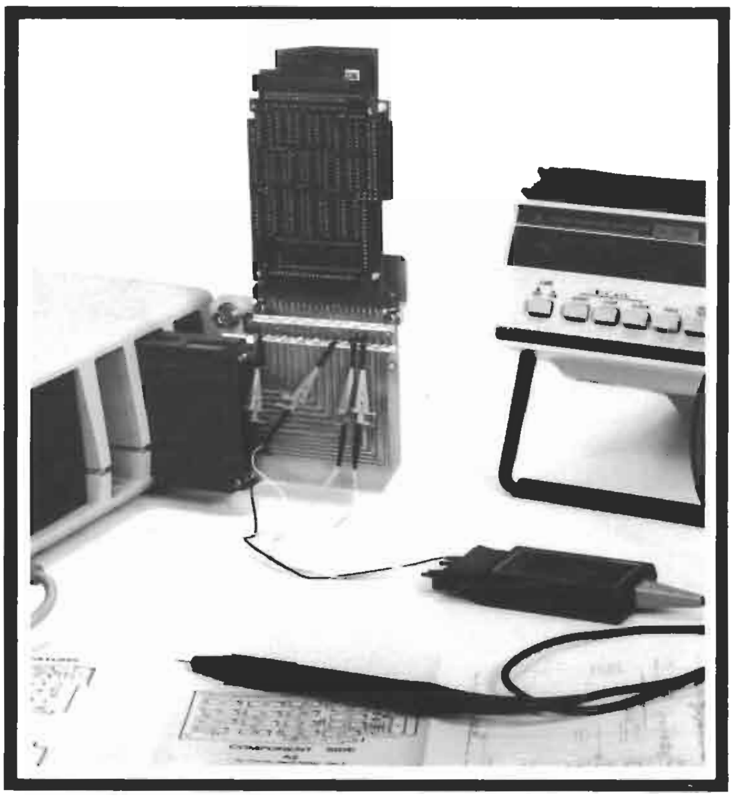
Series 9800 Desktop Computers

98046B Interface Installation and Service

For the HP 9835A/B and 9845B/C



HEWLETT PACKARD

98046B Interface
Installation and Service Manual

Hewlett-Packard Desktop Computer Division
3404 East Harmony Road, Fort Collins, Colorado 80525

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Printing History

New editions of this manual will incorporate all material updated since the previous edition. Update packages may be issued between editions and contain replacement and additional pages to be merged into the manual by the user. Each updated page will be indicated by a revision date at the bottom of the page. A vertical bar in the margin indicates the changes on each page. Note that pages which are rearranged due to changes on a previous page are not considered revised.

The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates which are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

March 1980...First Edition
December 1980...Second Edition. Updated pages: v, vi, 2-1, 2-2, 2-5 thru 2-8, 3-1 thru 3-4, 4-5, 4-6, 4-9 thru 4-22, 5-1 thru 5-4

Chapter 1
General Information

Introduction

This is the Installation and Service Manual for the HP 98046B Data Communications Interface. The primary purpose of this manual is to provide information to help in repairing an interface that is known to be malfunctioning. In addition, it describes how to install the Interface into a Data Communications system containing a 9835A/B or a 9845B/C. It shows the user how to re-configure the option cable to allow it to work with a particular set of modems. Once the installation has been done, the user can consult the Data Communications ROM Manual for information on how to use the system.

Before the repair technician uses this manual, the system user should have verified that the interface is indeed malfunctioning. This is done by using the software aids described in the appropriate data communications programming manual.

- Chapter 1 introduces the manual, gives specifications, and the options that are available.
- Chapter 2 shows how to install the interface into the 9835A/B and the 9845B/C.
- Chapter 3 contains a detailed description of the electronic functions of the interface.
- Chapter 4 describes how to isolate a problem to a particular component using signature analysis and the test program.
- Chapter 5 gives the overall schematic diagram and a list of replaceable parts.

Specifications

Weight:	790 grams
Cable Length:	2 metres
Power:	+5 Volts at 402 ma. +12 Volts at 25 ma. −12 Volts at 46 ma.
Temperature:	0°C to 45°C
Humidity:	0 to 80%

Generally speaking, any environment in which an HP desktop computer can operate is also acceptable for the 98046 Serial Interface. If extreme environmental conditions exist, or if there is a question about specifications not listed here, consult your local HP Sales and Service Office.

Cable Options

The standard 98046 Interface is supplied with a female RS-232 connector. The 98046 Opt 001 Interface is supplied with a male RS-232 connector. Table 1-1 describes the options. The Data Communications Basics Manual explains the difference between Data Communications Equipment and Data Terminal Equipment.

Table 1-1. Options

Option	Connector	Purpose
Standard	25 Pin Female RS-232C	For Connecting a 9835A/B or 9845B/C to Data Terminal Equipment.
001	25 Pin Male RS-232C	For Connecting a 9835A/B or 9845B/C to a Modem or to Other Data Communications Equipment.

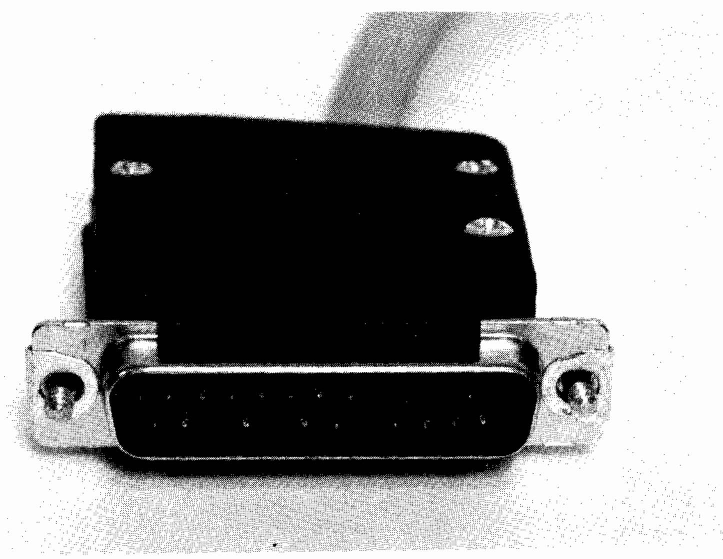


Figure 1-1. 25 Pin Male Connector for RS-232C

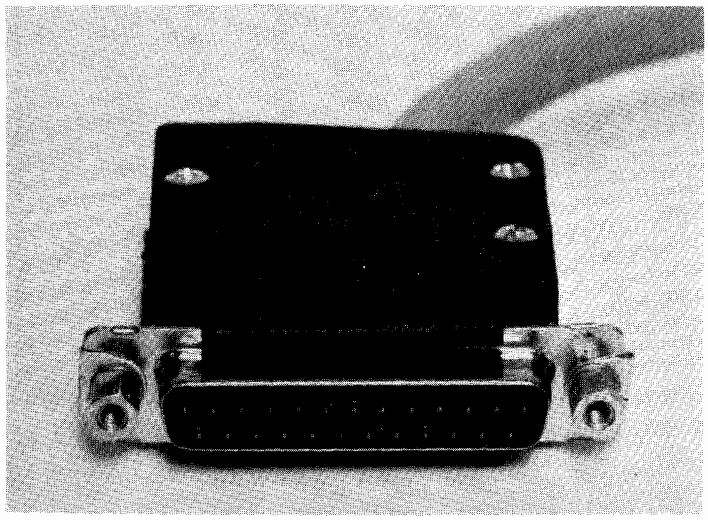


Figure 1-2. 25 Pin Female Connector for RS-232C

Figure 1-3 shows a typical point to point installation using the 98046 Interface. Note that one computer uses the Standard Interface while the other is using Option 001.

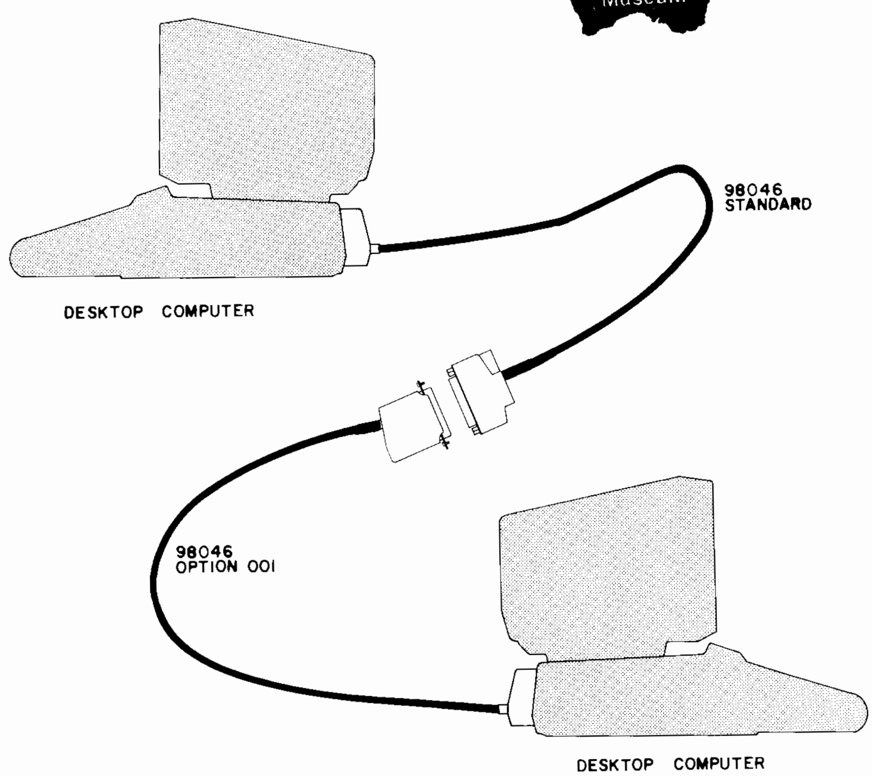


Figure 1-3. Point-to-Point System

Figure 1-4 shows a typical installation using modems to convey information over commercial telephone lines. Both the desktop computer and the remote computer in this example use Option 001.

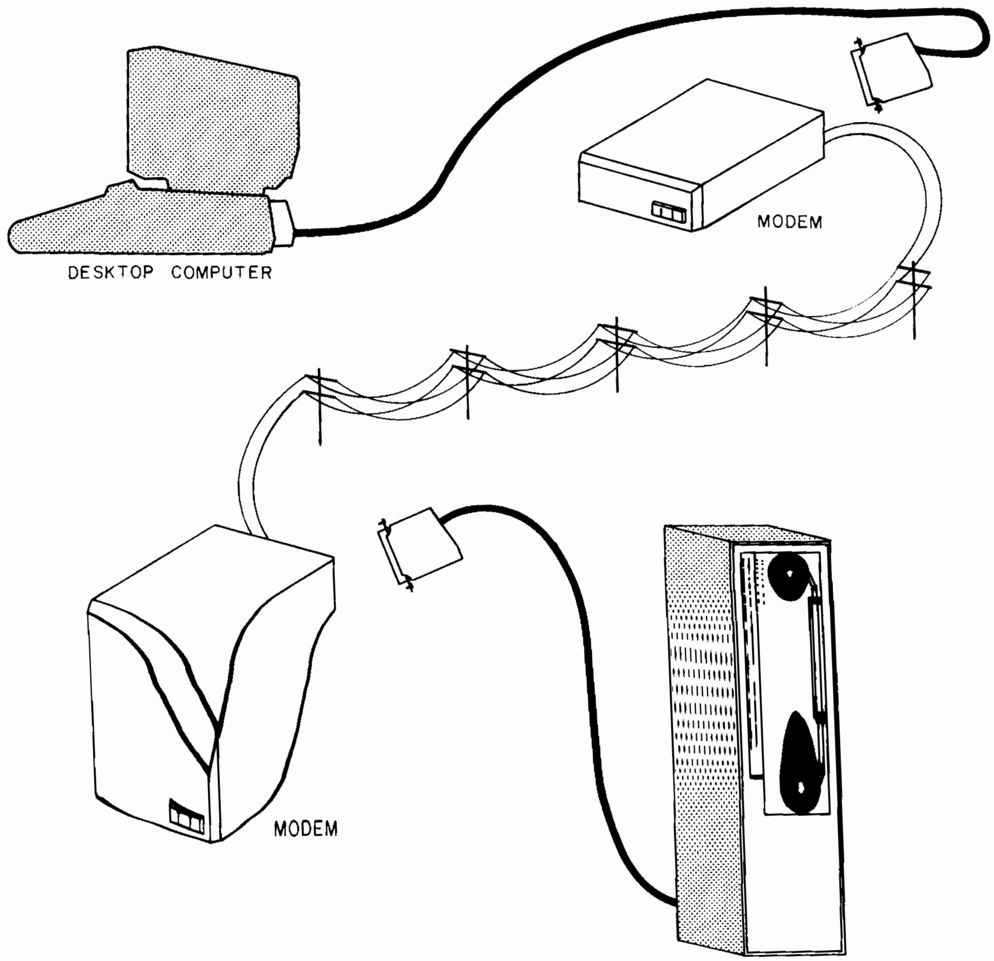


Figure 1-4. Typical Data Communication System with Modems

Chapter 2
Installation

Connecting to the Computer

To connect the 98046 Serial Interface to an HP desktop computer, the interface must be plugged into an I/O slot, and the appropriate ROM must be plugged into an Option ROM slot.

CAUTION
POWER TO THE DESKTOP COMPUTER MUST BE OFF WHEN INSERTING OR REMOVING ROMS OR INTERFACES. HAVING POWER ON FOR EITHER OPERATION COULD DAMAGE EQUIPMENT.

Here is a summary of the Data Communication ROMs and their use.

Desktop Computer	ROM Part Number	Description
9835	98317A	Basic Data Communications ROM
	98318A	RJE Bi-synchronous ROM
9845	98417A	Basic Data Communications ROM
	98418A	RJE Bi-synchronous ROM

Connecting to the 9835A/B

To install the interface:

- Insert the interface housing into any of the three I/O slots in the back of the computer. See Figure 2-1.
- Before switching power on, ensure that the interface housing is firmly seated in the slot, and that the latch on top has engaged the case of the computer.

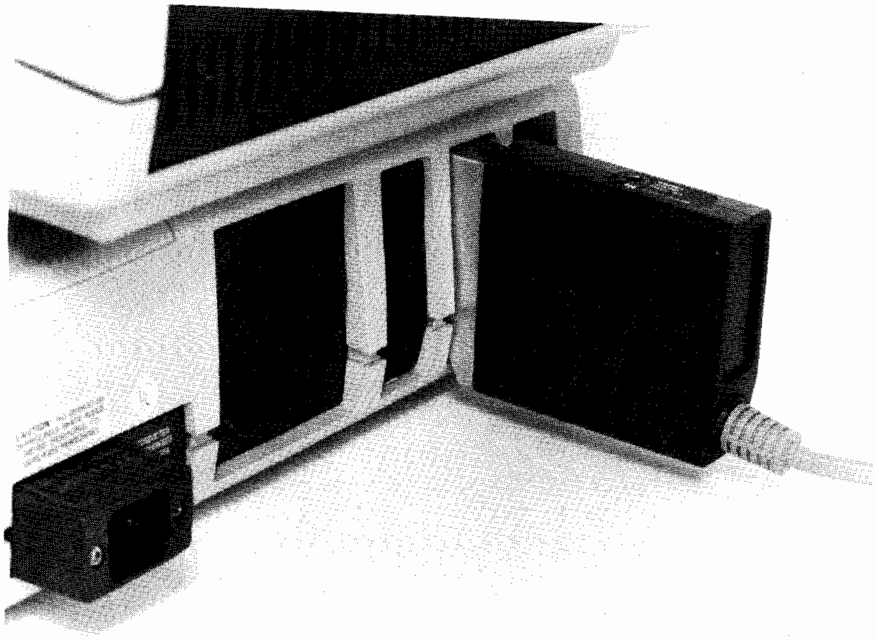


Figure 2-1. Inserting the Interface Housing into the 9835 I/O Backplane.

Connecting to the 9845B/C

To install the interface:

- Insert the interface housing into any of the four I/O slots in the back of the computer. See Figure 2-2.
- Before switching power on, ensure that the interface housing is firmly seated in the slot, and that the latch on top has engaged the case of the computer.

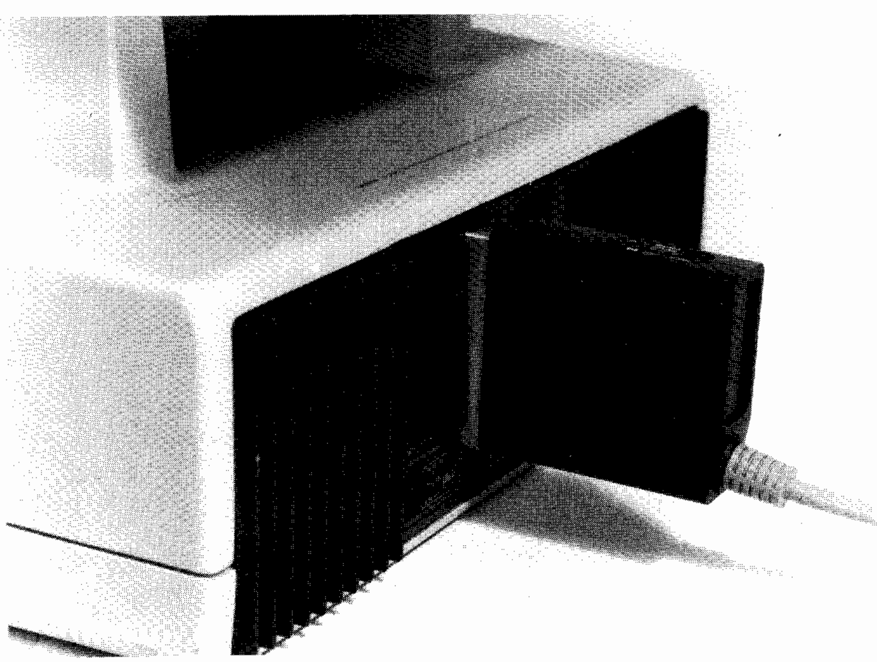


Figure 2-2. Inserting the Interface Housing into the 9845 I/O Backplane.

The Select Code

The 98046 Serial Interface responds to two adjacent select codes to allow it to handle the transmit function and the receive function as separate processes. It is intended that the switch be set to an even numbered select code, either 2, 4, or 6; at the factory it is set to select code 4. This select code is for the transmit function, and the next higher select code is for the receive function.

NOTE

The Interface is not intended to be used with a select code higher than 7. Assigning it a high level select code (8-15) could result in a system deadlock in which the computer appears to be inoperative. This can be recovered by pressing CONT'L and STOP simultaneously or by turning power to the computer OFF and back ON.

Setting the Select Code

The select code is set by rotating a switch on the Interface as shown in Figure 2-3. A small arrow on the switch rotor points to the select code. Table 2-1 shows the results of the available switch settings. As the table shows, select codes 0 through 7 are low level interrupts; select codes 8 through 15 are high level interrupts. The significance of this is explained more fully in Chapter 3.

Table 2-1. Select Codes

Switch Settting	Transmit Select Code	Receive Select Code	Interrupt Level	Comments
0 or 1	DO NOT USE		Low	Conflicts with Keyboard operations
2 or 3	2	3	Low	
4 or 5	4	5	Low	Set at the factory
6 or 7	6	7	Low	
8 or 9	8	9	High	
10 or 11	10	11	High	
12 or 13	12	13	High	Could conflict with 9845 graphics option
14 or 15	DO NOT USE		High	Conflicts with tape cartridge operations

When setting the select code, make sure that neither select code on the 98046 conflicts with that of another device. Possible conflicts from within the computer are shown in Table 2-1. Conflicts from other peripherals must be resolved at the time of installation.

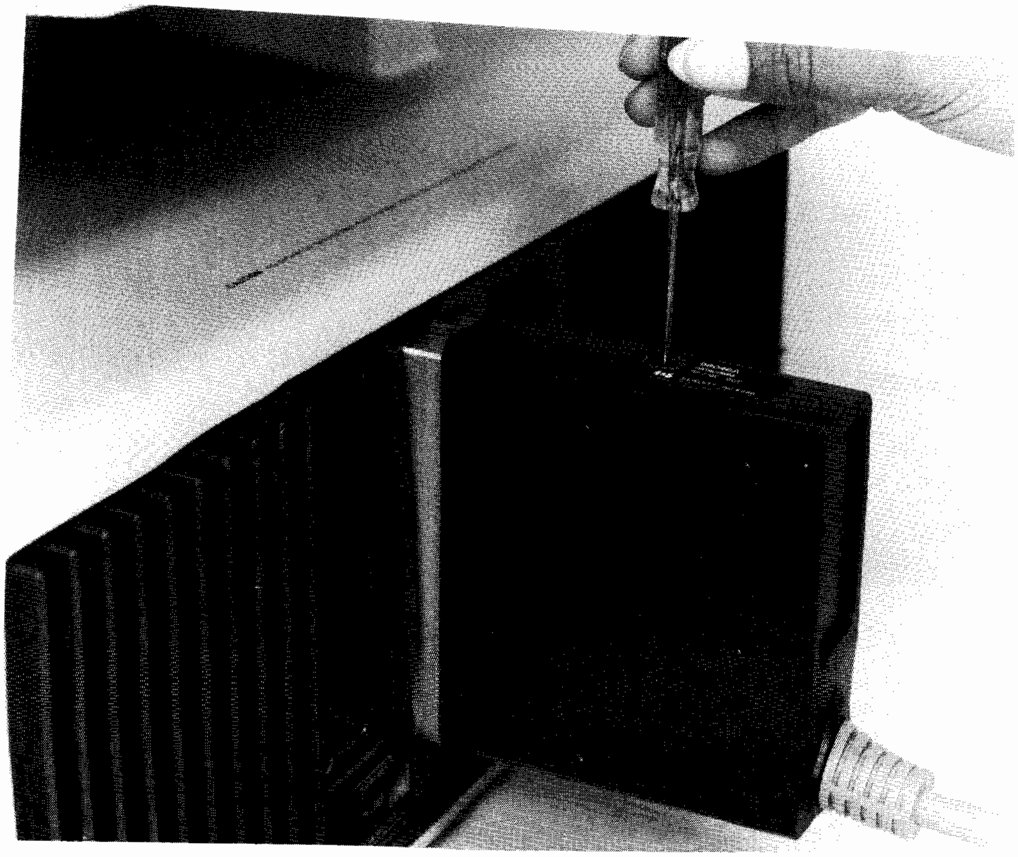


Figure 2-3. Setting the Select Code.

Re-Configuring the Cable

Individual modems may have features that are not compatible with the interface cable which is furnished with the 98046. These features may require re-configuring of the interface cable before connecting it to the modem. The 32 pin connector that is on the interface housing end of the cable can be re-configured in the field if an application requires it. Re-configuring the cable is done by removing a wire from one pin position on the 32 pin connector, and re-inserting it into another pin position. Refer to the interface schematic diagram in Chapter 5 for the interface connector pin numbers and their destinations.

CAUTION

RE-CONFIGURING THE INTERFACE CABLE WILL CAUSE THE TEST PROGRAM TO PRODUCE MISLEADING RESULTS. THIS IS BECAUSE THE STANDARD OR OPTION 001 TEST CONNECTOR THAT IS USED IN CONJUNCTION WITH THE TEST PROGRAM HAS BEEN WIRED TO COINCIDE WITH THE STANDARD CABLE CONFIGURATION. TO AVOID THIS, THE INTERFACE CABLE SHOULD BE CLEARLY MARKED AS HAVING BEEN RE-CONFIGURED, SO THAT SUBSEQUENT USERS CAN CHANGE IT BACK TO THE STANDARD CONFIGURATION PRIOR TO RUNNING THE TEST PROGRAM.

The pin which is crimped onto each wire is held in place in the connector body by nylon locking rod (see Figure 2-4). There are two of these locking rods; they run the length of each side of the connector body.

To re-configure the cable:

- Use a pair of needle-nosed pliers to withdraw the locking rod. Do not withdraw the rod any further than necessary, since re-inserting it can be difficult.
- When the locking rod has been sufficiently withdrawn, the wire and pin can be pulled from its position in the connector body.
- Re-insert the wire into the desired pin position, withdrawing the appropriate locking rod as necessary.
- Re-insert both locking rods. The flared heads should be flush with the end of the connector body.

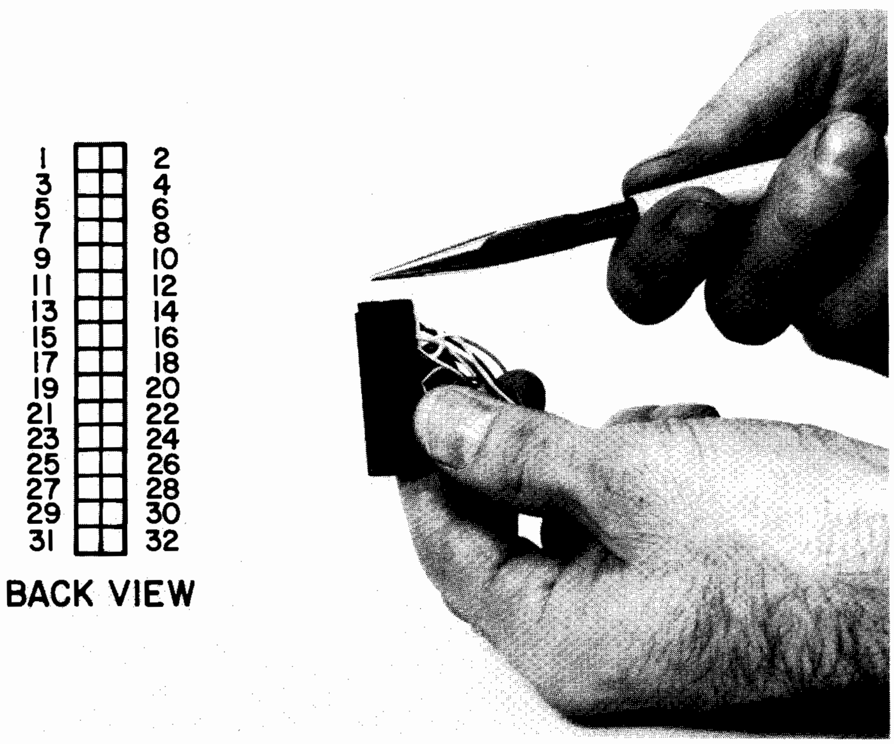


Figure 2-4. Removing a Wire From the Interface Connector

Pin	Cable Wire Colors	RS-232C	V.24	Name	I/O
1	DRAIN WIRE	AA	101	Protective Ground	—
2	RED	BA	103	Transmitted Data	Input
3	ORN	BB	104	Received Data	Output
4	YEL	CA	105	Request to Send	Input
5	GRN	CB	106	Clear to Send	Output
6	BLU	CC	107	Data Set Ready	Output
7	VIO	AB	102	Signal Ground	—
8	GRA	CF	109	Data Carrier Detect	Output
9					
10					
11					
12	WHT/BRN	SCF	122	Secondary Carrier Detect	Output
13					
14	WHT/BLU			New Sync/Secondary Transmit Data	Not Connected
15	BLK	DD	115	Receiver Timing (DCE)	Output
16					
17	BRN	DB	114	Transmitter Timing (DCE)	Output
18					
19	WHT	SCA	120	Secondary Request to Send	Input
20	WHT/BLK	CD	108.2	Data Terminal Ready	Input
21					
22	WHT/RED	CE	125	Ring Indicator	Output
23	WHT/ORN			Data Rate Select	Not Connected
24	WHT/YEL	DA	113	Transmitter Timing	Input
25	WHT/GRN			Out of Service	Not Connected

Table 2-3. Pin Functions for Option 001 Cable at RS-232 Connector

Pin	CABLE Wire Colors	RS-232C	V.24	Name	I/O
1	DRAIN WIRE	AA	101	Protective Ground	—
2	RED	BA	103	Transmitted Data	Output
3	ORN	BB	104	Received Data	Input
4	YEL	CA	105	Request to Send	Output
5	GRN	CB	106	Clear to Send	Input
6	BLU	CC	107	Data Set Ready	Input
7	VIO	AB	102	Signal Ground	—
8	GRA	CF	109	Data Carrier Detect	Input
9					
10					
11					
12	WHT/BRN	SCF	122	Secondary Carrier Detect	Input
13					
14	WHT/BLU			New Sync/Secondary Transmit Data	Not Connected
15	BLK	DD	115	Receiver Timing (DCE)	Input
16					
17	BRN	DB	114	Transmitter Timing (DCE)	Input
18					
19	WHT	SCA	120	Secondary Request to Send	Output
20	WHT/BLK	CD	108.2	Data Terminal Ready	Output
21					
22	WHT/RED	CE	125	Ring Indicator	Input
23	WHT/ORN		111	Data Rate Select (DTE)	Output
24	WHT/YEL	DA	113	Transmitter Timing (DTE)	Output
25	WHT/GRN			Out of Service	Not Connected

NOTES

Chapter 3
Theory of Operation

Introduction

This chapter explains how the circuitry in the 98046 Data Communications Interface works. Circuits that connect directly with the desktop computer are discussed first. The computer's I/O processes are discussed, followed by an explanation of how each interface circuit interacts with them. The discussion then goes to the major devices on the interface: the microcomputer, the Universal Synchronous/Asynchronous Receiver/Transmitter (USART), and the First In/First Out memories (FIFO's). Finally, the flow of data is followed through the interface; first, data to be transmitted, then received data.

The text in this chapter refers several times to particular components on the interface. It may be easier to follow these discussions if the schematic diagram, Figure 5-1, is folded out so that it can be consulted while reading this chapter.

A reference to a particular component is preceded by either A1 or A2 to signify which printed circuit assembly contains the component.

CAUTION

IT IS INTENDED THAT THE 98046 BE CONTROLLED ONLY BY THOSE COMMANDS AND STATEMENTS MADE AVAILABLE WITH THE DATA COMMUNICATIONS ROMS. AT SEVERAL PLACES THE TEXT REFERS TO OTHER COMMANDS WHICH CONTROL INDIVIDUAL I/O REGISTERS. THESE COMMANDS CAN ONLY BE EXECUTED BY A DESKTOP COMPUTER HAVING AN I/O ROM. THEY ARE INCLUDED SOLELY FOR THEIR USE AS TROUBLESHOOTING AIDS. USE OF THESE OR SIMILAR I/O COMMANDS FOR CONTROL PURPOSES CAN PRODUCE UNEXPECTED OR UNDESIRED RESULTS, AND SHOULD THEREFORE BE AVOIDED.

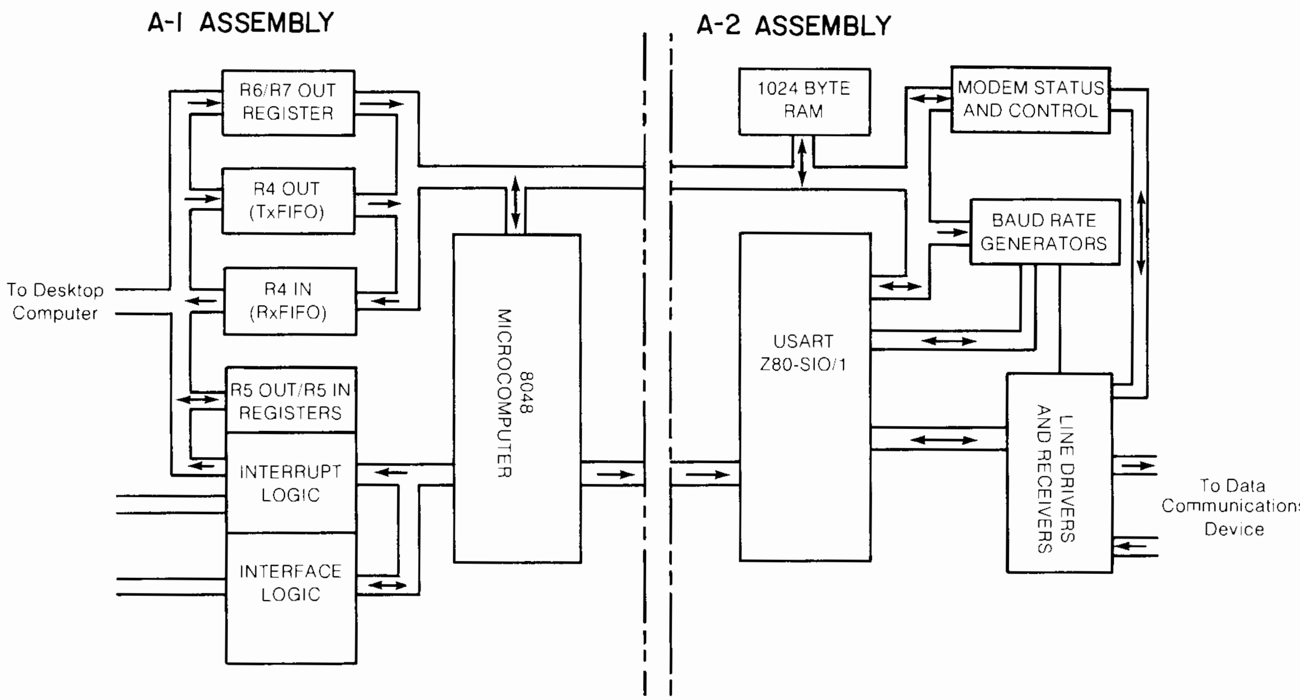


Figure 3-1. 98046 Block Diagram.

Identifying the Peripheral

Peripheral Address Lines

Before doing an I/O operation, either input or output, the computer's operating system causes four bits to be latched into the I/O controller's Peripheral Address register. These serve to identify which I/O device is involved in the forthcoming I/O operation. There are sixteen possible peripheral addresses. These four bits remain on the output of the Peripheral Address register until subsequent I/O operations require them to be changed. The Peripheral Address lines are sensed by each I/O device, where they are compared with that device's select code.

The Select Code

Each I/O device using the I/O bus is assigned a unique select code from 0 to 15.[1] This includes devices inside the computer, such as tape transports, keyboard, printer, and the 9845B graphics option. Conflicts occur if two devices are assigned the same select code. Even if the devices are similar, subtle timing differences can cause errors.

If the peripheral device's select code matches the peripheral address, the device is enabled to perform its part in an I/O operation. All devices with non-matching select codes ignore the activity on the I/O bus and control lines.

The 98046 uses two adjacent select codes, an even select code for the transmit operations, and the next higher odd select code for receive operations. Chapter 2 describes how to set the select code. The rest of this chapter assumes that the select code switch is set to 4 as is done at the factory.

1 Various programming manuals show select codes ranging from 0 to 16, giving a total of 17 possible select codes. This apparent contradiction is the result of the computer's operating system assigning select code 16 to the CRT. The CRT is not connected to the I/O bus. The operating system correctly interprets I/O commands involving select code 16 into data compatible with the CRT. All this is transparent to the user, who can then treat the CRT as an output device and control its display with I/O commands.

Data Transfer Over the I/O Bus

The computer exchanges information with the interface by means of the sixteen-bit I/O bus. The sequence of events that transfers this information in either direction is called an I/O cycle. It is always initiated and controlled by the desktop computer.

I/O Cycles

I/O cycles result from memory cycles which address one of four pseudo-registers: R4, R5, R6, or R7. The addresses of these registers would indicate that they are within the desktop computer's microprocessor, but they do not exist in the computer. A read operation involving R4 through R7 results in an input I/O cycle; a write to R4 through R7 results in an output I/O cycle. Therefore there must be a register on each I/O device to correspond to whichever pseudo-registers the individual device requires. The Interface Control lines IC1 and IC2 indicate which of the four registers is involved in the I/O cycle. DOUT indicates whether the direction of data flow is in to or out of the computer.

A further word about I/O cycles: there is no handshake involved in the data transfer within each I/O cycle. The signal $\overline{\text{IOSB}}$ defines when the data is valid. If the data is not latched by the receiving device at the end of the $\overline{\text{IOSB}}$ pulse, that data is lost.

Figure 3-2 shows a typical I/O cycle. The $\overline{\text{STM}}$ and $\overline{\text{SMC}}$ waveforms are shown only to give a reference to the initiating memory cycle. They do not go to the I/O backplane and so are not directly involved with the interface. The figure shows an Input cycle, meaning that $\overline{\text{DOUT}}$ will go HIGH. $\overline{\text{IC1}}$ and $\overline{\text{IC2}}$ are either HIGH or LOW depending on which register is being read, as shown by the broken line. During an OUTPUT cycle, the desktop computer sets the data onto the $\overline{\text{IOD}}$ bus earlier as shown by the broken line.

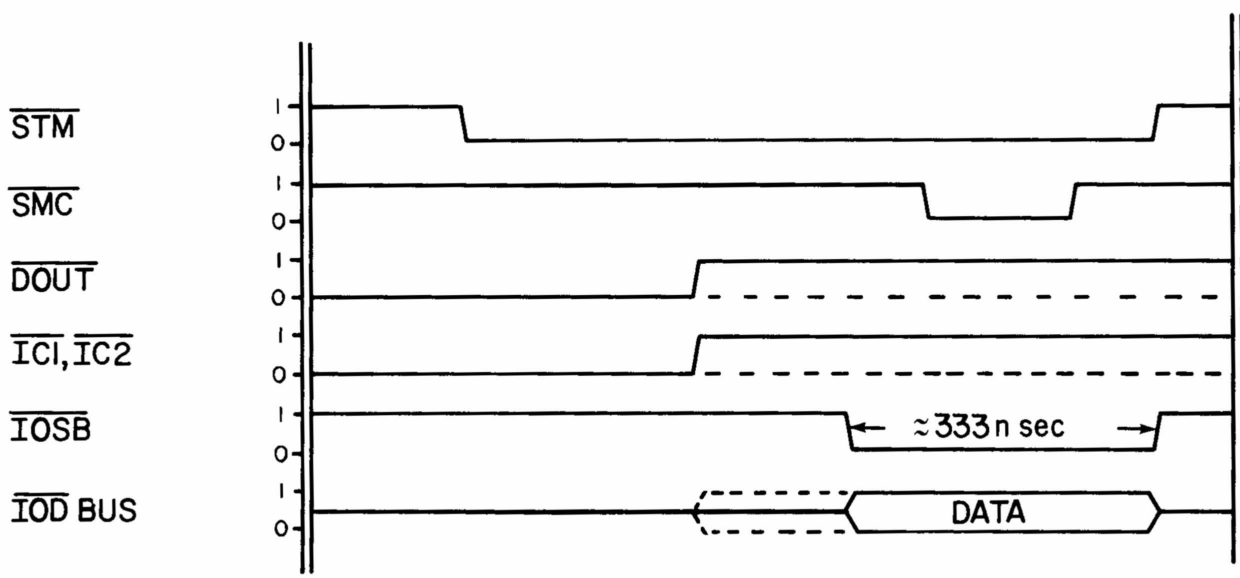


Figure 3-2. I/O Cycle Timing Diagram

Decoding I/O Instructions

The computer supplies four negative-true signals which define the data on the I/O bus. They operate as follows:

- $\overline{\text{DOUT}}$ Defines the direction of data flow.
- $\overline{\text{IOSB}}$ Data is valid at the rising edge of IOSB.
- $\overline{\text{IC1}}$, $\overline{\text{IC2}}$ Defines which of four registers is involved in the data transfer.

$\overline{\text{DOUT}}$	$\overline{\text{IC2}}$	$\overline{\text{IC1}}$	Operation
1	1	1	R4 IN
1	1	0	R5 IN
1	0	1	R6 IN
1	0	0	R7 IN
0	1	1	R4 OUT
0	1	0	R5 OUT
0	0	1	R6 OUT
0	0	0	R7 OUT

The outputs of the I/O instruction decoder, A1U6, are used to control the hardware registers on the 98046 which are associated with each operation. The 98046 uses six of the eight possible I/O operations. They are used as follows:

- R4 OUT Used to transfer data bytes and indirect register address information (pointers) from the computer to TxFIFO on the 98046.
- R5 OUT Used to enable and disable interrupt requests and to reset the 98046.
- R6 OUT Used to transfer data bytes to the R6/R7 OUT register for immediate write operations.
- R7 OUT Used to transfer register pointers to the R6/R7 OUT register for immediate read or write operations.
- R4 IN Used to transfer data bytes and indirect register address information from the RxFIFO on 98046 to the computer.
- R5 IN Used to transfer status information from the 98046 to the computer.
- R6 IN Not used.
- R7 IN Not used.

Control Information

Control information is sent to 98046 Interface by an R5 OUT operation. Figure 3-3 shows the significance of the various bits in an R5 OUT operation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DIS. ALL INT.		RESET					DIS. TX INT.

Figure 3-3. R5-OUT Bit Map

Bit 0	LOW	Disables only those interrupt requests originating at the TxFIFO.
	HIGH	Enables only those interrupt requests from the TxFIFO.
Bit 5	LOW	Has no effect.
	HIGH	Resets the interface.
Bit 7	LOW	Disables all interrupt requests from the interface.
	HIGH	Enables interrupt requests from the RxFIFO. Whether interrupt requests from the TxFIFO are enabled or disabled is determined by the state of Bit 0.

Resetting the Interface

All interfaces are automatically reset when power to the desktop computer is switched ON. After that there are two ways to reset the 98046. One is by manually resetting the computer. This is accomplished by holding the CONT'D key down while pressing the STOP key, which results in the INIT line going LOW for about 100 microseconds. This drives A1U12 pin 6 LOW, and enables U15A. The microcomputer is reset by A1U12 pin 6 going LOW, and interrupt requests are disabled by A1U15 pins 2 and 6 going LOW.

The other way to reset the interface is by program control. Any of the following commands which are available with the I/O ROM can accomplish this:

```
RESET 4
RESET 5
WRITE IO 4, 5; 2^5
WRITE IO 5, 5; DECIMAL 40
```

These are not the only ways to reset the interface, they are just the more common ways. There are many expressions that can be used to produce the same result: setting bit 5 during an R5 OUT operation.

If bit 5 is set during an R5 OUT operation, A1U12 pin 3 goes LOW, discharging A1C7 and resetting the microcomputer. This has the effect of:

- Setting the Data Bus to its high impedance state.
- Setting ports 1 and 2 to their input mode, which causes A1U14 pin 10 to go LOW, temporarily setting the R6/R7 Busy flag, resetting the USART, and disabling the inputs to the line drivers.
- Disabling the 2 MHz clock output at T0 (A1U22 pin 1).

The $\overline{\text{RESET}}$ input to the microcomputer, A1U22 pin 4, has an internal pullup resistor and a Schmitt trigger input, so the charging of A1C7 keeps the voltage at pin 4 below the threshold for at least fifteen microseconds. When the $\overline{\text{RESET}}$ input goes HIGH, the microcomputer goes through an initialization routine which:

- Puts a 2 MHz clock signal onto T0 (A1U22 pin 1).
- Sets the modem control latch, A2U4, outputs HIGH.
- Clears the RxINT flip-flop, A1U21A.
- Resets the RxFIFO Overrun latch, A1U21B.
- Resets the FIFOs, A1U7 and A1U11, which erases their contents.
- Sets A1U22 pin 38 LOW, which releases the RESET line.
- Initializes the RAMs, A2U6 and A2U7, and on-board scratchpad memory.
- Sets up the USART with the interrupt vector and interrupt mask.
- Reads the R6/R7 register to clear the R6/R7 BUSY latch.
- Writes a series of interface ID bytes to the RxFIFO.
- Enables the microcomputer interrupts.

When all these are done, the microcomputer goes to an idle loop until further operations are initiated by the desktop computer.

Status Information

The computer can read the status of the 98046 Interface by means of an R5 IN operation. It can be done at any time, regardless of the state of either FLG or STS. An R5 IN operation can be performed from the keyboard, if the computer has an I/O ROM installed, by executing the following instruction:

STATUS 4; variable

Then in order to display the data:

PRINT OCTAL (variable)

The conversion to octal notation makes it easier to interpret the sixteen-bit word. Figure 3-4 shows the significance of the various bits in an R5 IN operation. Bits 1, 2, 3, 6, 12, 13 and 14 of the input word are not driven and are interpreted as 0, so the fifth character is always a "0".

Bits 4 and 5 are identification bits and are always 0 on the 98046, therefore octal character 2 is always a "0".

Bits 8, 9, 10 and 11 are also identification bits which, for only the 98046, are always the polarity shown in Figure 3-4. Therefore octal character 4 is always a "4", to signify that the addressed interface is a 98046.

The variable bits are 0, 7 and 15; they influence octal characters 1, 3 and 6. Depending on the state of bit 0, octal character 1 is either a "1" or a "0". A "1", indicates that the R6/R7 register is not busy, which is the normal condition. If octal character 1 is a "0", it indicates that R6/R7 is busy.

Depending on the state of bit 7, octal character 3 is either a "2" or a "0". A "2" indicates that interrupts are enabled; a "0" indicates that they are disabled.

Depending on the state of bit 15, octal character 6 is either a "1" or a "0". A "1" indicates that the RxFIFO has overrun; a "0", which is the normal value, indicates that the RxFIFO has not overrun.

In summary:

4001	is the reset value
4000	indicates that the R6/R7 register is busy
4201	indicates that interrupts are enabled
104001	indicates that the RxFIFO has overrun

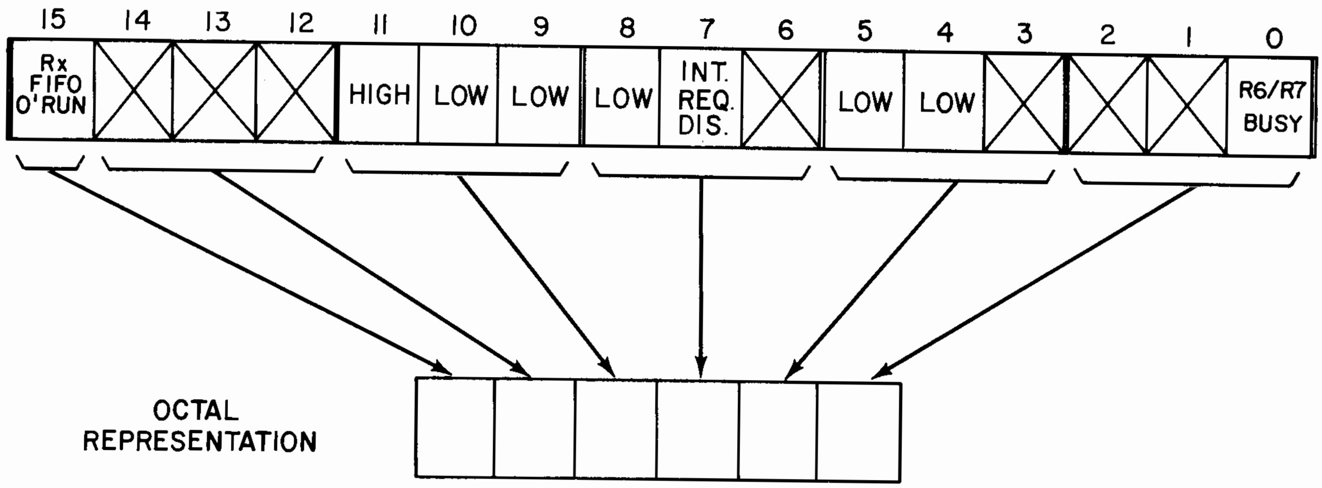


Figure 3-4. R5-IN Bit Map

Bit 0	LOW	Means that the R6/R7 register is busy.
	HIGH	Means that the R6/R7 register is not busy, and therefore can be written to.
Bit 4		Identification bit; always LOW.
Bit 5		Identification bit; always LOW.
Bit 7	LOW	Means all interrupt requests are disabled.
	HIGH	Means interrupt requests are enabled.
Bit 8		Identification bit; always LOW.
Bit 9		Identification bit; always LOW.
Bit 10		Identification bit; always LOW.
Bit 11		Identification bit; always HIGH.
Bit 15	LOW	Means that the RxFIFO Overrun latch has not been set.
	HIGH	Means that the RxFIFO Overrun latch has been set, an error condition which indicates that received data has been lost.

Note that bit 7 shows the status of only the main interrupt request disable latch. Keyboard operations cannot check the status of the TxFIFO interrupt request disable latch.

Data To and From the Interface

Information other than control information just discussed consists of either indirect register pointers or data bytes, and is handled by the microcomputer. When written to the interface, this information goes either to the TxFIFO or to the R6/R7 OUT register. When read by the computer, this information comes only from the RxFIFO.

R4 OUT

Table 2-1 shows that all transmit operations use the even select code. Before writing to R4, the computer sets the correct peripheral address, checks the $\overline{STS}$ line to see if there is a device with that select code, and checks the $\overline{FLG}$ line for that select code. If the $\overline{FLG}$ line, A1U16 pin 9 is HIGH, the 98046 is not ready to receive information from the computer. This can be because an R6/R7 operation is in progress, or because the TxFIFO is full. When $\overline{FLG}$ goes LOW, all these conditions have been met and the computer can write its information to R4.

The lower nine bits of the I/O bus are latched at the rise of R4 OUT. About a microsecond later a positive transition at A1U13 pin 5 will load the contents of the latches into the TxFIFO, U7.

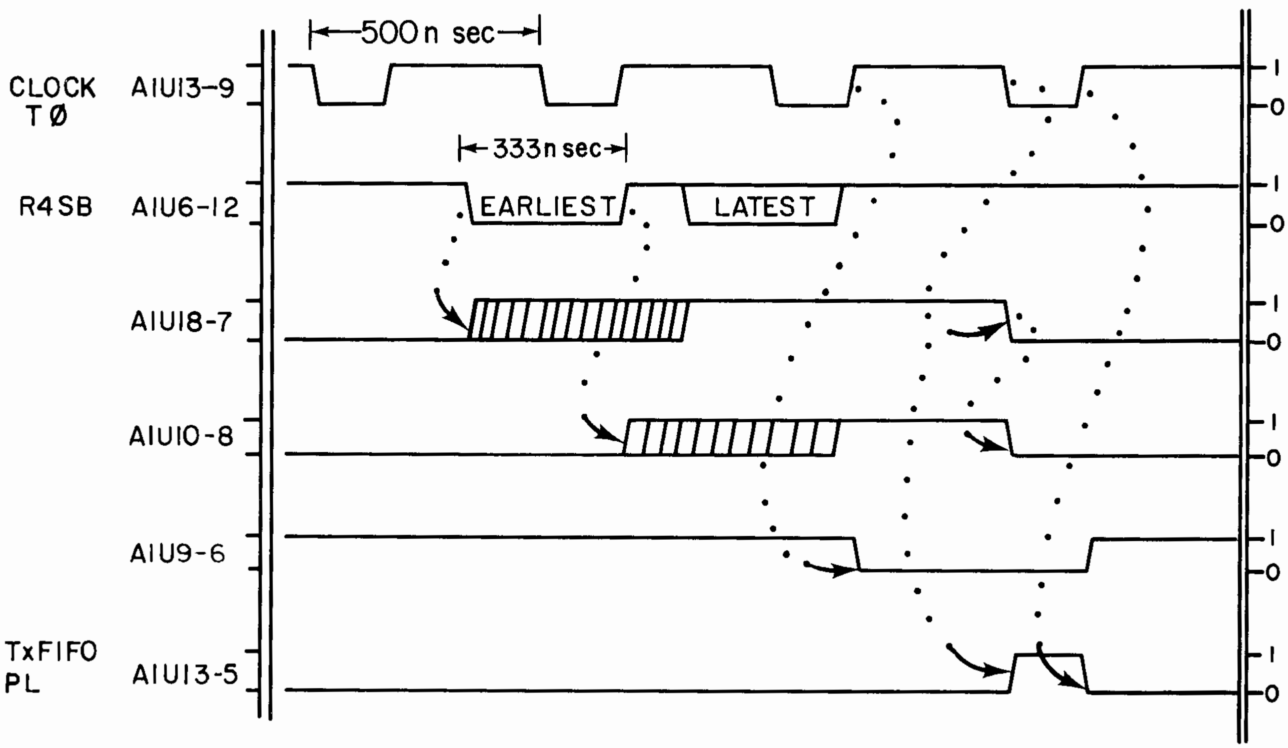


Figure 3-5. R4 OUT Timing

R4 IN

Data that is to be transferred from the interface to the computer is stored in the RxFIFO, A1U11. When the computer initiates an R4 IN operation the I/O instruction decoder enables a tri-state bus driver, which puts the RxFIFO output data onto the lower nine bits of the IOD bus.

R6/R7 OUT

The R6/R7 OUT register, A1U2, latches the lower eight bits of the I/O bus during a write operation to either R6 or R7. The R6/R7 latch, U18D, indicates to the microcomputer whether the contents of the R6/R7 OUT register are the result of an R6 operation or an R7 operation. When R6 or R7 is written to, the R6/R7 Busy flag, A1U18-9, goes LOW inhibiting interrupt requests to the desktop computer and initiating an interrupt on the interface's microcomputer. The interrupt results in a read of the R6/R7 register, which resets the R6/R7 Busy flag. This immediate handling of R6/R7 data is the primary feature of R6/R7 OUT operations.

Flag and Status

Several problems arise when the computer attempts to exchange information with an I/O device. Two of them are the speed mismatch between the two devices, and the ability to detect the presence of the interface. The FLG input to the computer solves the first problem; the STS input to the computer solves the second. These lines are driven only by the selected I/O device.

FLG

The computer cannot indiscriminately send data to an interface and completely disregard the ability of the interface to accept and process the data. Some kind of information exchange has to be done to inform the computer that the interface cannot accept data as fast as the computer can send it. This is the function of the negative-true FLG line driven by A1U16-9. The interface sets the FLG line true (LOW) when it is addressed, and it is ready for register access, either input or output, to R4, R6, or R7. As mentioned previously, R5IN and R5OUT can be done at any time, regardless of the state of FLG or STS.

The transmit FLG goes HIGH after data has been written to the interface and does not go LOW until the interface is ready to accept data again. The transmit FLG can be read by executing the following keyboard operation:

```
IOFLAG(4)
```

The computer displays a value corresponding to the inverse of the FLG line. If the value returned is 0, the interface is busy. This could mean that either a Reset routine is still in progress, an R4 OUT operation is in progress, or an R6/R7 OUT operation is in progress. If the value returned is 1, the interface is ready to accept data.

The receive FLG can be read by executing the following keyboard operation:

```
IOFLAG(5)
```

The computer displays a value corresponding to the inverse of the FLG line. If the value returned is 0, either the interface has no data in the RxFIFO or there is an R6/R7 operation in progress. If the value returned is 1, there is received data in the RxFIFO which can be transferred to the desktop computer.

STS

The Status line (STS) is a one-bit signal that is used for a variety of purposes by different interfaces. When STS is true (LOW), it indicates that the interface is plugged in, that it is powered, that it is being addressed by the desktop computer, and that no exceptional status condition exists on the interface. An exceptional status condition is one that requires service from the desktop computer other than, or in addition to, a normal data transfer.

The 98046, having two select codes, has two sources for STS, which is driven by A1U16 pin 7. The transmit STS signal originates in the microcomputer. It goes HIGH when the interface is reset, and is set LOW during the initialization routine.

The transmit STS can be read by executing the following keyboard operation:

```
IOSTATUS(4)
```

The computer displays a value corresponding to the inverse of the STS line. If the value returned is 0, the interface is malfunctioning. If the value returned is 1, the interface is operational.

The receive STS signal is HIGH when the interface is reset. Thereafter it is LOW until either the output word of the RxFIFO is an indirect address pointer (A1U11-15 is LOW) or the Rx FIFO overruns.

The receive STS can be read by executing the following keyboard operation:

```
IOSTATUS(5)
```

If the value returned is 0, the RxFIFO has overrun, or the RxFIFO output word is an indirect address pointer. The value that is usually returned is 1.

Interrupts

The computer's interrupt system is implemented in two distinct methods: hardware and software. This section describes only the hardware interrupt mechanisms. The software interrupt scheme, which in some cases emulates the hardware scheme, is described in the I/O ROM Programming manuals.

Interrupt Requests

Since the computer controls all I/O cycles, it must have a way of knowing that a peripheral device requires service. The computer has two inputs for this purpose: $\overline{\text{IRH}}$ and $\overline{\text{IRL}}$.

IRH and IRL

When a peripheral device has data to be sent to the computer, or if it requires service for any other reason, it drives either $\overline{\text{IRH}}$ or $\overline{\text{IRL}}$ LOW. The device's select code determines which of the two lines is used to request an interrupt. Select codes 0 through 7 use the low-priority interrupt request, $\overline{\text{IRL}}$; select codes 8 through 15 use the high priority interrupt request, $\overline{\text{IRH}}$.

The 98046 requests service from the computer by setting the INT REQ line, U15 pin 14, HIGH. An interrupt is requested because either the RxFIFO has data to send to the computer, or the TxFIFO is capable of accepting data from the computer.

Disabling the Interrupt Requests

Most I/O devices have a means of enabling or disabling their interrupt requests. While this defeats the purpose of the interrupt scheme, it is usually only temporary. The computer or the peripheral may be involved in something of a higher priority or a time-sensitive operation, and therefore should not be bothered with handling interrupts.

It is possible to disable interrupts at two levels on the 98046.

- All interrupt requests can be disabled. This means requests originating either at the TxFIFO or the RxFIFO do not result in an $\overline{\text{IRH}}$ or $\overline{\text{IRL}}$ to the computer. This is done under computer control, setting A1U15-2 LOW with an R5 OUT operation; it also occurs whenever A1U18 pin 9 is LOW, which signifies that the R6/R7 OUT register contains data that has not yet been read by the microcomputer.
- Interrupt requests originating at the TxFIFO can be disabled without affecting those coming from the RxFIFO. This is done under computer control, setting A1U15 pin 6 LOW with an R5 OUT operation. The reason for doing this is that as long as the FLG output of the TxFIFO, A1U11 pin 19, is HIGH, an interrupt request can be generated indicating that the interface is requesting the desktop computer to send data. This can be a nuisance if the desktop computer has no data to send over the data channel. Therefore the desktop computer disables these interrupt requests until it enters a mode that requires transmission of data.

Interrupt Priorities

The computer is designed to handle two levels of interrupt priorities, high and low. As long as only one I/O device requests service, it makes no difference what its select code is, or what its priority is. When more than one device requests service, however, a decision must be made as to which request is most urgent.

When the computer's microprocessor acknowledges an interrupt request, it stops what it is doing and branches to an interrupt service routine. If the request came from a low priority device, the interrupt service routine can in turn be interrupted by a request from a high priority device. The interrupt service routine for a high priority device cannot be interrupted, not even by a request from a device having a higher select code. So if several I/O devices request service while a high priority device is being serviced, they have to wait until the service routine is finished. Then the computer, seeing other interrupt requests, conducts a poll and services the I/O with the highest select code.

The Interrupt Poll

An interrupt request can be sent to the computer at any time; it is asynchronous with relation to the computer's internal operations. When the computer sees an $\overline{\text{IRH}}$ or $\overline{\text{IRL}}$ it must do two things:

- First: it must check the current interrupt status. If the computer is currently servicing a high level interrupt, no action is taken. If a low level interrupt is in progress an $\overline{\text{IRL}}$ will have no effect, but an $\overline{\text{IRH}}$ will cause an interrupt. And if no interrupt is in progress, either interrupt request will result in an interrupt.
- Second: once it has been determined that an interrupt can be done, the computer must wait until a time when it can safely suspend its current operation. This is usually only a few microseconds. Everything is now ready to start the actual interrupt process.

From sensing $\overline{\text{IRH}}$ or $\overline{\text{IRL}}$, the computer already knows the priority (most significant bit of the select code) of the requesting device. To identify the requesting device, the computer conducts an interrupt poll. It is a period of time, marked by $\overline{\text{INT}}$ going LOW, during which the I/O devices are each allowed to set one line on the $\overline{\text{IOD}}$ bus LOW. Since only eight peripheral devices can be involved at each priority level, only $\overline{\text{IOD0}}$ through $\overline{\text{IOD7}}$ are used for this interrupt poll. Each I/O device's select code (lower three bits) determines which $\overline{\text{IOD}}$ line is pulled LOW. An eight-bit priority encoder senses $\overline{\text{IOD0}}$ through $\overline{\text{IOD7}}$ during the interrupt poll. The output of this priority encoder is determined by the highest numbered $\overline{\text{IOD}}$ line which has been pulled LOW. This three-bit output provides the computer with the lower three bits of the requestor's select code.

The desktop computer now knows the select code of the interrupting device, so it can set the Peripheral Address lines to correspond. It then branches to the start of the correct interrupt service routine.

Data Flow Within the Interface

It has already been shown that data written to the interface will go to either the R6/R7 OUT register, or to the TxFIFO. Thereafter it is under control of the interface's microcomputer. But since the first complex device encountered is the FIFO, a few words about that would be in order.

The FIFOs

There are two identical 32-deep by 9-wide FIFO's (First In, First Out memories) on the 98046. One, the TxFIFO, A1U7, handles the transmit function, and the other, the RxFIFO, A1U11, handles the receive function. Loading the FIFO is done at a positive transition on the Parallel Load (PL) input, pin 18. A positive transition on the Parallel Dump (PD) input, pin 5, causes the FIFO contents to shift toward the output. If there is more than one word stacked in the FIFO, the word driving the output is lost as the subsequent word replaces it. The last word in the FIFO remains at the output until either the FIFO is reset, or another word is written into it.

Other outputs indicate the status of the FIFO contents. A high level at Output Ready (OR), pin 3, indicates that the output is valid data. It pulses low during the shift caused by a Parallel Dump, and remains low if no new word was shifted to the output. A high level at Input Ready (IR), pin 25, indicates that the FIFO can accept data. It goes low while data is being shifted down through the FIFO, and remains low if the FIFO is full. Once the FIFO is full, any further data written to it is lost. The Flag output (FLG), pin 19, is HIGH when the FIFO contains more than 16 words. The FLG output of each FIFO is used to generate an interrupt request: the TxFIFO when it is less than half full, the RxFIFO when it is more than half full.

NOTE

An anomaly within the FIFO makes it difficult to determine when the FLG output on a particular device goes HIGH. It can go HIGH when either the 13th, 14th, 15th, or 16th word is written to the FIFO. It then remains HIGH until there are less than 13, 14, 15, or 16 words remaining in the FIFO. It is always HIGH when there are more than 16 words in the FIFO.

The contents of both FIFO's can be cleared and their Q outputs set LOW by setting the Master Reset input, pin 4, LOW. This is done under control of the microcomputer during the initialization routine.

The Microcomputer

Most of the activity on the 98046 is controlled by its on-board 8048 microcomputer. It has 1024 bytes of mask programmable ROM and 64 bytes of scratchpad read/write memory. The eight bit, bi-directional Data Bus connects the microcomputer to other major components on the interface.

The microcomputer drives the Data Bus only when exchanging information with external devices. The timing for these external cycles is supplied by ALE for the address, $\overline{\text{PSEN}}$ for external memory references, $\overline{\text{WR}}$ for output operations, and $\overline{\text{RD}}$ for input operations. The Data Bus is kept in its high-impedance state when the microcomputer is doing operations involving only internal memory and registers. $\overline{\text{PSEN}}$, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ are also maintained HIGH throughout these internal operations. Only ALE marks the occurrence of each memory cycle.

The two, eight-bit, input/output ports are referred to as Port 1 and Port 2. The individual lines are P10 through P17 for Port 1 and P20 through P27 for Port 2. They are assigned the following uses:

Line	Direction	Signal	
P10	INPUT	RxFIFO Input Ready	1=FIFO can accept data
P11	INPUT	RxFIFO Flag	1=FIFO has more than 16 words stored
P12	INPUT	TxFIFO Output Ready	1=FIFO contains valid data
P13	INPUT	TxFIFO Flag	1=FIFO has more than 16 words stored
P14	INPUT	R6/R7 Latch	0=R6 data 1=R7 pointer
P15	INPUT	RxFIFO Output Ready	1=FIFO has valid data at its output
P16	INPUT	RxFIFO Overrun Latch	0=Data was written to FIFO when it was full
P17	INPUT	TxFIFO bit 8 out	0=lower byte is data 1=lower byte is pointer
P20	OUTPUT	RAM Address Bit 8	
P21	OUTPUT	RAM Address Bit 9	
P22	OUTPUT	External device select	1=RAM 0=other registers
P23	NOT USED		
P24	NOT USED		
P25	OUTPUT	Even select code STS	0=true
P26	OUTPUT	Even select code FLG	0=disable
P27	OUTPUT	System Reset	0=Run 1=Reset

The clock for the microcomputer is derived from a 6.0 MHz crystal. An internal divider produces the 2.0 MHz signal that serves as the system clock; this signal appears at the T0 pin (A1U22 pin 1) during the initialization routine. The duration of a memory cycle is always five of these clock cycles; thus the frequency of ALE is 400 kHz. Either of these signals can be used to check the accuracy of the crystal frequency.

A complete instruction cycle on the 8048 can consist of either one or two memory cycles. The first cycle fetches the instruction from internal ROM or external RAM. .

The second cycle, if one is necessary, either fetches the second byte of the instruction or else is an external cycle to execute the instruction.

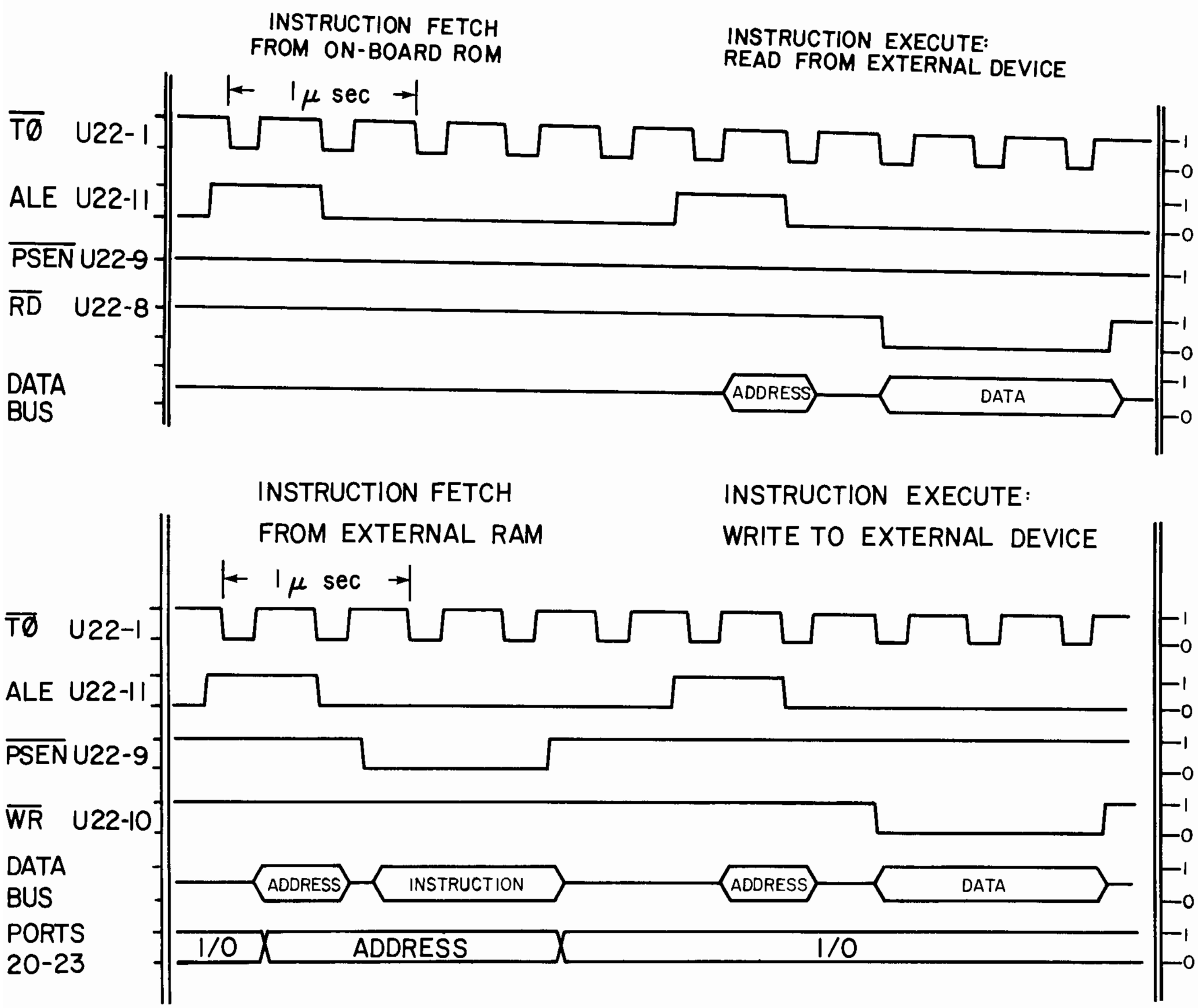


Figure 3-6. Microcomputer Timing

Information that has been stacked in the TxFIFO is extracted by the microcomputer as its program directs. Since the data on the Data Bus is maneuvered by the microcomputer's Move External (MOVX) instructions, all data passes through the accumulator register. This means that transferring a byte from one device to another requires two instructions, each consisting of two memory cycles. The first instruction would, for example, read the byte from the TxFIFO into the accumulator. The second instruction would then take the byte in the accumulator and write it out to the USART. The source or destination address for accumulator data is contained in one of two working registers in the microcomputer. This address consists of a group of eight bits which is latched by the Address Latch, A2U5, and decoded by the External Address Decoder, A2U12, during the execution of the instruction. The output of the decoder controls the devices (other than the microcomputer) which drive the Data Bus.

Using an instruction that reads data from the TxFIFO into the accumulator as an example, the MOVX instruction is fetched from a particular program address in internal ROM or in external RAM. This is the first memory cycle. Then in the second memory cycle, the execute cycle, the address of the TxFIFO is first set onto the Data Bus. It had previously been stored in one of the working registers. It is latched into the external address latch, A2U5, at the fall of ALE. The latched address is decoded by the external address decoder, A2U12, to enable the output of the TxFIFO at the time when the microcomputer expects data to be on the Data Bus.

The microcomputer's ROM contains a number of routines and subroutines which can be called by the desktop computer. Therefore the desktop computer can send information (through R4OUT) which directs the microcomputer to execute a particular routine.

The USART

The 98046 uses a Z80-Serial Input/Output (SIO) chip to convert parallel data to serial and vice versa. The generic name for this kind of device is a USART, an acronym for Universal Synchronous/Asynchronous Receiver/Transmitter.

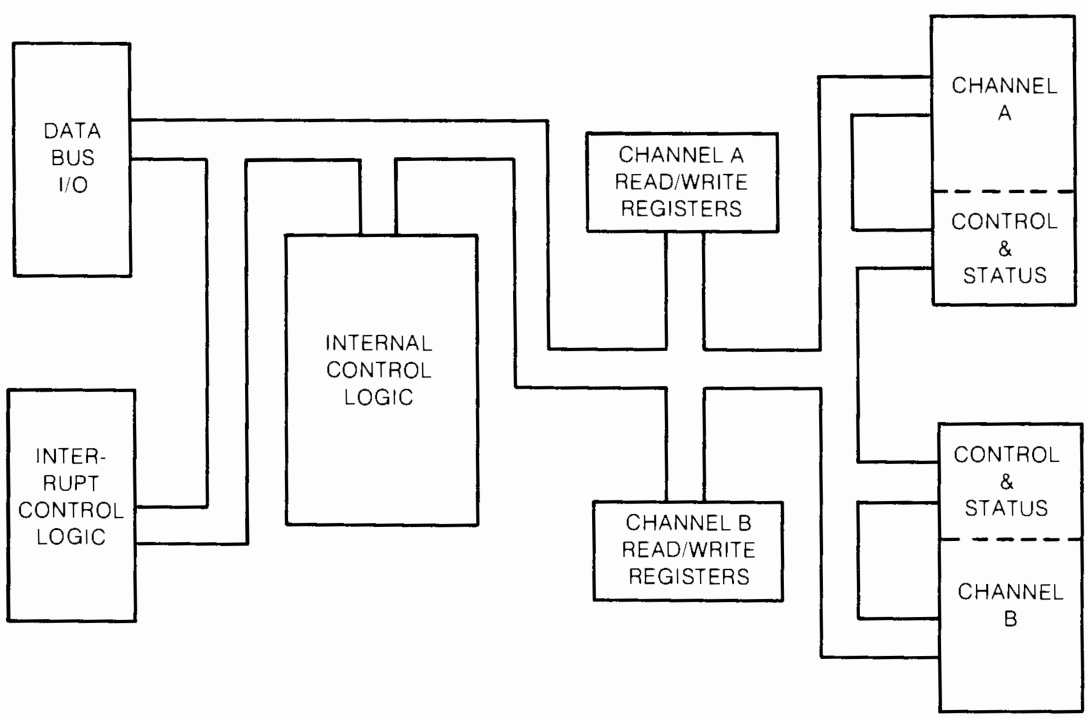


Figure 3-7. USART Block Diagram

It has two input/output channels, A and B, for bit serial data, and a bi-directional Data Bus for bit parallel data and control information. Control information can be stored in registers on the USART. The contents of these registers determine the configuration of the USART for synchronous or asynchronous operation, parity, number of bits per character, sync character recognition, etc. System firmware in the desktop computer handles the details of how and when these registers are loaded. The USART formats the data in the manner defined by the contents of the control registers and transmits it to the outside world via the line drivers.

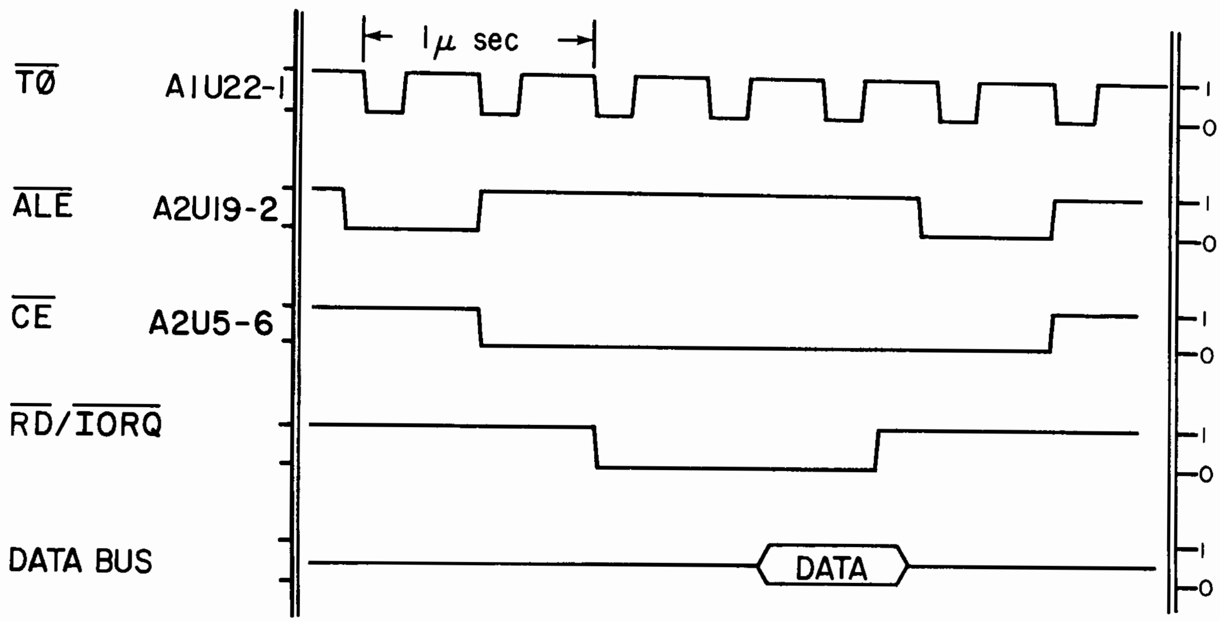


Figure 3-8. USART Timing Diagram

Summary of Data Flow

Data to be transmitted is sent to the TxFIFO by the computer after the USART has been properly configured. The data ripples down through the TxFIFO and is sent through the microcomputer's accumulator register to the USART. The USART then manipulates the data and shifts it serially out the TxD output to the line drivers. The line drivers send the data to the modem in conformance to CCITT V.28 and RS-232C electrical standards.

Information coming from the modem is detected by the line receivers, A2U15 and A2U16, and sent to the modem status register, A2U11, and to the USART. As with transmitted data, the contents of the USART's control registers determine what happens to the received data. The control registers must be set up to interpret the data protocol that is being received, or else chaos results. The function of the USART is to assemble the received data into bytes, which the microcomputer withdraws from the USART and stacks into the RxFIFO via the microcomputer's accumulator register.

The Rx Interrupt Request latch, A1U21A, can be set when information is written into the RxFIFO. Whether it is set or not depends on the state of address bits A3 and A4 when the external address is latched into A2U5. In any event, the Rx Interrupt Request is set HIGH when the RxFIFO is approximately half full, as indicated by its FLG output, A1U11 pin 19, going HIGH. The Rx Interrupt Request going HIGH causes an interrupt request to be generated if interrupt requests are enabled.

Although the firmware is designed to prevent it, the RxFIFO can be overrun. An overrun occurs when the interface tries to store received data into an already full FIFO. This condition could be due to a higher priority I/O device occupying the computer's time just as a burst of data is being received by the interface. Should this happen, the FIFO contents stay unchanged, the received data is lost, but the fact that the FIFO has been overrun is detected by the RxFIFO Overrun Latch, A1U21B. The output of this latch is set on $\overline{\text{IOD15}}$ when an R5 IN operation is done so the computer can determine if received data has been lost.

The Output Ready line of the RxFIFO, pin 3 of U11, being HIGH signifies that information is in the RxFIFO, and can be read by the computer. The computer can determine this by reading FLG for the Receive select code: if it is LOW, the RxFIFO contains valid information. When the computer initiates an R4 IN cycle, the output of the RxFIFO is set onto the lower nine bits of the $\overline{\text{IOD}}$ bus, and a pulse is sent to the PD input of the RxFIFO, which shifts the next word to the output.

Chapter 4
Troubleshooting

Initial Testing

Programs on the 98046-90449 or 98046-90450 Test Cartridges can be used to effectively isolate a suspected problem in the 98046. These programs can isolate the problem to a particular interface PC assembly or the interface cable. The tests are:

- Standard interface test
- Option 001 interface test
- Extended interface test

The tests should be run in the order listed above. Run either the standard or the option 001 test depending on the interface in use, and then the extended interface test.

Each of the tests listed above also includes a "common circuit" test and a ROM test.

The common test checks the interface circuits on the A1 assembly (98046-66501) and the circuits on the A2 assembly (98046-66502) except for the input and output lines going to the interface cable.

The test includes checks on:

- Tx and Rx FIFOs
- Interface RAM
- Handshake and interface logic between mainframe and interface
- Microcomputer operations including RAM and ROM
- Reset circuit

The ROM test provides a bit-by-bit check of the microcomputer's ROM.

Standard Interface Test

This test checks the standard 98046 interface and its cable. With the aid of the standard test connector, normal interface operations are tested.

Option 001 Interface Test

This test checks the option 001, 98046 interface and its cable. With the aid of the option 001 test connector, normal interface operations are tested.

Extended Interface Test
This test checks the operation of the USART and associated circuits. This test uses the interface test connector (ESK) and includes the following tests:

- Modem control
- Status registers
- Both USART channels in asynchronous and bi-synchronous
- Parity generator and detector
- Framing and overrun errors
- CRC error reception and transmission

Equipment Required
Items needed to perform the tests are listed below.

HP Part Number	Description
98241-67901	Interface Test Fixture (for ESK Test)
	#2 Pozidriv Screwdriver
1251-6624	Standard Test Connector
1251-6625	Option 001 Test Connector
98046-67906	98046 Test Connector (ESK)
98046-90450	Test Cartridge for 9835 or
98046-90449	Test Cartridge for 9845

Initial Interface Set-Up
Table 4-1 describes the interface set-up for each test. Figures 4-1 through 4-3 show the set-up for each test. The test set-up is the same for the 9835 and 9845.

Table 4-1. Interface Set-Up

Test	Interface Set-Up
Standard	Connect the standard test connector on the end of the standard interface cable. Interface installed in I/O slot or on interface test fixture.
Option 001	Connect the option 001 connector on the end of the option 001 interface cable. Interface installed in I/O slot or on interface test fixture.
Extended	Interface installed on interface test fixture with interface test connector installed on the interface output connector on the A2 assembly.

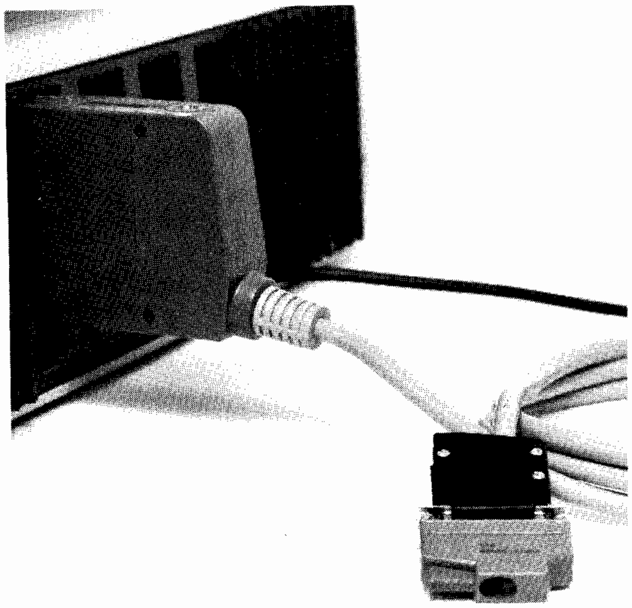


Figure 4-1. Standard Test Set-Up

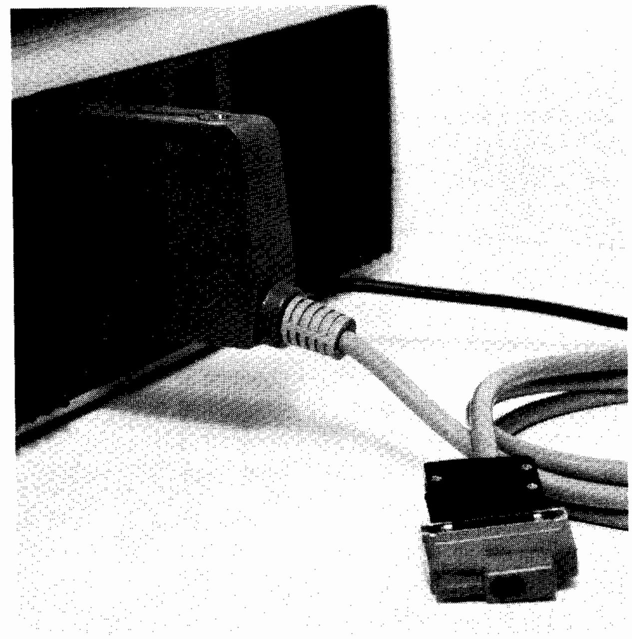


Figure 4-2. Option 001 Test Set-Up

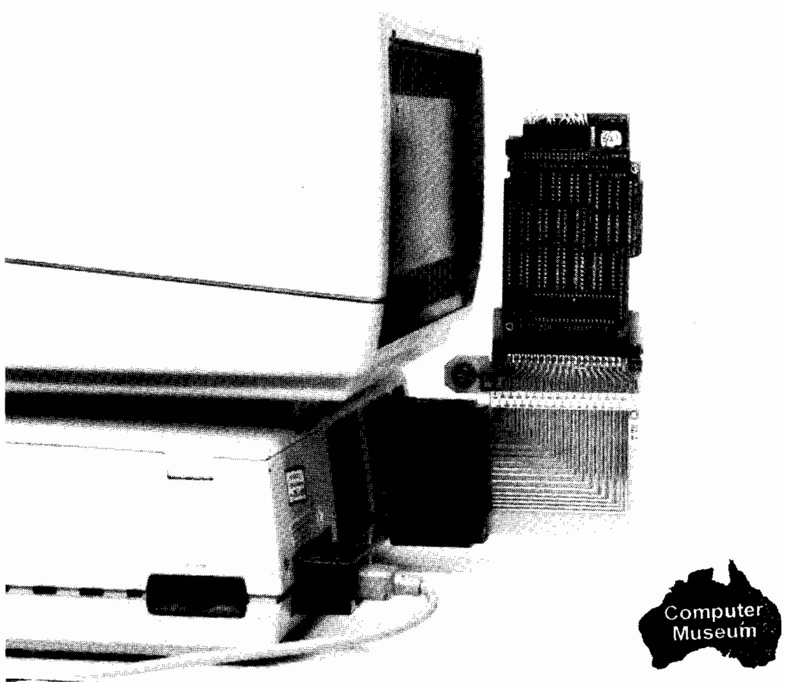


Figure 4-3. Extended Test Set-Up

Starting the Tests

After setting up the interface for the test you wish to perform (described in Table 4-1), install the appropriate test cartridge (listed below) in the desktop computer cartridge drive (T15 for the 9845).

Desktop Computer	Use Cartridge Part Number
9835A/B	98046-90450
9845B/C	98046-90449

Switch the computer on (latch the AUTOST key on the 9845), the test programs will be loaded by the auto start feature. The programs can also be loaded by pressing LOAD "AUTOST" EXEC; then press RUN.

Enter the interface select code and the name of the test you have the interface set up for. Press CONT after entering each input.

Displayed messages will describe failures when they occur. The tests stop on the first error detected. Displayed messages may also recommend a particular circuit to check, or a particular signature analysis test (described later) to perform.

If you wish to perform signature analysis tests, refer to the "Signature Analysis" section which follows.

Press STOP CONT to return to the initial test program information. The same test or a different test may be selected at this time.

Signature Analysis

Once the cause of a problem has been isolated to the interface, there remains the problem of finding the faulty component. Because of the increased complexity of logic circuits used to control interface operations, malfunctions in the interface are difficult to locate. The concept of signature analysis is based on the fact that at a particular point in a circuit, the data bit stream is predictable under specifically programmed conditions. An instrument such as the HP Model 5004A Signature Analyzer compresses the data at a given point during a controlled time span (window) and displays the resulting four-character signature. The signature indicates whether the correct data was present within the window at the measurement point. This information can be used to locate a defective component.

If the signature at a particular point matches the signature given for that test, then that point in the circuit is operating properly. If a different signature is displayed, the circuit is malfunctioning and the device causing the incorrect signature must be replaced.

Equipment Required

To troubleshoot the 98046 using signature analysis, the following equipment is required:

HP Part Number	Description
98241-67901	Interface Test Fixture
98046-90450	Test Cartridge for 9835 or
98046-90449	Test Cartridge for 9845
HP 5004A	Signature Analyzer
	#2 Pozidriv Screwdriver
98046-67906	98046 Test Connector (ESK)

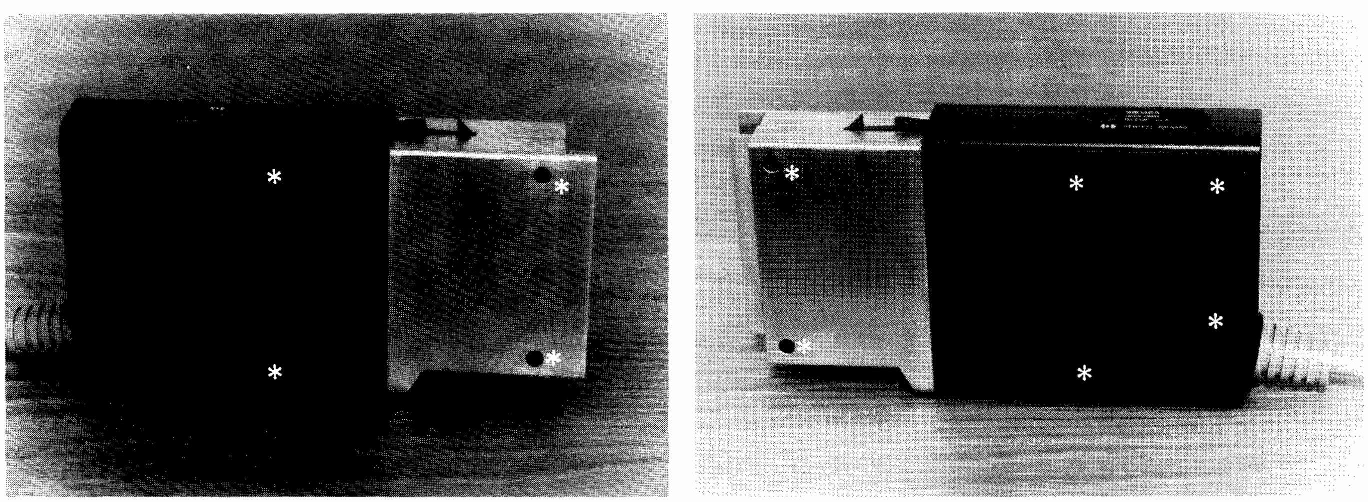


Figure 4-4. Interface Access Screws

Test Set-Up

Use the following procedure to prepare for signature analysis testing.

- Switch the computer off.
- Remove the interface from the system and remove the interface case as shown in Figure 4-5.

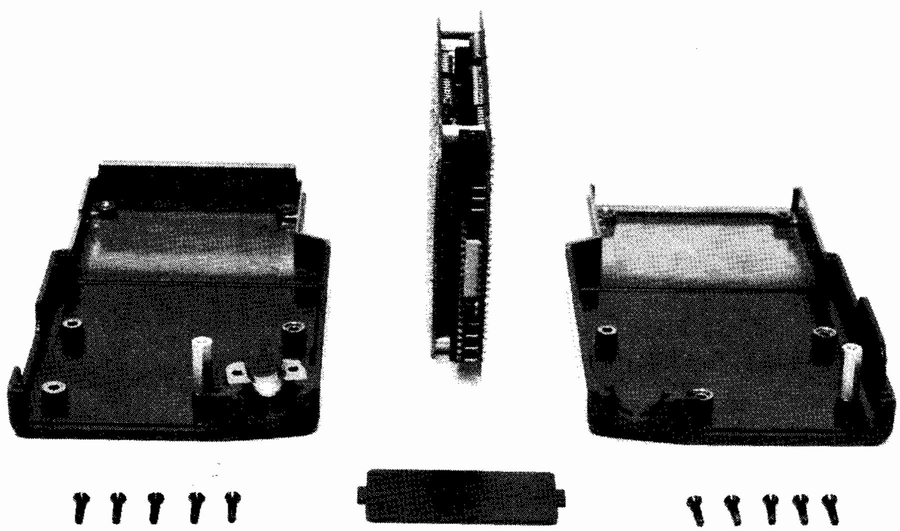


Figure 4-5. Removing the Interface Case

- Disconnect the interface cable from the 98046-66502 PC assembly.
- Install the interface test fixture in one of the computer's I/O slots as shown in Figure 4-6. Then, install the interface on the interface test fixture.
- Remove all option ROMs and any other interfaces from the computer.

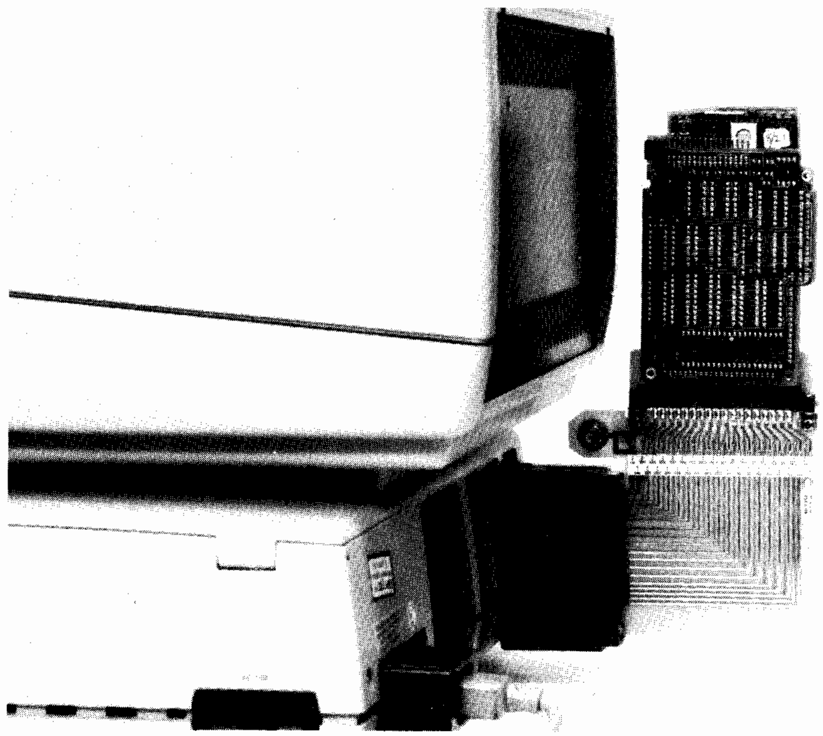


Figure 4-6. SA Test Set-Up

- Switch the computer on and install the test cartridge.
- Refer to "Testing the Interface" for the test sequence and procedure.

Helpful Hints

1. Make all the connections for a particular test with the computer switched off.
2. When applying power, switch on the signature analyzer first; then switch on the computer.
3. When testing is completed, switch off the computer first; then the signature analyzer.
4. If a lot of signatures for a particular test are incorrect, first try to reset the computer and start the test again to ensure that the test is running properly.

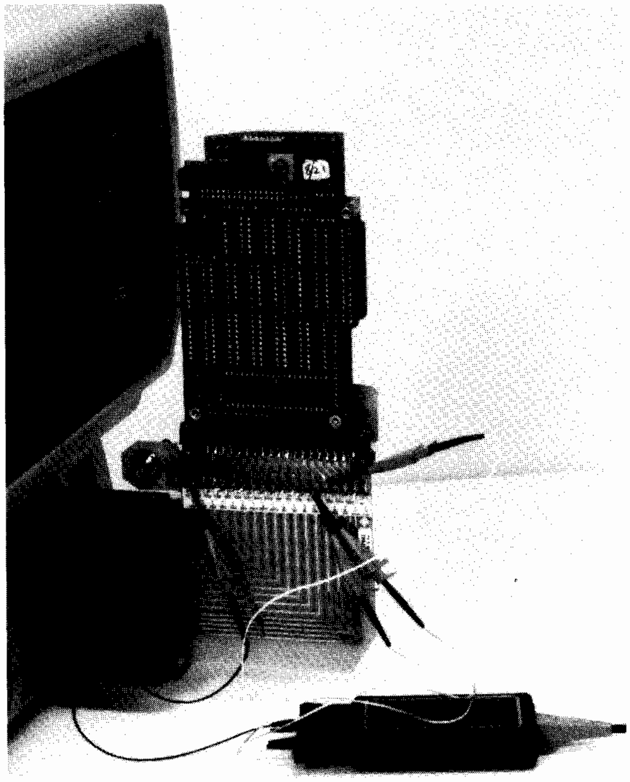
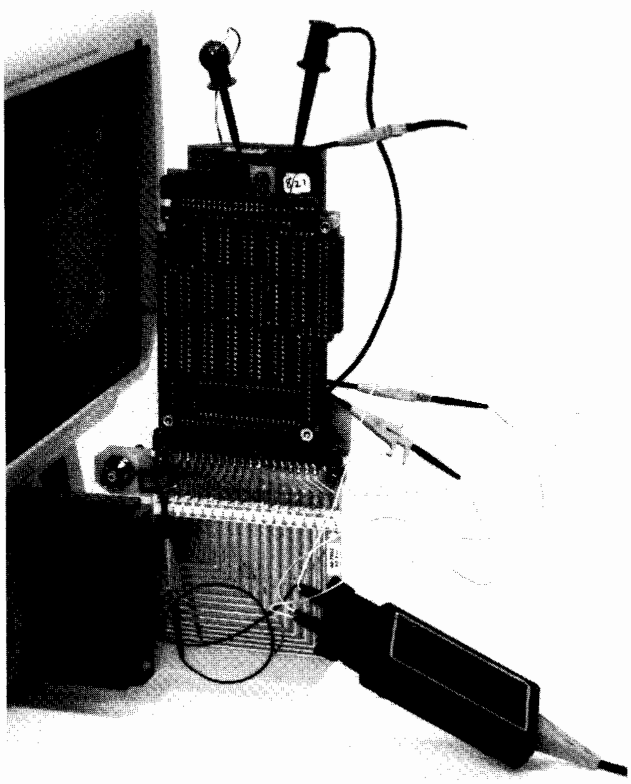
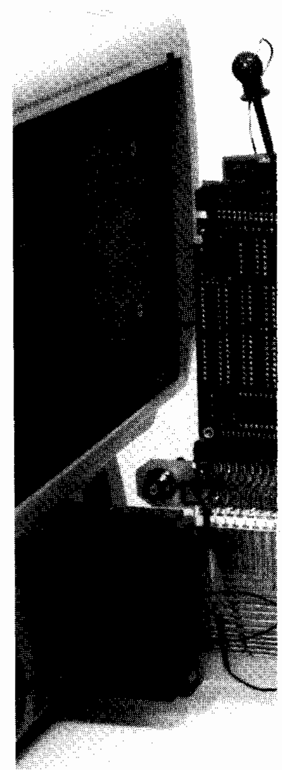


Figure 4-7. Signature Analyzer Connections for Tests 1, 2, 3 and 4

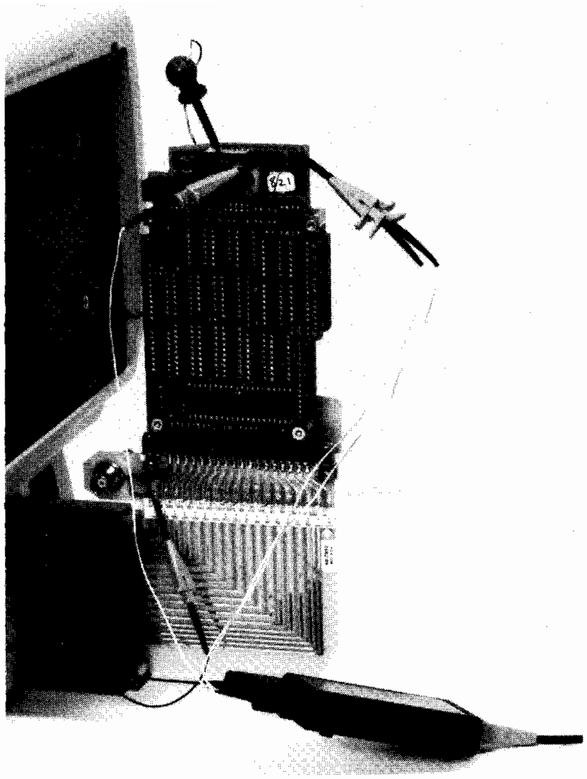


Section 1

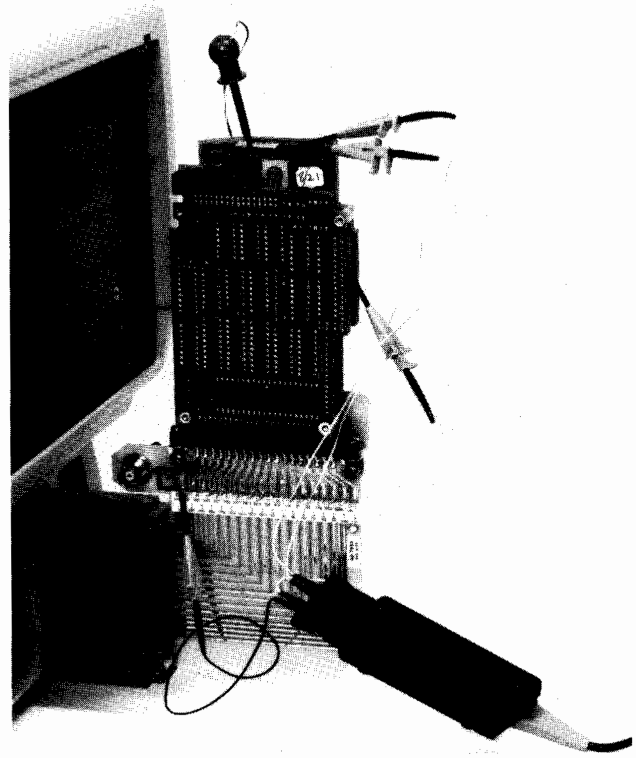


S

Figure 4-9. Signature A



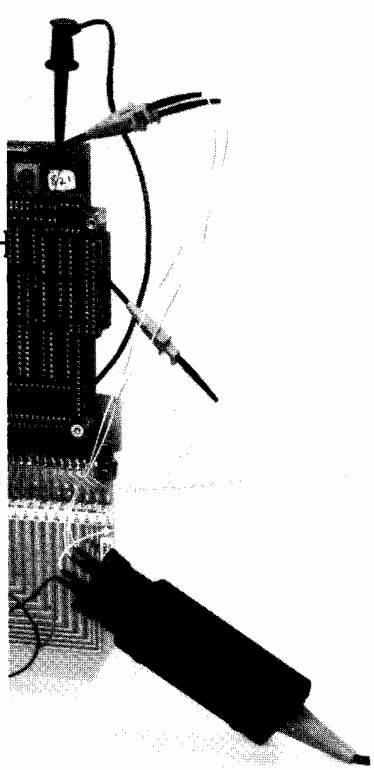
Section 1



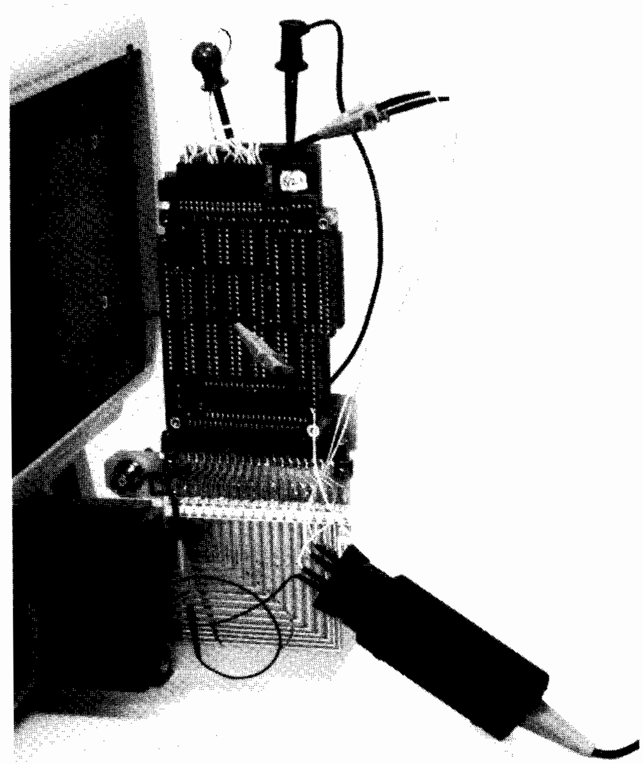
Section 2 and 3

Figure 4-8. Signature Analyzer Connections for Test 6

H



ection 2



Section 3

nalyzer Connections for Test 7

Testing the Interface

NOTE

Remove all option ROMs and any other interfaces from the computer before starting the tests.

The SA routines on the test cartridge are designed to test different segments of the interface in a logical sequence.

The set-up for each test and the signatures for each test are described later in this chapter. Here is the procedure to initiate the SA tests.

Load the interface test programs (previously described) via the auto start feature or by pressing LOAD "AUTOST" (EXEC). Then press (RUN).

The signature analysis tests are accessible after one of the interface tests has run.

Enter the interface select code and enter ESK for the test to be run.

The test will fail and information will be printed. At the end of this display, a signature analysis test number will be requested.

The following tests are available:

Test Number	Test
1	PA Decoder
2	Register Decoder
3	IOD Bus
4	R5 OUT Register
5	Not Used
6	R6/R7 Communications
7	Tx/Rx FIFO Test
0	Cancels Previous Test

Enter the number of the test and press (CONT).

To stop a test, press stop.

The recommended sequence in which to run the tests is from 1 to 7.

It may be helpful to refer to the 98046 Schematic Diagram in Chapter 5 while performing the tests.

Test 1

This test checks the peripheral address decoder circuit, specifically U5, U17 pins 11, 12 and 13, and S1. U17's action during interrupt is not tested.

Set the signature analyzer as follows:

START	⌝_	(in)
STOP	_⌐	(out)
CLOCK	_⌐	(out)

Connect the signature analyzer as follows (see Figure 4-3):

START to PA0 (TP5)
STOP to PA0 (TP5)
CLOCK to IOSB (TP4)

Compare the signatures observed with those shown in Table 4-2. Note that any particular select code setting has its own signature list. All components tested are on the A1 (98046-66501) assembly.

Tests: PA decoder circuit (U5, U7, 11-13, 51)

Table 4-2. Test 1 Signatures

First Check:	**2**	**4**	**6**	**8**	**10**	**12**
U17 Pin 2	0000	0000	0000	003U	003U	003U
U17 Pin 5	003U	003U	003U	0000	0000	0000
U17 Pin 11	003H	003C	0037	002U	001U	003U
Other Signatures:						
U5 Pin 1 (+5V)	003U	003U	003U	003U	003U	003U
U5 Pins 2, 4	000U	000U	000U	0030	0030	0030
U5 Pins 3, 10, 11	0002	0004	0008	0010	0020	0000
U5 Pin 5	000U	000U	000U	000U	000U	000U
U5 Pin 6	003U	003U	003U	0000	0000	0000
U5 Pin 7 (GND)	0000	0000	0000	0000	0000	0000
U5 Pin 8	0015	0015	0015	0015	0015	0015
U5 Pin 9	0000	003U	0000	003U	0000	003U
U5 Pin 12	0033	0033	0033	0033	0033	0033
U5 Pin 13	003U	0000	0000	003U	003U	0000
U5 Pin 14 (−5V)	003U	003U	003U	003U	003U	003U
U17 Pin 7	0000	0000	0000	0000	0000	0000
U17 Pin 12	003U	003U	003U	003U	003U	003U
U17 Pin 13	0002	0004	0008	0010	0020	0000
U17 Pin 14 (+5V)	003U	003U	003U	003U	003U	003U

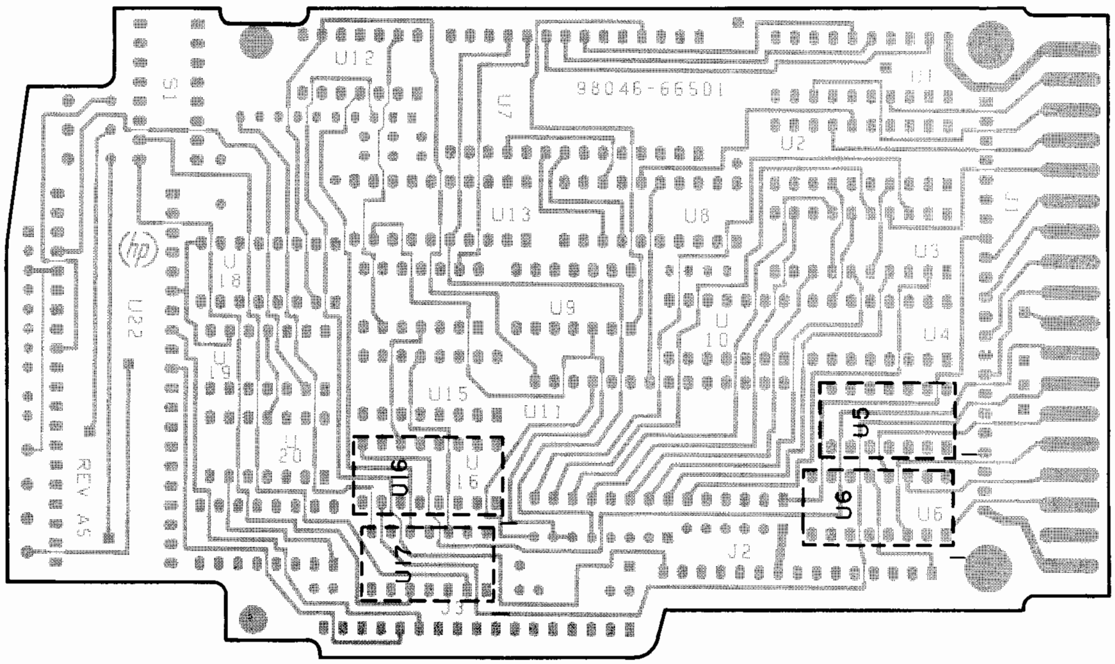


Figure 4-10. Test 1 Component Locator

Test 2

This test checks the register decoder circuit, specifically U6, U10 Pins 4, 5 and 6, U18 Pins 13, 14 and 15, and U20 Pins 1 through 6.

Set the analyzer as follows:

START	⌊	(in)
STOP	⌈	(out)
CLOCK	⌈	(out)

Connect the signature analyzer as follows (see Figure 4-7):

START to PA0 (TP5)
STOP to PA0 (TP5)
CLOCK to IOSB (TP4)

Compare the signatures observed with those shown in Table 4-3. All components tested are on the A1 (98046-66501) assembly.

Tests register decoder circuit (U6, U10 Pin 4-6, U18 Pin 13-15, U20 Pin 1-3)

Table 4-3. Test 2 Signatures

First Check:

Test Point	Signature
U6 Pin 4	UFP6
U6 Pin 5	UC59
U6 Pin 6	7886
U6 Pin 9	UHF6
U6 Pin 10	U3HH
U6 Pin 11	P9P5
U6 Pin 12	H99P
U10 Pin 6	U7H7
U18 Pin 13	040A

Other Signatures:

Test Point	Signature
U6 Pin 1	F7C3
U6 Pin 2	01UF
U6 Pin 3	365U
U6 Pin 8 (GND)	0000
U6 Pin 13	AU74
U6 Pin 15	F7AF
U6 Pin 16 (+5V)	F7AF
U10 Pin 4	U3HH
U10 Pin 7 (GND)	0000
U10 Pin 14 (+5V)	U9FF
U18 Pin 8 (GND)	0000
U18 Pin 14	U3HH
U18 Pin 15	UHF6
U18 Pin 16 (+5V)	U9FF
U20 Pin 1	F7C3
U20 Pin 2	O1UF
U20 Pin 3	F7AF
U20 Pin 7 (GND)	0000
U20 Pin 14 (+5V)	U9FF

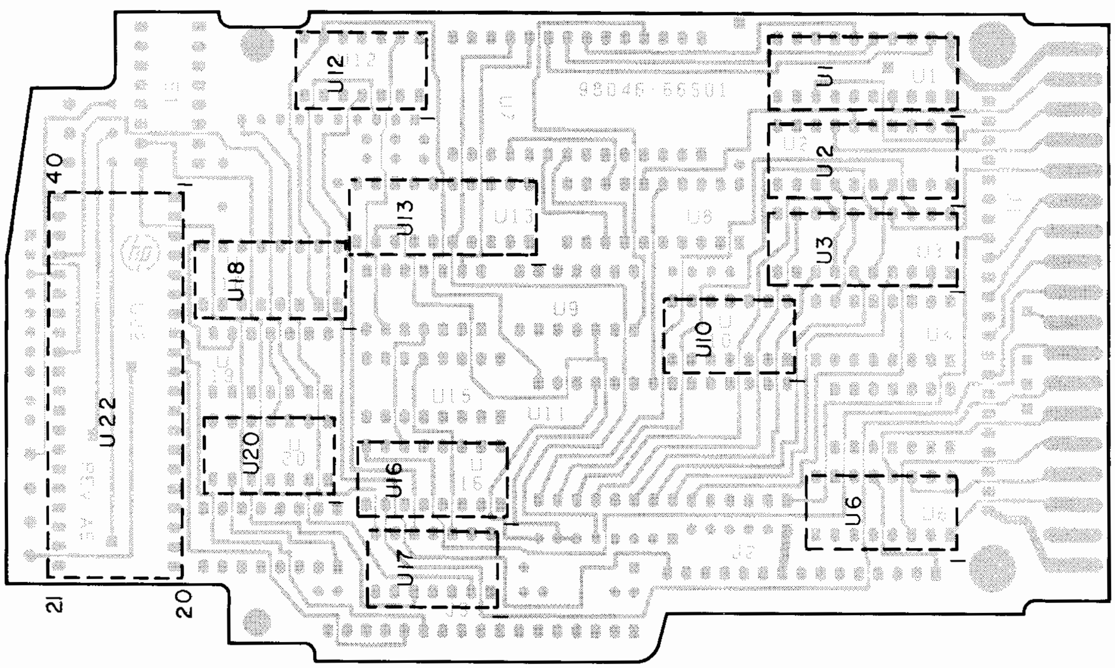


Figure 4-11. Test 2 Component Locator

Test 3

This test checks the IOD lines (IOD0-7) and their destinations on the A1 assembly.

Set the analyzer as follows:

START	(in)
STOP	(out)
CLOCK	(out)

Connect the signature analyzer as follows (see Figure 4-7):

START to PA0 (TP5)
STOP to PA0 (TP5)
CLOCK to IOSB (TP4)

Compare the signatures observed with those shown in Table 4-4.

Table 4-4. Test 3 Signatures

First Check:

Test Point	Signature
IOD0	H2P7
IOD1	CIU0
IOD2	8A82
IOD3	49U6
IOD4	AFC0
IOD5	29A8
IOD6	P45F
IOD7	6861
IOD8	F819
IOD11	A7H1
IOD15	2935

Other Signatures:

Test Point	Signature
U3 Pin 19	2935
U4 Pin 2, Pin 14	2935
U10 Pin 11	3HAU
U10 Pin 12	3HAU
U10 Pin 13	unstable
U12 Pin 10	2935
U13 Pin 1	2935
U14 Pin 1	2935
U14 Pin 2	0000
U15 Pin 12	2935
U15 Pin 14	0000
U15 Pin 15	2935
U19 Pin 3	0000
U19 Pin 4	0000
U19 Pin 5	2935
U19 Pin 6	2935
U19 Pin 6	2935
U19 Pin 8	2935
U19 Pin 10	0000

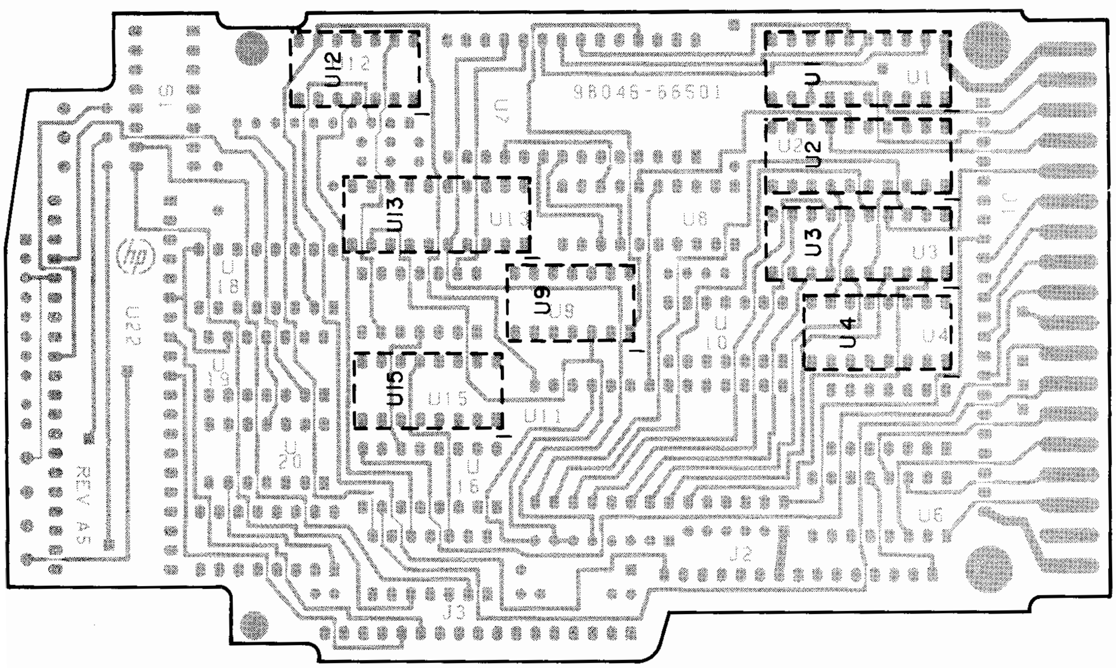


Figure 4-12. Test 3 Component Locator

Test 4

This test checks the R5OUT register and the reset circuit, specifically, U15 and U12.

Set the analyzer as follows:

START	↓	(in)
STOP	↑	(out)
CLOCK	↑	(out)

Connect the signature analyzer as follows (see Figure 4-7):

START to PA0 (TP5)
STOP to PA0(TP5)
CLOCK to IOSB (TP4)

Compare the signatures observed with those shown in Table 4-5. All components tested are on the A1 (98046-66501) assembly.

Tests reset circuit and interrupt enable latch (U15 Pin 1-7).

Table 4-5. Test 4 Signatures

First Check:

Test Point	Signature
U15 Pin 2	0006
U15 Pin 5	0033
U15 Pin 6	000F

Other Signatures:

Test Point	Signature
U12 Pin 1	0010
U12 Pin 2	001U
U12 Pin 3,6	001U
U12 Pin 4	003U
U12 Pin 5,7 (GND)	0000
U12 Pin 11	0039
U12 Pin 12	0039
U12 Pin 13	0000
U12 Pin 14 (+5V)	003U
U14 Pin 5	003U
U14 Pin 6	0000
U15 Pin 1	0039

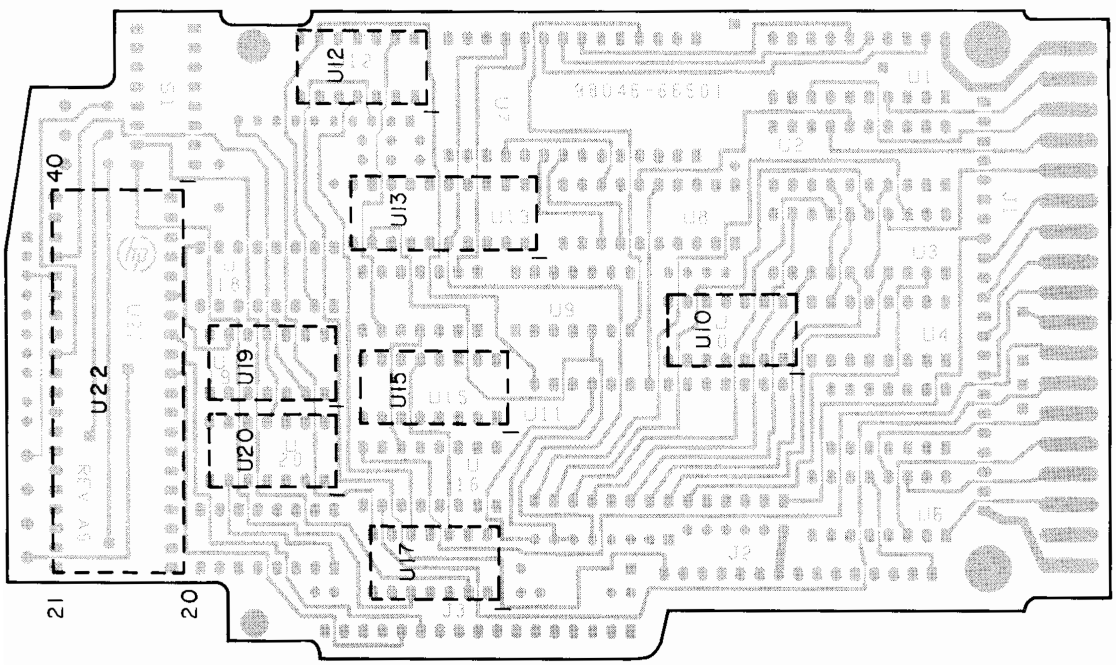


Figure 4-13. Test 4 Component Locator

NOTE
There is no Test 5

Test 6

This test checks the R6 and R7 register communications. On the A1 assembly (98046-66501), the test checks data flow from U2 to U22 and the I/O lines (P lines) from U22. On the A2 assembly (98046-66502), the external address latch, U12, is checked.

For this test, connect U22 Pin 35 to ground (TP1). There are three sections to this test.

Section 1

Set the analyzer as follows:

START	⎺⎽	(in)
STOP	⎽⎺	(out)
CLOCK	⎽⎺	(out)

Connect the signature analyzer as follows (see Figure 4-8A):

START to TP6
STOP to TP6
CLOCK to TP4

Compare the signatures observed with those shown in Table 4-6. All components tested in this section are on the A1 assembly (98046-66501).

Tests mainframe side of U2 (R6/R7), R6/R7 flag, R5 in.

Table 4-6. Test 6, Section 1, Signatures

First Check:		Other Signatures:			
Test Point	**Signature**	**Test Point**	**Signature**	**Test Point**	**Signature**
U2 Pin 3	A9A0	U10 Pin 4	8448	U21 Pin 8 (GND)	0000
U2 Pin 4	UFP1	U10 Pin 5	8C6C	U21 Pin 9	22FC
U2 Pin 7	499F	U10 Pin 11	ZHP8	U21 Pin 11	22FC
U2 Pin 8	5CH9	U10 Pin 12	2HP8	U21 Pin 12	0000
U2 Pin 10 (GND)	0000	U10 Pin 13	22FC	U21 Pin 13	22FC
U2 Pin 11	2HP8	U13 Pin 1	3F8H	U21 Pin 14	0000
U2 Pin 13	F247	U13 Pin 2	0000	U21 Pin 15,16 (+5V)	22FC
U2 Pin 14	28U5	U13 Pin 4	2HP8	U22 Pin 38	0000
U2 Pin 17	64H8	U13 Pin 6,20 (+5V)	22FC		
U2 Pin 18	2H46	U13 Pin 8	22FC		
U2 Pin 20 (+5V)	22FC	U13 Pin 10 (GND)	0000		
U13 Pin 12	22FC	U14 Pin 10	0000		
U2 Pin 14	3F8H	U14 Pin 11	0000		
U18 Pin 9	2HP8	U18 Pin 10	2HP8		
U22 Pin 6	2HP8	U18 Pin 11	22FC		
U22 Pin 31	7H70	U18 Pin 12	22FC		
		U18 Pin 13	7H70		
		U18 Pin 14	8448		
		U18 Pin 15	8C6C		

Section 2

Set the analyzer as follows:

START	_/‾	(out)
STOP	‾_	(in)
CLOCK	_/‾	(out)

Connect the signature analyzer as follows (see Figure 4-8B):

START to TP3
STOP to TP3
CLOCK to A1U22 Pin 8 (J3 Pin 12)

Compare the signatures observed with those shown in Table 4-7. All components tested in this section are on the A1 assembly (98046-66501).

Table 4-7. Test 6, Section 2, Signatures

First Check:

Test Point	Signature
U2 Pin 2	4C76
U2 Pin 5	AUF1
U2 Pin 6	3877
U2 Pin 9	867A
U2 Pin 12	53UH
U2 Pin 15	0037
U2 Pin 16	9F79
U2 Pin 19	20A0
U18 Pin 9	CC34

Other Signatures:

Test Point	Signature	Test Point	Signature
U2 Pin 1	0000	A2U12 Pin 12	0000
A2U5 Pin 1,10 (GND)	0000	A2U12 Pin 13	CC34
A2U5 Pin 2	CC34	A2U12 Pin 14	0000
A2U5 Pin 3	4C76	A2U12 Pin 16 (+5V)	CC34
A2U5 Pin 4	AUF1	A2U18 Pin 3	0000
A2U5 Pin 5	CC34	A2U18 Pin 4	CC34
A2U5 Pin 6	CC34	A2U18 Pin 5	0000
A2U5 Pin 7	3877	A2U18 Pin 6	CC34
A2U5 Pin 11	CC34	A2U18 Pin 7 (GND)	0000
A2U5 Pin 20 (+5V)	CC34	A2U18 Pin 14 (+5V)	CC34
A2U10 Pin 7 (GND)	0000		
A2U10 Pin 8	0000		
A2U10 Pin 9	CC34		
A2U10 Pin 10	CC34		
A2U10 Pin 14 (+5V)	CC34		
A2U12 Pin 1	CC34		
A2U12 Pin 2	CC34		
A2U12 Pin 3	CC34		
A2U12 Pin 8 (GND)	0000		
A2U12 Pin 9	CC34		
A2U12 Pin 10	CC34		
A2U12 Pin 11	CC34		

Section 3

Set the analyzer as follows:

START	⌄ (falling edge)	(in)
STOP	⌃ (rising edge)	(out)
CLOCK	⌃ (rising edge)	(out)

Connect the signature analyzer as follows (see Figure 4-8B):

START to TP3
STOP to TP3
CLOCK to A1U22 Pin 8 (J3 Pin 12)

Compare the signatures observed with those shown in Table 4-8. Components are tested on both the A1 and A2 assemblies.

Table 4-8. Test 6, Section 3, Signatures

First Check:

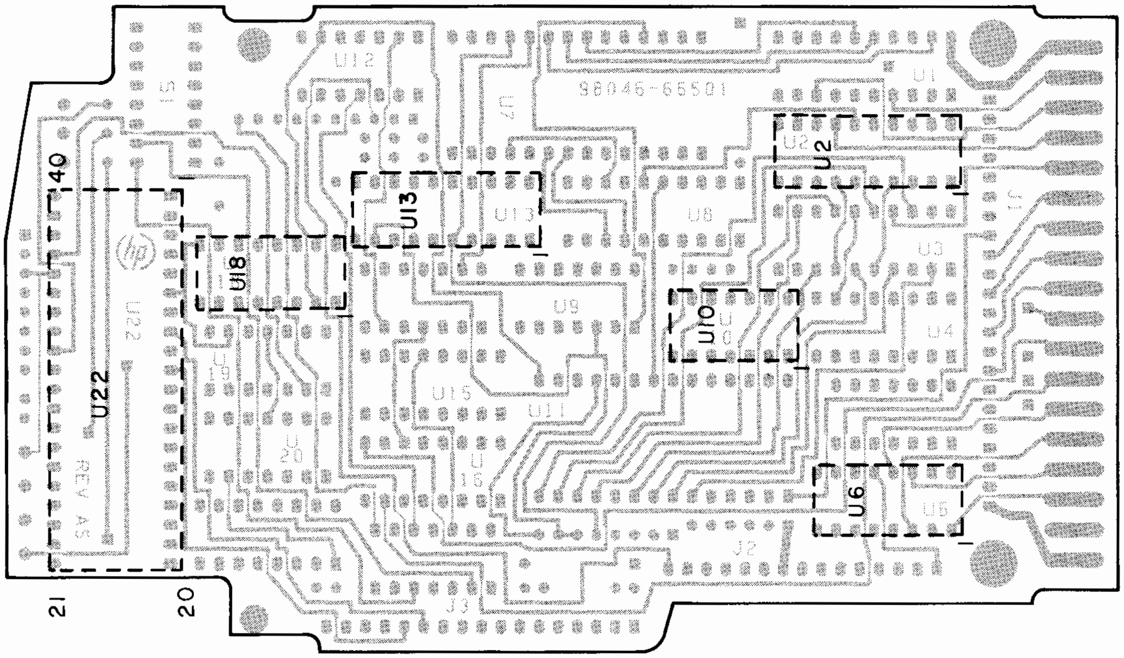
On A1 (98046-66501)

Test Point	Signature
A1U7 Pin 4	0001
A1U11 Pin 4	0001
A2U11 Pin 1,15	99FC
A2U11 Pin 1,15	99FC
A2U11 Pin 8 (GND)	0000
A2U11 Pin 16 (+5V)	99FA
A2U12 Pin 4	99FA
A2U12 Pin 5	99FA
A2U12 Pin 6	99FA
A2U12 Pin 7	99FA
A2U12 Pin 9	99FA
A2U12 Pin 10	99FC
A2U12 Pin 11	0001
A2U12 Pin 12	99FA

Other Signatures:

On A2 (98046-66502)

Test Point	Signature
A2U5 Pin 1,10 (GND)	0000
A2U5 Pin 2	0001
A2U5 Pin 3	0001
A2U5 Pin 3	0001
A2U5 Pin 4	99FA
A2U5 Pin 5	99FC
A2U5 Pin 6	99FA
A2U5 Pin 7	99FA
A2U5 Pin 11	99FA
A2U5 Pin 20 (+5V)	99FA
A2U10 Pin 7 (GND)	0000
A2U10 Pin 8	0000
A2U10 Pin 9	99FA
A2U10 Pin 10	99FA
A2U10 Pin 14 (+5V)	99FA
A2U12 Pin 1	99FA
A2U12 Pin 2	99FA
A2U12 Pin 3	99FC
A2U12 Pin 13	0001
A2U12 Pin 14	0000
A2U18 Pin 3	0000
A2U18 Pin 4	99FA
A2U18 Pin 5	0000
A2U18 Pin 6	99FA
A2U18 Pin 7 (GND)	0000
A2U18 Pin 14 (+5V)	99FA



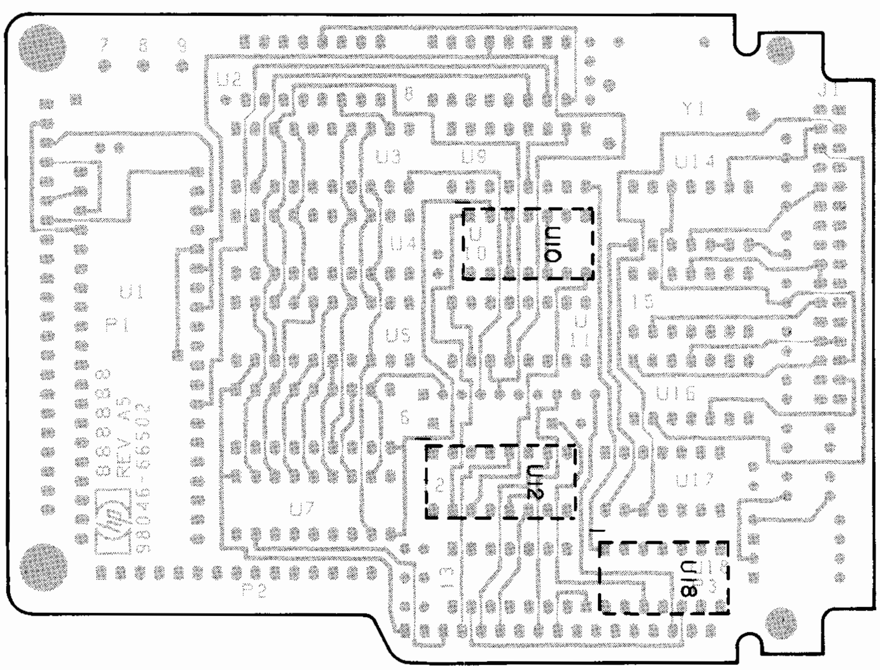


Figure 4-14. Test 6 Component Locators

Test 7

This test checks the TxFIFO, the RxFIFO and associated circuits. In the different sections, data is written into the TxFIFO from the mainframe and data is written into the RxFIFO from the microprocessor.

For this test, connect U22 Pin 35 (TP1) and U22 Pin 24 (TP2) to ground.

There are three sections to this test.

Section 1

Set the analyzer as follows:

START	⌐	(out)
STOP	⌐	(out)
CLOCK	⌐	(out)

Connect the signature analyzer as follows (see Figure 4-9A):

START to J2 Pin 7
STOP to J2 Pin 8
CLOCK to TP4

Compare the signatures observed with those shown in Table 4-9. All components tested in this section are on the A1 assembly (98046-66501).

Tests mainframe side of TxFIFO and RxFIFO (U1, U3, U7, U11), Flglsts decoder (U16), Interrupt latch (U15).

Table 4-9. Test 7, Section 1, Signatures

First Check:

Test Point	Signature	Test Point	Signature
U3 Pin 3	CDUF	U7 Pin 22	75U6
U3 Pin 5	0505	U7 Pin 23	6P01
U3 Pin 7	3C83	U7 Pin 26	0373
U3 Pin 9	CIF5	U7 Pin 27	5C46
U3 Pin 11	7269	U7 Pin 28	U04F
U3 Pin 13	16CP	U12 Pin 8	PA0P
U3 Pin 15	8FP4	U16 Pin 7	24UP
U3 Pin 17	13FF	U16 Pin 9	12PC
U7 Pin 1	125U	**U17 Pin 3	A188
U7 Pin 17	0UHU	*U17 Pin 6	377A or HH5F
U7 Pin 20	76F0	U22 Pin 29	50F4
U7 Pin 21	08FP		

** This is for s.c. 2,4 or 6. U17.3 and .6 signatures interchange for s.c. 8, 10 or 12.

* 4 possible signatures, all correct.

Other Signatures:

Test Point	Signature
U1 Pin 1	0000
U1 Pin 2	125U
U1 Pin 3	C9UF
U1 Pin 4	0505
U1 Pin 5	0U4F
U1 Pin 6	5C46
U1 Pin 7	3C83
U1 Pin 8	CIF5
U1 Pin 9	0373
U1 Pin 10 (GND)	0000
U1 Pin 11	84CF
U1 Pin 12	6P01
U1 Pin 13	7269
U1 Pin 14	16CP
U1 Pin 15	75U6
U1 Pin 16	08FP
U1 Pin 17	8FP4
U1 Pin 18	13FF
U1 Pin 19	76F0
U1 Pin 20 (+5V)	A188
U3 Pin 1	0000
U3 Pin 2	11AP
U3 Pin 4	4C29
U3 Pin 6	1AH5
U3 Pin 8	9882
U3 Pin 10 (GND)	0000
U3 Pin 12	H283
U3 Pin 14	7H5U
U3 Pin 16	229H
U3 Pin 18	56P5
U3 Pin 19	H35P

Test Point	Signature
U3 Pin 20	A188
U7 Pin 3	50F4
*U7 Pin 19	5462
U7 Pin 25	HAUU
U9 Pin 7 (GND)	0000
U9 Pin 8	OUHU
U9 Pin 10,13,14 (+5V)	A188
U9 Pin 11	84CF
U9 in 12	PAOP
*U10 Pin 1	U5PA
U10 Pin 2	AUF1
*U10 Pin 3	5A05
U10 Pin 7 (GND)	0000
U10 Pin 14 (+5V)	A188
U11 Pin 2 (−12V)	0000
U11 Pin 3	PF43
U11 Pin 4	A188
U11 Pin 5	72H6
U11 Pin 6	11AP
U11 Pin 7	4C29
U11 Pin 8	1AH5
U11 Pin 9	9882
U11 Pin 10	A188
U11 Pin 11	H283
U11 Pin 12	7H5U
U11 Pin 13	229H
U11 Pin 14	56P5
U11 Pin 15	60AU
U11 Pin 16 (GND)	0000
*U11 Pin 19	HU3U
U11 Pin 24 (+5V)	A188

** This is for s.c. 2,4 or 6. U17.3 and .6 signatures interchange for s.c. 8, 10 or 12.

* 4 possible signatures, all correct.

Section 2

Set the analyzer as follows:

START	⌊	(in)
STOP	⌈	(out)
CLOCK	⌈	(out)

Connect the signature analyzer as follows (see Figure 4-9B):

START to TP3
STOP to TP3
CLOCK to J3 Pin 12

Compare the signatures observed with those shown in Table 4-10. Components tested in this section are all on the A1 assembly.

Tests Proc side of TxFIFO (U7)

Table 4-10. Test 7, Section 2, Signatures

First Check:

Test Point	Signature
U7 Pin 3	0000
U7 Pin 15	1C9U
U8 Pin 2	569P
U8 Pin 5	2UA3
U8 Pin 6	1U11
U8 Pin 9	9C7C
U12 Pin 12	2C6C
U8 Pin 15	HA30
U8 Pin 16	HC32
U8 Pin 19	97U1

Other Signatures:

Test Point	Signature
A1U7 Pin 2 (−12V)	0000
A1U7 Pin 4	133H
A1U7 Pin 5	PUHC
A1U7 Pin 6	569P
A1U7 Pin 7	2UA3
A1U7 Pin 8	1U11
A1U7 Pin 9	9C7C
A1U10 Pin 10,24 (−5V)	133H
A1U7 Pin 11	2C6C
A1U7 Pin 12	26H6
A1U7 Pin 13	HC32
A1U7 Pin 14	97U1
A1U7 Pin 16 (GND)	0000
A1U8 Pin 1	UFP6
A1U8 Pin 3	569P
A1U8 Pin 4	2UA3
A1U8 Pin 7	1U11
A1U8 Pin 8	9C7C
A1U8 Pin 10 (GND)	0000
A1U8 Pin 11,20 (+5V)	133H
A1U8 Pin 13	2C6C
A1U8 Pin 14	26H6
A1U8 Pin 17	HC32
A1U8 Pin 18	97U1
A1U13 Pin 7	PUHC
A1U13 Pin 13	UFP6
A1U13 Pin 19 (GND)	0000

Test Point	Signature
A2U5 Pin 1,10 (GND)	0000
A2U5 Pin 2	UFP6
A2U5 Pin 3	569P
A2U5 Pin 4	2UA3
A2U5 Pin 5	UFP6
A2U5 Pin 6	133H
A2U5 Pin 7	1U11
A2U5 Pin 20 (+5V)	133H
A2U10 Pin 7 (GND)	0000
A2U10 Pin 8	0000
A2U10 Pin 9	133H
A2U10 Pin 10	133H
A2U10 Pin 14 (+5V)	133H
A2U12 Pin 1	133H
A2U12 Pin 2	133H
A2U12 Pin 3	UFP6
A2U12 Pin 8 (GND)	0000
A2U12 Pin 9	UFP6
A2U12 Pin 10	133H
A2U12 Pin 11	133H
A2U12 Pin 12	PUHC
A2U12 Pin 13	UFP6
A2U12 Pin 14	0000
A2U12 Pin 16 (+5V)	133H
A2U18 Pin 3	0000
A2U18 Pin 4	133H
A2U18 Pin 5	0000
A2U18 Pin 5	0000
A2U18 Pin 6	133H
A2U18 Pin 7 (GND)	0000
A2U18 Pin 14 (+5V)	133H

Section 3

NOTE
The ESK test connector must be installed on the A2 output connector to perform this test.

Set the analyzer as follows:

START	╲	(in)
STOP	╱	(out)
CLOCK	╱	(out)

Connect the signature analyzer as follows (see Figure 4-9C):

START to TP3
STOP to TP3
CLOCK to A2U10 Pin 3 (TP9)

Compare the signatures observed with those shown in Table 4-11. Components tested in this section are located on both the A1 and A2 assemblies.

Tests µProc side of TxFIFO (U11) and Rx interrupt FF (U21), Modem control register (A2U4), µProc side of bit-rate generators (A2U2 and U8, A2U3), line drivers and receivers (A2U14, U15, U16 and U17) and line side of modem status register (A2U11), address decoder (AwU12).

Table 4-11. Test 7, Section 3, Signatures

First Check:

Test Point	Signature	Test Point	Signature
A1U11 Pin 1	2F0C	A2U8 Pin 12	0121
A1U11 Pin 17	F08H	A2U8 Pin 13	FU06
A1U11 Pin 20	5PC0	A2U8 Pin 14	7464
A1U11 Pin 21	8334	A2U11 Pin 2	07F2
A1U11 Pin 22	6417	A2U11 Pin 4	5U72
A1U11 Pin 23	12F1	A2U11 Pin 6	64U0
A1U11 Pin 26	9629	A2U11 Pin 10	057C
A1U11 Pin 27	562H	A2U11 Pin 12	1C37
A1U11 Pin 28	4C06	A2U11 Pin 14 (+5V)	7F4A
A1U18 Pin 4	6538	A2U12 Pin 4	F77P
*A1U21 Pin 6	2965	A2U12 Pin 5	C116
A1U21 Pin 9	2U08	A2U12 Pin 6	810P
A2U2 Pin 11	8F20	A2U12 Pin 7	3H16
A2U2 Pin 12	5326	A2U12 Pin 9	9474
A2U2 Pin 13	98UH	A2U12 Pin 10	7F4A
A2U2 Pin 14	PAA6	A2U12 Pin 11	7F4A
A2U4 Pin 2	2889	A2U12 Pin 12	224P
A2U8 Pin 11	HU4H		

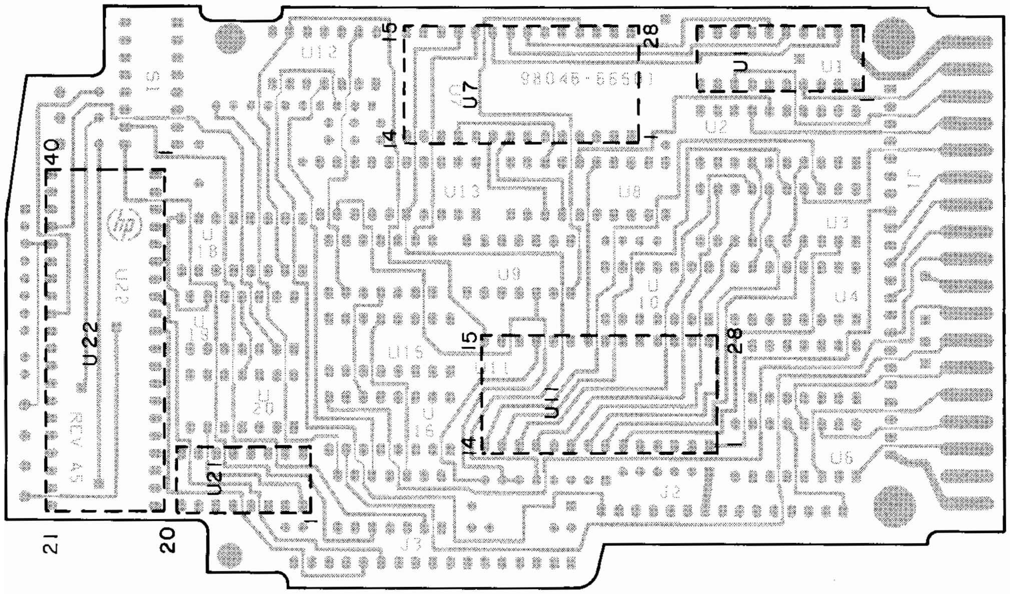
Other Signatures:

Test Point	Signature	Test Point	Signature
A1U14 Pin 8	3F71	A2U3 Pin 5	98UH
A1U14 Pin 9	403C	A2U3 Pin 6	5326
A1U18 Pin 2	1972	A2U3 Pin 7	562H
A1U18 Pin 3	5342	A2U3 Pin 8	9629
A1U20 Pin 4	7F4A	A2U3 Pin 9	8F20
A1U20 Pin 5	7F4A	A2U3 Pin 11	F77P
A1U20 Pin 6	7F4A	A2U3 Pin 12	7464
A1U21 Pin 7	552U	A2U3 Pin 13	12F1
A1U21 Pin 8 (GND)	0000	A2U3 Pin 14	6417
A1U21 in 10	5342	A2U3 Pin 15	FU6
A1U21 Pin 11	C116	A2U3 Pin 16	0121
A1U21 Pin 12	0000	A2U3 Pin 17	8334
A1U21 Pin 13	HU26	A2U3 Pin 18	5PC0
A1U21 Pin 14	0000	A2U3 Pin 19	HU4H
A1U21 Pin 1516 (+5V)	7F4A	A2U3 Pin 20 (+5V)	7F4A
A2U3 Pin 1,10 (GND)	0000	A2U4 Pin 1	0000
A2U3 Pin 2	PAA6	A2U4 Pin 2	2889
A2U3 Pin 3	2FOC	A2U4 Pin 3	2FOC
A2U3 Pin 4	4C06	A2U4 Pin 4	4C06

*4 possible correct signatures

Other Signatures cont.:

Test Point	Signature
A2U4 Pin 5	1C37
A2U4 Pin 6	057C
A2U4 Pin 7	562H
A2U4 Pin 8	9629
A2U4 Pin 9	64U0
A2U4 Pin 10 (GND)	0000
A2U4 Pin 11	810P
A2U4 Pin 12	5U72
A2U4 Pin 13	12F1
A2U4 Pin 14	6417
A2U4 Pin 15	07F2
A2U4 Pin 20 (+5V)	7F4A
A2U5 Pin 1	0000
A2U5 Pin 2	1874
A2U5 Pin 3	2FOC
A2U5 Pin 4	4C06
A2U5 Pin 5	286F
A2U5 Pin 6	7F4A
A2U5 Pin 7	562H
A2U5 Pin 8	9629
A2U5 Pin 9	691F
A2U5 Pin 10 (GND)	0000
A2U5 Pin 11	7F4A
A2U5 Pin 12	H9P6
A2U5 Pin 13	12F1
A2U5 Pin 16	2840
A2U5 Pin 17	8334
A2U5 Pin 20 (+5V)	7F4A
A2U10 Pin 7 (GND)	0000
A2U10 Pin 8	0000
A2U10 Pin 9	7F4A
A2U10 Pin 10	7F4A
A2U10 Pin 14 (+5V)	7F4A
A2U12 Pin 1	7F4A
A2U12 PIN 2	Unstable
A2U12 Pin 3	286F
A2U12 Pin 8 (GND)	0000
A2U12 Pin 13	1874
A2U12 Pin 14	0000
A2U12 Pin 15	unstable
A2U12 Pin 16 (+5V)	7F4A
A2U13 Pin 7 (GND)	0000
A2U13 Pin 8	0000
A2U13 Pin 9	0000
A2U13 Pin 10	2849
A2U13 Pin 12	0000
A2U13 Pin 13	415F
A2U13 Pin 14 (+5V)	7F4A
A2U14 Pin 1 (−12V)	0000
A2U14 Pin 8	7C88
A2U14 Pin 9,10	07F2
A2U14 Pin 11	2338
A2U14 Pin 12,13	5U72
A2U14 Pin 14 (+12V)	7F4A
A2U15 Pin 1	2338
A2U15 Pin 3	5U72
A2U15 Pin 4	18CA
A2U15 Pin 6	64U0
A2U15 Pin 7 (GND)	0000
A2U15 Pin 8	1C37
A2U15 Pin 10	677H
A2U15 Pin 11	057C
A2U15 Pin 13	7931
A2U15 Pin 15 (+5V)	7F4A
A2U16 Pin 7 (GND)	0000
A2U16 Pin 8	07F2
A2U16 Pin 10	7C88
A2U16 Pin 14 (+5V)	7F4A
A2U17 Pin (−12V)	0000
A2U17 Pin 2	64U0
A2U17 Pin 3	18CA
A2U17 Pin 4,5	057C
A2U17 Pin 6	7931
A2U17 Pin 8	677H
A2U17 Pin 9,10	1C37
A2U17 Pin 14 (−12V)	7F4A
A2U18 Pin 3	0000
A2U18 Pin 4	7F4A
A2U18 Pin 5	0000
A2U18 Pin 6	7F4A
A2U18 Pin 7 (GND)	0000
A2U18 Pin 10	415F
A2U18 Pin 11	3H16
A2U18 Pin 12	7F4A
A2U18 Pin 13	0000
A2U18 Pin 14 (+5V)	7F4A



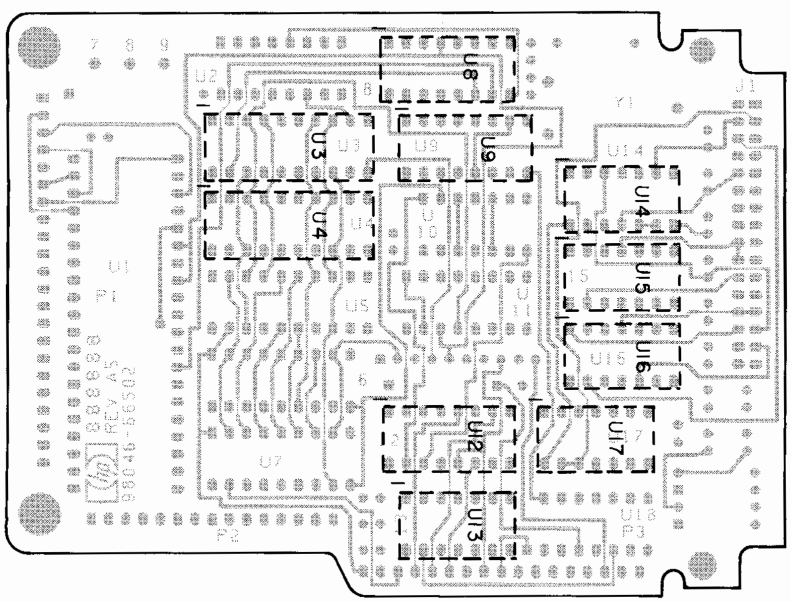


Figure 4-15. Test 7 Component Locators

Chapter 5
Replaceable Parts

This chapter provides parts ordering information for the 98046. This information includes the replaceable parts list, schematic diagram and component locators.

Table 5-1 lists the 98046 replaceable parts. Here is a description of each table column.

Part Number Check Digit

HP Part No.

Description of the Part

Reference Designator	CD	hp Part No.	TQ	Description

Component reference designator, shown on schematic diagram and component locator

Total quantity of a part used on an assembly. The quantity is given the first time a part is listed for a particular assembly. Thus, some parts used more than once on an assembly may not have a number in this column.

The major assemblies are shown in darker type. The components listed after a major assembly heading are a part of the major assembly.

Table 5-1. Replaceable Parts

	REFERENCE DESIGNATOR	CD	-hp- PART NO.	TQ	DESCRIPTION
		8	0050-2015	1	Left Case
		9	0050-2016	1	Right Case
		5	2200-0510	2	4-40, .75 in. Long, Flat Head, Pozidriv Screw
		5	2200-0536	8	4-40, .438 in. Long, Flat Head, Pozidrive Screw
		4	7120-8188	1	Data Comm Label-STD
		4	7120-8196	1	Data Comm Label-OPT 1
	A1	**9**	**98046-66501**		**Processor Assembly**
	C1	7	0180-0229	1	C-F: 33 μF 10 V
	C2, C3	5	0160-0576	7	C-F: .1 μF 20% 50 V
	C4	8	0180-0197	1	C-F: 2.2 μF 20 V
	C5, C6	5	0160-0576		C-F: .1 μF 20% 50 V
	C7	0	0160-0571	1	C-F: 470 pF 20%
	C8	5	0160-0576		C-F: .1 μF 20% 50 V
	C9	2	0160-4385	1	C-F: 15 pF 5%
	C10, C11	5	0160-0576		C-F: .1 μF 20% 50 V
	J1	9	1251-5956	1	22-Pin Connector
	J2	9	1251-5675	1	15-Pin Connector
	J3	7	1251-5798	1	17-Pin Connector
	R1	4	1810-0278	1	R-Network 3.3 K (10 Pin)
	R2	2	1810-0367	1	R-Network 4.7 K (6 Pin)
	R3	6	1810-0204	1	R-Network 1 K (8 Pin)
	R4	3	1810-0206	1	R-Network 10 K (8 Pin)
	S1	2	3100-3364	1	Switch: SW-53137
	TP1-TP7	0	0380-0630		Test Points
	U1, U2	5	1820-2216	2	IC: 74C374
	U3	2	1820-1794	1	IC: 81LS95
	U4	8	1820-1427	1	IC: 74LS156
	U5	0	1820-1297	1	IC: 74LS266
	U6	8	1820-1245	1	IC: 74LS155
	U7	9	1818-0277	2	IC: AM2813A
	U8	4	1820-2215	1	IC: 74C373
	U9	8	1820-1112	1	IC: 74LS74
	U10	6	1820-1201	1	IC: 74LS08
	U11	9	1818-0277		IC: AM2813A
	U12	8	1820-1568	1	IC: 74LS125
	U13	1	1820-1917	1	IC: 74LS240
	U14	1	1820-1199	1	IC: 74LS04
	U15	0	1820-1445	1	IC: 74LS375
	U16	9	1820-1238	1	IC: 74LS253
	U17	0	1820-1198	1	IC: 74LS03
	U18	5	1820-1440	1	IC: 74LS279
	U19	7	1820-1202	1	IC: 74LS10
	U20	3	1820-1208	1	IC: 74LS32
	U21	3	1820-1282	1	IC: 74LS109
	U22	6	1820-2431	1	IC: 8048 Processor
	Y1	2	0410-0738	1	6 MHz Crystal
		3	0380-0635	2	Standoff
		4	1200-0817	1	40-Pin Socket for U22

	REFERENCE DESIGNATOR	CD	-hp- PART NO.	TQ	DESCRIPTION
	A2	**0**	**98046-66502**		**USART Assembly**
	C1		0180-0229	1	C-F: 33 μF 10 V
	C2, C3	5	0160-0576	8	C-F: .1 μF 20% 50 V
	C8, C9	6	0160-4503	2	C-F: 56 pF
	C5-C7	5	0160-0576		C-F: .1 μF 20% 50 V
	C4	3	0180-0374	1	C-F: 10 μF 20 V
	C10, C18, C20	5	0160-0576		C-F: .1 μF 20% 50 V
	C11-17, C19	4	0160-3694	8	C-F: 330 pF 10%
	CR1, CR2	2	1901-0025	2	DIO: SI
	J1	5	1251-6467	1	2 x 16 Connector
	P1-P3	5	1251-4326	2	Connector Pins for J2, J4 and J5 (36 Pins)
	R1	7	0683-1065	1	10 MΩ 5% ¼ W
	R2	4	1810-0278	1	R-Network: 3.3 KΩ (10 Pin)
	R3, R4	4	0683-3315	2	330 Ω 5% ¼ W
	TP1-TP3	0	0380-0630		Test Points
	U1	1	1820-2288	1	IC: Z-80 SIO (USART)
	U2	5	1820-1854	2	IC: HD4702
	U3,U4	5	1820-2216	2	IC: 74C374
	U5	7	1820-1997	1	IC: 74LS374
	U6, U7	0	1818-0955	2	IC: HM6514
	U8	5	1820-1854		IC: HD4702
	U9	8	1820-1195	1	IC: 74LS175
	U10	9	1820-1197	1	IC: 74LS00
	U11	3	1820-1266	1	IC: 80C97
	U12	8	1820-1245	1	IC: 74LS155
	U13	6	1820-1205	1	IC: 74LS21
	U14	5	1820-0509	2	IC: MC1488
	U15, U16	8	1820-0990	2	IC: MC1489
	U17	5	1820-0509		IC: MC1488
	U18	1	1820-1199	1	IC: 74LS04
	Y1	0	0410-0736	1	2.4576 MHz Xtal
		3	0380-0635	2	Standoff
		4	1200-0817	1	40-Pin Socket for U1
		7	**8120-3114**		**Standard Cable Assembly**
		8	8120-3115		Option 001 Cable Assembly

Standard Test Connector, 1251-6624 Wiring Table

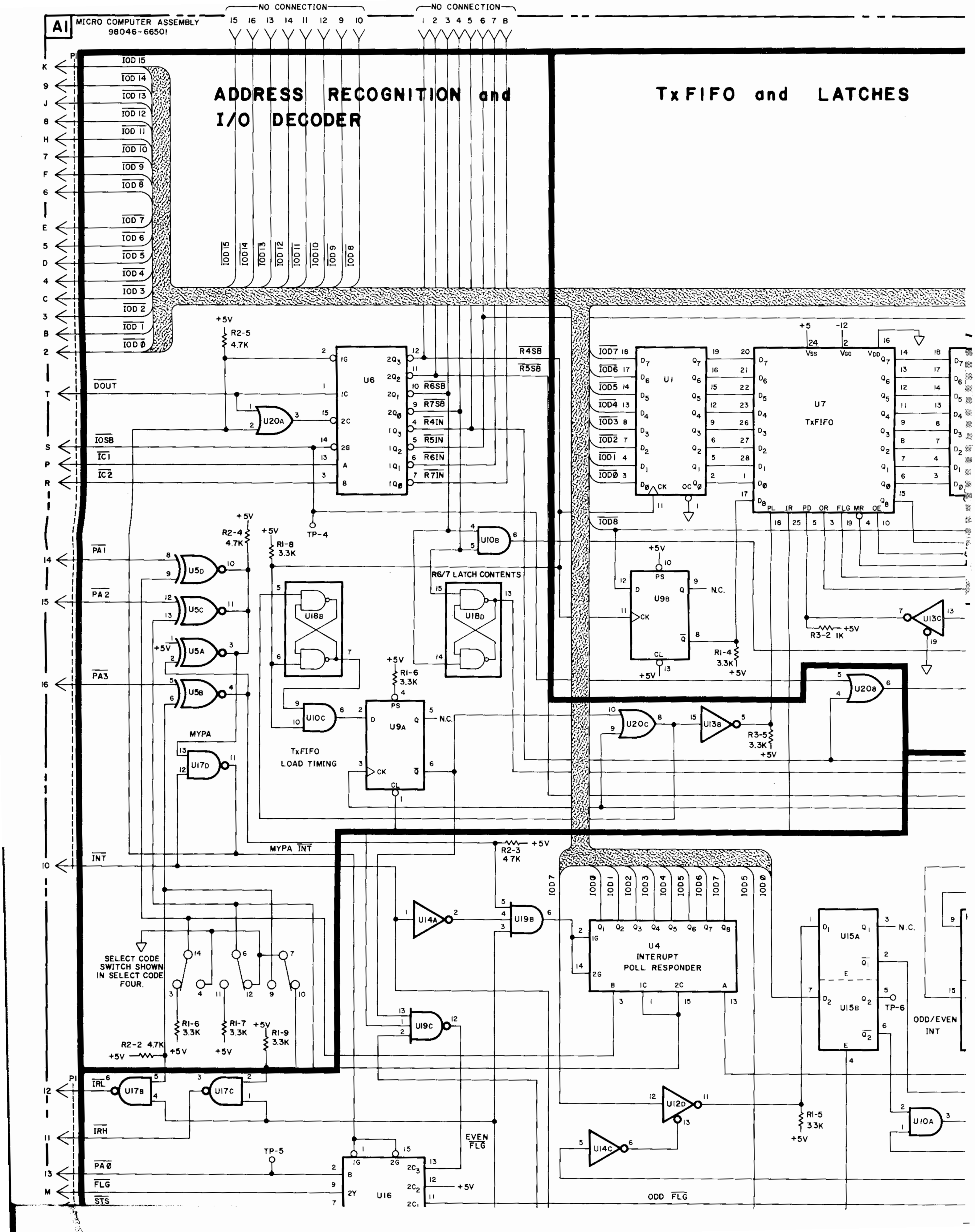
From Pin #	To Pin #	From Pin #	To Pin #
1	NC	14	NC
2	3	15	NC
3	2	16	NC
4	8	17	24
5	NC	18	NC
6	20	19	12
7	NC	20	6
8	4	21	NC
9	NC	22	NC
10	NC	23	NC
11	NC	24	17
12	19	25	NC
13	NC		

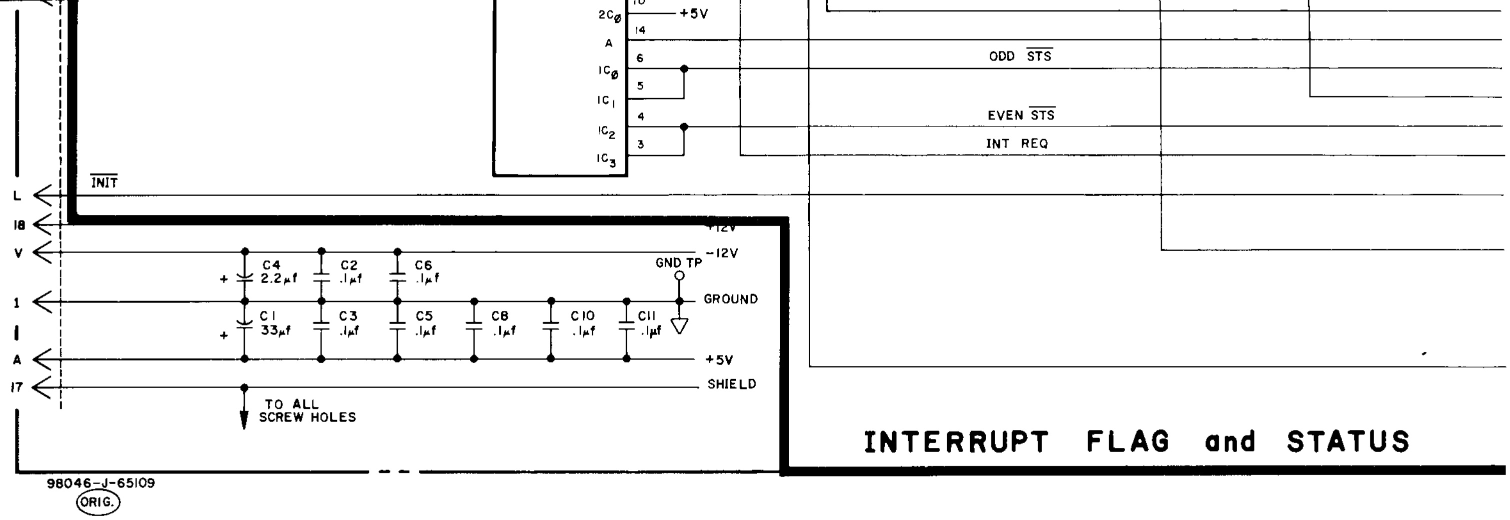
Option 001 Test Connector, 1251-6625 Wiring Table

From Pin #	To Pin #	From Pin #	To Pin #
1	NC	14	25
2	3	15	23
3	2	16	NC
4	5, 8 & 22	17	24
5	4, 8 & 22	18	NC
6	20	19	12
7	NC	20	6
8	4, 5 & 22	21	NC
9	NC	22	4, 5 & 8
10	NC	23	15
11	NC	24	17
12	19	25	14
13	NC		

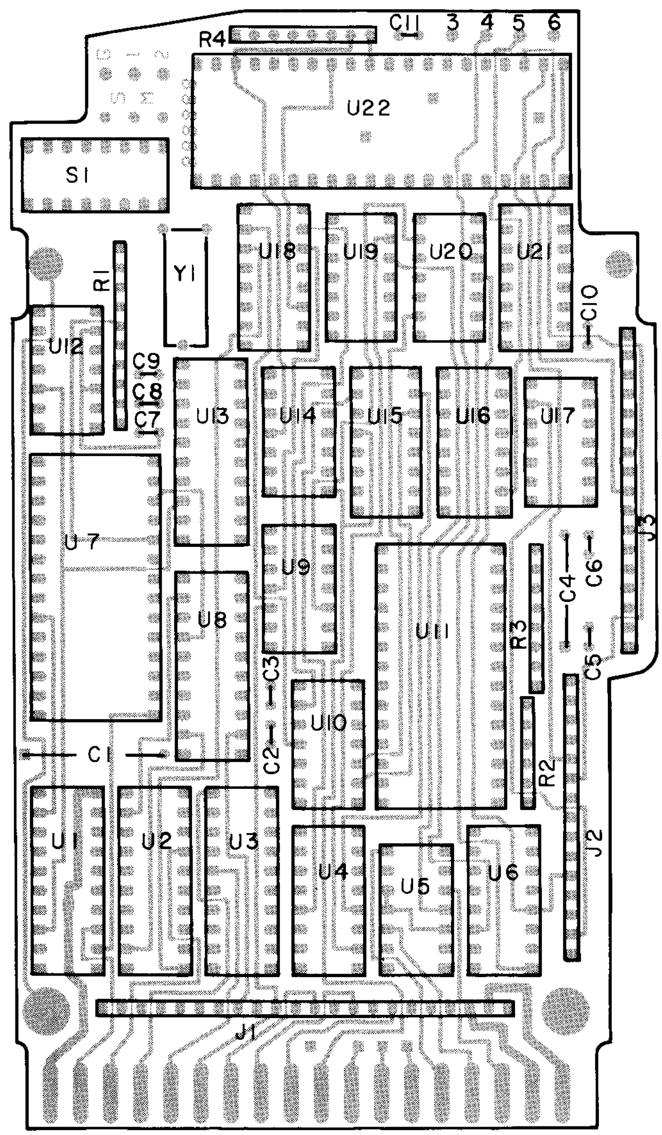
98046 Test Connector (ESK), 98046-67906 Wiring Table

From Pin #	To Pin #	From Pin #	To Pin #
1	NC	2	Key
3	5	4	6
5	3	6	4
7	NC	8	12
9	NC	10	NC
11	NC	12	8
13	18	14	30
15	22	16	NC
17	NC	18	13
19	NC	20	NC
21	NC	22	15
23	NC	24	26
25	NC	26	24
27	28	28	27
29	32	30	14
31	NC	32	29

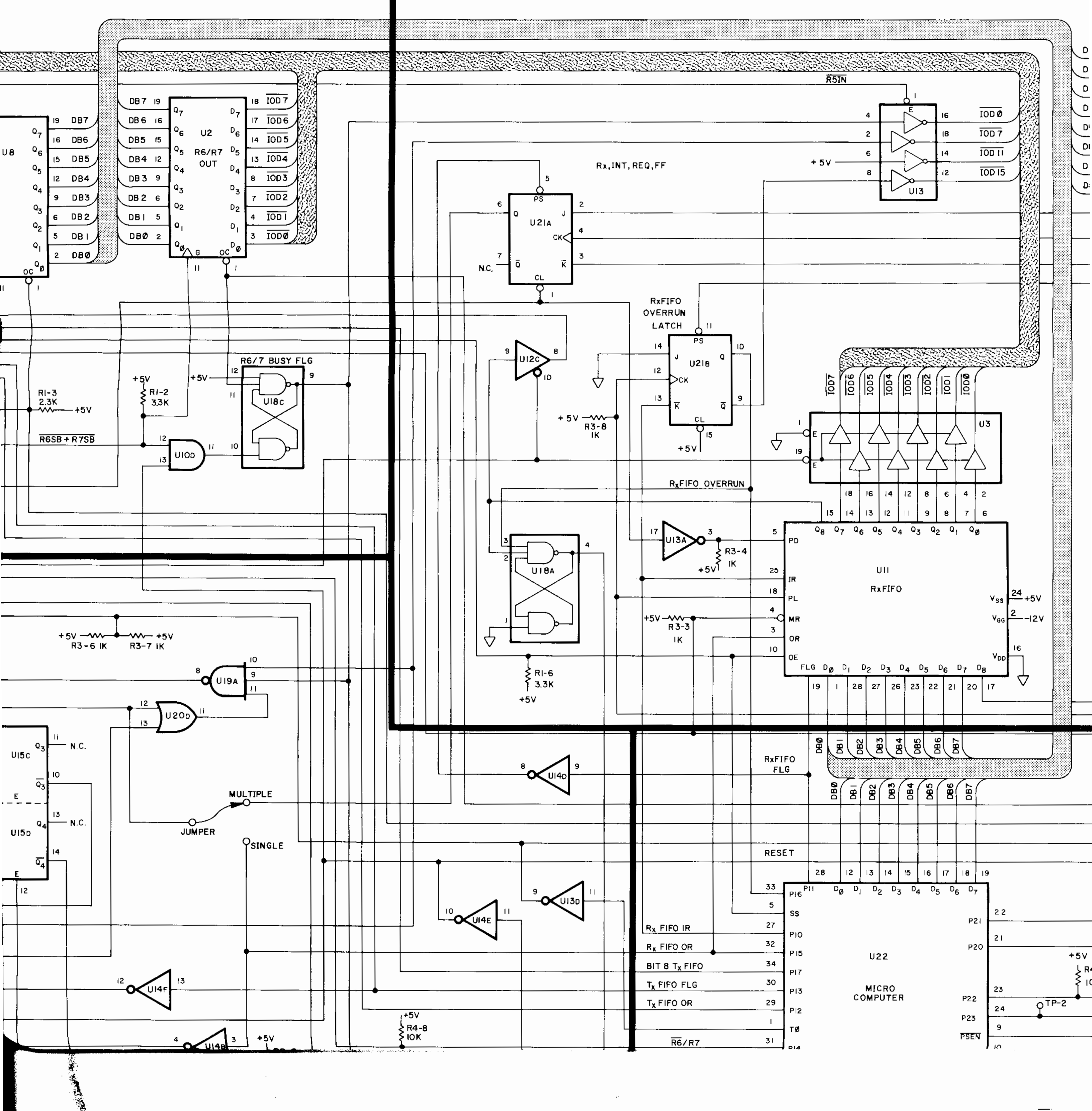

A1 MICRO COMPUTER ASSEMBLY
98046-66501
NO CONNECTION
NO CONNECTION
ADDRESS RECOGNITION and I/O DECODER
TxFIFO and LATCHES
U6
U20A
U1
U7
TxFIFO
U10B
U5D
U5C
U5A
U5B
U18B
R6/7 LATCH CONTENTS
U18D
U9B
U13C
U20B
U10C
U9A
TxFIFO
LOAD TIMING
U20C
U13B
MYPA
U17D
MYPA INT
U14A
U19B
U4
INTERUPT
POLL RESPONDER
U15A
U15B
ODD/EVEN
INT
SELECT CODE
SWITCH SHOWN
IN SELECT CODE
FOUR.
U19C
U17B
U17C
U12D
U14C
U10A
U16
EVEN
FLG
ODD FLG
TP-4
TP-5
TP-6

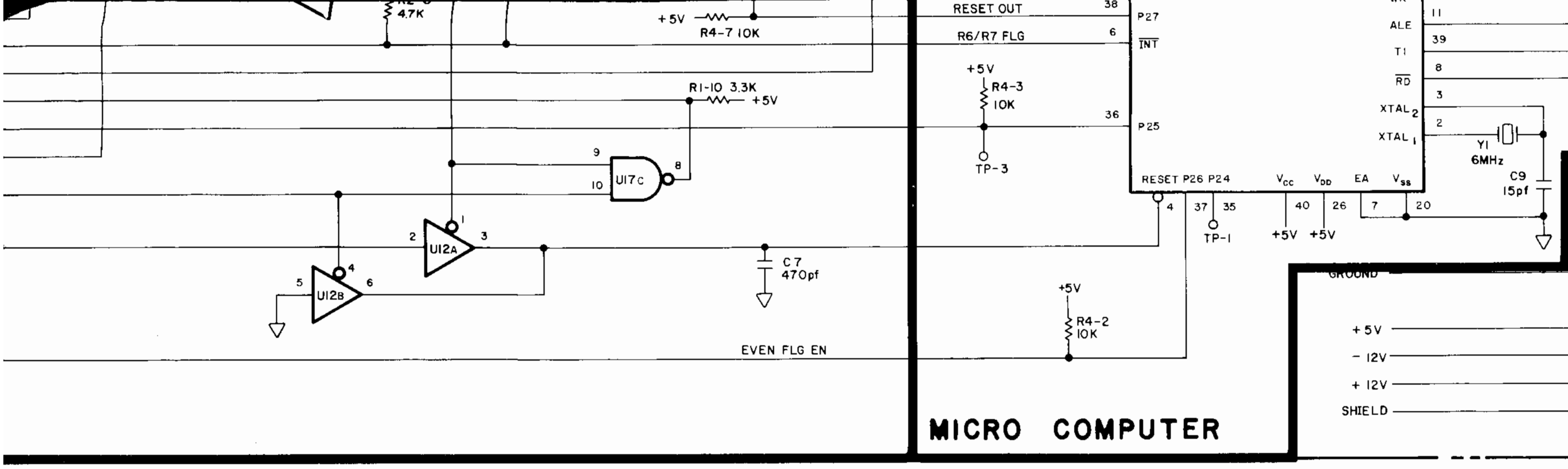


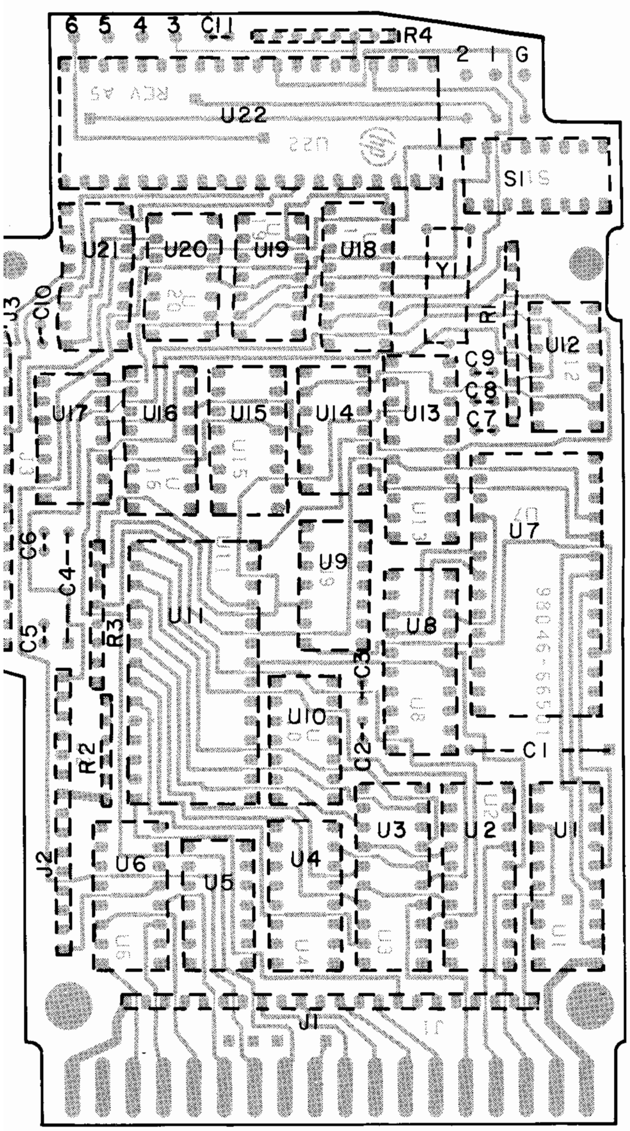
A1
Component Side



RxFIFO, R4IN, R5IN



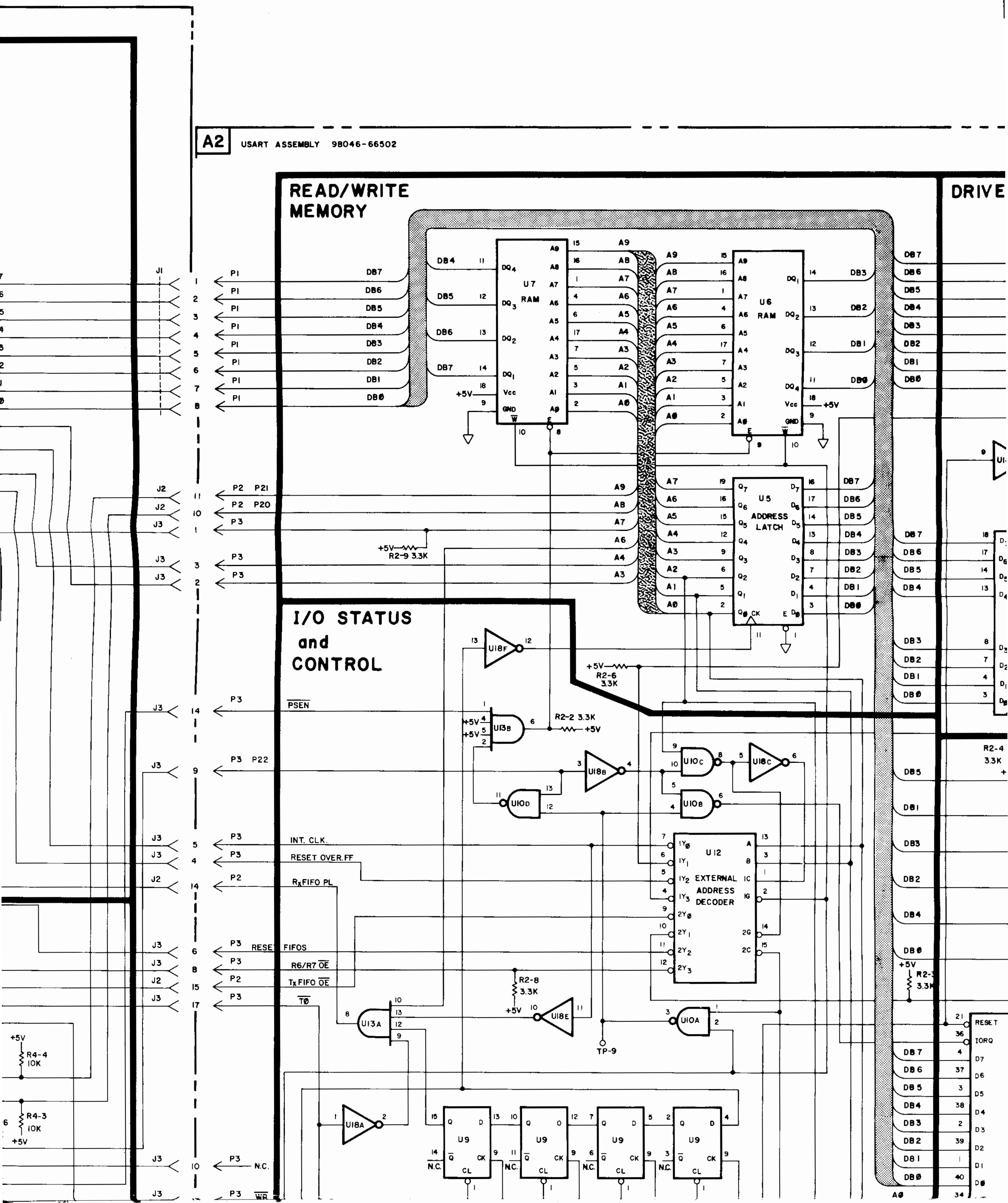


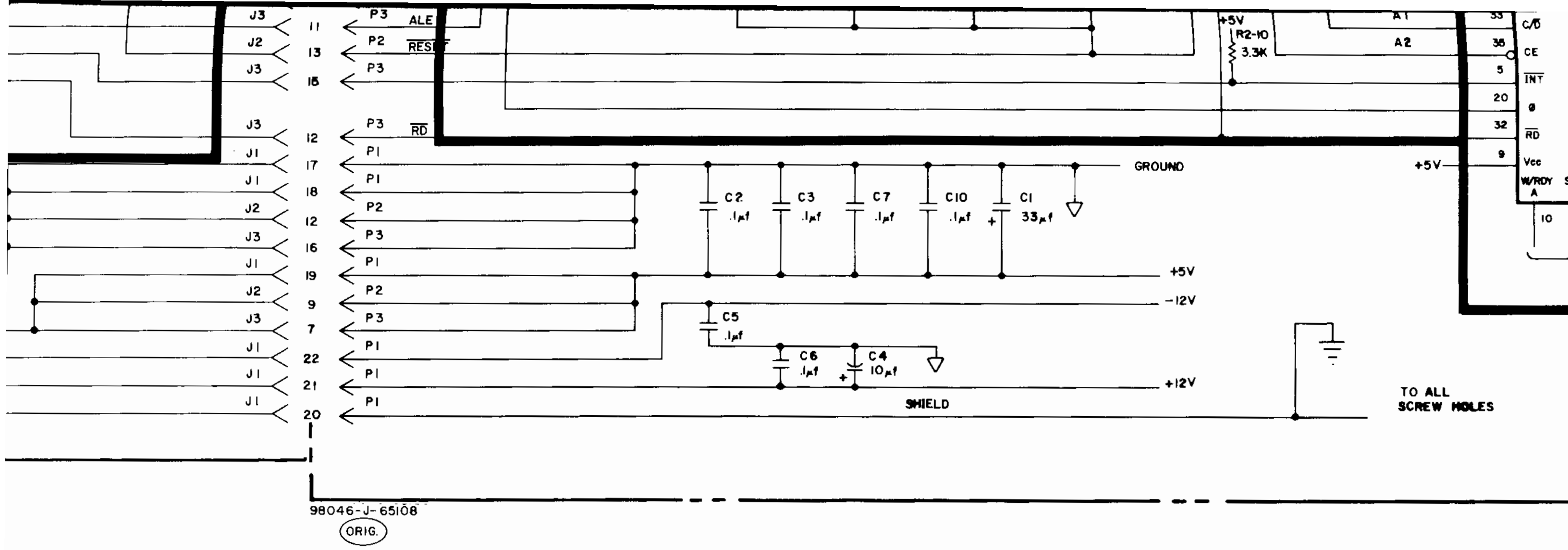


A1
Circuit Side

Schematic sections tested by the various signature

Signature Analysis Test Number	Tests Compo
1	Address recogniti
2	Address recogniti
3	Interrupt, flag and TxFIFO and latch RxFIFO, R4IN, R
4	Interrupt, flag and
Test 5 – Not Used	
6 Section 1	TxFIFO and latch Microcomputer
6 Section 2	Microcomputer
6 Section 3	Microcomputer I/O status and co
7 Section 1	TxFIFO and latch
7 Section 2	Microcomputer RxFIFO, R4IN, R
7 Section 3	RxFIFO, R4IN, R Driver control and I/O status and co


A2 USART ASSEMBLY 98046-66502
READ/WRITE MEMORY
DRIVE
U7 RAM
U6 RAM
U5 ADDRESS LATCH
I/O STATUS and CONTROL
U12 EXTERNAL ADDRESS DECODER
PSEN
INT. CLK.
RESET OVER.FF
RxFIFO PL
RESET FIFOS
R6/R7 OE
TxFIFO OE
T0
WR
R2-9 3.3K
R2-6 3.3K
R2-2 3.3K
R2-8 3.3K
R4-4 10K
R4-3 10K
TP-9
RESET
IORQ



analysis tests.

ents in These Schematic Sections

n and I/O decoder

n and I/O decoder

status

s

IN

status

s

ntrol

s

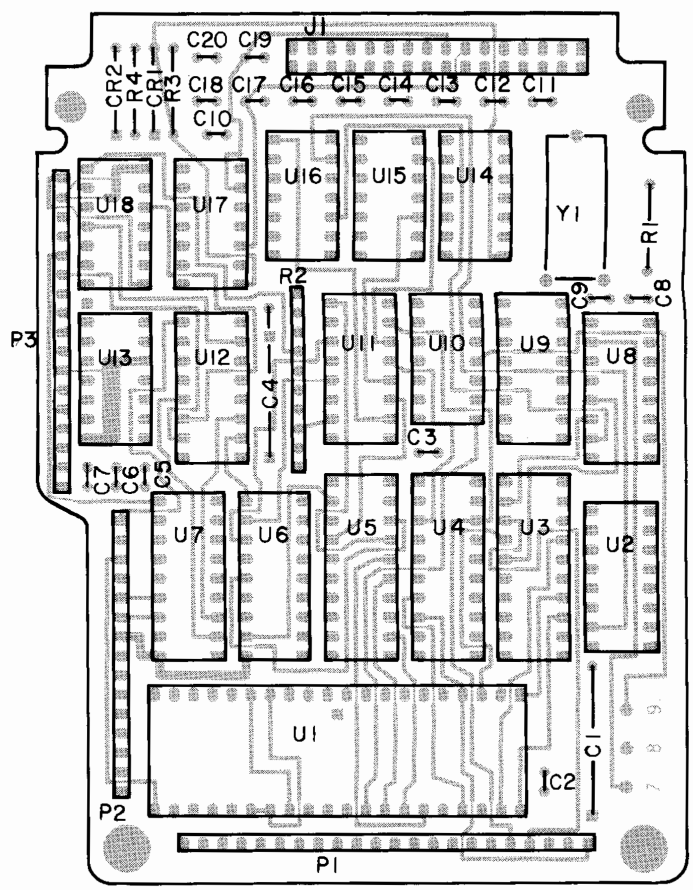
IN

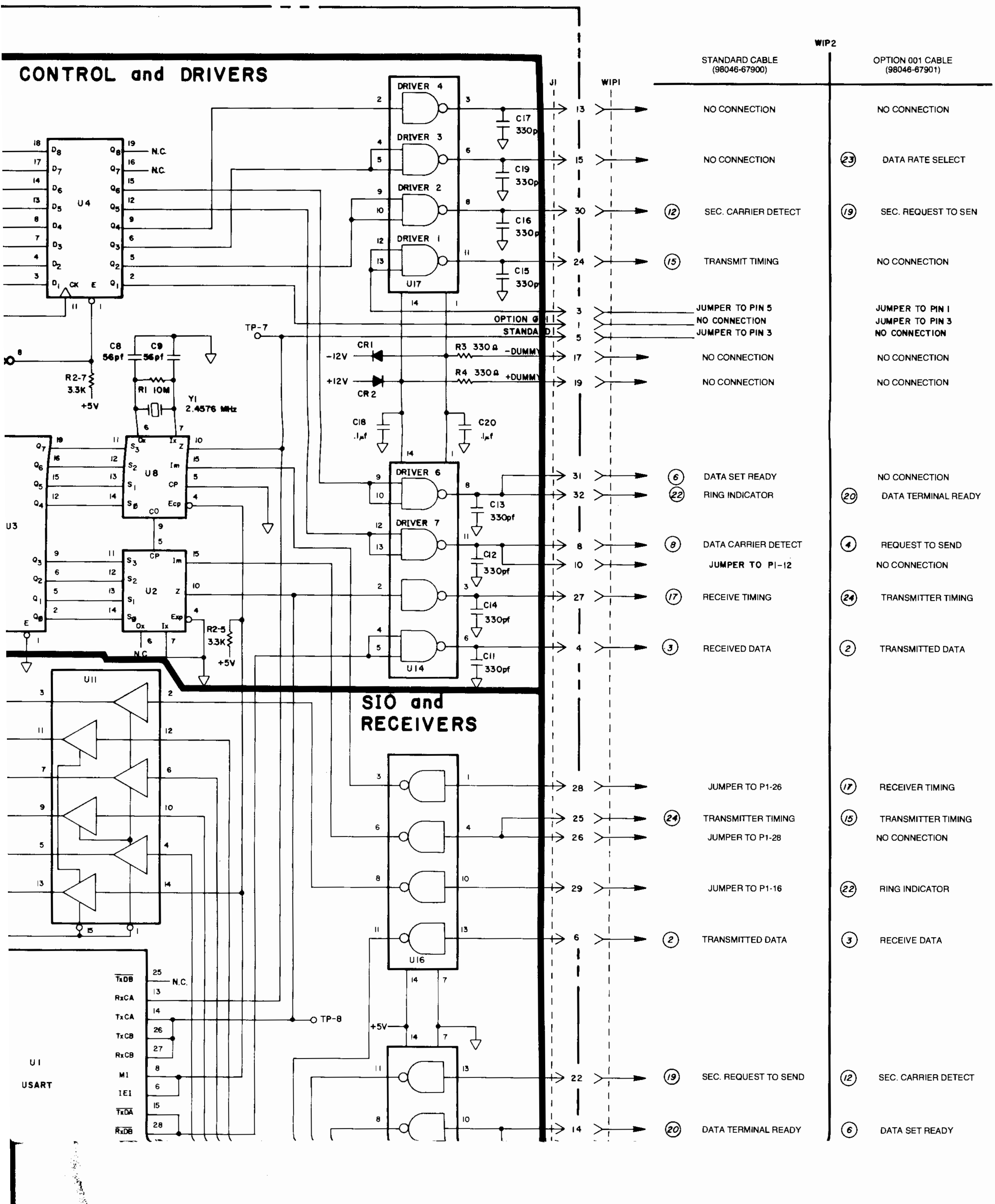
IN

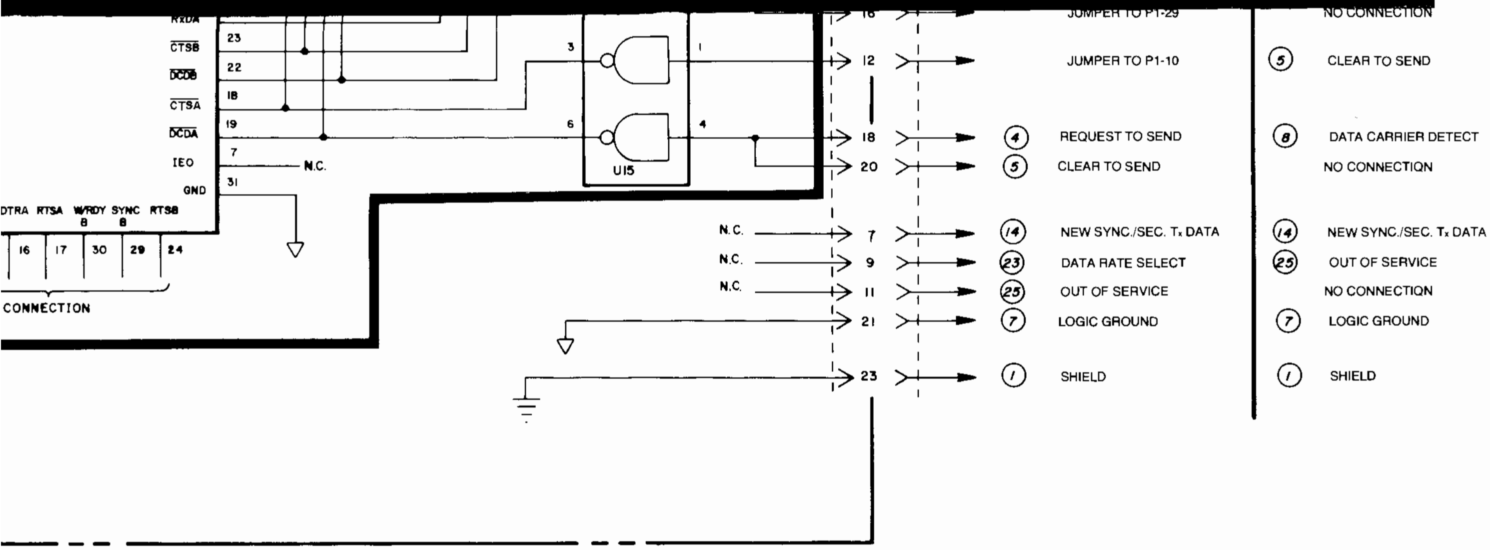
drivers

ntrol

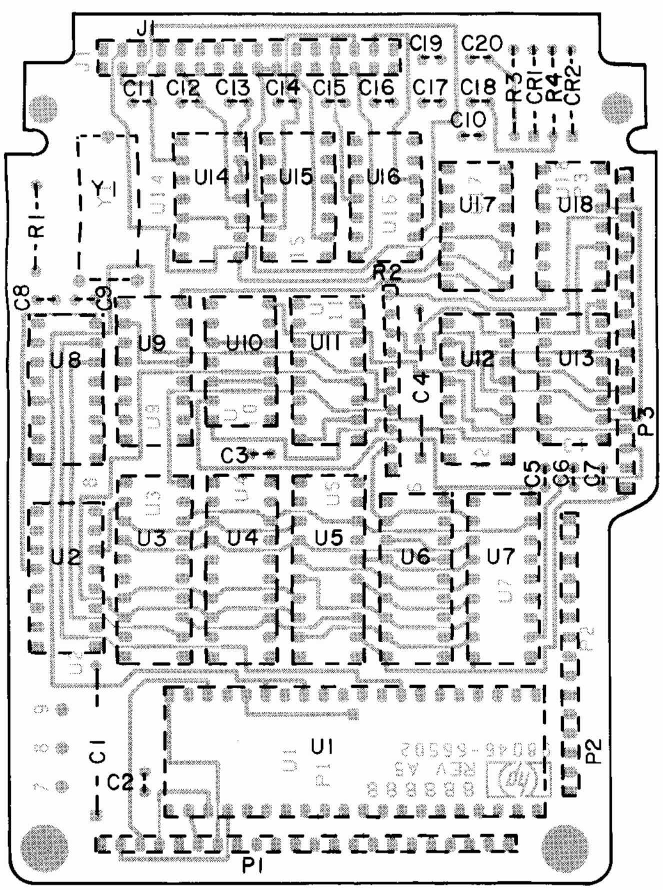
A2
Component Side




CONTROL and DRIVERS
SIO and RECEIVERS
DRIVER 4
DRIVER 3
DRIVER 2
DRIVER 1
DRIVER 6
DRIVER 7
U4
U17
U8
U2
U3
U14
U11
U16
U1
USART
TP-7
TP-8
CR1
CR2
-12V
+12V
+5V
R3 330Ω
R4 330Ω
-DUMMY
+DUMMY
R2-7 3.3K
R2-5 3.3K
R1 10M
Y1 2.4576 MHz
C8 56pf
C9 56pf
C17 330pf
C19 330pf
C16 330pf
C15 330pf
C18 .1µf
C20 .1µf
C13 330pf
C12 330pf
C14 330pf
C11 330pf
N.C.
OPTION 001
STANDARD
J1
W1P1
W1P2
STANDARD CABLE (98046-67900)
OPTION 001 CABLE (98046-67901)
NO CONNECTION
DATA RATE SELECT
SEC. CARRIER DETECT
SEC. REQUEST TO SEN
TRANSMIT TIMING
JUMPER TO PIN 5
JUMPER TO PIN 1
NO CONNECTION
JUMPER TO PIN 3
DATA SET READY
RING INDICATOR
DATA TERMINAL READY
DATA CARRIER DETECT
REQUEST TO SEND
JUMPER TO P1-12
RECEIVE TIMING
TRANSMITTER TIMING
RECEIVED DATA
TRANSMITTED DATA
JUMPER TO P1-26
RECEIVER TIMING
JUMPER TO P1-28
JUMPER TO P1-16
RECEIVE DATA
SEC. REQUEST TO SEND
TxDB
RxCA
TxCA
TxCB
RxCB
M1
IEI
TxDA
RxDB



A2
Circuit Side



Appendix A
RS-232C

RS-232C Compatible

What is the meaning of "RS-232C Compatible"? Or, of more importance, what doesn't it mean?

To answer the latter question first, it does not mean that every piece of equipment bearing that label will work perfectly with every other piece of equipment so labelled. What it does mean is that the equipment does not exceed any of the specifications or characteristics set down in the standard known as EIA RS-232C. But within the scope of RS-232C there is enough latitude to permit minor incompatibilities from one device to another, and these minor incompatibilities can cause unpleasant surprises for the unwary.

What is RS-232C?

In 1963 the Electronic Industry Association (EIA) established a standard to govern the Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Interchange. The latest revision of this standard has been in effect since 1969 and is known colloquially as RS-232C. It specifies:

- Mechanical characteristics of the interface.
- Electrical characteristics of the interface.
- A number of interchange circuits with descriptions of their functions.
- The relationship of interchange circuits to standard interface types.

The Comite Consultatif International Telephonique et Telegraphique (CCITT) has established standards that correspond to RS-232C. While these standards, CCITT V.24 and CCITT V.28, are very similar to RS-232C, they are not identical. Because it does not make use of all the circuits defined in both RS-232C and CCITT V.24, the 98046 Data Communications Interface conforms to both RS-232C and CCITT V.24 without any modification of the interface. The circuits which are utilized vary with different applications and with different modems. The drivers and receivers used in the 98046 conform to voltage and other electrical specifications of both CCITT V.28 and RS-232C.

Mechanical Characteristics

The standard gives definitions to 22 pins and designates three pins as unassigned, but does not specify a 25 pin connector. Although a particular 25 pin connector is not defined, the industry has accepted the connector shown in Figure A-1 as a de facto standard. The male connector is used with Data Terminal Equipment (the desktop computer) and the female connector is used with Data Communications Equipment (the modem).

The length of the cable used by Data Terminal Equipment to connect to Data Communications Equipment should not be longer than 15.24 metres (fifty feet). This is assuming that the load capacitance at the interface point is the worst case value of 2500 picofarads. Longer cables are often used, especially in point-to-point configurations when the user knows that the total load capacitance will not exceed the 2500pf maximum.

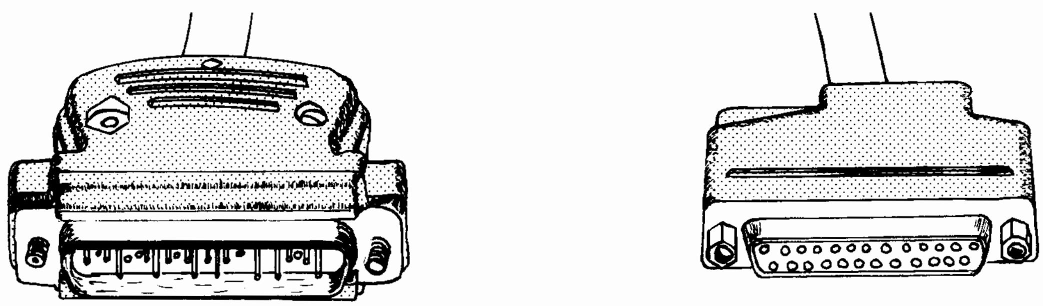


Figure A-1. 25 Pin Connector

Electrical Characteristics

A number of electrical parameters and limitations are defined by RS-232C for each interchange circuit. They refer to the Equivalent Interchange Circuit shown in Figure A-2. All voltage measurements are made at the interface point and with reference to Signal Ground.

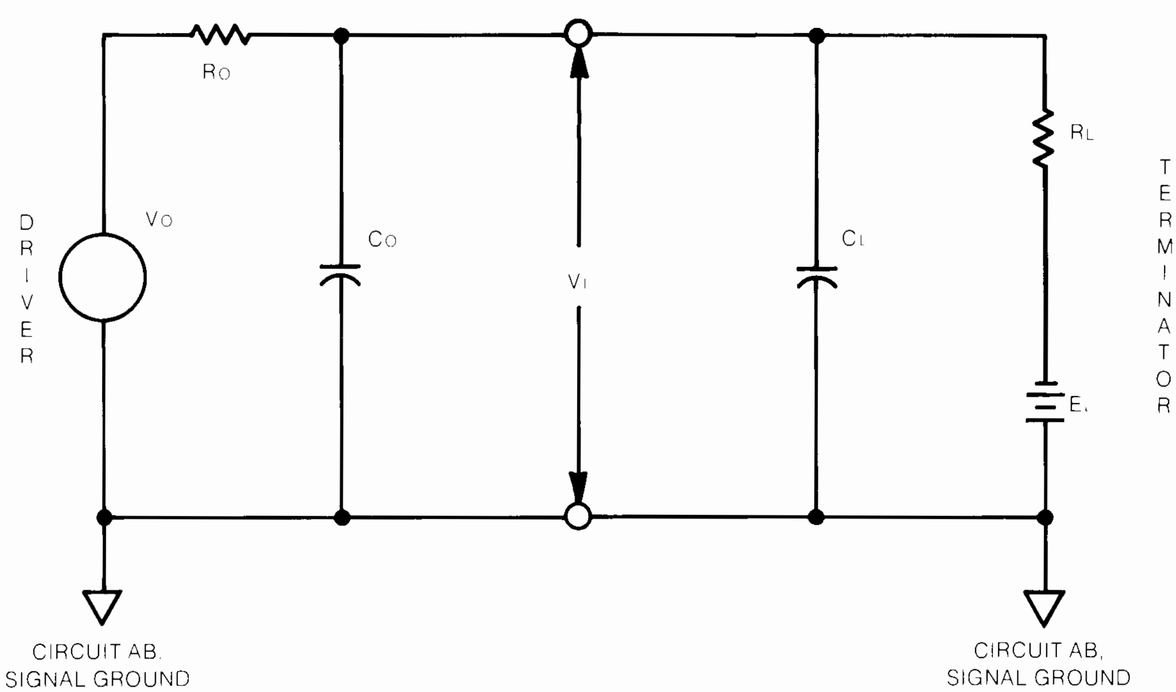


Figure A-2. Interchange Equivalent Circuit

- Open circuit voltage from the driver shall not be greater than ±25 volts.
- The open circuit voltage of the terminator shall not exceed ±two volts.
- The total capacitance of the terminator shall not exceed 2500 picofarads.
- The driver output voltage must be between 5 and 15 volts when the total terminator input resistance is between 3000 Ω and 7000 Ω.
- The output impedance of the driver circuit, when the driver power is off, shall not exceed 300Ω.
- The rate of change of the driver output voltage (slew rate) shall not exceed 30 volts per microsecond.

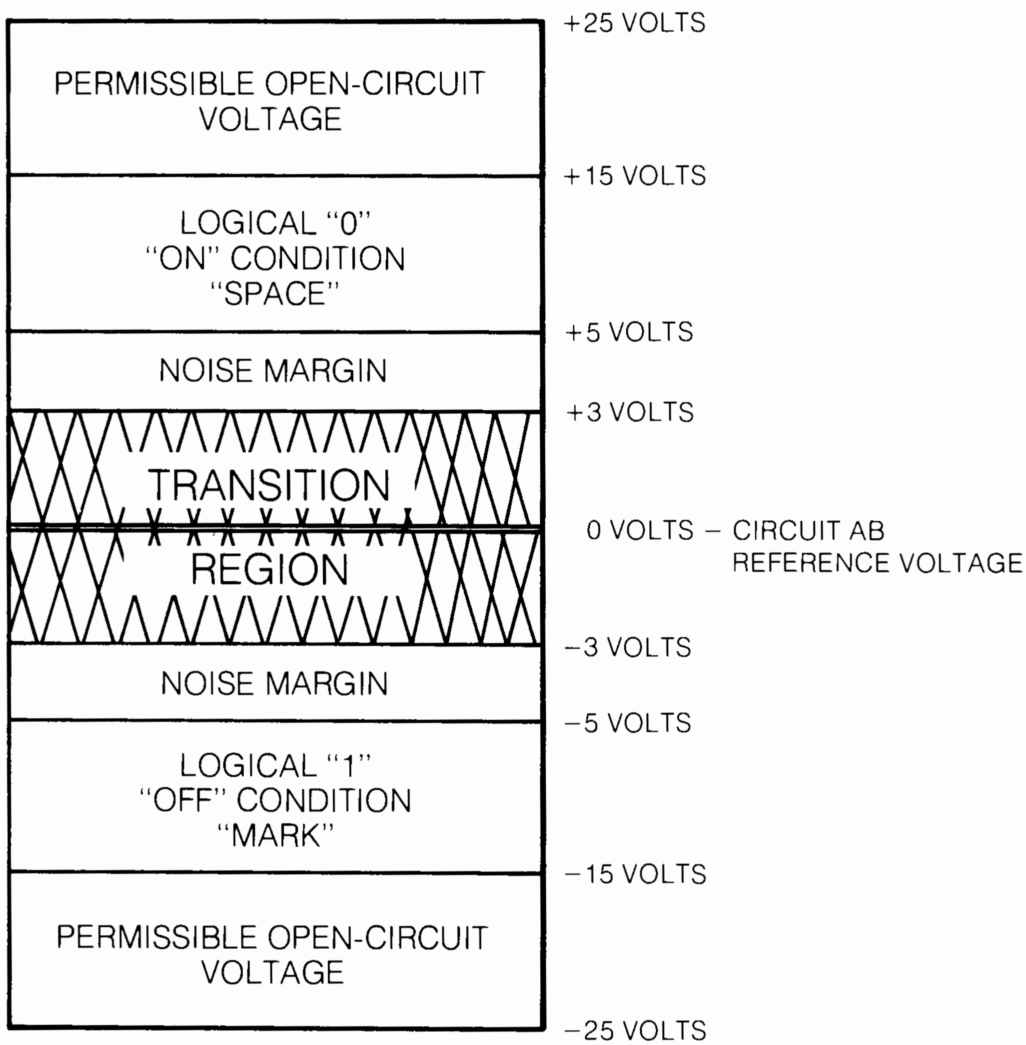


Figure A-3. Circuit Voltage Levels

In addition, several rules define the logic state indicated by voltage levels on the circuit.

- A logical "1" (MARK) is indicated when the voltage at the interface point is more negative than −3 volts.
- A logical "0" (SPACE) is indicated when the voltage at the interface point is more positive than +3 volts.
- To indicate a "1" signal condition (MARK), the driver shall assert a voltage between −5 volts and −15 volts.
- To indicate a "0" signal condition (SPACE), the driver shall assert a voltage between +5 volts and +15 volts.

Note that these standards allow for a 2 volt noise margin between the minimum driver voltage of 5 volts and the maximum undefined voltage of 3 volts. Other specifications that govern the transition region:

- All interchange signals entering the transition region shall proceed to the opposite valid signal state. It shall not re-enter the transition region until the next significant change in signal state.
- While in the transition region, the direction of the voltage change must not reverse.
- The time required for a control signal to cross the transition region shall not exceed one millisecond.
- The time required for a data or timing signal to cross the transition region shall not exceed one millisecond or four percent of the nominal signal period, whichever is the lesser.

Table A-1. RS-232C Pin Identification

Pin	Circuit Reference RS-232C	CCITT	Description
*1	AA	101	EARTH or Frame Ground
*2	BA	103	Transmitted Data
*3	BB	104	Received Data
*4	CA	105	Request to Send
*5	CB	106	Clear to Send
*6	CC	107	Data Set Ready
*7	AB	102	Signal Ground
*8	CF	109	Received Line Signal Detector
9	+P		Positive DC Test Voltage
10	−P		Negative DC Test Voltage
11			Unassigned
*12	SCF	122	Secondary Received Line Detector
13	SCB	121	Secondary Clear to Send
14	SBA	118	Secondary Transmitted Data
*15	DB	114	Transmitter Clock
16	SBB	119	Secondary Received Data
*17	DD	115	Received Clock
18			Unassigned
*19	SCA	120	Secondary Request to Send
*20	CD	108 / 2	Data Terminal Ready
21	CG	110	Signal Quality Detector
*22	CE	125	Ring Indicator
*23	CH / CI	112, 111	Data Rate Selector
*24	DA	113	External Transmitter Clock
25			Unassigned

* Used by the 98046 Interface. In the case of Pin 23, only Circuit CH (CCITT 112) is implemented, not Circuit CI (CCITT 111).

Circuit Functions

There are four categories of interchange circuits: Ground, Timing, Data, and Control. With the exception of the grounds, they can originate either in the modem (Data Communications Equipment, or DCE) or in the computer (Data Terminal Equipment, or DTE).

The ground circuits are:

Circuit AA (CCITT 101)
Protective Ground: Electrically connected to the frame of the equipment and to earth ground as external regulations demand.

Circuit AB (CCITT 102)
Signal Ground: The zero-voltage reference point. Also acts as the common return for unbalanced interchange circuits.

Timing Circuits

The clock generated by the Data Terminal Equipment:

Circuit DA (CCITT 113)
Transmitter Signal Element Timing: Provides timing for the transmitted data on Circuit BA (CCITT 103). A transition from ON to OFF (positive to negative) indicates the approximate center of each signal element.

The clocks generated by Data Communications Equipment:

Circuit DB (CCITT 114)
Transmitter Signal Element Timing: Provides DTE with a timing signal to be used with the transmitted data on Circuit BA (CCITT 103). A transition from OFF to ON (negative to positive) indicates the transition between signal elements.

Circuit DD (CCITT 115)
Receiver Signal Element Timing: Provides timing for the received data on Circuit BB (CCITT 104). The transition from ON to OFF (positive to negative) indicates the approximate center of each signal element.

Data Circuits

There are four Data Circuits, a primary circuit and a secondary circuit in each direction. Each is named in reference to the Data Terminal Equipment. For example, Received Data is driven by the DCE, and Transmitted Data is driven by the DTE.

Data circuits from the Data Terminal Equipment:

Circuit BA (CCITT 103)

Transmitted Data: The primary circuit for data originating at the DTE. Timing for data on this circuit can be provided either by circuit DA or DB.

Circuit SBA (CCITT 118)

Secondary Transmitted Data: The circuit for data originating at the DTE and transmitted via the secondary channel.

Data circuits from the Data Communications Equipment:

Circuit BB (CCITT 104)

Received Data: The circuit for data signals which have been generated by the DCE in response to signals received on the primary data channel. If necessary, timing for data on this circuit can be provided by circuit DD (CCITT 115).

Circuit SBB (CCITT 119)

Secondary Received Data: The circuit for data signals which have been generated by the DCE in response to signals received on the secondary data channel.

Control Circuits

These circuits are used to indicate to the receiving device the status or condition of the driving device.

Control circuits from the Data Terminal Equipment:

Circuit CA (CCITT 105)

Request to Send: Used to indicate to the DCE that data is ready to be sent, and also to control the direction of data transmission on a half duplex channel.

Circuit CD (CCITT 108.2)

Data Terminal Ready: Used to control the switching of the DCE to the communication channel. This means that it allows the modem to enter the data mode in preparation for data transfer, as compared to the standby mode.

Circuit CH (CCITT 111)

Data Signal Rate Selector: Used to select between two data signalling rates when using dual rate synchronous modems. Also used to select between two ranges when using dual range asynchronous modems. Use of this circuit is not compatible with Circuit CI (CCITT 112) which performs a similar function, but is driven by the DCE.

Circuit SCA (CCITT 120)

Secondary Request to Send: Functionally similar to Circuit CA (CCITT 105) except that it requests establishment of the secondary data channel.

Control circuits from the Data Communications Equipment:

Circuit CB (CCITT 106)

Clear to Send: Indicates whether the data set is conditioned to transmit on the data channel or not.

Circuit CC (CCITT 107)

Data Set Ready: Indicates the status of the data set. It indicates only that the DCE is connected to the line, is in the data mode, and is ready to exchange further control signals with the DTE.

Circuit CE (CCITT 125)

Ring Indicator: Indicates that a calling signal is being received on the data channel.

Circuit CF (CCITT 109)

Received Line Signal Detector: Indicates that the signal received on the data channel is within specifications set by the DCE manufacturer and is therefore suitable for demodulation.

Circuit CG (CCITT 110)

Signal Quality Detector: Indicates whether there is a probability of an error in the received data.

Circuit CI (CCITT 112)

Data Signal Rate Selector: Used to select between two data signalling rates in the DTE so that it coincides with the rate used in a dual rate synchronous DCE. Also used to select between two ranges of rates in the DTE so that it coincides with the range of rates used in a dual range asynchronous DCE.

Circuit SCB (CCITT 121)

Secondary Clear to Send: Functionally similar to Circuit CB (CCITT 106) except that it indicates the availability of the secondary channel.

Circuit SCF (CCITT 122)

Secondary Received Line Signal Detector: Functionally similar to Circuit CF (CCITT 109) except that it indicates the suitability of the signal received on the secondary data channel.

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Tel: 316627, 314786, 664715
Telex: 4192 Teltro Gu
A,C,E,M,P

HONG KONG
Hewlett-Packard Hong Kong, Ltd.
Room 105, Austin Center
1st Floor
21 Austin Avenue
TST P.O. Box 98524
KOWLOON, Hong Kong
Tel: 3-721143/8
Telex: 36678 HEWPA HX
Cable: PASIALTO Hong Kong
E,CP,P

Hewlett-Packard Hong Kong, Ltd.
11th Floor,Four Seas Building
212 Nathan Road
P.O. Box 795
KOWLOON, Hong Kong
Tel: 3697446
Telex: 36678 HEWPA HX
Cable: HEWPACK Hong Kong
E,CP,P

Schmidt & Co. (Hong Kong) Ltd.
Wing On Centre, 28th Floor
Connaught Road, C.
HONG KONG
Tel: 5-455644
Telex: 74766 SCHMX HX
A,M

ICELAND
Elding Trading Company Inc.
Hafnarnvoli-Tryggvagotu
P.O. Box 895
*IS-**REYKJAVIK***
Tel: 1-58-20, 1-63-03
M

INDIA
Blue Star Ltd.
Bhavdeep
Stadium Road
***AHMEDABAD** 380 014*
Tel: 42932
Telex: 012-234
Cable: BLUEFROST
E

Blue Star Ltd.
11 Magarath Road
***BANGALORE** 560 025*
Tel: 55668
Telex: 0845-430
Cable: BLUESTAR
A,CM,C,E

Blue Star Ltd.
Band Box House
Prabhadevi
***BOMBAY** 400 025*
Tel: 45-73-01
Telex: 011-3751
Cable: BLUESTAR
A,M

Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
***BOMBAY** 400 025*
Tel: 46 65 55
Telex: 011-4093
Cable: FROSTBLUE
A,CM,C,E,M

Blue Star Ltd.
7 Hare Street
***CALCUTTA** 700 001*
Tel: 12-01-31
Telex: 021-7655
Cable: BLUESTAR
A,M

Blue Star Ltd.
Meenakshi Mandiram
XXXXV/1379-2 Mahatma Gandhi Road
***COCHIN** 682-016*
Tel: 32069
Telex: 085-514
Cable: BLUESTAR
*A**

Blue Star Ltd.
133 Kodambakkam High Road
***MADRAS** 600 034*
Tel: 82057
Telex: 041-379
Cable: BLUESTAR
A,M

Blue Star Ltd.
Bhandari House, 7th/8th Floors
91 Nehru Place
***NEW DELHI** 110 024*
Tel: 682547, 682970
Telex: 031-2463
Cable: BLUESTAR
A,CM,C,E,M

Blue Star Ltd.
1-1-117/1 Sarojini Devi Road
***SECUNDERABAD** 500 033*
Tel: 70126
Telex: 0155-459
Cable: BLUESTAR
A,E

Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
***TRIVANDRUM** 695 013*
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

SALES & SUPPORT OFFICES
Arranged alphabetically by country

INDONESIA
BERCA Indonesia P.T.
P.O.Box 496/Jkt.
JL. Abdul Muis 62
JAKARTA
Tel: 373009
Telex: 46748 BERSAL IA
Cable: BERSAL
A,E,M,P

BERCA Indonesia P.T.
J.L. Jimento 23
SURABAYA
Tel: 42027
Telex: 31146 BERSAL S.D.
Cable: BERCACON
A,E,M,P*

IRAQ
Hewlett-Packard Trading S.A.
Mansoor City 9B/3/7
BAGHDAD
Tel: 5514973
Telex: 2455 HEPAIRAQ 1k
CP

IRELAND
Hewlett-Packard Ltd.
Kestrel House
Clanwilliam Place
Lower Mount Street
DUBLIN 2, Eire
Tel: 680424, 680426
Telex: 30439
A,E,P*

Hewlett-Packard Ltd.
2C Avongberg Ind. Est.
Long Mile Road
DUBLIN 12, Eire
Tel: 514322, 514224
Telex: 30439
A*,CP,E,MS,P*

Cardiac Services Ltd.
Kilmore Road
Artane
***DUBLIN** 5, Eire*
Tel: (01) 315820
M

ISRAEL
Electronics & Engineering Div.
Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
TEL-AVIV
Tel: 338973
Telex: 33569
Cable: BASTEL Tel-Aviv
A,CM,C,E,M,P

ITALY
Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/III
I-40132 **BOLOGNA**
Tel: (051) 402394
Telex: 511630
CM,CS,E,MS

Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 **CERNUSCO SUL NAVLIGLIO**
Tel: (2) 903691
Telex: 334632
A,CM,CP,E,MP,P

Hewlett-Packard Italiana S.p.A.
Via Nuova san Rocco A
Capadimonte, 62A
I-80135 **NAPOLI**
Tel: (081) 7413544
A,CM,CS,E

Hewlett-Packard Italiana S.p.A.
Via Turazza 14
I-35100 **PADOVA**
Tel: (49) 664888
Telex: 430315
A,CM,CS,E,MS

Hewlett-Packard Italiana S.p.A.
Via G. Armellini 10
I-00143 **ROMA**
Tel: (06) 546961
Telex: 610514
A,CM,CS,E,MS,P*

Hewlett-Packard Italiana S.p.A.
Corso Giovanni Lanza 94
I-10133 **TORINO**
Tel: (011) 682245, 659308
Telex: 221079
CM,CS,E

JAPAN
Yokogawa-Hewlett-Packard Ltd.
Inoue Building
1348-3, Asahi-cho
ATSUGI, Kanagawa 243
Tel: (0462) 24-0451
CM,C*,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Ashai Building
4 Tusukuba, 3-chome
KUMAGAYA, Saitama 360
Tel: (0485) 24-6563
CM,CS,E

Yokogawa-Hewlett-Packard Ltd.
Mito Mitsui Building
4-73, San-no-maru, 1-chome
MITO, Ibaragi 310
Tel: (0292) 25-7470
CM,CS,E

Yokogawa-Hewlett-Packard Ltd.
Sunitomo Seimei Bldg.
11-2 Shimo-sasajima-cho
Nakamura-ku
NAGOYA, Aichi 450
Tel: (052) 581-1850
CM,CS,E,MS

Yokogawa-Hewlett-Packard Ltd.
Chuo Bldg., 4TH FLOOR
54-20 Nishinakajima, 5-chome
Yodogawa-ku, Osaka-shi
OSAKA, 532
Tel: (06) 304-6021
Telex: 523-3624 YHPOSA
A,CM,CP,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
29-21 Takaido-Higashi 3-chome
Suginami-ku **TOKYO** 168
Tel: (03) 331-6111
Telex: 232-2024 YHPTOK
Cable: YUHPMARKET TOK23 724
A,CM,CP,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
Tanigawa Building
2-24-1 Tsuruya-cho
Kanagawa-ku
YOKOHAMA, Kanagawa 221
Tel: (045) 312-1252
Telex: 382-3204 YHP YOK
CM,CS,E

JORDAN
Mouasher Cousins Company
P.O. Box 1387
AMMAN
Tel: 21456, 24907, 39907
Telex: 21456 SABCO JO
E,M,P

KENYA
International Aeradio (E.A.) Ltd.
P.O. Box 95221
MOMBASA
M

ADCOM Ltd., Inc.
City House, Wabera Street
P.O. Box 30635
NAIROBI
Tel: 331955
Telex: 22639
A,E,M*

International Aeradio (E.A.) Ltd
P.O. Box 19012
Nairobi Airport
NAIROBI
Tel: 336055, 336056
Telex: 22201, 22301
M

KOREA
Samsung Electronics
C.P.O. 2775
SEOUL
Tel: 8334311, 8330002, 8330006
Telex: SAMSAN 27364
A,C,E,M,P

KUWAIT
Al-Khalidya Trading & Contracting
P.O. Box 830 Safat
KUWAIT
Tel: 42-4910, 41-1726
Telex: 2481 Areeg kt
A,E,M

Photo & Cine Equipment
P.O. Box 270 Safat
KUWAIT
Tel: 42-2846, 42-3801
Telex: 2247 Matin
P

LUXEMBOURG
Hewlett-Packard Belgium S.A./N.V.
Boulevard de la Woluwe 100
Woluwedal
B-1200 **BRUSSELS**
Belgium
Tel: 762/32/00
Telex: 23-494 paloben bru
A,CP,E,MP,P

MALAYSIA
Hewlett-Packard Sales (Malaysia)
Sdn. Bhd.
Suite 2.21/2.22
Bangunan Angkasa Raya
Jalan Ampang
KUALA LUMPUR
Tel: 483544
Telex: MA31011
A,CP,E,M,P*

Protel Engineering
P.O. Box 1917
Lot 319, Satok Road
*Kuching, **SARAWAK***
Tel: 53544
Telex: MA 70904 PROMAL
Cable: PROTELENG
A,E,M

MEXICO
Hewlett-Packard Mexicana, S.A. de C.V.
Av. Periferico Sur No. 6501
Tepepan, Xochimilco
MEXICO CITY 23, D.F.
Tel: (905) 676-4600
Telex: 017-74-507
A,CP,E,MS,P

Hewlett-Packard Mexicana, S.A. de C.V.
Rio Volga #600 Colonia del Valle
MONTERREY, N.L.
Tel: 78-42-93, 78-42-40, 78-42-41
Telex: 038-410
CS

MOROCCO
Dolbeau
81 rue Karatchi
CASABLANCA
Tel: 3041-82, 3068-38
Telex: 23051, 22822
E

Gerep
2 rue d'Agadir
Boite Postale 156
CASABLANCA
Tel: 272093, 272095
Telex: 23 739
P

MOZAMBIQUE
A.N. Goncalves Ltd.
162, 1° Apt. 14 Av. D. Luis
Caixa Postal 107
MAPUTO
Tel: 27091, 27114
Telex: 6-203 NEGON Mo
Cable: NEGON
A,E,M,P

NETHERLANDS
Hewlett-Packard Nederland B.V.
Van Heuven Goedhartlaan 121
NL1181KK **AMSTELVEEN**
Tel: (20) 47-20-21
Telex: 13 216
A,CM,CP,E,MP,P

Hewlett-Packard Nederland B.V.
Bongerd 2
NL2906 VK **CAPELLE** A/D Ijssel
Tel: (10) 51-64-44
Telex: 21261 hepac nl
A,CM,CP

NEW ZEALAND
Hewlett-Packard (N.Z.) Ltd.
169 Manukau Road
P.O. Box 26-189
Epsom, **AUCKLAND**
Tel: 68-7159
Cable: HEWPACK Auckland
CM,CS,E,P*

Northrop Instruments & Systems Ltd.
Eden House, 44 Khyber Pass Road
P.O. Box 9682
*Newmarket, **AUCKLAND***
Tel: 794-091
A,M

Northrop Instruments & Systems Ltd.
Terrace House, 4 Oxford Terrace
P.O. Box 8388
CHRISTCHURCH
Tel: 64-165
A,M

Hewlett-Packard (N.Z.) Ltd.
4-12 Cruickshank Street
P.O. Box 9443
Kilbirnie, **WELLINGTON** 3
Tel: 877-199
Cable: HEWPACK Wellington
CM,CP,E,P

Northrop Instruments & Systems Ltd.
Sturdee House
85-87 Ghuznee Street
P.O. Box 2406
WELLINGTON
Tel: 850-091
Telex: NZ 31296
A,M

NIGERIA
The Electronics Instrumentations Ltd.
N6B/770 Oyo Road
Oluseun House
P.M.B. 5402
IBADAN
Tel: 461577
Telex: 31231 TEIL NG
A,E,M,P

The Electronics Instrumentations Ltd.
144 Agege Motor Road, Mushin
P.O. Box 6645
*Mushin, **LAGOS***
A,E,M,P

NORTHERN IRELAND
Cardiac Services Company
95A Finaghy Road South
***BELFAST** BT 10 OBY*
Tel: (0232) 625-566
Telex: 747626
M

NORWAY
Hewlett-Packard Norge A/S
Nygaardsgaten 114
P.O. Box 4210
N-5013 Nygaardsgaten, **BERGEN**
Tel: (05) 21-97-33
Telex: 16621 hpnas n
CM,CS,E

Hewlett-Packard Norge A/S
Oestendalen 18
P.O. Box 34
N-1345 **OESTERAAS**
Tel: (02) 17-11-80
Telex: 16621 hpnas n
A*,CM,CP,E,MS,P

OMAN
Khimjl Ramdas
P.O. Box 19
MUSCAT
Tel: 72-22-17, 72-22-25
Telex: 3289 BROKER MB MUSCAT
P

PAKISTAN
Mushko & Company Ltd.
10, Bazar Road
Sector G-6/4
ISLAMABAD
Tel: 28624
Cable: FEMUS Rawalpindi
A,E,M,P

Mushko & Company Ltd.
Oosman Chambers
Abdullah Haroon Road
***KARACHI** 0302*
Tel: 511027, 512927
Telex: 2894 MUSHKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

PANAMA
Electronico Balboa, S.A.
Apartado 4929
Panama 5
Calle Samuel Lewis
Edificio "Alfa" No. 2
CIUDAD DE PANAMA
Tel: 64-2700
Telex: 3480380
Cable: ELECTRON Panama
A,E,M,P

Foto Internacional, S.A.
P.O. Box 2068
Free Zone of Colon
COLON 3
Tel: 45-2333
Telex: 3485126
Cable: IMPORT COLON/Panama
P

PERU
Compania Electro Medica S.A.
Los Flamencos 145, San Isidro
Casilla 1030
LIMA 1
Tel: 41-4325
Telex: Pub. Booth 25424 SISIDRO
Cable: ELMED Lima
A,E,M,P

PHILIPPINES
The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. Box 1510
*Metro **MANILA***
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,C,E,M

Electronic Specialists and Proponents Inc.
690-B Epifanio de los Santos Avenue
*Cubao, **QUEZON CITY***
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 742-40287
Cable: ESPINC MANILA
P

POLAND
Buro Informacjii Technicznej
Hewlett-Packard
Ul Stawki 2, 6P
*PL00-950 **WARSZAWA***
Tel: 39-59-62, 39-67-43
Telex: 81 24 53
A,C,E*,M*,P**

PORTUGAL
Telectra-Empresa Tecnica de Equipmentos Electricos S.a.r.l.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
P-LISBON 1
Tel: (19) 68-60-72
Telex: 12598
A,C,E,P

Mundinter
Intercambio Mundial de Comercio S.a.r.l
P.O. Box 2761
Avenida Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

PUERTO RICO
Hewlett-Packard Puerto Rico
Calle 272
#203 Urb. Country Club
RIO PIEDRAS, Puerto Rico 00924
Tel: (809) 762-7255
Telex: 345 0514
A,CP

QATAR
Business Communications Quatar
P.O. Box 3656
DOHA
Tel: 5851
Telex: 4454
P

Nasser Trading & Contracting
P.O. Box 1563
DOHA
Tel: 22170
Telex: 4439 NASSER
M

RHODESIA
Field Technical Sales
45 Kelvin Road North
P.O. Box 3548
SALISBURY
Tel: 705231
Telex: RH 4122
A,E,M,P

ROMANIA
Hewlett-Packard Reprezentanta
Boulevard Nicolae Balcescu 16
BUCURESTI
Tel: 130725
Telex: 10440
C,E**

SAUDI ARABIA
Modern Electronic Establishment
P.O. Box 193
AL-KHOBAR
Tel: 44-678, 44-813
Telex: 670136
Cable: ELECTA AL-KHOBAR
C,E,M,P

Modern Electronic Establishment
P.O. Box 1228, Baghdadiah Street
JEDDAH
Tel: 27-798
Telex: 401035
Cable: ELECTA JEDDAH
C,E,M,P

Modern Electronic Establishment
P.O. Box 2728
RIYADH
Tel: 62-596, 66-232
Telex: 202049
C,E,M,P

SCOTLAND
Hewlett-Packard Ltd.
Royal Bank Buildings
Swan Street
BRECHIN, Angus, Scotland
Tel: 3101, 3102
CM,CS

Hewlett-Packard Ltd.
SOUTH QUEENSFERRY
West Lothian, EH30 9TG
GB-Scotland
Tel: (031) 3311000
Telex: 72682
CM,CP,E,MS

SINGAPORE
Hewlett-Packard Singapore (Pte.) Ltd.
6th Floor, Inchcape House
450-452 Alexandra Road
SINGAPORE 0511
P. O. Box 58 Alexandra Post Office
Singapore 9115
Tel: 631788
Telex: HPSGSO RS 32409
Cable: HEWPACK, Singapore
A,CP,E,MS,P

SOUTH AFRICA
Hewlett-Packard South Africa (Pty.) Ltd.
Pine Park Center
Forest Drive, Pinelands
CAPE PROVINCE, 7405
P.O. Box 120
Howard Place
CAPE PROVINCE 7450
Tel: 53-7955, 53-7956, 53-7957, 53-7958, 53-7959
Telex: 57-0006
A,CM,CS,E,MS,P

Hewlett-Packard South Africa (Pty.) Ltd.
P.O. Box 37066
Overport
DURBAN 4067
Tel: 28-4178, 28-4179, 28-4110
CM,CS

Hewlett-Packard South Africa (Pty.) Ltd.
Hewlett-Packard Centre
Daphne Street
Private Bag Wendywood
SANDTON 2144
Tel: 802-5111
Telex: 84782
Cable: HEWPACK Johannesburg
A,CM,CP,E,MS,P

SPAIN
Hewlett-Packard Espanola S.A.
c/Entenza 312
E-BARCELONA 29
Tel: (3) 322-24-51, 321-73-54
Telex: 52603 hpbe e
A,CM,CP,E,MS,P

Hewlett-Packard Espanola S.A.
c/San Vicente s/n
Edificio Albia II, 7°B
E-BILBAO 1
Tel: 423-82-06, 423-83-06
A,CM,E,MS

Hewlett-Packard Espanola S.A.
Calle Jerez 3
E-MADRID 16
Tel: (1) 458-2600
Telex: 23515 hpe
A,CM,E,MP,P

Hewlett-Packard Espanola S.A.
Colonia Mirasierra
Edificio Juban
c/o Costa Brava 13
E-MADRID 34
Tel: (1) 734-8061, 734-1162
CM,CP

Hewlett-Packard Espanola S.A.
Av Ramon y Cajal 1
Edificio Sevilla 1, Planta 9
E-SEVILLA 5
Tel: (954) 64-44-54, 64-44-58
A,CM,CS,MS,P

Hewlett-Packard Espanola S.A.
C/Ramon Gordillo 1 (Entlo.)
E-VALENCIA 10
Tel: (96) 361-1354
CM,CS,P

SRI LANKA
Metropolitan Agencies Ltd.
209/9 Union Place
COLOMBO 2
Tel: 35947
Telex: 1377METROLTD CE
Cable: METROLTD
A,E,M,P

SUDAN
Radison Trade
P.O. Box 921
KHARTOUM
Tel: 44048
Telex: 375
A,E,M

SURINAM
Surtel Radio Holland N.V.
Grote Hofstr. 3-5
P.O. Box 155
PARAMARIBO
Tel: 72118, 77880
Cable: Surtel
E,M

SWEDEN
Hewlett-Packard Sverige AB
Enighetsvagen 3
S-16120 **BROMMA**
Tel: (08) 730-0550
Telex: (854) 10721 MESSAGES
Cable: MEASUREMENTS
A,CM,CP,E,MS,P

Hewlett-Packard Sverige AB
Sunnanvagen 14K
S-22226 **LUND**
Tel: (46) 13-69-79
CM,CS

Hewlett-Packard Sverige AB
Vastra Vintergatan 9
S-70344 **OREBRO**
Tel: (019) 14-07-20
CM,CS

Hewlett-Packard Sverige AB
Frotallisgatan 30
S-42132 **VASTRA-FROLUNDA**
Tel: (031) 49-09-50
Telex: 85410721
CM,CS,E,P

SWITZERLAND
Hewlett-Packard (Schweiz) AG
Clarastrasse 12
CH-4058 **BASEL**
Tel: (061) 33-59-20
A,CM

Hewlett-Packard (Schweiz) AG
Bahnhoherweg 44
3018 **BERN**
Tel: (031) 56-24-22
CM

Hewlett-Packard (Schweiz) AG
47 Avenue Blanc
CH-1202 **GENEVA**
Tel: (022) 32-30-05, 32-48-00
CM,CP

Hewlett-Packard (Schweiz) AG
29 Chemin Chateau Bloc
CH-1219 **LE LIGNON**-Geneva
Tel: (022) 96-03-22
Telex: 27333 hpag ch
Cable: HEWPACKAG Geneva
A,CM,E,MS,P

Hewlett-Packard (Schweiz) AG
Zurcherstrasse 20
P.O. Box 307
CH-8952 **SCHLIEREN**-Zurich
Tel: (01) 730-5240, 730-1821
Telex: 53933 hpag ch
Cable: HPAG CH
A,CM,CP,E,MS,P

SYRIA
General Electronic Inc.
Nuri Basha-Ahnaf Ebn Kays Street
P.O. Box 5781
DAMASCUS
Tel: 33-24-87
Telex: 11215 ITIKAL
Cable: ELECTROBOR DAMASCUS
E

Sawah & Co.
Place Azme
Boite Postale 2308
DAMASCUS
Tel: 16-367, 19-697, 14-268
Telex: 11304 SATACO SY
Cable: SAWAH, DAMASCUS
M

Suleiman Hilal El Mlawi
P.O. Box 2528
Mamoun Bitar Street, 56-58
DAMASCUS
Tel: 11-46-63
Telex: 11270
Cable: HILAL DAMASCUS
M

TAIWAN
Hewlett-Packard Far East Ltd.
Kaohsiung Branch
68-2, Chung Cheng 3rd Road
Shin Shin, Chu
KAOHSIUNG
Tel: 241-2318, 261-3253
CS,E,MS,P

Hewlett-Packard Far East Ltd.
Taiwan Branch
Bank Tower, 5th Floor
205 Tun Hwa North Road
TAIPEI
Tel: 751-0404
Cable:HEWPACK Taipei
A*,CP,E,MS,P

San Kwang Instruments Co., Ltd.
20 Yung Sui Road
TAIPEI
Tel: 361-5446, 361-5447, 361-5448, 361-5449
Telex: 22894 SANKWANG
Cable: SANKWANG Taipei
A

TANZANIA
International Aeradio (E.A.) Ltd.
P.O. Box 861
DAR ES SALAAM
Tel: 21251
Telex: 41030
M

THAILAND
UNIMESA Co. Ltd.
Elcom Research Building
2538 Sukhumvit Ave.
*Bangchak, **BANGKOK***
Tel: 393-2387, 393-0338
Telex: TH81160, 82938, 81038
Cable: UNIMESA Bangkok
A,E,M

Bangkok Business Equipment Ltd.
5/5-6 Dejo Road
BANGKOK
Tel: 234-8670, 234-8671, 234-8672, 234-8673
Cable: BUSIQUIPT Bangkok
P

TRINIDAD & TOBAGO
CARTEL
Caribbean Telecoms Ltd.
P.O. Box 732
50/A Jerningham Avenue
PORT-OF-SPAIN
Tel: 62 4214, 62 4213
A,E,M,P

SALES & SUPPORT OFFICES

Arranged alphabetically by country

TUNISIA

Tunisie Electronique
31 Avenue de la Liberte
TUNIS
Tel: 280-144
E,P

Corema
1 ter. Av. de Carthage
TUNIS
Tel: 253-821
Telex: 12319 CABAM TN
M

TURKEY

Teknim Company Ltd.
Riza Sah Pehlievi
Caddesi No. 7
Kavaklidere, ***ANKARA***
Tel: 275800
Telex: 42155
E

UNITED ARAB EMIRATES

Emitac Ltd.
P.O. Box 2711
ABU DHABI
Tel: 331370, 331371
E,M,P

Emitac Ltd.
P.O. Box 1641
SHARJAH
Tel: 354121, 354123
Telex: 68136
E,M,P

UNITED KINGDOM
see: GREAT BRITAIN
NORTHERN IRELAND
SCOTLAND

UNITED STATES OF AMERICA

Alabama

Hewlett-Packard Co.
700 Century Park South
Suite 128
BIRMINGHAM, AL 35226
Tel: (205) 822-6802
CM,CS,MP

Hewlett-Packard Co.
P.O. Box 4207
8290 Whitesburg Drive, S.E.
HUNTSVILLE, AL 35802
Tel: (205) 881-4591
CM,CP,E,M*

Alaska

Hewlett-Packard Co.
1577 "C" Street, Suite 252
ANCHORAGE, AK 99510
Tel: (206) 454-3971
CM,CS**

Arizona

Hewlett-Packard Co.
2336 East Magnolia Street
PHOENIX, AZ 85034
Tel: (602) 273-8000
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Hewlett-Packard Co.
2424 East Aragon Road
TUCSON, AZ 85706
Tel: (602) 889-4661
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Arkansas

Hewlett-Packard Co.
P.O. Box 5646
Brady Station
LITTLE ROCK, AR 72215
Tel: (501) 376-1844
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California

Hewlett-Packard Co.
7621 Canoga Avenue
CANOGA PARK, CA 91304
Tel: (213) 702-8300
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Hewlett-Packard Co.
1579 W. Shaw Avenue
FRESNO, CA 93771
Tel: (209) 224-0582
CM,MS

Hewlett-Packard Co.
1430 East Orangethorpe
FULLERTON, CA 92631
Tel: (714) 870-1000
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Hewlett-Packard Co.
5400 W. Rosecrans Boulevard
LOS ANGELES, CA 90260
Tel: (213) 970-7500
CM,CP,MP

Hewlett-Packard Co.
3939 Lankersham Blvd.
NORTH HOLLYWOOD, CA 91604
Tel: (213) 877-1282
regional headquarters

Hewlett-Packard Co.
3200 Hillview Avenue
PALO ALTO, CA 94304
Tel: (415) 857-8000
CM,CP,E

Hewlett-Packard Co.
646 W. North Market Boulevard
SACRAMENTO, CA 95834
Tel: (916) 929-7222
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Hewlett-Packard Co.
9606 Aero Drive
P.O. Box 23333
SAN DIEGO, CA 92123
Tel: (714) 279-3200
CM,CP,E,MP

Hewlett-Packard Co.
363 Brookhollow Drive
SANTA ANA, CA 92705
Tel: (714) 641-0977
A,CM,C*,E

Hewlett-Packard Co.
3003 Scott Boulevard
SANTA CLARA, CA 95050
Tel: (408) 988-7000
A,CM,CP,E,MP

Hewlett-Packard Co.
454 Carlton Court
SO. SAN FRANCISCO, CA 94080
Tel: (415) 877-0772
CM,CP

Colorado

Hewlett-Packard Co.
5600 DTC Parkway
ENGLEWOOD, CO 80110
Tel: (303) 771-3455
A,CM,CP,E,MS

Connecticut

Hewlett-Packard Co.
47 Barnes Industrial Road South
P.O. Box 5007
WALLINGFORD, CT 06492
Tel: (203) 265-7801
A,CM,CP,E,MS

Florida

Hewlett-Packard Co.
P.O. Box 24210
2727 N.W. 62nd Street
FORT LAUDERDALE, FL 33309
Tel: (305) 973-2600
CM,CP,E,MP

Hewlett-Packard Co.
4080 Woodcock Drive, #132
Brownett Building
JACKSONVILLE, FL 32207
Tel: (904) 398-0663
CM,C*,E*,MS**

Hewlett-Packard Co.
P.O. Box 13910
6177 Lake Ellenor Drive
ORLANDO, FL 32809
Tel: (305) 859-2900
A,CM,CP,E,MS

Hewlett-Packard Co.
P.O. Box 12826
Suite 5, Building 1
Office Park North
PENSACOLA, FL 32575
Tel: (904) 476-8422
A,CM,MS

Hewlett-Packard Co.
110 South Hoover, Suite 120
TAMPA, FL 33609
Tel: (813) 872-0900
A*,CM,CS,E*,M*

Georgia

Hewlett-Packard Co.
P.O. Box 105005
450 Interstate N. Parkway
ATLANTA, GA 30339
Tel: (404) 955-1500
Telex: 810-766-4890
A,CM,CP,E,MP

Hewlett-Packard Co.
Executive Park Suite 306
P.O. Box 816
AUGUSTA, GA 30903
Tel: (404) 736-0592
CM,MS

Hewlett-Packard Co.
P.O. Box 2103
1172 N. Davis Drive
WARNER ROBINS, GA 31098
Tel: (912) 922-0449
CM,E

Hawaii

Hewlett-Packard Co.
2875 South King Street
HONOLULU, HI 96826
Tel: (808) 955-4455
A,CM,CS,E,MS

Idaho

Hewlett-Packard Co.
11311 Chinden Boulevard
BOISE, ID 83707
Tel: (208) 376-6000
CM,CS,M*

Illinois

Hewlett-Packard Co.
211 Prospect Road
BLOOMINGTON, IL 61701
Tel: (309) 663-0383
CM,CS,MS**

Hewlett-Packard Co.
1100 31st Street
DOWNERS GROVE, IL 60515
Tel: (312) 960-5760
CM,CP

Hewlett-Packard Co.
5201 Tollview Drive
ROLLING MEADOWS, IL 60008
Tel: (312) 255-9800
A,CM,CP,E,MP

Indiana

Hewlett-Packard Co.
P.O. Box 50807
7301 No. Shadeland Avenue
INDIANAPOLIS, IN 46250
Tel: (317) 842-1000
A,CM,CS,E,MS

Iowa

Hewlett-Packard Co.
5815 S.W. 5th Street
DES MOINES, IA 50315
Tel: (515) 243-5876
CM,MS**

Hewlett-Packard Co.
2415 Heinz Road
IOWA CITY, IA 52240
Tel: (319) 351-1020
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Kansas

Hewlett-Packard Co.
514 South Westview
DERBY, KA 67037
Tel: (316) 265-5200
CM,CS

Kentucky

Hewlett-Packard Co.
10170 Linn Station Rd., Suite 525
Atkinson Square
LOUISVILLE, KY 40223
Tel: (502) 426-0100
A,CM,CS,MS

Louisiana

Hewlett-Packard Co.
P.O. Box 1449
3229 Williams Boulevard
KENNER, LA 70062
Tel: (504) 443-6201
A,CM,CS,E,MS

Maryland

Hewlett-Packard Co.
7121 Standard Drive
HANOVER, MD 21076
Tel: (301) 796-7700
A,CM,CP,E,MS

Hewlett-Packard Co.
2 Choke Cherry Road
ROCKVILLE, MD 20850
Tel: (301) 948-6370
A,CM,CP,E,MP

Massachusetts

Hewlett-Packard Co.
32 Hartwell Avenue
LEXINGTON, MA 02173
Tel: (617) 861-8960
A,CM,CP,E,MP

Michigan

Hewlett-Packard Co.
23855 Research Drive
FARMINGTON HILLS, MI 48024
Tel: (313) 476-6400
A,CM,CP,E,MP

Hewlett-Packard Co.
4326 Cascade Road S.E.
GRAND RAPIDS, MI 49506
Tel: (616) 957-1970
CM,CS,MS

Minnesota

Hewlett-Packard Co.
2025 W. Larpenteur Ave.
ST. PAUL, MN 55113
Tel: (612) 644-1100
A,CM,CP,E,MP

Mississippi

Hewlett-Packard Co.
322 N. Mart Plaza
JACKSON, MS 39206
Tel: (601) 982-9363
CM,MS

Missouri

Hewlett-Packard Co.
11131 Colorado
KANSAS CITY, MO 64137
Tel: (816) 763-8000
Telex: 910-771-2087
A,CM,CS,E,MS

Hewlett-Packard Co.
1024 Executive Parkway
ST. LOUIS, MO 63141
Tel: (314) 878-0200
A,CM,CP,E,MP

Nebraska

Hewlett-Packard
Suite 101
7101 Mercy Road
OMAHA, NE 68106
Tel: (402) 392-0948
CM,MS

Nevada

Hewlett-Packard Co.
Suite D-130
5030 Paradise Blvd.
LAS VEGAS, NV 89119
Tel: (702) 736-6610
CM,MS**

New Jersey

Hewlett-Packard Co.
W120 Century Road
PARAMUS, NJ 07652
Tel: (201) 265-5000
A,CM,CP,E,MP

Hewlett-Packard Co.
60 New England West
PISCATAWAY, NJ 08854
Tel: (201) 981-1199
A,CM,CP,E

New Mexico

Hewlett-Packard Co.
P.O. Box 11634
Station E
11300 Lomas Blvd.,N.E.
ALBUQUERQUE, NM 87192
Tel: (505) 292-1330
Telex: 910-989-1185
CM,CP,E,MS

Hewlett-Packard Co.
156 Wyatt Drive
LAS CRUCES, NM 88001
Tel: (505) 526-2484
Telex: 910-9983-0550
CM,C*,E,M*

New York

Hewlett-Packard Co.
6 Automation Lane
Computer Park
ALBANY, NY 12205
Tel: (518) 458-1550
Telex: 710-444-4691
A,CM,CS,E,MS

Hewlett-Packard Co.
650 Perinton Hill Office Park
FAIRPORT, NY 14450
Tel: (716) 223-9950
Telex: 510-253-0092
CM,CP,E,MS

Hewlett-Packard Co.
No. 1 Pennsylvania Plaza
55th Floor
34th Street & 8th Avenue
NEW YORK, NY 10001
Tel: (212) 971-0800
CM,CP,E*,M*

Hewlett-Packard Co.
5858 East Molloy Road
SYRACUSE NY 13211
Tel: (315) 455-2486
A,CM,CS,E,MS

Hewlett-Packard Co.
3 Crossways Park West
WOODBURY, NY 11797
Tel: (516) 921-0300
Telex: 510-221-2183
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