HEWLETT PACKARD

SPECIAL

HP 93698W General Purpose RTE-A Driver IDS71

For Parallel Interface Cards

Programming and Operating Manual

This manual reflects information that is compatible with driver IDS71 Software Revision Code ~~2320~~ 2404

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Any text changes to this manual are supplied in the form of manual change notices or as reissues of the manual. Change notice packages, issued between editions, contain replacement (and/or additional) pages or write-in instructions to be merged into the manual by the user. All changed pages are identified by a change number at the bottom of the page and the changed information is specifically identified by a vertical line (change bar) on the outer margin of the page. The manual will be reprinted as necessary to incorporate all prior updates. No new information is incorporated into a reprinting unless it appears as a prior update. The edition designation does not change for reprinting. The publication history of any changes is given under "Printing History" below. This history is updated when reprinting or reissuing the manual. A complete revision of the manual involves a reissue and a new edition is specified. A new edition may have new information not appearing in older editions.

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THE PURPOSE OF THIS MANUAL UPDATE
is to adapt the manual to product changes or to correct errors in the current edition or printing of the manual. Earlier updates, if any, are contained herein. *(If you have made all previous changes to this manual, you need only make the changes described under the change number indicated above.)* This update consists of: this cover letter, all replacement and/or new pages, and write-in instructions (if any).

CHANGED PAGES ARE IDENTIFIED
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NEW PAGES ARE IDENTIFIED
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TO UPDATE THE MANUAL
follow the instructions provided in this notice under the appropriate change number. Insert any attached change pages in the manual and discard old pages. Be sure to incorporate changes in sequence (e.g., if you have change 4, be sure to incorporate changes 1 through 3 before 4 is incorporated).

TECHNICAL MANUAL CHANGE
(93698-90003)

CHANGE 1: (7 March 1984)

Reason for change; to update driver.

A. On the title page, change the software revision code for driver IDS71 to read; 2404

B. On page 1-3, paragraph 1.4, steps a. and b., change RTE-A.1 to read RTE-A.

C. On page 3-1, paragraph 3.2, second sentence, change text to read as follows:

During the Driver Relocation Phase the . . .

Table of Contents

Illustrations

Tables

GENERAL INFORMATION — SECTION I

1.1 INTRODUCTION

This manual contains information that will allow you to prepare programs which use General Purpose RTE-A Driver IDS71 to accomplish input or output operations through Parallel Interface Cards (PIC); the HP 12006A for example. Section I provides a description of features available with IDS71 and outlines the components supplied with the HP 93698W product. Section II contains information that will enable you to write programs using the software, and section III provides the RTE-A configuration information for driver IDS71. The information in this manual is presented with the assumption that you are familiar with HP RTE-A operating systems and have some knowledge of RTE-A drivers and the interface (12006A PIC for example) with which you will use IDS71.

1.2 DESCRIPTION

Figure 1-1 illustrates a typical operating environment for IDS71. The general purpose driver is used in any HP A/L-Series Computer with Parallel Interface Cards (e.g., 12006A). The operating modes that are selectable for the driver allow the transfer of data into or out of the computer with or without the use of Direct Memory Access (DMA). Under DMA transfers, two different submodes are available. Also, six different submodes of non-DMA operation are available for use. The various modes that may be selected allow the programmer choices for asynchronous or synchronous low-, medium-, and high-speed data transfer rates. The choice as to the mode of transfer depends upon the application. The driver features may be implemented through FORTRAN or HP Assembly Language (or any other RTE-A supported language) EXEC Read, Write, Control, or Status calls to the RTE-A system.

1.3 COMPONENTS SUPPLIED

The following software is supplied with product HP 93698W to operate in an RTE-A environment.

a. RTE-A Driver IDS71 relocatable on mini-cartridge part no. 93698-13302.

b. RTE-A Driver IDS71 Programming and Operating Manual part no. 93698-90003.

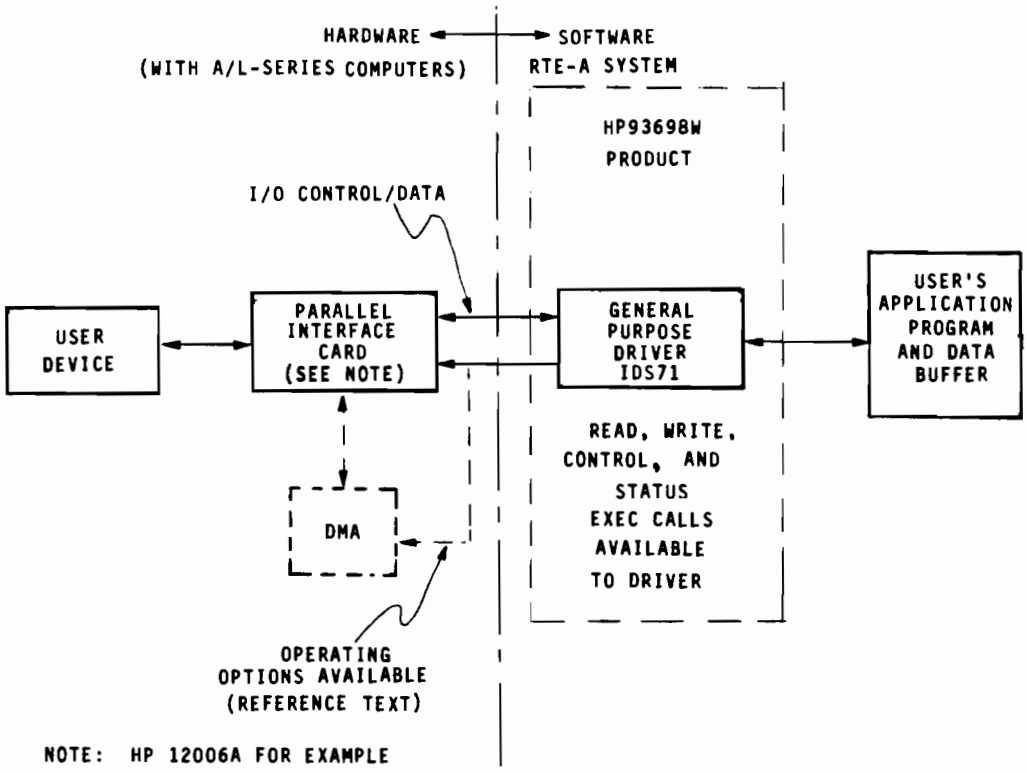


Figure 1-1. Typical Operating Environment for Driver IDS71

1.4 REFERENCES

The following manuals will prove helpful in using the software:

a. RTE-A Driver Reference Manual, part no. 92077-90011.

b. RTE-A Programmer's Reference Manual, part no. 92077-90007.

c. HP 12006A Parallel Interface Reference Manual, part no. 12006-90001.

APPLICATION INFORMATION	SECTION II

2.1 INTRODUCTION

This section provides the information that will allow you to prepare application programs to operate the interface cards (and peripheral devices) through driver IDS71.

2.2 OVERALL OPERATION

Driver IDS71 is a general purpose I/O driver as well as the interface driver for the Parallel Interface Cards (e.g., 12006A) that perform 8- or 16-bit parallel data transfers between the system and a peripheral I/O device.

The driver will perform a basic set of I/O read, write, and control operations via EXEC requests. Through the use of a control parameter specified in the Read or Write call, the mode of operation is set for any particular transfer. Table 2-1 shows the eight modes available. The mode parameter is specified in the MODE (IPRM2) word in the Read or Write call.

Recommendations are to use mode 1 for low-speed transfer operations. Mode 2 or 3 or 4 can be used for medium-speed transfer rates. Modes 1 through 6 do not employ DMA.

Modes 7 and 8 employ DMA and are therefore used for high-speed transfer rates. Eight bit parallel data transfers are possible ONLY WITH THESE TWO MODES.

In modes 2 through 4 (SFS operation), the data transfer "window" has a limitation of 10 milliseconds. If the Device Flag (DEVFLG) does not come back within this window the driver will down the device and give the error message "IO-NR" (IO NOT READY).

Modes 5 and 6 (no Interrupt, no Flag) would rarely be used for normal data transfers. One application for mode 6 is in the control of the 93550A I/O Switch (the 93550A does not return a Device Flag nor does it require a Device Command signal).

Table 2-1. Driver Operating Modes

MODE	DESCRIPTION
1	No DMA, Interrupt, DEVCMD, DEVFLG
2	No DMA, non-Interrupt, DEVCMD, DEVFLG
3	No DMA, non-Interrupt (after initial Interrupt), DEVCMD, DEVFLG
4	No DMA, non-Interrupt, no DEVCMD, DEVFLG
5	No DMA, non-Interrupt, DEVCMD, no DEVFLG
6	No DMA, non-Interrupt, no DEVCMD, no DEVFLG
7	DMA, DEVCMD, DEVFLG
8	DMA, no DEVCMD, DEVFLG

NOTES:

1. Modes 1 through 6 are for 16-bit parallel data transfers only.
2. Modes 7 and 8 are for 8- or 16-bit parallel data transfers.

The following sections cover the programming considerations with which an applications programmer should be familiar when making I/O requests to the card. Refer also to the HP 12006A Interface Kit Reference Manual for hardware-dependent information.

2.3 IDS71 READ/WRITE REQUESTS

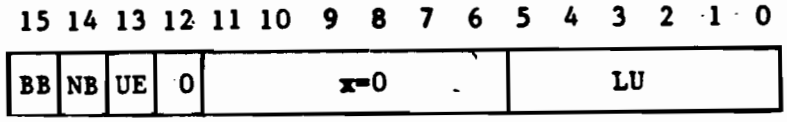
The call sequences for the IDS71 Read and Write requests are:

```
(Read request)

CALL EXEC (1,ICNWD,IBUFR,IBUFL[,IPRM1],IPRM2)

(Write request)

CALL EXEC (2,ICNWD,IBUFR,IBUFL[,IPRM1],IPRM2)
```

The parameters are explained in the following paragraphs.

2.3.1 Control Word ICNWD

The format of the Control Word (ICNWD) for performing an EXEC Read or Write request to IDS71 is shown below.



LU is the logical unit number (1 - 63) of the device.

UE is a user error bit. If UE is 1, it informs the driver to not suspend a calling program if a device error occurs.

If UE is 0, the system provides normal error handling.

NB identifies the buffered/non-buffered mode in effect.

NB is 1 if the non-buffered mode is in effect, overriding normal device buffering. Programs issuing read/write request in this mode are always suspended while the request executes. Using the non-buffered mode will allow the calling program to obtain any error and status information after the request has completed.

The EXEC will iginore the NB bit for a Read request and will force non-buffered operation.

NB is 0 if normal device buffering is used. If a device normally uses buffered mode, the program will execute in parallel with the output operation.

BB is the device driver bypass bit. When writing programs that use the interface driver and no device driver is defined for the LU, the BB-bit will be ignored. However, if a device driver is defined for the LU being programmed, and you want to use the interface driver directly, the BB-bit must be set.

2.3.2 Buffer Name IBUFR

IBUFR is the buffer name if used in FORTRAN or PASCAL; in ASMB or MACRO it is the address of the user buffer into which data is to be read for a Read request (EXEC 1), or from which data is to be

written for a Write request (EXEC 2).

2.3.3 Buffer Length IBUFL

IBUFL is the length of the buffer, a variable defining the length of the data record to be transferred. When using mode 1 through 6 this must always be a positive number and is used to specify the length of the data record in words. When using modes 7 or 8, either a positive number is used to specify the length of the data record in words, or a negative number is used to specify the length of the data record in characters (8-bit bytes). If the data record contains REAL data, this must be allowed for in the IBUFL parameter. For example: a data record containing 10 REAL values would require IBUFL to be +20 or -40 since REAL numbers require two words. If the data record contains double precision data, three words are required for each value, and therfore, a 10-word double precision data record would require IBUFL to be +30 or -60.

2.3.4 Optional Parameter IPRM1

All bits set in IPRM1 will be set in the card control register. The value in IPRM1 will ORed with the first driver parameter word to determine the actual card control register setting before the Read or Write request is executed.

If IPRM1 is not supplied in the EXEC request, the first parameter word will be used to set the card control register.

The first driver parameter word is set either at generation or with a configure card control request, function code 40B. The card control register for the Parallel Interface card is described later in this section.

2.3.5 Parameter IPRM2

IPRM2 specifies the mode of operation as described in table 2-1. It must ALWAYS be specified in a Read or Write call.

2.4 IDS71 CONTROL REQUEST

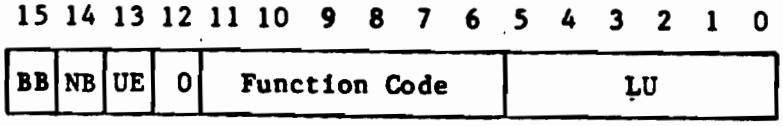
The call sequence for the Control request is:

```
CALL EXEC (3,ICNWD,IPRM1[,IPRM2][,IPRM3][,IPRM4])
```

The parameters are explained in the following paragraphs.

2.4.1 Control Word ICNWD

The format of the ICNWD used by IDS71 when programming a Control request is shown below.



The NB (Non-Buffered mode), UE (User Error), and LU (Logical Unit assignment) bits are defined as in the Read/Write request paragraphs above. The BB-bit (Bypass device driver) must be set to one (1) if a driver has been defined for the device. The Function Code bits are summarized below and explained in the following paragraphs.

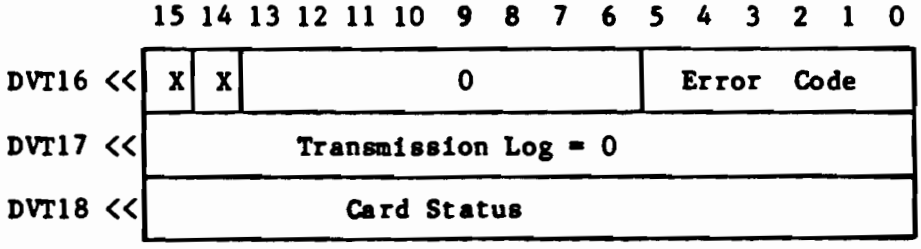
00 = Clear and Reset Card
06 = Return Dynamic Status of Card
20B = Enable Program Scheduling
21B = Disable Program Scheduling
40B = Configure Card Control Word

2.4.1.1 Function Code 00B

This function code in the Control Request sets the interface card to a known state by halting all processing.

2.4.1.2 Function Code 06B

A dynamic status request will return information on the immediate status of the device to DVT16 through DVT18. The format of the status information is shown below. After completion of the request, subsequent calls to RMPAR will retrieve the status information from the DVT.



DVT16 reflects any error information for the device that is connected to the interface card. The error codes are device-dependent; a definition of the bits should be obtained from the associated device documentation.

DVT17 is the transmission log (0 on an error, else the original will be posted).

DVT18 reflects the status as read from Control Register 32.

2.4.1.3 Function Code 20B

The Enable Program Scheduling function code in the Control request will enable a user program, defined by parameters IPRM1 through IPRM3, to be scheduled in response to any subsequent card asynchronous interrupt. The program name must be five characters or; if the name is less than five characters, trailing blanks are used to fill to the required five-character length.

IPRM4 may contain a single valued integer to be passed to the program, which may be retrieved by a call to RMPAR from the scheduled program. IPRM4 will be the second value returned by RMPAR. When the program is scheduled, it will also be passed the card status as read from card register 32. It too may be retrieved in RMPAR parameter 3.

The effective program schedule request is:

```
RU,(program),(interrupting LU), (passed parameter),(status)
     ↑                              ↑                 ↑
Defined by                     Defined by        From Card
IPRM1 - IPRM3                  IPRM4             Register 32
```

2.4.1.4 Function Code 21B

The program that was enabled by the function code 20B request is disabled by this Disable Program Scheduling function code. All card interrupts will be disabled when the card is not busy.

2.4.1.5 Function Code 40B

IPRM1 is the value to be saved in word 1 of the driver parameter area and contains the reconfigured Control Word to be sent to the interface card for each subsequent I/O operation. The value in IPRM1 (DVP1) will be ORed with the value specified in IPRM1 for a Read/Write request before the request executes.

Bits 0 and 1 of IPRM2 will be stored in bits 0 and 1 of driver parameter word 2; all other bits are ignored. Bit 1 should be set to 1 if the DMA AUTO bit is to be asserted on input. Bit 0 should be set to 0 for 16-bit parallel data transfers, or to 1 for 8-bit parallel data transfers.

NOTE

IPRM2 is relevant only when using modes 7 or 8. For modes 1 through 6, IPRM2 is ignored.

2.5 IDS71 STATUS REPORTING

The call sequence for the IDS71 status-reporting request is as follows:

```
CALL EXEC (13,ICNWD,ISTA1[,ISTA2][,ISTA3][,ISTA4]
```

The parameters are explained in the following paragraphs.

2.5.1 Control Word ICNWD

The Control Word format for an EXEC Status request for IDS71 is shown below.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			Z	0							LU				

2.5.2 Status Parameters ISTA1 and ISTA2

The format of the returned status parameters (ISTA1/ISTA2) is shown below.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISTA1	AV		DEVICE TYPE						0	DB	0	0	0	X	X	E
ISTA2	AV		INTERFACE TYPE=71						0	0	I/O SELECT CODE					

Specific details for each parameter follow.

2.5.2.1 ISTA1

Note that ISTA1 is the device status parameter, the only required parameter. It will contain the device status from word 6 of the device table (DVT), and is specifically defined as shown above.

NOTE

This field may in some instances contain driver dependent information, differing from the following conventions.

AV is the current device availability and is used by the system for I/O control. The DS operator command can also be used to examine the availability.

If AV is 00, the DVT is available for a new request to be initiated (the device is free to process new request).

If AV is 01, the associated device has been set "down" by the driver or the operator. New requests will be suspended on the downed device.

If AV is 10, the device is busy processing an I/O request. New requests may be pending (linked through word 2 of the DVT).

If AV is 11, the device is down, but busy with a request (such as an abort request).

DEVICE TYPE is a logical 6-bit value used to describe the type of device associated with the current DVT. All device type values are initially established at generation.

DB is set to 1 if the device is busy to indicate that the device is performing some function that prevents other operations from starting.

E is a hard error indicator set to 1 when an error condition prevents the completion of a request. When an error of this nature occurs, the appropriate error message is displayed on the system console, if the UE-bit has not been set. Whether or not the device has also been set down can be determined by examining AV as described above. Note that when the UE-bit of the control word (ICNWD) is set in an I/O request, this

error flag can be examined by the user program that made the request. RMPAR can be called to retrieve DVT16 for determining the error (only if the request was non-buffered).

X indicates device/driver dependent status bits.

2.5.2.2 ISTA2

ISTA2 is an optional interface status parameter that defines the characteristics of the interface card associated with device LU requested, obtained from word 6 of the interface table. The format is shown above.

AV indicates interface availability (the current status of the I/O interface) and is used by the system for I/O control:

00 = Interface is free; no operation is in progress.

01 = Interface locked to a device driver for future operation (is not busy with request, but locked).

10 = Interface busy with device driver request, but not locked.

11 = Interface is locked and is busy with a request.

INTERFACE TYPE is a logical 6-bit value used to describe the I/O interface card to which a device or a set of devices are connected. All interface type values are initially established at generation.

I/O SELECT CODE is the select code by which the particular interface card is addressed. This is set on the card itself by switches and is specified at generation time.

X is reserved.

2.5.3 ISTA3 and ISTA4 Status Parameters

If the Z bit of ICNWD is zero, ISTA3 returns the first word of the Driver Parameter Area, and ISTA4 returns the second word of the Driver Parameter Area.

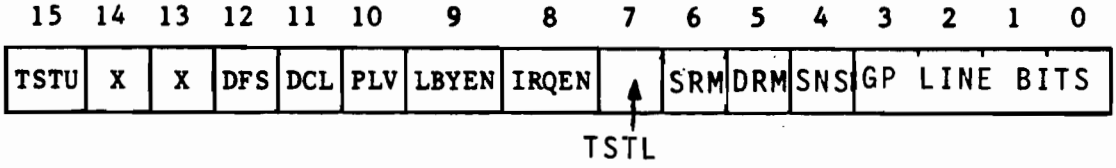
If Z is set to 1, ISTA3 is the buffer to return the Driver Parameter Area, and ISTA4 is the length of the ISTA3 buffer.

Note that IDS71 requires two words in the Driver Parameter Area,

both of which are set by the configure card control request (function code 40B). Words 3 and above of the Driver Parameter Area may be defined as required by device drivers using IDS71.

2.6 IDS71 PARALLEL INTERFACE CARD CONTROL REGISTER

The driver automatically includes the output control word for each I/O operation with the Parallel Interface Card (PIC). Bits 4 through 15 of the output control word are, in general, supplied from the first word of the Driver Parameter Area established at system generation. These bits can be redefined by a configure card control request (function code 40B). Refer to the card's Reference Manual (e.g., HP 12006A Reference Manual, part no. 12006-90001) for details of the functional operation of the card. The PIC control register format is shown below.



TSTU - test upper byte. Used for diagnostic checkout of the upper byte of the control and status registers.

X - Not used.

DFS - Device Flag Select. Selects the edge of the Device Flag (DEVFLG) pulse that will cause the data service request (SRQ) to the I/O master. The transition signals "data ready" on the input and "ready for more data" on the output:

1 - positive-going edge.

0 - negative-going edge.

DCL - Device Command Clear. Selects the edge of DEVFLG that will clear Device Command (DC). This bit only has an effect if PLV (bit 10) is clear.

1 - clear DC on the opposite edge as that seleted by DFS (i.e., DFS 1 = positive-going edge; DCL 1 = negative-going edge.)

0 - clear DC on the same edge as that selected by DFS

PLV - Pulse/Level Select. Selects between a level-mode or a pulsed command signal. The 200-nanosecond pulsed signal is one period of the system clock (SCLK).

1 - pulsed command signal

0 - level-mode Device Command

The Device Command signal is asserted during execution of an STC command, or produced automatically during each DMA transfer.

The level-mode Device Command is cleared on a selected edge of DEVFLG. If the control flip-flop is clear, the level-mode Deive Command is held in the cleared state while DMA is running.

LBYEN - this bit is set to 1 enable early termination of a DMA input transfer. Causes the assertion of ST1 for shutdown of a DMA input before word-count rollover occurs. When this feature is used, ST1 should be asserted prior to the DEVFLG accompanying the last word or byte.

IRQEN - Interrupt Request Enable. Enables the interrupt request signal to the I/O master. ST0 is asserted to set the flag, thereby causing an interrupt.

1 - enable interruprt request

0 - disable interrupt request from ever being asserted.

TSTL - Test Lower Byte. TSTL is connected to bit 7 of the status word. When set, enables diagnostic testing of the operation of the lower byte of the control and status registers.

SRM - Select Status Register Mode.

1 - load status register (register 32) on each DEVFLG assertion.

0 - cause status register to act like a transparent latch so that status is dynamically available. (If device does not have DEVFLG, SRM must always be set to 0.)

DRM - Select Data Register Mode.

1 - load input data register on each DEVFLG assertion.

0 - cause data register to act like a transparent latch so that 16 data bits are dynamically available. Note that

for modes 5 and 6, DRM must always be set to 0.

SNS - Interface Sense select. Select either ground-true or high-true for transfer of all 40 status, dat, and control signals.

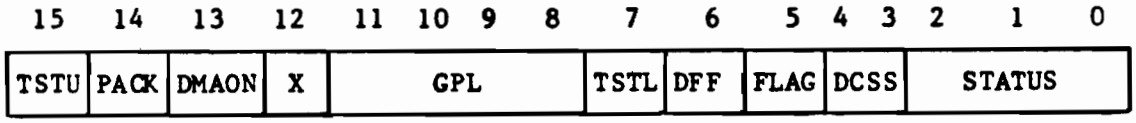
0 - invert all signals for ground-true device interface.

1 - do not invert signals; a high-true positive device interface results.

GPL - General Purpose Lines. The four GPL bits may be used to address, control, or handshake with various types of peripheral devices. Then are latched on the 12006A during DMA self-configuration, and are constantly driven out to the device.

2.7 IDS71 PARALLEL INTERFACE CARD STATUS

DVT18 reflect the Parallel Interface Card status from register 32 after each EXEC request to the driver. This value can be obtained by making a dynamic status control request to obtain the immediate status of the device, or by making a call to RMPAR after an EXEC Read, Write, or Control request to obtain the status of the last request. The format of the word is shown below (DVT18 word format for IDS71 dynamic status request):



TSTU - set to 1 to test upper byte of control and status registers. This bit is used for diagnostic purposes. It is connected to the TSTU bit of the control register.

PACK - Q output of PACK flip-flop. This bit is set to 1 whenever byte mode DMA is running.

DMAON - Q output of DMAON flip-flop. This bit is set to 0 when DMA is running, and set to 1 at all other times.

X - Not used.

GPL - General Purpose Lines. These are identical to the GPL

bits of the control register and are used for addressing, control, or handshaking with various types of peripheral devices.

TSTL - used for diagnostic purposes to check out the operation of the lower byte of the control and status registers. This bit is connected to the TSTL-bit of the control register.

DFF - used for diagnostic purposes to check out the operation of the Device Command flip-flop.

FLAG - contains the inverted sense of the Device Flag line. Initially, FLAG should be in its non-active state. The information is chiefly used for diagnostic purposes.

DCSS - contains the state selected for the Device Command sense switch.

1 - active-high Device Command selected.

0 - active-low Device Command selected.

The four STATUS lines are loaded on each DEVFLG assertion if bit 6 (SRM) of the control register is set to 1. If SRM is set to 0, the four lines will reflect dynamic status information of the device connected to the PIC.

GENERATION REQUIREMENTS	SECTION III

3.1 INTRODUCTION

This section provides information necessary for the generation of IDS71 into the RTE-A operating system. The information is presented in the manner of types of action to be taken (or not required) in each phase.

3.2 GENERAL CONSIDERATIONS

During the Initialization Phase no additional action requirements exist for IDS71 inclusion.

During the driver Relocation Phase the following module must be relocated:

```
%IDS71
```

3.3 TABLE GENERATION PHASE

The Interface Table (IFT) for driver IDS71 must be constructed during this phase. It can be done with the following command:

```
IFT,%IDS71,SC:sc
```

Where: sc is the octal select code of the PIC (e.g., 12006A).

The defaults contained in the default file (%IDS71) are:

```
Entry point (Eentry point): IDS71
Queuing option (QU:qu): None
IFT extension (TX:tx): 8 words
```

At this point the DVT's must be set up for all devices to be

attached to the Parallel Interface Card (e.g., 12006A). A minimum of two words must be allocated for each DVT parameter area.

3.4 MEMORY ALLOCATION PHASE

No specific action required for inclusion of IDS71.

3.5 USER PROGRAM RELOCATION PHASE

Again no specific action is required for IDS71 inclusion.

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