SERVICE MANUAL

HEWLETT-PACKARD MODEL 91000A

PLUG-IN 20kHz ANALOG-TO-DIGITAL INTERFACE SUBSYSTEM

15 APRIL 1974

HEWLETT hp PACKARD

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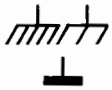
Terminal devices fed from the interior by live voltages that may be dangerous when connecting to or disconnecting from those devices shall be marked with the flash shown when the voltage exceeds 1 KV: The flash shall be red (IEC 348;18c).

Earth Terminals. If the use of this symbol for the protective earth terminal is not permitted by National Standards, it may be modified, for example, by being placed inside a circle (IEC 348;18a).

AC current (IEC 117-1, symbol No. 3).

DC current (IEC 117-1, symbol No. 2).

AC or DC current (IEC 117-1, symbol No. 8).



Frame or chassis connection. The hatching may be completely or partly omitted if there is no ambiguity. If the hatching is omitted, the line representing the frame or chassis shall be thicker (IEC 117-1, symbol No. 87).

A Ampere (IEC 117-4, symbol No. 356).

V Volt (IEC 117-4, symbol No. 357).

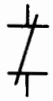
VA Voltampere (IEC 117-4, symbol No. 358).

W Watt (IEC 117-4, symbol No. 360).

Wh Watthour (IEC 117-4, symbol No. 361).

VAh Voltamperehour (IEC 117-4, symbol No. 362).

Hz Hertz (IEC 117-4, symbol No. 365).



Contactor, normally closed. In order to avoid confusion with the symbol for a capacitor, the distance between the horizontal (as drawn here) lines should be at least equal to the length of those lines (IEC 117-3, symbol No. 215.2).

In addition the following describes the use of Warnings, Cautions and Notes used in HP Automatic Test Sytem Manuals.

Warnings, cautions and notes. (All) Warnings and cautions shall precede the text to which each applies but notes may precede or follow applicable text depending on the material to be highlighted. Warnings, cautions, and notes shall not contain procedural steps nor shall they be numbered. When a warning, caution, or note consists of two or more paragraphs, the heading WARNING, CAUTION, NOTE, shall not be repeated above each paragraph. If it is ever necessary to precede a paragraph by both a warning and a note, or a caution and a note, etc, they shall appear in the sequence as noted, namely, warnings, cautions, notes. Such inserts in the text shall be short and concise and be used to emphasize important and critical instructions.

WARNING

An operating procedure, practice, etc, which, if not correctly followed, could result in personal injury or loss of life.

CAUTION

An operating procedure, practice, etc, which, if not strictly observed, could result in damage to, or destruction of, equipment.

NOTE: An operating procedure, condition, etc, which it is essential to highlight.

Health hazards precaution data. (All) When hazardous chemicals or adverse health factors, in the environment or use of the equipment cannot be eliminated, appropriate precautionary requirements shall be included.

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual provides general information, installation instructions, theory of operation, maintenance instructions and replaceable parts information for the HP 91000A plug-in 20 kHz analog-to-digital interface subsystem, hereinafter referred to as the DAS (data acquisition subsystem).

1-3. DESCRIPTION

1-4. The DAS, Figure 1-1, is a complete computer-controlled data acquisition subsystem contained on a single printed circuit card. The DAS plugs into the mainframe of an HP 2100 series computer, deriving its control signals from and delivering its data output to the computer. External analog data, either eight differential or 16 single-ended channels, are input to the DAS via a cable and connector separate from the mainframe interface.

1-5. The DAS contains a high-level multiplexer (HLMPX), a sample and hold (S/H), an analog-to-digital converter (ADC), and a DC-to-DC converter, as well as the interface and control logic necessary to communicate with the computer.

1-6. Under computer control, the DAS scans multiple analog input signals, converts the signals to 12-bit two's complement binary representation, and returns the binary data to the computer for processing. The computer commands the DAS to perform a specific data acquisition by sending a control word which defines mode of operation and address of desired data. This word is followed by a set control signal (STC) which initiates the actual data acquisition. After the DAS executes the specified operation, it announces completion of the operation by setting the flag and interrupt lines of the computer I/O bus and returning a 12-bit response word which is the binary equivalent of the acquired analog data. Data can be sequentially scanned or selected in any desired order under software control.

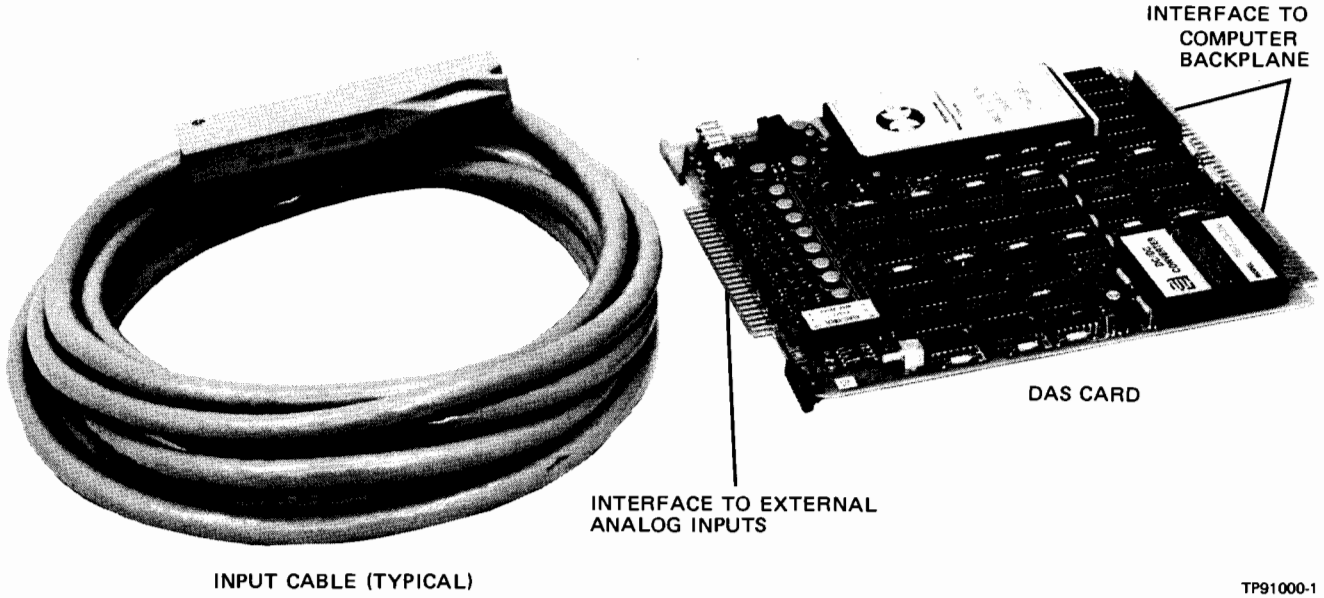


Figure 1-1. HP 91000A Data Acquisition Subsystem (DAS)

1-7. Input data channels can be configured as eight differential or 16 single-ended. Input range is +10.235 to -10.240 volts, with overvoltage protection. This voltage range produces a resolution of exactly 5 millivolts for the least significant bit (LSB).

1-8. EQUIPMENT SUPPLIED

1-9. The standard DAS kit contains the following items:

Item	HP Part Number
DAS Card	91000-60001
Pacer Connector Assembly	1250-1223
Input Connector Assembly	02313-60010
Verification Program	91000-60002
Service Manual	91000-93001
Programming Manual	91000-93003

1-10. OPTIONS

1-11. Hardware and software options are listed below.

Option	Item	HP Part Number
005	Single-Ended Input Cable	02313-60007
006	Differential Input Cable	02313-60008
S30	D.62 Non-DMA Driver	29007-60001
	D.62 DMA Driver	29008-60001
	I2313 Interface Routine	29010-60001
S50	DVR62 RTE Driver	29009-60001
	R2313 RTE Module	29011-60001
	P2313 RTE Module	29011-60002
	D2313 RTE Module	29011-60004
S60	DVR62 RTE Driver	29009-60001

1-12. IDENTIFICATION

1-13. The HP 91000A Data Acquisition Subsystem is identified by a serial number, a part number, and a revision code (see figure 4-5). The 10-character serial number (e.g., 1009A99999) identifies a specific DAS card, whereas the part number (91000-60001) is the same for all cards. The revision code (e.g., C 1217 6) is a manufacturing identification of the card. Cards having the same part number but different revision codes are electrically identical unless noted otherwise. If the revision code stamped on the card is not the same as the revision code specified on the title page of this manual, a supplement supplied with this manual will define the differences between the card and the card described herein.

1-14. SPECIFICATIONS

1-15. Table 1-1 lists the more important electrical and physical specifications of the DAS.

1-16. REFERENCE PUBLICATIONS

1-17. The following Hewlett-Packard publications contain information that is useful in programming and using the DAS.

Publication Number	Title
02100-90002	Installation and Maintenance Manual, Model 2100A Computer
5950-8718	A Pocket Guide to Interfacing HP Computers

Table 1-1. DAS Specifications

Number of Inputs		16 single-ended or 8 differential; jumper selectable
Resolution		12 bits, including sign; LSB = 5 mV
Full Scale Input		+10.235V to -10.240V
Throughput Rate to Buffer		To 20 kHz, maximum, via direct memory access (DMA)
Sample & Hold	Delay	150 nsec from trailing edge of pace pulse to "hold" strobe
	Aperture	<250 ns total jitter with respect to external pace pulse
External Pace Pulse Input		+4.5V ±0.5V, 1.5 ±0.5 μS pulse referenced to 0 ±0.5V baseline, 100Ω source, TTL compatible[3]
Overall Accuracy[1]	At 25° ±5°C	±0.1% fs ±1/2 LSB
	Temp. Coeff.	±0.004% fs/°C over 0° to 55°C range[2]
Input Impedance	Power On	>5MΩ
	Power Off	1 kΩ ±10%
Maximum Input		±10.5V diff. + common mode, or high-to-computer chassis (S.E. inputs); ±10.24V high-to-common (S.E. inputs) for rated accuracy; up to ±15V, any input line to computer chassis, w/o damage.
Input Protection		To ±15V, any input to computer chassis without damage.
Source Resistance		To 1 kΩ balanced or unbalanced.
Crosstalk Rejection		⩾80 dB, dc to 100 Hz, using differential input
Common Mode Rejection		⩾80 dB, dc to 100 Hz, using differential input
Common Mode Return		To 10K ohms +50 μh with up to 125 ft of HP 8120-1781 input cable for differential inputs.
Computer I/O Channel		One
Interface Current		2.4A (+4.75V), 0.065A (-2V) drawn from computer or I/O extender.
Memory Words Required		560 words for D.62 (non-DMA BCS driver) or 700 words for D.62A (DMA BCS driver) and 130 words for I2313 (FORTRAN/ALGOL interface). 440 words for RTE driver DVR62 and 370 words for R2313 (FORTRAN/ALGOL interface).
Operating Conditions		0° to 55°C (32° to 131°F)[2] , same as HP 2100 series computers, up to 15°C (59°F) should be allowed for temperature rise inside HP system cabinets.
Weight		Net: 4 lb. (1.8 kg); Shipping: 6 lb. (2.7 kg).
System Compatibility		Hardware and software compatible with all HP 9600 series computer systems for data acquisition and control.

1. With respect to source used for calibration. Includes 3-sigma noise; linearity; offsets; 8-hour stability; gain calibration transfer, and dynamic response errors; ±10% line voltage variation. Includes multiplexer, sample-and-hold amplifier, and ADC.

2. Temperature range outside computer.

3. Mating connector supplied.

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. The installation instructions in this section provide the recommended procedures to prepare the DAS for operation with the computer in the user's system. Subsystem installation instructions include unpacking and initial inspection, cable preparation, and card installation.

2-3. UNPACKING AND INITIAL INSPECTION

2-4. Any shipping container that appears damaged should be unpacked with the carrier's agent present. Carefully inspect plug-in card for damage (scratches, cracks, etc.). Check that all equipment specified in the purchase order has been delivered; refer to Section I for the list of components supplied with the standard subsystem and the list of optional equipment. If any equipment is missing, damaged, or fails to meet specifications, immediately notify the carrier and nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Retain the shipping containers and packing material for the carrier's inspection and for future use.

2-5. POWER REQUIREMENTS

2-6. The DAS derives its operating power from the 2100 computer, and requires the following:

+5.0 Vdc ±5% at 2.4A
-2.0 Vdc at 0.05A

2-7. PLUG-IN CARD INSTALLATION

CAUTION

Always make sure that the HP 2100 power is OFF when installing or removing the DAS card. Failure to observe this caution may damage the card.

2-8. The DAS is a clean assembly and should be handled only by its side edges (edges without PC strip connections) or extractor handles to avoid contamination of the card and degradation of performance.

2-9. Jumpers on the DAS card are used to program the DAS to accept either single-ended or differential inputs. Jumper W2 must always be installed. If the requirement is to switch differential input signals, install jumpers as shown in Figure 2-1. If the requirement is to switch single-ended input signals, install jumpers as shown in Figure 2-2. In either case, all jumpers must be positioned before the card is installed.

2-10. To install DAS card in the HP 2100 card cage, proceed as follows:

a. At front of HP 2100 set POWER switch to POWER OFF. Remove cover to access I/O slots.
b. Hold DAS card vertical with component side facing left and plastic card extractors facing away from HP 2100 mainframe.
c. Carefully slide DAS card down into its assigned card slot.
d. Seat DAS card fully in its mating backplane receptacle by pressing firmly inward on its card extractors.

2-11. SINGLE-ENDED INPUT SIGNAL CONNECTION

2-12. Table 2-1 provides detailed wiring information for the accessory single-ended input cable assembly, HP part number 02313-60007, and Figure 2-3 illustrates the proper method of connecting the unterminated end of this cable assembly to high-level (±10.24 volt) single-ended sources. If the user wishes to fabricate his own cable using the connector kit supplied with the DAS, refer to the following paragraph.

2-13. Figure 2-4 presents the construction details and parts list for the input connector kit, HP part number 02313-60010, supplied with the DAS. Cable of the type specified in Table 2-1 is available from Hewlett-Packard (HP part number 8120-1782). To fabricate the cable, proceed as follows:

a. Strip outer jacket of cable back 5 inches (127 mm) and prepare each cable end as shown in Figure 2-5.

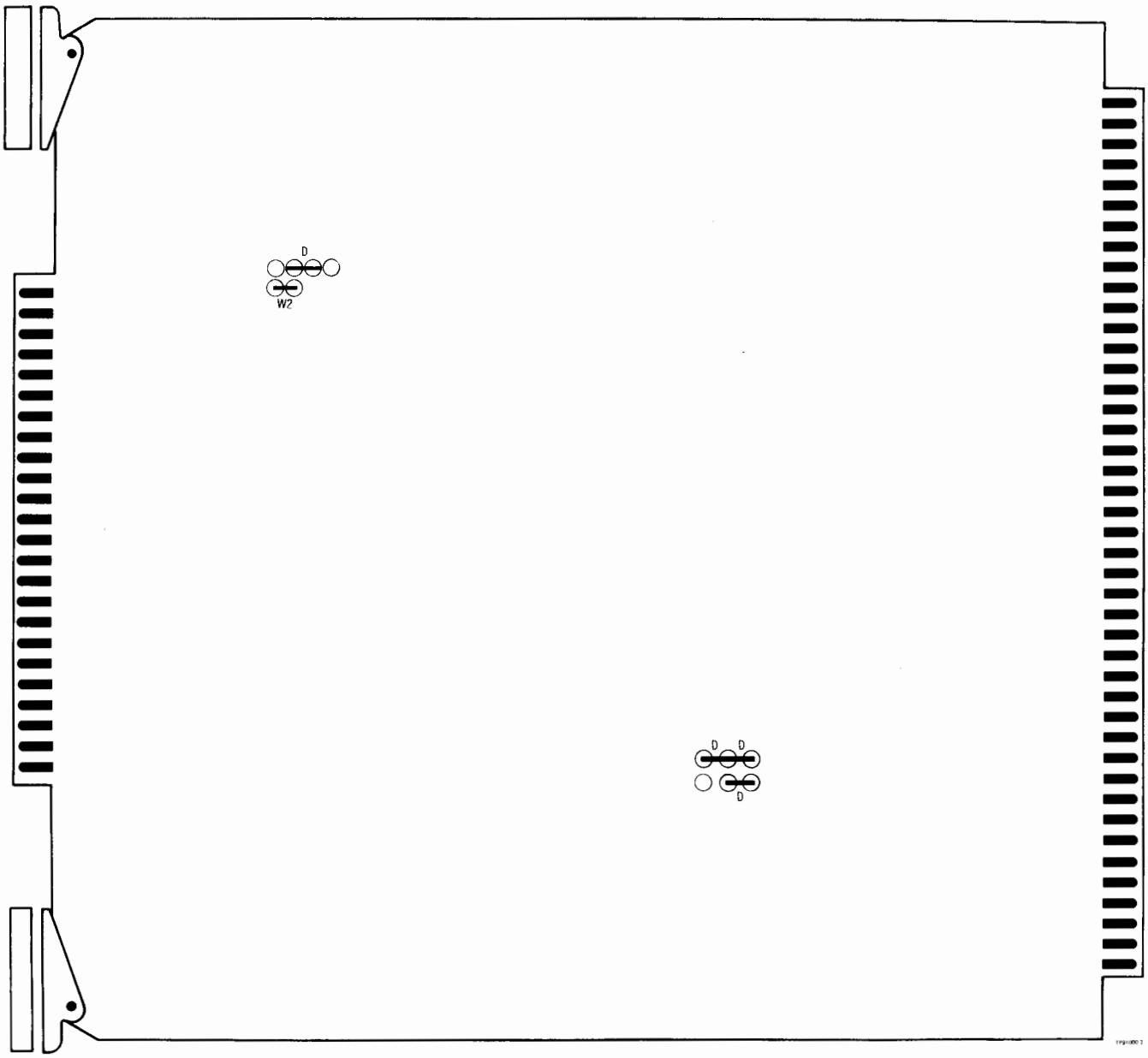


Figure 2-1. Jumper Configuration for Differential Inputs

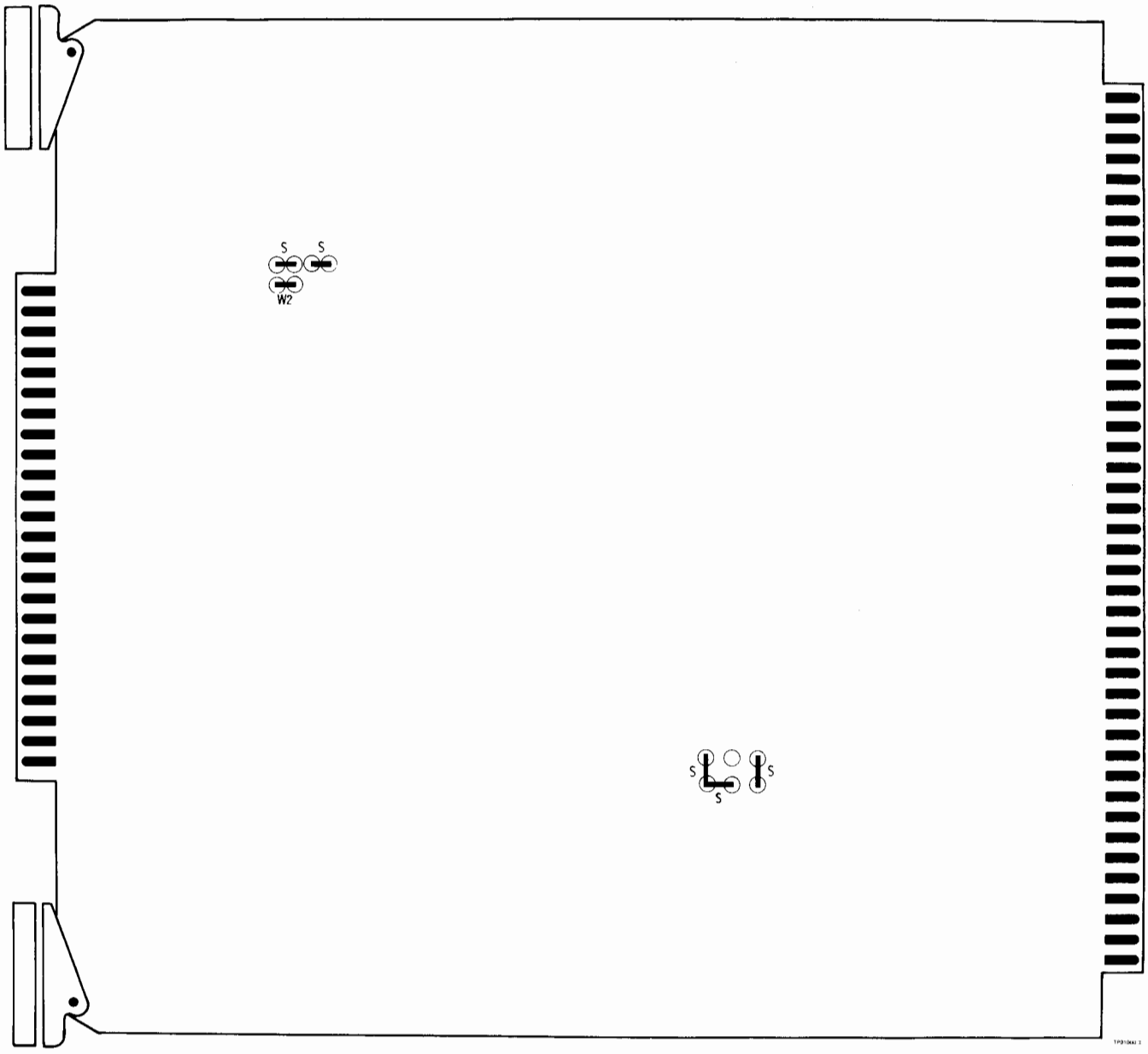
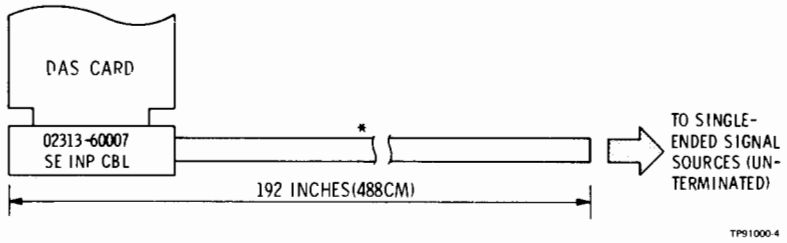


Figure 2-2. Jumper Configuration for Single-Ended Inputs

Table 2-1. Single-Ended Input Cable Assembly, HP Part No. 02313-60007



Connector Pin Assignment	Color Code	Remarks
1	Gray/Black	SE CH0
2	Shields	SE CH0 and CH1 Shields
3	Gray/Brown	SE CH1
4	Gray/Red	SE CH2
5	Shields	SE CH2 and CH3 Shields
6	Gray/Orange	SE CH3
7	Gray/Yellow	SE CH4
8	Shields	SE CH4 and CH5 Shields
9	Gray/Green	SE CH5
10	Gray/Blue	SE CH6
11	Shields	SE CH6 and CH7 Shields
12	Gray/Violet	SE CH7
13	Gray	SE CH8
14	Shields	SE CH8 and CH9 Shields
15	Gray/Black/Brown	SE CH9
16	Gray/Black/Red	SE CH10
17	Shields	SE CH10 and CH11 Shields
18	Gray/Black/Orange	SE CH11
19	Gray/Black/Yellow	SE CH12
20	Shields	SE CH12 and CH13 Shields
21	Gray/Black/Green	SE CH13
22	Gray/Black/Blue	SE CH14
23	Shields	SE CH14 and CH15 Shields
24	Gray/Black/Violet	SE CH15
A	Gray/Brown/Red	* *
B	Shields	
C	Gray/Brown/Orange	
D	Gray/Brown/Yellow	* *
E	Shields	
F	Gray/Brown/Green	

Table 2-1. Single-Ended Input Cable Assembly, HP Part No. 02313-60007 (Continued)

Connector Pin Assignment	Color Code	Remarks
H	Gray/Brown/Blue	* *
J	Shields	
K	Gray/Brown/Violet	
L	Gray/Red/Orange	* *
M	Shields	
N	Gray/Red/Yellow	
P	Gray/Red/Green	* *
R	Shields	
S	Gray/Red/Blue	
T	Gray/Red/Violet	* *
U	Shields	
V	Gray/Orange/Yellow	
W	Gray/Orange/Green	* *
X	Shields	
Y	Gray/Orange/Blue	
Z	Gray/Orange/Violet	* *
AA	Shields	
BB	Gray/Yellow/Green	

*32 miniature coaxial cables in jade gray PVC outer jacket; bulk cable is HP Part No. 8120-1782.

**These wires provided for possible future use with an upgraded HP analog subsystem.

b. Referring to Table 2-1 for the channel assignment versus connector pin number, start making connections at bottom of connector; i.e., pin 24 and pin 23. Connect coaxial shield to adjacent pins as specified in Table 2-1.

c. Continue connecting individual coaxial cables to next pins used, following pin sequence in descending order (23, AA....A).

d. After all connections have been made, assemble connector kit as shown in Figure 2-4, using appropriate strain relief (cable clamp) as required by cable size. Insert set screw and tighten strain relief sufficiently to prevent cable from moving inside hood.

CAUTION

Do not over-tighten the strain relief; firm tightening is sufficient. Over-tightening may split the connector hood or damage the cable.

NOTE

Additional wires indicated in Table 2-1 are provided for possible future use with an upgraded analog subsystem. It is advisable to connect all cable wires to the 48-pin connector even though not all are used. Connecting them later would be very difficult.

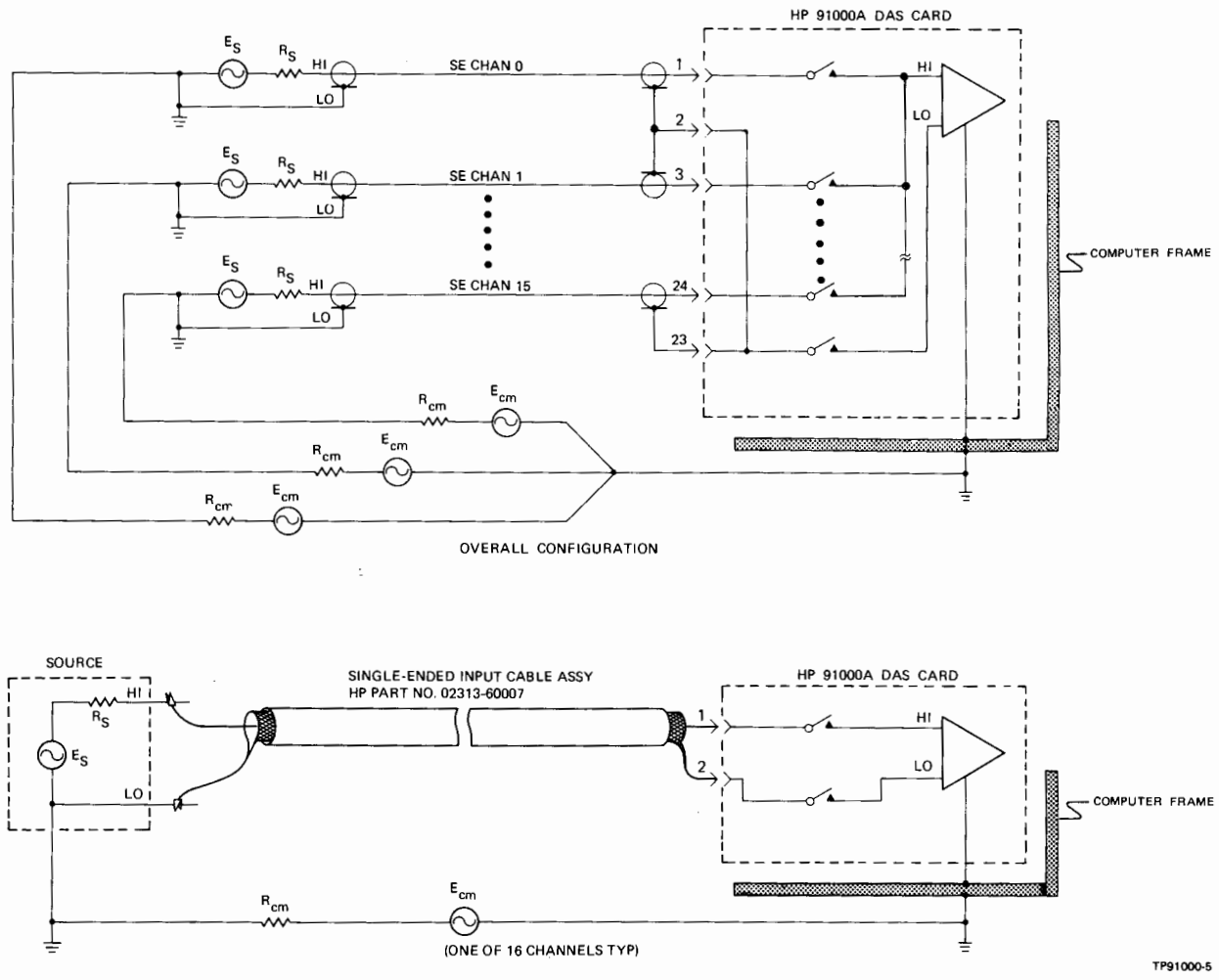
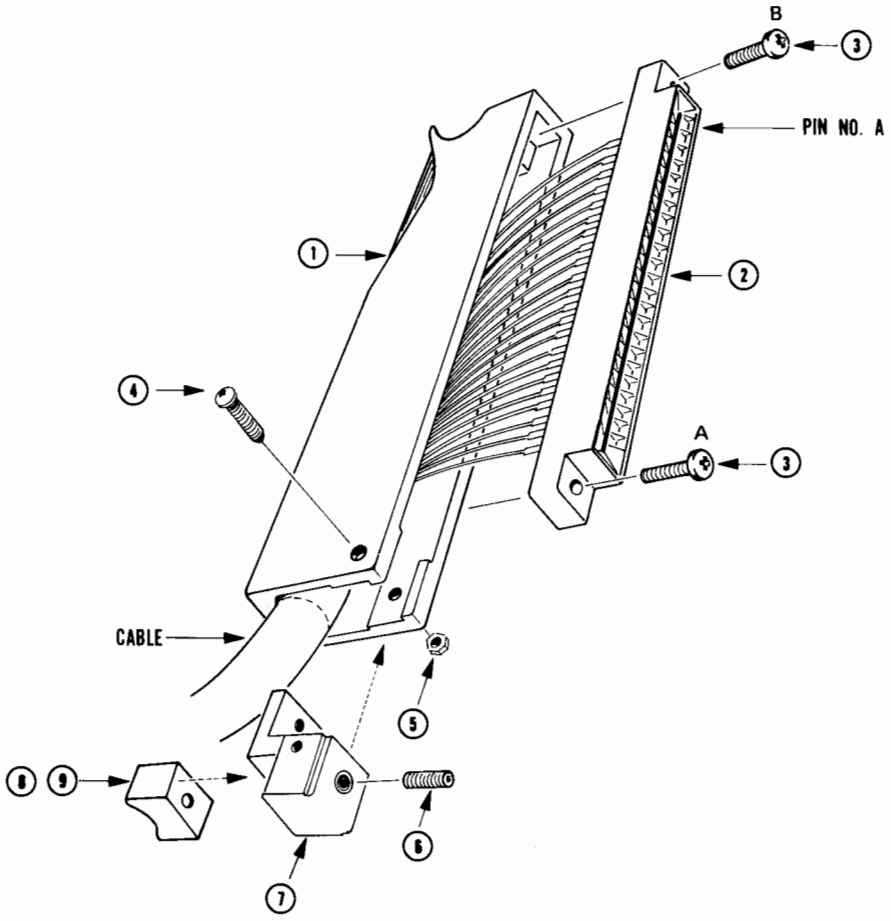


Figure 2-3. Single-Ended Input Wiring

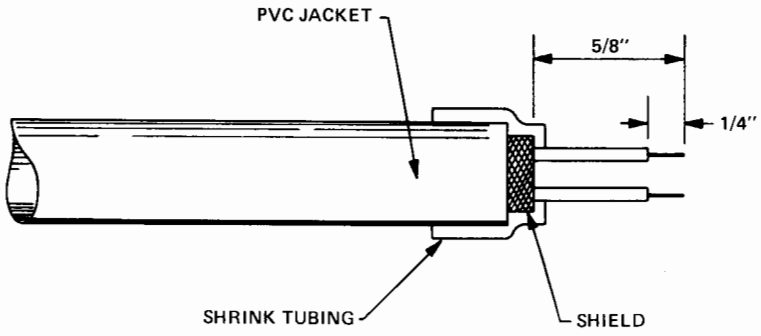


PARTS LIST:

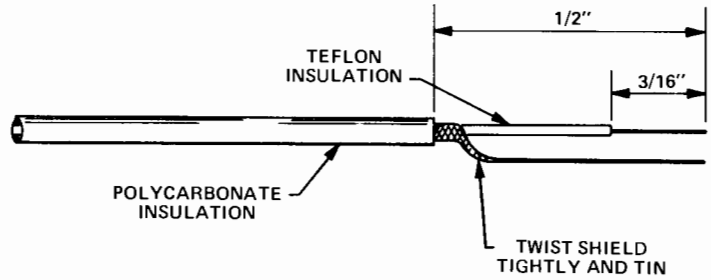
ITEM	DESCRIPTION	QTY	HP PART NO.
1	HOOD	1	5040-6071
2	CONNECTOR	1	1251-2518
3	SELF-TAPPING SCREW	2	0624-0098
4	PAN-HEAD SCREW, 4-40 x .562	1	2200-0091
5	HEX NUT, .187	1	2260-0002
6	SET SCREW	1	3030-0143
7	MOUNTING BLOCK	1	5040-6072
8	LARGE CABLE CLAMP	1	5040-6003
9	SMALL CABLE CLAMP	1	02313-20003

TP91000-6

Figure 2-4. Connector Kit (HP Part No. 02313-60010)



TWISTED-PAIR CABLE END PREPARATION



MINIATURE COAXIAL CABLE END PREPARATION TP91000-7

Figure 2-5. Cable End Preparation

2-14. DIFFERENTIAL INPUT SIGNAL CONNECTION

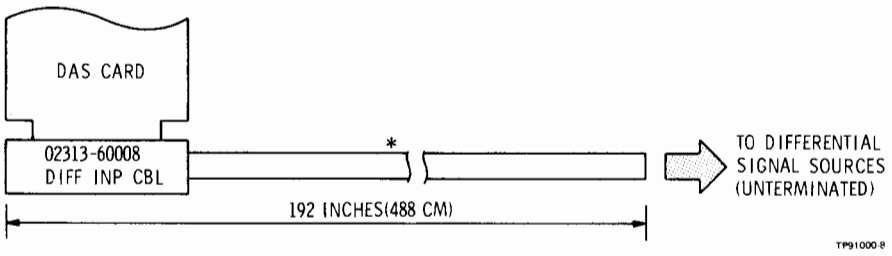
2-15. Table 2-2 provides detailed wiring information for the accessory differential input cable assembly (HP part number 02313-60008), and Figures 2-6 and 2-7 show the proper methods of connecting the unterminated end of this cable assembly to high-level (±10.24 volts) differential or single-ended signal sources; high-level, single-ended sources are shown intentionally connected as differential inputs to eliminate ground loops and thereby effectively reduce the common-mode voltage. A separate wire (not shielded) connected between the power main ground and the computer mainframe chassis is recommended to ensure a good common ground.

NOTE

Every differential source must have a return to power main ground through an impedance not greater than the maximum common-mode impedance specified in Table 1-1.

If the user wishes to fabricate his own cable using the connector kit supplied with the DAS, refer to the following paragraph.

Table 2-2. Differential Input Cable Assembly, HP Part No. 02313-60008



Connector Pin Assignment	Color Code	Remarks
1	Black	HI
3	White	DIFF CH0 LO
		SH
4	Brown	HI
6	White	DIFF CH2 LO
		SH
7	Red	HI
9	White	DIFF CH4 LO
		SH
10	Orange	HI
12	White	DIFF CH6 LO
		SH
13	Yellow	HI
15	White	DIFF CH8 LO
		SH
16	Green	HI
18	White	DIFF CH10 LO
		SH
19	Blue	HI
21	White	DIFF CH12 LO
		SH
22	Violet	HI
24	White	DIFF CH14 LO
		SH
A	White/Black	* *
C	White	
D	White/Brown	* *
F	White	

Table 2-2. Differential Input Cable Assembly, HP Part No. 02313-60008 (Continued)

Connector Pin Assignment	Color Code	Remarks
H	White/Red	* *
K	White	
L	White/Orange	* *
N	White	
P	White/Yellow	* *
S	White	
T	White/Green	* *
V	White	
W	White/Blue	* *
Y	White	
Z	Gray	* *
BB	White	

*Cable is 16 shielded twisted pairs in jade gray PVC outer jacket; bulk cable is HP Part No. 8120-1781. Note that shields are not connected at DAS end of cable.

**These wires provided for possible future use with an upgraded HP analog subsystem.

2-16. Figure 2-4 presents the construction details and parts list for the input connector kit, HP part number 02313-60010, supplied with the DAS. Cable of the type specified in Table 2-2 is available from Hewlett-Packard (HP part number 8120-1781). To fabricate the cable, proceed as follows:

a. Strip outer jacket of cable back 5 inches (127 mm) and prepare each cable end as shown in Figure 2-5.

b. Referring to Table 2-2 for channel assignments versus connector pin numbers, start making connections at bottom of connector; i.e., pin BB and pin Z.

c. Continue connecting the individual twisted-pair cables to next pins used, following pin sequence in descending order (24, 22, Y, W.....C, A, 3, 1).

d. After all connections have been made, assemble connector kit as shown in Figure 2-4, using appropriate strain relief (cable clamp) as required by cable size. Insert set screw and tighten strain relief sufficiently to prevent cable from moving inside hood.

CAUTION

Do not over-tighten the strain relief; firm tightening is sufficient. Over-tightening may split the connector hood or damage the cable.

NOTE

Additional wires indicated in Table 2-2 are provided for possible future use with an upgraded analog subsystem. It is advisable to connect all cable wires to the 48-pin connector even though not all are used. Connecting them later would be very difficult.

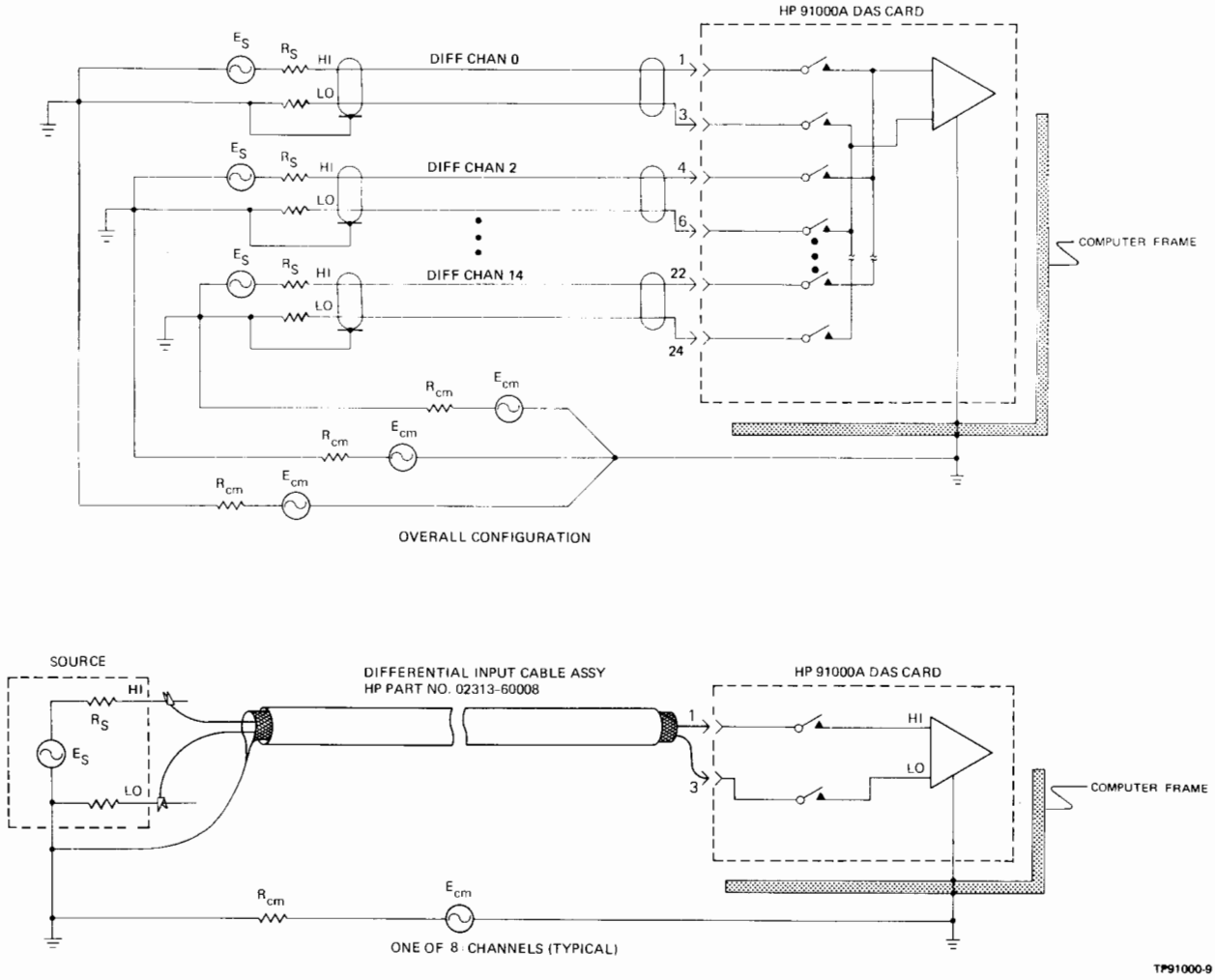


Figure 2-6. Differential Input Wiring-Differential Sources

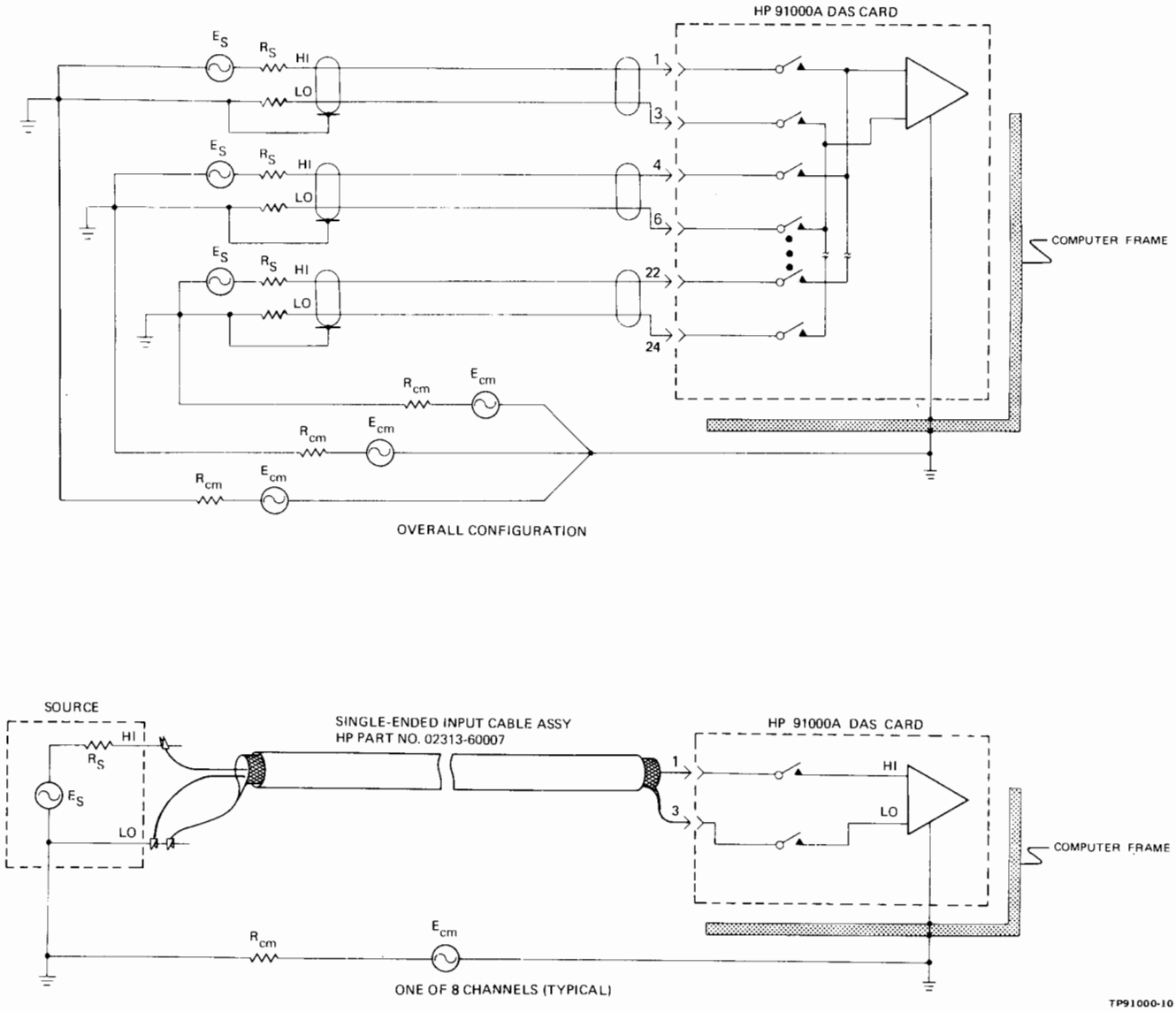


Figure 2-7. Differential Input Wiring-Single-Ended Sources

2-17. PACE PULSE SIGNAL CONNECTION

2-18. If the DAS is to be timed with an external pace pulse, the pulse must have the characteristics defined in Figure 2-8, and must be brought into the DAS via a cable (not supplied) fabricated in accordance with Figure 2-9.

2-19. CABLE INSTALLATION

CAUTION

Always make sure that the HP 2100 power is OFF when installing or removing cables. Failure to observe this precautiom may damage the equipment.

2-20. To install a subsystem cable to the 48-pin connector of the DAS card installed in the HP 2100, carry out the following steps:

a. At front of the HP 2100, set POWER switch to POWER OFF.

b. Gain access to the computer card cage and place the cable connector near the DAS card in the computer.

c. Check that card is firmly seated in its backplane receptacle.

d. Orient hood on cable connector so that cable points toward cable exit port.

e. Carefully slide cable connector onto PC pin connections on card.

2-21. PERFORMANCE VERIFICATION

2-22. Perform verification test as specified in Section IV.

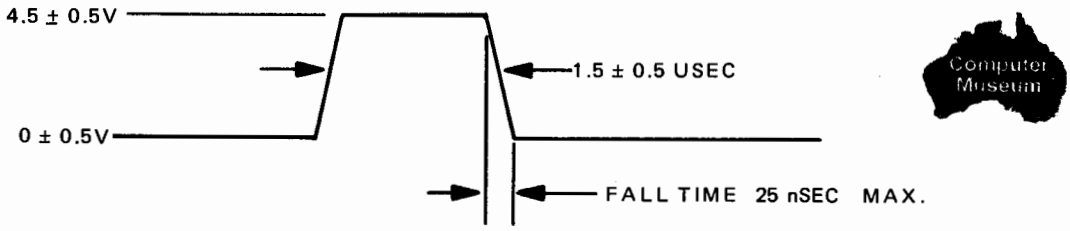
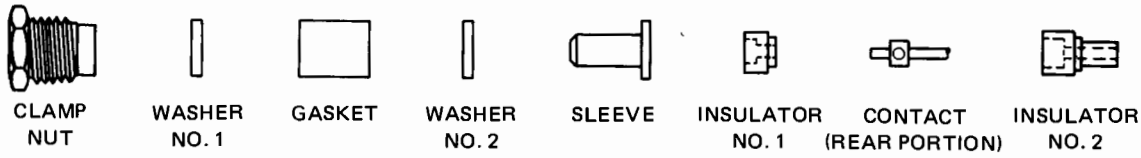
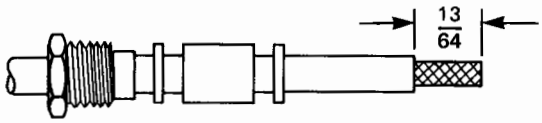
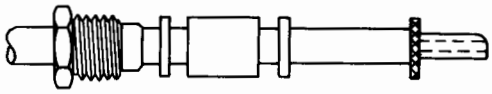


Figure 2-8. Characteristics of Pace Pulse

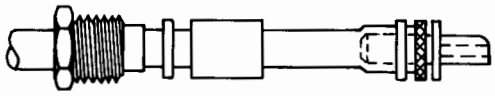




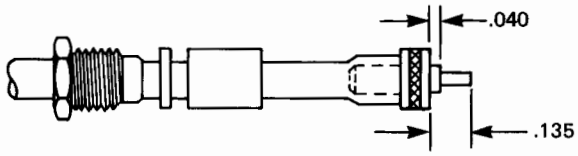
(1) USING 50-OHM CABLE, RG-174/U, RG-180/U, RG-188/U OR EQUIVALENT SLIDE CLAMP NUT, WASHER NO. 1, GASKET AND WASHER NO. 2 BACK ON CABLE. TRIM CABLE JACKET TO DIMENSION SHOWN, BEING CAREFUL NOT TO NICK BRAID.



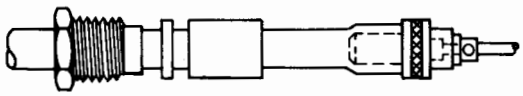
(2) SPREAD OUT BRAID AS SHOWN. MAKE A SLIGHT CHAMFER ON CABLE CORE TO ASSIST IN ASSEMBLING SLEEVE.



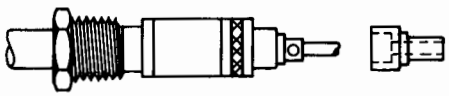
(3) MOVE WASHER NO. 2 UP CLOSE TO BRAID. THEN INSERT SLEEVE BETWEEN THE BRAID AND CORE AND TRIM BRAID TO A DIAMETER SMALLER THAN FLANGE.



(4) SLIDE SLEEVE IN UNTIL FLANGE RESTS AGAINST BRAID. TRIM CABLE CORE AND CENTER CONDUCTOR TO DIMENSIONS SHOWN, BEING CAREFUL NOT TO NICK STRANDS OF CENTER CONDUCTOR.



(5) TIN CENTER CONDUCTOR (DO NOT OVER TIN). SLIP INSULATOR NO. 1 OVER CABLE DIELECTRIC UNTIL IT IS FLUSH AGAINST SLEEVE FLANGE, ASSEMBLE CONTACT ONTO CENTER CONDUCTOR UNTIL SHOULDER OF CONTACT IS FLUSH AGAINST INSULATOR. HEAT CONTACT BRIEFLY TO MAKE SOLDERED CONNECTION.



(6) PLACE FRONT INSULATOR NO. 2* OVER CONTACT, MOVE GASKET, WASHER NO. 1 AND CLAMP NUT UP TO WASHER NO. 2. INSERT INTO BACK END OF BODY AND TIGHTEN CLAMP NUT TO TORQUE OF 90 - 100 IN. OZ.

*JACK FRONT INSULATOR IS PRE-ASSEMBLED INTO BODY AT THE FACTORY.

TP91000-33

Figure 2-9. Fabrication of Pace Pulse Input Cable

SECTION III
PRINCIPLES OF OPERATION

3-1. INTRODUCTION

3-2. This section provides a functional analysis, a discussion of the modes of operation, and a detailed circuit analysis of the DAS. The functional analysis presents a general overview to show how the DAS performs its intended functions in a computer- controlled environment. The discussion of modes of operation highlights the more important features of the three methods of data acquisition: random, digitize, and sequential. The detailed circuit analysis defines the specific purpose and function of each component in the subsystem.

3-3. FUNCTIONAL ANALYSIS

3-4. The DAS card is a computer-controlled data acquisition subsystem which scans as many as 16 analog input signals, converts them to 12-bit parallel digital form, and returns the digital data to the computer.

3-5. The DAS card can be configured for 16 single-ended or 8 differential analog signals in the range of +10.235 to -10.240 volts. The DAS can scan these inputs or it can take single or multiple readings on a selected channel. The different modes which may be programmed are defined as Random Mode, Digitize Mode, and Sequential Mode. The Random mode is normally used to obtain a single isolated reading whereas the Digitize and Sequential modes are employed for multiple readings and yield maximum operating speed.

3-6. Figure 3-1 shows the structural organization of the DAS card. The major functions are:

High-Level Multiplex (HLMPX) – Selects 1 of 16 single-ended or 1 of 8 differential analog data channels with a nominal range of ±10.240 volts

Differential-to-Single-Ended Converter – Converts differential signals to single-ended.

Sample and Hold – Holds signal while analog-to-digital converter converts to digital

Analog-to-Digital Converter – Converts analog input data to 12-bit binary in two's complement format

Digital Logic – Interfaces to computer I/O bus, decodes commands, controls analog circuitry, returns data to computer.

3-7. MODES OF OPERATION

3-8. The DAS has two basic modes of operation: multiplex and normalize. Both modes are controlled by bits 15, 14, and 13 of the computer command word, as shown in Figure 3-2. The available operating modes are described in the following paragraphs.

3-9. MULTIPLEX MODES

3-10. In the multiplex mode the DAS digitizes analog input data. Three possible modes are available:

a. Digitize Mode-Program-selected channels are digitized. Each flag returned with data corresponds to previously addressed channel. This mode enables the subsystem to operate at maximum speed.

b. Sequential Mode–Channels are digitized in sequential order, starting with a program- selected first channel. Timing and speed are similar to digitize mode.

c. Random Mode-Program-selected channels are digitized, not necessarily in a sequential order. Each flag returned with data corresponds to addressed channel.

3-11. When bit 12 is 0, the DAS makes the data acquisition at a time determined by the computer program. When bit 12 is 1, the DAS waits for an external pace pulse to perform the data acquisition. The pacing concept is described in detail in paragraphs 3-19 through 3-23.

3-12. DIGITIZE MODE–Digitize mode timing is shown in Figure 3-3. The computer commands the subsystem to perform a specific operation by sending to the DAS card a 16-bit command word, caused by an OTA instruction (IOO signal), followed by set control, clear flag (STC, CLF)

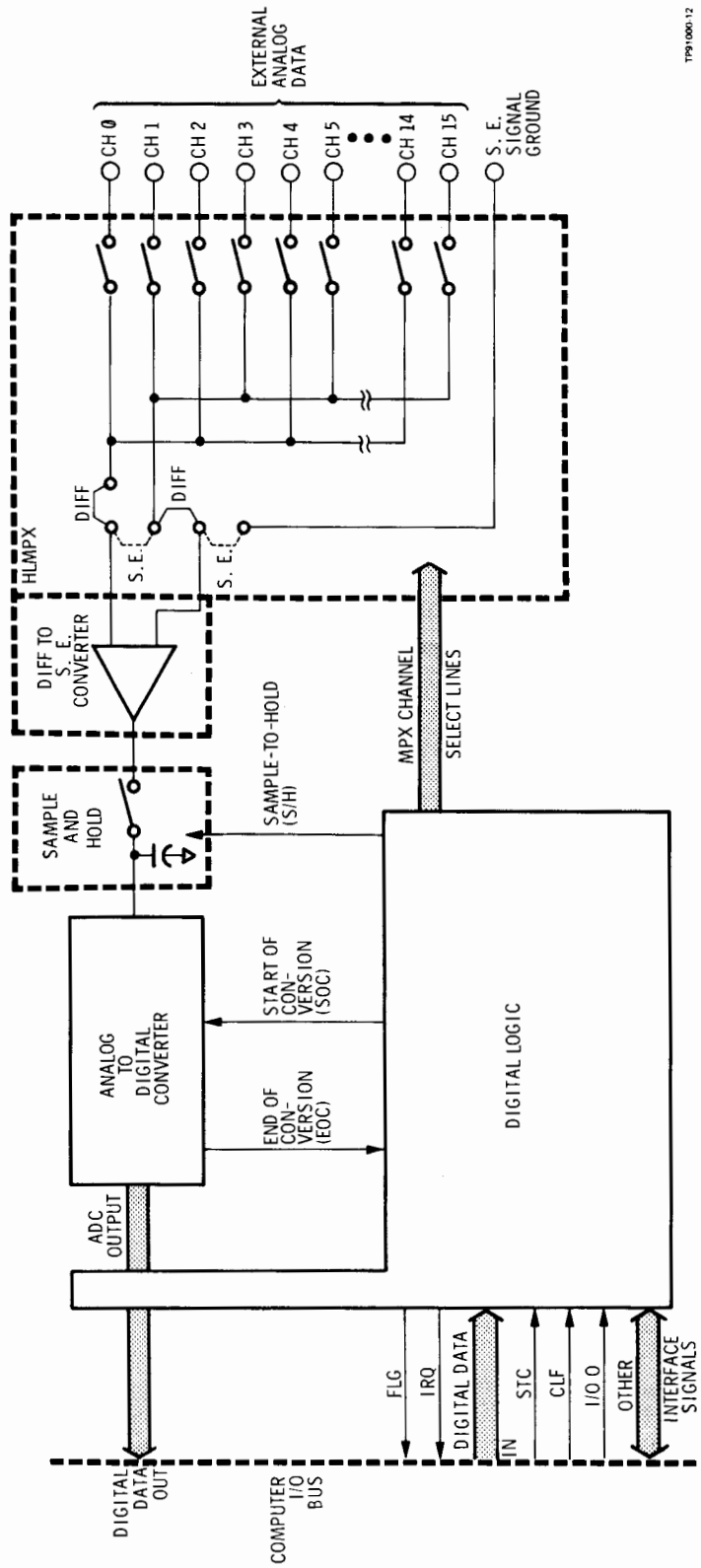


Figure 3-1. Simplified Block Diagram

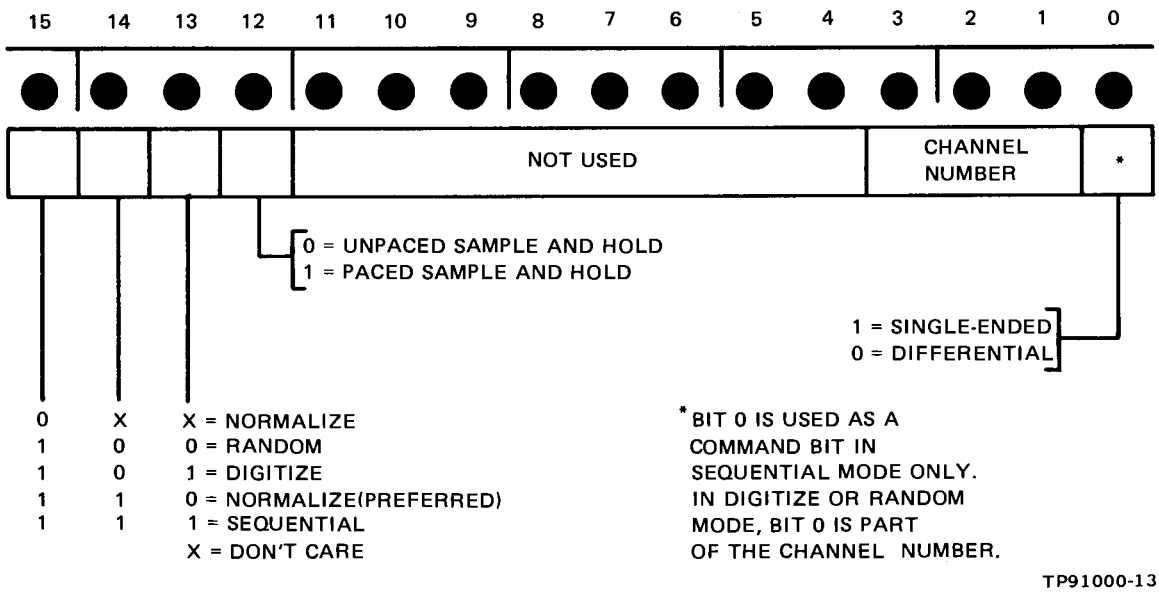


Figure 3-2. DAS Command Word Format

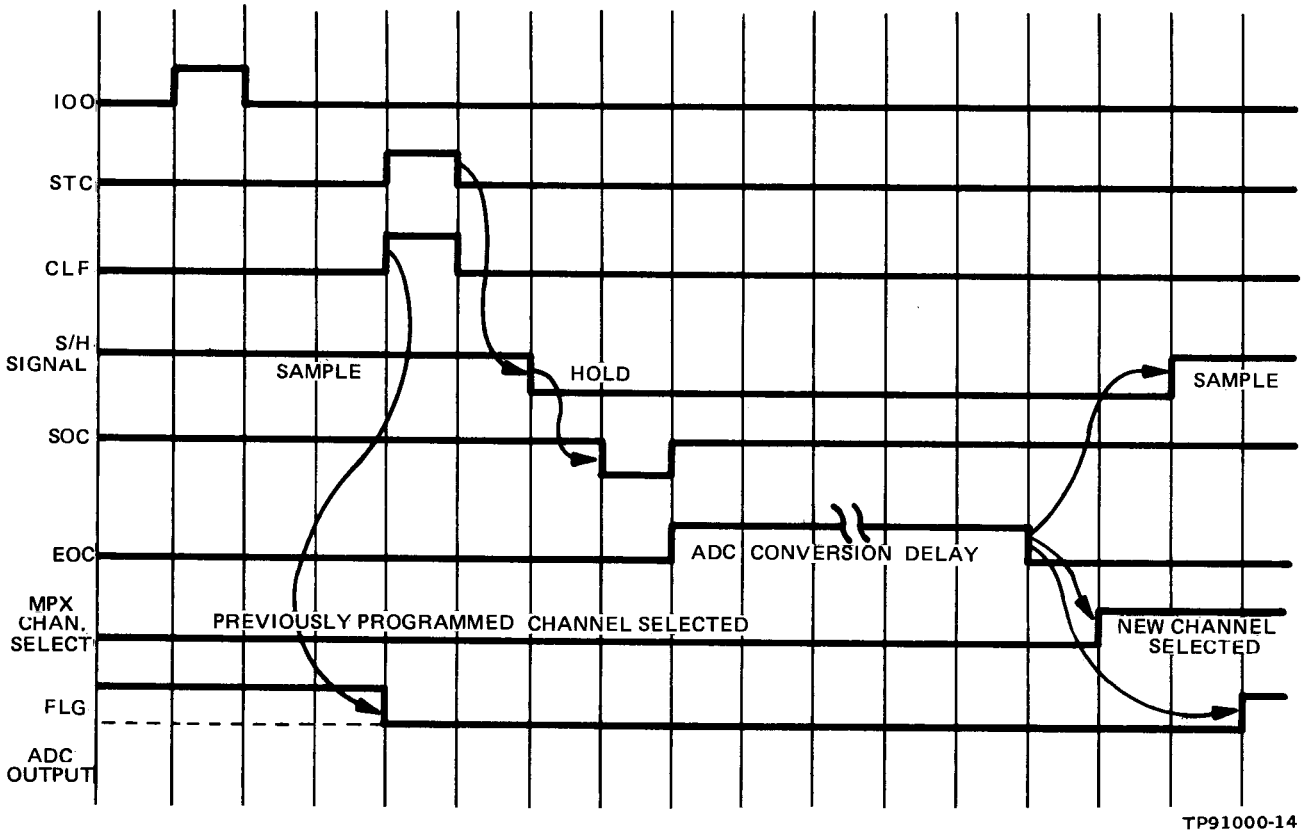


Figure 3-3. Simplified Timing Diagram, Digitize Mode

signals. This causes the DAS to latch the command word and reset the flag and interrupt lines, indicating that the DAS is busy. The DAS then sets the Sample-and-Hold (S/H) amplifier to hold and generates a start of conversion (SOC) pulse to the Analog-to-Digital Converter (ADC). While the ADC is converting, it sets the End-of-Conversion (EOC) signal high to indicate it is busy. When the ADC has finished, EOC goes low. This causes three events:

a. The S/H amplifier returns to sample.
b. The channel multiplexer is enabled to the currently programmed channel and a delay one-shot is fired to prevent the next data acquisition from occurring until the multiplexer and S/H amplifier have had time to settle on the new channel.
c. The flag and interrupt lines are set, announcing completion of the programmed operation. The program may now access the digitized data by executing an LIA or LIB instruction.

3-13. Since the multiplexer is not set to the programmed channel until after the S/H amplifier goes to hold, the data returned from the first digitize command is unknown. The next digitize command returns data corresponding to the channel programmed in the first command. In general, the data returned by a digitize command corresponds to the channel address programmed in the previous digitize command. This approach allows the multiplexer and S/H amplifier settling time to go in parallel with the computer overhead, allowing a higher throughput rate.

3-14. SEQUENTIAL MODE–Sequential mode timing is identical to that of the Digitize mode. Instead of latching in a new channel address each time, however, the sequential command results in the channel address already set in the DAS being incremented by one (single-ended) or two (differential). For proper operation, the DAS must first be programmed with a digitize mode command to set the starting channel address before being programmed for sequential mode.

3-15. The DAS has a channel reset capability in Sequential mode. This allows a continuous sequential scan of the DAS where sequencing is automatically reset to a programmed starting channel after the last channel on the DAS is measured. For instructions on the use of this feature, refer to the operating and programming manual.

3-16. RANDOM MODE–Random mode is essentially the same as programming the digitize command twice. The timing sequence of Figure 3-3 is executed once, as shown, to set the DAS to the programmed channel. No flag is returned at this point, however, and the entire sequence is repeated to actually measure the selected analog signal. Thus, the data returned with a Random mode command corresponds to the same channel programmed. Although from a programming stand point this mode is easier to use, it is slower than digitize or sequential mode commands.

3-17. NORMALIZE MODE

3-18. The second basic mode of operation is normalize mode. There are eight possible combinations of control bits 15, 14, 13 of the DAS command word. Only three are used for multiplex modes. The remaining five are considered normalize commands, but the bit pattern with bits 15, 14, 13 = 110 is the preferred normalize command. The DAS command word is compatible with an upgraded HP Data Acquisition Subsystem which uses the bit pattern 110 as the normalize command (bit 0 must also be 1). For consistency and for ease of later upgrading to this subsystem, it is recommended that this bit pattern be used for the normalize command. The purpose of the command is to put the DAS into a known starting condition so that multiplex operations can start from a defined initial state.

3-19. PACED MEASUREMENTS

3-20. In the absence of an external pacing pulse, the DAS will take measurements at a rate determined by the computer program, up to the maximum rate allowed by the hardware. Using software alone, it is not possible to achieve an exact scan rate or exact synchronization with some external signal. The DAS card allows these capabilities by accommodating an external pacing signal. When properly programmed, the pacing signal will determine the scan rate and provide synchronization of the data acquisition (sample-to-hold transition) with external events.

3-21. The pace pulse must have a cyclic rate slower than the normal computer program cycle. For example, the throughput may be software-limited and require perhaps 80 microseconds between data acquisitions, whereas the DAS card can execute an acquisition in 50 microseconds. In addition, the software time may contain a time jitter, in that there is no absolute certainty how much time the software requires - 80, 82, or 79 microseconds, for example - to tell the DAS card to perform its function. If the pacer is running slower than 82 microseconds, if that is the longest time the software may take, then the entire system will synchronize to the pacer. Now the jitter becomes a function only of the DAS card aperture time and the time jitter of the pacer pulse; the latter can be reduced to any arbitrarily small amount as a function of pacer accuracy. In DMA mode, the acquisition cycle is limited by the DAS card throughput time which, as noted above, is 50 microseconds.

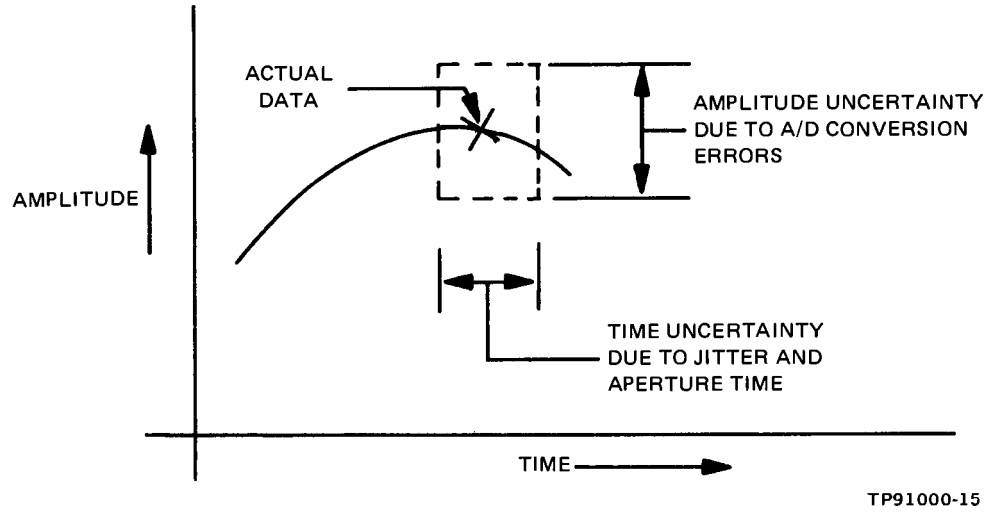


Figure 3-4. Data Uncertainties Due to Jitter, Aperture, and Conversion Errors

3-22. Figure 3-4 shows the two types of data acquisition errors, one a time uncertainty due to software or pacer jitter and aperture time, the other an amplitude uncertainty due to analog-to-digital conversion errors. The pacer reduces the time uncertainty to the DAS aperture time, but of course does not affect the amplitude uncertainty.

3-23. The DAS aperture time is the uncertainty of the sample-to-hold transition time in relation to the pace pulse time. If exact synchronization to an external event is required, the DAS delay time must also be considered. Figure 3-5 shows the relationship of the sample-to-hold transition to the pace pulse trailing edge. There is a delay of 150 nanoseconds and an uncertainty of 250 nanoseconds.

3-24. CIRCUIT ANALYSIS

3-25. GENERAL

3-26. The remainder of this section is devoted to a detailed circuit analysis of the DAS card. The DAS circuits can be partitioned into two major categories, analog and digital. The following paragraphs describe each of these categories. Refer to the schematic diagram, Figure 4-9.

3-27. ANALOG CIRCUITS

3-28. GENERAL—The analog circuits, shown on sheet 2 of the schematic, perform the actual sampling of the analog input data from the external world, converting the data from analog to 12-bit parallel digital. The circuits, capable of accommodating 16 single-ended or eight differential channels, can be partitioned into four functions (Figure 3-1):

- High-level multiplexer
- Differential-to-single-ended converter
- Sample-and-hold amplifier
- Analog-to-digital converter

The following paragraphs describe each of these functions.

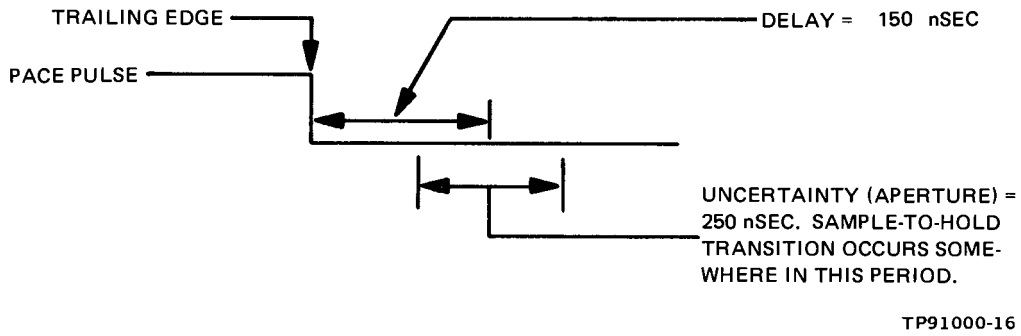


Figure 3-5. Aperture Time

3-29. HIGH-LEVEL MULTIPLEXER–The high-level multiplexer consists of clamp diodes CR1 through CR32, CR40, CR41, and analog switches Q1 through Q8. Two clamp diodes limit the excursion of each analog input to approximately ±12 volts to protect analog switches Q1 through Q8; even-numbered diodes CR2 through CR32 limit the positive excursion to +12 volts, while odd-numbered diodes CR1 thorugh CR31 limit the negative excursion to -12 volts. Zener diodes CR39 and CR38 establish the positive and negative clamping levels, respectively.

3-30. Eight identical analog switching devices, Q1-Q8, connect a particular analog signal to voltage followers U1 and U2. Each device contains two identical logic-controlled semiconductor switches, one switch between terminals 5 and 4, controlled by a logic signal on terminal 2, the other switch between terminals 8 and 9, controlled by a logic signal on terminal 1. When the logic input on terminal 2, for example, is high terminals 5 and 4 are open; when the logic input on terminal 2 is low terminals 5 and 4 are connected together by a semiconductor switch.

3-31. The analog switches can accommodate 16 single-ended or eight differential channels. In the differential configuration, the incoming differential signals must be connected between an even-numbered input and the next higher odd-numbered input; for example, between channels 0 and 1 or between 8 and 9, the lower-numbered channel being the non-inverting input (more positive). In addition, jumpers shown on the schematic near gates U105C and U105B, must be connected in the differential configuration, as shown in Figure 2-1. This configuration insures that two adjacent channels, one even and one odd, are addressed simultaneously. Also, the jumpers at the inputs to voltage followers U1 and U2 must be connected as indicated on the schematic and in Figure 2-1.

3-32. In the single-ended mode, one and only one logic input (address) to the analog switches is low at a given time, so that only one of the 16 analog inputs is connected to voltage follower U1. The jumpers between Q1-Q8 and U1, U2 are connected as shown by the dotted lines on the schematic. In this configuration, all 16 outputs from Q1-Q8 are routed to voltage follower U1, and ground is connected to the input of voltage follower U2.

3-33. DIFFERENTIAL-TO-SINGLE-ENDED CONVERTER–Voltage followers U1 and U2, in conjunction with operational amplifier U3, make up a unity-gain differential-to-single-ended converter which buffers the analog signal voltage to eliminate ground loops, rejects common-mode noise, provides a high impedance to the source, and a low output impedance to operational amplifier U4.

3-34. SAMPLE-AND-HOLD AMPLIFIER–The sample-and-hold amplifier consists of operational amplifier U4, shunt switch Q9, series switch Q10, storage capacitor C3, and differential switch Q11.

3-35. Operational amplifier U4 is configured as an inverting amplifier, with resistors R47 and R48 serving as R_{in} and R_f respectively. Shunt switch Q9 is an NPN transistor connected as an inverted transistor switch. When its base is positive it is turned on; when its base is negative, it is turned off. Series switch Q10 is a dual-junction field-effect transistor. Q10A actually acts as the switch, while Q10B balances the charge transfer which occurs at the input of U4 due to the switch transition. Q10A is normally on (closed) with approximately zero gate voltage, and is turned off (opened) with a negative gate voltage.

3-36. In the sample state, the S/H signal from S/H flip-flop U72B-8 is high, Q11-B is on, and Q11-A is off. The negative collector voltage at Q11-A turns off Q9, while the slightly positive collector voltage of Q11-B turns on Q10-A. The analog voltage is now connected to U4, which charges storage capacitor C3 to the value of the analog input voltage.

3-37. In the hold state, the S/H signal from U72B-8 is low, Q11-B is off, and Q11-A is on. The slightly positive collector voltage of Q11-A turns on Q9, grounding the analog voltage, while the negative collector voltage of Q11-B turns off Q10-A, isolating the charge on C3. U4 now applies whatever voltage is on C3 to the analog-to-digital converter.

3-38. When the S/H signal from U72B-8 goes high the sample-and-hold circuit reverts to the sample condition. However, approximately 26 microseconds must elapse before the sample-and-hold will be ready to go to hold again, due to the time required for settling and stabilization.

3-39. ANALOG-TO-DIGITAL CONVERTER–Figure 3-6 is representative of the internal configuration of a typical analog-to-digital converter (ADC). The ADC is a successive approximation device that converts the analog voltage input to it by U4 to a 12-bit parallel binary word in two's complement format. The conversion employs a 12-step comparison procedure in which the unknown input is compared to a series of quantized reference currents or voltages. The digital data resulting from this comparison becomes the ADC output.

3-40. The start-of-conversion signal (SOC) is a positive-going pulse with a width of 300 nanoseconds. This pulse causes the ADC to start its conversion; depending

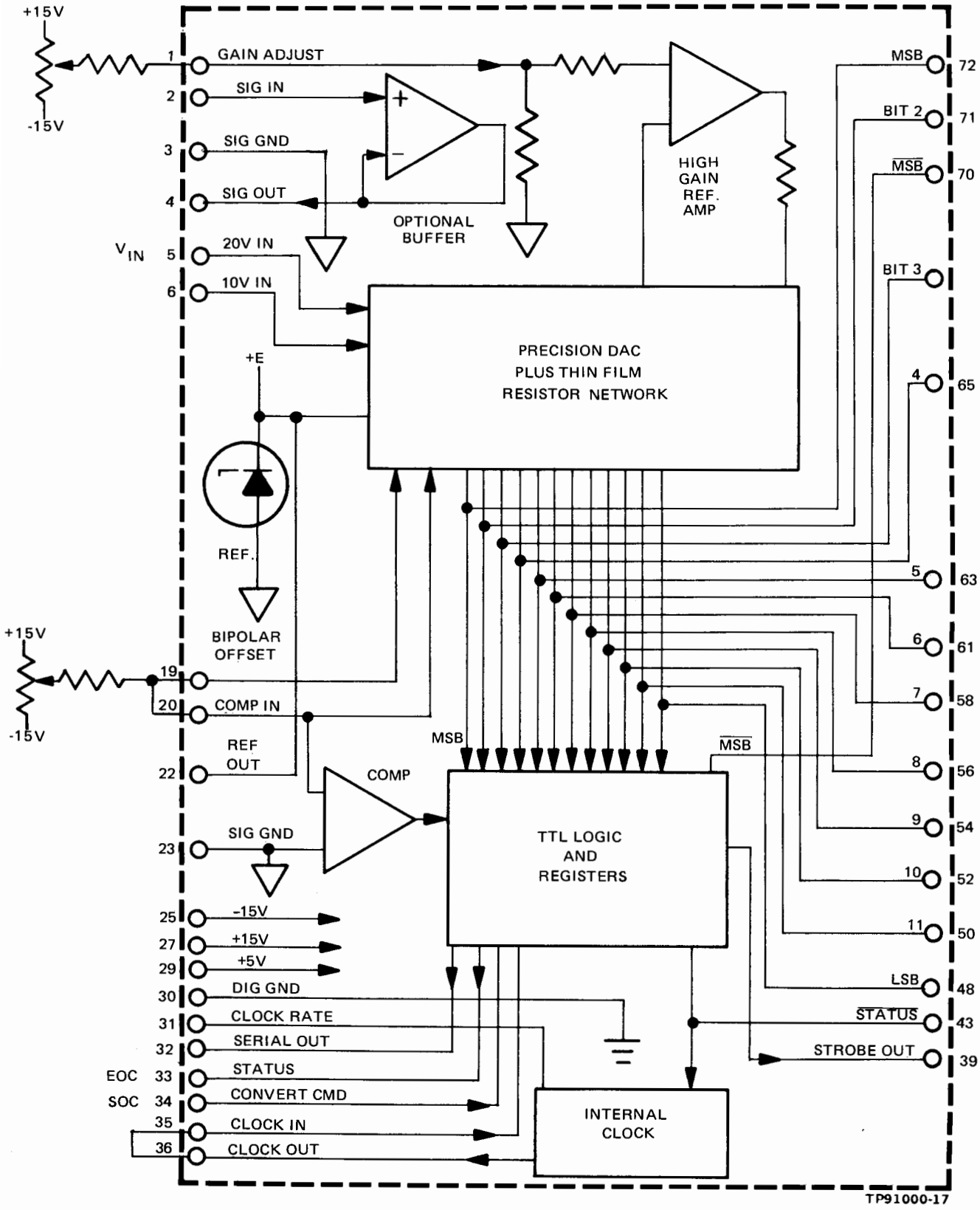


Figure 3-6. Typical ADC Internal Configuration

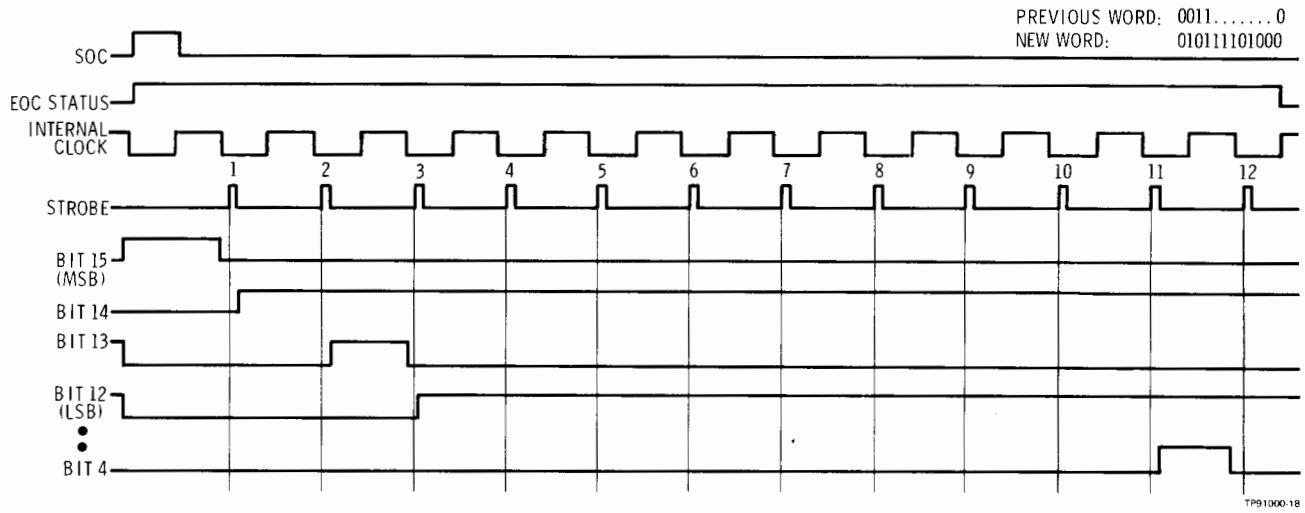


Figure 3-7. ADC Timing

upon the particular ADC, EOC may go high on either edge of SOC. When the ADC has finished its conversion and its output is valid, it will set EOC low.

3-41. The following description of the operation of a typical ADC is included to give a better understanding of the internal operation of the ADC and will not necessarily apply exactly to all ADC's used on the DAS card.

3-42. Figure 3-7 shows a typical timing sequence. The leading edge (low-to-high transition) of the SOC signal sets the EOC (status) and MSB outputs high, and bits 4 through 14 low. The conversion program begins on the trailing edge of the SOC signal with the starting of the internal clock. Bit decisions are made on successive high-to-low clock pulse transitions, with the MSB decision occurring first. At the completion of the conversion, the end-of-conversion (EOC) output goes low, signaling that the output data is valid.

3-43. Table 3-1 lists the two's complement output for various values of input voltage between +10.235 and -10.240 volts. Analog resolution is 5 millivolts per bit.

Table 3-1. Binary Output As a Function of Analog Input

Analog Input	2's Complement
+10.235	011111111111
+ 7.678	011000000000
+ 5.120	010000000000
+ 2.560	001000000000
0	000000000000
- 2.560	111000000000
- 5.120	110000000000
- 7.678	101000000000
-10.240	100000000000

3-44. DIGITAL CIRCUITS

3-45. GENERAL—The digital portion of the DAS contains two functions, the interface logic and the control logic. The interface logic contains an address latch, a mode latch, and flag and interrupt logic. The address latch stores four address bits which define the address, or channel, of the external analog data that is to be acquired. The mode latch stores four mode bits which define the mode of operation: sequential, random, digitize, or normalize. The flag and interrupt logic generates various internal commands from instructions supplied by the computer; two examples are a load command which dumps address and mode data into the address and mode latches, and a start command which starts a data acquisition. In addition, the flag and interrupt logic generates signals such as FLAG, interrupt request (IRQ)and priority low (PRL), which tell the computer what the DAS is doing.

3-46. The control logic section contains a mode decoder, an address counter, channel select logic, sample/hold logic, clock logic, and a state generator.

3-47. The mode decoder examines bits B13, B14, and B15 of the computer mode command, and determines which mode of operation the program wants: sequential, random,normalize, or digitize.

3-48. The address counter logic contains a counter which can be preset to the address contained in the address latch (Digitize and Random Modes) or can increment its current contents (Sequential Mode).

3-49. The channel select logic contains a one-of-sixteen decoder which is used to turn on the appropriate MPX switch (single-ended) or pair of switches (differential) in response to the address in the address counter.

3-50. The sample-and-hold logic controls the state of the sample-and-hold amplifier. Based on the state of its input signals it causes the S/H amplifier to switch to hold or to sample. It can also use an external pacing pulse to determine the sample-to-hold transition's timing.

3-51. The clock logic and state generator produce the control pulses and state signals which are routed to the other logic blocks. These signals cause the other blocks to perform their prescribed tasks.

3-52. The clock logic generates a burst of three clock pulses, CLK 1, CLK 2, and CLK 3. CLK 1, CLK 2, and CLK 3 occur in groups, five groups per acquisition cycle, as shown in Figure 3-8. In Random mode the cycle is repeated, resulting in ten groups. These pulses sequence the DAS through the various operations required for a data acquisition.

3-53. The state generator counts the CLK 3 pulses, directing the sequencing according to the number of CLK 3 pulses that have occurred. On the trailing edge of the last CLK 3 pulse, the state generator returns to its rest condition, state S0, and terminates the data acquisition cycle. The outputs of the state generator are combined with the CLK 2 pulses to enable the operation of the other logic blocks.

3-54. Paragraph 3-55 is devoted to a discussion of the digital signals input to and output from the DAS. Paragraphs 3-56 through 3-98 present a detailed circuit analysis of the digital logic, which can be partitioned into two major functions: interface logic and control logic. Unless otherwise noted, the following conventions are used:

a. Logic symbols are in accordance with MIL-STD-806B.
b. Logic levels are low (less than 0.8 volt) or high (greater than 2.0 volts).
c. A flip-flop is referred to as set when its Q output is high and its $\overline{Q}$ output is low; conversely, a flip-flop is referred to as reset when its Q output is low and its $\overline{Q}$ output is high.
d. Similarly, when a one-shot is fired, its $\overline{Q}$ output goes high and its Q output goes low for the duration of the one-shot's timing cycle.

3-55. Input and Output Signals–Table 3-2 defines the I/O signals of the DAS card. Figure 3-9 shows the timing relationships of some important computer control signals.

3-56. INTERFACE LOGIC–The interface logic performs three functions:

- Initialization
- Storage of computer command word
- Flag and interrupt control

3-57. Initialization–The DAS card must be in a defined initial condition before a data acquisition can be started. This initial condition is brought about in the following manner.

3-58. At the time of power turn-on, the positive-going power-on preset (POPI/O) signal sets flag buffer flip-flop U76A/U86C and presets normalize flip-flop U106A. Flag buffer flip-flop U76A/U86C enables input 5 of gate U107B. Input 4 of U107B goes high at computer time T2, when computer command signal ENF(T2) goes high. U107B-6 therefore goes low, setting flag flip-flop U97C/U107C.

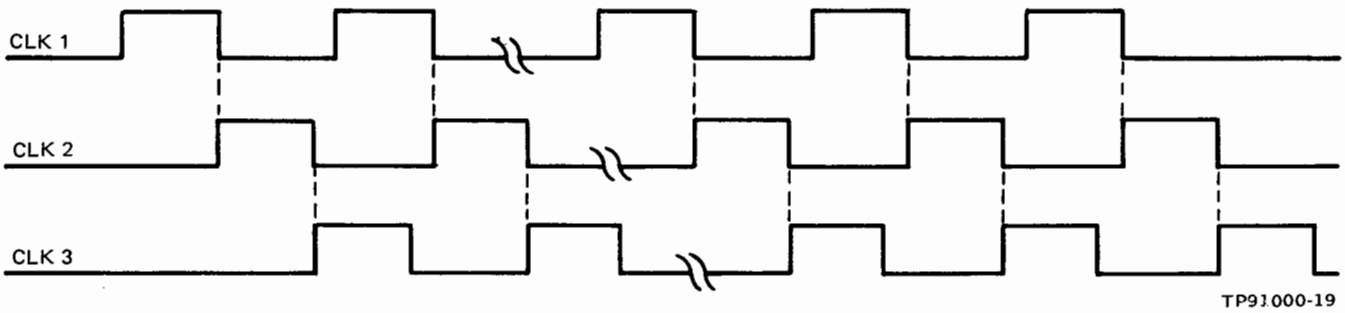


Figure 3-8. Clock Pulse Configuration

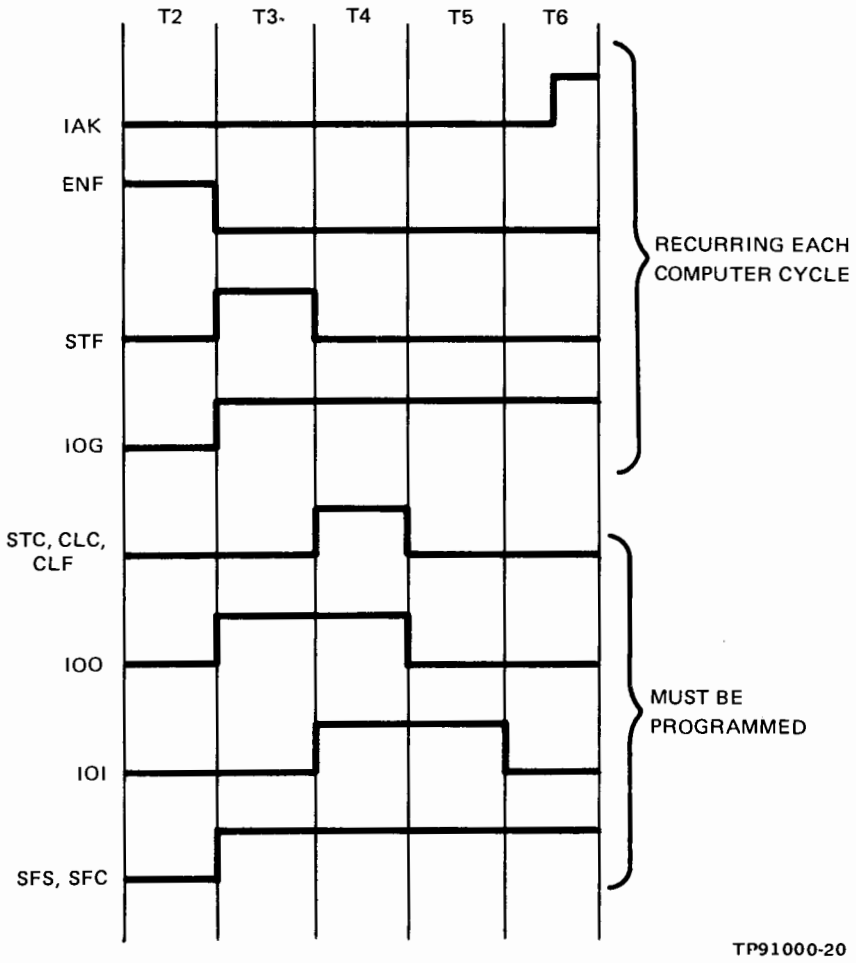


Figure 3-9. Command Inputs from HP2100 Computer

Table 3-2. Input and Output Signals*

Mnemonic	Signal	Description
SCM	Select code, most significant digit	The SCM, SCL, and IOG(B) signal combination determines the slot connector to which the instruction portion of the computer I/O command word is directed. When the DAS card is selected, all three signals will be high.
SLC	Select code, least significant digit	
IOG(B)	I/O group instruction	
IOBO 0, IOBO 1, IOBO 2, etc.	8-Bit parallel control command	Bits IOBO 15, IOBO 14, and IOBO 13 define the mode of operation: random, digitize, normalize or sequential, as listed below.

Table 3-2. Input and Output Signals* (Continued)

Mnemonic	Signal	Description
		Bit 15 / Bit 14 / Bit 13 / Mode High / Low / Low / Random High / Low / High / Digitize High / High / Low / Normalize High / High / High / Sequential Low / X / X / Normalize (X = don't care) Bit 12 defines paced or unpaced operation: High = paced (wait for pace pulse) Low = unpaced Bits 3 through 0 define the address of the external analog input data. In the digitize and random modes, the address bits must change (i.e., a new control word must be programmed) in order to change channels. In the sequential mode, the control word contains the starting address only; the DAS automatically sequences through the remaining addresses and returns to the starting address.
SIR(T5)	Set interrupt request	Positive pulse that occurs at computer time T5. If other interrupt prerequisites are met, sets interrupt request flip-flop to initiate interrupt.
IOBI 4 through IOBI 15	Response bits 4 through 15	Twelve-bit parallel binary output in two's complement format, representing digital equivalent of analog input data.
Pacer	External pace pulse	Precisely timed pulse from external pacer. If used, reduces timing errors due to software jitter. Refer to paragraph 3-19.
STF	Set flag	Sets DAS flag high.
IOO	I/O output operation	Strobes computer command word into DAS.
IOI	I/O input operation	Commands DAS card to output its acquired data onto computer bus.
FLG	Flag	Output from DAS card to computer. When FLG is low, indicates DAS is busy. When high, indicates DAS has completed assigned operation and is ready to transfer acquired data to computer.
CLF	Clear flag	Clears DAS flag (sets flag low).

Table 3-2. Input and Output Signals* (Continued)

Mnemonic	Signal	Description
SFS	Skip if flag set	Generated by SFS computer instruction. Used to determine if DAS flag is set.
SFC	Skip if flag clear	Generated by SFC computer instruction. Used to determine if DAS flag is cleared.
IEN	Interrupt enable	High when the computer interrupt system is on, low when it is off. Must be high if an interrupt is to occur.
POPI/O	Power-on preset	Initialization command which presets DAS card to known starting condition when power is applied to computer.
STC	Set control FF	Initiates data acquisition cycle in DAS card.
CLC	Clear control bit	Clears the control flip-flop upon execution of the CLC instruction.
CRS	Control reset	Generated by manual preset button on computer front panel. Same effect as CLC signal.
ENF(T2)	Enable flag	Positive pulse at computer time T2. Clears interrupt request flip-flop and permits flag flip-flop to be set.
IAK	Interrupt acknowledge	After detecting an interrupt, the computer responds with IAK which clears the flag buffer flip-flop, preventing setting of the interrupt request flip-flop and causing another interrupt from the same flag signal.
T3	Computer time T3	Permits computer command word (see IOBO 0, IOBO 1, etc.) to enter DAS card.
SKF	Skip	The SKF signal is generated by a programmed SFS (skip if flag set) or SFC (skip if flag clear) instruction with the select code of the DAS card. If the DAS flag has been set to produce an interrupt request and an SFS instruction has been decoded by the computer's instruction decoder, then an SKF signal will be generated and sent back to the computer from the DAS. If an SFC instruction has been decoded with the DAS select code and the DAS flag has not been set, then an SKF signal will also be sent to the computer.
SRQ	Service request	Output of flag flip-flop used in DMA cycles only.
IRQ	Interrupt request	Output of flag flip-flop gated by the priority bus.
FLG	Flag	Same as IRQ

Table 3-2. Input and Output Signals* (Continued)

Mnemonic	Signal	Description
PRH	Priority high	If high, indicates that no device of higher priority is requesting an interrupt. A service subroutine of any device can be interrupted by a higher priority device; then, after the higher priority interrupt subroutine is completed, the lower priority subroutine may continue.
PRL	Priority low	If low, prevents any interface card of lower priority from interrupting computer program.
+E	Nominal +4.85	Internally generated on DAS card. Used as fixed logic high-level bias.

*For a more complete discussion, refer to Appendix A of HP Document 5950-8718, "A Pocket Guide to Interfacing HP Computers", and to Section III of Installation and Maintenance Manual for HP 2100A computer.

3-59. Computer command ENF(T2) also clears interrupt request (IRQ) flip-flop U107A/U97D, which in turn forces the flag (FLG) and interrupt request (IRQ) outputs low. Finally, ENF(T2) clears IOO delay flip-flop U85A, which places a low disable on input 9 of gate U84C.

3-60. To complete the initialization, the computer must issue a control reset (CRS) command. This signal is generated by pushing the EXTERNAL PRESET pushbutton on the computer. The high CRS signal resets control flip-flop U85B via inverter U87D and gate U96B.

3-61. Gates U86A and U86B test the condition of flag flip-flop U97C/U107C using computer SFS or SFC instructions; this is done to determine if the DAS card is ready for a new operation. The clear condition of control flip-flop U85B prevents the start of a data acquisition cycle.

3-62. Storage of Computer Command Word—Assume that the DAS card has been initialized as described above. Before the DAS card can begin a data acquisition cycle, it must be loaded with a command word. This occurs when the computer executes an output instruction (OTA or OTB) to the correct select code. The DAS command word is an 8-bit mode and address word which is made up of IOBO bits 0 through 3 and 12 through 15 of the 16-bit computer output word.

3-63. Two registers, U133 and U132, store the command word. Both registers are configured to operate as latches, each register latching four bits when the clock input (i.e., the output of gate U84C) goes high. The latching signal is generated in the manner shown in figure 3-10. During each computer cycle, IOO delay flip-flop U85A is set and reset. Assuming U85A is initially reset, it is set at the end of period T3 (see figure 3-9) by the negative-going edge of control signal T3. This edge is inverted by U74C and clocks and a high +E signal into U85A, thus enabling gate U84C. Flip-flop U85A is later reset by control signal ENF(T2), which goes high at computer time T2, via inverter U87F. The purpose of this circuit is to insure that gate U84C is disabled during T2 and T3 and that the command word can not be latched during this time. When an output instruction (OTA or OTB) is executed by the computer, control signal IOO is set high during time periods T3 and T4. This enables input 10 of gate U84C. Input 11 of gate U84C will still disable the gate, however, unless the select code of the DAS is programmed. In this case, control signals SCM, SCL, and IOG(B) will all be high, enabling gate U75B and setting input 11 of U84C high via inverter U74B. Thus, all inputs to gate U84C are high and its output goes low. With gate U84C enabled, the mode and address command is dumped into registers U133 and U132 at the end of computer time T4 when the computer I/O output (IOO) signal goes low, causing U84-8 to go high.

3-64. Flag and Interrupt Control—To start a data acquisition, the computer program must execute a set control, clear flag (STC,C) command. The set control instruction causes the STC control line to go high, setting control flip-flop U85B via gate U97B. The low output of U97B also acts as a START signal for the DAS control logic, to be described later. The clear flag instruction causes the CLF control line to go high, resetting the flag buffer flip-flop U76A/U86C and flag flip-flop U97C/U107C via gate U97A. No further action occurs in the flag and interrupt control logic until the DAS acquisition is complete (signaled by a low output of gate U104B), with the exception of flag tests.

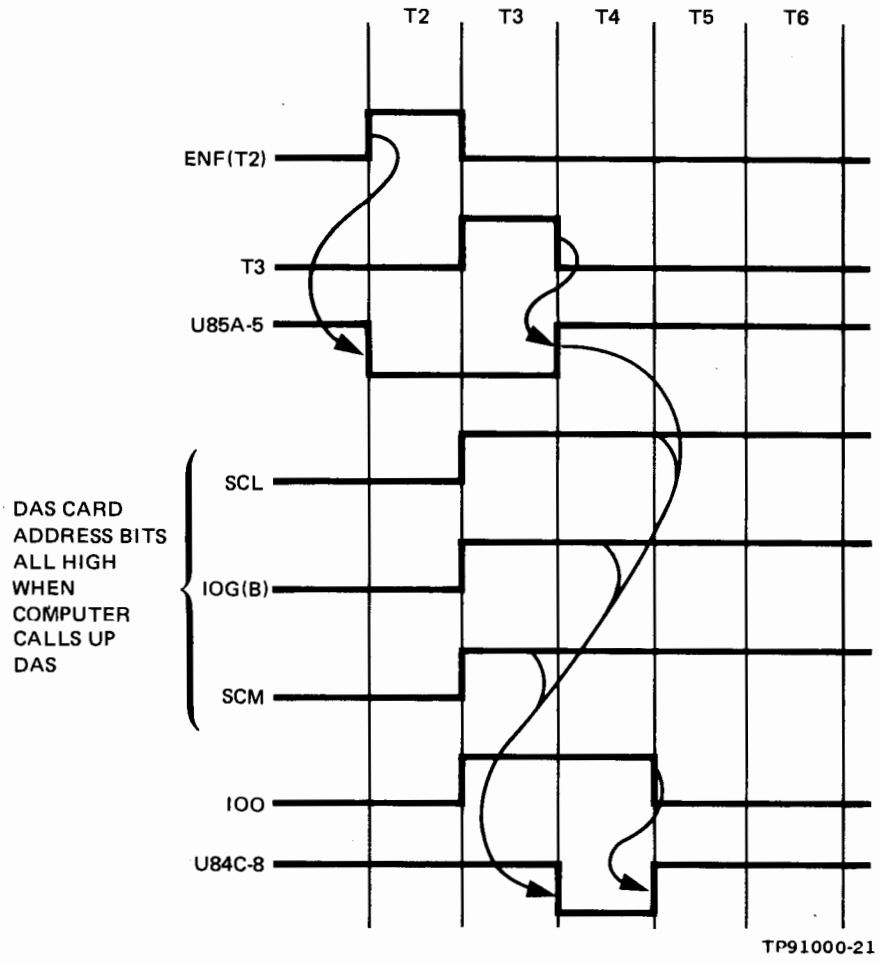


Figure 3-10. Storage of Computer Command Word

3-65. Flag Testing–At any time before or after the acquisition cycle is completed, the computer program may test the status of flag flip-flop U97C/U107C. When a SFS or SFC instruction is executed, the SFS or SFC control signal is set high, correspondingly, during time periods T3 through T6 (see figure 3-9). If the DAS card select code is programmed, control signals SCM, SCL, and IOG(B) will all be high, enabling gate U75B. The low output of U75B is inverted by U74B and applied to gates U86A and U86B. The above conditions are combined with the condition of flag flip-flop U97C/U107C and the test output SKF is set accordingly. For example, if the instruction SFS is executed to the DAS select code, the control signals SFS, SCM, SCL, and IOG(B) go high. This will cause inputs 13 and 2 of gate U86A to be enabled. If the flag flip-flop is set, U97-8 is high and enables the remaining input of gate U86A, causing its output to go low. This low output is inverted by gate U77B and its high output is coupled to the computer control line SKF by open-collector gate U65B. The computer will interpret this output as indicating that the flag flip-flop is set.

3-66. Flag Setting–When the acquisition cycle is complete, the output of gate U104B will go low (the sequence of operation between the START signal and the end of the acquisition cycle is described in the control logic section, paragraphs 3-73 through 3-98). This sets flag buffer flip-flop U76A/U86C. At the next T2 time period, control signal ENF(T2) goes high and is coupled with the output of the flag buffer flip-flop in gate U107B. This enables U107B and causes its output to go low, setting flag flip-flop U97C/U107C.

3-67. Interrupt Setting–To set interrupt request (IRQ) flip-flop U97D/U107A, gate U73B must first be enabled. Input 5 of gate U73B is enabled by a high from control flip-flop U85B, and input 3 is enabled by a high from flag flip-flop U97C/U107C. Input 4, however, is not enabled

unless the computer interrupt (IEN) signal is high. IEN is high if the computer interrupt system is turned on. If it is not, the IRQ flip-flop can not be set. If IEN is high, U73B places a high enable on input 12 of gate U76B via inverter U87A.

3-68. During computer time T5, the set interrupt request (SIR(T5)) signal is high, enabling input 10 of gate U76B. The priority high (PRH) signal will be high, enabling input 13 of gate U76B, unless a higher priority device is requesting service. Assuming that no higher priority device is requesting service, then all inputs to U76B are high, and U76B sets interrupt request flip-flop U97D/U107A. The output of U97D goes high, generating a high flag (FLG) signal via U64B and a high interrupt request (IRQ) signal via U64A. In addition, the low output from U73B drives the output of open-collector gate U66A low, generating a low priority (PRL) signal which prevents interrupts from all lower priority devices.

3-69. At the next computer time T2, ENF(T2) clears the IRQ flip-flop to allow any higher priority device to request service during the interrupt. If no higher priority device requests service, PRH remains high, and at time T5 the SIR(T5) signal sets the IRQ flip-flop a second time. The FLG and IRQ signals are then used to indicate the interrupt address.

3-70. The computer processes the IRQ signal, executes the instruction contained in memory at the interrupt address, and during computer time T6, returns a high interrupt acknowledge (IAK) signal to gate U94D, clearing flag buffer flip-flop U76A/U86C. Flag buffer flip-flop U76A/U86C disables gate U76B, preventing any further interrupts from the same flag signal. Flag flip-flop U97C/U107C remains set, however, to maintain the low PRL signal to lower priority devices until processing of the requested interrupt is complete. To enable lower priority devices, a clear flag (CLF) or clear control (CLC) instruction must be programmed.

3-71. CONTROL LOGIC–The control logic sequences the high-level multiplexer, sample-and-hold amplifier, and analog-to-digital converter through a data acquisition according to instructions contained in the computer command word.

3-72. The principal components of the control logic are normalize flip-flop U106A, mode decoder U123, status flip-flop U72A, HLMPX inhibit flip-flop U106B, S/H flip-flop U72B, S/H delay one-shot U124A, CLK 1 one-shot U134, CLK 2 one-shot U114A, CLK 3 one-shot U114B, 4-bit shift register U83, address counter U122, address latch U112, and address decoders U102 and U92. The remaining circuitry consists of gates which sequence the above components at appropriate times during the data acquisition.

3-73. Figure 3-2 shows the format of the command word, which defines the operation to be performed by the DAS.

3-74. Normalize Mode–When a normalize mode command is programmed either input 9 or input 10 of gate U95C is low, causing its output to go high and setting a high level at the D input of normalize flip-flop U106A. When the START (STC) signal goes low to initiate a DAS operation (see paragraph 3-64), it is inverted by U74D and clocks the high D input into flip-flop U106A, causing its $\overline{Q}$ output to go low.

3-75. Normalize flip-flop U106A, when preset as described above or when preset by POP I/O as described in paragraph 3-58, drives the output of gate U96A low. U96A clears HLMPX inhibit flip-flop U106B and status flip-flop U72A, resets four-bit shift register U83 (all outputs low), and clears S/H flip-flop U72B via gate U82A.

3-76. The START command is also input to the clock logic via U104-4. When the DAS card is not executing any command, all inputs to gate U104A are high, causing its output to be low. When the control signal STC causes START to go low, U104-6 goes high. At the end of the STC signal, START returns high, causing the output of U104A to go low. This negative edge fires CLK 1 one-shot U134. The trailing edge of the CLK 1 pulse fires CLK2 one-shot U114A. Because normalize flip-flop U106A is inhibiting circuit operation, this 310 nanosecond pulse does nothing but fire CLK 3 one-shot U114B on the trailing edge. One-shot U114B outputs a positive-going 310 nanosecond pulse at pin 10. This positive pulse enables input 10 of cycle complete gate U104B. Input 9 of U104B is high at this time because normalize flip-flop U106A is holding Status flip-flop U72A clear. Normalize flip-flop U106A, via gates U96A and U95A, holds input 12 of U104B high. The last input to U104B is held high by flag flip-flop U97C/U107C which was reset by the control signal CLF. Cycle complete gate U104B is thus enabled causing its output to go low and set flag buffer flip-flop U76A/U86C. From this point on, operation continues as described in paragraph 3-66.

3-77. It should be noted that the START signal is coupled through gate U96A to the NORM line. Thus, whenever any operation is programmed, the START signal resets all circuits as described in paragraph 3-75. This insures that all operations begin from a known starting point.

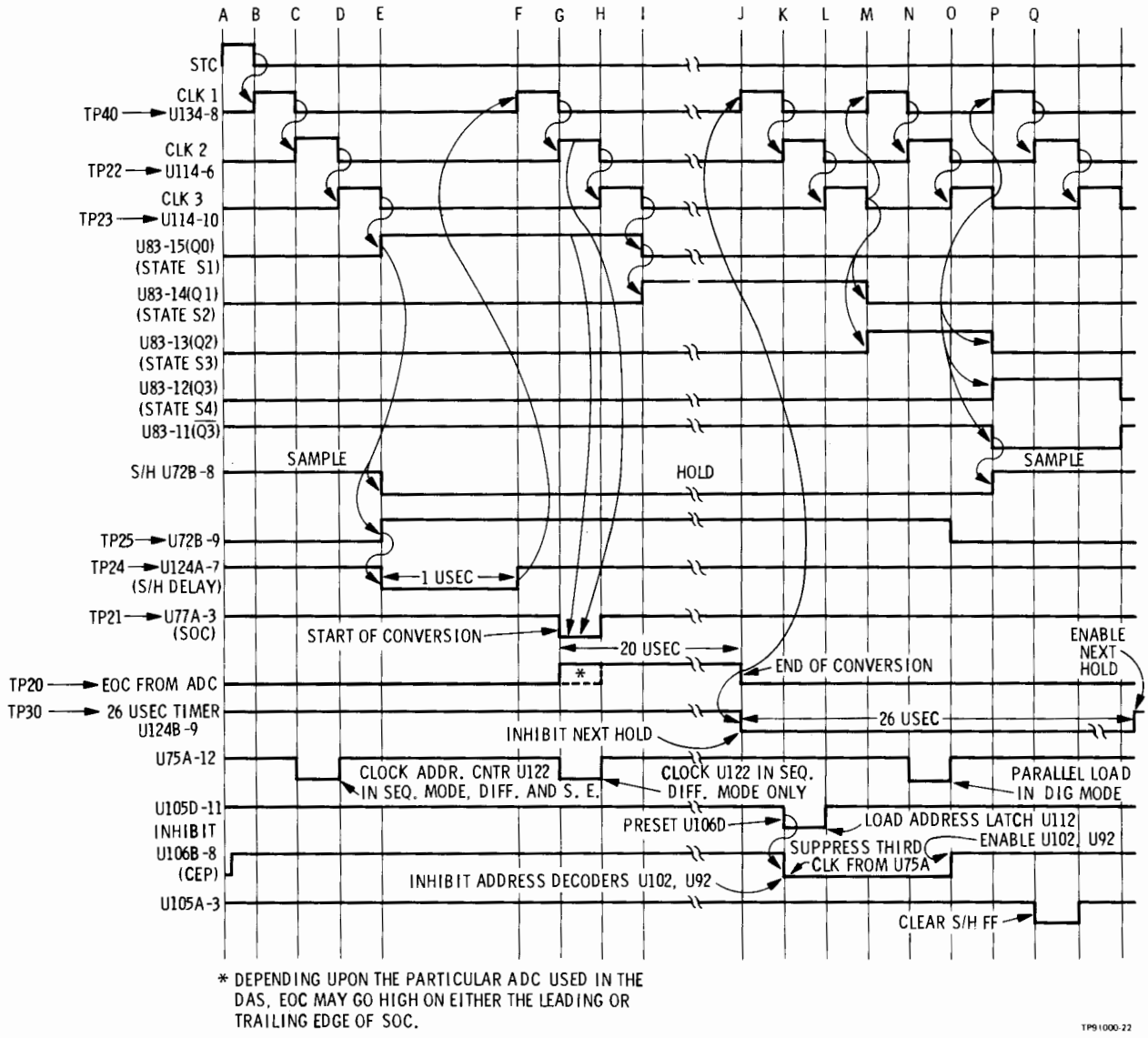


Figure 3-11. Timing Relationships, Sequential and Digitize Modes, Unpaced

3-78. Multiplex Modes—Refer to paragraph 3-9 for a summary of the multiplex modes: random, digitize, and sequential. The sequential mode circuit operation will be described in detail because it covers nearly all the circuit operation used in the random and digitize modes. The differences in random and digitize will then be presented.

3-79. Sequential Mode Operation—Figure 3-11 shows the key timing relationships for the sequential mode. Note that, along the top edge of the illustration, specific times are identified as A,B,C, and so on, for convenience in referencing. It is assumed that the DAS card has previously been set to some desired starting address by a digitize command

3-80. At time A, computer set control signal STC goes high, causing control signal START to go low and initialize the logic as described in paragraph 3-77. At time B, STC goes low, causing START to go high. This fires CLK 1 one-shot U134 via gate U104A. At time C the trailing edge of the pulse from U134 fires CLK 2 one-shot U114A. At this point, state generator U83 is in state 0, that is, S1, S2, S3, and S4 are all low. This condition (S0) is decoded by gate U103A, causing its output, U103-6, to go low. Signal S0 is

coupled through gate U75C and applied to inputs 1 and 2 of U75A. This signal, combined with the positive pulse output of CLK 2 one-shot U114A, enables gate U75A, which applies a low signal to the clock input (CP) of address counter U112.

3-81. At time D, U114A completes its pulse and its output goes low. This negative-going transition drives the output of gate U75A high, clocking address counter U122.

NOTE

Address counter U122 operates in the following manner:

1. To count (increment), the CET, $\overline{PE}$, and CEP inputs must be high at the time the CP input goes high.
2. To preset (parallel load B3, B2, B1, and B0), the $\overline{PE}$ input must be low at the time CP goes high.

3-82. At this time, the other inputs to U122 are as follows:

a. The CEP input is high because HLMPX Inhibit flip-flop U106B is initially reset.
b. In sequential mode, output 5 of mode decoder U123 is low, applying a high input to gate U96D-12. The other input to U96D is also high at this time, enabling the gate and causing $\overline{PE}$ to be high.
c. State signal S1 is low at this time, causing the CET input of U122 to be high via U95B.

Thus the CP input from U75A causes the address counter to increment its contents.

3-83. Simultaneously, CLK 2 one-shot U114A fires CLK 3 one-shot U114B. At time E, the trailing edge of CLK 3 clocks shift register U83. The Q0 output of U83 goes high, indicating state S1.

NOTE

Four-bit shift register U83 is configured as a standard D-input register by connecting the J and $\overline{K}$ inputs together. In this configuration, if the master reset ($\overline{MR}$) input is high, the signal that is present on the J and $\overline{K}$ inputs propagates into the Q0 stage and then progresses toward the Q3 stage, one stage at a time, each time the clock pulse (CP) goes high. A low master reset ($\overline{MR}$) sets all Q outputs low and the Q3 output high.

84. At this point it is assumed that MPX delay one-shot U124B (fired during a previous operation) is not active. Thus, the high S1 signal enables gate U82D, setting input 9 of gate U77C high. Further activity depends upon bit B12 of the computer command word. If B12 is low, for unpaced operation, gate U77D enables gate U77C. U77C presets sample/hold flip-flop U72B, initiating a hold on the analog input data. If B12 is high, for paced operation, gate U77D disables gate U77C, while inverter U113C enables gate U73C. The DAS now waits for a pace pulse, at which time gate U73C clocks sample/hold flip-flop U72B, initiating a hold on the analog input data.

NOTE

The pace pulse is an active high pulse having a duration of 1.5 ±0.5 microsecond. In the pace mode, S/H will go to hold on the trailing edge of the pace pulse, as shown in Figure 3-12.

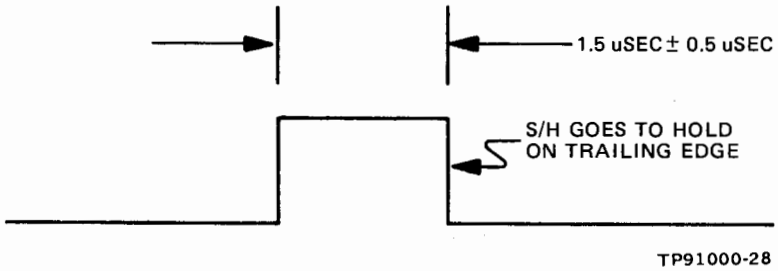


Figure 3-12. Pace Pulse

3-85. Also at time E, S/H flip-flop U72B fires S/H delay one-shot U124A, which begins a one-microsecond delay. The purpose of this delay is to give the sample/hold circuitry sufficient time to settle before analog-to-digital conversion begins.

3-86. At time F, the end of the one-microsecond delay, U124A-7 goes high and fires CKL 1 one-shot U134 via gate U104A. U134 in turn fires CLK 2 one-shot U114A at time G. During CLK 2, both inputs of gate U77A are high, driving the output low; this transition tells the analog-to-digital converter to convert whatever data is available at its input. The conversion requires approximately 20 microseconds; some analog-to-digital converters used in the DAS may operate faster.

3-87. During the CLK 2 pulse, gate U75A is again enabled, causing the CP input to address counter U122 to go low. At this time, the other inputs to address counter U122 are:

a. CEP and $\overline{PE}$ are as described in paragraph 3-82.
b. CET is determined by bit B0 of the command word.

If bit B0 is high, indicating single-ended mode, U96C is enabled and CET is set low via U95B. U122 will therefore not respond to CP. On the other hand, if bit B0 is low, indicating differential mode, U96C is disabled and causes CET to be high. Thus, at time F, address counter U122 is again incremented.

3-88. CLK 2 one-shot U114A completes its pulse at time H and fires CLK 3 one-shot U114B. At time I, the trailing edge of CLK 3 clocks shift register U83. The Q0 output of U83 goes low and the Q1 output goes high (state S2).

3-89. This situation prevails until the analog-to-digital converter completes its conversion at time J and outputs a low end-of-conversion (EOC) signal. EOC fires MPX delay one-shot U124B, which prevents S/H flip-flop U72B from initiating another hold until the sampling circuitry has settled. EOC also fires CLK 1 one-shot U134 via gates U84B and U104A. U134 in turn fires CLK 2 one-shot U114A at time K. The CLK 2 pulse is combined with a high S2 signal by gate U105D. U105D-11 goes low and presets HLMPX Inhibit flip-flop Ul06B. Ul06B-8 goes low and inhibits address decoders U102 and U92 via gates U105C and U105B; this is done in order to prevent possible channel overlap when address latch U112 is updated. The low on U106B-8 also sets the CEP input to address counter U122 low, preventing a third clock signal from incrementing the address counter contents.

3-90. At time L the trailing edge of CLK 2 clocks (loads) address latch U112 via gate U105D, and simultaneously fires CLK 3 one-shot U114B. U114B-10 goes high, then goes low at time M and fires U134 via gates U94B and U104A. U134 in turn fires CLK 2 one-shot U114A. U114B also clocks shift register U83, whose Q2 output goes high (state S3).

3-91. The DAS card provides a repetitive scan capability with the use of a last address detector (LAD) which consists of gate U103B and inverter U113D. When the sequential scan has reached the point where address latch U112 contains the last channel address available (channel 15 for single-ended, channel 14 for differential), gate U103B becomes enabled and applies a high to input 13 of gate U95D. During the interval that state signal S3 is high, gate U95D is enabled and applies a low PE input to address counter U122 via gate U96D. Another clock pulse is applied to the CP input of address counter U122 during the CLK 2 pulse. This loads the counter with the address contained in address register U132. This is the only time that the sequential mode accesses address register U132; at other times it merely increments the contents of address counter U122. Note that the address counter will be incremented once or twice (single-ended or differential) before its contents are applied to the channel decoders during the next cycle. Thus the sequential command word must contain the starting address minus one or two. Consult the operating manual for exact programming instructions.

3-92. Completing its CLK 2 pulse at time O, U114A clocks address counter U122 via gate U75A (inhibited by U106B unless a parallel load is enabled via last address detector U103B), and fires CLK 3 one-shot U114B. At time P U114B again fires CLK 1 one-shot U134 via gates U94B and U104A, and clocks shift register U83. The Q2 output of U83 goes low and clocks HLMPX inhibit flip-flop U106B via inverter U93B. U106B-8 goes high, enabling address decoders U102 and U92. Simultaneously, the Q3 output of U83 goes high (state S4), enabling one input of gate U105A. CLK 1 one-shot U134 in turn fires CLK 2 one-shot U114A, enabling the other input of gate U105A. U105A clears S/H flip-flop U72B via gate U82A.

3-93. At time P U114B clocks shift register U83, returning U83 to the normalized state. During the time that the CLK 3 pulse is present, cycle complete gate U104B is enabled and flag buffer flip-flop U76A/U86C is set. From this point, the sequence is completed as described in paragraph 3-66. This completes the sequencing for one sequential mode data acquisition. MPX delay one-shot U124B, which was fired during the cycle, inhibits the next sample-to-hold transition until the end of its 26-microsecond rundown.

3-94. Digitize Mode Operation—The foregoing paragraphs described the sequencing for the sequential mode of

operation. In the digitize mode, sequencing is identical except for the operation of address counter U122. In the digitize mode, mode decoder output U123-5 is high, setting the PE input to address counter U122 low via inverter U74E and gate U96D, and the CET input high via gates U96C and U95B. Thus, when the address counter is clocked via gate U75A at time D (paragraphs 3-81, 3-82) and time H (paragraph 3-88) the contents of address register U132 are loaded into address counter U122. The load operation again occurs at time O; although only one load operation is required, three are used to simplify the logic. In any case, the selected multiplex channel is not changed until address latch U112 is clocked at time I.

3-95. Random Mode Operation–The operation of the DAS card in random mode is essentially the same as sequential with the following two exceptions:

a. The operation of address counter U122 is as described in digitize mode.

b. The acquisition cycle is performed twice. The first cycle sets the multiplex address, and the second takes the measurement.

3-96. In random mode, output 9 of mode decoder U123 is low. This, combined with the state 0 signal (S0) and the first CLK 2 pulse, enables gate U73A and clocks status flip-flop U72A to the set state. The circuit now follows the normal sequence described above, with these exceptions:

a. The low $\overline{Q}$ output of status flip-flop U72A enables gate U77C via gate U77D. This inhibits the sample and hold from waiting for a pace pulse during this cycle.

b. When the cycle is completed the first time, the low $\overline{Q}$ output of U72A disables cycle complete gate U104B.

3-97. The high Q output of U72A enables gate U94B via U94A and U84A. This causes the last CLK 3 pulse of the first cycle to initiate a new series of clock pulses and a complete new cycle. At this point, the channel address programmed in the random command has been loaded into address latch U112.

3-98. During the first series of clock pulses of the second cycle, status flip-flop U72A is again toggled, this time to its reset state. The remainder of the cycle is exactly the same as in digitize mode.

SECTION IV
MAINTENANCE

4-1. INTRODUCTION

4-2. This section contains calibration procedures and troubleshooting information for the HP 91000 DAS card. Figures 4-8 and 4-9 show the physical and electrical configurations, respectively. The DAS card is very sensitive to contamination, such as can easily occur during replacement of components. For this reason, field repair should not be performed. Hewlett-Packard provides replacement cards on an exchange basis. The replacement card is available at a reduced rate in exchange for the defective card. The nearest Hewlett-Packard Sales and Service office can provide all procurement details.

4-3. TEST EQUIPMENT

4-4. Table 4-1 lists the test equipment required to conduct the calibration procedures and troubleshooting checks. Test equipment with characteristics similar to those specified may be substituted. A test input connector as specified in Table 4-1 and illustrated in Table 4-2 is also required.

4-5. PERFORMANCE CHECKS

4-6. The HP 91000A Verification Test Program (HP Part No. 91000-60002), described later in this section, will operate the DAS in its various operating modes, take readings of input voltage levels, and print the results on the system teleprinter.

4-7. Once the test results are obtained, subsystem accuracy and other specifications may be calculated and compared with the specifications listed in Section I of this manual.

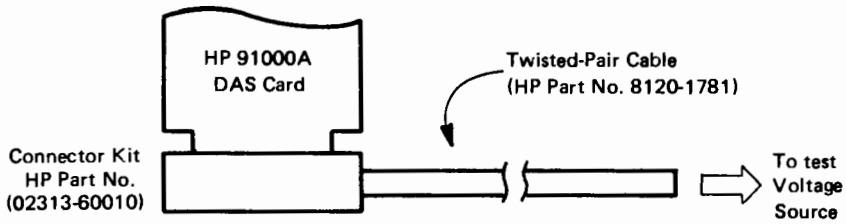
4-8. The performance test may be found near the end of this section, paragraphs 4-43 through 4-84. It is recommended that performance checks be performed for the following purposes:

- As part of an incoming inspection check
- As part of a preventive maintenance procedure to verify subsystem operation

Table 4-1. Recommended Calibration Test Equipment

Item	Characteristics	Recommended Type
Oscilloscope	Bandwidth: DC to 50 MHz Sensitivity: 10 mV to 10 volts	HP 180A with 1820A and 1801A plug-in
Digital Voltmeter	Range: 0 to 100 Vdc Accuracy: ±0.01% Resolution: 0.001%	HP 2402A or HP 3490A
Power Supply	Output: 0 to 20 volts Ripple/Noise: 40 μV /100 μV	HP 6111A
Input Test Connector		Fabricate as shown in Table 4-2. Requires the following components: a. Connector Kit, 02313-60010 b. Cable 8120-1781 (Twisted pair, shielded)
Card Extender		HP 02116-63216

Table 4-2. Input Test Connector



HLMPX Connector Pin Assignment	Remarks
1	HI } Differential Channel ø
3	LO } Differential Channel ø
	Shield*

*Do not connect shield at HLMPX end of cable.

*Refer to Section II for assembly instructions

TP 91000-23

- After replacement or repair of equipment to ensure correct operation before returning the subsystem to regular service

4-9. CALIBRATION PROCEDURE

4-10. The following paragraphs present detailed procedures for calibrating the HP 91000A DAS card. Calibration should be performed monthly or whenever the results of the performance checks clearly establish the need to do so. The calibration procedures should be performed exactly in the given sequence, since certain adjustments are interactive.

4-11. PRELIMINARY ADJUSTMENTS

4-12. Before calibrating the DAS card, perform the following steps.

CAUTION

Always make sure that mainframe power is off before installing or removing the DAS card. Failure to observe this precaution may result in damage to the card.

a. Remove power from computer mainframe and remove cover to gain access to the I/O cards.
b. Remove DAS card and install an extender card in its place.
c. Install DAS card in extender.
d. Connect test cables to DAS card.

4-13. THROUGHPUT RATE ADJUSTMENT

4-14. Set throughput rate adjustment as specified in the following steps.

a. Load verification program as specified in the programming manual.
b. Make following entries on keyboard:*

>CLEAR All

>SET Repeat

>SIngle Channel

No = 1

Channel = 0

*It is only necessary to type that portion of entry that is enclosed in box.

c. Connect oscilloscope input to TP 30 on DAS card. Set sweep speed to 5 μsec/div, sensitivity to 5 volts/div, trigger to internal negative slope. Oscilloscope should display a pulse train with a period of 30 to 60 μsec.
d. On DAS card, adjust delay one-shot potentiometer R69 until negative-going pulse width is 26 ±0.5 μsec. After adjusting R69, verify that the

negative-going edge of second pulse is less than 50 μsec from start of sweep, as shown in Figure 4-1.
e. When adjustment is complete, depress any teleprinter key to abort repeating test mode.

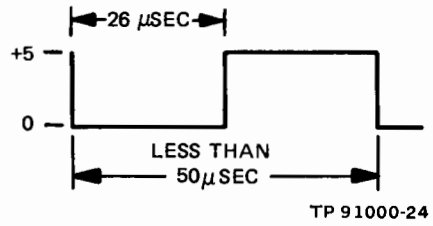


Figure 4-1. Delay One-Shot Output

4-15. DIFFERENTIAL-TO-SINGLE-ENDED ADJUSTMENT

4-16. Check calibration of the differential-to-single-ended zero circuit as specified in the following steps.

a. Connect test equipment to DAS card as shown in Figure 4-2. Connect HI lead of DVM to TP16 (DIFF TO SE OUT) on DAS card.
b. Set DC power supply output to 0.000 volts and short + and - output terminals together with a jumper.
c. Connect voltage source to the analog circuits with following teleprinter input:

>NOrmalize

>CLEAR All

>SIngle Channel

NO = 1

CHANNEL = 0

d. On DAS card, adjust differential-to-single-ended zero potentiometer R43 until voltmeter indicates 0 ±1 mV.

4-17. SAMPLE/HOLD ZERO

4-18. Adjust the sample/hold zero circuit as specified in the following steps.

a. With test equipment connected as shown in Figure 4-2, connect HI lead of DVM to TP17 (S/H AMP OUT) on DAS card.
b. Adjust S/H ZERO potentiometer R51 on DAS card for an indication of 0 ± 1 mV on DVM.

4-19. COMMON MODE REJECTION ADJUSTMENT

4-20. Adjust the common mode rejection circuit as specified in the following steps.

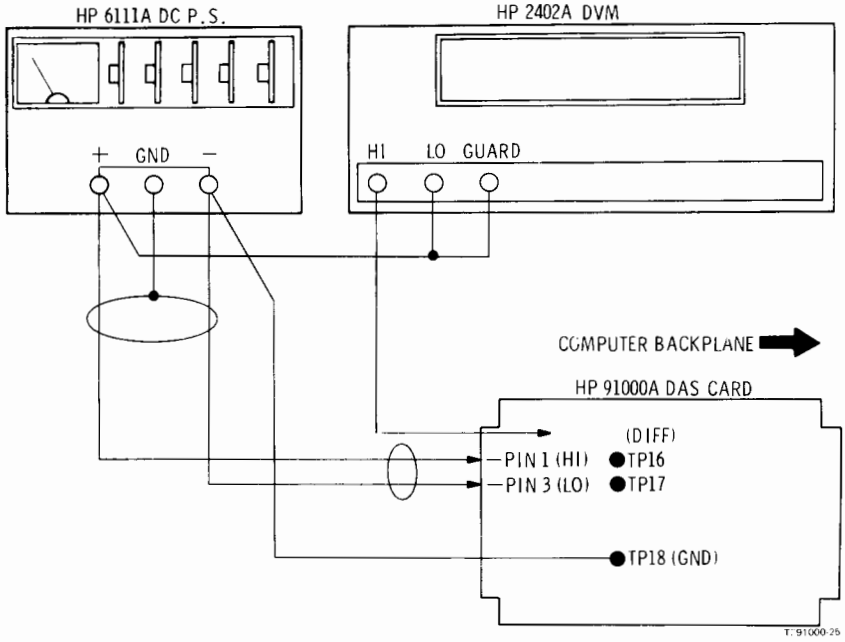


Figure 4-2. Zero Adjustment Test Setup

a. Connect test equipment to DAS as shown in Figure 4-3.
b. Set DC power supply output to 10.000 ±0.1 volts.
c. On DAS card, adjust CMR potentiometer R44 to obtain indication of 0 ±0.2 mV on DVM.
d. Reverse + and - leads of DC power supply. Verify that DVM still indicates 0 ±1 mV. Note exact indication.
e. Adjust CMR potentiometer R44 on DAS until DVM indicates half the value noted in step d.
f. Again reverse DC power supply leads. DVM indication should be the same as that noted in step e ±0.2 mV. If not, repeat steps d and e.

4-21. DYNAMIC OFFSET ADJUSTMENT

4-22. Adjust dynamic offset as specified in the following steps.

a. Make following keyboard entries.

>CLEAR All

>SET Repeat

>SIngle Channel

NO = 1

Channel = 0

b. Connect oscilloscope input to TP17 on DAS card.
c. Trigger oscilloscope externally from TP26 (STC) on DAS card, using negative slope. Set oscilloscope sweep speed to 5 μsec/div, sensitivity to 50 mV/div or better.
d. On DAS card, adjust dynamic offset potentiometer R55 to obtain a scope trace as straight as possible, centered at 0.0 volts.

4.23. ANALOG-TO-DIGITAL CONVERTER (ADC) OFFSET ADJUSTMENT

4-24. Set the ADC offset as specified in the following steps.

a. Connect test equipment to DAS card as shown in Figure 4-4.
b. Examine analog-to-digital converter on DAS card. If the card uses a Phoenix Data, Inc. (PDI) ADC, set DC power supply to obtain an indication of -0.0025 on DVM. If the card uses any other type of ADC, set power supply to -10.2375 volts.
c. Set up repeating histogram mode on computer as follows.

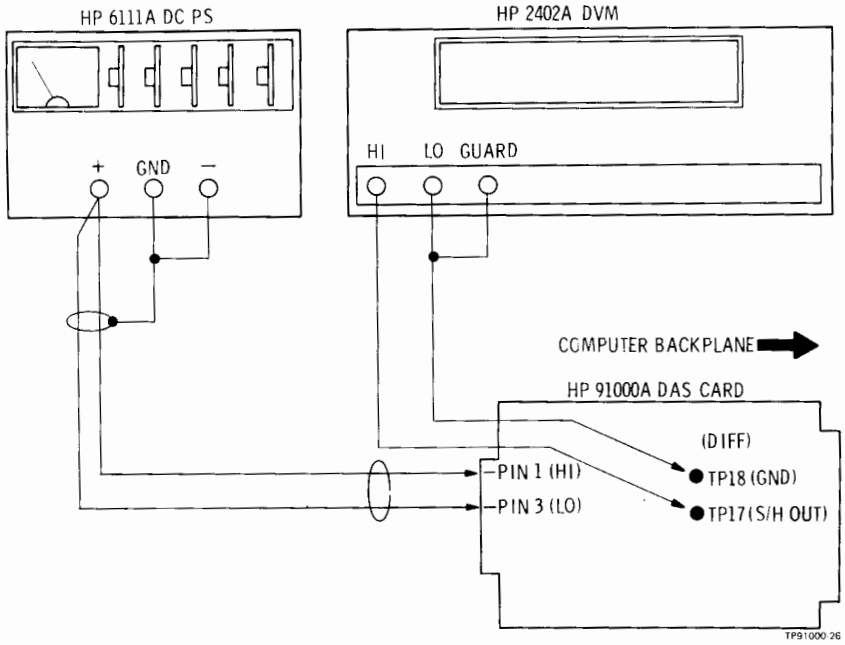


Figure 4-3. CMR Test Setup

d. Set SWITCH REGISTER switch 15 to "1". This suppresses printout except for average (AVG) reading.

e. Make following keyboard entries.

>CLEAR All

>SET Repeat

>HIstogram

NO = 32767

CHANNEL = 0

AVG = -----

AVG = -----

.
.
.

f. On DAS card, adjust ADC offset potentiometer R59 until TTY printout AVG reading equals the voltage input in step b.

g. Depress any teleprinter key to abort repeating histogram mode.

4-25. ADC GAIN ADJUSTMENT

4-26. Set ADC gain as specified in the following steps.

a. Continuing from previous setup, reverse + and - leads on DC power supply, connect jumper between GND and - terminals, and set power supply output to + 10.2325 volts, as indicated on DVM.

b. On keyboard, enter the command

REpeat.

c. On DAS card, adjust ADC gain potentiometer R61 until TTY printout of AVG reading is +10.2325.

d. Depress any teleprinter key to abort repeating histogram mode. The HP 91000A DAS card is now calibrated.

NOTE

If the sample/hold amplifier dynamic offset adjustment was not done accurately enough, the ADC OFFSET and ADC GAIN pots may not have sufficient range to achieve calibration. It may be necessary to readjust R55.

4-27. **TROUBLESHOOTING**

4-28. A malfunction in a previously operable subsystem can appear in many forms and any attempt to provide detailed

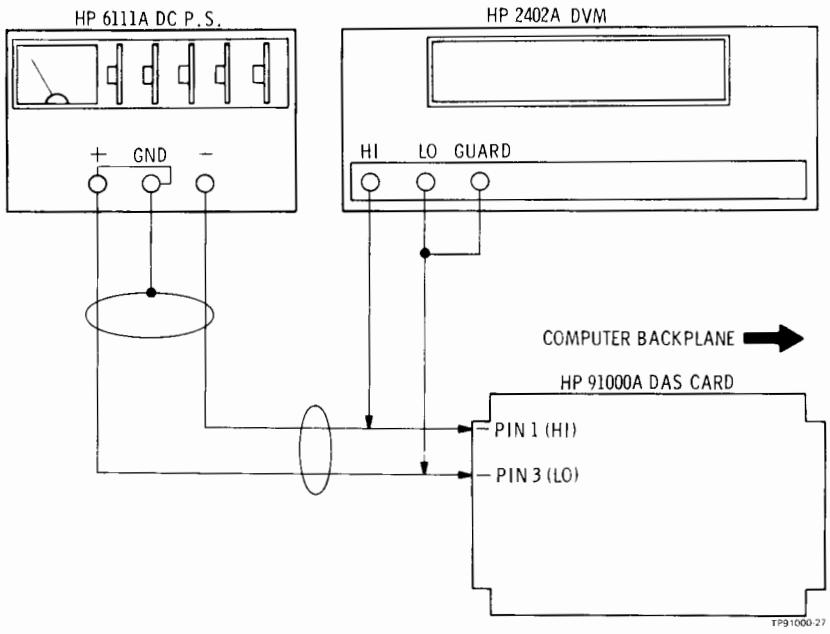


Figure 4-4. Calibration Test Setup

troubleshooting data for all possible failures that may occur is not practical. It is possible, however, to group certain malfunctions together and isolate them to major components or circuit areas on the card. The two major classifications of malfunctions are:

- Subsystem hangs up (stops) without completing a programmed operation
- Subsystem returns bad (incorrect) data to computer

4-29. PRELIMINARY CHECKS

4-30. Table 4-3 lists several of the more obvious causes of malfunctions which are often overlooked. These items should be checked before proceeding with other tests.

4-31. USE OF VERIFICATION PROGRAM

4-32. If the preliminary checks did not isolate the malfunction, simulate the malfunction using the Verification Program, Paragraph 4-43. This program is flexible enough to simulate any normal programming sequence. If the malfunction can not be duplicated, it is probably due to software problems. Assuming the failure can be repeated with the verification program, continue to the Subsystem Hang-Up or Subsystem Bad Data procedures, as appropriate.

4-33. SUBSYSTEM HANG-UP

4-34. A failure of this type implies a defect in the control or interface logic circuitry or the absence of a response signal from the analog-to-digital converter (ADC) module. The DAS can hang up in any of several states, as indicated by the outputs of shift register U83. The particular state should indicate the nature of the failure.

4-35. NORMALIZE CHECK - Before troubleshooting the logic circuitry, perform this test: Load the HP 91000A Verification Program and normalize the DAS card several times with the NORMALIZE command. This command exercises much of the interface logic and requires the occurrence of clock pulses CLK 1, CLK 2, and CLK 3. If the prompter >is not returned after typing NO, then the problem may be in the interface logic, clock one-shot string, mode decoder U123 and normalize flip- flop U106A, or cycle complete gate U104B.

Table 4-3. Preliminary Checks

Item	Check
Backplane connector	Check that the DAS card is firmly seated in its connector.
Input cable	Check that the input cable is firmly and properly connected to the front of the DAS card.
Jumpers	Check that the differential/single-ended jumpers are correctly positioned. See Figures 2-1 and 2-2.
Interrupt chain	Check that there are no higher priority I/O slots empty, if the program requires the interrupt system.
+5 volts	Check for presence of approximately +4.75 volts at backplane connector pins 39 and 40. Use pins 1 and 2 for ground.
-2 volts	Check for presence of 2 volts at backplane connector pins 47 and 48. Use pins 1 and 2 for ground.
+E	Check resistors R70 and R81 for positive bias voltage of at least 3.5 volts. One side of each resistor is connected to +4.85 volts.
±15 volts	Check TP32 for presence of +15 ±0.105 volts, and TP33 for -15 ±0.105 volts.
Pacer	Verify that pace mode is programmed correctly, pace pulse generator is operating, pace pulse rate is correct.

Table 4-4. Normalize Mode Troubleshooting Program

Memory Location	Contents	Label	Operation	Operand
100	060110		LDA	NORM
101	1067xx	REPT	CLC	SC
102	1026xx		OTA	SC
103	1037xx		STC	SC,C
104	064111		LDB	DELAY
105	034001		ISZ	1
106	024105		JMP	*-1
107	024101		JMP	REPT
110	140001	NORM	OCT	140001
111	177754	DELAY	OCT	177754

xx = Select Code of DAS.

4-36. Load the test program shown in Table 4-4 into the computer starting at location 100_8. This program repetitively programs a normalize command, delays approximately 100 μsec, then clears the control and flag flip-flops.

4-37. Check for the following signals:

1. Negative-going STC pulse at TP26 when program executes STC instruction.
2. Normalize flip-flop U106-6 set low by STC pulse.
3. Positive-going CLK 1 pulse at TP40 at the end of the STC pulse.
4. Positive-going pulse at TP22 and TP23.
5. Negative-going pulse at U104-8.
6. Flag buffer flip-flop U76-6 and flag flip-flop U97-8 set.

4-38. HANG-UP TROUBLESHOOTING – If the DAS responds properly with a NORMALIZE command but hangs up when programming other commands with the verification program, the fault is likely due to shift register U83, the gates feeding CLK 1 one-shot U134, the S/H control logic, or the ADC. Table 4-5 lists the possible states of the control logic, the corresponding shift register indication, and the signals required to cause the logic to advance to the next state. The sequence of operation is:

a. Shift register U83 is clocked to a new state (STATE) by a CLK 3 pulse
b. A particular signal causes the one-shot chain to fire (SIGNAL REQ'D TO ADVANCE)
c. The CLK 3 pulse of the chain causes the shift register to advance to the next state (NEXT STATE)

4-39. When the DAS card is stopped in some state, check the outputs of shift register U83 and compare the results with the INDICATION column of Table 4-5. This will identify the current state of the card. The SIGNAL REQ'D TO ADVANCE column or the COMMENTS column will identify the signal that is required to cause the DAS card to advance to the next state.

4-40. If it is desired to repetitively command the DAS to allow the use of an oscilloscope in troubleshooting the card, the program given in Table 4-6 may be loaded into the computer. Start the program at location 100 The program will first normalize the card and then repetitively:

a. Program a random mode reading on channel 0,
b. Delay approximately 150 μsec, and
c. Program a normalize command.

Table 4-5. DAS Logic State Table

State	Indication	Signal Required to Advance	Next State	Comments
S0	All shift register outputs low. U93-10 high.	STC	S1	Reset State. DAS is waiting for a command.
S1	U83-15 (Q0) high	S/H delay one-shot U124A	S2	S/H is enabled by transition from state S0 to state S1. If one-shot does not fire, check for proper programming of paced/unpaced mode and proper operation of pace pulse.
S2	U83-14 (Q1) high	EOC (TP20) high-to-low transition	S3	SOC pulse generated during state S1, CLK 2 pulse. EOC should be set high during that particular CLK 2 pulse. If SOC occurs, but EOC does not respond correctly, (should go low 15-20 μsec after SOC), then the ADC has probably failed.
S3	U83-13 (Q2) high	AUTOMATIC	S4	S3 pulses started by CLK 3 of state S2; enabled by U83-14 (Q1) via gates U93E and U84A.
S4	U83-12 (Q3) high	AUTOMATIC	S0	S4 pulses started by CLK 3 of state S3; enabled by U83-13 (Q2) via gates U93B and U84A.
S0	U93-10 high	AUTOMATIC	S1	Random mode only, second half of operation. S0 pulses started by CLK 3 of state S4; enabled by U83-12 (Q3) and status flip-flop U72A via gates U94A and U84A.

4-41. BAD DATA TROUBLESHOOTING

4-42. Using the HP 91000A Verification Program, determine if bad data is returned from all channels or just one channel. Bad data from all channels usually indicates a need to re-calibrate the DAS card, and this should be done if the preliminary checks along with the data listed below do not locate the malfunction. If it becomes impossible to complete the calibration procedure, refer to Table 4-7 under the appropriate step and take the action indicated. If only one channel is defective, check the following possibilities:

a. Improper cabling of inputs or poor input connector seating
b. Bits of wire or solder on circuit side of PC board
c. Defective CMOS input switch (Q1-Q8)
d. Faulty input switch drive circuitry (troubleshoot control logic)
e. Differential-to-single-ended jumpers incorrectly placed
f. Open or shorted input resistors or diodes
g. If user's software, wrong channel may be programmed.

4-43. SUBSYSTEM VERIFICATION AND PERFORMANCE TEST

4-44. GENERAL

4-45. The following paragraphs contain instructions for using the HP 91000A Verification Program (HP Part Number 91000-60002) as a confidence test to verify subsystem operation as part of an HP Computer System. The verification program is an absolute binary program that is loaded into memory using the computer's basic binary loader.

Table 4-6. Hang-Up Troubleshooting Program

Memory Location	Contents	Label	Operation	Operand
100	060115	REPT	LDA	NORM
101	1067xx		CLC	SC
102	1026xx		OTA	SC
103	1037xx		STC	SC,C
104	1023xx		SFS	SC
105	024104		JMP	*-1
106	060116		LDA	RANDM
107	1026xx		OTA	SC
110	1037xx		STC	SC,C
111	064117		LDB	DELAY
112	034001		ISZ	1
113	024112		JMP	*-1
114	024100		JMP	REPT
115	140001	NORM	OCT	140001
116	100000	RANDM	OCT	100000
117	177742	DELAY	OCT	177742

xx = Select Code of DAS

4-46. Inputs to the subsystem are connected as described in Section II. In performing this test it is assumed that the user has completed the installation and will use the actual input signals to verify specifications. If the user desires to use a calibrated voltage source, the source should be adjustable between 0.000 and ±10.240 volts with a stability of ±100 μV and an output impedance of 1000 ohms or less. Both positive and negative polarity should be available.

4-47. DESCRIPTION

4-48. The verification program is a powerful component of the HP 91000A subsystem. The verification, properly applied, can perform the following tasks for the user:

a. Test the hardware system from inputs, through the HP 91000A and computer, to final displayed results. This means that the programmer can verify and debug inputs before writing operating software, and write operating programs without hardware debugging routines.

b. Provide a calibration aid.

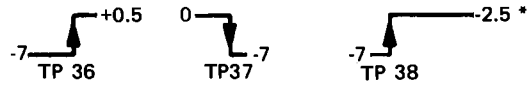
c. Provide a convenient means of troubleshooting the entire subsystem.

d. Operate the subsystem in all its various modes and configurations for training purposes.

4-49. The verification program is an interactive program which can exercise all the modes of the DAS card under operator control. The operator enters commands via a TTY or a tape reader, and the measured data will be printed on the TTY. If the input voltages are known, the DAS accuracy may be computed and compared to the specifications listed in Table 1-1.

4-50. Figure 4-5 and Table 4-8 describe each operating mode, operating command, and condition that is available to the user to check the subsystem. These items will be described further in subsequent paragraphs.

Table 4-7. Bad Data Troubleshooting

Calibration Step Failed	Symptoms	Possible Cause
Throughput rate adjust (Para. 4-13)	Waveform is absent or differs greatly from that specified.	a. Test equipment improperly connected. b. Wrong test or conditions entered to verification program. c. Verification program configured for DAS card in differen slot. d. Fault in logic section; check U124, C7, R68, R69.
	Cannot adjust R69 for correct timing.	a. Check R68, R69, C7.
Differential-to-single-ended zero adjust (Para. 4-15)	Cannot obtain correct adjustment	a. Check R43. b. Verify approximately zero volts between pin 3 of U1 and pin 3 of U2. If zero, suspect U1, U2, or U3. If not zero, suspect Q1 and associated drive circuitry.
Sample-to-hold-zero adjust (Para. 4-17)	Cannot obtain correct adjustment	a. Check R51. b. Verify presence of zero volts between TP16 and TP18. If zero, suspect U3, Q10, and associated components. If not zero, perform checks in step b above.
CMR adjust (Para. 4-19)	Cannot obtain correct adjustment	a. Suspect U2, R40, R41, R42, R44.
Dynamic offset adjust (Para. 4-21)	Cannot obtain correct adjustment	a. Use verification to take one reading, single channel, channel = 0, and set repeat. Check test points 36, 37, and 38 for the indicated waveforms. Trigger oscilloscope externally from TP25, + slope.  * APPROXIMATE. ADJUSTABLE BY R55. If waveforms are incorrect, suspect Q11 or U72 and associated circuitry. If waveforms are correct, suspect Q10 and/or Q9.
ADC offset adjust (Para. 4-23)	Cannot obtain correct adjustment	a. Check R59 and R60 for proper operation. b. Suspect ADC module.
ADC gain adjust (Para. 4-25)	Cannot obtain correct adjustment	a. Check R61 and R62 for proper operation. b. Suspect ADC module.

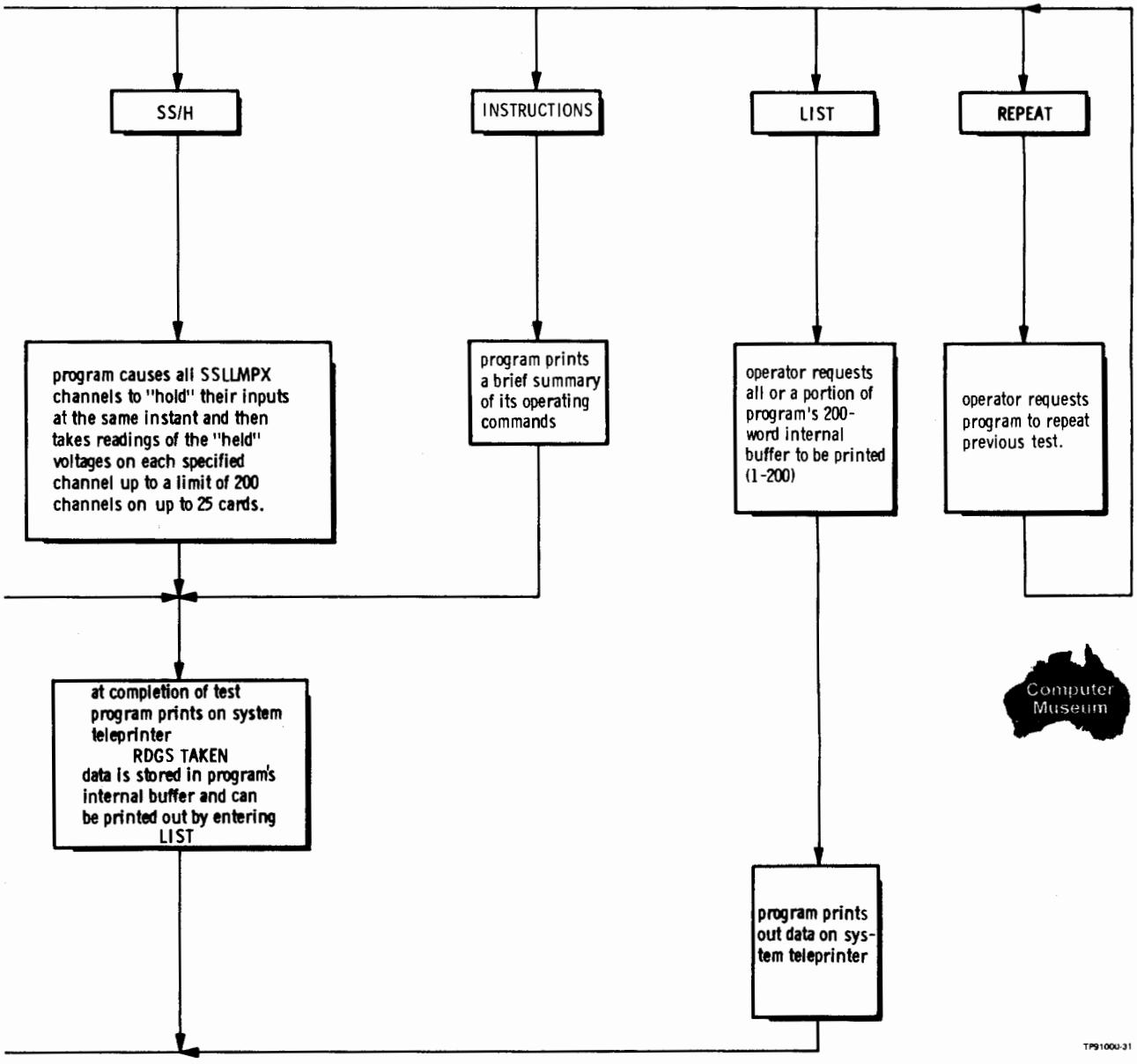
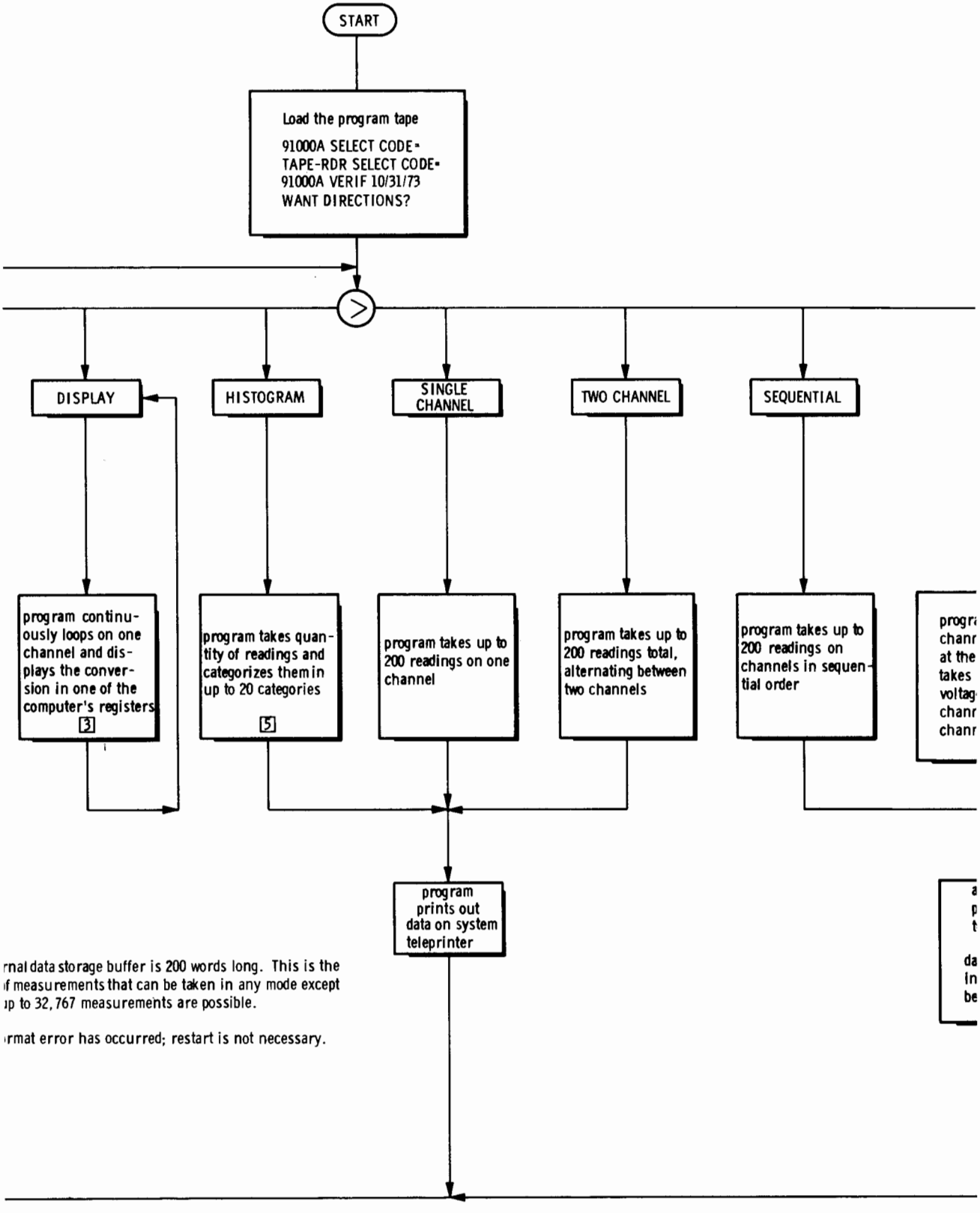
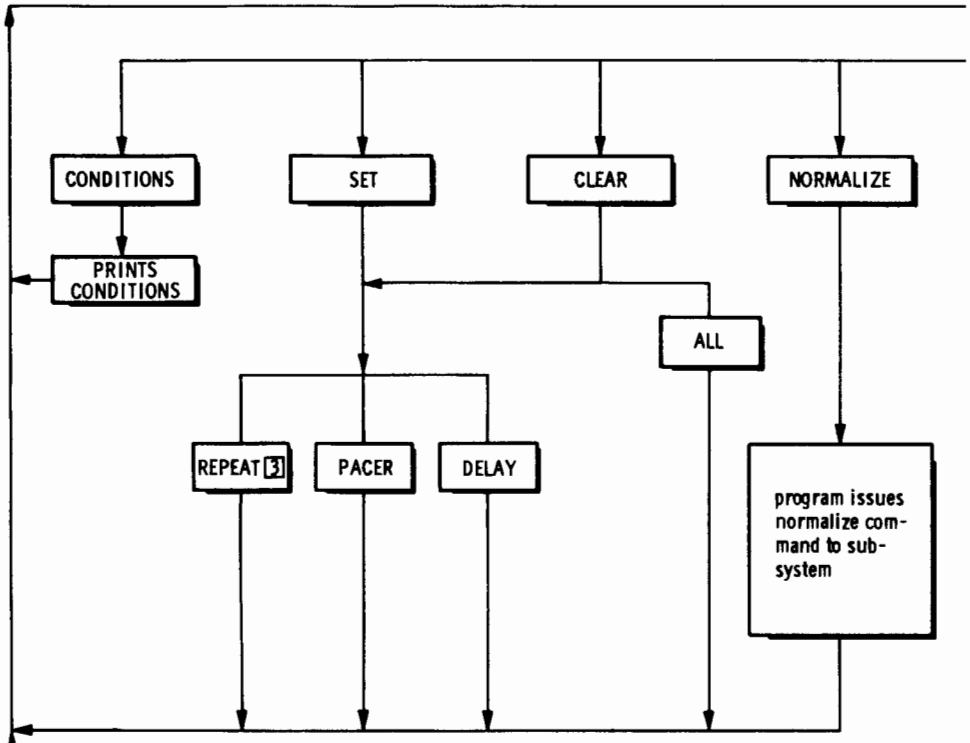


Figure 4-5. Flowchart of Verification Commands



rnal data storage buffer is 200 words long. This is the
f measurements that can be taken in any mode except
p to 32,767 measurements are possible.

rmat error has occurred; restart is not necessary.



NOTES

1. If a negative number (-1 to -9) is entered for an answer to any question that expects a number, that test will abort or the condition will be cleared.
2. If the word ABORT is entered for an answer to any question that expects a YES or NO answer, that test will abort or the condition will be cleared.
3. To abort a test once it has started running, or, to exit the Display mode or Repeat condition, strike any key on the keyboard.
4. Restart at address 2 does not clear any conditions nor return control to the keyboard. Restart at address 2000 clears any conditions that were set and returns control to the keyboard.
5. The program's inte
maximum number
Histogram, where
6. * FMT indicates a f

Table 4-8. Description of Verification Commands

Type of Command	Command	Example/Description
Test Mode	Sequential	>SE NO= 5 — Enter the total number of readings. 1ST CH CHANNEL= 0 — Enter the channel number for the starting channel. Starting channel must be even if scan will exceed last channel on card. DIFF: — Answer YES if the channels are differential of NO if they are single-ended. RDGS TAKEN — Readings are taken and are available for listing. If the Repeat condition is set, this message is not printed.
	Histogram	>HI NO= 3000 — Enter the total number of readings. For a meaningful test, between 10,000 and 30,000 readings should be taken. CHANNEL= 3 — Enter the channel number to be measured. If the inputs are differential, there are only even numbered channels. AVG= .404950 PP= 005000 HI= 405000 LO= .400000 RMS= .00049749 In this space the readings are categorized according to how many readings were taken at a specific voltage. If more than 20 categories are attempted, the program terminates the test and prints the message: NO FINISH: X RDGS — Where X is the total number of readings taken. If Set Repeat is used with Histogram, the test is repeated and the above data is continuously printed. Setting switch 15 = "1" eliminates all print-out except the average.
	Display	>DI CHANNEL= 3 — Enter the channel number to be displayed. The channel selected will be continuously converted and displayed in the computer's B-register (HP 2115/2116) or switch register (HP 2100/2114).

Table 4-8. Description of Verification Commands (Continued)

Type of Command	Command	Example/Description
Test Mode (Continued)		AVERAGE? — A YES answer will cause 16 readings to be averaged and displayed with bit 0 (LSB) = 0.125 mV. A NO answer will cause each individual reading to be displayed with bit 4 (LSB) = 5.0 mV. To abort the Display mode strike any key on the keyboard.
	Single Channel	>SI NO= 200 — Enter the total number of readings desired. CHANNEL= 4 — Enter the channel number to be measured. If the inputs are differential, there are only even numbered channels. AVG= .404950 PP= 005000 HI= .405000 LO= .400000 RMS= .00049749 Data is printed in the above form unless the Repeat condition is set.
	Two Channel	>TW NO= 200 — Enter the total number of readings desired on both channels. CHANNEL= 4 — Enter the channel number to be measured. If the inputs are differential, there are only even numbered channels. CHANNEL= 10 — Same as above for second channel. 1ST CH AVG= .404958 PP= 0.00500 HI= .405000 LO= .400010 RMS= .00049749 2ND CH AVG= 3.120000 PP= .000008 HI= 3.120000 LO= 3.120000 RMS= .00000000
	Instructions	>IN — The program prints a summary of the operating commands.

Table 4-8. Description of Verification Commands (Continued)

Type of Command	Command	Example/Description	
Program Control	Conditions	>CO	What conditions are set? All active conditions are identified as follows: COND: P for PACER mode D for DELAY is enabled R for REPEAT is enabled. When restart is exercised at address 2 any conditions that are set are listed and remain set. When restart is exercised at address 2000 (configuration required), any conditions previously set are cleared.
	Tape	>TA	Take all further commands from the punched tape reader. When control is switched to the tape reader, the keyboard can only be used to abort the Display mode, any test continuously running under the Repeat condition, or whenever the system is hung-up in a loop. However, if the tape reader select code question was answered with a 0 allowing punched tape control through the TTY, this abort feature is not available. To abort a test the computer must be halted and then restarted. Control is always returned to the keyboard when KE is encountered on the punched tape. When the computer is halted and restart is exercised at address 2, control remains delegated to the tape reader. If the program is restarted at address 2000, control reverts to the keyboard.
	Keyboard	>KE	Take all further commands from the keyboard key (TTY). When the Tape mode is used, keyboard should always be the last command on the punched tape. When the program is restarted at address 2000, control is delegated to the keyboard.
	Asterisk	>*	The asterisk signifies a comment statement. When used, everything between the * and carriage return/line feed becomes a comment and is ignored by the verification program. There is no limit to the number of consecutive lines of comments.

Table 4-8. Description of Verification Commands (Continued)

Type of Command	Command	Example/Description	
Program Control (Continued)	Repeat	>RE	Repeat the last test with the same parameters. Repeat is not available after entering a negative number to abort a test. It is also not available initially.
	List	>LI START,FINISH=	Enter a pair of numbers to list any part or all of the data buffer (readings 1 to 200). If the last test was Histogram, requesting List causes the Histogram results to be repeated. List is not available after Display, or with Repeat condition set, or whenever a test is aborted. Use switch 15 to terminate the print-out early. If switch 15 is set when List is called, then only one reading will be printed.
	Normalize	>NO	Issue the normalize command to the subsystem. The DAS should return to its home state.
Conditions	Set Repeat	>SET R	Continuously repeat the next test without print-outs until a keyboard key is pressed. Histogram continues to print all information unless switch 15 is set; then only the average is printed. If commands are being entered by punched tape through the high-speed tape reader, the test can still be aborted by pressing any key on the keyboard. If commands are being entered by punched tape through the teleprinter tape reader, the test cannot be aborted through the keyboard. To abort a test the computer must be halted and restarted.
	Clear	>CLEAR	Conditions are cleared as follows: CLEAR P for PACER CLEAR R for REPEAT CLEAR D for DELAY CLEAR A for all conditions.

Table 4-8. Description of Verification Commands (Continued)

Type of Command	Command	Example/Description	
Conditions (Continued)	Set Pacer	>SET P	The pacer condition is to allow the use of an external pulse generator to time the occurrence of each reading. When this condition is set, no readings will be taken until the pulse occurs. If readings are attempted with the pacer condition set and there is no pacer connected, the DAS will hang up and no data will be returned. To get out of this condition, hit any keyboard key to get the prompter back and type CLEAR P.
	Set Delay	>SET D MULT=	Enter the delay desired between readings as a multiple of 10 microseconds; i.e., a multiple of 100 would yield a delay of 1 millisecond. The delay occurs between each reading in SINGLE CHANNEL, HISTOGRAM, or DISPLAY mode, between every other reading in TWO CHANNEL mode, and between SCANS if repeat is set in SEQUENTIAL mode.

4-51. OPERATING VERIFICATION PROGRAM

4-52. The following paragraphs describe the characteristics of the verification program and, together with Figure 4-5 and Table 4-8, present all the information required to operate the program.

4-53. LOADING AND STARTING THE PROGRAM–The HP 91000A verification program is loaded into memory using the computer's basic binary loader. After the tape is loaded, go to the starting address of the program (octal 002000), clear the switch register, and then set the switch register to the octal I/O location of the teleprinter (TTY) interface card. Press the PRESET button(s) and then the RUN button on the computer, then clear the switch register. The verification program requires initialization the first time it is run and each time it is restarted at address 002000 as follows:

NOTE

All entries from teleprinter or tape reader must be followed by RETURN and LINE FEED (CR/LF).

a. 91000A SELECT CODE =
Respond with the octal I/O select code of the DAS card.

b. TAPE-RDR SELECT CODE =
Respond with the octal select code of tape reader I/O card or 0 if tape reader on TTY is to be used.

c. 91000A VERIF 10/31/73
This is the date of the lates version of the program and should agree with the data printed on the cover page preceding the listing.

d. WANT DIRECTIONS?
Answer YES or NO; a sample printout is provided in Figure 4-6.

4-54. If the response to the above question was NO, a prompter (>) is printed and the program awaits the first command. (The program always issues the prompter when it is ready to accept a command).

4-55. ENTERING COMMANDS–It is only necessary to type the first two characters of any command. That is, SI is equivalent to SINGLE CHANNEL. When setting or clearing conditions, it is only necessary to type the first character of the condition in addition to the word SET or CLEAR. That is, SET D is equivalent to SET DELAY.

4-56. INPUT CONTROL–The command input device will always be the TTY when the program is first started. Input control may be passed to the tape reader by typing TAPE (TA). In order for the TTY to regain control, the word KEYBOARD (KE) must be read by the tape reader. Alternatively, the program may be restarted at address 2000_8. Restarting at address 2 will not change the input control device assignment. Regardless of the input mode, all commands, comments, and responses will be printed on the TTY.

4-57. DIRECTIONS PRINTOUT–The WANT DIRECTIONS question will be asked only the first time the program is run after loading. If the program is restarted, that question is omitted, but a list of instructions may be obtained at any time by typing the command INSTRUCTIONS (IN) in response to the prompter.

4-58. CONDITIONS– The operating commands may be modified somewhat by setting or clearing certain conditions. There are three conditions:

PACER (P) – This condition causes all DAS measurements to be made in the paced mode. If P is not set, measurements are made in the unpaced mode.

DELAY (D) – This condition sets a desired delay between readings as a multiple of 10 microseconds, see Table 4-8.

REPEAT (R) – This condition allows the DAS to be put in a continuous looping condition and is intended primarily to be a troubleshooting aid. See Table 4-8.

4-59. Conditions may be set by typing SET followed by the condition to be set; i.e., SET PACER or SET P. Conditions may be cleared by typing CLEAR followed by the condition to be cleared. Typing CLEAR ALL (CLEAR A) will cause all conditions that are set to be cleared. The conditions which are currently set may be determined by typing CONDITIONS (CO).

4-60. OPERATING COMMANDS–The commands which cause DAS operations are described in Table 4-8 and Figure 4-5. The commands are: NORMALIZE (NO), DISPLAY (DI), HISTOGRAM (HI), SINGLE CHANNEL (SI), TWO CHANNEL (TW), and SEQUENTIAL (SE). Each time the same test is reprogrammed with different parameters, all the parameters must be entered. For example, if the Single Channel mode was programmed and the same test is desired on another channel, the number of readings and channel of interest must be reentered.

4-61. REPEAT COMMAND–Typing REPEAT (RE) causes the last command to be executed again.

```
91000A SELECT CODE= 26
TAPE-RDR SELECT CODE= 16

91000A VERIF 10/31/73
WANT DIRECTIONS? YE


1-200 RDGS TOTAL UNLESS NOTED

A PROMPTER IS ISSUED:

>

RESPOND WITH:

   SINGLE CH = ONE CH
      TWO CH = ALTERNATING CHS
  SEQUENTIAL = FROM START CH
   HISTOGRAM = 1-32767 RDGS ON 1 CH ARE CATEGORIZED
     DISPLAY = LOOP ON 1 CH, DISPLAY RDGS IN B OR SW REG
               AVERAGE=YES: 16 WD AVG; BIT 0 (LSB)=0.3125MV
               AVERAGE=NO: DISPLAY EACH RDG; BIT 4 (LSB)=5.0MV
      REPEAT = REPEAT LAST TEST AS SPECIFIED
        LIST = LIST ANY PART OF DATA BUFFER
   NORMALIZE = ISSUE SYSTEM NORMALIZE
  CONDITIONS = LIST COND THAT ARE SET
INSTRUCTIONS = GIVE BRIEF INSTRUCTIONS
        TAPE = INPUT COMMANDS FROM TAPE-RDR
    KEYBOARD = INPUT COMMANDS FROM KEYBD
           * = COMMENT - IGNORE LINE

CONDITIONS:

SET DELAY   (LIMITS SCAN RATE)
SET PACER   (OVERRIDES DELAY)
SET REPEAT

CLEAR DELAY
CLEAR PACER
CLEAR REPEAT
CLEAR ALL   (CLEARS ALL COND)

NOTES:

SW15 = 1 CAUSES EXIT FROM LIST

ABORT REQUEST WITH NEG # (REPEAT DISABLED)

ABORT A TEST; EXIT REPEAT OR DISPLAY WITH ANY KEYBD KEY (LIST DISABLED)
```

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Figure 4-6. Sample Printout of Verification Instructions

4-62. LISTING DATA–The SINGLE CHANNEL, TWO CHANNEL, and SEQUENTIAL commands are limited to a total of 200 readings each because all of the readings must be stored in a 200-word data buffer. The LIST (LI) command allows the operator access to the buffer. After typing LIST, the program will respond with FIRST,LAST = . The operator should enter the first and last reading desired and the program will list all entries between these numbers (inclusive). It should be noted that the numbers entered correspond to the lines of the buffer itself and are not channel addresses. If the last test was HISTOGRAM, requesting LIST causes the histogram results to be repeated. List is not available after Display, or with the REPEAT condition set, or whenever a test is aborted while executing. To exit from the test mode, set switch 15 = "1".

4-63 ABORTING A TEST – A test can be aborted in two ways before it has run to completion. A negative number (i.e., -1 to -9) is entered as an answer to a question expecting a number; or, the word ABORT (AB) can be typed as an answer to a question expecting YES or NO. If List is requested after the test has been aborted, measurements from the previous test are listed. Repeat is not available after a test has been aborted. To abort a test while it is executing, simply hit any teleprinter key. When control is switched to a tape reader other than the teleprinter tape reader, the keyboard may still be used to abort a test while it is executing. However, if the tape reader select code question was answered with a 0 allowing punched tape control through the TTY, this abort feature is not available; to abort a test the computer must be halted and then restarted.

4-64. RESTARTING– The program may be restarted at either address 2 or 2000_8. Restarting at address 2000_8 causes all conditions previously set to be cleared and sets input control to the TTY (the TTY I/O select code must again be placed in the switch register). Restarting at address 2 causes all conditions to remain set or reset as they were and does not change the input control device (the program does not read the switch register). The program will list the conditions currently set.

4-65. INPUT ERRORS–*FMT indicates a format error has occurred; restart is not necessary, the program will print ? and ask the question again. *FMT will generally occur if an invalid number sequence is entered as one of operator responses. A method of avoiding invalid number sequences is to use a blank space as a separator rather than a comma.

4-66. COMMENTS – The subsystem test can be documented by using the asterisk character (*) following the prompter (>). When used, everything between the * and CR/LF becomes a comment and is ignored by the verification program. For example:

```
>*DATE – 7/15/73. THIS IS TEST NO. 7
>*91000A IN I/O SLOT 12
```

4-67. The subsystem test can also be documented with comments following the parameter entries on the same line. For example:

```
>SEQ SCAN STARTING ON CHANNEL 0

NO = 64 USING AUTO-RESET

1ST CH

CHANNEL = 0

DIFF? NO-CHANS ARE SINGLE ENDED

RDGS TAKEN

>
```

4-68. CHANNEL ADDRESSING–Consideration must be given to single-ended or differential inputs when adressing channels. Differential inputs are addressed as: 0,2,4 . . . 14, while single-ended inputs are addressed as 0,1,2,3,4 . . . 15.

4-69. DATA PRINTOUT FORMAT–When data is printed out in the Single Channel, Two Channel, or Histogram mode, the printout has the meaning:

AVG = average of all readings for that channel
PP = peak-to-peak, or the difference between the highest and lowest reading
HI = highest reading of all readings taken
LO = lowest reading of all readings taken (most negative)

$$RMS = \sqrt{\frac{\sum_{i=1}^{N}(Ri - AVG)^2}{N}}$$

which is the square root of the sum of the squares of the difference between each reading and the average, divided by the number of readings. R_i is each reading.

A large RMS value is an indication of a noisy channel, while a low RMS value is an indication of a quiet channel.

4-70. PERFORMANCE TEST

4-71. Subsystem power should be applied at least one hour before performing the test to allow sufficient warm-up time. The first test is the sequential scan of all channels in the subsystem. This test allows the user to check all known inputs for accuracy, and test the sequential mode circuitry.

NOTE

The operator responses are underlined and only examples; actual responses should be appropriate to the particular system being used.

>SEQUENTIAL

NO = 16

1ST CH

CHANNEL = 0

DIFF? NO

RDGS TAKEN

>LIST

START, FINISH = 116

4-72. Compare the voltages listed to the known inputs. The values should be within the specified tolerances listed in Table 1-1.

4-73. The random mode circuitry is tested next using the single-channel, one-reading mode.

>SINGLE CHANNEL

NO = 1

CHANNEL = 4

(data printed here)

4-74. To test the subsystem's digitize mode circuitry, use single-channel with several readings.

>SINGLE CHANNEL

NO = 200

CHANNEL = 4

(data printed here)

4-75. AUTOMATIC RESET TEST

4-76. The AUTOMATIC RESET FEATURE is tested using the sequential scan. Eight channels are selected that are in sequential order and should have different input levels. The channels are then scanned twice and the readings checked for repeat.

>SEQUENTIAL

NO = 16

1ST CH

CHANNEL = 8

DIFF? NO

RDGS TAKEN

>LIST

START, FINISH = 116

4-77. The list of voltages produced by the above LIST command corresponds to the channel sequence: channel 9, channel 10, . . . channel 16, channel 9, channel 10, . . . channel 16.

4-78. PACED MODE TEST

4-79. Paced mode operation can be verified by using an external pulse generator connected to the pace pulse input and a wristwatch to time the pace pulses. Set the pulse generator for 1-second pace pulses and take 20 readings on a single channel. At the end of 20 seconds the verification program will return the requested data. Proceed as follows:

a. Set the pulse generator for a +5-volt pulse 1.5 μsec wide.
b. Adjust the repetition rate to 1 second.

Enter the following program.

>SET PACER

>SINGLE CHANNEL

NO = 20

CHANNEL = 0 (Do not type CR/LF)

4-80. After entering the channel number above, type CR. Observe the second hand on the watch and type LF. After a

lapse of 20 seconds the TTY will print the data from the 20 paced readings.

4-81. HISTOGRAM TEST

4-82. Accuracy and noise specifications on any HP 91000A channel can be checked using the Histogram mode. The operator can request from 1 to 32767 readings, the greater the number of readings the more accurate the evaluation. The program takes each measurement and remembers the value of the reading. As each subsequent measurement is taken the program determines if it is the same as one of the previous readings, or slightly different. If the measurement is the same as one previously taken, the number of measurements counter for that measurement is incremented. If the measurement is different a new counter is established. Using this procedure of counting the number of readings at a particular value, the program will establish up to 20 counters, or more accurately, histogram cells. The end result is a histogram similar to the example shown in Figure 4-7.

4-83. The noise specification of the subsystem is based on 3-sigma limits and it can be verified with the Histogram mode. If 30,000 readings are requested, up to 80 of the worst readings can be discarded. The remainder must be within the subsystem specifications as defined in Table 1-1.

4-84. The Histogram mode can be continuously repeated with data printout by using the Set Repeat mode. This provides the user with a continuous evaluation of noise on any one channel. By setting switch register switch 15 = "1", only the average is printed, all other data printout is suppressed.

THREE HISTOGRAMS SHOWING RESULTS OF 10,000 READINGS ON CHANNEL Ø.

```
>HI
 NO= 10000
 CHANNEL = Ø
 AVG=-10.169319 PP=    .075001 HI=-10.164999 LO=-10.240000 RMS= .00549952
 -10.240000             52
 -10.170000           7857
 -10.164999           2091

>HI
 NO= 10000
 CHANNEL = Ø
 AVG=-10.169390 PP=    .075001 HI=-10.164999 LO=-10.240000 RMS= .00631543
 -10.240000             70
 -10.235001              1
 -10.170000           7716
 -10.164999           2213

>HI
 NO= 10000
 CHANNEL = Ø
 AVG= -5.076177 PP=    .015000 HI= -5.065000 LO= -5.080000 RMS= .00230187
  -5.080000           2511
  -5.075000           7333
  -5.070000            154
  -5.065000              2
```

HISTOGRAM SHOWING RESULTS OF SEQUENTIAL SCAN, 16 READINGS STARTING AT CHANNEL 0, DIFFERENTIAL MODE, LISTED IN ORDER.

```
>SE
 NO= 16
 1ST CH
 CHANNEL = Ø
 DIFF? YE
 RDGS TAKEN
>LI
 START,FINISH= 1,16

  -5.075000
  -5.070000
  -5.070000
  -5.070000
  -5.075000
  -5.075000
  -5.075000
  -5.070000
  -5.075000
  -5.070000
  -5.075000
  -5.075000
  -5.075000
  -5.070000
  -5.075000
  -5.075000
```

TP91000-32-1

Figure 4-7. Sample Printout of Histogram

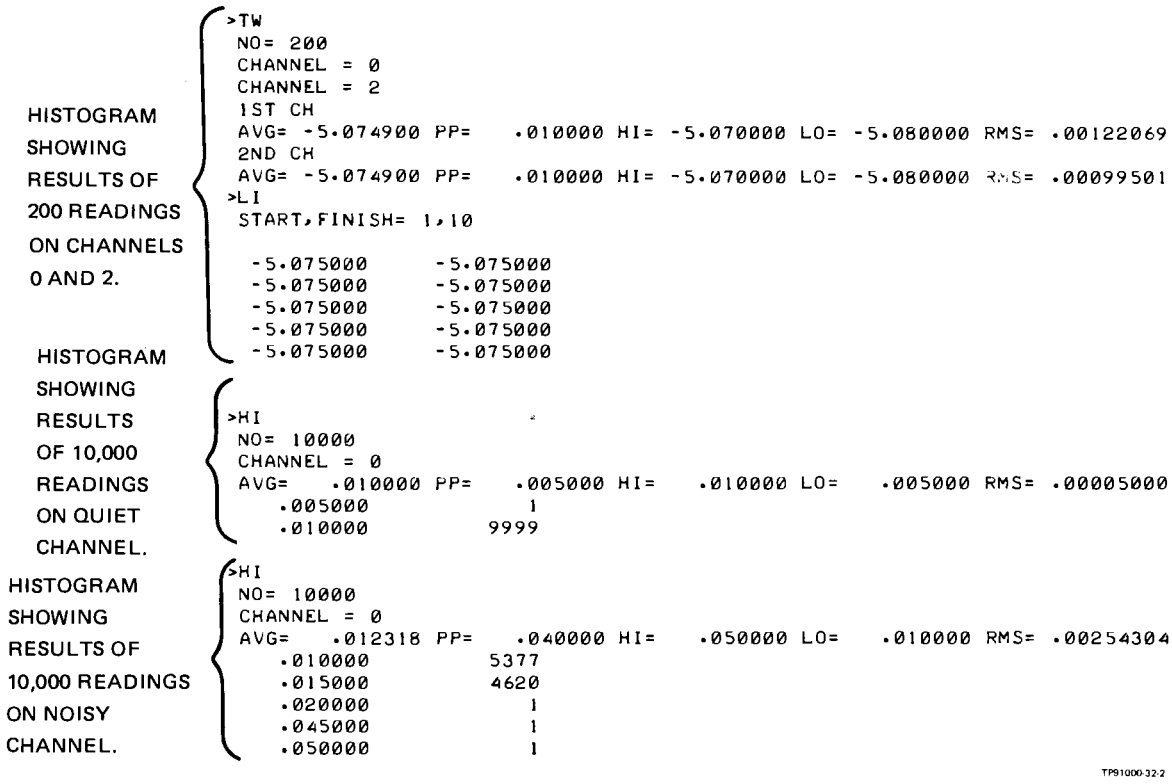


Figure 4-7. Sample Printout of Histogram (Continued)

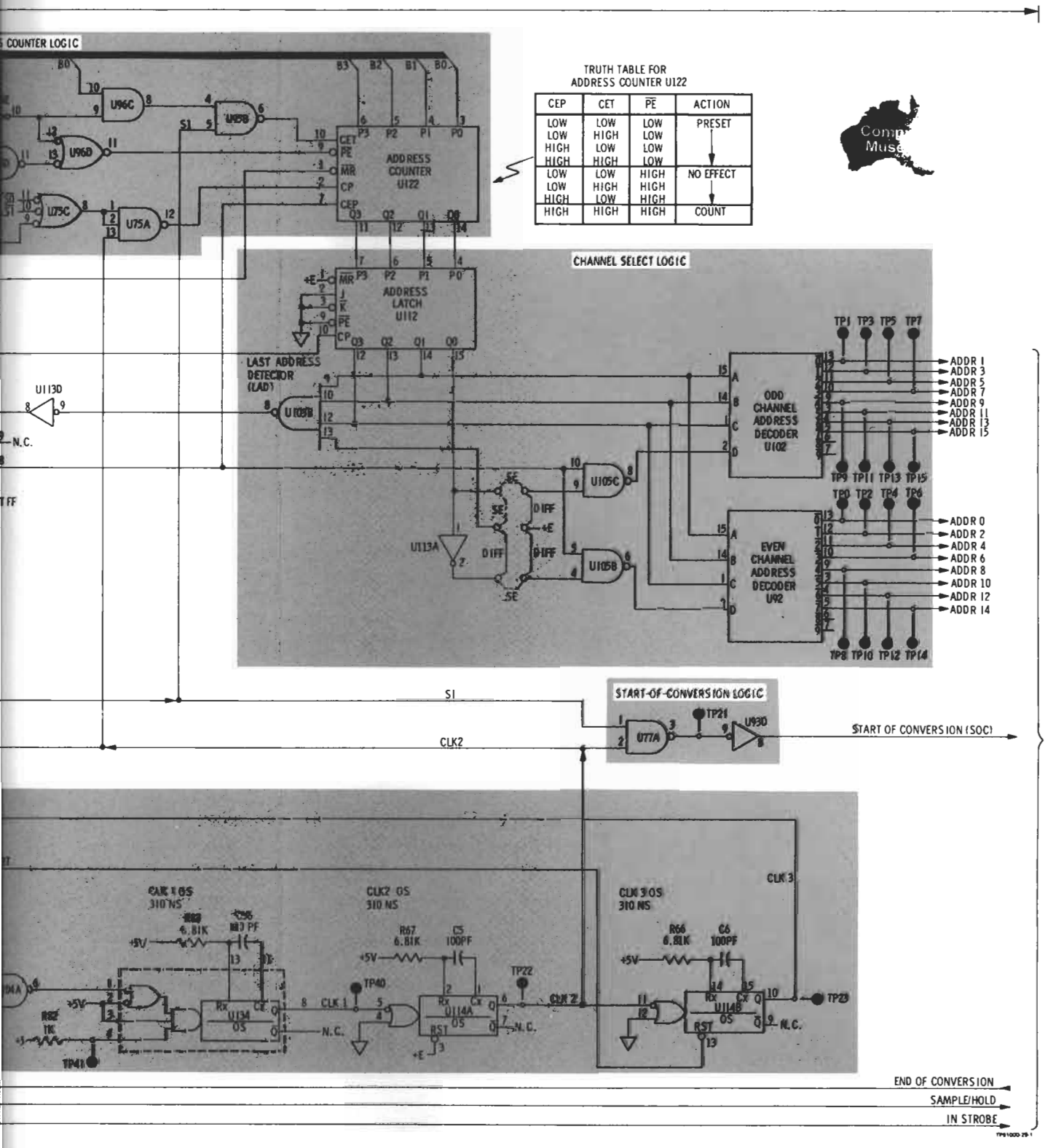
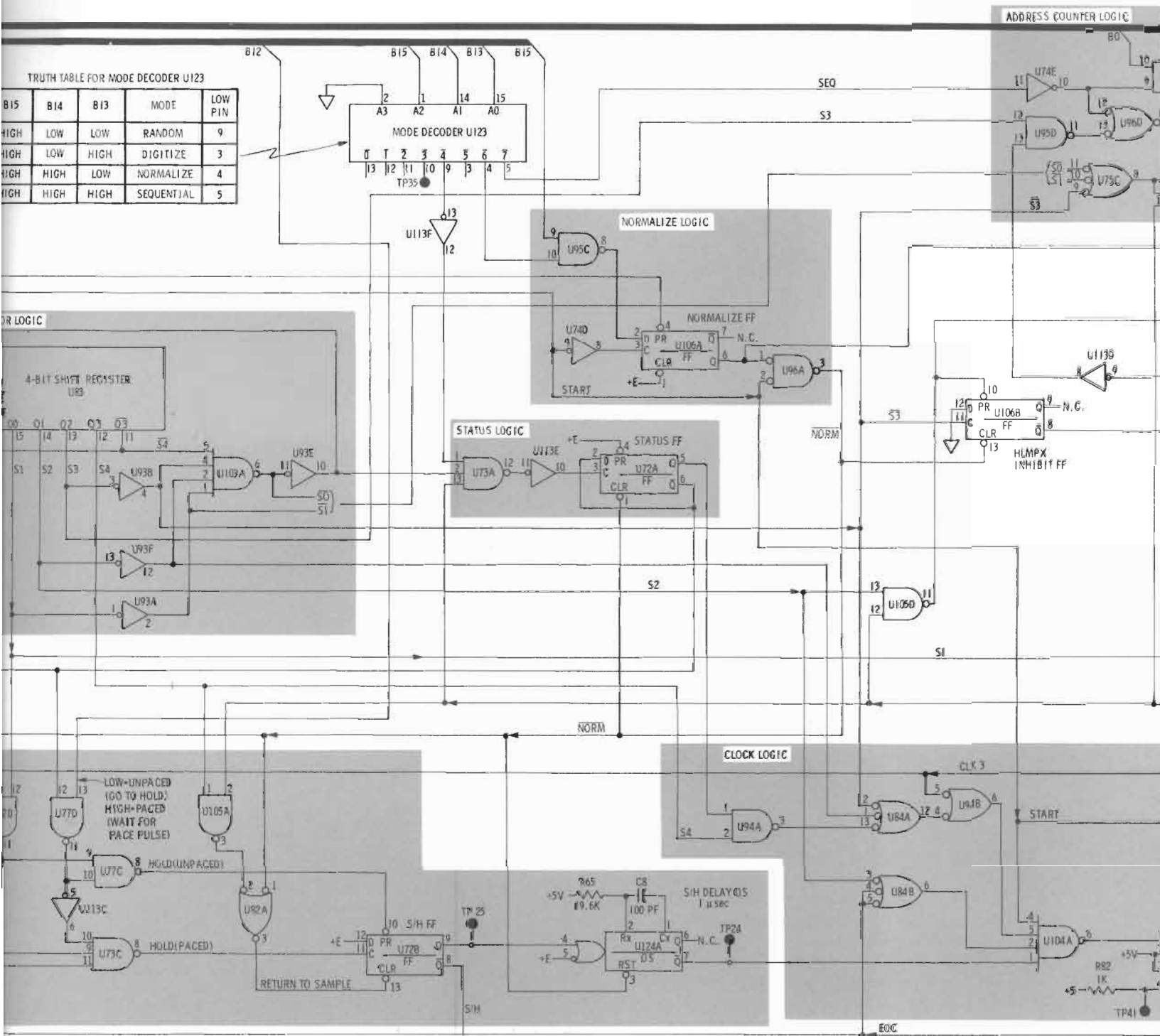


Figure 4-9. HP 91000A Schematic Diagram (Sheet 1 of 2)

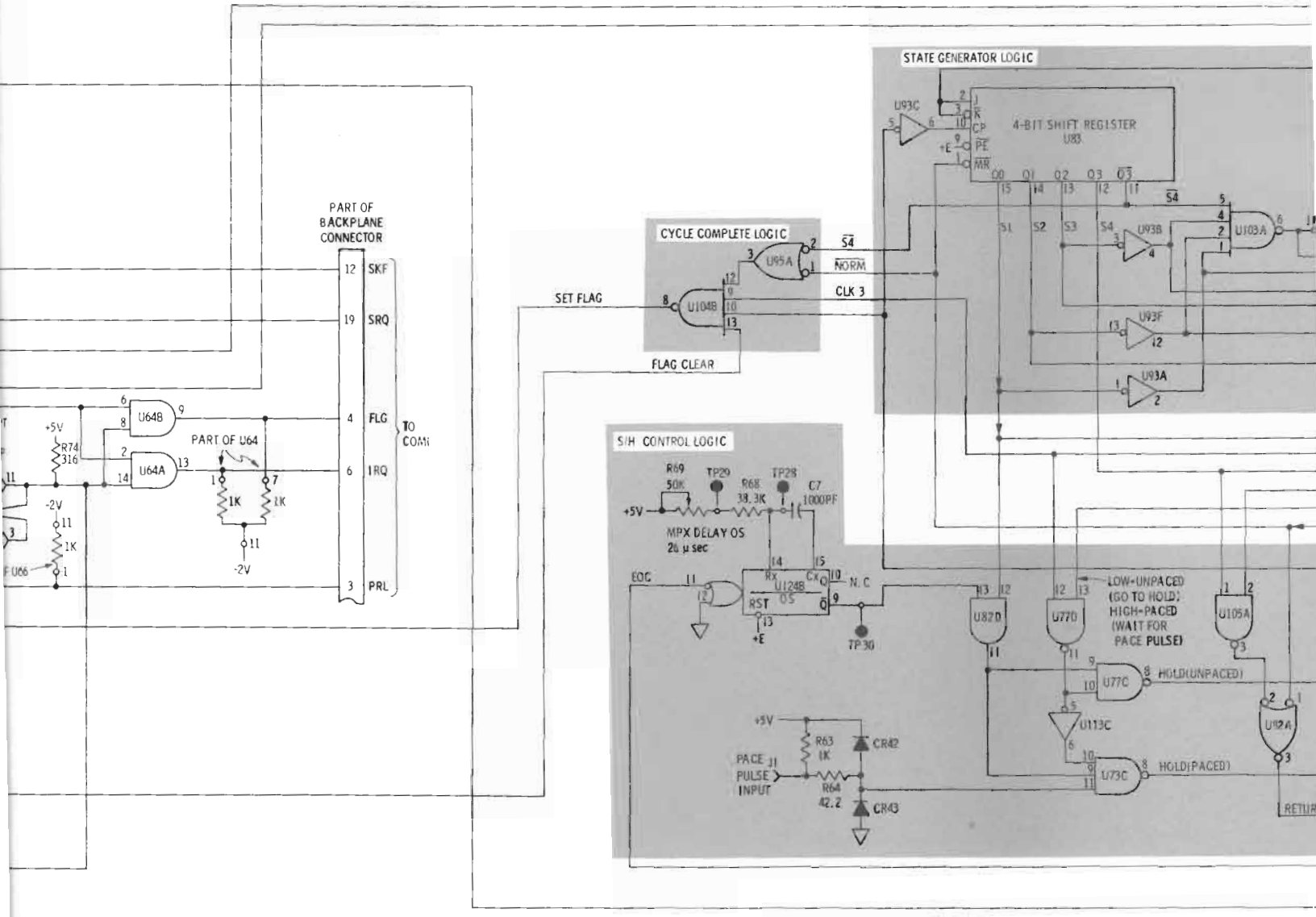
TRUTH TABLE FOR MODE DECODER U123

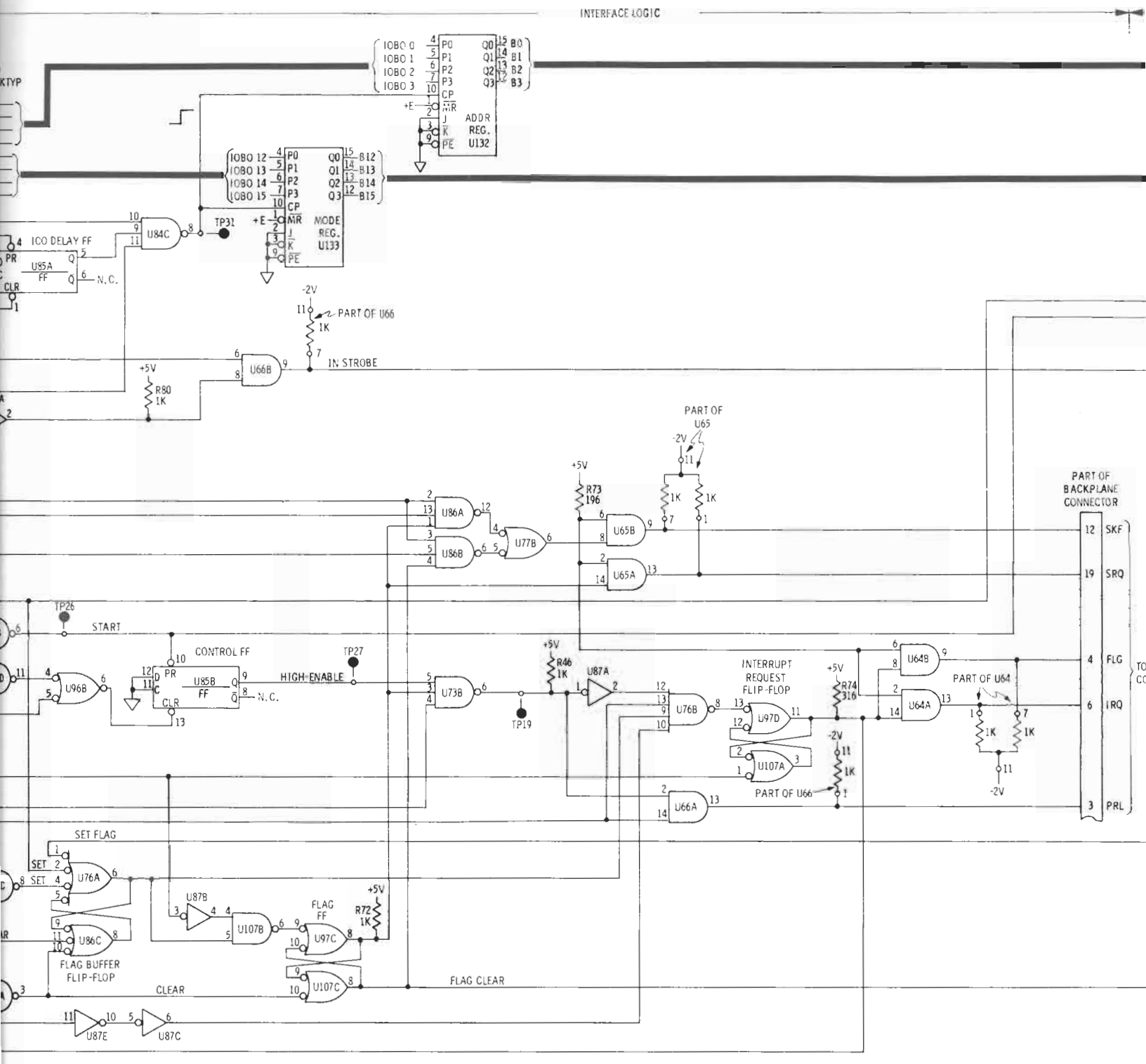
B15	B14	B13	MODE	LOW PIN
HIGH	LOW	LOW	RANDOM	9
HIGH	LOW	HIGH	DIGITIZE	3
HIGH	HIGH	LOW	NORMALIZE	4
HIGH	HIGH	HIGH	SEQUENTIAL	5

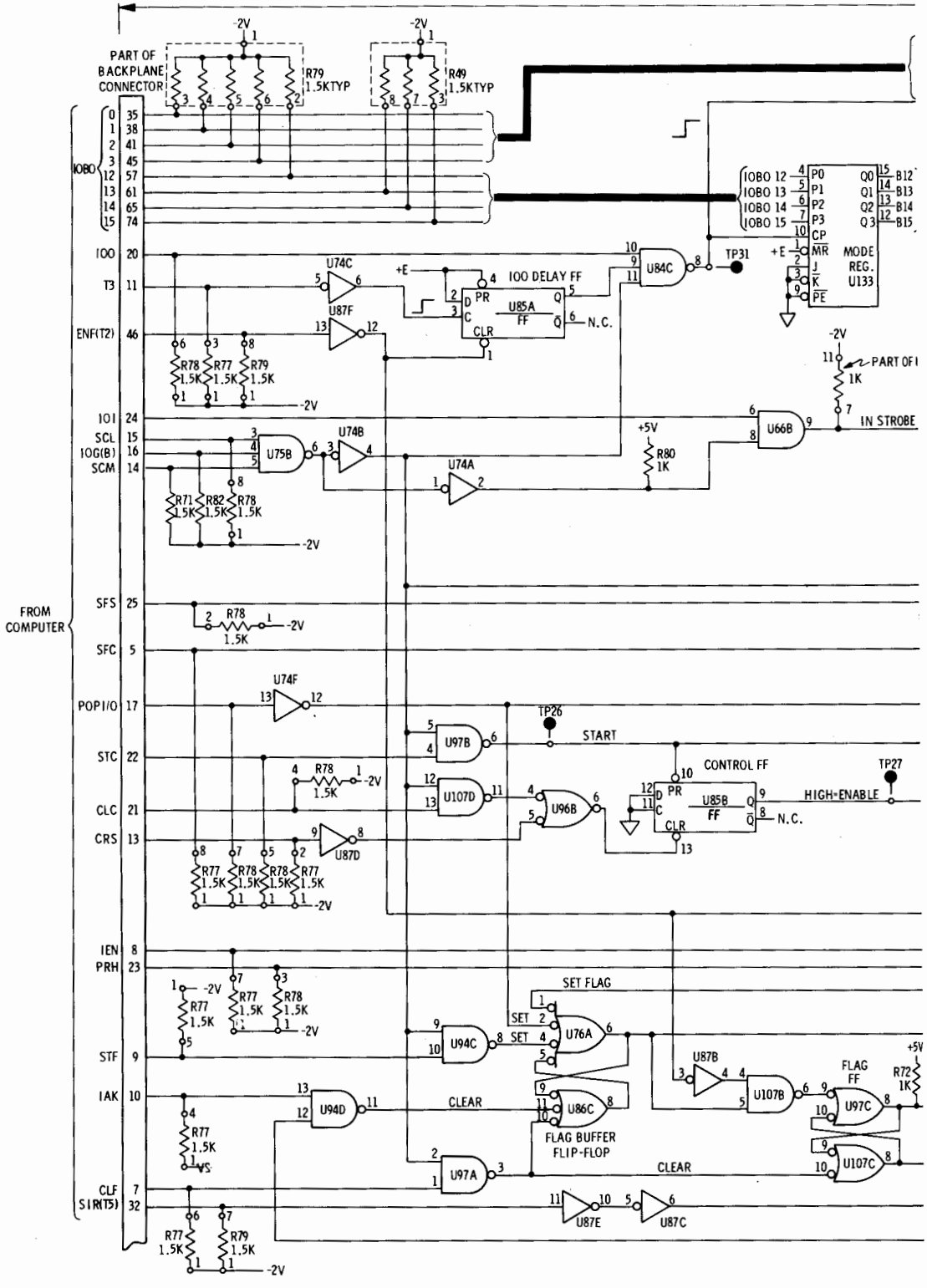


TRUTH TABLE FOR MODE DECODER U123

B15	B14	B13	MODE	LOW PIN
HIGH	LOW	LOW	RANDOM	9
HIGH	LOW	HIGH	DIGITIZE	3
HIGH	HIGH	LOW	NORMALIZE	4
HIGH	HIGH	HIGH	SEQUENTIAL	5




INTERFACE LOGIC
IOBO 0
IOBO 1
IOBO 2
IOBO 3
P0
P1
P2
P3
CP
MR
J
K
PE
ADDR REG. U132
Q0
Q1
Q2
Q3
B0
B1
B2
B3
+E
IOBO 12
IOBO 13
IOBO 14
IOBO 15
MODE REG. U133
B12
B13
B14
B15
TP31
U84C
ICO DELAY FF
U85A FF
N.C.
-2V
PART OF U66
1K
IN STROBE
U66B
+5V
R80 1K
PART OF U65
R73 196
U65B
U65A
U86A
U86B
U77B
PART OF BACKPLANE CONNECTOR
SKF
SRQ
FLG
IRQ
PRL
TP26
START
CONTROL FF
U96B
U85B FF
HIGH-ENABLE
TP27
TP19
U73B
R46 1K
U87A
INTERRUPT REQUEST FLIP-FLOP
U97D
U107A
R74 316
U76B
U66A
U64B
U64A
PART OF U64
SET FLAG
SET
U76A
U86C
FLAG BUFFER FLIP-FLOP
U87B
U107B
FLAG FF
U97C
U107C
R72 1K
CLEAR
FLAG CLEAR
U87E
U87C


PART OF BACKPLANE CONNECTOR
-2V
R79 1.5KTYP
R49 1.5KTYP
IOBO
IOO
T3
ENF(T2)
IOI
SCL
IOG(B)
SCM
SFS
SFC
POPI/O
STC
CLC
CRS
IEN
PRH
STF
IAK
CLF
SIR(T5)
FROM COMPUTER
U74C
U87F
U74B
U75B
U74A
U74F
U87D
U84C
U85A FF
100 DELAY FF
TP31
MODE REG. U133
IOBO 12
IOBO 13
IOBO 14
IOBO 15
B12
B13
B14
B15
PART OF I
1K
IN STROBE
U66B
+5V
R80 1K
TP26
START
U97B
U107D
U96B
CONTROL FF
U85B FF
HIGH-ENABLE
TP27
N.C.
SET FLAG
U76A
U94C
U94D
CLEAR
U86C
FLAG BUFFER FLIP-FLOP
U97A
U87B
U107B
FLAG FF
U97C
U107C
R72 1K
U87E
U87C
R78 1.5K
R77 1.5K
R71 1.5K
R82 1.5K
R79 1.5K

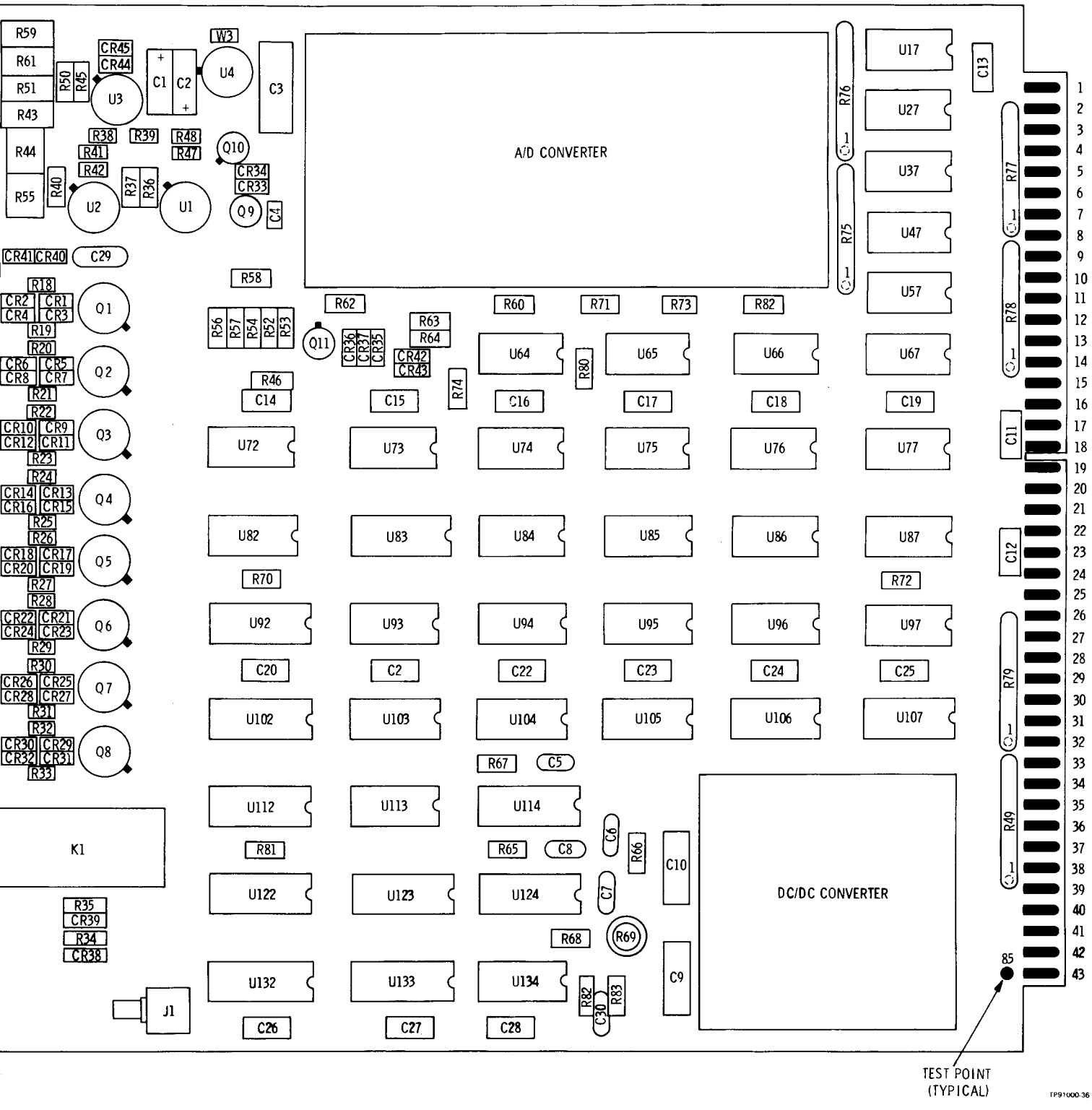
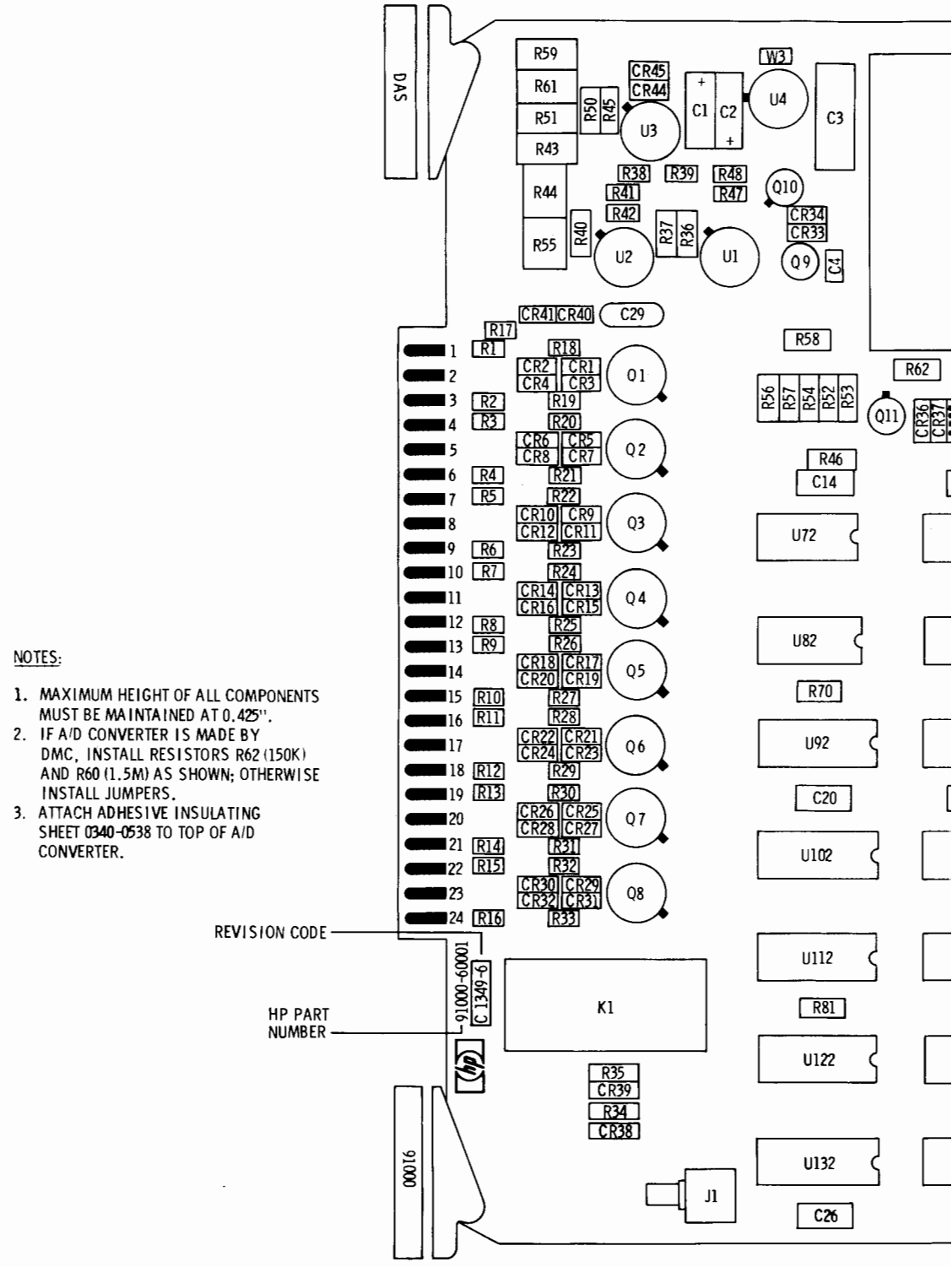


Figure 4-8. HP 91000A Parts Location Diagram


NOTES:
1. MAXIMUM HEIGHT OF ALL COMPONENTS MUST BE MAINTAINED AT 0.425".
2. IF A/D CONVERTER IS MADE BY DMC, INSTALL RESISTORS R62 (150K) AND R60 (1.5M) AS SHOWN; OTHERWISE INSTALL JUMPERS.
3. ATTACH ADHESIVE INSULATING SHEET 0340-0538 TO TOP OF A/D CONVERTER.
REVISION CODE
HP PART NUMBER
91000-60001
C1349-6
DAS
91000
J1
K1
U1
U2
U3
U4
U72
U82
U92
U102
U112
U122
U132
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
C1
C2
C3
C4
C14
C20
C26
C29
W3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R50
R51
R52
R53
R54
R55
R56
R57
R58
R59
R61
R62
R70
R81
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
CR21
CR22
CR23
CR24
CR25
CR26
CR27
CR28
CR29
CR30
CR31
CR32
CR33
CR34
CR38
CR39
CR40
CR41
CR44
CR45

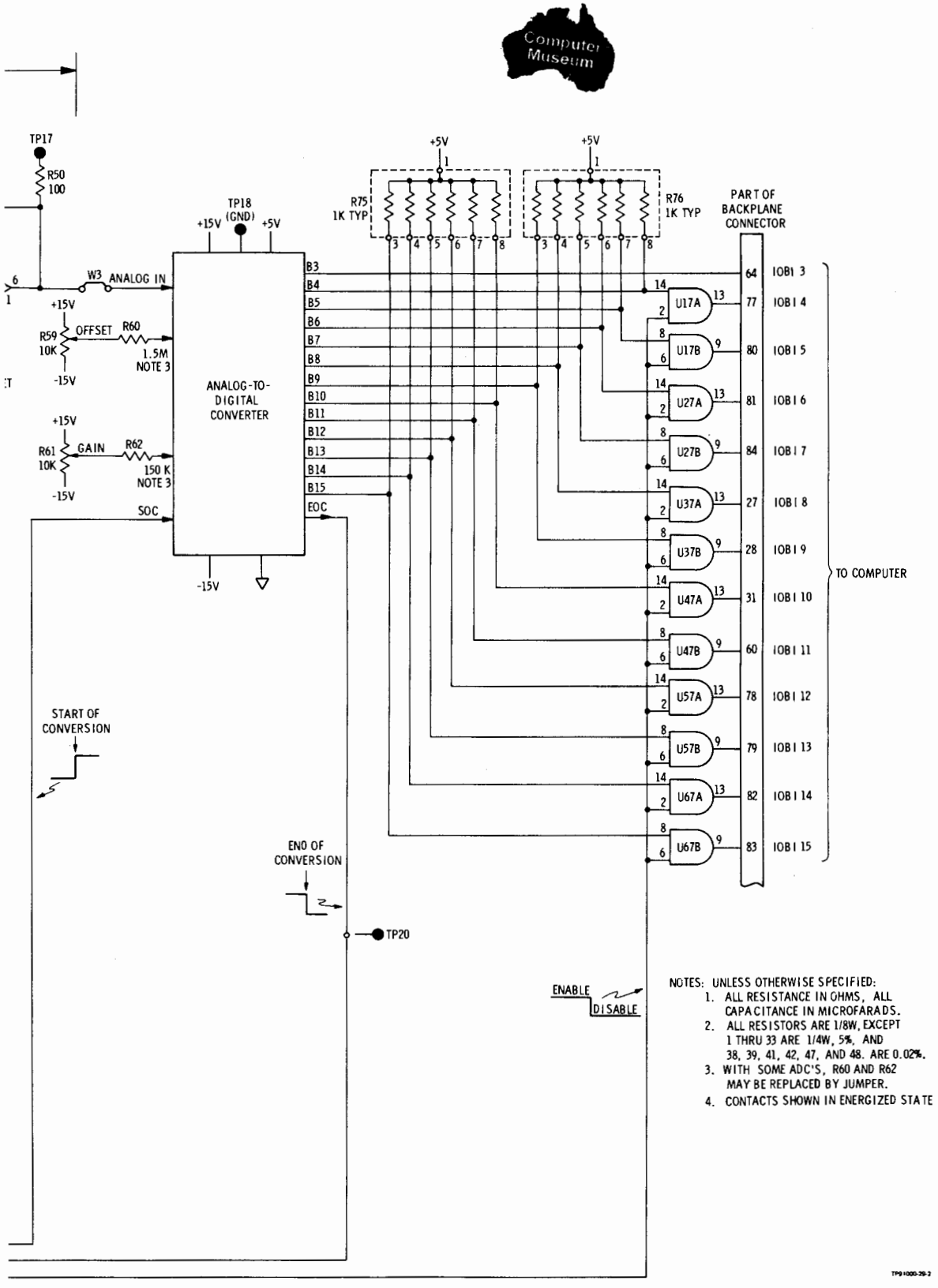
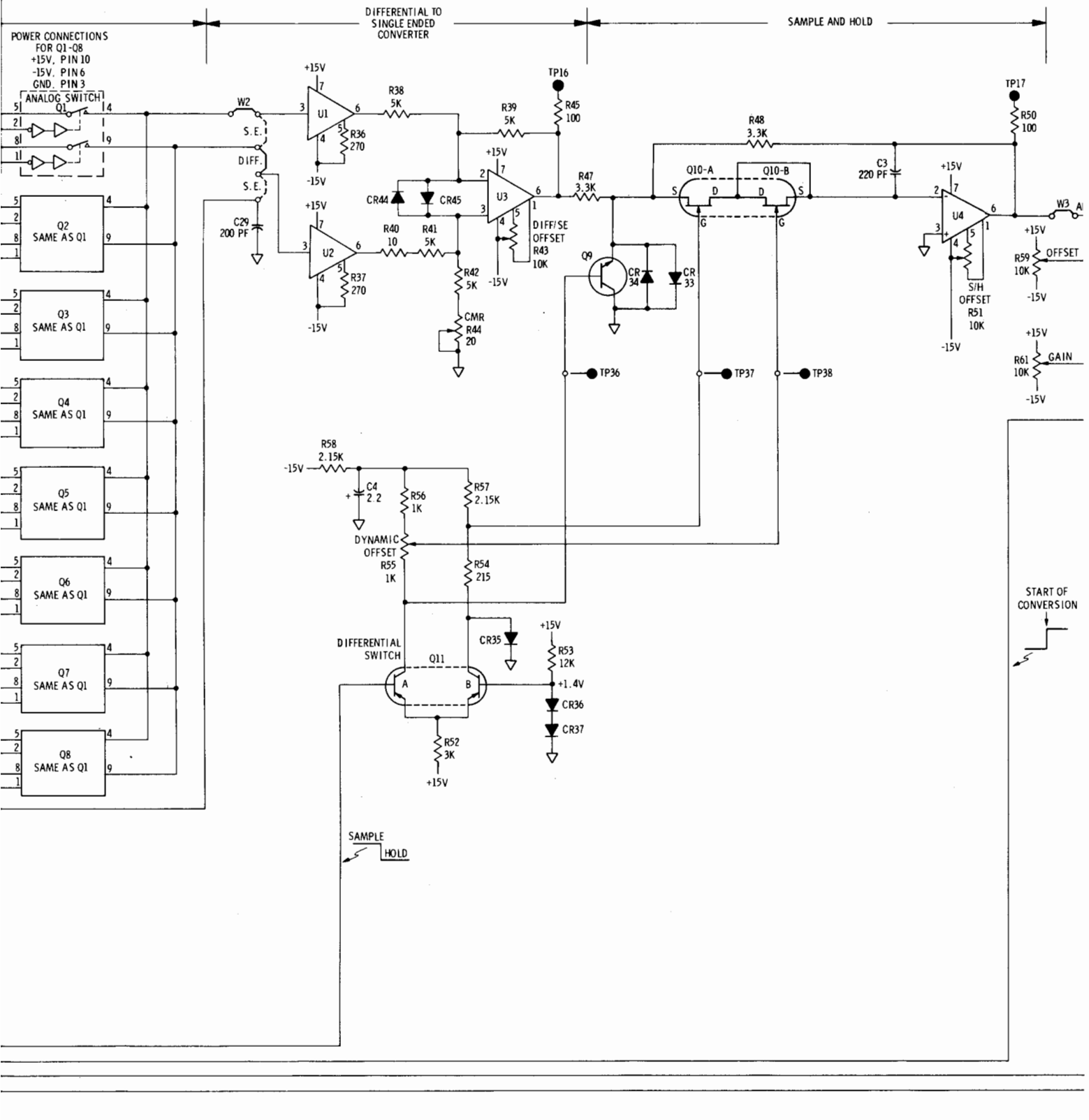
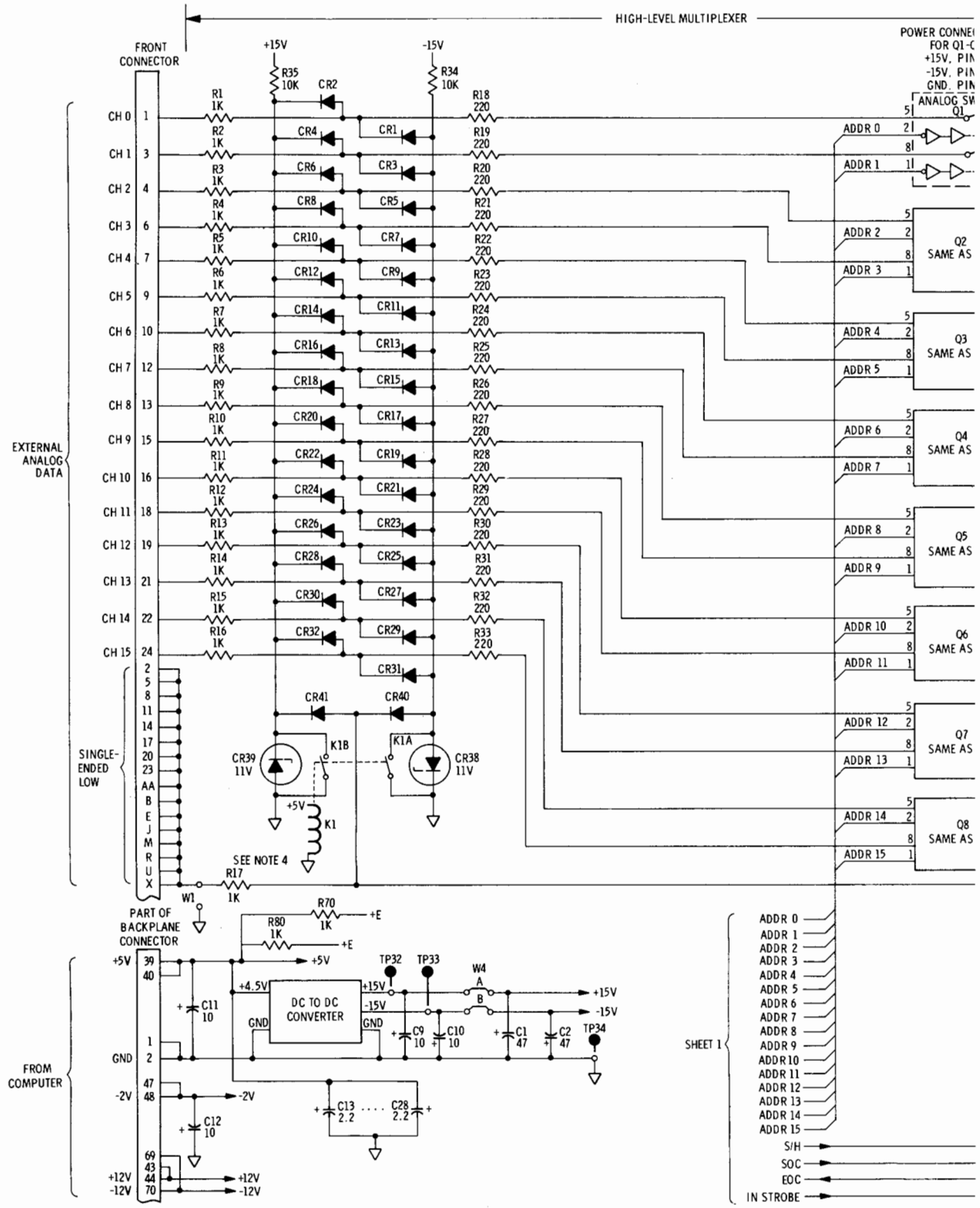


Figure 4-9. HP 91000A Schematic Diagram (Sheet 2 of 2)


DIFFERENTIAL TO SINGLE ENDED CONVERTER
SAMPLE AND HOLD
POWER CONNECTIONS FOR Q1-Q8 +15V, PIN 10 -15V, PIN 6 GND, PIN 3
ANALOG SWITCH
Q1
Q2 SAME AS Q1
Q3 SAME AS Q1
Q4 SAME AS Q1
Q5 SAME AS Q1
Q6 SAME AS Q1
Q7 SAME AS Q1
Q8 SAME AS Q1
W2
S.E.
DIFF.
S.E.
C29 200 PF
U1
U2
U3
U4
R36 270
R37 270
R38 5K
R39 5K
R40 10
R41 5K
R42 5K
CMR R44 20
R43 10K DIFF/SE OFFSET
R45 100
R47 3.3K
R48 3.3K
CR44
CR45
Q9
CR 34
CR 33
Q10-A
Q10-B
C3 220 PF
R50 100
R59 10K OFFSET
R51 10K S/H OFFSET
R61 10K GAIN
W3
TP16
TP17
TP36
TP37
TP38
R58 2.15K
C4 2.2
R56 1K
R57 2.15K
DYNAMIC OFFSET R55 1K
R54 215
DIFFERENTIAL SWITCH
Q11
CR35
R53 12K
+1.4V
CR36
CR37
R52 3K
START OF CONVERSION
SAMPLE
HOLD
+15V
-15V

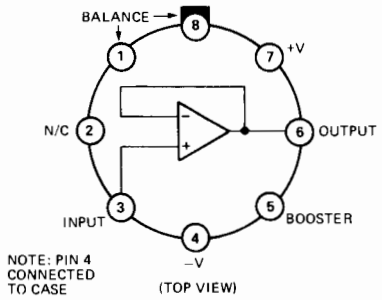

HIGH-LEVEL MULTIPLEXER
FRONT CONNECTOR
+15V
-15V
R35 10K
R34 10K
CR2
EXTERNAL ANALOG DATA
CH 0 1
CH 1 3
CH 2 4
CH 3 6
CH 4 7
CH 5 9
CH 6 10
CH 7 12
CH 8 13
CH 9 15
CH 10 16
CH 11 18
CH 12 19
CH 13 21
CH 14 22
CH 15 24
R1 1K
R2 1K
R3 1K
R4 1K
R5 1K
R6 1K
R7 1K
R8 1K
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
R16 1K
R17 1K
R18 220
R19 220
R20 220
R21 220
R22 220
R23 220
R24 220
R25 220
R26 220
R27 220
R28 220
R29 220
R30 220
R31 220
R32 220
R33 220
CR1
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
CR21
CR22
CR23
CR24
CR25
CR26
CR27
CR28
CR29
CR30
CR31
CR32
CR40
CR41
SINGLE-ENDED LOW
2 5 8 11 14 17 20 23 AA B E J M R U X
CR39 11V
CR38 11V
K1A
K1B
K1
+5V
SEE NOTE 4
W1
PART OF BACKPLANE CONNECTOR
R70 1K
+E
R80 1K
+E
FROM COMPUTER
+5V 39 40
GND 1 2
-2V 47 48
+12V 69 43 44
-12V 70
C11 10
C12 10
+4.5V
DC TO DC CONVERTER
GND
+15V
-15V
TP32
TP33
W4
A
B
C9 10
C10 10
C1 47
C2 47
TP34
C13 2.2 .... C28 2.2
POWER CONNE
FOR Q1-C
+15V, PIN
-15V, PIN
GND, PIN
ANALOG SW
Q1
ADDR 0
ADDR 1
ADDR 2
ADDR 3
ADDR 4
ADDR 5
ADDR 6
ADDR 7
ADDR 8
ADDR 9
ADDR 10
ADDR 11
ADDR 12
ADDR 13
ADDR 14
ADDR 15
Q2 SAME AS
Q3 SAME AS
Q4 SAME AS
Q5 SAME AS
Q6 SAME AS
Q7 SAME AS
Q8 SAME AS
SHEET 1
S/H
SOC
EOC
IN STROBE

1826-0021 **VOLTAGE FOLLOWER**

DESCRIPTION

Operational amplifier internally connected as a unity-gain non-inverting amplifier. Internal frequency compensation and provision for offset balancing are incorporated in unit.

CONNECTION DIAGRAM



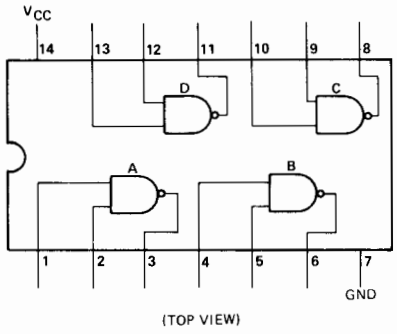
1820-0054 **QUAD 2-INPUT NAND GATE**

DESCRIPTION

Four independent 2-input NAND gates. Each gate can perform the NAND function or the NOR function.

For the NAND function, the output is low if both inputs are high. For the NOR function, the output is high if either input is low.

CONNECTION DIAGRAM



1820-0068 **TRIPLE 3-INPUT NAND GATE**

DESCRIPTION

Three independent 3-input NAND gates. Each gate can perform the NAND function or the NOR function.

For the NAND function, the output is low if all three inputs are high. For the NOR function, the output is high if any input is low.

CONNECTION DIAGRAM

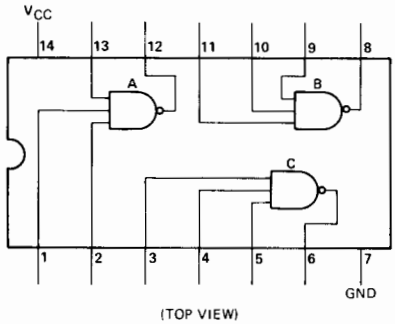


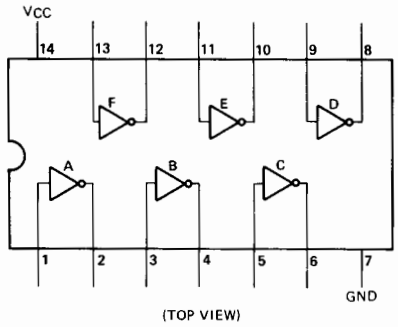
Figure 4-10. Integrated Circuits (Sheet 1 of 10)

1820-0174 **HEX INVERTER**

DESCRIPTION

Six independent logic inverters. Each output goes low if the corresponding input goes high, or high if the corresponding input goes low.

CONNECTION DIAGRAM



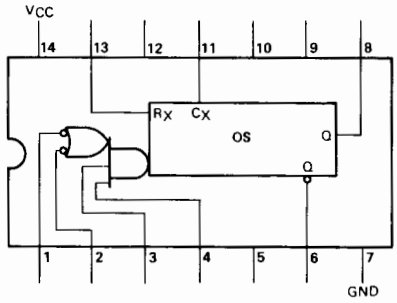
(TOP VIEW)

1820-0207 **RETRIGGERABLE ONE-SHOT**

DESCRIPTION

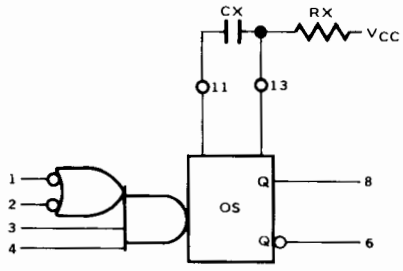
A one-shot with four inputs, two active high and two active low. This allows a choice of leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. Duration and accuracy of output pulse depend upon value of external timing capacitor (C_X) and external timing resistor (R_X). When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to change. An input cycle time shorter than the output cycle time will retrigger the one-shot and result in a continuous high Q output. Retriggering may be inhibited by tying the Q output to an active low input. Active pullups are provided on the outputs for good drive capability into capacitive loads.

CONNECTION DIAGRAM



(TOP VIEW)

LOGIC DIAGRAM



V_{CC} = PIN 14, GND = PIN 7

Figure 4-10. Integrated Circuits (Sheet 2 of 10)

1820-0134 **4 BIT SHIFT REGISTER**

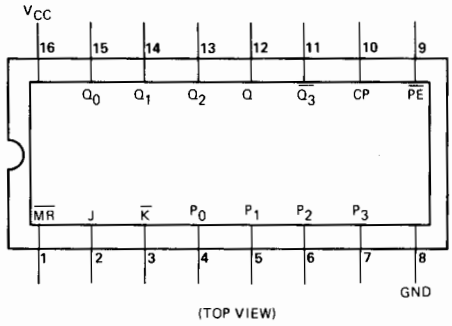
DESCRIPTION

A 4-bit shift register. As a high-speed multi-functional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The functional characteristics of the register are:

1. A JK input is provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for most general applications. At the same time the simple D-type input most appropriate for a shift register can be easily obtained by tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logic operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the parallel enable input is low. With the parallel enable input low, the element appears as four common clocked D flip-flops. When the parallel enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip-flops occurs after the low to high transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous reset input allows all stages to be set to zero independent of any other input condition.

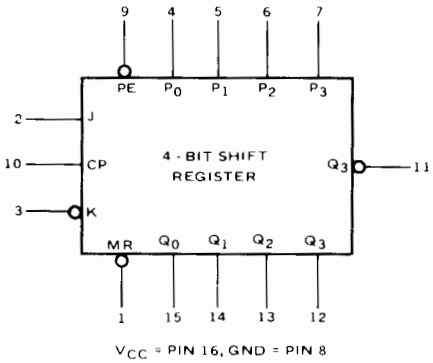
$\overline{MR}$ = Master reset
J = First stage J input
$\overline{K}$ = First stage K input
P_0, P_1, P_2, P_3 = Parallel inputs
Q_0, Q_1, Q_2, Q_3 = Parallel outputs
$\overline{Q}_3$ = Complementary last stage output
$\overline{CP}$ = Clock
$\overline{PE}$ = Parallel enable input

CONNECTION DIAGRAM



(TOP VIEW)

LOGIC DIAGRAM



V_{CC} = PIN 16, GND = PIN 8

Figure 4-10. Integrated Circuits (Sheet 3 of 10)

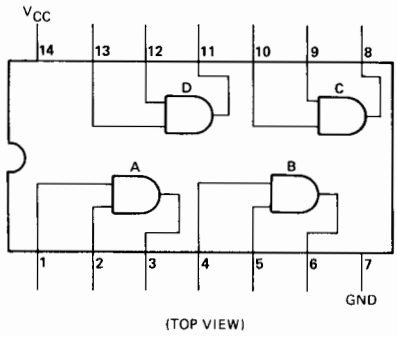
1820-0511 **QUAD 2-INPUT AND GATE**

DESCRIPTION

Four independent 2-input AND gates. Each gate can perform the AND function or the OR function.

For the AND function, the output is high if both inputs are high. For the OR function, the output is low if either input is low.

CONNECTION DIAGRAM



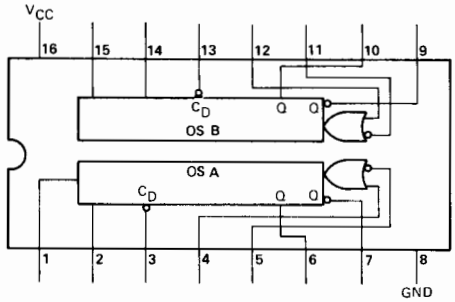
(TOP VIEW)

1820-0515 **DUAL RETRIGGERABLE RESETTABLE ONE-SHOT**

DESCRIPTION

Two independent low-power retriggerable resettable one-shots. Each one-shot can be triggered by a negative-going or a positive-going transition. Duration and accuracy of output pulse depend upon value of external timing capacitor C_X and external timing resistor R_X. Triggering is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the one-shot and result in a continuous true output. The output pulse may be terminated at any time by connecting the reset pin to logic low. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the $\overline{Q}$ output to the active low input or the Q output to the active high input.

CONNECTION DIAGRAM



(TOP VIEW)

LOGIC DIAGRAM

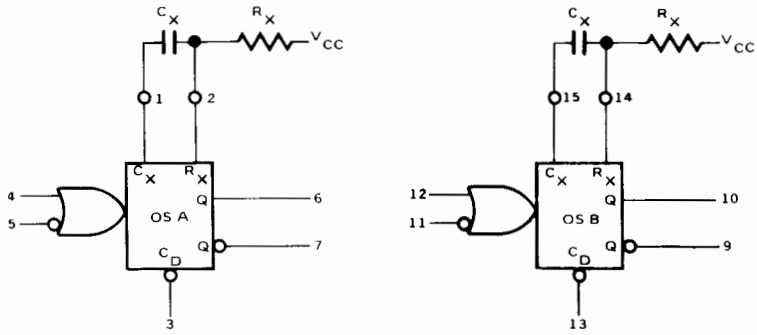


Figure 4-10. Integrated Circuits (Sheet 4 of 10)

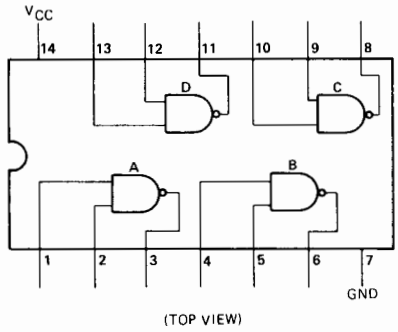
1820-0583 **QUAD 2-INPUT NAND GATE**

DESCRIPTION

Four independent low-power 2-input NAND gates. Each gate can perform the NAND function or the NOR function.

For the NAND function, the output is low if both inputs are high. For the NOR function, the output is high if either input is low.

CONNECTION DIAGRAM



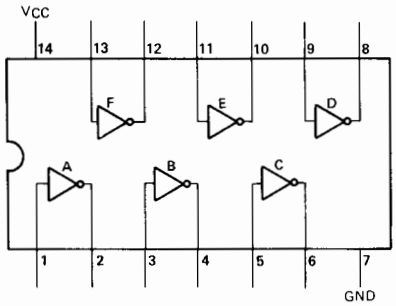
(TOP VIEW)

1820-0586 **HEX INVERTER**

DESCRIPTION

Six independent low-power logic inverters. Each output goes low if the corresponding input goes high, or high if the corresponding input goes low.

CONNECTION DIAGRAM



(TOP VIEW)

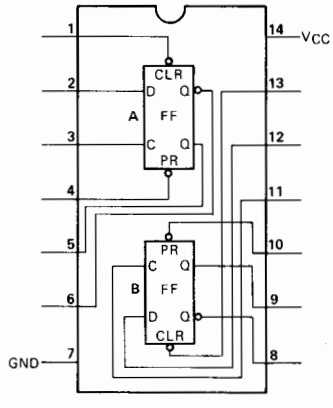
1820-0596 **DUAL D FLIP-FLOP**

DESCRIPTION

Two independent low-power D-type edge-triggered flip-flops. Information present on the D (data) input is transferred to the Q output on the positive-going transition of the clock input. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the clock. After the clock input threshold voltage has been passed, the D input is locked out. Low input to preset sets Q output high. Low input to clear sets Q output low. Preset and clear are independent of clock.

C = Clock input
D = Data input
PR = Preset
CLR = Clear

CONNECTION DIAGRAM



(TOP VIEW)

Figure 4-10. Integrated Circuits (Sheet 5 of 10)

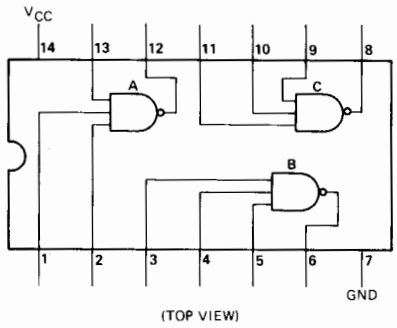
1820-0587 **TRIPLE 3-INPUT NAND GATE**

DESCRIPTION

Three independent low-power 3-input NAND gates. Each gate can perform the NAND function or the NOR function.

For the NAND function, the output is low if all three inputs are high. For the NOR function, the output is high if any input is low.

CONNECTION DIAGRAM



(TOP VIEW)

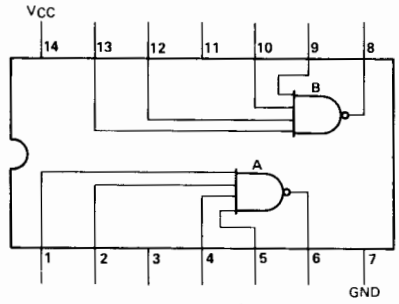
1820-0588 **DUAL 4-INPUT NAND GATE**

DESCRIPTION

Two independent low-power four-input NAND gates. Each gate can perform the NAND function or the NOR function.

For the NAND function, the output is low if all four inputs are high. For the NOR function, the output is high if any input is low.

CONNECTION DIAGRAM



(TOP VIEW)

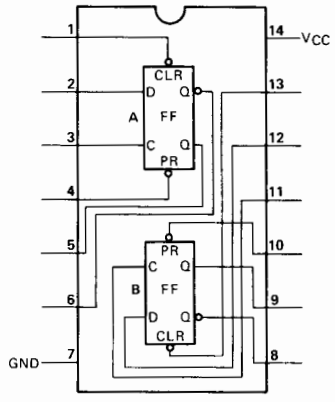
1820-0077 **DUAL D FLIP-FLOP**

DESCRIPTION

Two independent D-type edge-triggered flip-flops. Information present on the D (data) input is transferred to the Q output on the positive-going transition of the clock input. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the clock. After the clock input threshold voltage has been passed, the D input is locked out. Low input to preset sets Q output high. Low input to clear sets Q output low. Preset and clear are independent of clock.

C = Clock input
D = Data input
PR = Preset
CLR = Clear

CONNECTION DIAGRAM



(TOP VIEW)

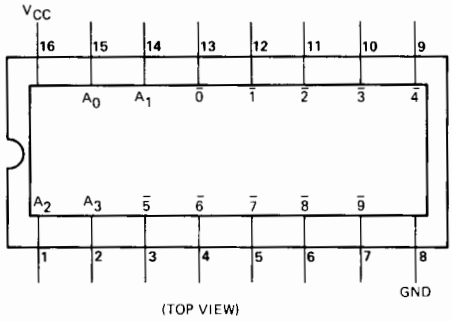
Figure 4-10. Integrated Circuits (Sheet 6 of 10)

1820-0627 **ONE-OF-TEN DECODER**

DESCRIPTION

A low-power one-of-ten decoder which accepts four active high BCD inputs, A_0 through A_3, and provides ten mutually exclusive low outputs, $\overline{0}$ through $\overline{9}$, as shown in the truth table. All outputs are high when a binary code greater than 9 is applied to the input. The most significant input, A_3, can be used as an inhibit if the decoder is used in a one-of-eight application.

CONNECTION DIAGRAM

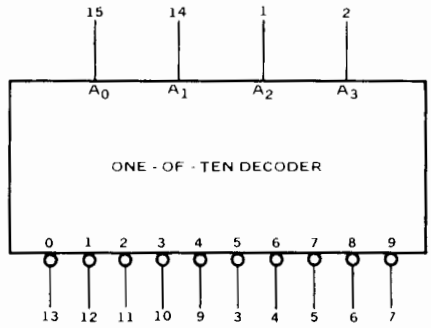


(TOP VIEW)

TRUTH TABLE

INPUT				OUTPUT									
A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC DIAGRAM



V_{CC} = PIN 16, GND = PIN 8

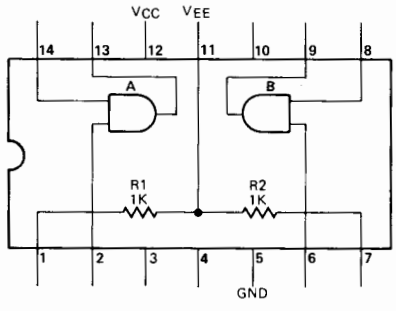
1820-0956 **DUAL 2-INPUT AND GATE**

DESCRIPTION

Two independent 2-input AND gates, each capable of performing the AND function or the OR function. The output is open-collector, and is normally tied to V_{EE} via an integral 1K resistor, R1 or R2.

For the AND function, the output is high if both inputs are high. For the OR function, the output is low if either input is low.

CONNECTION DIAGRAM



(TOP VIEW)

Figure 4-10. Integrated Circuits (Sheet 7 of 10)

1820-0778 **4-BIT BINARY COUNTER**

DESCRIPTION

A high-speed binary counter, fully synchronous, with the clock pulse driving four master/slave flip-flops in parallel through a clock buffer. During the low to high transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is high, the masters are inhibited and the master/slave data path remains established. During the high to low transition of the clock, the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic.

The three control inputs, parallel enable ($\overline{PE}$), count enable parallel (CEP), and count enable trickle (CET), select the mode of operation as shown in the tables below. When the conditions for counting are satisfied, the rising edge of a clock pulse will change the counters to the next state of the count sequence. The count mode is enabled when CEP and CET inputs and PE are high.

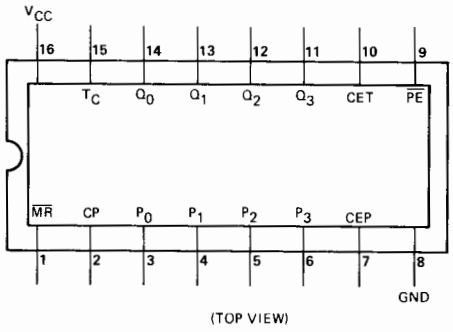
The counter can be synchronously preset from the four parallel inputs, (P_{0-3}) when PE is low. When the parallel enable and clock are low, each master of the flip-flop is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes high, the masters are inhibited and this information is transferred to the slaves and reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when low.

Terminal count is high when the counter is at terminal count and count enable trickle is high, as is shown in the logic equations. Without additional logic, multistage synchronous counting at high speeds is made possible with a speed lookahead technique utilizing the count enable and terminal count logic.

When low, the asynchronous master reset input ($\overline{MR}$) overrides all other inputs resetting the four outputs low.

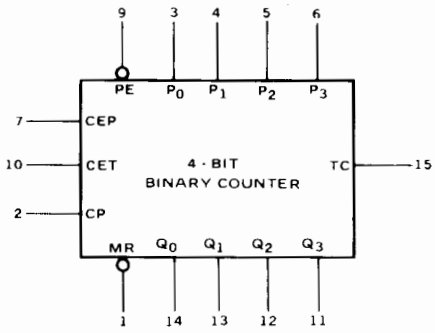
Conventional operation, as shown in the mode selection table, requires that the mode control inputs ($\overline{PE}$, CEP, CET) are stable while the clock is low. This is no constraint for a normal synchronous system where all signals are generated by the rising edge of the clock.

CONNECTION DIAGRAM



(TOP VIEW)

LOGIC DIAGRAM



V_{CC} = PIN 16, GND = PIN 8

$\overline{PE}$ = Parallel enable input
P_0, P_1, P_2, P_3 = Parallel inputs
CEP = Count enable parallel input
CET = Count enable trickle input
CP = Clock input
$\overline{MR}$ = Master reset input
Q_0, Q_1, Q_2, P_3 = Parallel outputs
TC = Terminal count outputs

MODE SELECTION

$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

$\overline{MR}$ = high

TERMINAL COUNT GENERATION

CET	$(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$

LOGIC EQUATIONS

COUNT ENABLE = CEP • CET • PE
$TC = CET \bullet Q_1 \bullet Q_2 \bullet Q_2 \bullet Q_3$
PRESET = $\overline{PE}$ • CP + (RISING CLOCK EDGE)
RESET = $\overline{MR}$

Figure 4-10. Integrated Circuits (Sheet 10 of 10)

SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION

5-2. This section contains a list of information for ordering replacement parts. Table 5-1 lists parts alphanumerically by reference designation. It also provides:

- HP part numbers.
- A general description of the parts.
- Typical manufacturing of the part expressed as a five-digit code (a list of manufacturers and their code numbers appears in Table 5-2).
- Manufacturer's part, stock, or drawing number.

5-3. ORDERING INFORMATION

5-4. When ordering replacement parts, each part must be identified by the Hewlett-Packard part number. To order a part that is not listed in the tables, include the following information:

- Instrument model number.
- Instrument serial number.
- Description of the part.
- Function and location of the part.

5-5. Address your order or inquiry to your local Hewlett-Packard Sales and Service Office (listed at the rear of this manual).

5-6. If parts are ordered from the original manufacturer, a complete description should be included with each manufacturer's part number. Many numbers listed are type numbers only, and descriptions are needed to facilitate selection.

Table 5-1. Replaceable Parts

Ref Des	HP Part No.	Description	Mfr Code	Mfr Part No.
	91000-60001	Data Acquisition Subsystem Card	28480	91000-60001
C1	0180-0479	Capacitor, 47 μF		
C2	Same as C1			
C3	0610-4199	Capacitor, 220 pF, 10%		
C4	0180-0478	Capacitor, 2.2 μF		
C5	0160-4139	Capacitor, 100 pF, mica		
C6	Same as C5			
C7	0160-3915	Capacitor, 100 pF, cerm		
C8	Same as C5			
C9 thru C12	0180-0374	Capacitor, 10 μF,tantalum		
C13 thru C28	0180-0197	Capacitor, 2.2 μF, tantalum, 10%		
C29	0160-4138	Capacitor, 200 pF, mica		
C30	Same as C5			

Table 5-1. Replaceable Parts (Continued)

Ref Des	HP Part No.	Description	Mfr Code	Mrf Part No.
CR1 thru CR32	1901-1067	Diode, silicon	07263	FDH4114
CR33 thru CR37	1901-0040	Diode, silicon	07263 14433 03877 01295	FDG1088 S541 SG9142 PG512
CR38	1902-1296	Diode, Zener, 11.0V, 0.4W	04713	SZ10939-194
CR39	Same as CR38			
CR40 thru CR43	Same as CR1			
CR44	Same as CR33			
CR45	Same as CR33			
Q1	1826-0154	Dual SPST CMOS switch	17856	DG200BA
Q2	Same as Q1			
Q3	Same as Q1			
Q4	Same as Q1			
Q5	Same as Q1			
Q6	Same as Q1			
Q7	Same as Q1			
Q8	Same as Q1			
Q9	1854-0557	Transistor, NPN	07263	2N2432A
Q10	1855-0319	Transistor, dual FET, D mode	17856	DN281
Q11	1858-0036	Transistor, dual PNP		
R1 thru R17	0683-1025	Resistor, 1K, 5%, ¼W	01121	CB1025
R18 thru R33	0683-2215	Resistor, 220Ω 5%	01121	CB2215
R34	0757-0442	Resistor, 10K, 1%, 1/8W	07716, et al	CEA,TO
R35	Same as R34			
R36	0757-0910	Resistor, 270Ω, 1%, 1/8W	07716, et al	CEA,TO
R37	Same as R36			
R38	0698-6424	Resistor, 5K, 0.02%	18612	V53-1
R39	Same as R38			
R40	0757-0346	Resistor, 10Ω, 1%, 1/8W	07716, et al	CEA,TO
R41	Same as R38			
R42	Same as R38			
R43	2100-0670	Resistor, variable, 10K		
R44	2100-2670	Resistor, var., 20Ω, ½W	84048, et al	172-200

Table 5-1. Replaceable Parts (Continued)

Ref Des	HP Part No.	Description	Mfr Code	Mfr Part No.
R45	0757-0280	Resistor, 1K, 1%, 1/8W	07716, et al	CEA,TO
R46	Same as R45			
R47	0698-6584	Resistor, 3.3K, 0.02%, 1/8W		
R48	Same as R47			
R49	1810-0020	Resistor network, 1.5K	56289	200C1098-CRR
R50	Same as R45			
R51	Same as R43			
R52	0757-0935	Resistor, 3K, 2%, 1/8W	07716, et al	CEA,TO
R53	0757-0950	Resistor, 12K, 1%, 1/8W, MF	07716, et al	CEA,TO
R54	0698-3441	Resistor, 215Ω, 1%, 1/8W	07716, et al	CEA,TO
R55	2100-2633	Resistor, var., 1K, ½W	84048, et al	172-102
R56	Same as R45			
R57	0698-0084	Resistor, 2.15K, 1%	07716, et al	CEA,TO
R58	Same as R57			
R59	Same as R43			
R60	0683-1555	Resistor, 1.5M		
R61	Same as R43			
R62	0683-1545	Resistor, 150K	01121	CB154S
R63	Same as R45			
R64	0757-0316	Resistor, 42.2Ω, 1%, 1/8W	07716, et al	CEA,TO
R65	0698-3157	Resistor, 19.6K, 1%, 1/8W	07716, et al	CEA,TO
R66 and R67	0757-0439	Resistor, 6.81K, 1%, 1/8W	07716, et al	CEA,TO
R68	0698-3161	Resistor, 38.3K, 1%, 1/8W	07716, et al	CEA,TO
R69	2100-2031	Resistor, variable, 50K	84048	170-503
R70	Same as R45			
R71	0757-1094	Resistor, 1.47K, 1%, 1/8W	07716, et al	CEA,TO
R72	Same as R45			
R73	0698-3440	Resistor, 196Ω, 1%		
R74	0698-3444	Resistor, 316Ω, 1%		
R75	1810-0030	Resistor network, 1.0K	56289	200C1618-CRR
R76	Same as R75			
R77 thru R79	Same as R49			
R80	Same as R45			
R81	Same as R45			

Table 5-1. Replaceable Parts (Continued)

Ref Des	HP Part No.	Description	Mfr Code	Mfr Part No.
R82	Same as R71			
R83	Same as R66			
R84	Same as R45			
U1	1826-0021	Voltage follower	27014	LM310H
U2	Same as U1			
U3	1826-0176	FET operational amp	32293	8007C
U4	Same as U3			
U17	1820-0956	Dual 2-input gate	07263	U6A9956X
			14433	MIC 956
U27	Same as U17			
U37	Same as U17			
U47	Same as U17			
U57	Same as U17			
U64	Same as U17			
U65	Same as U17			
U66	Same as U17			
U67	Same as U17			
U72	1820-0077	Dual D-type flip-flop	01295	SN7474N
			04713	MC7474P
			27014	DM7474N
U73	1820-0068	Triple 3-input gate	01295	SN7410N
			04713	MC7410P
			27014	DM7410N
U74	1820-0174	Hex inverter	01295	SN7404N
			04713	MC7404P
			27014	DM7404N
U75	1820-0587	Triple 3-input gate	27014	DM74L10N
U76	1820-0588	Dual 4-input gate	27014	DM74L20N
U77	1820-0054	Quad 2-input gate	01295	SN7400N
			04713	MC7400P
			27014	DM7400N
U82	1820-0511	Quad 2-input gate	01295	SN7408N
			07263	U9A9N0859X
			27014	DM7408N
U83	1820-0134	Four-bit shift register	07263	U7B930059X
U84	Same as U75			
U85	1820-0596	Dual D flip-flop	27014	DM74L74N
U86	Same as U75			
U87	1820-0586	Hex inverter	27014	DM74L04N
U89	Same as U75			
U92	1820-0627	One-of-ten decoder	07263	U7B93L0159X
U93	Same as U74			
U94	1820-0583	Quad 2-input gate	27014	DM74L00N
U95	Same as U94			
U96	Same as U82			
U97	Same as U77			
U102	Same as U92			
U103	Same as U76			
U104	Same as U76			

Table 5-1. Replaceable Parts (Continued)

Ref Des	HP Part No.	Description	Mfr Code	Mfr Part No.
U105	Same as U94			
U106	Same as U85			
U107	Same as U94			
U112	1820-0659	Four-bit shift register	07263	U7B93L0059X
U113	Same as U87			
U114	1820-0515	Dual retriggerable O.S.	07263	U6B960259X
U122	1820-0778	4-Bit binary counter	07263	93L16
U123	Same as U92			
U124	1820-0730	Dual retriggerable O.S.	07263	U7B96L0259X
U132	Same as U112			
U133	Same as U112			
U134	1820-0207	Retriggerable one-shot	07263	SL12895 (9601 PC)
None	0960-0392	A/D converter, 12-bit, 40 kHz, 5 mV		
None	0960-0381	DC/DC converter, +5 to ±15V		
K1	0490-0561	Relay, dual form B, reed, 80 ohms		
None	0360-0294	Terminal, test point		
None	0360-0474	Terminal pin		
None	0360-1149	Terminal pin		
None	0360-1208	Terminal, teflon, insul.		
J1	1250-0543	Connector, coaxial		

Table 5-2. Manufacturer's Code List

Mfg. No.	Manufacturer Name	Address
01121	Allen Bradley Co.	Milwaukee, Wisconsin 53204
01295	Texas Instruments, Semiconductor Division	Dallas, Texas 75321
03877	Transitron Electronics Corp.	Wakefield, Mass. 01880
04713	Motorola Semiconductor Products	Phoenix, Arizona 85008
07263	Fairchild Semiconductor Division	Mt. View, Calif. 94040
07716	IRC	Burlington, Iowa 52601
14433	ITT Semiconductor	W. Palm Beach, Fla 33401
17856	Siliconix, Inc.	Santa Clara, Calif. 95051
18612	Vishay Instruments	Malvern, Pa. 19355
25403	Amperex Electronic Corp.	Slatersville, R.I. 02876
27014	National Semiconductor Corp.	Santa Clara, Calif. 95051
28480	Hewlett-Packard	Palo Alto, Calif. 94304
32293	Intersil, Inc.	Cupertino, Calif. 95014
56289	Sprague Electric Co.	N. Adams, Mass. 01247
84048	TRW, St. Petersburg Div.	St. Petersburg, Fla. 33702