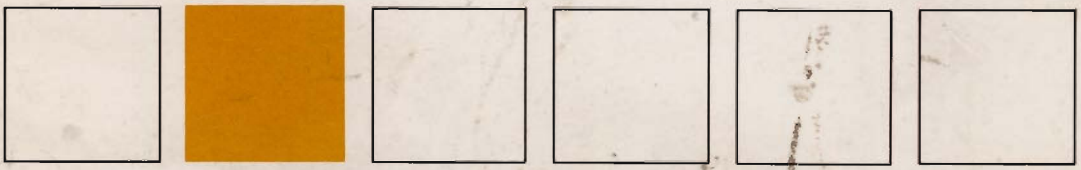
HEWLETT PACKARD

HP 82481A

AC Steady-State Circuit Analysis Pac Owner's Manual

For the HP-71



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HEWLETT PACKARD

AC Steady-State Circuit Analysis Pac

Owner's Manual

For Use With the HP-71

based on programs written for Hewlett-Packard by
Bruce K. Murdock

December 1983

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Introducing the Circuit Analysis Pac

The HP 82481A AC Steady-State Circuit Analysis Pac contains a general purpose Computer Network Analysis Program called CNAP. The building blocks that are available to construct circuit models are resistors, capacitors, inductors, voltage-controlled current sources (VCCS), lossless transmission line segments, open transmission line stubs, and shorted transmission line stubs. The program can output the complex ac voltage at any node in the network. Optionally, group delay is calculated.

CNAP provides rapid ac steady-state analysis of virtually any type of electronic network. Numerous uses include:

- Active filter simulation.
- Analysis of LC filters containing transformers and coupled inductors.
- General transistor amplifier circuit analysis.
- Operational amplifier circuit analysis.
- High-frequency amplifier analysis (including transmission line segments).

You do not have to have a knowledge of programming to use this pac. To run CNAP, just answer the questions that appear in the display. The results are formatted for the display or a peripheral printer. All of the display formats and headings are contained in RAM files and may be changed by the user.

This pac dimensions arrays based on available memory. With an HP-71, a circuit with a maximum of 17 nodes and 51 branches can be solved. When three memory modules are added, the number of nodes and branches increases to 24 and 72 respectively.

Contents

How to Use This Manual

This manual contains detailed information on the operation of the Circuit Analysis Pac. The explanations assume that you know how to use the HP-71 to the level described in sections 1 and 6 of the *HP-71 Owner's Manual.* It is also assumed that you are familiar with circuit modeling theory.

There are three sections in this manual. The first one, "Getting Started," introduces you to the use of the Circuit Analysis Pac: how to install and remove the module, how to set up a circuit analysis problem, and how to put a circuit into the proper form to be analyzed.

The second section, "CNAP Operating Instructions," explains how to run CNAP, the Computer Network Analysis Program. Specifically, it describes circuit input and modification, circuit storage, and circuit analysis and output.

The third section, "CNAP Examples," presents three circuit analysis problems and their solutions.

The appendixes contain reference information:

- Appendix A, "Owner's Information," has warranty and service information.
- Appendix B, "The Crout Reduction," describes Crout's method of solving linear algebraic equations.
- Appendix C, "List of Files and Variables," lists the files and variables used in this pac.
- Appendix D, "CNAP Program Structure and Description," shows how CNAP uses nodal analysis to obtain a matrix equation set.
- Appendix E, "Optional Printer Routine," gives another subroutine for formatting CNAP output on a 24-character printer.

A complete subject index is also included at the end of this manual.

Section 1

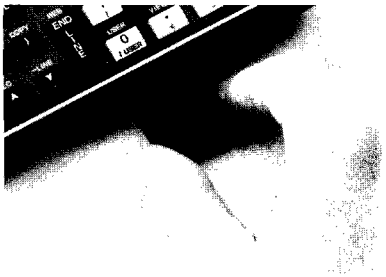
Getting Started

Installing the Circuit Analysis Module

The circuit analysis module can be plugged into any of the four ROM ports on the front edge of the computer.

- Be sure to turn off the HP-71 (press f OFF or execute BYE) before installing or removing a module.
- If you have removed a module to make a port available for the circuit analysis module, before installing the circuit analysis module, turn the computer on and then off to reset internal pointers.
- Do not place fingers, tools, or other foreign objects into any of the ports. Such actions could result in minor electrical shock hazard and interference with pacemaker devices worn by some persons. Damage to port contacts and internal circuitry could also result.

To insert the circuit analysis module, orient it so that the label is right side up, hold the computer with the keyboard facing up, and push in the module until it snaps into place. During this operation be sure to observe the precautions described above.



To remove the module, use your fingernails to grasp the lip on the bottom of the front edge of the module and pull the module straight out of the port. Install a blank module in the port to protect the contacts inside.

Once you install the circuit analysis module, you will probably want to leave it installed most of the time. The module does not use any battery power, and it has no effect on the normal operation of your computer.

Using the Circuit Analysis Pac

The programs in this pac are designed to run and display results without the need for peripherals. If a printer is available, the results will be printed. If you want a different format, you can create your own BASIC program to print the results. (The BASIC program would be called instead of the output routine in the module.)

This pac dynamically dimensions arrays based on available memory. With an HP-71, a circuit with a maximum of 17 nodes and 51 branches can be solved (the number of branches is three times the number of nodes). Additional memory modules can increase the number of nodes and branches to 24 and 72 respectively.

CNAP Circuit Configurations

Before an electronic circuit can be analyzed using CNAP, the circuit must be put into the proper form.* This means the circuit must be drawn using elements from the CNAP menu: resistors, capacitors, inductors, voltage-controlled current sources (VCCS), transmission line segments, open transmission line stubs, or shorted transmission line stubs. First, the active circuit elements must be replaced with models containing a VCCS as shown on page 11.

Transistors

Transistors come in several families: bipolar, junction field-effect transistors (JFET), and metal oxide semiconductor field-effect transistors (MOSFET). In general, their responses are frequency-dependent and nonlinear. However, around any given dc operating point, the ac behavior can be described using a linear, incremental, two-port model. The characteristics of this two-port model can have many descriptions. Commonly Z parameters, Y parameters, H parameters, or S parameters are used. Unfortunately, these parameters are frequency dependent. What is needed for CNAP is a model whose elements remain constant with frequency. One such model is the common-emitter hybrid-pi as shown in figure 1-1. This model is reasonably simple, accurately describes the ac behavior over many decades of frequency without element change, and has parameters that are easily determined.

* A circuit must consist of at least two nodes in addition to node 0.

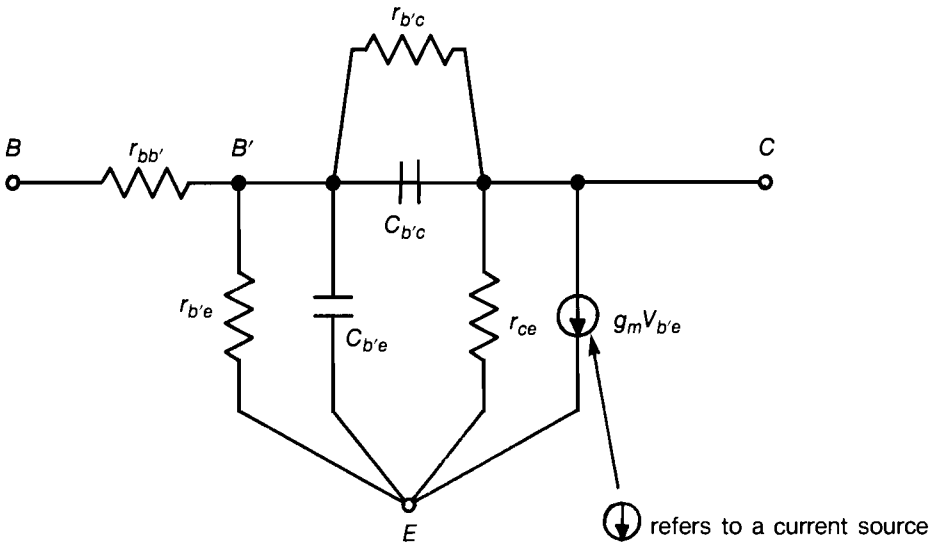


Figure 1-1. Hybrid-Pi Transistor Model

Hybrid Pi Element Values:

1. $r_{bb'}$—base spreading resistance. This resistance is practically constant for a given transistor. It is generally between 5 and 100 ohms. For low frequency modeling, it can be neglected.
2. $r_{b'e}$—base-emitter resistance. This resistance is the dynamic resistance of the base-emitter diode reflected to the base by the current gain of the transistor (β or h_{fe}):

$$r_{b'e} = r_e(1 + h_{fe}) \cong r_e \times h_{fe}$$

r_e is the base-emitter diode dynamic resistance, and is related to the emitter current by:

$$r_e = \frac{kT}{qI_e} = \frac{0.0260}{I_e}$$

where T is equal to room temperature (°K).

3. $C_{b'e}$—base-emitter capacitance. This is the forward-biased base-emitter junction capacitance, and is responsible for the high-frequency gain roll-off in transistors. The $C_{b'e}r_e$ time constant determines the transistor's gain-bandwidth product (f_t), hence:

$$C_{b'e} = \left(\frac{1}{2\pi \times f_t \times r_e}\right)$$

where r_e is the dynamic resistance of the base-emitter diode as defined in step 2.

4. $r_{b'c}$—the feedback resistance (generally greater than 1 megohm). It can be found from the open-circuit reverse voltage gain, h_{re}, by:

$$r_{b'c} = \frac{r_e(1 + h_{fe})}{h_{re}} \cong \frac{r_{b'e}}{h_{re}}$$

5. $C_{b'c}$—collector-base junction capacitance. This is given as C_{ob} on the manufacturer's data sheet. It can also be calculated from the collector-base junction area, A, and the collector-emitter voltage, V_{ce}:

$$C_{b'c} = A\left(\frac{k}{V_{ce}}\right)^{1/3}$$

where k is a constant related to the junction impurity profile and the dielectric constant of silicon.

6. g_m—the transconductance gain of the transistor. This is basically the dynamic conductance of the forward-biased base-emitter diode ($1/r_e$). The exact formula is:

$$g_m = \frac{h_{fe}}{r_e(1 + h_{fe})} \cong \frac{1}{r_e}$$

7. r_{ce}—the common-emitter output resistance. It is related to the following hybrid parameters:

$$r_{ce} = \frac{1}{(h_{oe} - g_m h_{re})}$$

This resistance is generally larger than 1 megohm and can usually be neglected.

Field-Effect Transistors

The topology of the hybrid-pi model serves equally well for field-effect transistors. The element definitions are different and some are missing. Starting with the hybrid-pi model, replace the base by the gate, the emitter by the source, and the collector by the drain.

1. $r_{bb'}$—also present in FETs. It represents the bulk resistance of the silicon gate (in a junction FET) plus the associated bond wire and lead resistance, and is typically 1 to 100 ohms. This element can generally be neglected except in high frequency analyses. Since g_{iss} is given at a specified frequency (f), and C_{iss} is known, $r_{bb'}$ can be calculated using a parallel to series conversion:

$$Q = 2\pi f \times \frac{C_{iss}}{g_{iss}} = \frac{b_{iss}}{g_{iss}}$$

$$r_{bb'} = r_s = \frac{r_p}{(1 + Q^2)} = \frac{1}{((1 + Q^2) \times g_{iss})}$$

$$C_s = C_p \times \frac{(Q^2 + 1)}{Q^2} \cong C_p$$

2. $r_{b'e}$—this element can be replaced by an open circuit in FETs. Although it will be found as g_{iss} on FET data sheets, it represents the series-to-parallel conversion of the equivalent gate series resistance. The series representation is more accurate since the series resistance is not frequency dependent, while the parallel transformed element is quite frequency dependent.
3. $C_{b'e}$—this capacitance is equivalent to C_{iss}, the gate-source input capacitance.
4. $r_{b'c}$—this element can be replaced by an open circuit in FETs.
5. $C_{b'c}$—this capacitance is equivalent to C_{rss}, the common-source reverse transfer capacitance.
6. g_m—this is the FET transconductance, g_{fs}.
7. r_{ce}—this is equivalent to the reciprocal of the FET common-source output conductance, g_{os}.

Operational Amplifiers

An "ideal" operational amplifier (op amp) has infinite gain, infinite bandwidth, infinite input impedance, zero input capacitance, and zero output impedance. Physical op amps don't achieve any of these parameters, but some come close. Figure 1-2 shows some of the parasitic elements of a physical (real world) op amp. The input impedance is generally acceptably high, but the input capacitance of a few picofarads can cause problems with gyrator circuits, and must be compensated for. Neither the gain nor the bandwidth are infinite. Typical gain is 100,000, and typical bandwidth is 0.5 MHz for 741 type op amps. The op amp frequency response (Bode plot) is usually characterized by a low-frequency dominant pole. Parasitic, high-frequency poles are not encountered until the unity-gain crossover frequency has been attained.*

* *Computer Aided Analysis of Electronic Circuits*, by Chua and Lin, Prentice-Hall, 1975, has an excellent discussion of the modeling of these higher frequency parasitic poles.

For our purposes, a single-pole op amp model will be given and used in the examples to follow. The output impedance of the physical op amp is finite rather than zero. A typical value is 75 ohms. The output impedance is incorporated using a Norton equivalent circuit—a resistor shunting a VCCS. Figure 1-3 shows a model of a single pole physical op amp. Note that the compensation pole is added to the input circuit with a 10-gigaohm resistor and 3-pF capacitor. This location is a convenient way to add the compensation pole in a way that does not load other circuit elements. For FET-input op amps, the compensation elements can have a higher impedance consistent with the higher-impedance input networks.

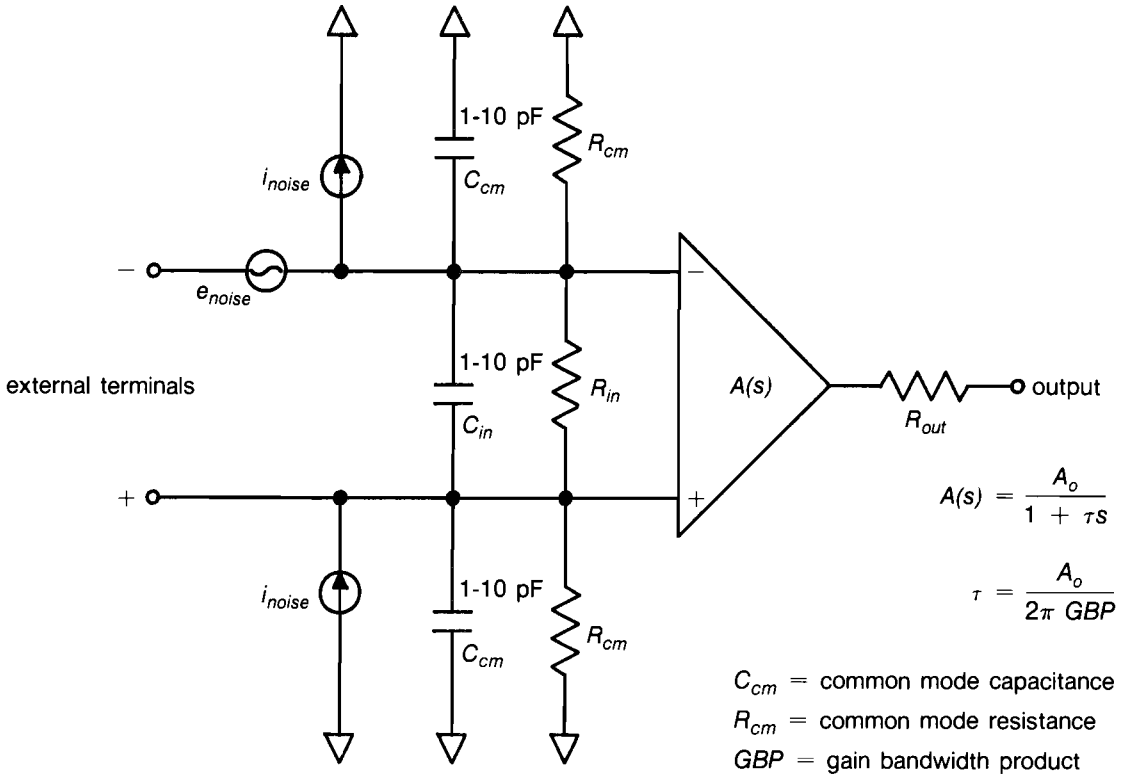


Figure 1-2. Physical Op Amp Showing Parasitic Elements

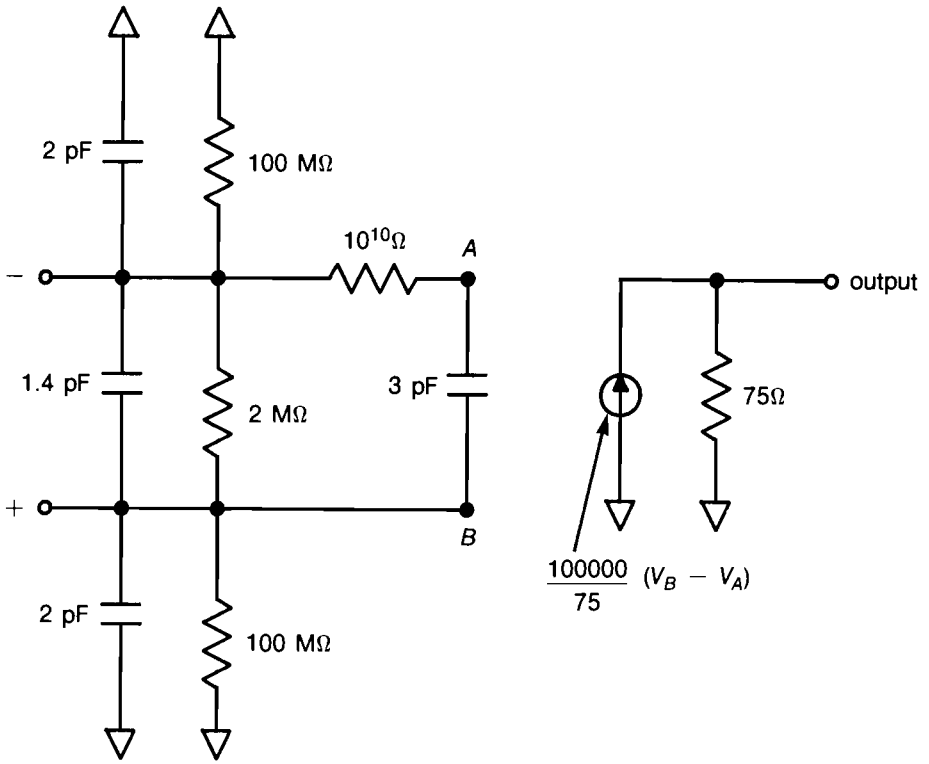


Figure 1-3. CNAP Model For μA741 Including Parasitic Elements (Parasitics may be neglected depending on the application.)

Voltage Sources

The voltage-controlled current source (VCCS) is the only source permitted in CNAP. However, it can be changed into a very acceptable voltage source by paralleling a resistor. As long as the resistor is small with respect to other circuit impedances, the "voltage source" will indeed appear as a voltage source. For example, in a circuit where the smallest resistance (or reactance) is 100 ohms, this voltage source can be created by paralleling a 100 ampere/volt current source ($g_m = 100$) with a 0.01-ohm resistor. The net effect is a 1 volt/volt Thevenin equivalent "voltage source" with a 0.01 ohm output impedance. Since there are four orders of magnitude difference between the "voltage source" output impedance and the rest of the circuit impedances, the voltage source loading is negligible.

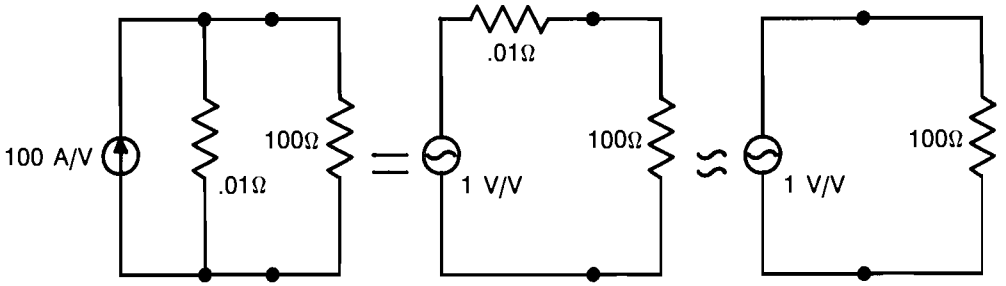


Figure 1-4. Voltage Source Obtained From A Current Source

Transformers

CNAP accomodates transformers very easily through their equivalent circuit representation. Figures 1-5 through 1-8 show four equivalent circuits for both floating and one-common-terminal applications. Example 1 on page 33 will demonstrate the inclusion of a transformer in a circuit being analyzed.

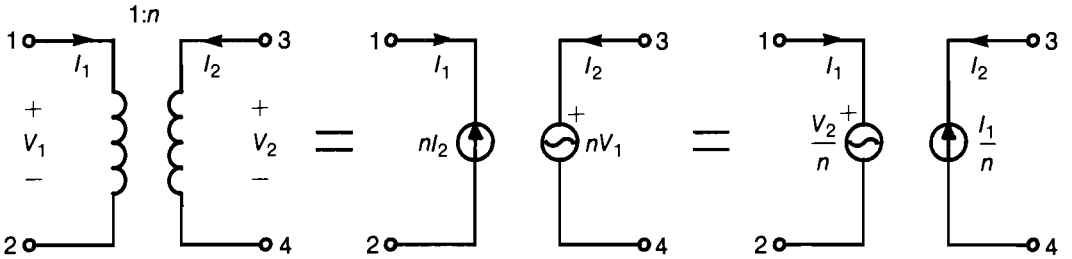


Figure 1-5. Ideal Transformer

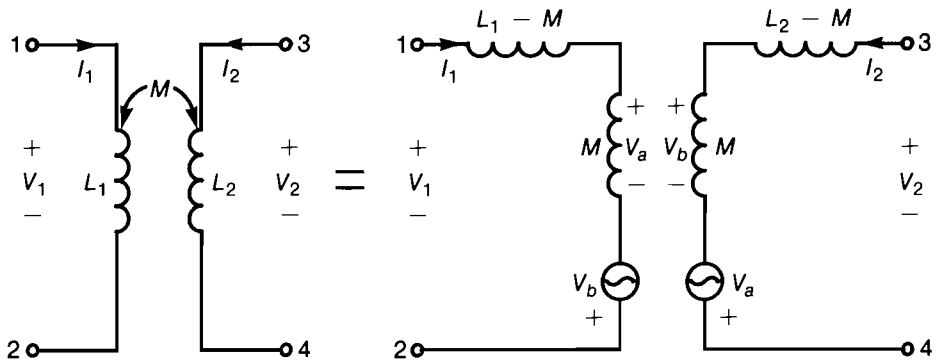


Figure 1-6. Pair of Floating Mutual Inductors

Note the opportunity to incorporate winding resistances in the model of figure 1-6 via Norton equivalents of the voltage sources V_a and V_b:

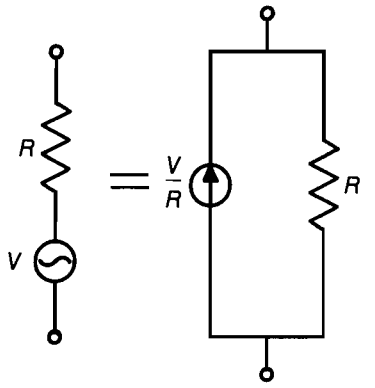


Figure 1-6a. Norton Equivalent

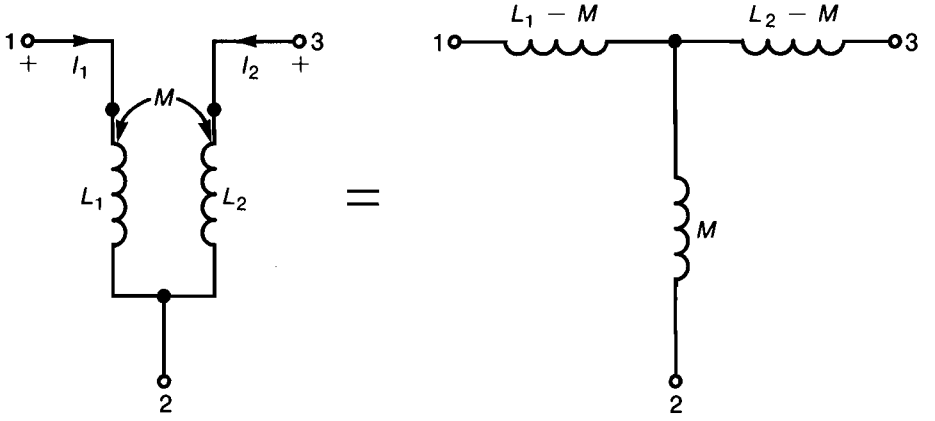
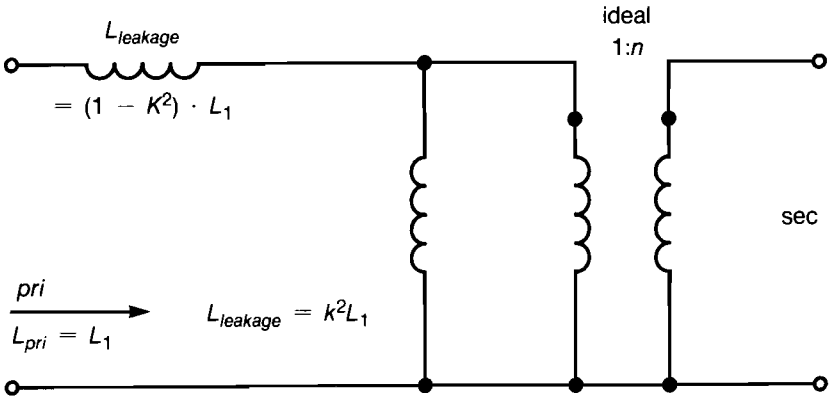


Figure 1-7. Pair of Grounded Mutual Inductors



where k is the coupling coefficient

$$k \equiv \frac{M}{\sqrt{L_1 L_2}}$$

and n is the turns ratio

$$n \equiv k\sqrt{\frac{L_2}{L_1}}$$

Figure 1-8. Application of T Model to Physical Transformer Model (Note that the winding resistances are pushed outside of the model boundaries.)

Circuit Configuration Example

Given the following circuit schematic of a 1000-Hz tuned transistor amplifier, determine the transistor dc operating point, calculate element values for the transformer "T" equivalent circuit, and assemble the whole circuit.

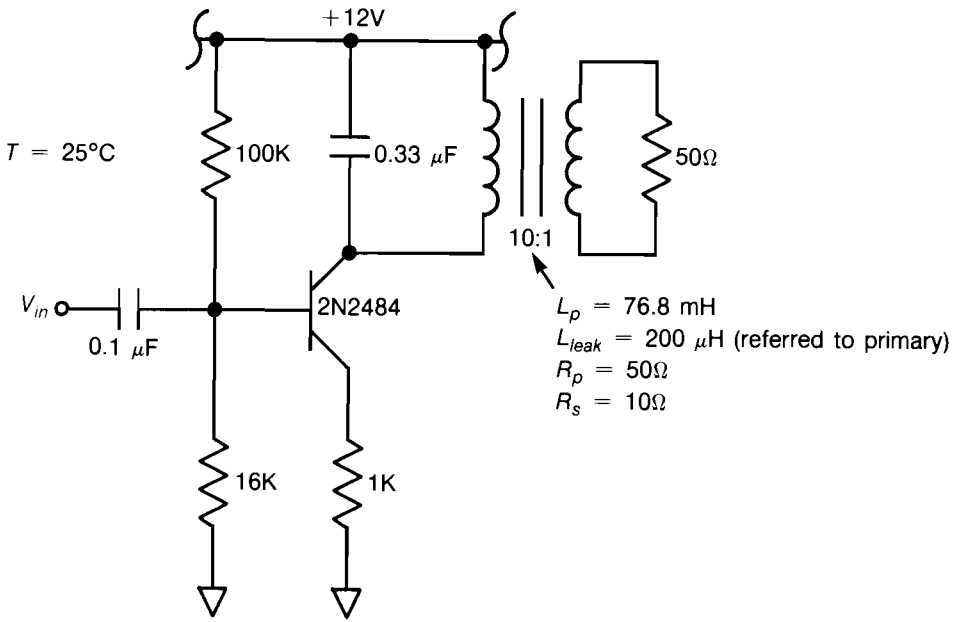


Figure 1-9. Circuit Schematic

Determining the Transistor DC Operating Point

1. For the moment, neglect the base current and calculate the current through the base bias network and the base bias voltage.

$$i_{bias} = \frac{12\text{V}}{116\text{K}} = 103\ \mu\text{A}$$

$$V_{bias} = \frac{16}{116} \times 12\text{V} = 1.66\text{V}$$

2. Assuming a V_{be} of 0.65V, calculate emitter voltage and emitter current.

$$V_e = V_{bias} - V_{be} = 1.01\text{V}$$

$$I_e = \frac{1.01\text{V}}{1\text{K}} \cong 1\ \text{mA}$$

3. Look up the 2N2484 transistor parameters for $I_e = 1$ mA, $V_{ce} = 11$V, $T = 25°C$.

   $h_{fe,\,min} = 250$

   $f_{t,\,min} = 60$ MHz

   $c_{ob,\,max} = 2.5$ pF

   $h_{oe} = 15\ \mu$S

   $h_{re} = 425 \times 10^{-6}$

4. Calculate the actual base current to see if the assumption of step 1 is valid, i.e., the base current is negligible.

$$i_b = \frac{1\text{ mA}}{250} = 4\ \mu\text{A}$$

   Since 100 μA is flowing through the bias network, 4 μA is negligible.

5. Calculate the various parameters for the hybrid-pi model.

   $r_{bb'}$ is negligible with respect to other circuit impedances and operation frequencies.

$$r_e = \frac{.026}{.001\text{A}} = 26\Omega$$

$$r_{b'e} \cong r_e \times h_{fe} = 26 \times 250 = 6500$$

$$c_{b'e} = \frac{1}{(2\pi \times 60\text{ mHz} \times 26)} = 102\text{ pF}$$

$$r_{b'c} \cong \frac{r_{b'e}}{h_{re}} = \frac{6500}{(425 \times 10^{-6})} = 15.3\text{ M}\Omega\text{ (neglectable)}$$

$$c_{b'c} = c_{ob} = 2.5\text{ pF}$$

$$g_m = \frac{1}{r_e} \times \frac{h_{fe}}{(1 + h_{fe})} = 36.9 \times 10^{-3}\text{ S}$$

$$r_{ce} = \frac{1}{(h_{oe} - g_m\, h_{re})} = -1.47 \times 10^6\ \Omega$$

Note the negative value for r_{ce} because the manufacturer rounded both h_{oe} and h_{re}. Neglect r_{ce}.

Calculating Values For the Transformer "T" Equivalent Circuit

Calculate the element values for the transformer "T" equivalent circuit below.

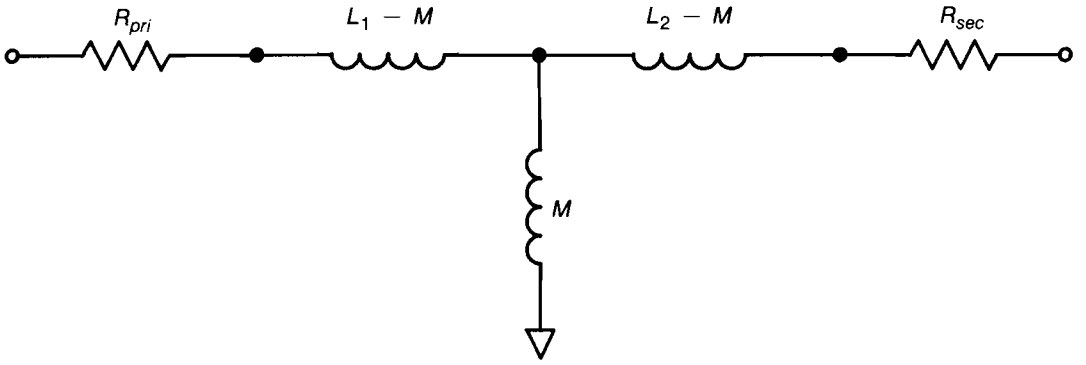


Figure 1-10

Referring to figure 1-8, the primary inductance seen at the primary terminals, with the secondary open-circuited, is:

$$L_{pri} = L_1 = 76.8 \text{ mH}$$

Since the transformer was wound with 10 times as many primary turns as secondary turns, the secondary inductance must be:

$$L_{sec} = L_2 = \frac{L_1}{n^2} = 768 \ \mu\text{H}$$

The mutual inductance can be found from:

$$M = k \times \sqrt{(L_1 \times L_2)} = \sqrt{(k^2 \times L_1 \times L_2)}$$

where k, the coupling coefficient, can be found from:

$$L_{leakage} = (1-k^2) \times L_1$$

hence

$$k^2 = 1 - (L_{leakage} \div L_1) = 0.9974$$

$$M = \sqrt{((.9974)(76.8 \text{ mH})(768 \ \mu\text{H}))} = 7.67 \text{ mH}$$

The transformer "T" model becomes:

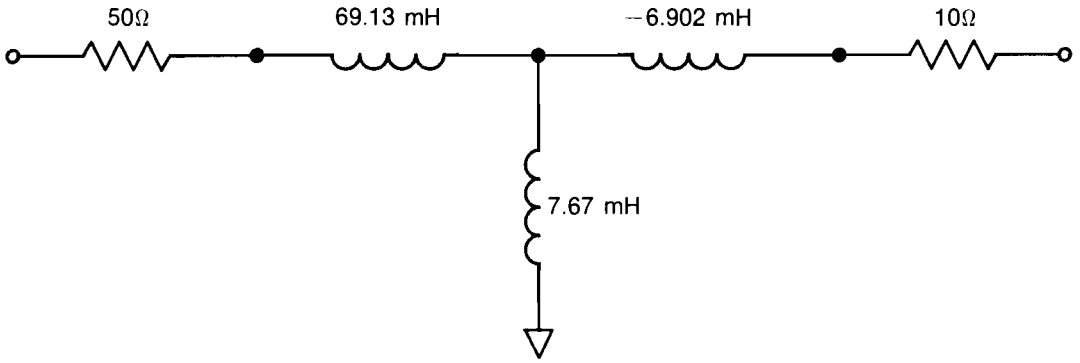
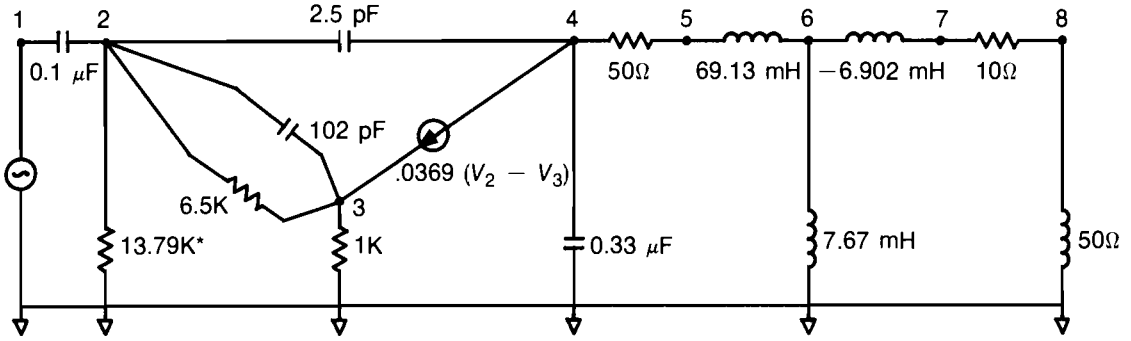


Figure 1-11

Assembling the Whole Circuit

Neglectable elements are omitted, and the nodes are numbered. The +12V power supply is considered ac ground. The input node is always node 1 and the output node is node 8.



* 16K//100K

Figure 1-12. CHAP **Model For Transistor Amplifier Circuit**

This circuit will be analyzed as an example on page 33.

Section 2

CNAP Operating Instructions

Running the CNAP Program

The CNAP program is executed by typing RUN CNAP [END LINE].

CNAP is controlled by responding to the menus or questions that appear in the display. There is a main menu (explained on page 25) that is used to select a number of more detailed menus and operations. The program is designed to be self-guiding; that is, the various menus automatically guide you through the program operation.

There are two general areas of CNAP.

- Circuit input, modification, and review.
- Circuit analysis and output.

A third area of CNAP involves circuit storage and retrieval. This part of the program surfaces during the use of the first two parts.

When CNAP is run, the program sets the following HP-71 modes, states, and formats:

- The User keyboard is disabled.
- Degrees mode is set.
- DEFAULT ON is set.
- Standard format (STD) is set.
- If the program is stopped prematurely, it may be necessary to reestablish the PRINTER IS device and the DELAY rate.

The numeric input range is $\pm 9.99 \times 10^{-99}$ to $\pm 9.99 \times 10^{99}$.

Circuit Input

The circuit interconnection is described as branches connected between numbered nodes. A node, within the context of this program, is any point where two or more elements are connected together. *Node 0 is the ground, or common node, and node 1 is the node where the 1 VRMS input voltage source is connected.* The rest of the nodes are numbered consecutively from 2 upward. There is no particular significance to these higher node numbers. *Any node, with the exception of nodes 0 and 1, can be an output node,* and all node voltages are calculated by the program. The program assumes that the highest numbered node is the output unless told otherwise.

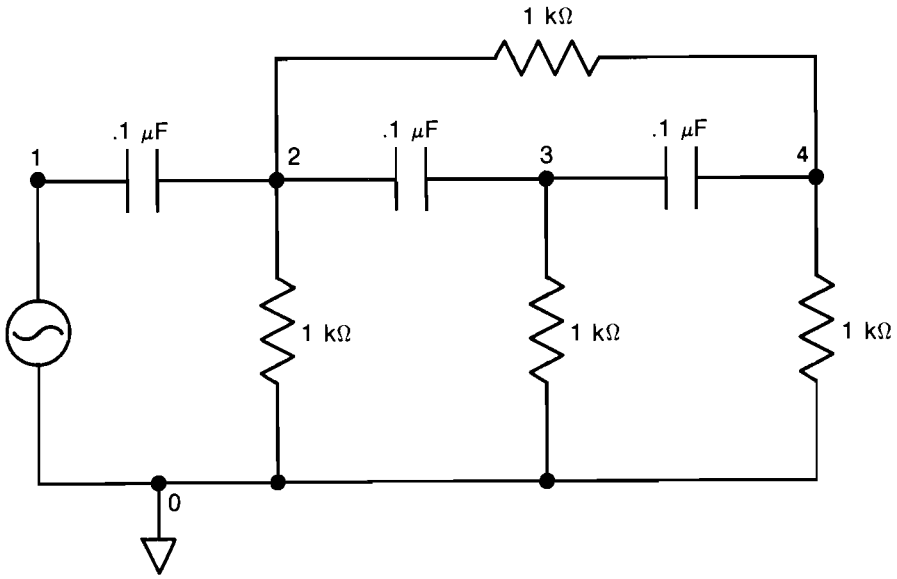


Figure 2-1. Example of Consecutive Node Numbering

This circuit has the nodes consecutively numbered from left to right. The nodes could have been numbered from right to left—as long as node 1 is reserved for the source and node 0 is reserved for the circuit common (or ground). The circuit would then look like this:

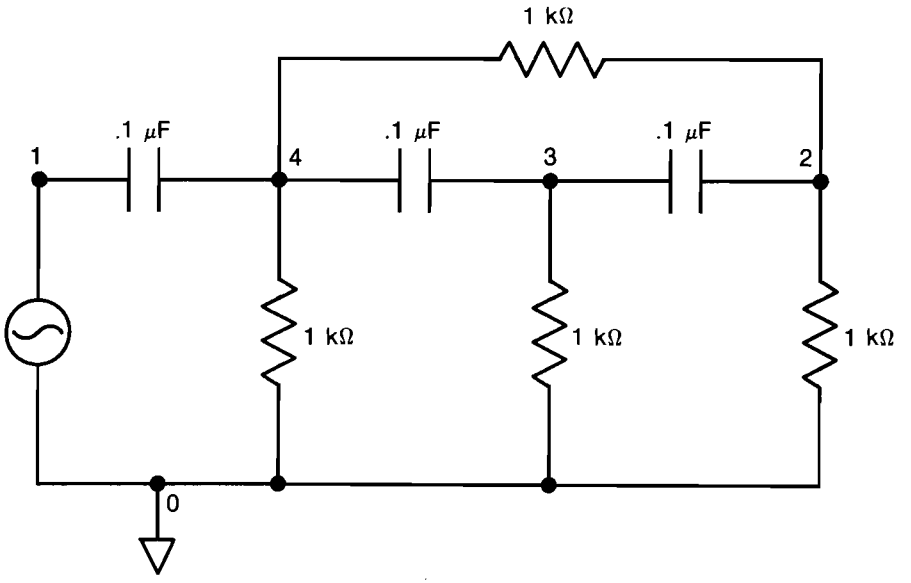


Figure 2-2. Example of Nonconsecutive Node Numbering

Each element in turn must be entered into the program. Elements may be entered in any order, but all elements must be entered. Seven element types are available: resistors, inductors, capacitors, voltage-controlled current sources, transmission line segments, shorted transmission line stubs, and open transmission line stubs. The details of the element entry are covered below.

Main Menu Description

As menus appear in the display, entries are selected by typing in the first letter of the keyword. The main menu appears as follows:

```
Nw Ad Dl Ch Pr Fl O ?
```

The meanings of the abbreviations in the main menu are:

Nw (*New*): Press [N]. This entry erases any circuit currently in memory and prepares the program to accept a new circuit. The element selection menu appears in the display. This menu also appears when Ad or Ch is selected:

```
R L C Vc Xm Os Ss E ?
```

Ad (*Add*): Press [A]. This entry allows branches to be added to an existing circuit. The element selection menu appears in the display.

Dl (*Delete*): Press [D]. This entry allows branches to be deleted. As with Ch below, the program asks for the node numbers of the branch as follows:

```
FROM NODE, TO NODE?
```

If the branch to be deleted is between nodes 4 and 6, you type 4,6 [END LINE]. The program starts searching for branches connected between the specified nodes. If an element (say a resistor) is found on the first branch, the display shows:

```
[NODES:4,6]  R  100   Save/Delete? *
```

The program expects you to press either [S] to save the branch and continue to search for branches connected between the specified nodes, or a [D] to delete the branch found. If no additional branches (or no branch in the first place) are found, the program displays:

```
BRANCH NOT FOUND
```

Then the main menu reappears:

```
Nw Ad Dl Ch Pr Fl O ?
```

Ch (*Change*): Press [C]. This entry allows an existing branch to be changed. The program asks for the node numbers of the branch as follows:

```
FROM NODE, TO NODE?
```

If the branch to be changed is between nodes 5 and 2, you type 5,2 [END LINE]. The program starts searching for the branch. If an element (say a resistor) is found connected between the specified nodes, the display shows:

```
[NODES:5,2]  R 1M  Save/Change?
```

* The display will scroll and only the last 22 characters will be displayed.

Again, the program is expecting either an [S] to save the branch or a [C] to change the branch. If [S] is pressed, the program searches for the next branch connected between the specified nodes. If no additional branches are found, the display shows:

```
BRANCH NOT FOUND
```

Then the main menu reappears:

```
Nw Ad Dl Ch Pr Fl O ?
```

If [C] is pressed, then the element selection menu appears. The branch can now be entered again through the element selection menu. If no element is reentered (if [E] is selected in the element selection menu), then the branch just found is saved.

Pr (*Print*): Press [P]. This causes the currently stored circuit description to be displayed or printed on an external printer.

F l (*File*): Press [F]. This entry allows reading or writing of files. If a file is to be written, the currently stored circuit is stored in the named file. If a file is read, the circuit stored in the named file replaces the circuit currently in memory.

> **Note:** When a file is stored, the memory that is used is no longer available to the program for calculation purposes. If you are using the maximum amount of nodes possible for a given amount of memory, you should store the file **after** the circuit calculation is complete and the results have been displayed.

O (*Output*): Press [O]. This entry selects the output (analysis) mode of CNAP. The output menu is described later.

Element Selection Menu Description

Whenever Nw, Ad, or Ch is selected, the element selection menu ultimately appears in the display:

```
R L C Vc Xm Os Ss E ?
```

Only the first character of each element type need be entered. The character can be either upper- or lowercase. The meanings of the abbreviations are as follows:

R allows entry of a resistor (ohms).

L allows entry of an inductor (henries).

C allows entry of a capacitor (farads).

V allows entry of a voltage-controlled current source (siemens).

X allows entry of a transmission line segment (ohms, hertz).

O allows entry of an open transmission line stub (ohms, hertz).

S allows entry of a shorted transmission line stub (ohms, hertz).

E exits this menu and returns to the main menu.

When [R], [L], or [C] is pressed, the program asks for the nodes between which the element is connected. Also, the element value is requested. For example, suppose [R] is pressed, then:

```
R; FROM, TO? ■
```

appears in the display. If the resistor is connected between nodes 1 and 2, type 1 , 2 [END LINE]. Next, the display shows:

```
R VALUE? ■
```

If the resistor value is 100 ohms, you type 100 [END LINE], and the element selection menu reappears.

```
R L C Vc Xm Os Ss E ?
```

The Vc is a two-port device consisting of an output port and a control port. If Vc is selected, three items are needed—the "from" and "to" nodes for the current source, the transconductance (g_m), and the "+" and "−" controlling nodes. When Vc is selected, the display first shows:

```
VCCS; FROM, TO? ■
```

If the VCCS is connected from nodes 2 to 5, you type 2 , 5 [END LINE].

The display then shows:

```
gm =? ■
```

If g_m is 2000 μS, you respond: 2000E-6 [END LINE].

The display then shows:

```
CONTROL NODES: +, -? ■
```

If the controlling nodes are 5 and 6, you type 5 , 6 [END LINE].

The main element selection menu then reappears:

```
R L C Vc Xm Os Ss E ?
```

If you select a transmission line segment as input, by pressing [X], both port 1 and port 2 nodes must be entered. Furthermore, the transmission line characteristic impedance (Z_o) and electrical length (specified through the quarter-wave frequency) must be entered. The details of this entry sequence follow.

The display shows:

```
PORT 1; FROM, TO? ■
```

If port 1 is connected from node 1 to node 2, you type 1 , 2 [END LINE].

The display then shows:

```
PORT 2; FROM, TO? ■
```

If port 2 is connected from node 3 to node 4, you type 3 , 4 [END LINE].

Next, the display shows:

```
X-LINE, Zo=? ■
```

If the transmission line characteristic impedance is 50 ohms, you type 50 [END LINE].

Lastly, the display shows:

```
X-LINE, QTR-WAVE Hz? ■
```

If the transmission line is quarter-wave resonant at 100 MHz (about 1.25 meters long), you type 100E6 [END LINE].

The element selection menu now reappears:

```
R L C Vc Xm Os Ss E ?
```

Open or shorted transmission line stubs are one-port devices. Hence, only the "from" and "to" nodes, characteristic impedance, and quarter-wave resonant frequency are needed as input. In response to O, the display shows:

```
O-STUB; FROM, TO? ■
```

If the stub is connected from nodes 5 to 8, you type 5,8 [END LINE].

The display then shows:

```
O-STUB, Zo=? ■
```

If Z_o is 50 ohms, you type 50 [END LINE].

Finally the quarter-wave resonant frequency is requested:

```
O-STUB, QTR-WAVE Hz? ■
```

If the quarter-wave resonant frequency is 50 MHz, you type 50E6 [END LINE].

The element selection menu reappears:

```
R L C Vc Xm Os Ss E ?
```

The entry sequence for a shorted transmission line stub is the same as the one shown above for the open transmission line stub.

To exit the routine, press [E]. The main menu reappears.

```
Nw Ad Dl Ch Pr Fl O ?
```

Program Output (Circuit Analysis)

To select the output or analysis function of CNAP, [O] is pressed from the main menu. (Be sure that the main menu is in the display, and not the element selection menu.)

Before the program asks any more questions, it calculates the real elements of the nodal admittance matrix. Depending on the size of the network, this operation will take from a fraction of a second to many seconds. During this calculation, the following message will be displayed:

```
CALC REAL MATRIX ELEM
```

Next, the first of three questions is asked:

```
OUTPUT NODE ? n
```

The cursor is on the number that represents the highest node of the current circuit. If this is the desired output node, press [END LINE]. If a different output node is desired, key in the node number, then press [END LINE].

Secondly, the program asks if the group delay calculation is desired:

```
group delay, Yes/No?
```

The group delay calculation is performed by analyzing the CNAP circuit at frequencies slightly below and slightly above the current analysis frequency. The rate-of-change of phase with respect to frequency is the group delay, and this quantity is obtained by numerical differentiation with the two phase values obtained above. The calculation of group delay doubles the analysis time. The display will show both the upper and lower frequencies at which it is calculating before displaying the current analysis frequency.

To select the group delay calculation, press [Y] in response to the group delay question. Press [N] to skip the group delay calculation.

The last question is the type of frequency sweep desired:

```
loG or liN sweep ?
```

The loGarithmic sweep means the frequency increment is multiplicative. In other words, the ratios of adjacent sweep frequencies are constant. A loGarithmic sweep is selected by pressing [G]. If loGarithmic sweep is selected, the program asks:

```
START,STOP,#PTS/DEC? ■
```

Three numbers separated by commas are expected: the starting frequency, the stopping frequency, and the number of frequency increments per decade. The program automatically calculates the multiplicative constant, which is the *n*th root of 10 for *n* points per decade.

The liNear sweep means the frequency increment is additive, e.g., 5 Hz steps. liNear is selected by pressing [N]. The program then asks:

```
START,STOP,INCR? ■
```

Again, three numbers separated by commas are expected: the sweep starting frequency, the stopping frequency, and the frequency increment.

At this point, if the HP-IL module is installed, the program asks:

```
use printer, Y/N?
```

If the printer option is not selected, the results will be formatted for the display. If group delay was previously selected, then the display format will be [frequency, delay, magnitude, and phase]. Without group delay, the display format will be [frequency, magnitude, and phase].

If results are being displayed, the display will not change until you press a key (with the exception of the cursor keys ([<], [>], [f] [<], and [f] [>])). If the calculated result is too big for the 22-character display, then the left cursor key can be pressed to see the entire line. Numerical results are rounded and engineering notation is used.

If group delay and the printer option are selected, the printer format will be [frequency, magnitude, phase, and delay]. Without group delay, the printer format will be [frequency, magnitude, and phase]. When numerical results are printed, the numbers are truncated and in a format that allows them to be easily read.

After the output sweep is finished, the main menu reappears:

```
Nw Ad Dl Ch Pr Fl O ?
```

If new output is desired, [O] is pressed, and the output sequence starts over.

Section 3

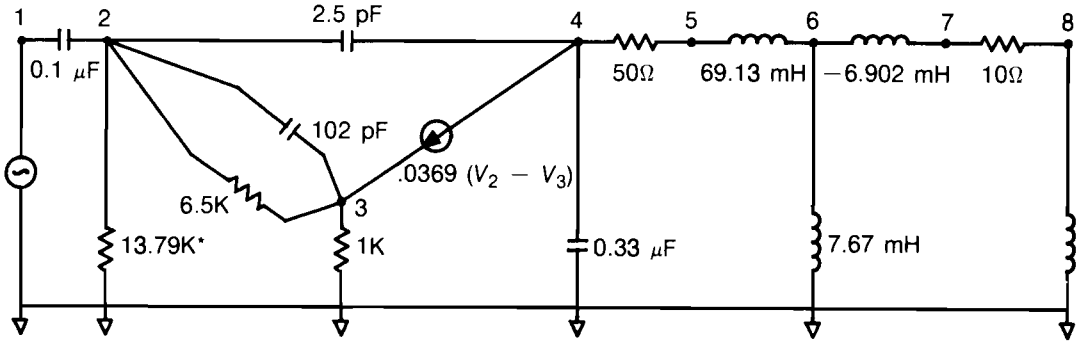
CNAP Examples

Introduction

This section contains three examples using the Circuit Analysis Pac. The examples demonstrate entry of elements to describe a circuit, analysis of input by the program, review and modification of an entered circuit, and program output.

Example 1: Tuned Transistor Amplifier

The CNAP model for a 1000-Hz tuned transistor amplifier was developed earlier (figure 1-12), and is repeated here for reference.



* 16K//100K

Figure 3-1. CNAP **Model for Transistor Amplifier Circuit**

The nodes have already been numbered in accordance with CNAP conventions, so the CNAP model is ready for input to the program.

To run the CNAP program, type RUN CNAP [END LINE]. After displaying the maximum number of nodes possible,* the main menu appears:

```
Nw Ad Dl Ch Pr Fl O ?
```

Since this is a new circuit, press [N], and the element selection menu appears:

```
R L C Vc Xm Os Ss E ?
```

The element input is completely free-form, and elements can be entered in any order. The elements for this example are entered more-or-less from left to right.

Input/Result

[C] — Selects a capacitor.

```
C; FROM, TO? ■
```

1,2 [END LINE] — Enters nodes the capacitor is between.

```
C VALUE? ■
```

.1E-6 [END LINE] — Enters capacitor value.

```
R L C Vc Xm Os Ss E ?
```

[R] — Selects a resistor.

```
R; FROM, TO? ■
```

* If the circuit has more than the maximum number of nodes, use the PURGE command to reclaim memory (refer to "Purging Files" in section 6 of the *HP-71 Owner's Manual*).

Input/Result

2,0 END LINE

Enters nodes the resistor is between.

```
R VALUE? ■
```

13790 END LINE

Enters resistor value.

```
R L C Vc Xm Os Ss E ?
```

R

Selects a resistor.

```
R; FROM, TO? ■
```

2,3 END LINE

```
R VALUE? ■
```

6500 END LINE

```
R L C Vc Xm Os Ss E ?
```

C

Selects a capacitor.

```
C; FROM, TO? ■
```

2,3 END LINE

```
C VALUE? ■
```

102E-12 END LINE

```
R L C Vc Xm Os Ss E ?
```

Input/Result

R

Selects a resistor.

```
R; FROM, TO? ■
```

3,0 END LINE

```
R VALUE? ■
```

1000 END LINE

```
R L C Vc Xm Os Ss E ?
```

C

Selects a capacitor.

```
C; FROM, TO? ■
```

2,4 END LINE

```
C VALUE? ■
```

2.5E-12 END LINE

```
R L C Vc Xm Os Ss E ?
```

V

Selects a voltage-controlled current source.

```
VCCS; FROM, TO? ■
```

4,3 END LINE

```
gm=? ■
```

Input/Result

.0369 END LINE

```
CONTROL NODES: +, -? ■
```

2,3 END LINE

```
R L C Vc Xm Os Ss E ?
```

C

Selects a capacitor.

```
C; FROM, TO? ■
```

4,0 END LINE

```
C VALUE? ■
```

.33E-6 END LINE

```
R L C Vc Xm Os Ss E ?
```

R

Selects a resistor.

```
R; FROM, TO? ■
```

4,5 END LINE

```
R VALUE? ■
```

50 END LINE

```
R L C Vc Xm Os Ss E ?
```

Input/Result

[L] Selects an inductor.

```
L; FROM, TO? ■
```

5,6 [END LINE]

```
L VALUE? ■
```

69.13E-3 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[L] Selects an inductor.

```
L; FROM, TO? ■
```

6,0 [END LINE]

```
L VALUE? ■
```

7.67E-3 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[L] Selects an inductor.

```
L; FROM, TO? ■
```

6,7 [END LINE]

```
L VALUE? ■
```

Input/Result

-6.902E-3 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[R]

Selects a resistor.

```
R; FROM, TO? ■
```

7,8 [END LINE]

```
R VALUE? ■
```

10 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[R]

Selects a resistor.

```
R; FROM, TO? ■
```

8,0 [END LINE]

```
R VALUE? ■
```

50 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[E]

Exits the element menu. The main menu is displayed.

```
Nw Ad Dl Ch Pr Fl O ?
```

At this point the circuit description is complete and the program is awaiting the next command. To verify that the input was correct, the current working file can be listed by responding to the main menu with [P]. This procedure assumes that you do not have an HP-IL module installed.*

Input/Result

[P] — Selects the print option.

```
CIRCUIT DESCRIPTION OF

[FM,TO] TYPE    VALUE

BRANCH  1
[1,2] C         100.0 nF
```

If the circuit had been given a file name, it would be displayed here.

[END LINE]

```
BRANCH  2
[2,0] R         13.79 K
```

[END LINE]

```
BRANCH  3
[2,3] R         6.500 K
```

⋮

[END LINE]

```
BRANCH  7
[4,3] VCCS      36.90 mS
ctrl nodes: + 2 , - 3
```

⋮

* If an HP-IL module is installed, the program prompts:

```
use printer, Y/N?
```

If you press [Y], the results will automatically be displayed (you will not need to press [END LINE]).

Input/Result

END LINE

```
BRANCH 13
[7,8] R        10.00
```

END LINE

```
BRANCH 14
[8,0] R        50.00
```

END LINE

The main menu appears.

```
Nw Ad Dl Ch Pr Fl O ?
```

The analysis phase of the program operation is now executed. The output option is selected by pressing O, whereupon, the display shows `Working...` and then:

```
CALC REAL MATRIX ELEM
```

After the real parts of the admittance matrix elements are calculated, the program asks for the output node:

```
OUTPUT NODE ? 8
```

Since the highest numbered node (eight) is the output node, press END LINE. Next, the display shows:

```
group delay, Yes/No?
```

Since group delay is not desired, press N. Next, the program asks which type of frequency sweep is desired:

```
loG or liN sweep ?
```

Since a linear sweep is desired, press N. The program prompts for the sweep starting frequency, the stopping frequency, and the frequency increment:

```
START,STOP,INCR? ■
```

You respond by typing `800,1200,10` END LINE. If you do not have an HP-IL module installed, the following output is displayed.

Input/Result

```
Working...
FREQ, dB, PHASE
Working, F= 800
B=-21.91,PHASE=-103.90
```

The frequency, dB, and phase are displayed on one line. Since this is longer than the 22-character display, use the g < key to view the entire display.

END LINE

```
Working, F= 810
B=-21.47,PHASE=-105.23
```

⋮

END LINE

```
Working, F= 990
B=-13.57,PHASE=-169.47
```

END LINE

```
Working, F= 1000
B=-13.56,PHASE=-175.82
```

END LINE

```
Working, F= 1010
dB=-13.65,PHASE=177.95
```

END LINE

```
Working, F= 1020
dB=-13.84,PHASE=171.98
```

⋮

Input/Result

END LINE

```
Working, F= 1190
dB=-20.37,PHASE=122.88
```

END LINE

```
Working, F= 1200
dB=-20.70,PHASE=121.77
```

Since the load resistance reflected through the transformer is about 5000 ohms (10*10*50), and the unbypassed emitter resistance is 1000 ohms, the transistor stage voltage gain should be about 5. Since the 10:1 turns ratio of the transformer provides a voltage stepdown to the load, the expected overall voltage gain is 1/2, or −6 dB. The actual voltage gain at resonance is −13.57 dB. The reason for the 7 dB disagreement is due to the 50-ohm primary resistance of the transformer. This resistor kills the Q of the output tank circuit; that is, the parallel Q due to the reflected load resistance is:

$$Q_p = \frac{R_p}{\omega L} = \frac{5000}{(2\pi * 1000 * 76.8 \text{ mH})} = 10.36$$

This low Q is acceptable since it represents the power transmitted into the load. However, the series Q due to the 50-ohm primary resistance is:

$$Q_s = \frac{\omega L}{R_s} = \frac{(2\pi * 1000 * 76.8 \text{ mH})}{50} = 9.65$$

This low Q is not acceptable since it represents power lost in the winding resistance. Since Qs add like parallel resistors, the total circuit Q is:

$$Q_{total} = \frac{1}{\frac{1}{Q_s} + \frac{1}{Q_p}} = 5.00$$

Thus, the output stage is somewhat lossy; approximately half of the output power is lost in the winding resistance of the transformer primary. Let's use the change feature of CNAP to replace the 50-ohm primary resistance with a 5-ohm resistance.

With the main menu in the display, press [C] to select the change mode. The display responds:

```
FROM NODE, TO NODE?
```

Since the transformer primary resistance is between nodes 4 and 5, you type 4,5 [END LINE]. The program searches for branches connected between nodes 4 and 5, and then displays:

```
[NODES:4,5]  R  50  Save/Change?
```

Pressing [C] signals the program you want to change this node. The element selection menu appears:

```
R L C Vc Xm Os Ss E ?
```

Press [R] and the display shows:

```
R; FROM, TO?
```

Type 4,5 [END LINE], and the display shows:

```
R VALUE?
```

Type 5 [END LINE], and the display shows the main menu again:

```
Nw Ad Dl Ch Pr Fl O ?
```

To see the effect of this change, press [O], and answer the output questions as before—the questions dealing with output node (node 8), no delay, and linear sweep. Select the same sweep limits (800, 1200, 10). The analysis of the changed circuit is as follows:*

* This analysis was produced on an HP 82905B Printer. Refer to page 55 for a discussion of the print option.

FREQ,Hz	dB	PHASE,deg
800.000	-21.51	-92.8
810.000	-21.02	-93.5
820.000	-20.51	-94.4
830.000	-19.98	-95.3
840.000	-19.43	-96.3
850.000	-18.85	-97.4
860.000	-18.24	-98.7
870.000	-17.60	-100.1
880.000	-16.93	-101.7
890.000	-16.21	-103.5
900.000	-15.45	-105.6
910.000	-14.65	-108.2
920.000	-13.79	-111.1
930.000	-12.88	-114.7
940.000	-11.92	-119.1
950.000	-10.93	-124.5
960.000	-9.92	-131.2
970.000	-8.96	-139.5
980.000	-8.14	-149.6
990.000	-7.58	-161.3
1000.0	-7.40	-173.9
1010.0	-7.63	173.6
1020.0	-8.20	162.4
1030.0	-9.00	153.0
1040.0	-9.89	145.3
1050.0	-10.81	139.1
1060.0	-11.70	134.0
1070.0	-12.55	130.0
1080.0	-13.35	126.6
1090.0	-14.10	123.9
1100.0	-14.80	121.5
1110.0	-15.45	119.5
1120.0	-16.06	117.8
1130.0	-16.63	116.3
1140.0	-17.17	115.0
1150.0	-17.67	113.8
1160.0	-18.15	112.8
1170.0	-18.60	111.9
1180.0	-19.03	111.0
1190.0	-19.43	110.3
1200.0	-19.82	109.6

The changing of the transformer primary resistance from 50 ohms to 5 ohms clearly has the desired effect. Hence, the low Q was the source of the problem as suspected.

Example 2: Deliyannis Active Resonator

In figure 3-2, a second-order Deliyannis active resonator is designed using a type 741 operational amplifier.*

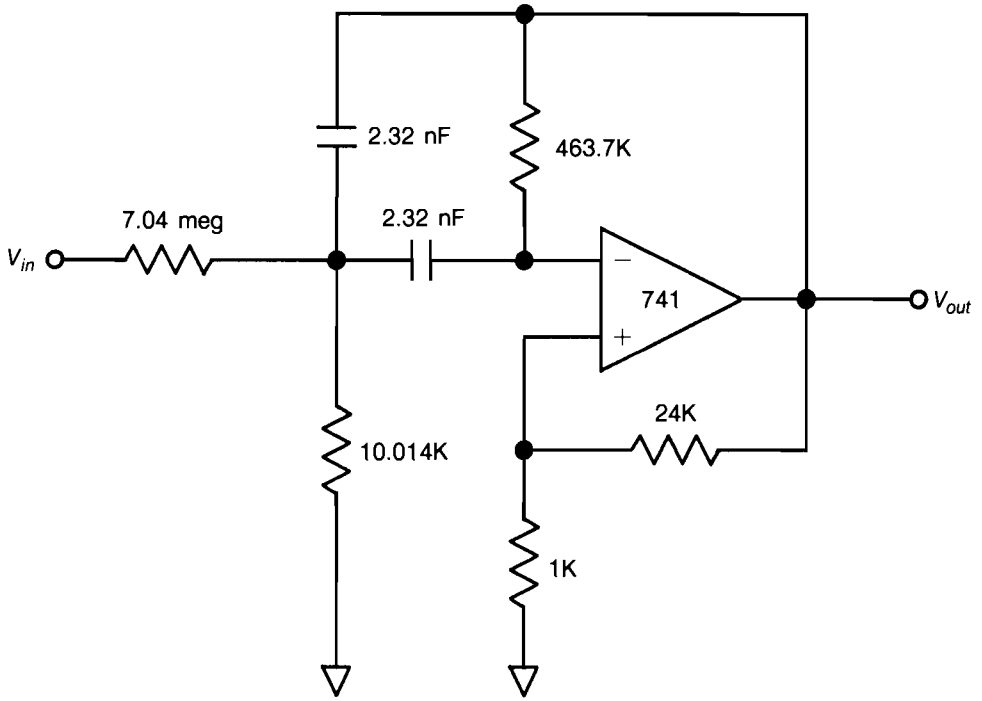


Figure 3-2

* This example appears in *Handbook of Electronic Design and Analysis Procedures Using Programmable Calculators*, B. K. Murdock, Van Nostrand Reinhold Co., N.Y., 1979.

The operational amplifier characteristics and the resonator specifications are:

Center Frequency: 1000 Hz
Resonant Q: 100
Gain at Resonance: 1.0 (0 dB)
Capacitor Ratio: 1.0
Positive Feedback Ratio: 0.04
Design Resistance Level: 10000 ohms
Op Amp Gain-Bandwidth: 500,000 Hz
Op Amp DC Gain: 100,000 V/V

The following model is used to represent the operational amplifier:

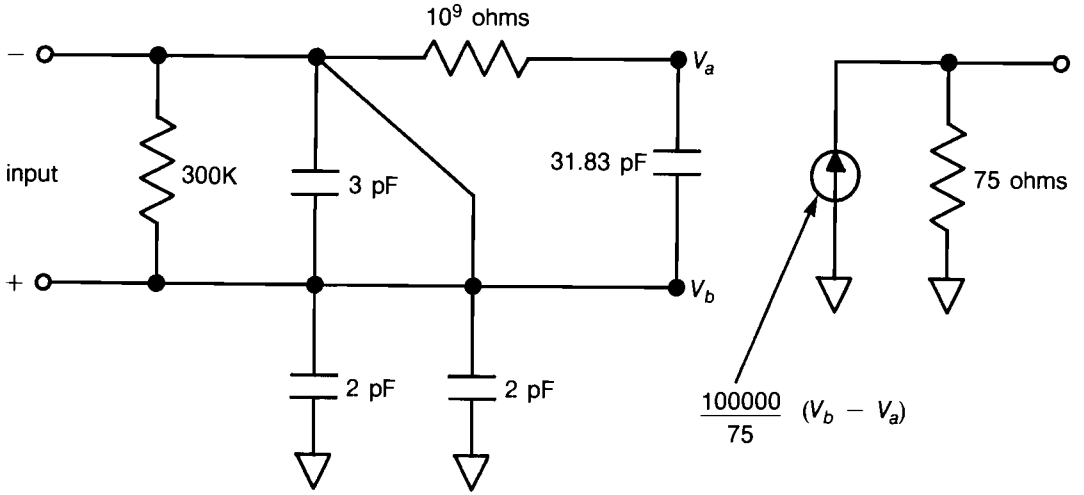


Figure 3-3

The 300K resistor and the 3-pF capacitor simulate the input impedance of the op amp. The 2-pF capacitors represent the parasitic input capacitance from the input leads to the case. The 10^9-ohm resistor and the 31.83-pF capacitor simulate the op amp compensation pole in a manner that does not load the input circuit. The compensation pole has a break frequency of 5 Hz. The controlled current source and the 75-ohm resistor model the op amp dc gain and output impedance.

When the op amp is combined with the active filter circuit, the following model results. This model is in the proper format for CNAP analysis.

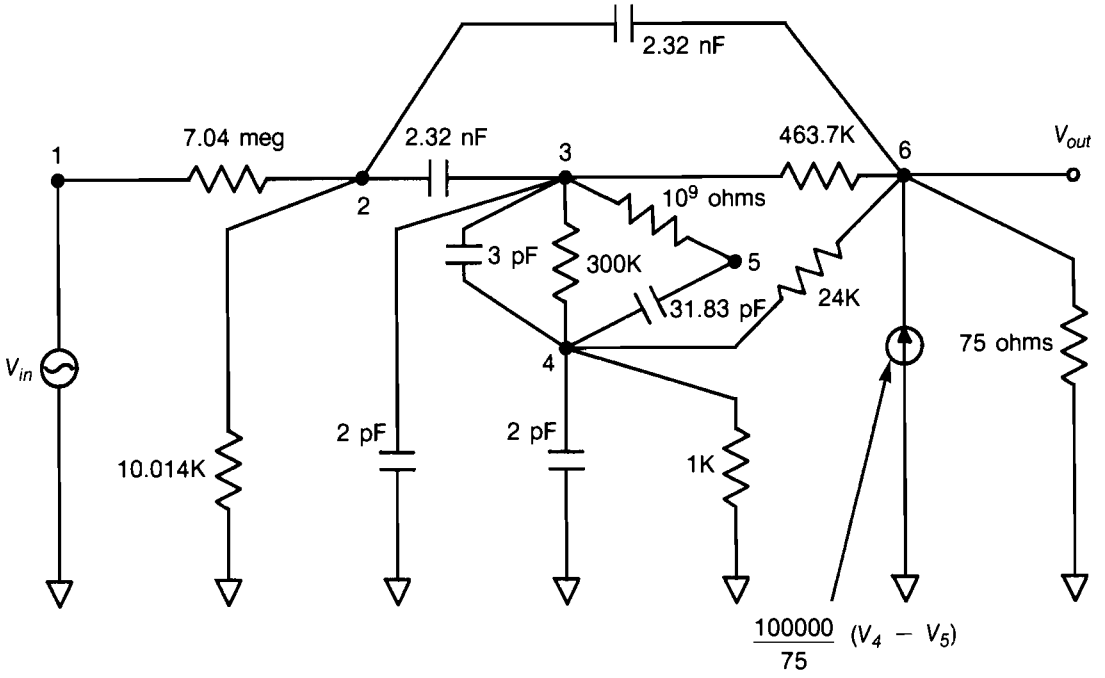


Figure 3-4

After CNAP is run, the maximum number of nodes is displayed, followed by the main menu:

```
Nw Ad Dl Ch Pr Fl O ?
```

Since this circuit is new, press [N], and the element selection menu appears.

Input/Result

```
R L C Vc Xm Os Ss E ?
```

R

Selects a resistor.

```
R; FROM, TO? ■
```

1,2 END LINE

```
R VALUE? ■
```

7.04E6 END LINE

```
R L C Vc Xm Os Ss E ?
```

R

Selects a resistor.

```
R; FROM, TO? ■
```

2,0 END LINE

```
R VALUE? ■
```

10014 END LINE

```
R L C Vc Xm Os Ss E ?
```

Input/Result

C

Selects a capacitor.

```
C; FROM, TO? ■
```

2,3 END LINE

```
C VALUE? ■
```

2.32E-9 END LINE

```
R L C Vc Xm Os Ss E ?
```

C

Selects a capacitor.

```
C; FROM, TO? ■
```

2,6 END LINE

```
C VALUE? ■
```

2.32E-9 END LINE

```
R L C Vc Xm Os Ss E ?
```

C

Selects a capacitor.

```
C; FROM, TO? ■
```

3,0 END LINE

```
C VALUE? ■
```

Input/Result

2E-12 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[C] Selects a capacitor.

```
C; FROM, TO? ■
```

3,4 [END LINE]

```
C VALUE? ■
```

3E-12 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[R] Selects a resistor.

```
R; FROM, TO? ■
```

3,4 [END LINE]

```
R VALUE? ■
```

3E5 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

Input/Result

R

Selects a resistor.

```
R; FROM, TO? ■
```

3,5 END LINE

```
R VALUE? ■
```

1E9 END LINE

```
R L C Vc Xm Os Ss E ?
```

C

Selects a capacitor.

```
C; FROM, TO? ■
```

5,4 END LINE

```
C VALUE? ■
```

31.83E-12 END LINE

```
R L C Vc Xm Os Ss E ?
```

C

Selects a capacitor.

```
C; FROM, TO? ■
```

4,0 END LINE

```
C VALUE? ■
```

Input/Result

2E-12 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[R] Selects a resistor.

```
R; FROM, TO? ■
```

4,0 [END LINE]

```
R VALUE? ■
```

1000 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[R] Selects a resistor.

```
R; FROM, TO? ■
```

4,6 [END LINE]

```
R VALUE? ■
```

24000 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[R] Selects a resistor.

```
R; FROM, TO? ■
```

Input/Result

3,6 END LINE

```
R VALUE? ■
```

463700 END LINE

```
R L C Vc Xm Os Ss E ?
```

R — Selects a resistor.

```
R; FROM, TO? ■
```

0,6 END LINE

```
R VALUE? ■
```

75 END LINE

```
R L C Vc Xm Os Ss E ?
```

V — Selects a voltage-controlled current source.

```
VCCS; FROM, TO? ■
```

0,6 END LINE

```
gm=? ■
```

100000/75 END LINE

```
CONTROL NODES: +, -? ■
```

Input/Result

4,5 [END LINE]

```
R L C Vc Xm Os Ss E ?
```

[E]

Exits the element menu. The main menu is displayed.

```
Nw Ad Dl Ch Pr Fl O ?
```

At this point the circuit description is complete. The following procedures show how you can write the circuit to a file.

Input/Result

[F]

Selects file manipulation option.

```
FILE NAME ? ■
```

EXAMPL2 [END LINE]

Enters file name.


```
Read or Write file ?
```

[W]

Selects option to write the file to EXAMPL2.

```
Nw Ad Dl Ch Pr Fl O ?
```

Next, the circuit description is printed for documentation and error checking. You respond to the main menu by pressing [P]. If the HP-IL module is installed, the program asks:

```
use printer, Y/N?
```

If you have an HP-IL printer attached and press [Y], the following printout occurs:

CIRCUIT DESCRIPTION OF
EXAMPL2

[FM,TO]	TYPE	VALUE
BRANCH 1		
[1,2]	R	7.040 M
BRANCH 2		
[2,0]	R	10.01 K
BRANCH 3		
[2,3]	C	2.320 nF
BRANCH 4		
[2,6]	C	2.320 nF
BRANCH 5		
[3,0]	C	2.000 pF
BRANCH 6		
[3,4]	C	3.000 pF
BRANCH 7		
[3,4]	R	300.0 K
BRANCH 8		
[3,5]	R	1.000 G
BRANCH 9		
[5,4]	C	31.83 pF
BRANCH 10		
[4,0]	C	2.000 pF
BRANCH 11		
[4,0]	R	1.000 K
BRANCH 12		
[4,6]	R	24.00 K
BRANCH 13		
[3,6]	R	463.7 K
BRANCH 14		
[0,6]	R	75.00
BRANCH 15		
[0,6]	VCCS	1.333 KS
ctrl nodes:		+ 4 , - 5

The printout shows that the circuit description is correct. The output mode is selected by pressing [O] in response to the main menu. The display shows:

```
CALC REAL MATRIX ELEM
```

After this operation is complete, the display shows:

```
OUTPUT NODE ? 6
```

Since the highest numbered node was set to be the output node, no answer is required (just press [END LINE]). Next, the display shows:

```
group delay, Yes/No?
```

To demonstrate this function, press [Y]. The display shows:

```
loG or liN sweep ?
```

In this example, first select log sweep so that the global response of the filter can be seen (press [G]). The sweep is from 100 Hz to 10 kHz with 20 steps per decade. Thus, when the display shows:

```
START,STOP,#PTS/DEC? ■
```

You type `100,10000,20` [END LINE] and the display shows:

```
use printer, Y/N?
```

If you have an HP-IL printer attached and press [Y], the following printout occurs:

FREQ,Hz	dB	PHASE,deg	DELAY,sec
100.000	-59.91	-90.1	2.45E-06
112.202	-58.89	-90.1	2.47E-06
125.893	-57.86	-90.1	2.49E-06
141.254	-56.82	-90.1	2.52E-06
158.489	-55.78	-90.1	2.55E-06
177.828	-54.72	-90.2	2.60E-06
199.526	-53.65	-90.2	2.66E-06
223.872	-52.55	-90.2	2.73E-06
251.189	-51.43	-90.2	2.83E-06
281.838	-50.28	-90.3	2.96E-06
316.228	-49.08	-90.3	3.13E-06
354.813	-47.83	-90.3	3.37E-06
398.107	-46.50	-90.4	3.71E-06
446.684	-45.06	-90.5	4.19E-06
501.187	-43.48	-90.6	4.94E-06
562.341	-41.69	-90.7	6.14E-06
630.957	-39.58	-90.9	8.30E-06
707.946	-36.95	-91.1	1.28E-05
794.328	-33.33	-91.7	2.51E-05
891.251	-27.24	-93.3	8.82E-05

FREQ,Hz	dB	PHASE,deg	DELAY,sec
1000.0	-2.28	175.7	2.44E-02
1122.0	-27.32	93.1	6.90E-05
1258.9	-33.37	91.4	1.58E-05
1412.5	-36.98	90.9	6.55E-06
1584.9	-39.60	90.6	3.49E-06
1778.3	-41.71	90.4	2.16E-06
1995.3	-43.50	90.3	1.48E-06
2238.7	-45.08	90.1	1.10E-06
2511.9	-46.51	90.1	8.66E-07
2818.4	-47.84	90.0	7.14E-07
3162.3	-49.09	89.9	6.12E-07
3548.1	-50.29	89.8	5.41E-07
3981.1	-51.44	89.7	4.90E-07
4466.8	-52.56	89.6	4.52E-07
5011.9	-53.65	89.6	4.25E-07
5623.4	-54.73	89.5	4.04E-07
6309.6	-55.79	89.4	3.88E-07
7079.5	-56.83	89.3	3.76E-07
7943.3	-57.87	89.1	3.66E-07
8912.5	-58.90	89.0	3.59E-07
10000.0	-59.92	88.9	3.53E-07

If printout is not selected, the output is formatted for the display.

The linear sweep mode is used to go back and examine the passband behavior in more detail. When the output frequency sweep is finished, the main menu reappears. You again press [O] to access the output mode. The output node and group delay questions are answered as before (node 6 is the output node and you want group delay). In response to the `loG/liN` sweep question, linear mode is selected by pressing [N]. The display then shows:

```
START,STOP,INCR? ■
```

The passband center is nominally 1000 Hz. The frequency sweep is 950 to 1050 Hz. A frequency increment of 5 Hz is chosen, so you type `950,1050,5` [END LINE]. The analysis then commences:

FREQ,Hz	dB	PHASE,deg	DELAY,sec
950.000	-20.22	-97.4	4.14E-04
955.000	-19.29	-98.2	5.10E-04
960.000	-18.25	-99.2	6.43E-04
965.000	-17.09	-100.6	8.36E-04
970.000	-15.76	-102.3	1.13E-03
975.000	-14.22	-104.7	1.60E-03
980.000	-12.37	-108.3	2.44E-03
985.000	-10.11	-114.0	4.08E-03
990.000	-7.29	-124.2	7.78E-03
995.000	-3.99	-145.1	1.65E-02
1000.0	-2.28	175.7	2.44E-02
1005.0	-4.58	139.8	1.42E-02
1010.0	-7.80	121.8	6.78E-03
1015.0	-10.46	112.8	3.65E-03
1020.0	-12.58	107.6	2.23E-03
1025.0	-14.32	104.3	1.49E-03
1030.0	-15.77	102.1	1.06E-03
1035.0	-17.02	100.4	7.92E-04
1040.0	-18.11	99.1	6.13E-04
1045.0	-19.08	98.2	4.88E-04
1050.0	-19.95	97.4	3.98E-04

The passband response at resonance is supposed to be 0 dB. The previous response listing shows the response to be −2.28 dB instead. A narrower linear sweep could be done to look at the resonance peak.

The Deliyannis design procedure accounts for the compensation pole of the op amp, but it does not take into account the parasitic capacitances and resistances present at the op amp input. Because of these parasitic elements, the resonator doesn't peak at the design resonant frequency of 1000 Hz. The main element that causes this resonance shift is the 300-kohm op amp input resistance. The Delete function is used to remove this resistor from the circuit under analysis, so its circuit effect can be seen. To access the Delete function, press [D]. The program displays:

```
FROM NODE, TO NODE?
```

Since the 300-kohm input resistor is between nodes 3 and 4, type `3,4` [END LINE], and the display responds:

```
[NODES:3,4]  C 3pF Save/Delete? *
```

We don't want to delete this branch, so press [S] to search for the next branch connected between nodes 3 and 4. The display then shows:

```
R 300K Save/Delete?
```

* Since the HP-71 display contains only 22 characters, the first part of the display scrolls to the left.

This is the branch we want to delete. Press [D] and the branch is deleted. The main menu appears, and the output sequence can again be selected. A linear sweep of 990 to 1010 Hz in 1-Hz increments is selected. The printer output resulting from this new analysis is shown below:

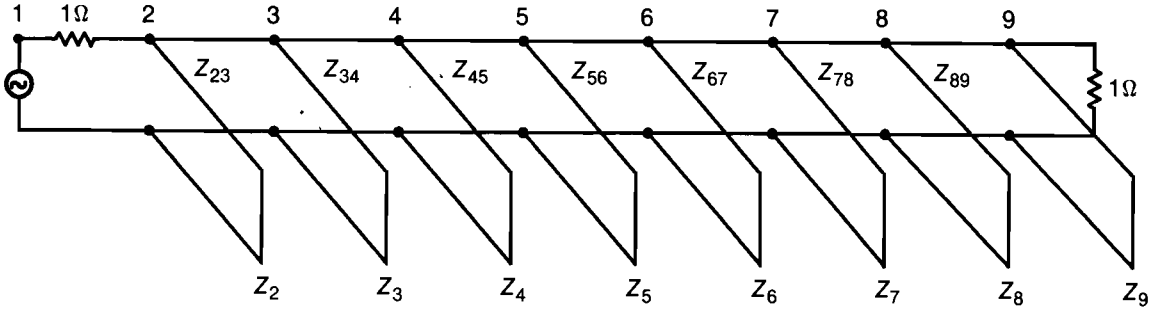
FREQ,Hz	dB	PHASE,deg	DELAY,sec
990.000	-6.99	-115.9	6.25E-03
991.000	-6.26	-118.4	7.39E-03
992.000	-5.49	-121.3	8.82E-03
993.000	-4.67	-124.8	1.06E-02
994.000	-3.81	-129.0	1.29E-02
995.000	-2.92	-134.2	1.58E-02
996.000	-2.03	-140.5	1.95E-02
997.000	-1.18	-148.3	2.36E-02
998.000	-4.52E-001	-157.6	2.79E-02
999.000	+5.18E-002	-168.3	3.13E-02
1000.0	+2.37E-001	180.1	3.27E-02
1001.0	+6.31E-002	168.4	3.13E-02
1002.0	-4.30E-001	157.7	2.79E-02
1003.0	-1.15	148.4	2.37E-02
1004.0	-1.98	140.6	1.95E-02
1005.0	-2.87	134.3	1.59E-02
1006.0	-3.75	129.1	1.29E-02
1007.0	-4.60	124.8	1.06E-02
1008.0	-5.41	121.3	8.83E-03
1009.0	-6.18	118.4	7.40E-03
1010.0	-6.90	116.0	6.26E-03

Now the magnitude is 0.24 dB high at resonance. This is caused by the input capacitors. If you delete these elements and run the output analysis again, the response indeed does peak with close to 0-dB gain at center frequency.

Example [illegible] Transmission [illegible] and Stub [illegible]

This example demonstrates two new features of CHAP: the use of transmission lines and stubs, and the ability to change the output format with a separate BASIC program.

The following figure* is a 0.10-dB ripple Chebyshev filter with eight reactive elements and a loaded Q of 1.54. This filter is constructed from quarter-wave transmission line segments and quarter-wave shorted stubs, with the values printed below.



All transmission lines and shorted stubs are λ/4

Figure 3-5

```
CIRCUIT DESCRIPTION OF
EXAMPL3

[FM,TO] TYPE    VALUE

BRANCH  1
[1,2] R         1.000

BRANCH  2
[2,0] S-STUB 959.7 m      (Z2)
1/4 F:      1.000  Hz

BRANCH  3
[2,0] X-LINE 776.4 m      (Z23)
 3   0 1/4 F: 1.000  Hz

BRANCH  4
[3,0] S-STUB 487.8 m      (Z3)
1/4 F:      1.000  Hz

BRANCH  5
[3,0] X-LINE 733.1 m      (Z34)
 4   0 1/4 F: 1.000  Hz
```

* Matthaei, Young, and Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, McGraw-Hill, 1964.

```
BRANCH  6
[4,0] S-STUB 488.0 m      (Z4)
1/4 F:     1.000  Hz

BRANCH  7
[4,0] X-LINE 774.0 m      (Z45)
 5   0 1/4 F: 1.000  Hz

BRANCH  8
[5,0] S-STUB 479.2 m      (Z5)
1/4 F:     1.000  Hz

BRANCH  9
[5,0] X-LINE 783.1 m      (Z56)
 6   0 1/4 F: 1.000  Hz

BRANCH 10
[6,0] S-STUB 479.2 m      (Z6)
1/4 F:     1.000  Hz

BRANCH 11
[6,0] X-LINE 774.0 m      (Z67)
 7   0 1/4 F: 1.000  Hz

BRANCH 12
[7,0] S-STUB 488.0 m      (Z7)
1/4 F:     1.000  Hz

BRANCH 13
[7,0] X-LINE 733.1 m      (Z78)
 8   0 1/4 F: 1.000  Hz

BRANCH 14
[8,0] S-STUB 487.8 m      (Z8)
1/4 F:     1.000  Hz

BRANCH 15
[8,0] X-LINE 776.4 m      (Z89)
 9   0 1/4 F: 1.000  Hz

BRANCH 16
[9,0] S-STUB 959.7 m      (Z9)
1/4 F:     1.000  Hz

BRANCH 17
[9,0] R       1.000
```

To demonstrate the ability to modify program output, both the filter input impedance and transmission function will be calculated and printed. New output headings will also be printed. The program CHAP calls subprograms HEAD for the column headings and OUT to calculate and print the column values. The HP-71 first searches main memory (RAM) for these subprogram names before searching the module (ROM). Hence, having the subprograms HEAD and OUT in RAM will allow the user to control these subprogram functions.

Key in the following subprogram in file HEAD.

```
5000 SUB HEAD(Q7,G8)
5010 IF NOT G8 THEN DISP "HZ,R(Z),I(Z),dB,PHASE" @ GOTO 5030
5020 PRINT "     FREQ     Re(Z)     Im(Z)      dB       PHASE " @ PRINT
5030 END SUB
```

Before the subprogram OUT can be written, the equations for calculating the filter input impedance must be developed as follows:

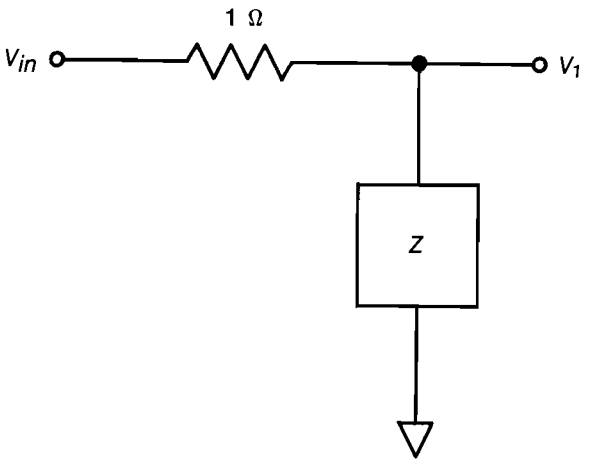


Figure 3-6

Given:

$$\frac{V_1}{V_{in}} = K = \frac{Z}{(Z + 1)}$$

$$V_{in} = 1$$

This can be rewritten as:

$$Z = \frac{K}{(1 - K)} = \left(\frac{1}{K} - 1\right) = \left(\frac{1}{V_1} - 1\right)$$

If S is the real part of V_1, T is the imaginary part of V_1, and $M = S^2 + T^2$, then:

$$Z = \frac{M}{(S - M) - jT}$$

Replacing $(S-M)$ with S gives:

$$Z = \frac{M}{S^2 + T^2} \times (S + jT)$$

The subprogram OUT is then written as follows. (The transmission function in dB and angle is calculated on line 4020, while the input impedance is calculated on line 4030.) Key in the subprogram in file OUT.

```
4000 SUB OUT(N,N1,Q2,Q7,F3,F4,V(),V1(),U(),U1(),G8)
4010 S=V(1) @ T=V1(1) @ S1=V(N1-1) @ T1=V1(N1-1) @ IF NOT G8 THEN
DELAY 8 @ PRINTER IS *
4020 M=10*LOG10(S1*S1+T1*T1) @ A=ANGLE(S1,T1)
4030 M1=S*S+T*T @ S=S-M1 @ M1=M1/(S*S+T*T)
4040 S=M1*S @ T=M1*T
4050 PRINT USING "4(5D.3D),6D.D";F3,S,T,M,A
4060 END SUB
```

After these subprograms are in main memory under their respective names, HEAD and OUT, CNAP is run in the normal manner—by typing RUN CNAP.
After displaying the maximum number of nodes possible,* the display shows the main menu:

```
Nw Ad Dl Ch Pr Fl O ?
```

Since this circuit is new, press [N], and the element menu appears:

```
R L C Vc Xm Os Ss E ?
```

Enter the elements of the circuit detailed on page 61. The elements of the network can be entered in any order. For this network they are entered from left to right.

When the circuit is entered, exit the element selection menu. The circuit can now be analyzed by selecting the output mode ([O] is pressed in response to the main menu), and the display shows:

```
CALC REAL MATRIX ELEM
```

After this operation finishes, the display shows:

```
OUTPUT NODE ? 9
```

Since the highest numbered node is the output node, no answer is needed; just press [END LINE].

Looking back at the OUT auxillary output subprogram, the parameter N1 was passed. N1 is the output node specified above and is used to find the appropriate voltage vector elements.

Next, the display shows:

```
group delay, Yes/No?
```

The auxillary output routine that was written doesn't calculate group delay. You respond by pressing [N].

Next the display shows:

```
loG or liN sweep ?
```

Linear sweep is desired, so press [N]. The display shows:

```
START,STOP,INCR? ■
```

This is a normalized bandpass filter. Select sweep limits of 0.2 and 1.8, with steps of 0.05 by pressing `.2,1.8,.05` [END LINE]. If you have an HP-IL module installed, the display shows:

```
use printer, Y/N?
```

If you have an HP-IL printer attached and press [Y], the printout commences using the column headings and format specified by subprograms HEAD and OUT respectively.*

* Do not be concerned if the HP-71 beeps and displays warnings during the analysis. Because DEFAULT ON is set, the HP-71 makes assumptions about certain math exceptions and continues the calculation using default values. For more information on math exceptions, refer to "Recovering From Math Exceptions" in section 2 of the *HP-71 Owner's Manual.*

FREQ	Re(Z)	Im(Z)	dB	PHASE
.200	.000	.171	-77.909	70.5
.250	.000	.222	-73.634	65.0
.300	.000	.279	-69.082	58.8
.350	.000	.346	-64.057	51.8
.400	.000	.428	-58.365	43.6
.450	.000	.536	-51.765	33.6
.500	.000	.694	-43.899	20.5
.550	.001	.977	-34.132	1.3
.600	.036	1.875	-21.105	-33.9
.650	1.293	-.850	-6.651	-140.6
.700	1.089	.034	-6.030	109.8
.750	.829	.211	-6.116	32.5
.800	1.037	.058	-6.026	-34.5
.850	.742	.028	-6.118	-97.0
.900	.878	.204	-6.090	-155.4
.950	.940	-.083	-6.033	146.5
1.000	.736	0.000	-6.122	90.0
1.050	.940	.083	-6.033	33.5
1.100	.878	-.204	-6.090	-24.6
1.150	.742	-.028	-6.118	-83.0
1.200	1.037	-.058	-6.026	-145.5
1.250	.829	-.211	-6.116	147.5
1.300	1.089	-.034	-6.030	70.2
1.350	1.293	.850	-6.651	-39.4
1.400	.036	-1.875	-21.105	-146.1
1.450	.001	-.977	-34.132	178.7
1.500	.000	-.694	-43.899	159.5
1.550	.000	-.536	-51.765	146.4
1.600	.000	-.428	-58.365	136.4
1.650	.000	-.346	-64.057	128.2
1.700	.000	-.279	-69.082	121.2
1.750	.000	-.222	-73.634	115.0
1.800	.000	-.171	-77.909	109.5

Appendix A

Owner's Information

Maintenance

The circuit analysis module does not require maintenance. However, there are several precautions, listed below, that you should observe.

CAUTIONS

- Do not place fingers, tools, or other objects into the plug-in ports. Damage to plug-in module contacts and the computer internal circuitry may result.
- Turn off the computer (press [f] [OFF]) before installing or removing a plug-in module.
- If a module jams when inserted into a port, it may be upside down. Attempting to force it further may result in damage to the computer or the module.
- Handle the plug-in modules very carefully while they are out of the computer. Do not insert any objects in the module connector socket. Always keep a blank module in the computer port when a module is not installed. Failure to observe these cautions may result in damage to the module or the computer.

Limited One-Year Warranty

What We Will Do

The HP 82481A Circuit Analysis Pac is warranted by Hewlett-Packard against defects in materials and workmanship affecting electronic and mechanical performance, but not software content, for one year from the date of original purchase. If you sell your unit or give it as a gift, the warranty is transferred to the new owner and remains in effect for the original one-year period. During the warranty period, we will repair or, at our option, replace at no charge a product that proves to be defective, provided you return the product, shipping prepaid, to a Hewlett-Packard service center.

What Is Not Covered

This warranty does not apply if the product has been damaged by accident or misuse or as the result of service or modification by other than an authorized Hewlett-Packard service center.

No other express warranty is given. The repair or replacement of a product is your exclusive remedy. **ANY OTHER IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS IS LIMITED TO THE ONE-YEAR DURATION OF THIS WRITTEN WARRANTY**. Some states, provinces, or countries do not allow limitations on how long an implied warranty lasts, so the above limitation may not apply to you. **IN NO EVENT SHALL HEWLETT-PACKARD COMPANY BE LIABLE FOR CONSEQUENTIAL DAMAGES**. Some states, provinces, or countries do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights that vary from state to state, province to province, or country to country.

Warranty for Consumer Transactions in the United Kingdom

This warranty shall not apply to consumer transactions and shall not affect the statutory rights of a consumer. In relation to such transactions, the rights and obligations of Seller and Buyer shall be determined by statute.

Obligation to Make Changes

Products are sold on the basis of specifications applicable at the time of manufacture. Hewlett-Packard shall have no obligation to modify or update products once sold.

Warranty Information

If you have any questions concerning this warranty, please contact an authorized Hewlett-Packard dealer or a Hewlett-Packard sales and service office. Should you be unable to contact them, please contact:

- In the United States:

Hewlett-Packard Company
Personal Computer Group
Customer Support
11000 Wolfe Road
Cupertino, CA 95014
(800) FOR-HPPC
(800 367-4772)

- In Europe:

Hewlett-Packard S.A.
150, route du Nant d'Avril
P.O. Box CH-1217 Meyrin 2
Geneva
Switzerland
Telephone: (022) 83 81 11

Note: Do *not* send units to this address for repair.

- In other countries:

Hewlett-Packard Intercontinental
3495 Deer Creek Rd.
Palo Alto, California 94304
U.S.A.
Telephone: (415) 857-1501

Note: Do *not* send units to this address for repair.

Service

Service Centers

Hewlett-Packard maintains service centers in most major countries throughout the world. You may have your unit repaired at a Hewlett-Packard service center any time it needs service, whether the unit is under warranty or not. There is a charge for repairs after the one-year warranty period.

Hewlett-Packard products are normally repaired and reshipped within five (5) working days of receipt at any service center. This is an average time and could vary depending upon the time of year and the work load at the service center. The total time you are without your unit will depend largely on the shipping time.

Obtaining Repair Service in the United States

The Hewlett-Packard United States Service Center for battery-powered computational products is located in Corvallis, Oregon:

Hewlett-Packard Company
Service Department
P.O. Box 999
Corvallis, Oregon 97339, U.S.A.
or
1030 N.E. Circle Blvd.
Corvallis, Oregon 97330, U.S.A.
Telephone: (503) 757-2000

Obtaining Repair Service in Europe

Service centers are maintained at the following locations. For countries not listed, contact the dealer where you purchased your unit.

AUSTRIA
HEWLETT-PACKARD Ges.m.b.H.
Kleinrechner-Service
Wagramerstrasse-Lieblgasse 1
A-1220 Wien (Vienna)
Telephone: (0222) 23 65 11

BELGIUM
HEWLETT-PACKARD BELGIUM SA/NV
Woluwedal 100
B-1200 Brussels
Telephone: (02) 762 32 00

DENMARK
HEWLETT-PACKARD A/S
Datavej 52
DK-3460 Birkerod (Copenhagen)
Telephone: (02) 81 66 40

EASTERN EUROPE
Refer to the address listed under Austria.

FINLAND
HEWLETT-PACKARD OY
Revontulentie 7
SF-02100 Espoo 10 (Helsinki)
Telephone: (90) 455 02 11

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Service Repair Charge

There is a standard repair charge for out-of-warranty repairs. The repair charges include all labor and materials. In the United States, the full charge is subject to the customer's local sales tax. In European countries, the full charge is subject to Value Added Tax (VAT) and similar taxes wherever applicable. All such taxes will appear as separate items on invoiced amounts.

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Service Warranty

Any out-of-warranty repairs are warranted against defects in materials and workmanship for a period of 90 days from date of service.

Shipping Instructions

Should your unit require service, return it with the following items:

- A completed Service Card, including a description of the problem.
- A sales receipt or other proof of purchase date if the one-year warranty has not expired.

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Whether the unit is under warranty or not, it is your responsibility to pay shipping charges for delivery to the Hewlett-Packard service center.

After warranty repairs are completed, the service center returns the unit with postage prepaid. On out-of-warranty repairs in the United States and some other countries, the unit is returned C.O.D. (covering shipping costs and the service charge).

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(800) FOR-HPPC
(800 367-4772)

Technical Assistance. For technical assistance with your product, call the number below:

(408) 725-2600

For either product information or technical assistance, you can also write to:

Hewlett-Packard
Personal Computer Group
Customer Support
11000 Wolfe Road
Cupertino, CA 95014

Appendix B

The Crout Reduction

Crout's method is used to solve a set of n linear algebraic equations in n unknowns. Crout's method is the LU (lower/upper) factorization technique of triangularizing a matrix. It is systematized to minimize the number of calculations required. The details and analytic justification of Crout's method are presented in either Hildebrand or Maron.*

Given a set of equations:

$$\begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1n} \\ a_{21} & a_{22} & \cdots & a_{2n} \\ \vdots & \vdots & \cdots & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nn} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix} = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{bmatrix}$$

The independent **Y** vector is included in the coefficient matrix of the system to form the *augmented matrix* of the system:

$$\mathbf{A} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1n} & y_1 \\ a_{21} & a_{22} & \cdots & a_{2n} & y_2 \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nn} & y_n \end{bmatrix}$$

* F.B. Hildebrand, *Methods of Applied Mathematics*, Prentice-Hall, 1952. Maron, Melvin J., *Numerical Analysis, A Practical Approach*, McMillan, 1982.

The elements of this augmented matrix are processed to yield an auxillary matrix:

$$\mathbf{B} = \begin{bmatrix} b_{11} & b_{12} & \cdots & b_{1n} & u_1 \\ b_{21} & b_{22} & \cdots & b_{2n} & u_2 \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ b_{n1} & b_{n2} & \cdots & b_{nn} & u_n \end{bmatrix}$$

Both matrices have the same dimensions. Initially, the auxillary matrix is all zero. The elements of **B** are then generated from the elements of **A** using the following rules:

1. The elements of **B** are generated in the following order: elements of the first column, then elements of the first row to the right of the first column; elements of the second column below the first row, then elements of the second row to the right of the second column; etc., until all elements are determined. This ordering is shown below:

$$\begin{bmatrix} a_{11}\,① & a_{12}\,② \rightarrow & a_{13} & \cdots & a_{1n} & y_1 \\ a_{21} & a_{22}\,③ & a_{23}\,④ \rightarrow & \cdots & a_{2n} & y_2 \\ a_{31} & a_{32} & a_{33}\,⑤ & \cdots & a_{3n} & y_3 \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\ a_{n1} & a_{n2} & a_{n3} & \cdots & a_{nn} & y_n \end{bmatrix}$$

2. The first column of **B** is the same as the first column of **A**. Each element of the first row to the right of the first column in **B** is obtained by dividing the corresponding element in **A** by a_{11}.
3. Each element b_{ij} on or below the main diagonal of **B** is obtained by subtracting from a_{ij} the sum of the products of the corresponding elements in the ith row and jth column of **B**, remembering that all uncalculated elements in **B** are zero, i.e.:

$$b_{ij} = a_{ij} - \sum_{k=1}^{j-1} b_{ik} \cdot b_{kj} \qquad i \geqslant j$$

4. Each element in **B** to the right of the main diagonal is calculated according to rule 3 on the previous page, and then normalized by b_{ii} in **B**, i.e.:

$$b_{ij} = \frac{a_{ij} - \sum_{k=1}^{i-1} b_{ik}\, b_{kj}}{b_{ii}} \qquad i < j$$

Notice that the Crout reduction procedure requires the **A** matrix to have nonzero main diagonal elements. In the case of nodal analysis, this requirement is automatically met provided at least one branch is connected to each node. Furthermore, the **A** matrix entries resulting from nodal analysis are complex numbers, and all of the above calculations must be carried out using complex arithmetic.

After the auxiliary matrix has been calculated, the solution vector **X** is obtained using the following three rules:

1. The elements of **X** are determined in order from the highest to the lowest: x_n, x_{n-1}, x_{n-2}, ..., x_2, x_1
2. x_n equals b_n.
3. Each x_i is obtained by subtracting from u_i the sum of the products of the ith row in **B** and the current **X** vector. Before this operation begins, all elements of **X** are set to zero. In equation form, these operations are:

$$x_i = u_i - \sum_{k=i+1}^{n} b_{ik} \cdot x_k$$

The Crout reduction algorithm from the output portion of CNAP is reproduced on the next page. The variables are:

B(,) and G(,) are the real and imaginary components of the augmented matrix.

B1(,) and G1(,) are the real and imaginary parts of the auxillary matrix, and have been previously set to zero before entering this routine.

V( ) and V1( ) are the real and imaginary parts of the node voltage solution vector.

```
247 FOR L=1 TO N
```

Operate on column.

```
    @ FOR I=L TO N
248 U9=0 @ V9=0 @ FOR H=1 TO L-1
249 U9=U9+G1(I,H)*G1(H,L)-B1(I,H)*B1(H,L) @ V9=V9+G1(I,H)*B1(H,L)+
B1(I,H)*G1(H,L) @ NEXT H
250 G1(I,L)=G(I,L)-U9 @ B1(I,L)=B(I,L)-V9 @ NEXT I
```

Operate on row.

```
    @ FOR J=L+1 TO N+1
251 U9=0 @ V9=0 @ FOR H=1 TO L-1
252 U9=U9+G1(L,H)*G1(H,J)-B1(L,H)*B1(H,J) @ V9=V9+G1(L,H)*B1(H,J)+
B1(L,H)*G1(H,J) @ NEXT H
253 W=G1(L,L) @ X=B1(L,L) @ M=W*W+X*X
254 IF M=0 THEN GOTO 274
255 U9=G(L,J)-U9 @ V9=B(L,J)-V9 @ G1(L,J)=(U9*W+V9*X)/M @ B1(L,J)=
(V9*W-U9*X)/M
256 NEXT J
```

Calculate solution vector.

```
    @ NEXT L @ V(N+1)=0 @ V1(N+1)=0 @ FOR I=N TO 1 STEP -1
257 U9=0 @ V9=0 @ FOR H=I+1 TO N
258 U9=U9+G1(I,H)*V(H)-B1(I,H)*V1(H) @ V9=V9+G1(I,H)*V1(H)+B1(I,H)
*V(H) @ NEXT H
259 V(I)=G1(I,N+1)-U9 @ V1(I)=B1(I,N+1)-V9 @ NEXT I @ RETURN
```

Appendix C

List of Files and Variables

Files

The circuit analysis module contains five named files. These names must not be used as the names of files in user memory, as the HP-71 first searches its own memory before searching the plug-in modules. The following list gives the name of each file in the module, along with a brief description of the file.

Circuit	A LEX file containing the software version of the circuit analysis module. The VER$ command reads this information.
KEYWAIT	A LEX file containing KEYWAIT$. KEYWAIT$ waits in a low power state until a key is pressed and then returns the key name. This is similar to KEY$.
CNAP	This is the main program. It calls the subroutine CNAP71 (which is actually a part of CNAP) to preserve the global environment of the HP-71.*
CNAPOUT	This file contains a subroutine named OUT, which is called by CNAP. This routine formats all printed or displayed results.
CNAPHEAD	This file contains the subroutine HEAD to generate the headers of the printed or displayed output.

Variables

The circuit analysis module uses the following variables.

* CNAP can be run without a file name conflict by entering RUN CNAP:PORT (*x*), where *x* is the number of the port that the circuit analysis module is plugged into.

Single Variables, Integer Precision

B: Branch number.
F: From node to port 1.
F1: From node to port 2.
I: Index—general use.
J: Index—general use.
K: Index—general use.
L: Index—used in Crout Reduction.
N: Number of nodes.
N1: Output node.
Q0: Flag—set for grounded from or to port 1 node.
Q1: Flag—set for port 1 node connected to node 1.
Q2: Flag—set for log sweep.
Q3: Flag—set for grounded from or to port 2 node.
Q4: Flag—set for port 2 node connected to node 1.
Q7: Flag—set for group delay.
Z: Port 1 node # not grounded or connected to node 1 when other node is so connected.
Z1: Port 2 node # not grounded or connected to node 1 when other node is so connected.

Arrays—Integer Precision

C(): Port 1 from and to nodes—coded: FFTT.
K(): Element kind and port 2 from and to nodes—coded KFFTT.

Arrays—Short Precision

E() : R, L, C, g_m, or Z_o for each branch as applicable.
E1(): Quarter-wave frequency for transmission lines and stubs.

Single Variables—Real Precision

A: Angle of transmission function.
F0: Frequency or log frequency.
F3: Current frequency.
F7: Start frequency.
F8: Stop frequency.
F9: Frequency increment or number of points per decade.
G: Conductance.
G8: Flag—set for printer output.
M: Transmission function magnitude in dB.
W0: Current radian frequency—`W0 = 2 * PI * F3`.
Y: Transmission line Y_{11} or Y_{22}.

Array Variables—Real Precision

B(,): Susceptance augmented array.
B1(,): Susceptance auxillary array.
G(,): Cunductance augmented array.
G1(,): Conductance auxillary array.
V(): Real voltage vector.
V1(): Imaginary voltage vector.

String Variables

A$: Answer to questions.
F$: File name.
H1$: General use string variable.
H2$: Output headings.
H3$: General use string variable.
I$: General use string variable.
I1$: Images used with PRINT, USING statements.
I2$: General use string variable.

Appendix D

CNAP Program Structure and Description

The Matrix Equations

CNAP uses nodal analysis to obtain the matrix equation set describing a network containing N independent nodes:

$$\mathbf{Y} \times \mathbf{E} = \mathbf{I}$$

Where $\mathbf{Y}$ is the N by N nodal admittance matrix, $\mathbf{E}$ is the node voltage vector, and $\mathbf{I}$ is the source current vector. Each element of the nodal admittance matrix and source current vector may be a frequency-dependent complex quantity. At each analysis frequency these quantities must be calculated. Then the nodal admittance matrix is inverted and multiplied by the source current vector to obtain the node voltage vector:

$$\mathbf{E} = \mathbf{Y}^{-1} \times \mathbf{I}$$

The Crout method, described in appendix B, is used to simultaneously invert $\mathbf{Y}$ and multiply by $\mathbf{I}$ by combining them into a single matrix, called the *augmented matrix*, which has dimensions N by $N + 1$. Since the elements of both $\mathbf{Y}$ and $\mathbf{I}$ (and likewise the augmented matrix) can be complex numbers, and since HP-71 BASIC only performs arithmetic operations on real numbers, the real and imaginary parts of the augmented matrix are generated and treated separately as real arrays. The matrix **G** (and auxillary matrix **G1**) contains the real part of the augmented matrix, while the matrix **B** (and auxillary matrix **B1**) contains the imaginary part. Likewise, the array **V** contains the real part of the voltage vector, while **V1** contains the imaginary part.

Node and Branch Information Storage

Two integer arrays, C( ) and K( ), are used to store branch interconnection information; two short arrays, E( ) and E1( ), are used to store branch value information. The branch number is the array index. There are two types of branches: *one-port* (resistors, capacitors, inductors, open and shorted transmission line stubs) and *two-port* (VCCS's and transmission lines). The C( ) array contains the node numbers connected to port 1 coded in the form FFTT (where FF is the "from" node and TT is the "to" node specified during the circuit input phase). For example, if branch 5 is a resistor connected from node 6 to node 10, then C(5) = 0610. The K( ) array contains the element type and the nodes connected to port 2 of a two-port (if it exists). This information is coded KFFTT, where K is the element type as shown in Table 1 and FF and TT are the from and to nodes for port 2. For branches containing one-port elements, FFTT = 0000 in the K( ) array.

Table 1. Element Type Coding For K Array

Element Type	K
resistor	1
capacitor	2
inductor	3
voltage-controlled current source	4
transmission line	5
shorted stub	6
open stub	7

Array E( ) contains the port 1 element values, while E1( ) is the quarter-wave transmission line resonant frequency (when appropriate). For each of the seven element types, the contents of these arrays are shown in table 2:

Table 2. Branch Element Value Storage

Element	E( )	E1( )
1	resistance	0
2	capacitance	0
3	inductance	0
4	g_m	0
5	Z_0	¼ wave frequency
6	Z_0	¼ wave frequency
7	Z_0	¼ wave frequency

The program uses the information stored in these four arrays (C, K, E, E1) to construct the real and imaginary parts of the augmented nodal admittance matrix. The construction details are covered next.

Nodal Matrix Element Storage

If memory space for matrix element storage were abundant, then the real and imaginary nodal admittance matrices and source current vectors could be generated considering the ground node (node 0) as a dependent node. All branches would be treated alike. Each branch would sum into two elements on the main diagonal, and subtract from two elements off the main diagonal of either the real or imaginary matrices, as is shown on page 88. After completing this construction, the row and column containing the ground node would be discarded, and the resulting reduced matrix inverted and multiplied by the source current vector to obtain the node voltages as described earlier on page 86.*

The construction of the real and imaginary parts of the nodal admittance matrix and source current vector proceed in a manner that minimizes memory requirements for storing matrix element values. No equations are written for the ground node. This means that branches connected to either the input node (node 1) or ground (node 0) must be treated differently, as they only sum into main diagonal elements of the admittance matrices and to the source current vector (for branches connected to node 1). The rest of the branches in the network sum into two main-diagonal elements and subtract from two off-diagonal elements of the nodal admittance matrices. The construction of the augmented nodal admittance matrices is described symbolically next (and by example on page 89).

Matrix Construction

The number of indices for the matrix elements is one less than the associated node number. This convention occurs because neither node 0 nor 1 are dependent nodes. Node 2 is the lowest numbered dependent node. Arrays in the HP-71 must start with either 0 or 1 as specified through the OPTION BASE command (OPTION BASE 1 is used). Thus, branches connected to node 2 generate admittance terms in the g_{11} and b_{11} elements of the real and imaginary arrays. In general, a branch connected to the jth and kth nodes will affect the matrix elements in the $j-1$ and $k-1$ rows and columns as described next.

* The details of the method can be found in Balabanian and Bickert, *Electrical Network Theory*, J. Wiley, 1969.

Real Matrix

Since the real part of the augmented nodal admittance matrix derives only from resistors and VCCS transconductances, the branches are scanned from lowest to highest for element types 1 or 4 to construct this real matrix. Since resistors and transconductances are frequency independent, the real matrix is only constructed once and saved. Let $g = 1/R$ (a conductance). The matrix construction steps are:

1. If j and k are neither 0 nor -1 (the other end of the branch does not connect to either the input node or ground):
   - Add g to the main diagonal elements:
   $$g_{jj} = g_{jj} + g$$
   $$g_{kk} = g_{kk} + g$$
   - Subtract g from the off-diagonal elements:
   $$g_{jk} = g_{jk} - g$$
   $$g_{kj} = g_{kj} - g$$
2. If $j = -1$ and $k > 0$ (or if $k = -1$ and $j > 0$) then the branch is connected to ground:
   - Add g to only one main diagonal element:
   $$g_{kk} = g_{kk} + g$$
   $$(\text{or } g_{jj} = g_{jj} + g)$$
3. If $j = 0$ and $k > 0$ (or $k = 0$ and $j > 0$) then the branch is connected to the input voltage source node (node 1). The input voltage source and branch conductance are transformed into a Norton equivalent source, i.e., a current generator shunted by a conductance. If the input voltage is V, then the value of the current generator in the Norton source is $g_{kn} \times V$ (or $g_{jn} \times V$). Since the input voltage source is assumed to be 1 V_{rms}, the input branch conductance alone appears:
   - Accommodate the Norton equivalent source contribution to the current source vector (contained in the augmented portion of the nodal matrix):
   $$g_{kn} = g_{kn} + g$$
   $$(\text{or } g_{jn} = g_{jn} + g)$$
   - Add the branch admittance to the main diagonal as in step 2 above:
   $$g_{kk} = g_{kk} + g$$
   $$(\text{or } g_{jj} = g_{jj} + g)$$

Real Matrix Generated From VCCSs

A VCCS is a two-port device (g_m is the VCCS transconductance) and is illustrated in figure D-1. Port 1 is the input, or control port, that has infinite input impedance and samples the applied voltage. Port 2 is the output port and is connected to an ideal current source. This particular current source has an output current that is proportional to the voltage applied to port 1. The constant of proportionality is g_m, the transconductance.

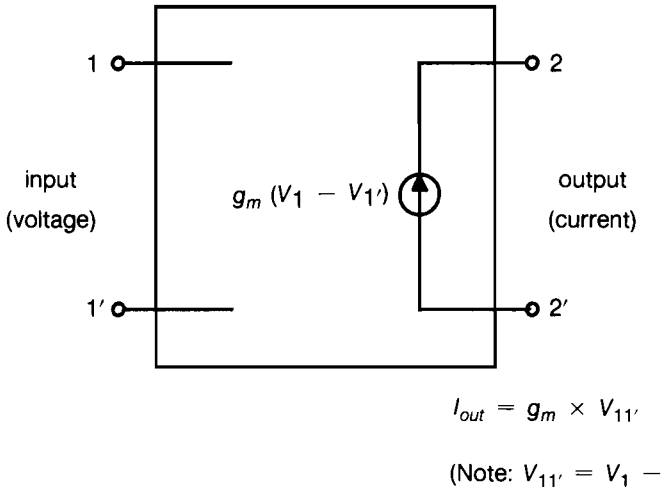

Figure D-1. Voltage Controlled Current Source (VCCS)

Because of the suppression of the ground node from the nodal matrices, the inclusion of the effect of a VCCS becomes somewhat complicated. A simplified example is shown next to guide you through some of the reasoning. A simple three-node network containing a VCCS is used (refer to figure D-2). The nodal equations are written using the procedure just presented. The current source vector contains the sum of the dependent and independent currents into each node. The dependent currents (dependent upon node voltages) are brought to the left-hand side of the equation. The matrix for the network is in figure D-3. Notice how the transconductance is added/subtracted to/from those matrix elements lying in rows determined by the VCCS output nodes, and in columns determined by the VCCS input nodes.

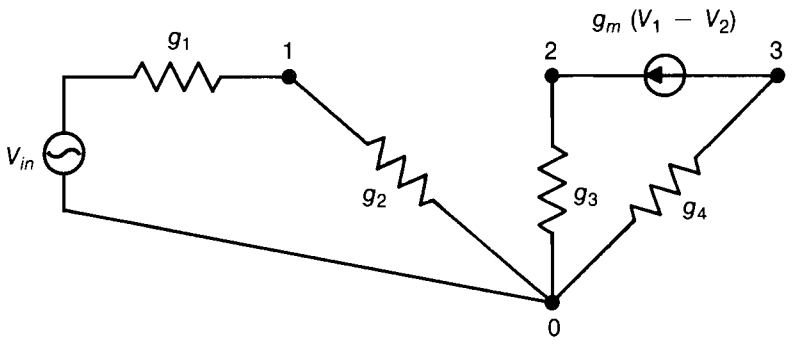

Figure D-2. Three-Node Network Containing a VCCS

$$\begin{bmatrix} g_1 + g_2 & 0 & 0 \\ 0 & g_3 & 0 \\ 0 & 0 & g_4 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} g_1\ V_{in} \\ g_m\ (V_1 - V_2) \\ -g_m\ (V_1 - V_2) \end{bmatrix}$$

$$\underbrace{\begin{bmatrix} g_1 + g_2 & 0 & 0 \\ -g_m & g_3 + g_m & 0 \\ g_m & -g_m & g_4 \end{bmatrix}}_{\text{column indices from + and − VCCS control nodes}} \cdot \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \left.\begin{bmatrix} g_1 V_{in} \\ 0 \\ 0 \end{bmatrix}\right\} \text{row indices from "to" and "from" VCCS output nodes}$$

Figure D-3. Nodal Matrix and Reduction of the Three-Node Network in Figure D-2

$$\begin{bmatrix} g_1 + g_2 & 0 & 0 & g_1 V_{in} \\ -g_m & g_3 + g_m & 0 & 0 \\ g_m & -g_m & g_4 & 0 \end{bmatrix}$$

Figure D-3a. Augmented Matrix

The augmented matrix is the matrix resulting from the nodal matrix and the source current vector. This form is ready for Crout reduction.

Imaginary Matrix

An imaginary matrix is generated from inductors, capacitors, and transmission line segments. Omega (ω) is the radian frequency at the current analysis frequency ($\omega = 2\pi f$). Depending upon the element type, the susceptance to be added to the current augmented imaginary matrix elements is shown in table 3.

Table 3. Element Susceptances

Element Type	Susceptance
capacitor, C	$\omega \times C$
inductor, L	$-1/\omega/L$
shorted stub	$-y_0 \times \cot(90 \times f \div f')$
open stub	$y_0 \times \tan(90 \times f \div f')$

Note: f′ is the frequency where the transmission line is quarter-wave resonant, and y_0 is the characteristic admittance ($y_0 = 1/Z_0$).

The susceptance of a component in the above table is added to or subtracted from the imaginary augmented elements using the same rules as outlined in the real matrix steps 1, 2, and 3—except the conductance "*g*" is replaced by the susceptance "*b*." Since the elements of the real matrix are frequency-independent conductances and transconductances, the real matrix is only constructed once, and saved. The elements of the imaginary matrix are frequency dependent and the imaginary matrix must be recreated at each new analysis frequency.

Lossless Transmission Lines

Transmission lines are modeled as two-port networks using the ITT handbook model (shown later in figure D-5).

The two-port y parameters can be defined in terms of a transmission line segment as shown in figure D-4.

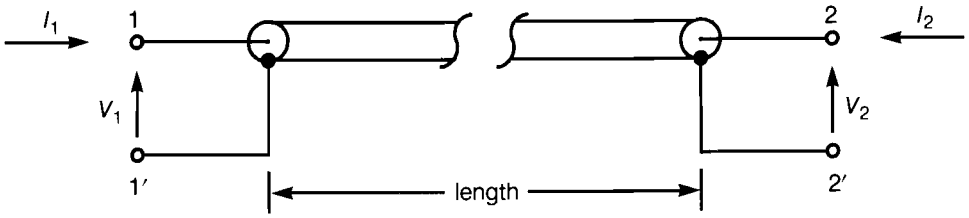

Figure D-4. Transmission Line Nomenclature

where $$\mathbf{I} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \text{ and } \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

then $$\mathbf{Y} \times \mathbf{E} = \mathbf{I}$$

where Y is the admittance matrix:

$$\mathbf{Y} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = y_0 \times \begin{bmatrix} -j \times \cot(\beta l) & j \times \csc(\beta l) \\ j \times \csc(\beta l) & -j \times \cot(\beta l) \end{bmatrix}$$

with:

$y_0 = 1/Z_0$ = characteristic admittance

β = phase constant = $\dfrac{2\pi}{\lambda}$

Note that

$$\beta l = \frac{2\pi l}{\lambda} = \frac{2\pi}{\frac{\lambda}{l}} \text{ (in radians)}$$

or

$$\beta l = \frac{360}{\frac{\lambda}{l}} \text{ (in degrees)}$$

and that

$$\lambda = \frac{v}{f}$$

where v is the phase velocity (propagation velocity) in the transmission line (typically 0.6c).

There exists a frequency, f', where l is a quarter-wave:

$$l = \frac{\lambda}{4} = \frac{v}{4f'}$$

Hence:

$$\beta l = \frac{360f}{4f'} = 90\,\frac{f}{f'} \text{ (degrees)}$$

By specifying the frequency where the transmission line is quarter-wave resonant, the need for determining and specifying the phase velocity, v, is eliminated.

A two-port network having a **Y**-matrix representation, as above, may also be modeled as two port admittances, and two dependent current sources as shown in figure D-6. This admittance and dependent current model is used to accommodate transmission lines within CNAP.

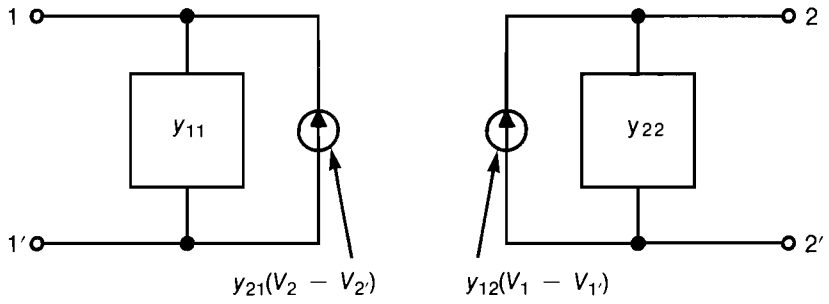

Figure D-5. Two-Port Representation of Transmission Line Using Dependent Current Sources

The tools already exist for adding the elements of this model to the augmented nodal admittance matrix as explained in the matrix construction part of this section. The only difference is that the values of both the shunt port admittance, y, and the dependent current source, g_m, are functions of βl, a function of frequency. Hence, at each analysis frequency, these values must be calculated and added to the augmented nodal admittancy matrix. Again, since the ground node has been suppressed from the equation set, those elements connecting to either the input (node 1) or ground (node 0) must be treated differently as in the real matrix construction (refer to page 88).

Appendix E

Optional Printer Routine

The following program is an optional routine for formatting output on a 24-character printer such as the HP 82162A Thermal Printer. The program provides one numerical result per line as shown in the sample printout.

Key in the program as it appears below. Then, when CNAP is run it will call this program in user memory instead of using its own subroutine.

```
10 SUB HEAD(Q7,G8)
20 PRINT "CIRCUIT OUTPUT"
30 PRINT
40 END SUB
50 SUB OUT(N,N1,Q2,Q7,F3,F4,V(),V1(),U(),U1(),G8)
60 S=V(N1-1) @ T=V1(N1-1) @ M=10*LOG10(S*S+T*T) @ A=ANGLE(S,T)
 @ IF NOT Q7 THEN GOTO 100
70 S=U(N1-1) @ T=U1(N1-1)
80 M1=10*LOG10(S*S+T*T) @ A1=ANGLE(S,T) @ IF ABS(A1-A)>180 AND
 A<0 THEN A=A+360
90 TO=RAD(ABS(A1-A))/F4/PI/4 @ A=(A+A1)/2 @ M=(M+M1)/2
100 IF NOT G8 THEN 190
110 IF F3>1000000 OR F3<1 THEN ENG 6 ELSE FIX 2
120 PRINT "FREQ.= ";F3;"HZ."
130 IF ABS(M)<1 AND M#0 THEN ENG 3 ELSE FIX 2
140 PRINT "MAGN.= ";M;"dB"
150 FIX 2 @ PRINT "PHASE= ";A;"DEG."
160 IF Q7 THEN ENG 3 @ PRINT "DELAY= ";TO;"SEC."
170 PRINT @ STD @ GOTO 220
180 IF M1=0 THEN F=0 @ RETURN
190 FIX 2 @ DISP "F="&STR$(F3)&",";
200 IF Q7 THEN ENG 3 @ DISP "DELAY="&STR$(TO)&",";
210 DELAY INF @ FIX 2 @ DISP "dB="&STR$(M)&",PHASE="&STR$(A) @
 STD
220 END SUB
```

Printed results would look like this:

```
CIRCUIT OUTPUT


FREQ.=   1000.00 HZ.
MAGN.= -128.14 dB
PHASE=   172.84 DEG.
DELAY=   19.69E-6 SEC.

FREQ.=   10000.00 HZ.
MAGN.= -92.19 dB
PHASE=   128.51 DEG.
DELAY=   7.755E-6 SEC.

FREQ.=   100000.00 HZ.
MAGN.= -70.08 dB
PHASE=   94.53 DEG.
DELAY=   126.4E-9 SEC.
```

Subject Index

Page numbers in **bold** type indicate primary references; page numbers in standard type indicate secondary references.

U-V-W

HP 82481A Circuit Analysis Pac
Owner's Documentation
Addendum

When you do not have an HP-IL module plugged into your HP-71B, and you attempt to print the current circuit (using the `Pr` routine in the main menu), the program stops and displays the following error message:

```
ERR L37:XWORD Not Found
```

The program is suspended. To proceed, type:

```
CONT 38 [END LINE]
```

The program continues and displays the circuit elements (instead of attempting to print them).

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