HP 9000 Computer Systems

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Series 800 Hardware Technical Data

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HP Precision Architecture

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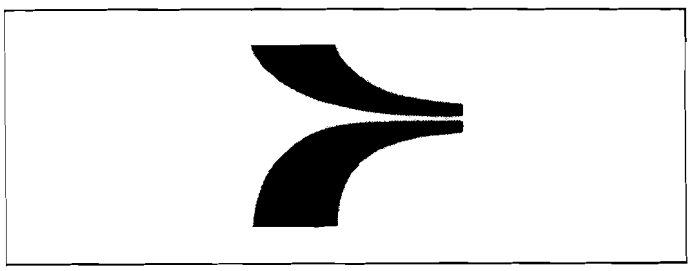
HP Precision Architecture is a reduced complexity architecture which provides the framework for Hewlett-Packard computer systems for the 1990's and beyond. Precision Architecture is an embodiment and extension of Reduced Instruction Set Computer (RISC) architectural principles. Processor hardware is optimized for the simple, often executed functions, leaving implementation of more complex functions to software. Instructions are executed directly in hardware in a single, fast CPU cycle, without the overhead and complexity of a microcoded control store. Support of a simple instruction set allows previous HP architectures to be emulated very effectively, providing full software compatibility and thus a convenient growth path to Precision Architecture systems. Full 48-bit virtual addresses are supported, representing a significant expansion over the addressability of typical 32-bit systems. A key design objective was scalability, such that cost-effective solutions can be provided from desktop systems all the way through systems with the power of today's mainframes. Provisions have been made for multiprocessors and special function coprocessors, as well as redundant, high availability features. Coupled with support for high-speed floating point calculations, HP Precision Architecture is ideally suited to providing cost-effective, high performance commercial and technical computing solutions.

Features

- Reduced instruction set
- 32-bit instructions, fixed format
- 48-bit virtual addressing
- Hardwired, single-cycle instruction execution
- Register intensive operation
- 32 general purpose registers
- 32 control registers
- 8 Space Registers
- Only LOADs and STOREs access memory
- Hardware support for floating point and decimal calculations
- Demand-Paged memory management scheme
- Multiprocessors and special function coprocessors
- Memory-Mapped I/O



RISC Motivations

Many computer architectures which have evolved over the last twenty years have tended towards increasing system complexity. System architectures which provide large, complex instruction sets are loosely called CISCs (Complex Instruction Set Computers). CISCs typically utilize a microcoded control store to provide instruction set support for high level languages and complex functions, such that instructions require multiple CPU cycles to execute.

Extensive research in industry and at leading universities has shown, however, that CISCs spend the great majority of the time executing simple instructions such as ADD, LOAD, STORE, and BRANCH. The more complex instructions, which necessitate a greater level of processor complexity, are utilized relatively infrequently. The net result with architectures that support large, complex instruction sets is that a performance penalty is often encountered even for the simple, often-executed instructions, due to the overhead of additional instruction decoding and control hardware. This overhead can increase CPU cycle time, and can negate any advantage of providing an instruction set which directly supports more complex functions.

These findings led to the concept of reduced complexity RISC architectures. The key RISC concept is to optimize the system to execute simple, often-used instructions directly in hardware in a single, fast CPU cycle. Extensions of RISC concepts have been embodied in HP Precision Architecture to provide a flexible, expandable architecture which maximizes performance realized from a given semiconductor technology, and achieves a given level of performance at a significantly lower cost than other systems.

Instruction Set

HP Precision Architecture defines 140 instructions. Each is 32-bits long and has a fixed format. The instruction set directly implements only simple functions in order to minimize processor complexity.

Memory Reference Instructions

Data in memory is referenced only via Load and Store instructions. Operands required for a given operation must first be brought into a CPU register with a Load instruction, and the result of the calculation must be explicitly moved to memory via a Store instruction. Accessing memory with only Load/Store instructions, coupled with support for a relatively large number of CPU registers, allows for frequently required operands to be held in the CPU. A performance increase can thus be realized, as the number of accesses to cache and main memory are minimized.

Arithmetic and Logical Instructions

The arithmetic and logical functions provided by the instruction set are limited to relatively simple functions, with appropriate primitives provided for common operations. For example, Shift-and-Add instructions accelerate integer multiplication, and Extract/Deposit instructions efficiently support bit-manipulation functions utilized by high-level languages. More complicated functions are implemented by executing a sequence of simple instructions.

Decimal Arithmetic Support

Primitives such as the *Decimal Correct* and *Unit Add Complement* instructions allow for packed and unpacked decimal addition to be performed with the binary *Add* instruction. Packed, unpacked, and zoned decimal operations can easily be supported by compilers.

Floating Point Instructions

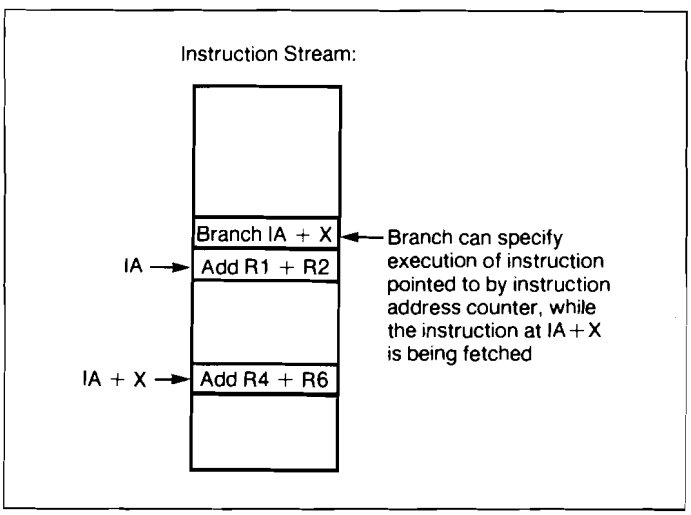
Floating point instructions are available to support single-precision (32-bit), double-precision (64-bit) and quadruple-precision (128-bit) arithmetic operations. Floating point instructions can either be executed directly in hardware by a coprocessor, or can be emulated in software. With a floating point coprocessor, floating point calculations can be performed while the CPU continues to execute in parallel.

Branch Instructions

Conditional branch instructions perform an operation, evaluate a branch condition, and perform the branch (if appropriate) in a single instruction. The need for some branch sequences is eliminated altogether as most computational instructions can specify conditional execution of the next instruction, allowing such common functions as boolean value generation to be performed in a simple, non-branching instruction sequence.

Single-Cycle Instruction Execution

Instructions are executed directly in hardware, and typically will execute in only one CPU cycle. Branch instructions and Load/Store instructions may require more than one cycle to execute, but are implemented and scheduled such that effective execution rates approaching one cycle per instruction are achieved. A delayed branch capability allows branch instructions to specify that the next sequential instruction be executed, and compilers schedule instructions to utilize this capability when possible. Thus the "dead" cycle typically encountered for taken branches on other systems can often be avoided. Similarly, Load instructions can be scheduled such that useful processing of other instructions is done while the data is being fetched. To avoid pipeline delays, instructions which require the data being loaded are not scheduled for execution, if possible, until the data is available in a CPU register.



Delayed-Branch Capability

Data Types

Integers

HP Precision Architecture supports 16-bit and 32-bit integers, either signed or unsigned. Signed integers are in 2's complement form. To help minimize processor complexity, halfword (16-bit) integers must be aligned at even byte addresses, and 32-bit integers must be aligned on a word boundary.

Characters

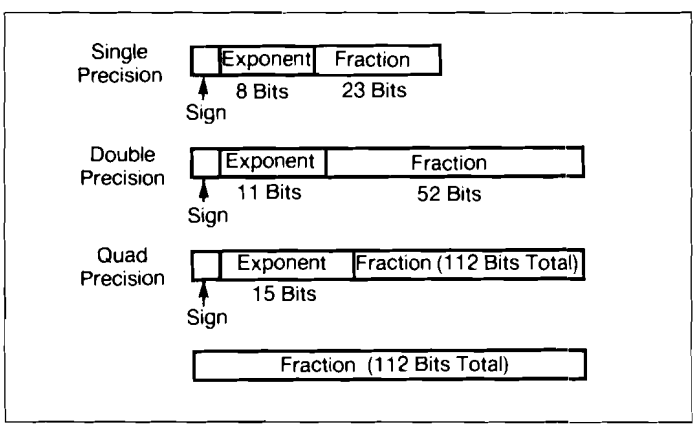
Characters are stored as 8-bit quantities, conforming to the ASCII standard for values 0 through 127, and HP's 8-bit extended Roman-8 character set for values 128 through 255.

Decimal Data

Both packed and unpacked decimal data representations are supported. Packed decimal data is always aligned on a word boundary, and consists of 7, 15, 23, or 31 Binary Coded Decimal digits.

Floating Point Operands

Single, Double, and Quadruple-word floating point operands are represented in accordance with the ANSI/IEEE 754-1985 standard. Single-precision floating point numbers must be aligned on word boundaries, and Double and Quadruple-precision numbers must be aligned on double-word boundaries.



Floating Point Operand Format

CPU Register Set

HP Precision Architecture specifies register-intensive operation. Calculations are performed only between high-speed CPU registers, or between a CPU register and a constant held in the instruction. Register-intensive operation allows for simplified data and control paths and increased processor performance. Optimizing compilers allocate the most frequently used variables to General Purpose Registers to minimize the number of memory references.

General Purpose Registers

There are 32 available General Purpose Registers for holding operands and results of processor computations. All General Purpose Registers are 32-bits wide.

Control and Status Registers

There are 32 control and status registers in the CPU, which are used for interrupt processing, virtual memory access protection, and other system functions. CPU status is maintained in the 32-bit Processor Status Word (PSW), which reflects the state of key CPU flags and status bits.

Space Registers

Eight Space Registers in the processor are used to specify up to eight possibly different 4GB virtual spaces that can be utilized for a given operation. These registers can hold 16-bit or 32-bit space identifiers, with the space identifier length chosen dependent upon the amount of addressability appropriate for a given system. Five of these registers can be used directly by application programs.

Instruction Address Registers

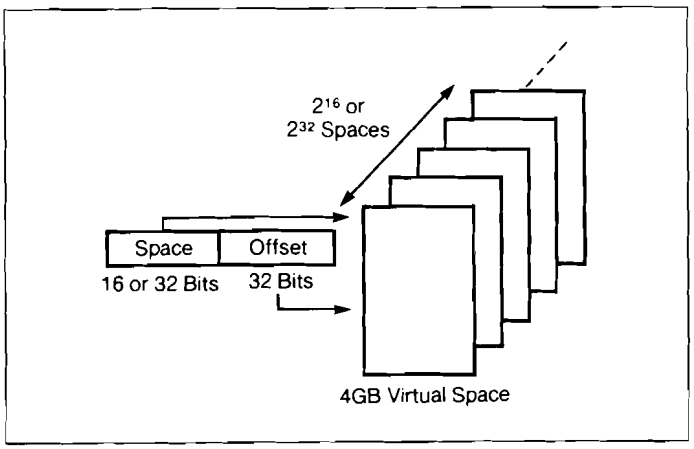
Two CPU registers are used to point to the next instruction to be executed. The Instruction Address Space Register (IA Space) points to the 4GB space which holds the next instruction. The Instruction Address Offset Register (IA Offset) points to the location, within that space, which holds the instruction. Each of these registers is, in fact, a two-element queue, reflecting architectural visibility of the next two instructions being processed in the pipeline.

Virtual Addressing

HP Precision Architecture provides for support of 48-bit virtual addresses, representing a significant expansion over the virtual addressability of typical 32-bit systems. The instruction set additionally provides direct access to physical memory locations, and low-cost systems will have the option of providing only physical addressing if appropriate. The smallest addressable quantity is a byte.

Virtual Memory Management

Virtual Memory is organized as a set of linear spaces, with each space 4GB in length. Spaces are further divided into fixed length 2KB pages, each of which can hold either code, data or both. Space Registers point to the virtual space to be accessed, and the specific location within that space is specified by a 32-bit quantity called the *byte offset*. Multiple simultaneous spaces are supported. Code can span spaces, and a single data structure can be up to a full 4GB space in length.



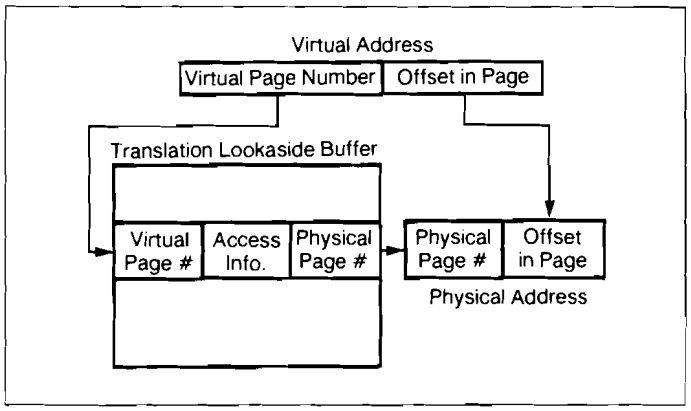
Virtual Memory Organization

Memory Mapped I/O

HP Precision Architecture incorporates a memory-mapped I/O scheme, whereby I/O operations are initiated and controlled via a series of Load/Store instructions to reserved virtual or real space locations. This allows I/O devices to efficiently utilize the same access protection mechanisms as code and data. No I/O-specific instructions are required for performing I/O. Coupled with other I/O subsystem features such as DMA Chaining, which allows multiple transactions to be processed without CPU intervention, I/O operations on Precision Architecture systems carry less overhead and are streamlined for increased I/O performance.

Virtual Address Translation

Virtual Addresses are translated to physical addresses using Translation Lookaside Buffer (TLB) hardware in the processor. TLBs contain translations for recently accessed virtual pages. They can be organized as two logical TLBs, one for code and one for data, or can be combined into a single TLB.



Virtual Address Translation

Virtual Memory Access Protection

The TLB hardware supports protection mechanisms to assure that the currently executing process can perform only the code, data, or I/O accesses for which it is authorized. Included in the access checking mechanisms are four privilege levels. Protection parameters are associated with each page, and these parameters define what privilege level is required to access that page, as well as what types of accesses are permitted. For each requested access, these privilege parameters are checked against the privilege level of the currently executing process, to ensure that the process has sufficient authorization to perform that access.

Caches

Processor caches may be organized as a single, unified cache, holding both instructions and data, or there may be separate instruction and data caches. So that the machine cycle time can be minimized, the I/O subsystems do not interface to the cache, and it is the responsibility of software to update main memory contents with any modified cache contents before launching a DMA I/O operation. Instruction caches are read only, as code is typically non-modifiable.

Coprocessors

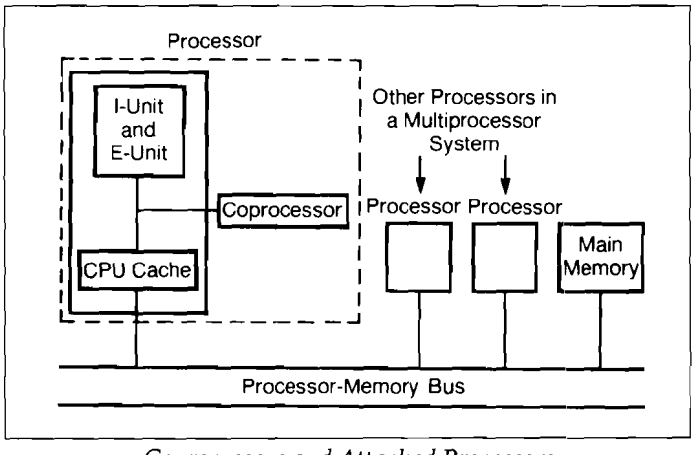
HP Precision Architecture has provisions for integration of coprocessors which share the main processor caches. Coprocessors are controlled by a subset of the instruction set, and are typically utilized to enhance performance of special functions, for example, high performance floating point calculations. Coprocessors contain their own register set which may directly interface with the cache.

Attached Processors

Provisions are made for attached processors, which interface to the system hierarchy at the memory bus level, and typically have their own register set and local cache(s). Attached processors can provide such functions as I/O processing or vector processing. They may execute either the same instruction set, or a different instruction set, as the main processor.

Multiprocessors

Multiprocessors are identical, attached processors. They can be configured either in parallel, to increase performance via distribution of the system workload, or can be configured redundantly to provide fault tolerance. Each processor has its own register set and local cache storage, and executes the entire instruction set. Provisions are made for development of tightly-coupled, symmetric multiprocessor systems.



Coprocessors and Attached Processors

Optimizing Compilers

Reduced complexity architectures are ideal for optimizing compilers, and compiler optimization is required for the highest performance on such machines. The optimizing compilers utilized with HP Precision Architecture systems maximize processor efficiency in a number of ways. For example, scheduling instructions to make the most efficient use of the available cycle after a taken Branch. By allocating the most frequently accessed operands in an instruction stream to CPU general purpose registers, the number of references to cache and main memory is minimized. Compilers used with Precision Architecture systems also provide features to correct some inefficient high-level language programming practices. For example, computations within a loop that produce the same result for each iteration can be moved outside of the object code loop, and other duplicate computations in a program can be eliminated during object code generation.

VLSI

Precision Architecture allows for systems to be implemented in a wide variety of semiconductor technologies. With a reduced amount of circuitry required to implement processor functions, maximum benefits can be realized from Very Large Scale Integrated (VLSI) components. Processor performance can be maximized by placing an entire CPU on-chip, thus keeping signal delays short and allowing CPU cycle time to be decreased. With further integration, such as placing CPU, caches, and TLBs on-chip, code and data access times can also be minimized, providing for additional performance gains. The performance advantages and low cost of VLSI implementations allow cost effective high performance systems, as well as powerful, low-cost office systems and workstation products.

Instruction Set Listing

Memory Reference Instructions

Load Word
Load Halfword
Load Byte
Load Word Indexed
Load Halfword Indexed
Load Byte Indexed
Load Word Short
Load Halfword Short
Load Byte Short
Load Word and Modify
Load Word Absolute
Load Word Absolute Short
Load Offset
Load and Clear Word Indexed
Load and Clear Word Short
Store Word
Store Halfword
Store Byte
Store Word Short
Store Halfword Short
Store Byte Short
Store Word and Modify
Store Word Absolute Short
Store Bytes Short

Unconditional Branches

Branch and Link
Gateway
Branch and Link Register
Branch Vectored
Branch External
Branch and Link External

Conditional Branches

Move and Branch
Move Immediate and Branch
Compare and Branch if True
Compare and Branch if False
Compare Immediate and Branch if True
Compare Immediate and Branch if False
Add and Branch if True
Add and Branch if False
Add Immediate and Branch if True
Add Immediate and Branch if False
Branch on Variable Bit
Branch on Bit

Arithmetic/Logical Instructions

Add
Add Immediate
Add Immediate Left
Load Immediate Left
Add Logical
Add and Trap on Overflow
Shift One and Add
Shift Two and Add
Shift Three and Add
Shift One and Add Logical
Shift Three and Add Logical
Shift One, Add, and Trap on Overflow
Shift Two, Add, and Trap on Overflow
Shift Three, Add, and Trap on Overflow
Add with Carry
Add with Carry and Trap on Overflow
Subtract
Subtract from Immediate
Subtract and Trap on Overflow
Subtract Immediate and Trap on Overflow
Subtract with Borrow
Subtract with Borrow and Trap on Overflow
Subtract and Trap on Condition
Subtract and Trap on Condition or Overflow
Divide Step
Compare and Clear
Inclusive OR
Exclusive OR
AND
AND Complement
Unit XOR
Unit Add Complement
Unit Add Complement and Trap on Condition
Decimal Correct
Intermediate Decimal Correct
Add Immediate and Trap on Overflow
Add Immediate and Trap on Condition
Add Immediate, Trap on Condition or Overflow
Compare Immediate and Clear
Variable Shift Double
Shift Double
Variable Extract Signed
Variable Extract Unsigned
Extract Signed
Extract Unsigned
Variable Deposit
Variable Deposit Immediate
Deposit
Deposit Immediate
Zero and Variable Deposit
Zero and Variable Deposit Immediate
Zero and Deposit
Zero and Deposit Immediate

System Control Instructions

Break
Return From Interrupt
Set System Mask
Reset System Mask
Load Space ID
Move to Space Register
Move to Control Register
Move from Space Register
Move from Control Register
Move to System Mask
Synchronize Caches
Probe Read Access
Probe Read Access Immediate
Probe Write Access
Probe Write Access Immediate
Load Physical Address
Load Hash Address
Purge Instruction TLB
Purge Instruction TLB Entry
Purge Data TLB
Purge Data TLB Entry
Insert Data TLB Address
Insert Data TLB Protection
Insert Instruction TLB Address
Insert Instruction TLB Protection
Purge Data Cache
Flush Data Cache
Flush Instruction Cache
Flush Data Cache Entry
Flush Instruction Cache Entry
Diagnose

Special Function Unit Operations

Special Operation Zero
Special Operation One
Special Operation Two
Special Operation Three

Coprocessor Loads and Stores

Coprocessor Load Word Short
Coprocessor Load Word Indexed
Coprocessor Load Doubleword Short
Coprocessor Load Doubleword Indexed
Coprocessor Store Word
Coprocessor Store Indexed
Coprocessor Store Doubleword
Coprocessor Store Doubleword Indexed
Coprocessor Operation*

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* *Floating Point Operations Included*

Model 840 Computer System

HEWLETT PACKARD

HP 9000 Series 800 Computer Systems

The Model 840 is the first HP 9000 to use HP Precision Architecture. Running under the HP-UX operating system, the Model 840 doubles CPU performance available with HP 9000 Model 550 or HP 1000 A900 systems. Significant enhancements have been added to HP-UX to equip it for real-time applications. These HP-UX enhancements make the HP 9000 Model 840 a logical, high capacity, high performance *extension* of both the HP 9000 and the HP 1000 computer system product lines.

In Computer-Aided Design (CAD) or Computer-Aided Engineering (CAE) applications, the high performance and capacity of the Model 840 are best employed in serving the computational needs of a group of HP 9000 Series 200, 300, or 500 design or engineering workstations. In this role of workstation server, the Model 840 would run simulations or solve problems with computational workloads beyond the capability of the individual HP 9000 workstations. The Model 840 also has ample capacity to provide multi-user applications development support.

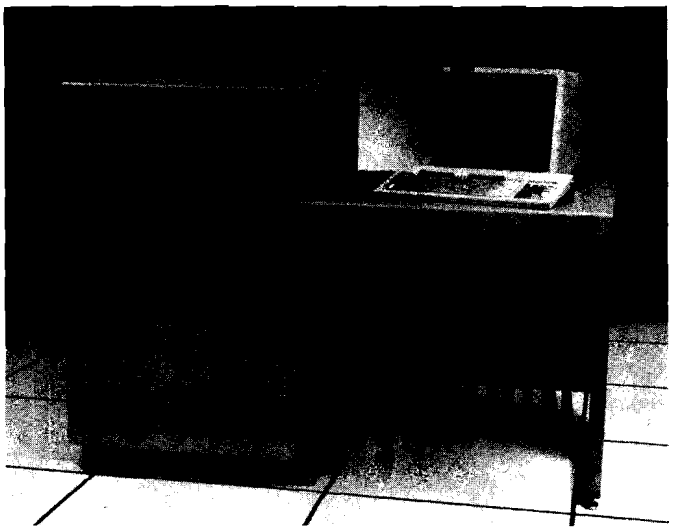
The high CPU throughput of the HP 9000 Model 840 makes it an excellent choice for compute-bound applications in the real-time and manufacturing environments. Its abilities are especially well-suited to process control, area management, and statistical quality control.

The real-time capabilities of the HP 9000 Model 840 and its HP-UX operating system, which is compatible with AT&T's System V Interface Definition (Issue 1), are valuable in telecommunications. Here, the Model 840 is well-suited for network monitoring, satellite control, and maintenance tasks.

The speed and capacity of the HP 9000 Model 840 make it a good match for scientific applications, such as those found in the defense and aerospace industries. These include mapping, tracking, communications, project management, software development, image processing, systems analysis, and research testing of equipment, weapons, and command/control/communications systems.

System Features

- HP Precision Architecture with 32-bit word size, reduced complexity, and 48-bit virtual addressing
- 4.5 MIPS CPU performance
- Floating point coprocessor for 2 million double-precision Whetstones per second performance
- 8 MB ECC memory, expandable to 24 MB
- 4096 entry Translation Lookaside Buffer for virtual-to-physical address translations



- 4 Gigabyte virtual address space per process
- Up to 60 concurrent users
- HP-UX operating system, a superset of AT&T's System V Interface Definition, with over 200 utilities from AT&T's System V.2 and other popular UNIX* versions, plus added enhancements, including real-time capability and Native Language Support (internationalization)
- Operating system compatibility with HP 9000 Series 200, 300, and 500 systems and the Integral PC
- PORT/HP-UX to assist migration of applications from RTE-A or RTE-6/VM based HP 1000 systems
- Support for:
  - C, FORTRAN 77, and Pascal programming with optimizing compilers
  - ALLBASE/HP-UX network and relational database management system with IMAGE interface
  - HPtoday for database-oriented application generation
  - Starbase graphics software based on evolving ANSI and international standards plus DGL and AGP graphics software to provide upward compatibility for existing applications
  - AdvanceNet Network Services and LAN Link software and hardware for communication with other HP 9000 systems and with HP 1000 A-Series systems
  - ARPA/Berkeley Network Services
- Remote console capability for invoking diagnostics and system reset

*UNIX is a trademark of AT&T in the U.S. and other countries.

HP Precision Architecture

The HP 9000 Model 840 utilizes the new reduced complexity HP Precision Architecture. The Model 840 embodies the basic principles of Reduced Instruction Set Computers and extends beyond them, including support for extended addressing, high performance Input/Output, and high speed floating point calculations. Other key characteristics of Precision Architecture include:

- 138 fixed-length, limited-format instructions
- Pipelined Instruction Execution
- Hardwired Control (no microcode required)
- Register Intensive Operation
- 32 General Purpose Registers
- 32 Control Registers
- 8 Space Registers for addressing
- Load/Store Instructions for Memory Access

System Organization

The processor communicates with memory and I/O via the Mid Bus (Figure 1). The Mid Bus provides a 32-bit data path, and can support sustained data transfer rates up to 20 MB/second. The Mid Bus is interfaced to a 16-bit wide Channel I/O Bus via a CIO Adapter. The Channel I/O Bus supports I/O interfaces to peripheral devices and data communications links.

The Model 840 Processor

The Model 840 processor (Figure 2) is a five-board set implemented with high-speed Schottky TTL logic. With hardwired control and a three-stage instruction pipeline, the Model 840 is capable of executing up to one instruction with every 125 nanosecond clock cycle. Separate Instruction and Execution Units facilitate pipelining and promote efficient parallel use of processor resources.

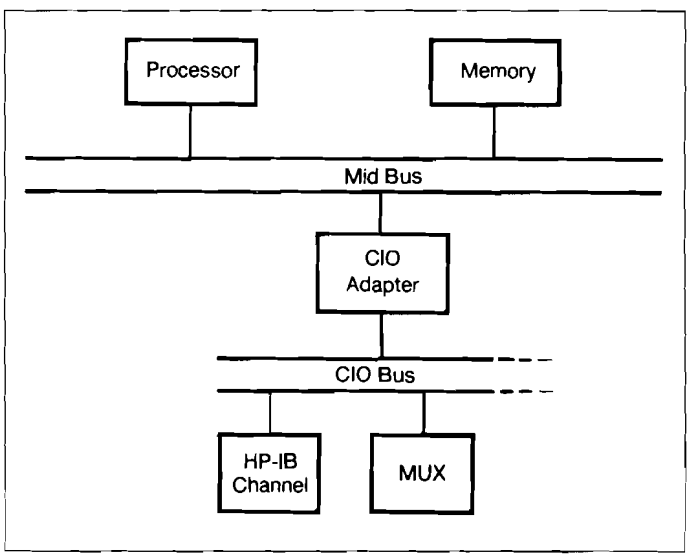


Figure 1. System Structure

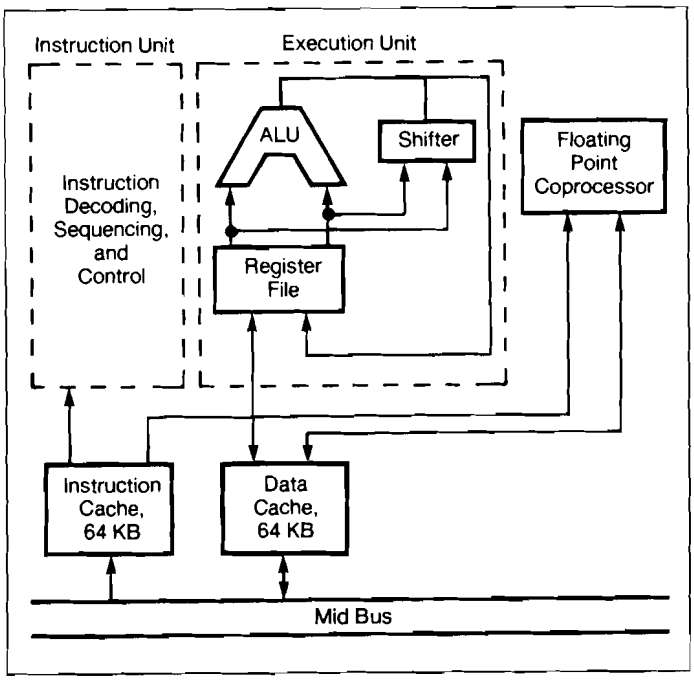


Figure 2. Central Processor Modules

Caches

A 128 kB high-speed cache memory is utilized in the Model 840. Separate 64 kB instruction and data caches promote parallel operation for maximum efficiency and optimum performance.

Both the instruction cache (I-cache) and the data cache (D-cache) are one-way associative (direct mapped), and are organized as sets of 4096 cache lines, with 16 bytes per cache line. The instruction cache is read only, as code is assumed to be non-modifiable. A write-to cache management scheme is used with the data cache. Modified data in the cache is written to main memory only when the processor requires other data to be in that cache location, or when a Direct Memory Access (DMA) operation is performed within that data area, or upon a power fail.

Instruction Pipelining

The Model 840 is pipelined at the instruction level, such that three instructions can be operated on at the same time (Figure 3). The instruction pipeline has three 125 nanosecond stages. During the first stage the instruction is fetched from the I-cache and decoded. The specified function or calculation is performed during the second stage, and in the third stage the result of the calculation is saved to a CPU general purpose register. Excepting penalties for cache misses, etc., the net effect is that one instruction completes with every 125 nanosecond CPU cycle. With all penalties, execution time averages 220 nanoseconds.

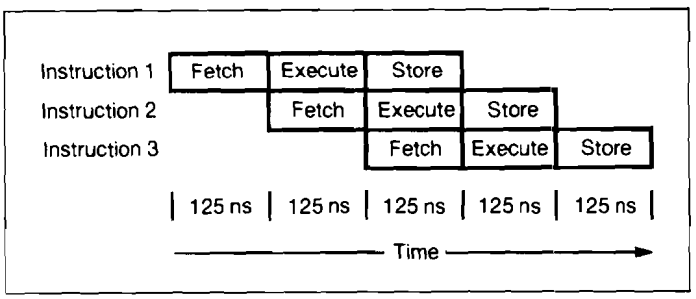


Figure 3. Instruction Pipelining

Floating Point Coprocessor

Single-precision and double-precision floating point calculations are performed by a Floating Point Coprocessor board. The coprocessor significantly decreases the time required to perform floating point calculations. The Floating Point Coprocessor and the CPU operate in parallel for maximum efficiency.

Virtual Memory Management

Virtual Addresses on the Model 840 are 48 bits long, ensuring sufficient expandability to meet growing software needs. As shown in Figure 4, Virtual Memory is divided into a set of 65,536 spaces, with each space 4 GB long. Spaces are further divided into fixed length 2 kB pages, with a given page holding data, code, or both. A single data structure can be up to 1 GB long.

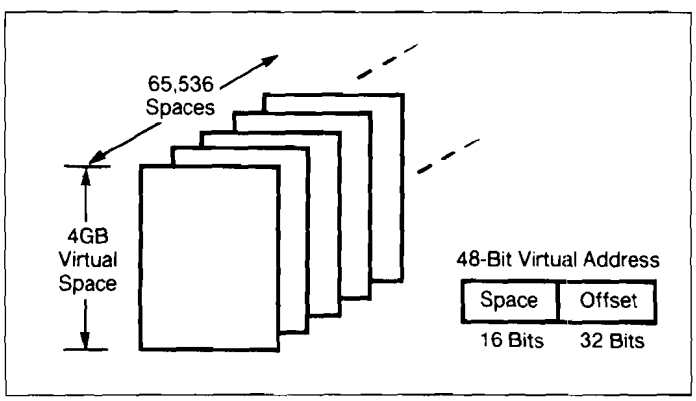


Figure 4. Virtual Memory Organization

Virtual Address Translation

Virtual-to-Physical address translation is done by Translation Lookaside Buffers (TLBs), which cache recently accessed virtual page translations and convert the 48-bit virtual address into a 28-bit physical address. The Model 840 TLB holds translations for 4096 virtual pages, and is split into a 2048-entry instruction TLB and a 2048-entry data TLB to facilitate parallel translation of instruction and data addresses. The Model 840 implements page-level access protection and the TLB hardware supports protection mechanisms to assure that the currently executing process has sufficient authorization to perform requested data, code, and I/O accesses.

Memory Subsystem

The Model 840 includes 8 MB of ECC memory, expandable in 8 MB increments to 24 MB. Each 8 MB block of memory includes its own integrated array and controller. The memory subsystem uses 256K-bit dynamic RAMs. Main memory is backed up such that if AC power is lost and restored within 15 minutes, the operating system is automatically restarted and processing can resume without data loss.

The internal memory word size is 39 bits, with 32 data bits plus seven bits for error detection and correction. Single-bit errors are automatically corrected. Multi-bit errors are automatically detected, causing an interrupt. Overall, the ECC memory of the Model 840 guarantees high performance and high availability.

I/O Subsystem

I/O Bus

The Model 840 has one general-purpose channel I/O (CIO) bus. This 16-bit I/O bus is used for connection of peripheral devices and data communication cards. It has 12 available I/O slots, two of which are used for included HP-IB and multi-plexer interfaces.

The I/O Manager

The Channel I/O (CIO) Adapter interfaces the central system bus to the CIO bus, synchronizing their differing speeds and bandwidths. The CIO Adapter manages Direct Memory Access (DMA) transfers between CIO interfaces with their associated peripherals and main memory. Because the CIO Adapter accomplishes this function with little CPU intervention, interrupting only to signal completion of DMA transfers, it leaves the CPU free to perform other operations during I/O. Large blocks of data can be transferred to/from main memory at rates to 5 MB per second with negligible CPU overhead.

Peripheral Connection

The HP 9000 Model 840 uses the following device interface cards for connection to peripheral devices or other systems:

- HP 27110B HP-IB card for discs, tape drives, printers, and plotters
- HP 27140A Six-channel Multiplexer for terminals and other RS-232-C devices and for uucp comunication with other systems running under the UNIX operating system
- Interface card in HP 98194A LAN/9000 Series 800 Link interface-software package for inter-system communication
- HP 27114A Parallel Asynchronous FIFO Interface (AFI) card for miscellaneous interfacing

NOTE: The following paragraphs briefly discuss the HP-UX operating system and other software products for the HP 9000 Model 840 super minicomputer system. More detailed information is provided in the HP 9000 Series 800 Software Technical Data book, HP Literature Stock Number 5953-8788.

The Operating System

The Model 840 System supports the HP-UX operating system. HP-UX is a superset of AT&T's System V Interface Definition (Issue 1). In addition, HP-UX incorporates features from U.C. Berkeley release 4.2 BSD and all non-hardware dependent utilities from AT&T's System V.2 UNIX system. HP-developed extensions add significant capabilities, such as real-time functionality that includes priority-ordered time and event scheduling of programs with real-time process dispatch latency for fast response.

Native Language Support

HP-UX, terminals, printers, and plotters provide facilities and options for supporting 18 different native languages. Languages supported include American English, Canadian French, Danish, Dutch, U.K. English, Finnish, French, German, Italian, Japanese, Greek, Turkish, Norwegian, Spanish, Swedish, Portuguese, Arabic, and Hebrew.

Graphics

Graphics applications in the Model 840 are supported by the HP 92436A Starbase Graphics Library for high performance or the HP 92437A DGL, AGP, and Starbase libraries package, which provides upward compatibility with AGP/DGL graphics applications moved from HP 1000 systems or HP 9000 computers.

Program Languages

HP-UX includes a C language program compiler and an Assembler and supports the HP 92430A FORTRAN 77 and HP 92431A Pascal compilers. The C, FORTRAN 77, and Pascal compilers all analyze their program input and optimize the object code to maximize execution efficiency.

Device I/O Library

A Device I/O Library (DIL) simplifies programming of control of, and communication with, peripheral devices or instruments connected to the Model 840 system via the HP 27110B HP-IB interface or the HP 27114A Parallel AFI interface.

System Networking

The Model 840 connects to other HP 9000 systems and to HP 1000 A-Series systems via an IEEE 802.3 compatible Local Area Network (LAN). The hardware interface and transport and interface software are provided in the HP 98194A LAN/9000 Series 800 Link product. Higher-level Network Services are supported by HP 98195A NS/9000 Series 800 software. Together, the 98194A and 98195A products support Remote File Access (RFA) between HP-UX based HP 9000 systems, Network File Transfer (NFT) with HP 9000 systems and HP 1000 systems, and Network Interprocess Communication (Net IPC) between HP 9000 Series 800 systems.

In addition to LAN communication, Model 840 systems can communicate with other UNIX systems via one or more multiplexer channels and hardwired or modem links using the uucp capability of the HP-UX operating system. The uucp capabilities include file transfer, remote command execution (uux), and terminal emulation (cu). HP-UX electronic mail uses the uucp facility.

ARPA/Berkeley networking services based on TCP/IP protocol are also available on the Model 840.

Database Management

Database management is provided by the uniquely versatile HP 32617A ALLBASE/HP-UX Database Management System (DBMS). The ALLBASE DBMS features both a relational data model HPSQL interface and a network model HPIMAGE interface for upward compatibility with existing IMAGE/1000 databases.

HPtoday

The HP 92440A HPtoday Developer Pack is a software system for computer-assisted development of applications. HPtoday applications are developed by filling in blanks on formatted screens instead of coding reams of program instructions. By bridging the gap between conception and the resulting application, HPtoday significantly shortens the time required to develop useful, bug-free applications, greatly boosting productivity. The HP 92441A HPtoday Run-Time Environment supports execution of developed HPtoday applications on target systems.

HP 1000 Applications Migration

The Model 840 system includes a PORT/HP-UX package to help customers move applications from HP 1000 systems operating under RTE-A or RTE-6/VM to the HP-UX environment of the Model 840 system. In addition to emulation of most RTE calls on HP-UX, PORT/HP-UX provides tools for analysis of applications to determine what program statements need to be changed and instructions on what kinds of changes are needed.

In addition to addressing operating system related migration issues, PORT/UX and the new ALLBASE/ HP-UX DBMS provide facilities for migration of IMAGE/1000 and IMAGE/1000-II databases. The DGL and AGP libraries for the Model 840 system differ only slightly from the DGL and AGP libraries for HP 1000 systems, which simplifies migration of graphics applications to the HP 9000 Model 840. For more information on HP 1000 applications migration, see the HP 9000 Series 800 Software Technical Data book, HP Literature Stock Number 5953-8788.

HP 9000 Applications Migration

Applications currently running under HP-UX on HP 9000 Series 200, 300, or 500 computers are highly compatible with the HP 9000 Model 840 In many cases a simple recompilation will be all that is needed to port current applications on HP 9000 computers to the HP 9000 Model 840.

Functional Specifications

Capacity

Memory: 8, 16, or 24 megabytes of ECC memory.

Battery Backup: Sustains 24 megabytes of memory for at least 15 minutes when fully charged.

Available I/O Channels: 12, of which two are used by the multiplexer and HP-IB interface cards that are included in the Model 840 system.

Terminals: The multiplexer card furnished with the Model 840 system can connect the system console, a modem for remote support, and four other terminals or other RS-232-C devices to the system. With additional multiplexers, each using one I/O channel and supporting six terminals, up to 60 terminals can be supported.

Disc Memory: The HP-IB interface furnished with the Model 840 system can connect four 132 MB or 404 MB disc drives to the system. Additional HP-IB interfaces can each connect four discs to the system. The total number of discs that can be supported is determined by I/O channel availability. An HP-IB interface used to connect discs can also support connection of CS-80 tape cartridge devices, but no other HP-IB devices.

Central Processor Unit

Word Size: 32 bits.

Virtual Memory Address Space: 48 bits (281,000 GB).

Physical Address Space: 28 bits (128 MB).

Base Instruction Set: 138 instructions.

Cycle Time: 125 nanoseconds.

Base Instruction Time: 125 ns, except for eight instructions that take 250 ns.

TLB Misses: Typically add 8125 ns to instruction time less than 1% of the time.

Data Cache Faults: Add 125 to 1875 ns to instruction time (1250 ns, average) less than 4% of the time.

Instruction Cache Faults: Add 500 to 875 ns to instruction time (750 ns, average) less than 3% of the time.

Nullified Instructions: Use 125 ns of processor time.

Average Instruction Time: 220 ns, including the effects of TLB misses, cache faults, nullified instructions, and interlocks.

Average CPU Execution Speed: 4.5 MIPS.

Floating Point Coprocessor

Floating Point Instructions: 40 instructions.

Floating Point Speed: 2 million B1D Whetstones per second.

Floating Point Format: ANSI/IEEE 754-1985 standard floating point format.

Input/Output

I/O Addresses: Determined programmatically and by card slot location.

Direct Memory Access: Data chaining and command chaining are supported with 32-bit count and address.

DMA Bandwidth: 5 MB/sec for transfers via the 27114A Parallel Async FIFO Interface, 3 MB/sec for transfers via the 27110B HP-IB Interface, the 27140A Six-Channel Multiplexer, or the LAN interface in the 98194A LAN/9000 Series 800 Link.

Data Packing: DMA transfers must be aligned to 32-byte boundaries in memory.

Supported Peripherals

See the HP 9000 Series 800 Configuration Guide for configuration requirements.

Supported Terminals

HP 2392A Display Terminal
HP 2393A Graphics Terminal
HP 2394A Data Entry Terminal
HP 2397A Color Graphics Terminal with 35741A Monitor
HP 45711A Portable Plus Computer
HP 45610B Touchscreen Terminal
HP 45850A Touchscreen II Terminal
HP 45851A Touchscreen II Personal Computer
HP 72425A VECTRA PC (req. 35731A or 35741A)
HP 72435A VECTRA PC (req. 35731A or 35741A)
HP 72445A VECTRA PC (req. 35731A or 35741A)
HP 9807A INTEGRAL Personal Computer
HP 98561A Model 310 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)
HP 98561B Model 320 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)

Supported Discs

HP 7933H* 404 MB CS-80 Fixed Disc
HP 7935H* 404 MB Removable Media CS-80 Disc
HP 7914CT 132.1 MB CS-80 Fixed Disc w/CTU backup
HP 7914P/R 132.1 MB CS-80 Fixed Disc w/CTU backup
HP 7914ST 132.1 MB CS-80 Fixed Disc and 1600 cpi Mag Tape Unit in tall cabinet

Supported Magnetic Tape Units

HP 7974A	Magnetic Tape Unit
HP 7978B	Magnetic Tape Unit
HP 35401A	Cartridge Autochanger Tape Subsystem
HP 9144A	CS-80 Cartridge Tape Subsystem

*The 7933H/7935H Disc is highly recommended as system disc because of its high capacity.

Supported Printers

HP 2563A	300 LPM Dot Matrix Line Printer
HP 2564B	600 LPM Dot Matrix Line Printer
HP 2566B	900 LPM Dot Matrix Line Printer
HP 2567B	1200 LPM Dot Matrix Line Printer
HP 2686A+300	LaserJet Plus Printer
HP 2934A+046	200/67/40 cps Office Printer

Supported Plotters

HP 7440A	8-pen ColorPro Plotter
HP 7475A	6-pen Plotter
HP 7550A	8-pen Plotter w/Auto sheet feed
HP 7586B	8-pen Roll-Feed Drafting Plotter

Supported Data Communication Devices

HP 37212A Intelligent 300/1200 baud modem
HP 92205A Hayes Smartmodem 1200™
HP 92223A LAN Repeater Kit

NOTE: For other LAN connection accessories, see the Hewlett-Packard Computer User's catalog.

Smartmodem 1200™ and Smartmodem 2400™ are trademarks of Hayes Microcomputer Products, Inc.

Electrical Specifications

AC Power Input

Line Voltage: 200-240VAC, single phase.

Input Voltage Tolerance: 170-276VAC.

Line Frequency: 50 or 60 Hz +10%/-5%.

Maximum Power Required: 1350W.

Maximum Operating Current: 13A.

Battery Backup Time: 15 minutes, minimum, for 24 MB memory.

DC Current Available and Required for I/O Interfaces and Accessories

The Model 840 system power supply provides enough current and power for any combination of I/O interfaces or other plug-in cards that can be installed in the system's card cage.

SPU Environmental Specifications

Temperature

Operating: 0° to 55°C (32° to 131°F).

Non-operating: -40° to 70°C (-40° to 158°F).

Relative Humidity

5% to 95% at 40°C, non-condensing.

Altitude

Operating: To 4.6 km (15,000 ft).

Non-operating: To 15.3 km (50,000 ft).

Vibration and Shock

HP 9000 Model 840 Systems are type tested for normal shipping and handling shock and vibration (contact factory for review of any application that requires operation under continuous vibration).

Regulatory Compliance

Safety

UL Listed, CSA Certified Compliant to IEC 380/435

Electromagnetic Interference

Complies with FCC Rules and Regulations, Part 15, Subpart J, as a Class A computing device. FTZ licensed as a Level A computing device.

Acoustics

6.5 bels (A) Sound Power

Physical Characteristics

Dimensions

1 metre (39.4 in.) high, 60 cm (23.6 in.) wide, 96.5 cm (38 in.) deep, including 15 cm (6 in.) rear clearance for ventilation and cables.

Weight

160 kg (352 lb).

Ventilation

Four fans pull air from top to bottom for system cooling.

Ordering Information

NOTE: HP 9741A SPUs require a terminal and a disc (not included) for operator communication and for operating system and program development support. A magnetic tape unit is strongly recommen-ded for software installation and backup and is required when an HP 7933H or 7935H is the system disc.

HP 9741A System Processor Unit for the HP 9000 Model 840 System

The HP 9741A System Processor Unit includes:

1. Processor with 8 MB ECC memory, floating point coprocessor, six-channel multiplexer and HP-IB disc interfaces, access port card, 10 available I/O channels, and power distribution unit with power cable in 1-metre cabinet.
2. HP-UX Version B.1, 1-16 user, featuring C compiler and the HP-UX Symbolic Debugger. Also includes Assembler, Device I/O Library, Real-Time package, and Port/HP-UX. On-line diagnostics and manuals listed in the HP-UX data sheet in the HP 9000 Series 800 Software Technical Data book are provided. Must order software Media Option AA0 or AA1.
3. Hardware Support Manual, Volume 1 of 2 (09740-90011).
4. Hardware Support Manual, Volume 2 of 2 (09740-90012).

5. System Log (09740-90013).
6. Architecture Manual (09740-90014).
7. Multiplexer Interface Installation Manual (27140-90002).
8. HP-IB Interface Installation Manual (27110-90005).
9. Site Preparation Consultation.
10. On-site installation assistance and checkout by a Hewlett-Packard Service Engineer, including integration and test with primary system.
11. 90-day on-site warranty.

Software Media Options

AA0: Software on CS-80 cartridge tape.

AA1: Software on 1600 cpi mag tape.

Additional Memory, I/O Cards, and Terminal Cable Management Accessories

19748A 8 MB ECC Memory (two cards, max. of two 19748A additional memory packages per 9741A).

27110B HP-IB Interface with 27110B Option 800 2 metre cable.

27140A Six-Channel Multiplexer with 27140A Option 800 4 metre interface-to-connector panel cable.

27114A Parallel Asynchronous FIFO Interface card (see data sheet to determine appropriate options to order).

98194A LAN/9000 Series 800 Link for communication over IEEE 802.3 compatible LAN. Link software is supplied on CS-80 cartridge tape unless Media Option AA1 is ordered to request the software on 1600 cpi mag tape. The HP 98194A product is orderable only with the HP 98195A NS/9000 Series 800 product, listed below.

98195A NS/9000 Series 800 Network Services Software for Network File Transfer and Remote File Access. Orderable only with the HP 98194A LAN/9000 Series 800 Link product. Software is on CS-80 cartridge tape unless Media Option AA1 is ordered to request the software on 1600 cpi mag tape.

19749A Cable Management System for housing up to 11 multiplexer connector panels and managing the associated interconnect cables. (See photo at right.) The connector panel compartment is mounted on the rear of a system console support table.

Upgrading HP-UX Licenses

92453A HP-UX 32-user license with same software as listed in 9741A, item 2, above. Must order soft-ware Media Option AA0 or AA1, listed above.
-0A0 Credit for upgrade from 16-user license.

92454A HP-UX 64-user license with same software as listed in 9741A, item 2, above. (Maximum of 60 users per system, due to limited I/O slots.) Must order software Media Option AA0 or AA1, listed above.
-0A1 Credit for upgrade from 16-user license.
-0A2 Credit for upgrade from 32-user license.

Additional Software

(Must order software media option AA0 or AA1.)

92430A/R	FORTRAN 77/HP-UX compiler.
92431A/R	Pascal/HP-UX compiler.
36217A/R	ALLBASE/HP-UX Relational and IMAGE database management system package with IMAGE/1000 translator.
92437A/R	DGL/AGP/HP-UX Graphics Libraries with Starbase/HP-UX Graphics Library to support Graphics/1000-II DGL/AGP applications on the HP 9000 Model 840 System.
92436A/R	Starbase/HP-UX Graphics Library.
92438A	Development System bundle, including FORTRAN 77 and Pascal compilers and DGL/AGP and Starbase graphics libraries.
92440A/R	HPtoday Developer Pack (includes 92441A).
92441A	HPtoday Run Time Environment.
92442A	ALLBASE and HPtoday Developer Pack bundle.

Supported Peripheral and Data Communication Devices

See page 11.

HP-IB Interface

HEWLETT PACKARD

For HP 9000 Series 800 Systems

product number 27110B

The HP 27110B HP-IB* interface supports connection of up to 14 Hewlett-Packard Interface Bus (HP-IB) devices to HP 9000 Series 800 Systems. HP-IB devices include discs, printers, plotters, magnetic tape devices, graphics digitizers and an extensive list of instruments.

Features

- Simplified implementation of computer-controlled instrumentation and peripheral systems
- IEEE-488-1978 compatibility
- 980 kilobytes per second high speed, 500 kilobytes per second standard speed
- On-board intelligence that off-loads the host computer, freeing CPU resources for application processing
- Support of up to 14 standard devices or up to 8 high speed devices (standard speed devices are not usable on the high speed bus)
- Support of Command Set 80 protocol for CS/80-based discs and tapes
- Selectable HP-IB controller or slave capabilities
- Parity and Cyclic Redundancy Checks for error detection
- Programatic enabling/disabling of parallel polling
- Firmware-based self-test of interface integrity

HP-IB Capabilities

The 27110B HP-IB Interface connects to the signal lines shown in Figure 1, acting as DEVICE A. Eight bidirectional data bus lines carry coded messages in bit-parallel, byte-serial form to/from other devices on the bus, with each byte transferred from one "talker" to one or more "listeners". Data is exchanged asynchronously using interface messages to set up, maintain, and terminate an orderly flow of device-dependent messages. Three data byte transfer control lines control the transfer of each byte of coded data on the eight data lines. The five general interface management lines ensure an orderly flow of information within the HP-IB.

Functional Specifications

Capacity

High speed devices per 27110B interface: Up to eight with load resistors installed. Up to 14 without.

Standard speed HP-IB devices per interface: Up to 14.

NOTE: Standard speed devices cannot be mixed on a high speed bus. High speed devices can be mixed on a standard speed bus if high speed cabling rules are observed.

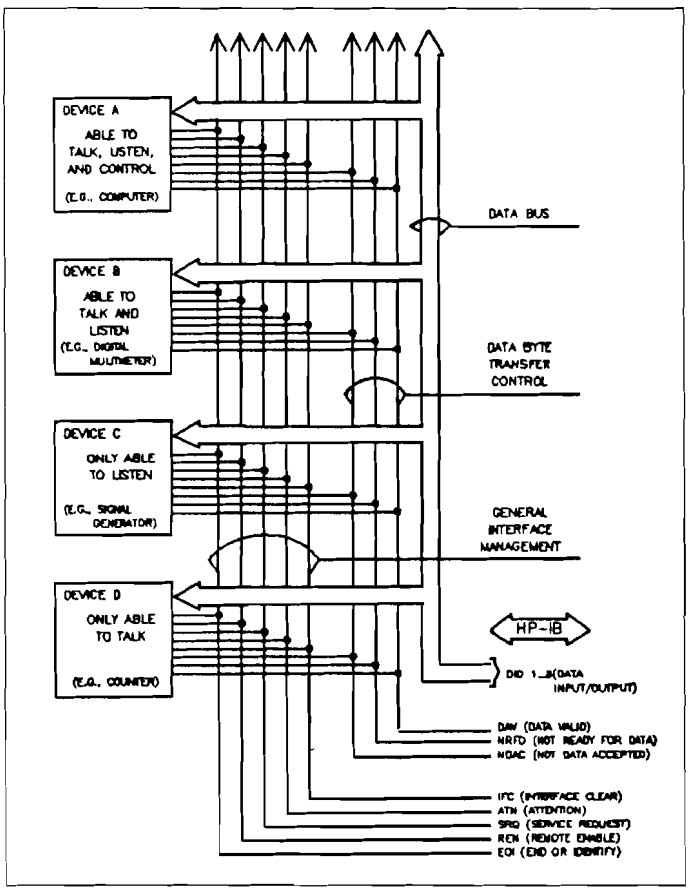


Figure 1. HP Interface Bus Concept

Operating Modes

High speed mode: Operation at data rates to 980 kilobytes per second.

Standard speed mode: Operation at data rates to 500 kilobytes per second.

NOTE: Realizable speed for a particular system is dependent on such factors as cable length, type of external device, system level software and number of devices. Higher transfer rates can be achieved when using less than maximum cable lengths and devices. Consult system documentation for further information.

*The Hewlett-Packard Interface Bus (HP-IB) is HP's implementation of IEEE Standard 488-1978: "Digital interface for programmable instrumentation" and identical ANSI standard MC1.1. The term "HP-IB" is also used to identify Hewlett-Packard instruments conforming with this standard.

System controller mode: A two position switch enables or disables 27110B operation as system controller.

Bus Characteristics

HP-IB Bus Signal lines:

DIO1	Data Input/Output 1
DI02	Data Input/Output 2
DI03	Data Input/Output 3
DI04	Data Input/Output 4
DI05	Data Input/Output 5
DI06	Data Input/Output 6
DI07	Data Input/Output 7
DI08	Data Input/Output 8
DAV	Data Valid
NRFD	Not Ready For Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Logic Levels: High > 2.4V/Low < 0.5V, all low-true

Supported HP-IB functions: C1-C5, SR1, RL2, PP1, DC1, SH1, AH1, T1, TE1, L1, LE1, DT1, E2. TE1 and LE1 require host system support.

Logic Levels, line terminations, line drivers, and line receivers: All characteristics conform to IEEE Standard 488-1978.

Maximum cable length for standard operation: 2 meters (6.5 ft) per device connected, with a 20 meter (65 ft) total length. The maximum number of devices is accommodated by interconnections using shorter than maximum cable length.

Maximum cable length for high speed operation: Interconnecting cable links should be as short as possible, with a maximum of 15 meters total length per system, and should have at least one equivalent resistive load per meter of cable (the high-speed resistor pack adds seven equivalent resistive loads).

Number of Devices	Maximum Total Cable Length (meters)
1	8
2	9
3	10
4	11
5	12
6	13
7	14
8 (maximum)	15

No more than eight devices are allowed in the system. A maximum system consists of the System Controller with its high-speed resistor pack and eight peripherals. Load resistors may need to be repositioned on the interface card for high speed operation. Refer to the installation manual.

NOTE: For high and low speed cable length operation, refer to the installation manual (27110-90005) for a complete explanation. The HP-IB connector mounting plate (30070-00043) should be used with extended cables. It is available from the Corporate Parts Center.

Error Detection

Data errors can be detected using Cyclic Redundancy Check-16 (CRC-16) on all data messages sent or received by another participating device that supports CRC-16. CRC-16 is invoked by the system for each transaction. See system documentation for details. Interface message errors are detected using odd byte parity.

Diagnostic Support

An interface resident self-test, initiated on reset, is provided in the firmware of the 27110B.

Direct Current Requirements

1.8A at +5V and 35 mA at +12V for total power dissipation of 9.42W.

Physical Characteristics

Dimensions: 172.7 mm (6.8 in.) long by 172 mm (6.75 in.) wide.

Weight: 234 grams (8.2 oz.); 679 grams (23.8 oz.) with HP-IB cable.

I/O Channel Interconnects: 80-pin connector, J1.

Device Interconnects: 26-pin connector, J2.

Environmental Specifications

Operating Temperature: 0° to 55°C (32° to 131°F).

Operating Humidity: 5% to 95% RH @ 40°C

Operating Altitude: 4600 metres (15,000 feet) maximum.

Ordering Information

HP 27110B HP-IB Interface

The 27110B includes:

1. HP-IB Interface Card (27110-60101).
2. Two-metre HP-IB cable (27110-63001).
3. Installation and Reference Manual (27110-90005).

27110B Options:

0B0: Deletes the Installation and Reference Manual (27110-90005).

800: Deletes standard cable (27110-63001) and substitutes two metre female cable (27113-63001) for use with HP 9000 Series 800 Computers.

Asynchronous 6-Channel Multiplexer

HEWLETT PACKARD

For HP 9000 Series 800 Systems — product number 27140A

The HP 27140A Multiplexer provides six asynchronous ports with full duplex modem control capability for connection of terminals or other RS-232-C devices to HP 9000 Series 800 Systems. A wide range of configurable transmission modes and formats supports direct or remote connection of CRT terminals, printers, plotters, and other asynchronous devices.

Features

- Six full-duplex asynchronous serial I/O ports with 10 wire modem control capability satisfying European license requirements.
- EIA RS-232-C and V.28 compatibility
- Full duplex modem operation only
- Supports local system console on port 0
- Programmable data rates for each channel
- Programmable character size: 5,6,7 or 8 data bits
- Programmable parity: odd, even, or none
- Programmable number of stop bits: 1, 1.5, or 2
- Parity, overrun, and framing error checks detect transmission faults
- Firmware based self-test of interface integrity
- Programmable device XON/XOFF handshaking to pace input and output data transmission
- On-board buffering with DMA capability to send/receive data to/from host for multiple ports in a single transfer

Functional Description

The HP 27140A Asynchronous 6-Channel multiplexer is used for interfacing up to six EIA RS-232-C compatible devices to the HP 9000 Series 800 System. As a Z80B microprocessor based interface, the HP 27140A MUX accesses a 16K byte EPROM which contains default port handling code for port zero and a power up self-test. Moreover, it monitors the download process and verifies the integrity of the code. The downloaded application software is optimized for character-at-a-time I/O.

Functional Specifications

Capacity

Channels: Six full-duplex channels

Buffering: On-card buffering with DMA capability to send/receive data for multiple ports in a single transfer increases throughput and reduces host CPU interrupts.

Transmit Buffer Size: 255 bytes per port.

Receive Buffer Size: Up to 1 Kbyte which is dynamically allocated among the 6 ports.

Communications

Interface Level: RS-232-C; CCITT V.28.

Data Rates: Baud rate defaults to 9600 and is software programmable to any of the following 15 rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19200.

Modem Support:

- originate mode
- auto answer mode
- modem connection timer
- lost receiver-ready timer
- no-activity timer
- host control of every interface output modem line

Supported Signal Lines:

RS-232-C	V.24	Common Abbrev.	Description	Input/ Output
AB	102	SG	Signal Gnd	
BA	103	SD	Trans'd Data	O
BB	104	RD	Received Data	I
CA	105	RS	Req. to Send	O
CB	106	CS	Clear to Send	I
CC	107	DM	Dataset Ready	I
CD	108/2	TR	Data Ter Ready	O
CF	109	RR	Received Line Signal Detector	I
CH	111	SR	Sig. Rate Sel.	O
CE	126	IC	Ring Indicator	I

Throughput: The 27140A 6-channel MUX will support six interactive terminal users running character mode at 19.2K baud. Other RS-232-C applications which may simultaneously send and receive data over all six ports should be run at 9600 baud or slower.

Communication Mode: Asynchronous, bit serial.

Break Detection and Transmission: Break condition is recognized by the interface and causes an interrupt to be sent to the host. Break condition can also be generated by the interface at the request of the host.

Optional Device Handshakes: The MUX is capable of pacing both inbound and outbound data via an "XON/XOFF" type of protocol. The "XON/XOFF" characters are programmable. Outbound MUX transmission or device controlled "XON/XOFF" is performed at the interface level. Host controlled "XON/XOFF" is available to pace the flow of incoming data from a peripheral. This is not done at the interface level but on host demand.

Edit Functions

Edit functions such as backspace, character delete, and line delete are passed to the host and managed by the host operating system.

Direct Current Requirements

Voltage	Typical Current	Two Standard Deviation Current
+5V	1.380 A	2.298 A
+12V	0.084 A	0.159 A
−12V	0.135 A	0.150 A

Physical Characteristics

Dimensions: 172.7 mm (6.8 in.) long by 172 mm (6.75 in.) wide.

Weight: Interface Card 270 grams (9.5 oz.); Cable and RS-232 panel 723 gram (26 oz.).

Environmental Specifications

Operating Temperature: 0° to 55°C (32° to 131°F).

Operating Humidity: 5% to 95% RH @ 40°C.

Ordering Information

HP 27140A Asynchronous 6-Channel Multiplexer

The 27140A includes:

1. 6-Channel Multiplexer Printed Circuit Assembly (27140-60001).
2. 1 metre interface to connector panel Cable (28659-63002).
3. RS-232-C Connector Panel (28659-60005).
4. Installation Manual (27140-90002).

27140A Options

0B0: Delete Manual (27140-90002).

001: 10 metre Extension Cable (28659-63004) used with 28659-63002 to remotely postion the RS-232-C connector panel.

019: 19 inch Rack Mounting Bracket Kit (5061-4962).

800: Deletes standard cable (28659-63002) and substitutes a longer 4 meter cable (28659-63006). Allows use with HP 9000 Series 800 computers.

A self-test hood connector for optional use with the on card self-test is available. Order HP Part Number 27140-60002.

Parallel Asynchronous FIFO Interface

HEWLETT PACKARD

For HP 9000 Series 800 Systems — product number 27114A

The HP 27114A Parallel Asynchronous FIFO Interface is designed to provide multipurpose 8 or 16-bit parallel communication capabilities between external devices and HP 9000 Series 800 Systems.

Features

- 16-bit parallel interface
- Separate data input and output lines
- Differential or single-ended line drivers/receivers
- Configurable to GND true or +5V true
- Asynchronous handshaking mode (interlocked) only
- Half-duplex operation (only)
- Up to 66 words of FIFO buffering
- Three frontplane control lines
- Two frontplane status lines
- Two parity bits for software parity checking
- Host interrupt via Attention line
- Switch-selectable data settling time

Functional Specifications

Data Transfer

Protocol: Transfer either 8 or 16 parallel bits at a time, without byte packing on 8-bit transfers. The backplane channel can operate either in byte mode or word mode.

Maximum Transfer Rates: For data transfers less than 66 words, the interface in word mode and using differential signaling, the theoretical maximum data transfer rate is:

3 Megabytes/sec at 50 meters
5 Megabytes/sec at 3 meters

Aggregate Transfer Rates: The aggregate throughput depends on the host processor, competing backplane activity and total transfer size. Throughput for 8 bit transfers will be roughly half that of the 16-bit transfers.

Maximum Distance: 50 meters

Backplane Polling

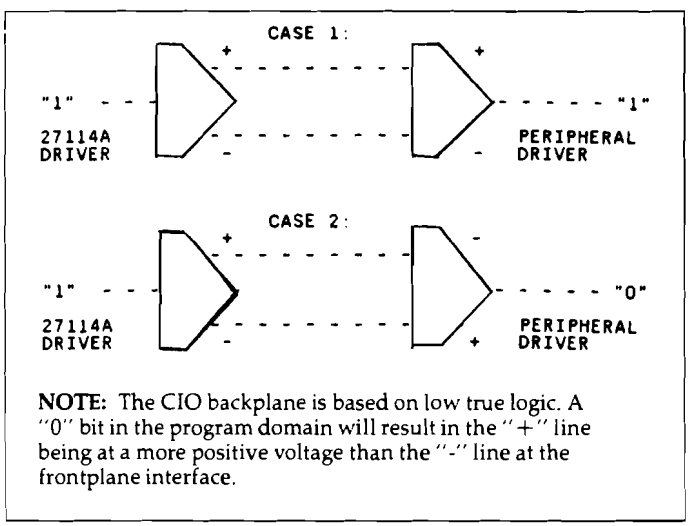
The 27114A is a group 0 polling device. This may impose certain backplane slot restrictions.

Line Characteristics

Signal Lines:

RD± 0-15	Received Data Positive/Negative Bus
SD± 0-15	Send Data Positive/Negative Bus
STS± 0-2	Status Input Positive/Negative Bus
CTL± 0-2	Control Output Positive/Negative Bus
RPAR± 0-1	Received Parity Positive/Negative Bus
SPAR± 0-1	Send Parity Positive/Negative Bus
PFLAG±	Peripheral Flag Positive/Negative
PCTL±	Peripheral Control Positive/Negative
ATTN±	Attention Positive/Negative
PDIR±	Peripheral Direction Positive/Negative
TEST−	Data Line Driver Enable (loopback hood detect)
GND 2	Signal Ground/Bus
SHIELD	Frame Ground

Logic Sense: Differential Mode — Logic sense is determined by the cable wiring. See example:



NOTE: The CIO backplane is based on low true logic. A "0" bit in the program domain will result in the "+" line being at a more positive voltage than the "-" line at the frontplane interface.

Single-ended Mode: Logic sense can be referenced to either +5V true or GND true. To minimize signal cross-talk, the optional single-ended cable should be used.

Internal Handshake Mode: The 27114A can also send data to or receive data from devices such as indicators or switches, that do not provide or use any type of handshake. This will require tying a control line to the peripheral flag line. Input data can be clocked on the rising or falling edge.

Control and Status Bit Communication

Control Output: Three control output bits may be sent to the interface device via an output control byte for use as control, command or address bits.

Status Input: Three status bits may be received from the interfaced device via an input control byte. The attention line can be programmed to cause an asynchronous request interrupt (ARQ).

Direct Current Requirements

Typically 2A at +5V; two standard deviation current is 2.25A.

Physical Characteristics

Dimensions: 172.2 mm (6.8 in,) long by 172 mm (6.75 in.) wide.

Weight: Interface Card, 243 grams (8.5 oz.); 3 meter cable 440 grams (15.5 oz.)

Environmental Specifications

Operating Temperature: 0° to 55°C (32° to 131°F).

Operating Humidity: 5% to 95% RH at 40°C.

Operating Altitude: 4600 metres (15,000 feet) maximum.

Ordering Information

HP 27114A Parallel Asynchronous FIFO Interface

The HP 27114A includes:

1. Printed circuit assembly (27114-60001).
2. Three metre cable assembly (27114-63001).
3. 96-pin Wirewrap connector kit (27114-60003).
4. (3) Resistor network, SIP, 8 x 1.5K x 3.3K ohm (1810-0906).
5. (3) Resistor network, SIP, 8 x 330 x 470 ohm (1810-0407).
6. Installation & Reference Manual (27114-90001).

27114A Options

0B0: Deletes Installation & Reference Manual (27114-90001).

002: Adds loopback test hood (27114-60002).

003: Deletes 3 meter cable (27112-63001) and adds single-ended positive true/ground true 3 meter cable (27114-63002).

HEWLETT PACKARD

For more information call the HP Sales Office listed in the White Pages. Or write or phone Hewlett-Packard, Data Systems Division, 11000 Wolfe Rd., Cupertino, CA 95014, (408) 257-7000.

Printed in U.S.A. 4/86
5953-8771