SERVICE MANUAL SUPPLEMENT

OPTIONS 050 AND 051 SERIAL INTERFACE

RS-232-C AND RS-423-A

For The MODEL 7310A GRAPHICS PRINTER

HEWLETT PACKARD

SERVICE MANUAL SUPPLEMENT

OPTIONS 050 AND 051 SERIAL INTERFACE RS-232-C AND RS-423-A FOR THE MODEL 7310A GRAPHICS PRINTER

SERIAL NUMBERS

This Service Manual Supplement applies to Options 050 and 051 in printers with Serial Prefix 1952A.

A higher Serial Prefix indicates that a change has been made to the printer, but not necessarily to Option 050 or 051. Any changes to these options will be described in a yellow Manual Changes Supplement to this manual.

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ILLUSTRATIONS

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual Supplement applies to Options 050 and 051 for the Model 7310A Graphics Printer, and is a supplement to the 7310A Service Manual, HP Part No. 07310-90000. For easy reference, this supplement is divided into the following sections:

Section I	General Information
Section II	Interfacing
Section III	Performance Test
Section IV	Replaceable Parts
Section V	Manual Changes
Section VI	Service

1-3. Information for interfacing, operating, and programming the Model 7310A with Option 050 or 051 will be found in the Model 7310A User's Manual, HP Part No. 07310-90001, and the Model 7310A Interface Manual, HP Part No. 07310-90002.

1-4. This General Information section contains the specifications for Options 050 and 051, safety considerations, and warranty information.

1-5. SPECIFICATIONS.

1-6. Table 1-1 lists the Model 7310A interface specifications that apply to Options 050 and 051.

Table 1-1. Specifications

OPTION 050 - RS-232-C/CCITT V.24 asynchronous serial interface for hardwired connection to remote computer systems and terminal.

Data Rate:	110 to 19 200 baud and external clock control
Transmission:	Full duplex protocol
Parity:	Odd, even, or none
Data Handshake:	ENQ/ACK, X-ON/X-OFF, and "Printer Busy" signal as selected by rear panel switch
Connector	25-pin female connector
Maximum Cable Length:	15 metres (50 feet)

OPTION 051 - RS-423-A asynchronous serial interface for hardwired connection to remote computer systems and terminal.

Data Rate:	110 to 19 200 baud and external clock control
Transmission:	Full duplex protocol
Parity:	Odd, even, or none
Data Handshake:	ENQ/ACK, X-ON/X-OFF, and "Printer Busy" signal as selected by rear panel switch
Connector:	37-pin female connector
Maximum Cable Length:	60 metres (200 feet)

1-7. SAFETY CONSIDERATIONS.

1-8. Safety information relevant to the service procedure being described is provided in the appropriate sections of the 7310A Service Manual and this Service Manual Supplement. The Model 7310A and both manuals should be reviewed for safety markings and instructions before service work is performed.

1-9. DESCRIPTION.

1-10. Options 050 and 051 provide full duplex serial interface instead of the HP-IB interface that is provided in the standard Model 7310A. Option 50 conforms to EIA Standard RS-232-C and CCITT V.24, and Option 051 conforms to EIA Standard RS-423-A.

1-11. RECOMMENDED TEST EQUIPMENT.

1-12. Test equipment needed to service the Model 7310A with Option 050 or 051 is listed in Section I of the Model 7310A Service Manual, HP Part No. 07310-90000.

SECTION II

INTERFACING

2-1. INTRODUCTION.

2-2. This section describes the interface requirements for Options 050 and 051. The interface rear panels for both options are identical except for the connector. Figure 2-1 lists the interface connections for Option 050 and Figure 2-2 shows Option 051.

2-3. BAUD RATE SELECTION.

2-4. The rear panel BAUD RATE switch may be set to select one of eight internally generated baud rates. The rate selected must be the same as the baud rate of the controlling device. The rear panel INTERNAL/EXT CLK switch must be set to INTERNAL in order to select the internally generated baud rates.

2-5. EXTERNAL CLOCK.

2-6. When the rear panel INTERNAL/EXT CLK switch is set to EXT CLK, the interface must be controlled by an externally supplied clock signal. The frequency supplied must be 16 times the desired baud rate. Maximum frequency is 307.2 kHz (16 x 19 200 Hz). The clock signal should be TTL compatible, 50% duty cycle. The input circuit is one TTL low power Schottky load.

2-7. PARITY SELECTION.

2-8. Parity checking is controlled by two rear panel switches, PRTY OFF/ON and PRTY EVEN/ODD.

2-9. STANDBY MODE.

2-10. When the 7310A (Option 050 or 051) is turned on, it automatically enters the "On Line" mode. Pressing the front panel STBY once places it in the "Standby" mode, which stops printing activity. Pressing STBY the second time returns the 7310A to the "On Line" mode.

2-11. STOP BIT.

2-12. One stop bit is supplied in all baud rates except 110 baud, when two stop bits are present.

2-13. INTERFACE CABLE LENGTH AND DATA SIGNAL RATE.

2-14. Maximum length of the interface cable for Option 050 is 15 meters (50 feet).

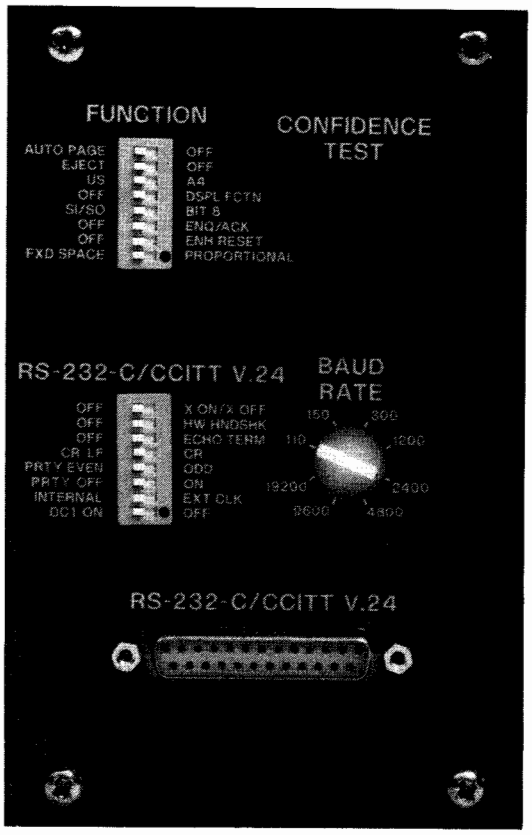
2-15. Maximum length of the interface cable for Option 051 is 60 meters (200 feet).

2-16. VOLTAGE LEVELS.

2-17. Table 2-1 shows the required voltage levels for data and control circuits for both options.

Table 2-1. Voltage Levels

		RS-232-C/CCITT V.24		RS-423-A	
	Voltage Range:	-5V to -15V	+5V to +15V	-4V to -6V	+4V to +6V
Data Circuits:	Binary State	1	0	1	0
	Signal Condition	Mark	Space	Mark	Space
Control Circuits:		Off	On	Off	On

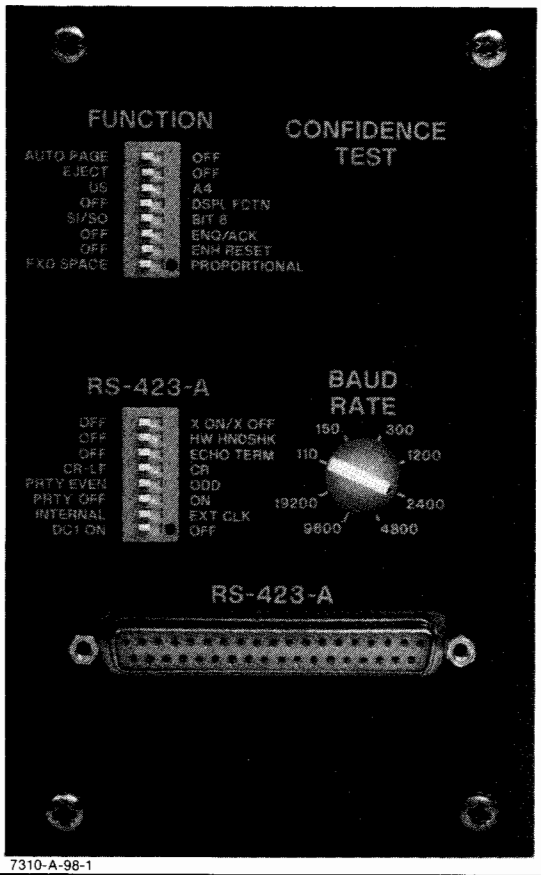


7310-A-97-1

Connector Pin No.*	RS-232-C Circuit	CCITT V.24 Circuit	Description
1	AA	101	Protective Ground
2	BA	103	Transmitted Data
3	BB	104	Received Data
4	CA	105	Request to Send
7	AB	102	Signal Ground (Common Return)
17	DD	115	External Clock (16 x Baud Rate)
19	SCA	120	Secondary Request to Send
20	CD	108.2	Data Terminal Ready

* Only those pins that are used in the 7310A Option 050 are listed.

Figure 2-1. RS-232-C/CCITT V.24 Interface Connections



7310-A-98-1

Connector Pin No.*	RS-423-A Circuit	Description
1		Shield
4	SD	Send Data
6	RD	Receive Data
7	RS	Request to Send
8	RT	Receive Timing (Ext Clk - 16 x Baud Rate)
12	TR	Terminal Ready
19	SG	Signal Ground
22	SD Ret	** Send Data Return
24	RD Ret	Receive Data Return
25	RS Ret	** Request to Send Return
30	TR Ret	** Terminal Ready Return
37	SC	** Send Common

* Only those pins that are used in the 7310A Option 051 are listed.
** These lines are connected to Signal Ground (pin 19).

Figure 2-2. RS-423-A Interface Connections

SECTION III

PERFORMANCE TEST

3-1. INTRODUCTION.

3-2. The Confidence Test checks most of the circuits on the Serial I/O PCA, A3. This test should be run before using the printer and after any service has been performed on the printer.

3-3. CONFIDENCE TEST.

a. Set the LINE switch to ON.

NOTE

If the printer does not contain paper, follow the instructions on the inside of the paper compartment cover to insert a roll of paper.

CAUTION

Before installing a new roll of paper, be sure to remove all the paper that has adhesive on it. Adhesive may cause the paper to stick to the transport path.

b. Wait until the printer has advanced, cut, and ejected the paper, then press and release the rear panel CONFIDENCE TEST switch.

c. If the printer passes the test, it should do the following:

1. After a short pause, print one full row of dots across the page (appears as a solid line except for small gaps between heads). Print intensity will be less than normal.

2. Advance, cut and eject the paper (about six inches).

3. Print ROM check sums. Figure 3-1 shows a sample printout.

4. After another pause, print "Confidence Test Passed" followed by a printout of all the character sets installed in the printer, together with the ROM location (@,@',A,B,C,D), Q Parameter, and ID Code.

5. Print the settings (1 or 0) of the rear panel FUNCTION and SERIAL switches, and the Character Q Parameter (SW1) and I.D. Code (SW2) switches located on the serial I/O PCA.

6. Advance, cut, and eject the paper.

d. If the printer fails the Confidence Test, it may print partial or complete tests results, or it may print nothing, depending upon the area of failure. In some cases, the printer logic may "lock up" in an area and never complete the test. Refer to the Confidence Test flow chart and failure information in Section VI in this manual supplement and in Section VI in the 7310A Service Manual. A sample printout of a Confidence Test failure is shown in Figure 3-2.

C3FF ← PROGRAM ROM CHECK SUM TOTAL +5

NOTE: CHECK SUMS ARE HEXADECIMAL

PROGRAM ROM CHECK SUMS:

ECFF ← A2U1
26FF ← A2U2
49FF ← A2U3
01FF ← A2U4
26FF ← A3U17
3CFF ← A3U18

CHARACTER SET ROM CHECK SUMS:

38FF ← A3U26
63FF ← A3U27
33FF ← A3U44

Confidence Test Passed

Default Primary
OU
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNO
PQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~▒

Default Secondary
OE
´ ` ˆ ¨ ˜ £ ¯ ° ÇÑñ¡¿¤£ § âêôûáéóúàèòùäëöü
ÅîØÆåíøæÄìÖÜÉïß ↑√π→Σ⊢|ʊFtÅ¥₁₀½ᵥ

Sets Installed

Location ●
OU
[illegible] !"#$%&'()*+,-./0123456789:;<=>?
@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~▒

Location ●'
3U
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNO
PQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~▒

Location D
OE
´ ` ˆ ¨ ˜ £ ¯ ° ÇÑñ¡¿¤£ § âêôûáéóúàèòùäëöü
ÅîØÆåíøæÄìÖÜÉïß ↑√π→Σ⊢|ʊFtÅ¥₁₀½ᵥ

Function
00000000
SERIAL
01000000
SW1
00000000
SW2
00000101

7310-A-99-1

Figure 3-1. Confidence Test Passed

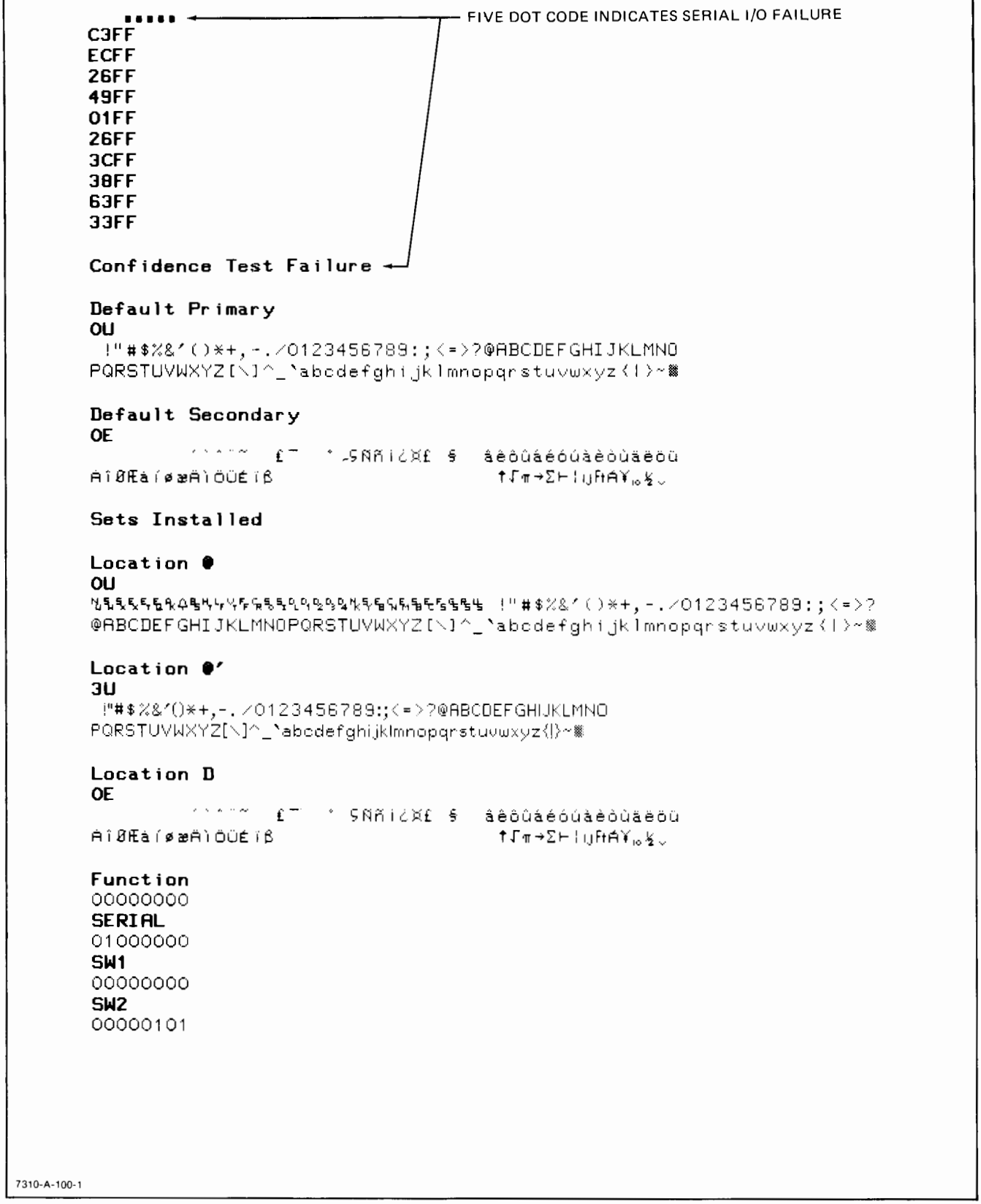


Figure 3-2. Confidence Test Failure

SECTION IV

REPLACEABLE PARTS

4-1. INTRODUCTION.

4-2. This section contains information needed to order parts for the Serial I/O option assemblies.

4-3. EXCHANGE ASSEMBLY.

4-4. The Serial I/O PCA, A3, used in both Option 050 and 051 is available as an exchange assembly. This factory repaired and tested assembly is available on an exchange basis; therefore, the defective assembly must be returned for credit. The part number of the exchange assembly is 07310-66530.

4-5. REPLACEABLE PARTS LISTS.

4-6. Replaceable Parts for the Option 050 and 051 assemblies are listed in Table 4-1 through 4-3. Parts for other assemblies in the printer are listed in Section IV of the 7310A Service Manual.

4-7. ORDERING INFORMATION.

4-8. To obtain replacement parts or assemblies, address an order or inquiry to the nearest Hewlett-Packard Sales and Service Office. The order should include the part or assembly number, its description and location, and the printer model and serial number. A list of Sales and Service Offices is located at the rear of this manual.

4-9. CODE LIST OF MANUFACTURERS.

4-10. Table 4-4 lists the five-digit code numbers assigned to the manufacturers of parts in Options 050 and 051. These code numbers appear with the parts in Tables 4-1 through 4-3, as an aid for ordering parts directly from the manufacturer.

4-11. DESIGNATORS AND ABBREVIATIONS.

4-12. Table 4-5 lists designators and abbreviations used throughout the manual. Abbreviations in the Parts Lists are always capital letters. In other parts of the manual both upper and lower case abbreviations are used.

Table 4-1. Replaceable Parts, Serial I/O PCA, A3, Options 050/051

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	07310-60530	2	1	PCA, SERIAL I/O, NEW	28480	07310-60530
	07310-66530	4		PCA, SERIAL I/O, REBUILT	28480	07310-66530
A3C1	0180-0197	8	3	CAPACITOR-FIXED 2.2μF 20V TA	04200	150D225X9020A2-DYS
A3C2,3	0160-3533	0	2	CAPACITOR-FIXED 470PF 300V MICA	28480	0160-3533
A3C4	0180-0197	8		CAPACITOR-FIXED 2.2μF 20V TA	04200	150D225X9020A2-DYS
A3C5	0180-0228	6	1	CAPACITOR-FIXED 22μF 15V TA	04200	150D226X9015B2-DYS
A3C6	0180-0197	8		CAPACITOR-FIXED 2.2μF 20V TA	04200	150D225X9020A2-DYS
A3C7-30	0160-3847	9	24	CAPACITOR-FIXED .01μF	04200	292CX7R153M050C
A3CR1,2	1901-0050	3	2	DIODE – SW 80V 200MA	02237	FDH 6308
A3J1	1251-6085	7	1	CONNECTOR, 40 PIN M	02312	SS-800-576
A3R1-4	0698-3449	6	4	RESISTOR-FIXED 28.7K 1% .12W F	02273	CEA-993
A3R5	0757-0280	3	1	RESISTOR-FIXED 1K 1% .12W F	02273	CEA-993
A3R6	0698-0090	7	1	RESISTOR-FIXED 464 1% .5W F	02273	CEC-993
A3R7,8	0757-0449	6	2	RESISTOR-FIXED 20K 1% .12W F	02273	CEA-T-O
A3R9	0757-1090	5	1	RESISTOR-FIXED 261 1% .5W F	02273	CEC-993
A3RN1-7	1810-0279	5	7	R NETWORK 4.7K 2% X 9	01607	210A472
A3S1,2	3101-2303	9	2	SWITCH-DIP 7 RKR	04990	76S807S
A3U1	1820-2198	2	1	IC-TTL S DUAL LINE RCVR	02237	9637ATC
A3U2	1820-2096	9	2	IC-TTL LS DUAL BIN CNTR	01698	SN74LS393N
A3U3	1820-1217	4	1	IC-MUX TTL LS	02910	SN74LS151N
A3U4	1820-1205	0	1	IC-GATE TTL LS AND DUAL 4-IN	02910	SN74LS21N
A3U5	1820-1208	3	2	IC-GATE TTL LS OR QUAD 2-IN	02910	SN74LS32N
A3U6	1820-1199	1	3	IC-INV TTL HEX LS	02910	SN74LS04N
A3U7	1820-1201	6	1	IC-GATE TTL LS AND QUAD 2-IN	02910	SN74LS08N
A3U8	1820-1216	3	2	IC-DCDR TTL LS	02910	SN74LS138N
A3U9,10	1820-1918	2	9	IC-TTL LS OCTAL LINE DRVR	01698	SN74LS241N
A3U11	1820-1416	5	1	IC-INV HEX TTL LS	01698	SN74LS14N
A3U12,13	1820-1430	3	2	IC-TTL LS 8IN CNTR	01698	SN74LS161AN
A3U14	1820-0471	0	1	IC-INV TTL HEX	02910	7406N
A3U15	1820-1195	7	1	IC-FF TTL LS	02910	SN74LS175N
A3U16	1820-1207	2	1	IC-GATE NAND TTL LS 8-IN	02910	SN74LS30N
A3U17	1818-1523	3	1	IC-ROM	28480	1818-1523
A3U18	1818-1522	1	1	IC-ROM	28480	1818-1522
A3U19,20	1820-1918	2		IC-TTL LS OCTAL LINE DRVR	01698	SN74LS241N
A3U21	1820-1199	1		IC-INV TTL HEX LS	02910	SN74LS04N
A3U22	1820-1197	9	1	IC-GATE TTL LS	02910	SN74LS00N
A3U23	1820-1112	8	2	IC-FF TTL LS	02910	SN74LS74AN
A3U24	1820-1918	2		IC-TTL LS OCTAL LINE DRVR	01698	SN74LS241N
A3U25	1820-1216	3		IC-DCDR TTL LS	02910	SN74LS138N
A3U26	1818-1306	7	1	IC-ROM USASCII FIXED SPACE	28480	1818-1306
A3U27	1818-1524	5	1	IC-ROM USASCII PROPORTIONAL SPACE	28480	1818-1524
A3U28	1820-2117	5	2	IC-TTL DUAL LINE DRVR	02237	9636ATC
A3U29	1820-1199	1		IC-INV TTL HEX LS	02910	SN74LS04N
A3U30	1820-1244	7	1	IC-DATA SEL TTL LS	01698	SN74LS153N
A3U31	1820-2096	9		IC-TTL LS DUAL BIN CNTR	01698	SN74LS393N
A3U32	1820-1208	3		IC-GATE OR TTL LS QUAD 2-IN	02910	SN74LS32N
A3U33,34	1820-1918	2		IC-TTL LS OCTAL LINE DRVR	01698	SN74LS241N
A3U35	1818-1309	0	1	IC-ROM LINE DRAW (OPTIONAL CHARACTER SET ROMs)	28480	1818-1309
A3U36	1818-1310	3	1	IC-ROM MATH SYMBOLS (OPTIONAL CHARACTER SET ROMs)	28480	1818-1310
A3U43	1818-1311	4	1	IC-ROM KATAKANA (OPTIONAL CHARACTER SET ROMs)	28480	1818-1311
	1818-1312	5	1	IC-ROM APL (OPTIONAL CHARACTER SET ROMs)	28480	1818-1312
A3U37	1820-2117	5		IC-TTL DUAL LINE DRVR	02237	9636ATC
A3U38	1820-0990	8		IC-DTL RCVR QUAD NAND	02037	MC1489AL
A3U39	1820-1918	2	1	IC-TTL LS OCTAL LINE DRVR	01698	SN74LS241N
A3U40	1820-1112	8		IC-FF TTL LS	02910	SN74LS74AN
A3U41	1820-2296	3	1	IC-PROG COM INTERFACE	03811	D8251A
A3U42	1820-1918	2		IC-TTL LS OCTAL LINE DRVR	01698	SN74LS241N
A3U44	1818-1308	9	1	IC-ROM ROMAN EXTENSIONS	28480	1818-1308
A3XU17,18,26,27,35, 36,43,44	1200-0541	1	8	SOCKET-IC 24 PIN DIP	02414	DIL824P-108
A3XU41	1200-0567	1	1	SOCKET-IC 28 PIN DIP	02414	DILB28P-108
	07310-60670	1	1	FRONT PANEL ASSY	28480	07310-60670

Table 4-2. Replaceable Parts, RS-232-C/CCITT V.24 Rear Panel, Option 050

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10	07310-60620	1	1	PCA-REAR PANEL RS-232-C	28480	07310-60620
A10C1	0160-3847	9	1	CAPACITOR-FIXED .01μF 50V CER	02798	CAC02X7R153M050A
A10C2	0180-0228	6	1	CAPACITOR-FIXED 22μF 15V TA	04200	150D226X9015B2-DYS
A10J1	1251-4946	5	1	CONNECTOR – 25 PIN F	04486	D8-25SV
A10S1,2	3101-1856	5	2	SWITCH – 8 DIP SLIDE	02484	11P-1434
A10S3	3101-0451	4	1	SWITCH – PUSHBUTTON SPST	02392	8631QCE
A10S4	3100-3446	1	1	SWITCH – ROTARY 8 POS. BCD	01380	1-435174-2
A10W1	07310-60120	6	1	CABLE ASSY	28480	07310-60120
	07310-00023	2	1	REAR PANEL RS-232-C/CCITT V.24	28480	07310-00023

Table 4-3. Replaceable Parts, RS-423-A Rear Panel, Option 051

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10	07310-60625	6	1	PCA-REAR PANEL RS-423-A	28480	07310-60625
A10C1	0160-3847	9	1	CAPACITOR-FIXED .01μF 50V CER	02798	CAC02X7R153M050A
A10C2	0180-0228	6	1	CAPACITOR-FIXED 22μF 15V TA	04200	150D226X901582-DYS
A10J1	1251-6074	4	1	CONNECTOR – 37 PIN F	04486	DC37SV
A10S1,2	3101-1856	5	2	SWITCH – 8 DIP SLIDE	02484	11P-1434
A10S3	3101-0451	4	1	SWITCH–PUSHBUTTON SPST	02392	8631QCE
A10S4	3100-3446	1	1	SWITCH–ROTARY 8 POS. BCD	01380	1-435174-2
A10W1	07310-60120	6	1	CABLE ASSY	28480	07310-60120
	07310-00036	7	1	REAR PANEL RS-423-A	28480	07310-00036

Table 4-4. Code List of Manufacturers

Mfr. No.	Manufacturer Name	Address	Zip Code
01380	Amp, Inc.	Harrisburg, PA	17105
01607	Allen-Bradley Co.	Milwaukee, WI	53204
01698	Texas Instruments Semiconductor Components Div.	Dallas, TX	75222
02037	Motorola Semiconductor Products	Phoenix, AZ	85008
02237	Fairchild Semiconductor Div.	Mountain View, CA	94042
02273	TRW Inc. Burlington Div.	Burlington, IA	52601
02312	Spectra-Strip Corp.	Garden Grove, CA	92642
02414	Burndy Corp.	Norwalk, CT	06852
02484	CTS Keene, Inc.	Paso Robles, CA	93446
02798	Corning Glass Works Components Div.	Raleigh,NC	27604
02910	Signetics Corp.	Sunnyvale, CA	94086
03811	Intel Corp.	Mountain View, CA	95051
04200	Sprague Electric Co.	N. Adams, MA	01247
04486	ITT Cannon Electric	Santa Ana, CA	92072
04990	Grayhill, Inc.	La Grange, IL	60525
28480	Hewlett-Packard Co.	Palo Alto, CA	94304

Table 4-5. Reference Designators and Abbreviations

REFERENCE DESIGNATIONS

A . . . . . assembly
B . . . . . fan; motor
C . . . . . capacitor
CR . . . . . diode; diode thyristor; varactor
DS . . . . . annunciator; signaling device (audible or visual); lamp; LED
E . . . . . miscellaneous electrical part
F . . . . . fuse
FL . . . . . filter
H . . . . . hardware
J . . . . electrical connector (stationary portion); jack
K . . . . . relay
L . . . . . coil; inductor
M . . . . . meter
MP . . . . . miscellaneous mechanical part
P . . . . electrical connector (movable portion); plug
Q . . . . . transistor; SCR; triode thyristor
R . . . . . resistor
RN . . . . . resistor network
S . . . . . switch
T . . . . . transformer
TB . . . . . terminal board
TP . . . . . test point
U . . . . . integrated circuit; microcircuit
VR . . . . breakdown diode; voltage regulator
W . . . . . cable; transmission path; wire
X . . . . . socket
Y . . . . . crystal unit (piezoelectric or quarts)

ABBREVIATIONS

A . . . . . ampere
ac . . . . alternating current
ADJ . . . . . adjustment
A/D . . . . analog-to-digital
AL . . . . . aluminum
AMPL . . . . . amplifier
ASSY . . . . . assembly
AUX . . . . . auxiliary
avg . . . . . average
AWG . . . . . American wire gauge
BAL . . . . . balance
BCD . . . . . binary coded decimal
BKDN . . . . . breakdown
CAL . . . . . calibrate
ccw . . . . counter-clockwise
CER . . . . . CERAMIC
CHAN . . . . . channel
cm . . . . . centimetre
COAX . . . . . coaxial
COEF . . . . . coefficient
COM . . . . . common
COMP . . . . . composition
CONN . . . . . connector
COS . . . . . cosine
CP . . . . . cadmium plate
cw . . . . . clockwise
D/A . . . . digital-to-analog
dc . . . . . direct current
deg . . degree (temperature interval or difference)
. . .°. . . degree (plane angle)
°C . . . . . degree Celsius (centigrade)
°F . . . . degree Fahrenheit
DET . . . . . detector
diam . . . . . diameter
DIA . . . . . diameter (used in parts list)
DIFF AMPL . . differential amplifier
div . . . . . division
DPDT . . . . . double-pole, double-throw
DR . . . . . drive
DTL . . . . diode transistor logic
DVM . . . . digital voltmeter
ECL . . . . emitter coupled logic
ELECT . . . . . electrolytic
EN . . . . . enable
ENCAP . . . . encapsulated
EXT . . . . . external
F . . . . . farad
FET . . . . . field-effect transistor
F/F . . . . . flip-flop
FH . . . . . flat-head
FIL H . . . . . fillister head
FP . . . . . front panel
FREQ . . . . . frequency
FXD . . . . . fixed
g . . . . . gram
GE . . . . . germanium
GHz . . . . . gigahertz
GL . . . . . glass
GRD . . . . . ground(ed)
H . . . . . henry
h . . . . . hour
HEX . . . . . hexagonal
HD . . . . . head
HDW . . . . . hardware
HP . . . . . Hewlett-Packard
HPF . . . . . high pass filter
HR . . . . . hour (used in parts list)
HV . . . . . high voltage
Hz . . . . . Hertz
IC . . . . integrated circuit
ID . . . . . inside diameter
IMPG . . . . . impregnated
in . . . . . inch
INCL . . . . . include(s)
INP . . . . . input
INS . . . . . insulation
INT . . . . . internal
I/O . . . . . input/output
kg . . . . . kilogram
kHz . . . . . kilohertz
kΩ . . . . . kilohm
kV . . . . . kilovolt
lb . . . . . pound
LC . . . . . inductance-capacitance
LED . . . . . light-emitting diode
LG . . . . . long
LH . . . . . left hand
LIM . . . . . limit
LIN . . . . . linear taper (used in parts list)
lin . . . . . linear
LK WASH . . . lock washer
LOG . . . logarithmic taper (used in parts list)
log . . . . . logrithm(ic)
LPF . . . . . low pass filter
LSB . . least significant bit
LV . . . . . low voltage
m . . . . . metre (distance)
mA . . . . . milliampere
MAX . . . . . maximum
mΩ . . . . . megohm
MEG . . . . . meg (10^6) (used in parts list)
MET FLM . . . . metal film
MET OX . . . metallic oxide
MFR . . . . . manufacturer
mg . . . . . milligram
MHz . . . . . megahertz
mH . . . . . millihenry
MIN . . . . . minimum
min . . . . . minute (time)
. . .′. . . minute (plane angle)
MINAT . . . . . miniature
mm . . . . . millimetre
MOM . . . . . momentary
MOS . . . . . metal-oxide semiconductor
ms . . . . . millisecond
MSB . . most significant bit
MTG . . . . . mounting
mV . . . . . millivolt
mVac . . . . . millivolt, ac
mVdc . . . . . millivolt, dc
mVpk . . . . millivolt, peak
mVp-p . . . . . millivolt, peak-to-peak
mVrms . . . . millivolt, rms
mW . . . . . milliwatt
MUX . . . . . multiplex
MY . . . . . mylar
μA . . . . . microampere
μF . . . . . microfarad
μH . . . . . microhenry
μs . . . . . microsecond
μV . . . . . microvolt
μVac . . . . . microvolt, ac
μVdc . . . . . microvolt, dc
μVpk . . . . microvolt, peak
μVp-p . . . . . microvolt, peak-to-peak
μVrms . . . . microvolt, rms
μW . . . . . microwatt
NC . . . . . no connection
N/C . . . . normally closed
NEG . . . . . negative
NI PL . . . . . nickel plate
N/O . . . . . normally open
NOM . . . . . nominal
NORM . . . . . normal
NPN . . . negative-positive-negative
NPO . . . negative-positive-zero (zero temperature coefficient)
NRFR . . not recommended for field replacement
NSR . . . . . not separately replaceable
ns . . . . . nanosecond
OBD . order by description
OD . . . . outside diameter
OH . . . . . oval head
OP AMPL . . . . operational amplifier
OPT . . . . . option
OSC . . . . . oscillator

NOTE

All abbreviations in the parts list will be in uppercase.

Table 4-5. Reference Designators and Abbreviations (Continued)

OX . . . . . oxide
oz . . . . . ounce
Ω . . . . . ohm
P . . . . . peak (used in parts list)
PC . . . . . printed circuit
PCA . . . . . printed circuit assembly
pF . . . . . picofarad
PIV . . . peak inverse voltage
pk . . . . . peak
PNP . . . positive-negative-positive
P/O . . . . . part of
POLY . . . . . polystyrene
PORC . . . . . porcelain
POS . . positive; position(s) (used in parts list)
POSN . . . . . position
POT . . . . . potentiometer
POZI . . . . . pozidriv
p-p . . . . . peak-to-peak
PP . . . . . peak-to-peak (used in parts list)
PWR . . . . . power
PWV . peak working voltage
RAM . . . . . random access memory
RC . . . . . resistance-capacitance
RECT . . . . . rectifier
REF . . . . . reference
REG . . . . . regulated
REPL . . . . . replaceable
RF . . . . . radio frequency
RFI . . . . radio frequency interference
RH . . . . . round head; right hand
RLC . . . . . resistance-inductance-capacitance
rms . . . . root-mean-square
RND . . . . . round
ROM . . read-only memory
RWV . . . . reverse working voltage
s . . . . . second (time)
. . . " . second (plane angle)
S-B . . . . . slow-blow (fuse) (used in parts list)
SCR . . . silicon controlled rectifier; screw
SE . . . . . selenium
SECT . . . . . sections
SEMICON . . semiconductor
SI . . . . . silicon
SIN . . . . . sine
SPDT . . . . . single-pole, double-throw
SPG . . . . . spring
SR . . . . . split ring
SPST . . . . . single-pole, single-throw
SST . . . . . stainless steel
STL . . . . . steel
SQ . . . . . square
SYNC . . . . . synchronize
T . . timed (slow-blow fuse)
TA . . . . . tantalum
TC . . . . . temperature compensating
TERM . . . . . terminal
TFT . . thin-film transistor
TGL . . . . . toggle
THD . . . . . thread
THRU . . . . . through
TI . . . . . titanium
TOL tolerance
TSTR . . . . . transistor
TTL . . . . . transistor-transistor logic
U . . . . . micro (10^{-6}) (used in parts list)
UF . . . . . microfard (used in parts list)
UNREG . . . . unregulated
V . . . . . volt
VA . . . . . voltampere
Vac . . . . . volts, ac
VAR . . . . . variable
Vdc . . . . . volts, dc
VDCW . . volts, dc, working (used in parts list)
Vpk . . . . . volts, peak
Vp-p . . volts, peak-to-peak
Vrms . . . . . volts, rms
W . . . . . watt
W/ . . . . . with
WIV . . . . working inverse voltage
WW . . . . . wirewound
W/O . . . . . without
Z_o . . . . . character impedance

NOTE

All abbreviations in the parts list will be in uppercase.

MULTIPLIERS

Abbreviation	Prefix	Multiple
G	giga	10^9
M	mega	10^6
k	kilo	10^3
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

SECTION V

MANUAL CHANGES

This section is reserved for information which adapts the manual to earlier instruments. No such information applies to this manual supplement.

SECTION VI

SERVICE

6-1. INTRODUCTION.

6-2. This section contains information needed for repair of the Option 050 and 051 circuits, including:

Theory of Operation
Character Set Selection
Parts Removal and Replacement
Troubleshooting
Functional Block Diagram
Schematic Diagrams
Component Location Figures

6-3. Service information in this supplement may refer to service information in the 7310A Service Manual, HP Part No. 07310-90000.

6-4. Each connection between the Serial I/O schematic in this supplement and the schematic diagrams in the 7310A Service Manual is identified by a signal connection letter. In addition, a number indicates the service sheet of the origin or destination of the signal connection.

6-5. THEORY OF OPERATION.

6-6. Figure 6-11 is a Functional Block Diagram of the Serial I/O circuits. This diagram replaces the HP-IB portion of the Functional Block Diagram of the standard printer on Service Sheet 1 in the 7310A Service Manual.

6-7. This explanation of circuit operation basically follows the block diagram. More detailed drawings of some circuits are provided with the text. Refer also to the schematic diagram.

6-8. Options 050 and 051 are both asynchronous bit-serial interfaces for hardwired connection to a remote computer system or terminal. Option 050 is compatible with EIA Standard RS-232-C and CCITT V.24 Option 051 is compatible with RS-423-A.

6-9. Timing for the interface operation is provided by an internal Baud Rate Generator or by an External Clock signal. The rear panel INTERNAL/EXT CLK must be set to the position corresponding to the timing method to be used. The external clock frequency must be 16 times the desired baud rate, and the clock input circuit is TTL compatible.

6-10. INTERNAL/EXTERNAL CLOCK SELECTION

6-11. A diagram of the Internal/External Clock Selection circuit is shown in Figure 6-1. In normal operation, the use of either Internal or External Clock is determined by the setting of the rear panel INTERNAL/EXT CLK switch. U22 is connected in a 2-input multiplexer configuration.

6-12. When the switch is set to the EXT CLK position, U22D is enabled and U22A is disabled. Consequently, the External Clock input is gated through U22B. With the switch in the Internal position, U22A is enabled and U22D is disabled, allowing the INT CLK signal from the Baud Rate Generator to be gated through U22B. The selected baud rate clock signal is synchronized to the 4MHz clock by U23 before being supplied to the UART.

6-13. When a Confidence Test is performed, the TEST signal to U14 is high, disabling U22D and enabling U22A. Consequently, the INT CLK signal is used for the Confidence Test regardless of the position of the rear panel INTERNAL/EXT CLK switch.

6-14. The baud rate clock signal (either external or internal) to the UART must be 16 times the desired baud rate. The internal clock frequencies are provided by the Baud Rate Generator.

6-15. BAUD RATE GENERATOR

6-16. A diagram of the Baud Rate Generator circuits is shown in Figure 6-2. The 4MHz clock signal from the Main Processor PCA, A1, is divided by U13, U2, and U12 to provide frequencies that are approximately 16 times the standard baud rate frequencies marked on the rear panel. These signals are multiplexed in U8, and the desired frequency is selected by the three Baud Rate selection lines (BR1, BR2, BR4) from the rear panel BAUD RATE switch. Schmitt Trigger buffering is used in the baud rate selection lines to provide noise immunity.

6-17. STANDBY CIRCUIT

6-18. Printers with Option 050 or 051 can be placed in the Standby mode by pressing the front panel STBY control. In Standby mode, printing is stopped and the front panel STBY light is on. Pressing the STBY the second time returns the printer to the On Line mode.

6-19. Figure 6-3 is a diagram of the standby switch circuits. Some elimination of switch bounce is provided by an RC network and a Schmitt trigger buffer. To make sure "multiple standby" does not occur, the switch buffer output is sampled only once every 53.2ms. A 1202Hz signal from the Baud Rate Generator is divided by 64 to provide

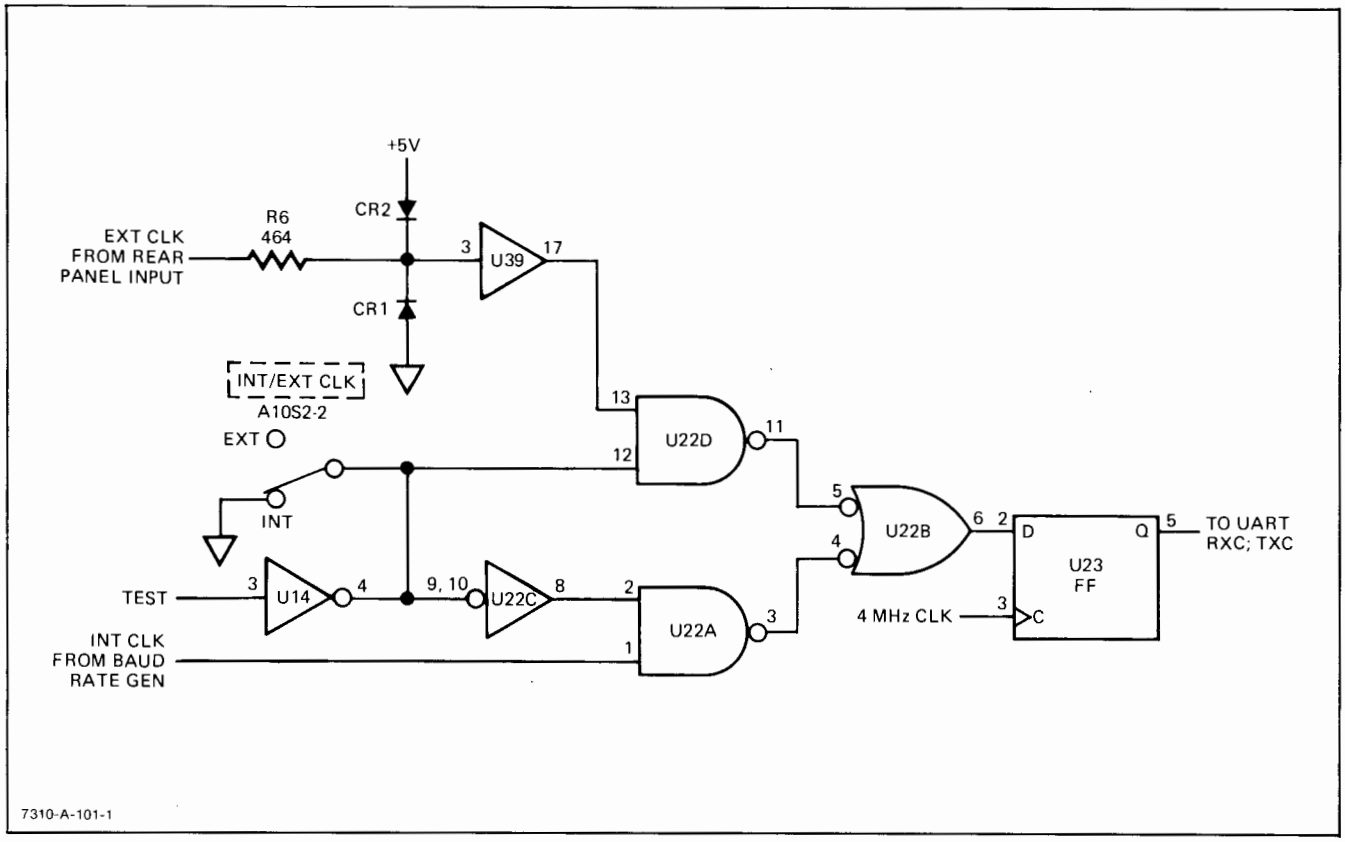


Figure 6-1. Internal/External Clock Selection

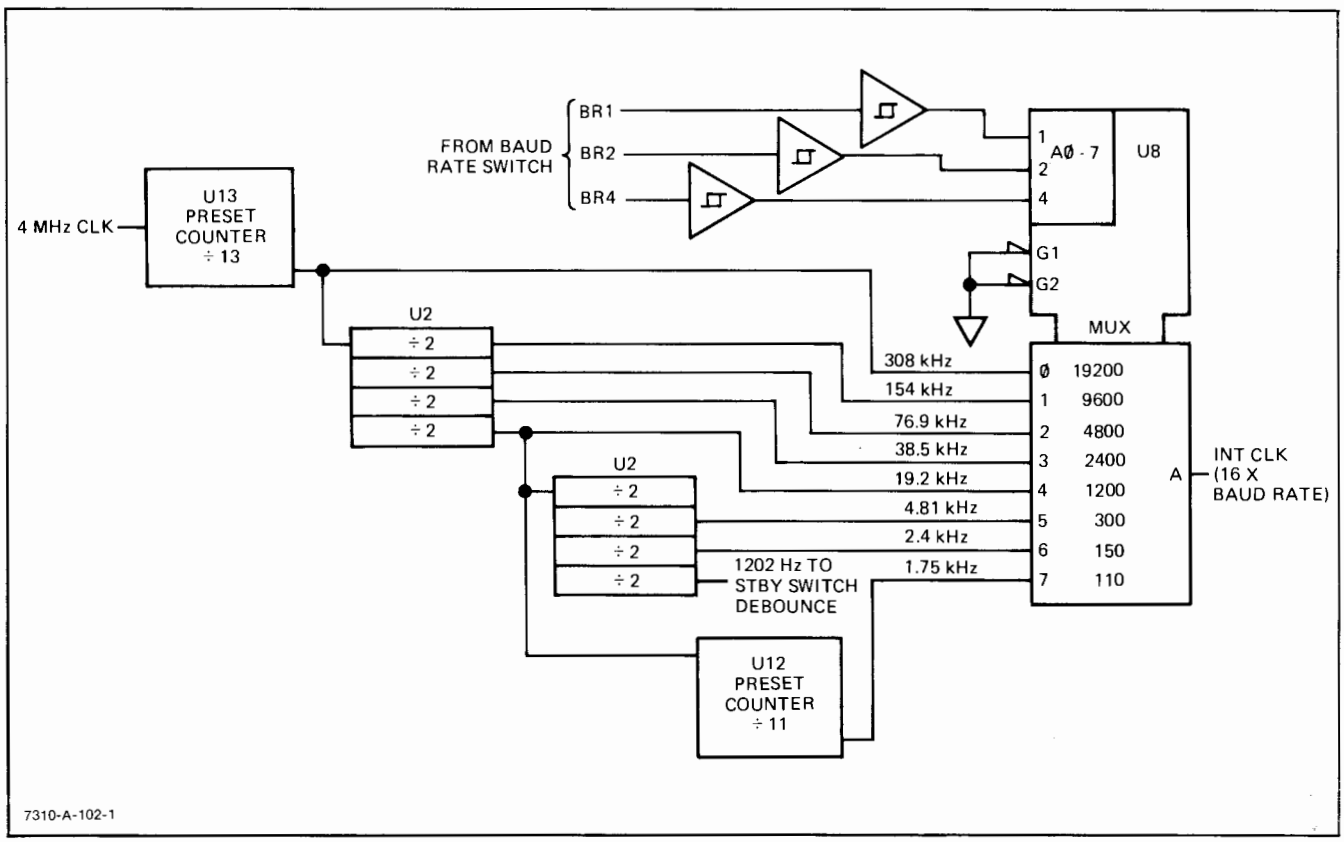


Figure 6-2. Baud Rate Generator

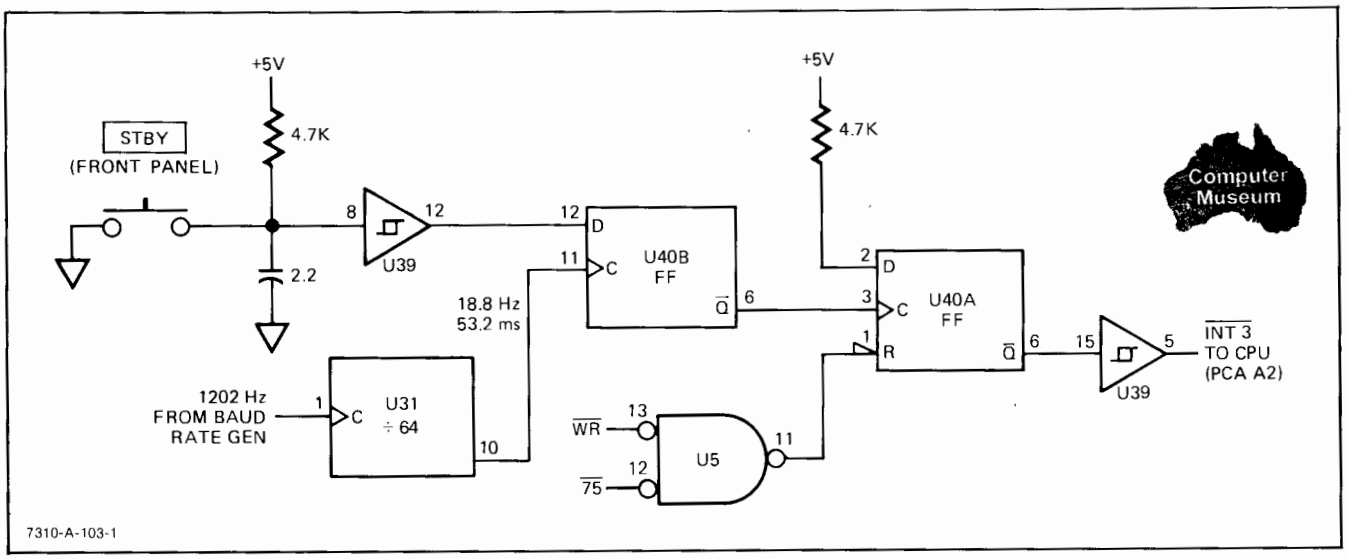


Figure 6-3. Standby Switch Debounce Circuit

the 18.8Hz (53.2ms) sample clock to the D flip-flop sampling circuit, U40B. The output of U40B clocks the high D input into U40A. The Q output of U40A becomes an interrupt signal to the CPU on I/O Processor PCA, A2.

6-20. The $\overline{INT3}$ status is assigned to Standby to insure a fast response, since this is the highest priority interrupt used in the printer. INT3 remains low until acknowledged by the CPU, which then clears the latch by sending $\overline{WR}$ and $\overline{PORT\ 75}$ through AND gate U5.

6-21. DATA INPUT AND OUTPUT CIRCUITS

6-22. The Serial I/O PCA circuits are designed for use with either RS-232-C/CCITT V.24 or RS-423-A systems. Because signals and data within the 7310A are positive-true TTL levels, inverting amplifiers are used in the input and output circuits to convert the logic and voltage levels. Both the RS-232-C and RS-423-A systems use negative-true logic at the levels shown in Table 2-1.

6-23. The Clear To Send (CTS), Received Data (Input), and Transmitted Data (Output) circuits are shown in Figure 6-4. Also shown is the Multiplexer, U30, which selects the RS-232-C or RS-423-A inputs, and the normal or Confidence Test data paths. The table in Figure 6-4 shows that in normal operation, the lower section of the multiplexer is used to select received data. In test operation, the transmitted data is returned through the multiplexer to the Received Data (RXD) input to the UART. This data is compared to the sent data to determine if circuit operation is correct. The Confidence Test does not check the gate, U32, and the output amplifier, U28, nor does it check the receiver amplifiers, U1 and U38. During a test operation, gate U32 is disabled so the test data is not transmitted.

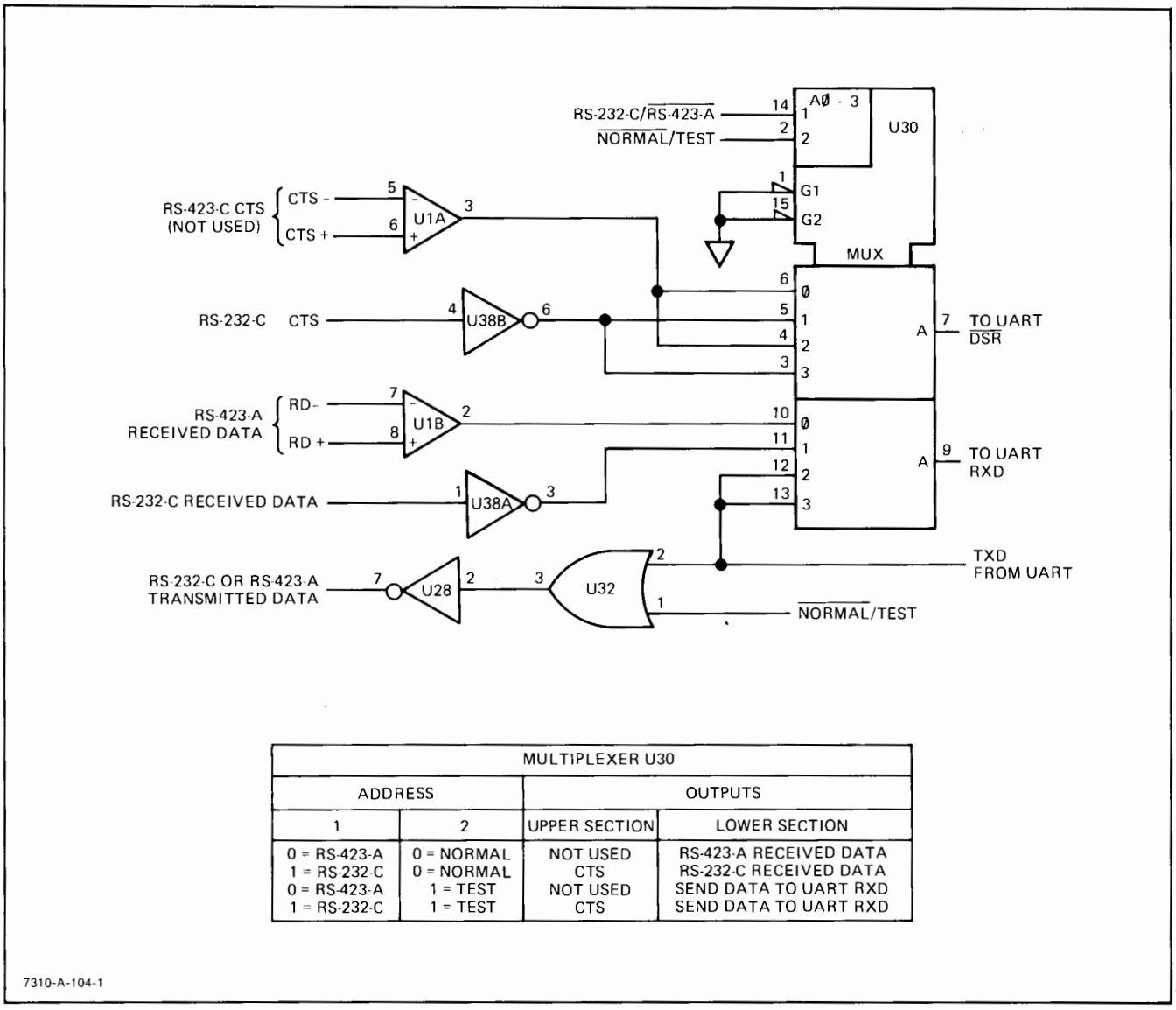
6-24. UNIVERSAL ASYNCHRONOUS RECEIVER/ TRANSMITTER

6-25. The 8251A interface IC used in the Serial I/O is capable of both synchronous and asynchronous operation. However, in the 7310A it is used only for asynchronous operation; therefore, in this manual it is referred to as a Universal Asynchronous Receiver/Transmitter, or UART. It receives data characters from the Z80 CPU (on the I/O Processor PCA) in parallel form and converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. Most of the UART functions such as number of stop bits, parity selection, and character length are externally programmable. Table 6-1 describes the UART input and output lines, which are shown on the fold-out schematic diagram.

6-26. Timing circuits for the Read, Write, and Chip Select signals to the UART are shown in Figure 6-5. The Port $\overline{70}$-$\overline{77}$ signal is gated with Address Bit 0 or 1 to produce a $\overline{70}$ or $\overline{71}$ Chip Select signal to the UART. The trailing edge of this signal is extended slightly by U23, which is clocked by the 2MHz clock signal. The $\overline{RD}$ and $\overline{WR}$ signals are gated with the $\overline{CSD}$ signal to make sure $\overline{CS}$ to the UART is low before $\overline{RD}$ or $\overline{WR}$ goes low.

6-27. INPUT/OUTPUT ROMs

6-28. Two Read Only Memory (ROM) ICs contain the fixed routines for handling the exchange of information between the Serial I/O (RS-232-C or RS-423-A) and the 7310A, as well as the exchange between the Serial I/O PCA and the I/O Processor. I/O ROM Chip Select signals ($\overline{CS4}$-$\overline{CS5}$) are received from the I/O Processor PCA.



MULTIPLEXER U30			
ADDRESS		OUTPUTS	
1	2	UPPER SECTION	LOWER SECTION
0 = RS-423-A 1 = RS-232-C 0 = RS-423-A 1 = RS-232-C	0 = NORMAL 0 = NORMAL 1 = TEST 1 = TEST	NOT USED CTS NOT USED CTS	RS-423-A RECEIVED DATA RS-232-C RECEIVED DATA SEND DATA TO UART RXD SEND DATA TO UART RXD

Figure 6-4. Input and Output Circuits

6-29. CHARACTER SET ROMs.

6-30. The Character Set ROMs contain the information required for printing text. The number and type of Character Set ROMs present in any 7310A is related to the language capabilities ordered. The chip select signals for these ROMs are decoded on the Serial I/O PCA from Address Bits AB11-15 furnished by the I/O Processor. Information for replacing Character Set ROMs is provided in Section VI of the 7310A Service Manual, supplemented by location and designator information later in this section.

6-31. ROM BUFFERS.

6-32. The I/O and Character Set ROM outputs go through buffers to the Data Bus. The buffer IC is enabled when the chip select input to any ROM is active and the Read signal from the I/O Processor is active. When the buffer IC is not enabled, its outputs are 3-state.

6-33. CHARACTER SET SWITCHES.

6-34. The default primary and secondary sets are designated by the setting of switches S1 and S2 on the Serial I/O PCA. The selection procedure is given in Section VI of the 7310A Service Manual, supplemented by location and designator information later in this section. Four sections in S1 are the Qualifier (Q) switches, and five sections in S2 are the Identifier (ID) switches. The Identifier is a five-digit binary number corresponding to a letter of the alphabet which is the initial letter of the language selected. The Q parameter selects a particular language from the available languages in the identified group. For example, the Identifier "S" could be Swedish-Finish, Spanish, or Swiss. The Q parameter "O" selects Swedish-Finish, and "1" selects Spanish, etc.

Table 6-1. UART Input and Output Connections

Pin No.	Signal	Description
1,2,5-8,27,28	D0-7	Parallel data bus in or out of the UART. Either a data character or a control word.
12	C/$\overline{D}$	Control / $\overline{\text{Data}}$. Informs the UART that the word on the data bus is.a data character or a control word.
11	$\overline{CS}$	$\overline{\text{Chip Select}}$. Enables the UART to rear or write information,
13	$\overline{RD}$	$\overline{\text{Read}}$. Processor reads data or command from the UART.
10	$\overline{WR}$	$\overline{\text{Write}}$. Processor writes data or command to the UART.
14	RXRDY	Active when UART has received a serial character which is ready to be input to the CPU. In this printer, causes $\overline{INT2}$ to the CPU.
3	RXD	Receiver Data. Input for serial data from external system.
17	$\overline{CTS}$	$\overline{\text{Clear to Send}}$. In the 7310A this input is held low, indicating that it is always clear to send data.
22	$\overline{DSR}$	$\overline{\text{Data Set Ready}}$. Functions as the CTS line from an RS-232-C system. CTS (DSR) is not used in an RS-423-A system.
19	TXD	Transmitter Data. Output for serial data to external system.
24	$\overline{DTR}$	$\overline{\text{Data Terminal Ready}}$. Handshake line to external system. State can be set under program control.
23	$\overline{RTS}$	$\overline{\text{Request to Send}}$. Drives Secondary Request to Send (SCA) handshake line. External RTS line is always active in 7310A.
20	CLK	2MHz Clock for internal UART timing.
9	TXC	Transmitter Clock. } Transmitter and Receiver Baud Rate Clock Input. 16 times the baud rate.
25	RXC	Receiver Clock. }
21	Reset	Inverted Power On Reset from Main Processor PCA, A1.

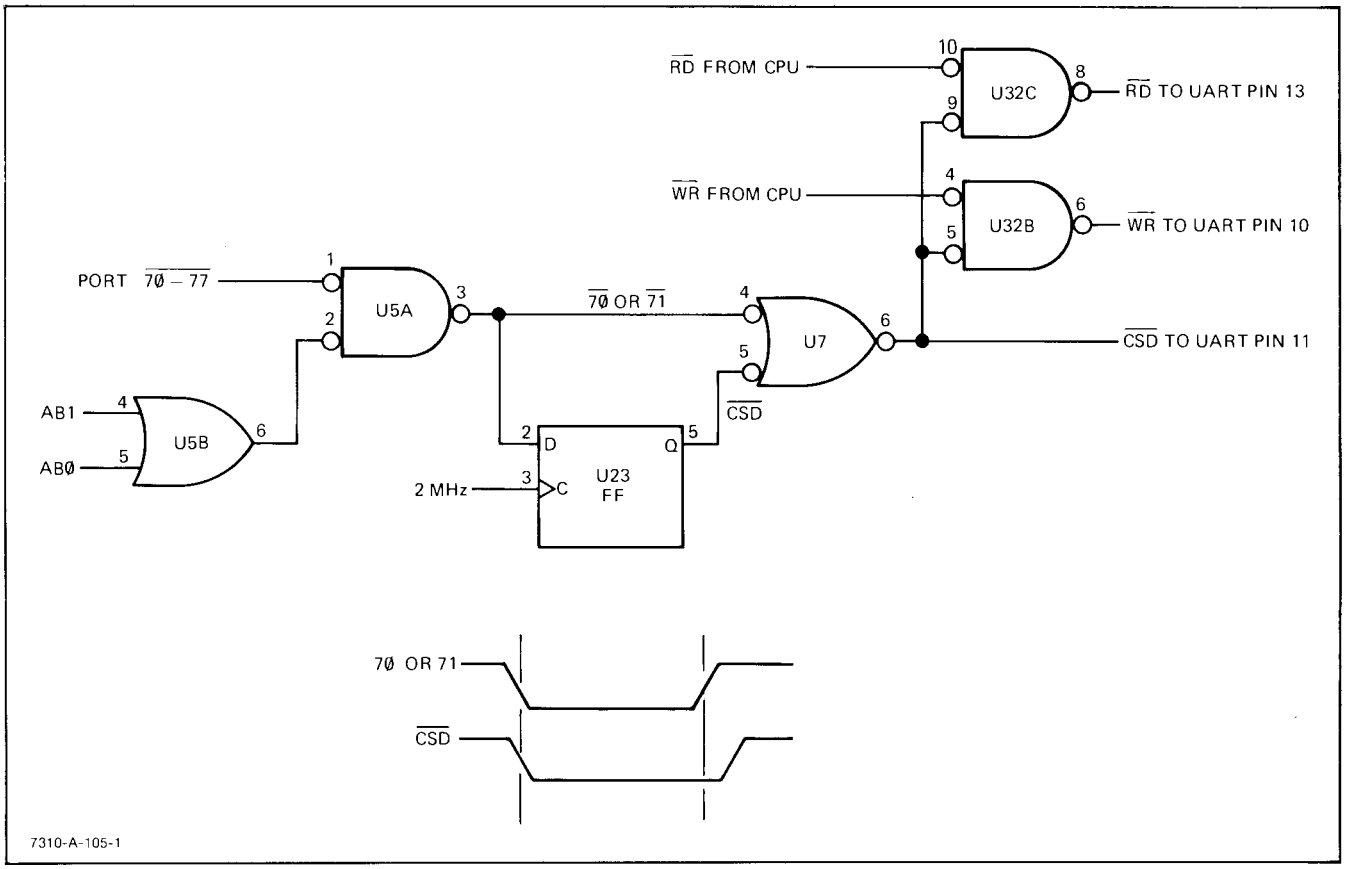


Figure 6-5. UART Chip Select and Read/Write Timing

6-35. SWITCH BUFFERS.

6-36. Outputs from the Character Set switches and the rear panel Function and Interface switches are buffered by A3U10, 19, 20, and 29 (see Block Diagram and Schematic Diagram). The outputs from these buffers are bussed together into another buffer, A3U33, and from there enter the Data Bus, DB0-7. Decoded Port signals are used to enable each of the four switch buffers, and the fifth buffer (U33) is enabled when any of the other buffers is enabled and the Read ($\overline{RD}$) line is active. Port signals $\overline{7D}$, $\overline{7E}$, and $\overline{7F}$ from the I/O Processor PCA are used to enable three of the buffers. The Port $\overline{70}$-$\overline{77}$ signal, also from the I/O Processor, is broken down by Address Bits 0-2 into Port $\overline{74}$, $\overline{75}$, etc., to enable other ICs. This is done by A3U4, 8 and 32.

6-37. OPENING THE PRINTER.

6-38. To open the printer, proceed as follows:

WARNING

The following service procedures should be performed only by service-trained personnel who are aware of the electrical shock hazards involved.

a. Set the LINE switch to OFF and disconnect the ac line cord.

b. Remove the screws in the rear panel indicated in Figure 6-6.

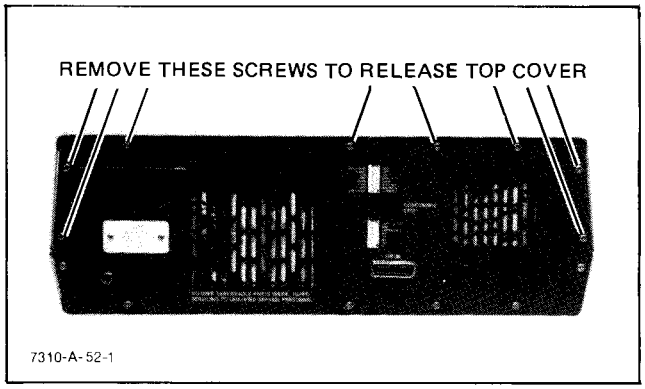
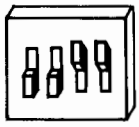


Figure 6-6. Opening the Printer

c. Lift the rear edge of the top cover about five centimetres (two inches) and slide the cover forward slightly to release from the bottom cover.

NOTE

Before replacing the top cover, make sure the test switches near the top center of A1 are set as shown below. When replacing the cover, be careful not to change the switch setting.



d. When replacing the top cover, make sure that the front edge of the top cover is inserted under the lip on the bottom cover.

6-39. CHARACTER SET DESIGNATION AND SELECTION.

6-40. Either Option 050 or 051 contains the same standard character sets as the standard Model 7310A, and is capable of accepting the same optional sets. Consequently, the Character Set Designation and Selection information in the 7310A Service Manual applies to both Option 050 and 051. The only differences are the ROM designators and the physical locations of the PCA. The ROM slot locations and designators are listed in Table 6-2. The Confidence Test prints the location code for each character set installed. For physical location, refer to the component location figure accompanying the schematic diagram. The standard sets are USASCII fixed space (U26), USASCII proportional space (U27), and Roman Extension (U44). These ROMs should always be in the same location in either Option 050 or 051. Table 6-3 shows the correct locations for optional Character Set ROMs.

Table 6-2. Character Set Location

A3S1 CBA	Location Code	Physical Location on Serial I/O PCA
000	@/@'	U26, U27
001	A	U35
010	B	U36
011	C	U43
100	D	U44

6-41. PARTS REMOVAL AND REPLACEMENT.

6-42. To remove and replace the Serial I/O PCA, A3, and the Rear Panel Assembly, A10, for either Option 050 or 051, use the procedures in the 7310A Service Manual for A3 and A10.

6-43. TROUBLESHOOTING.

6-44. DIAGRAMS.

6-45. A functional Block Diagram and a Schematic Diagram of the Serial I/O Circuits are on fold-out pages at the rear of this manual. The Block Diagram includes only the Option 050/051 Serial I/O circuit blocks and replaces the HP-IB I/O circuits included in the Functional Block Diagram in the 7310A Service Manual. The RS-232-C Rear Panel PCA is shown on the last fold-out page with the Serial I/O PCA. The RS-423-A Rear Panel PCA is shown on the preceding fold-out page, which may be folded out to cover the RS-232-C portion of the complete schematic.

6-46. TEST EQUIPMENT REQUIRED.

6-47. Test equipment needed to service the Serial I/O circuits is included in the table of Recommended Test Equipment in Section I of the 7310A Service Manual.

6-48. RECOMMENDED METHOD OF REPAIR.

6-49. Because of the complexity of the digital and logic circuits, repair by printed circuit assembly (PCA) replacement is recommended if at all possible. PCA substitution may also be used for troubleshooting in some cases.

6-50. CONFIDENCE TEST RESULTS.

6-51. The Confidence Test flow chart for Options 050 and 051 is shown in Figure 6-7. Certain failures in the Serial I/O PCA circuits (A3) may be indicated by the Confidence Test printout. For example, a five-dot code at the top of the test indicates that the circuits failed to complete the test within a set time limit. A six-dot code indicates that the "received" test data did not match the "transmitted" data. Each ROM check sum at the top of the test must end in "FF". (Check sums are four-digit hexadecimal numbers.) Any other character in the last two digits indicates a probable failure in the ROM. Figure 6-8 shows a Confidence Test indicating a failure on the Serial I/O PCA.

6-52. SERIAL I/O TROUBLESHOOTING (A3).

6-52. The 4MHz clock signal input to A3 may be checked at U39 pins 4 and 16. The 4MHz clock is the input to the Baud Rate Generator.

6-54. The 2MHz clock signal input to A3 may be checked at U39 pins 13 and 7. The 2MHz clock is the UART clock signal.

6-55. The $\overline{\text{Reset}}$ signal is used only to reset the UART at power turn-on. It may be checked at U39 pins 2 and 18, and U29 pins 5 and 6.

Table 6-3. Optional Character Set ROM Locations

Option	Character Set	Q/ID Code	ROM HP Part No.	Slot Location		
				A(U35)	B(U36)	C(U43)
008	Katakana	1K	1818-1311 (T-54853)	*		
010	Math Symbols	ØM	1818-1310 (T-54852)			*
011	Line Draw	ØL	1818-1309 (T-54851)		*	
009	APL	ØP	1818-1312 (T-54854)	*		
010	Math Symbols	ØM	1818-1310 (T-54852)			*
011	Line Draw	ØL	1818-1309 (T-54851)			*
010	Math Symbols	ØM	1818-1310 (T-54852)	*		
011	Line Draw	ØL	1818-1309 (T-54851)		*	

6-56. Figure 6-2 shows the approximate frequencies that should be present at various points within the Baud Rate Generator. These frequencies may be checked with an oscilloscope or an electronic counter.

6-57. The INT3 signal at U40 pin 6 can be observed (on an oscilloscope or with a logic probe) when the front panel STBY control is pressed.

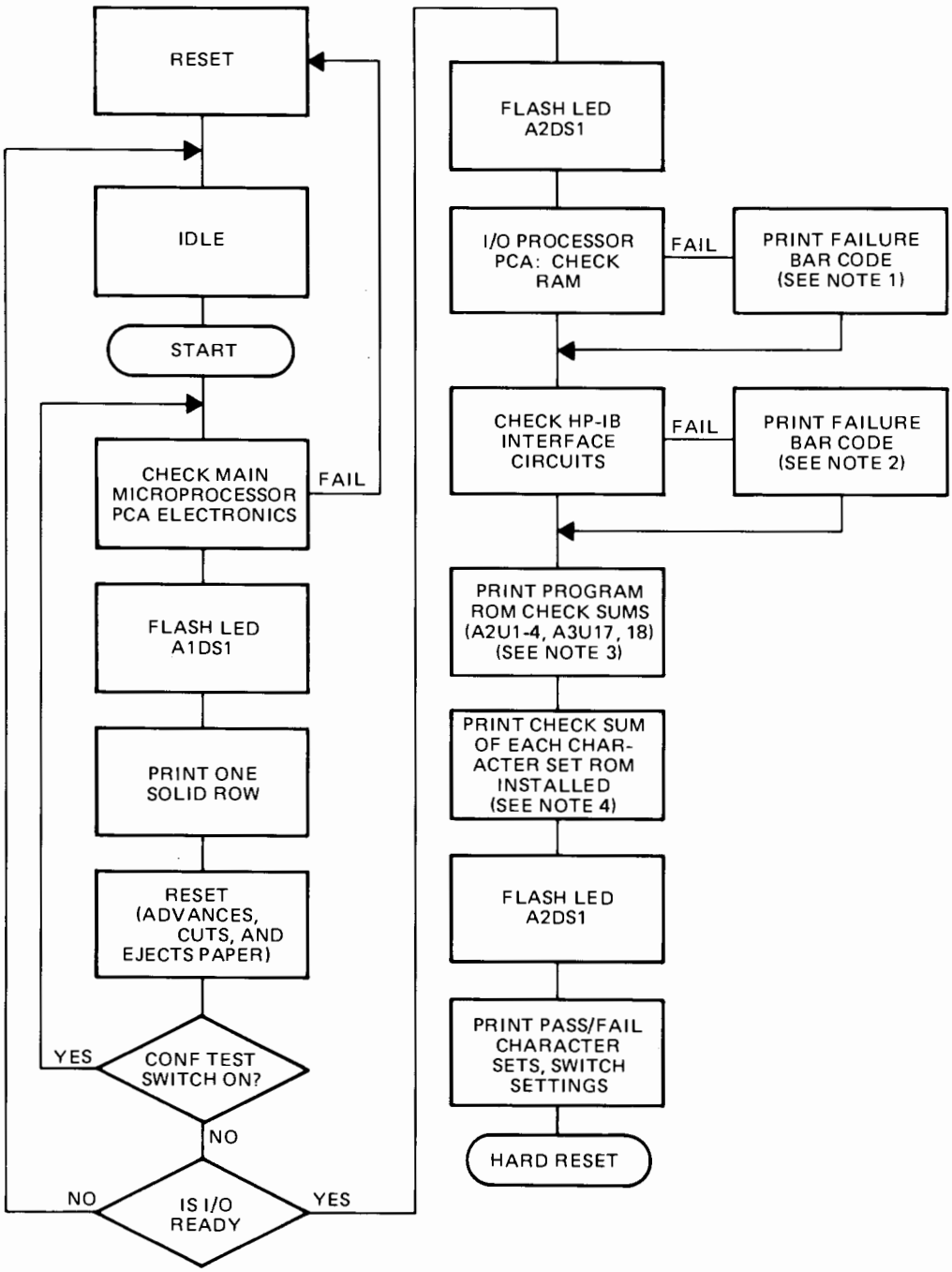
6-58. A logic probe may be used to determine the presence of various chip select, enable, read, and write signals.

6-59. SCHEMATIC NOTES.

6-60. Symbols and notations commonly used on schematic diagrams are shown in Figure 6-9.

6-61. LOGIC SYMBOLS.

6-62. Logic symbols for integrated circuits used in Options 050 and 051 are shown in Figure 6-10.



NOTES:

1. ONE DOT INDICATES A RAM FAILURE (A2U6,8).
2. PRINTOUT OF FIVE DOTS INDICATES A FAILURE OF THE SERIAL INTERFACE CIRCUITS TO COMPLETE THE TEST WITHIN A SET TIME LIMIT. PRINTOUT OF SIX DOTS INDICATES A TEST DATA SEND/RECEIVE ERROR.
3. PRINTOUT IS HEXADECIMAL SUM OF ALL PROGRAM ROMS PLUS FIVE, THEN CHECK SUM OF EACH ROM. LAST TWO DIGITS OF EACH SUM MUST BE FF.
4. LAST TWO DIGITS OF EACH HEXADECIMAL SUM MUST BE FF. PRINTOUT FOLLOWS THE SEQUENCE: U29, U30, U33, U34, U35, U19. PRINTOUT INCLUDES ONLY THOSE ROM LOCATIONS WITH ROMS INSTALLED (NOTHING IS PRINTED FOR A VACANT ROM LOCATION). FOR EXAMPLE, THE STANDARD CHARACTER ROM COMPLEMENT INCLUDES ONLY U29, U30 AND U19.

7310-A-106-1

Figure 6-7. Confidence Test Flow Chart

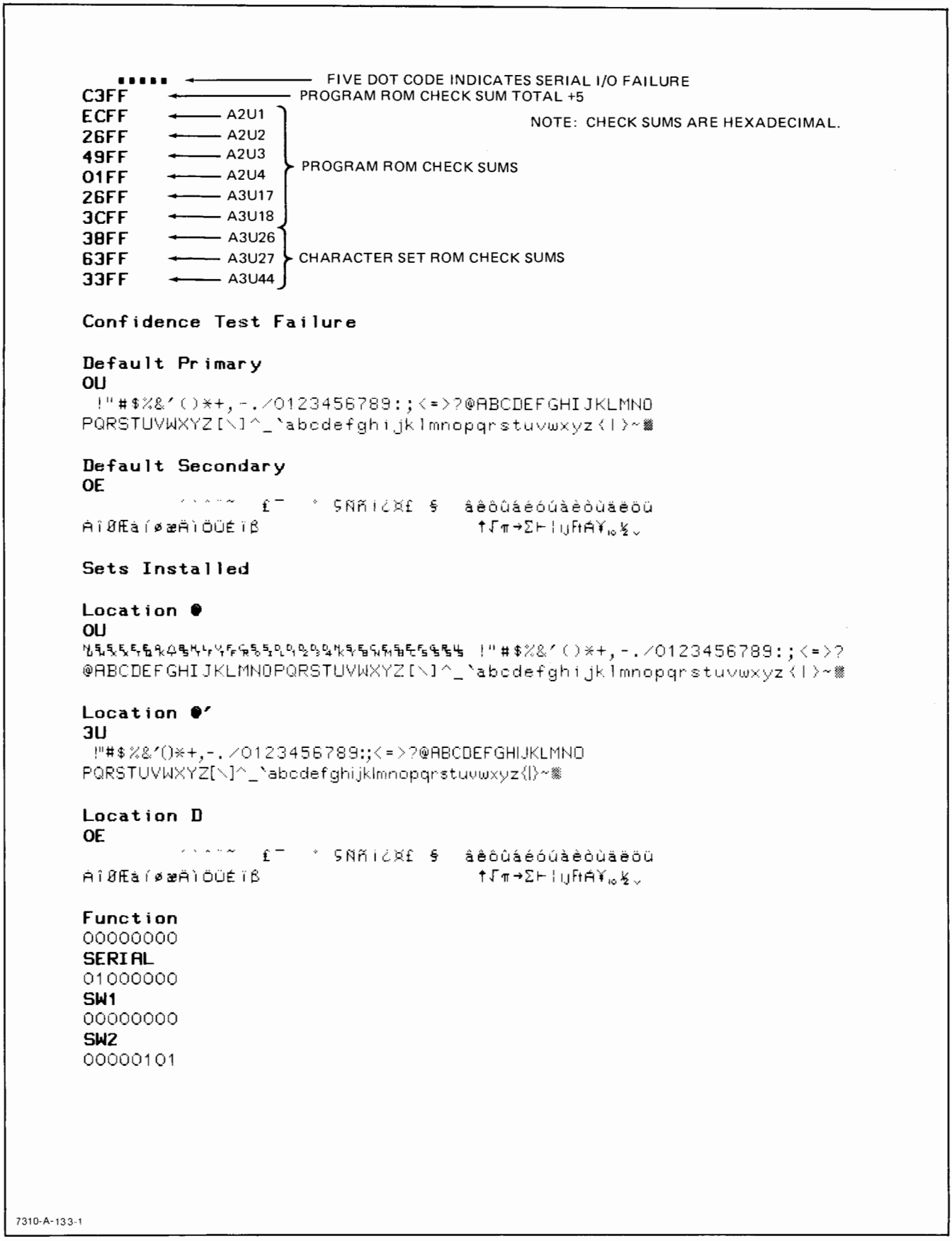


Figure 6-8. Confidence Test Failure

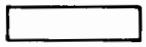
SCHEMATIC DIAGRAM NOTES

Resistance in ohms, capacitance in microfarads, inductance in millihenries unless otherwise noted.

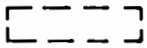
Indicates a NOTE on the schematic diagram.

Tool-aided adjustment.

Manual control.



Encloses a front-panel or circuit assembly silkscreened designator.

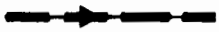


Encloses a rear-panel silkscreened designator.

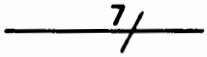
Circuit assembly borderline.

Other assembly borderline. Also used to indicate mechanical interconnection (ganging) and RF shielding.

Heavy line with arrows indicates path and direction of main signal.



Heavy dashed line with arrows indicates path and direction of main feedback.



Indicates cable run with seven lines.

Wiper moves toward CW with clockwise rotation of control (as viewed from shaft or knob).

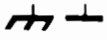
Numbered Test point. Measurement aid (metal post, circuit pad, etc.) provided.

Lettered Test point. No measurement aid provided.

( )

Encloses wire color code. Code used is the same as the resistor color code. First number identifies the base color, second number identifies the wider stripe, third number identifies the narrower stripe (e.g., (947) denotes white base, yellow wide stripe, violet narrow stripe).

A direct conducting connection to the earth, or a conducting connection to a structure that has a similar function (e.g., the frame of an air, sea, or land vehicle).



A conducting connection to a chassis or frame.

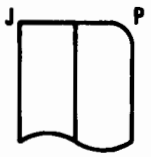
Common connections. All like-designated points are connected. When accompanied by a letter, indicates the type common (i.e., A = Analog, D = Digital, F = Floating).

1-A-1-1

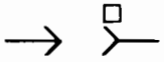
Figure 6-9. Schematic Diagram Notes (Sheet 1 of 2)

SCHEMATIC DIAGRAM NOTES (Continued)

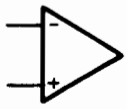
Light Emitting Diode (LED).



Cable and circuit assembly connectors.



Circuit assembly square-pin connectors.



Operational Amplifier (integrated circuit).

Voltage regulator (breakdown diode).

Denotes Field Effect transistor (FET) with N-type base.

Denotes FET with P-type base.

Denotes Silicon Controlled Rectifier (SCR).

Denotes spring-loaded switch.

Identifies service sheet for quick reference.

Signal line identification.

Combined service sheet and signal line identification.

1-A-2-1

Figure 6-9. Schematic Diagram Notes (Sheet 2 of 2)

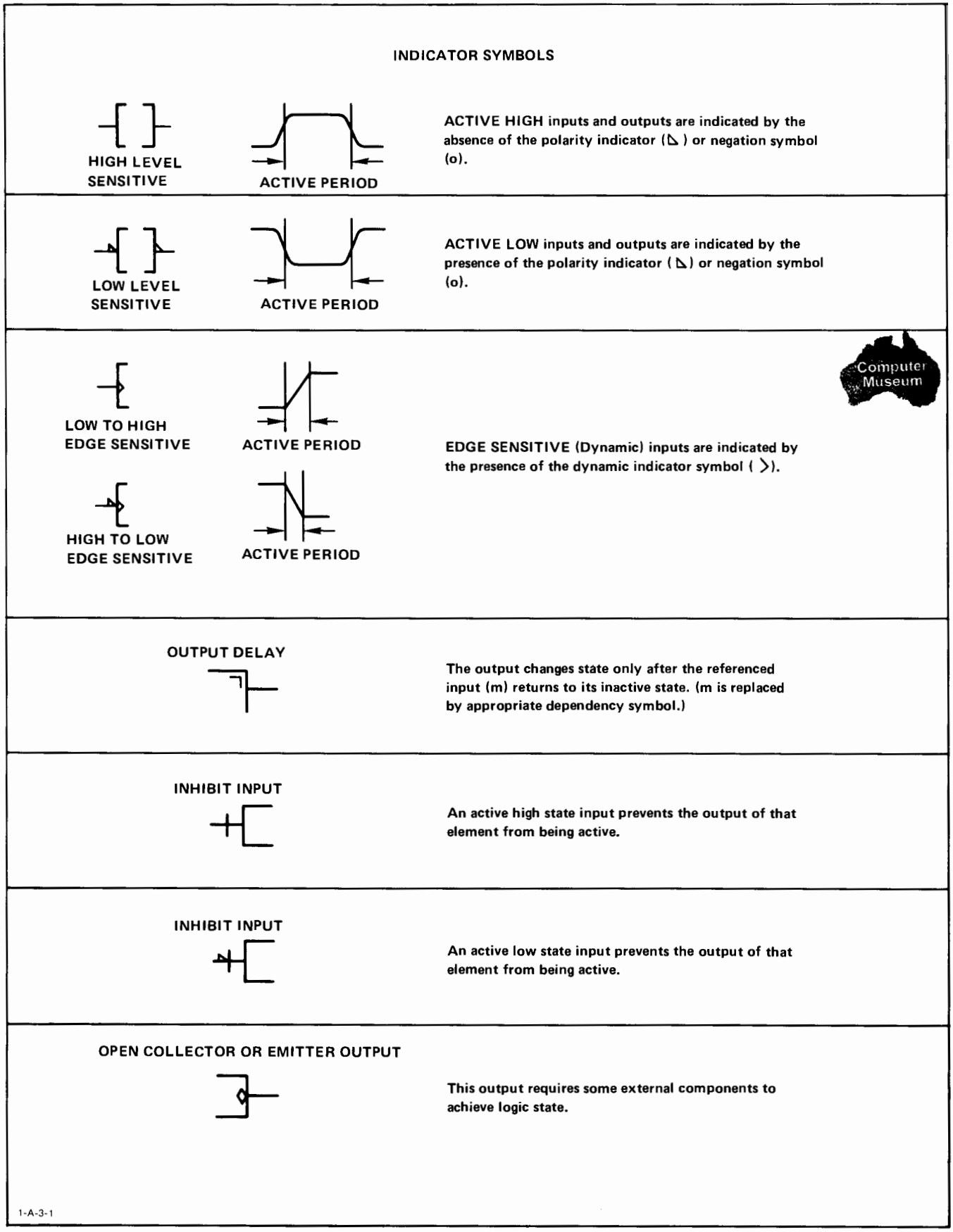


Figure 6-10. ANSI Y32.14 Logic Symbols (Page 1 of 7)

INDICATOR SYMBOLS (Continued)

SCHMITT TRIGGER

AND GATE WITH HYSTERESIS

Schmitt Trigger-⊓ indicates that hysteresis exists in the device.

Dependency Notation

G1
1

The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1".

G1
X_1

OR

G1
1X

When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.

C
X_C

If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.

G1
G2
1.2X

G1
G2
$X_{1.2}$

If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2".

GATE	IEEE STANDARD 91 ANSI Y32.14	TRUTH TABLE	FLIP FLOP	ANSI Y32.14 CONTROL DESIGNATIONS FOR F.F.	DESCRIPTION
AND	A, B → C; A, B, & → C	A B | C L L | L H H | H L H | L H L | L	R-S	R^{FF}, S, Q, $\overline{Q}$	R S | Q $\overline{Q}$ L L | N/C N/C L H | H L H L | L H H H | undetermined

1-A-4-1

Figure 6-10. ANSI Y32.14 Logic Symbols (Page 2 of 7)

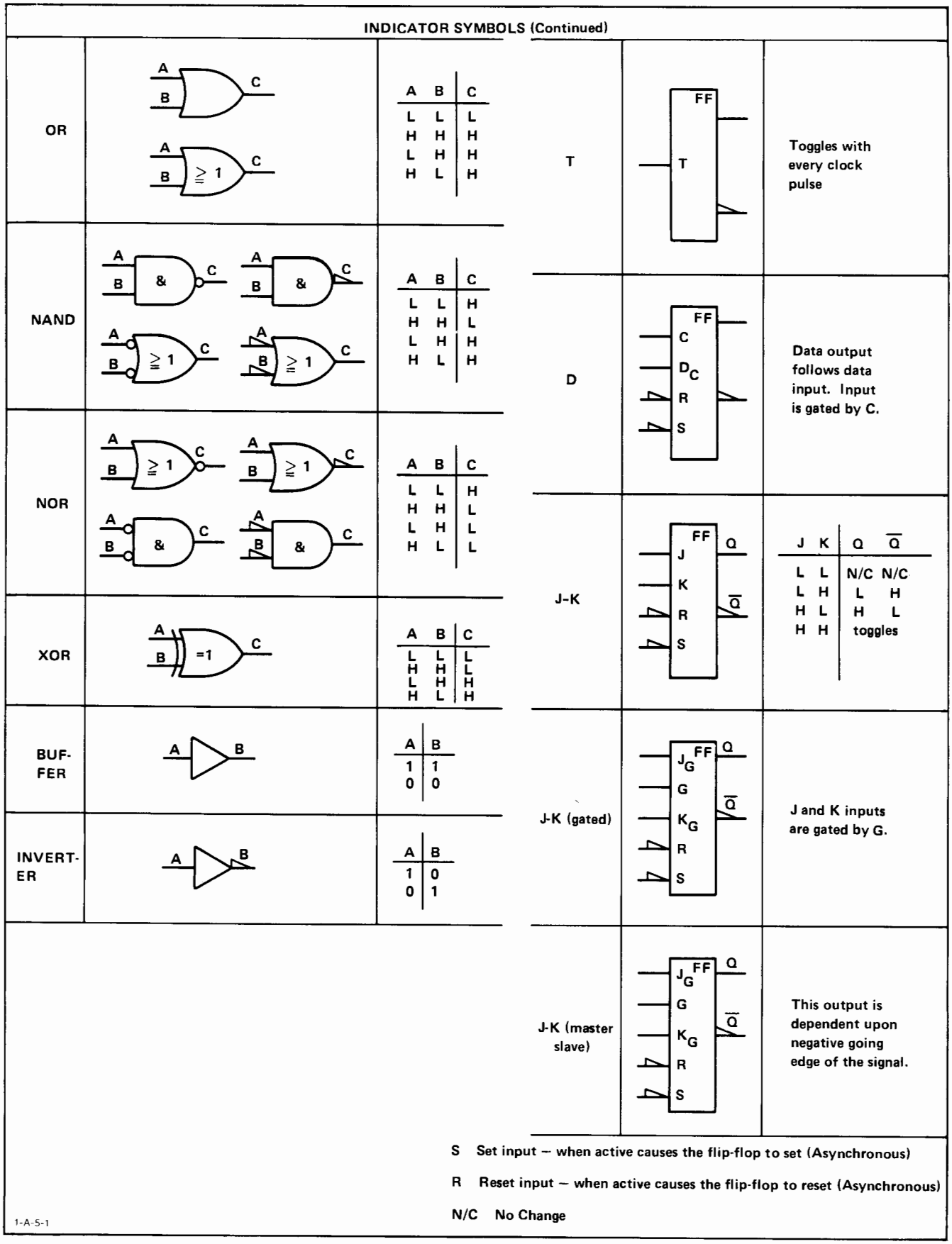
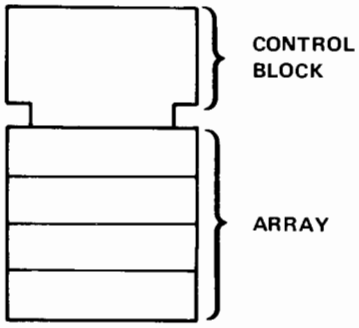


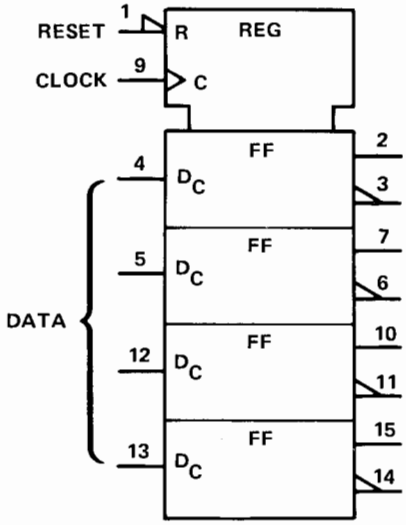
Figure 6-10. ANSI Y32.14 Logic Symbols (Page 3 of 7)

INDICATOR SYMBOLS (Continued)



COMMON CONTROL BLOCK

The Control Block is used to show when common control signals are applied to a group of mechanically connected, but functionally separate units.

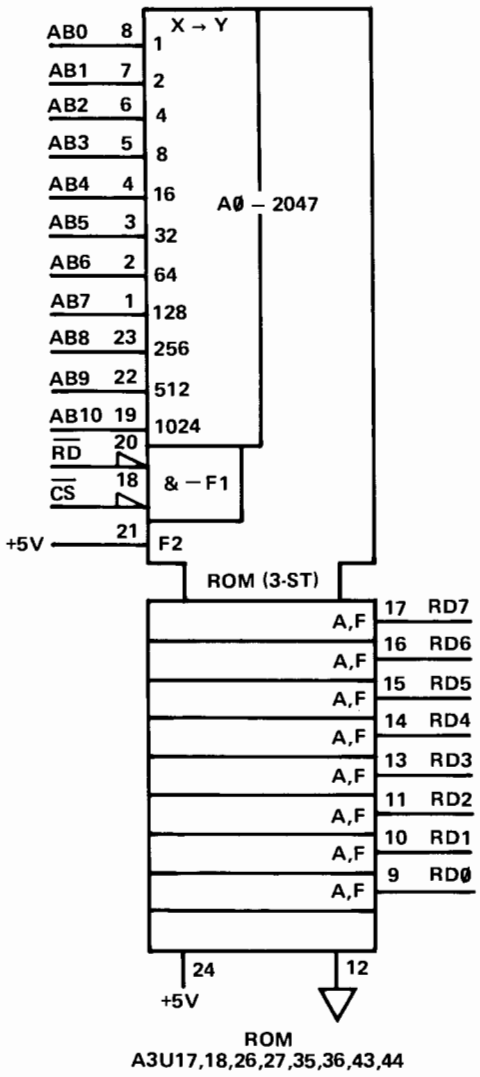


QUAD D-TYPE LATCH

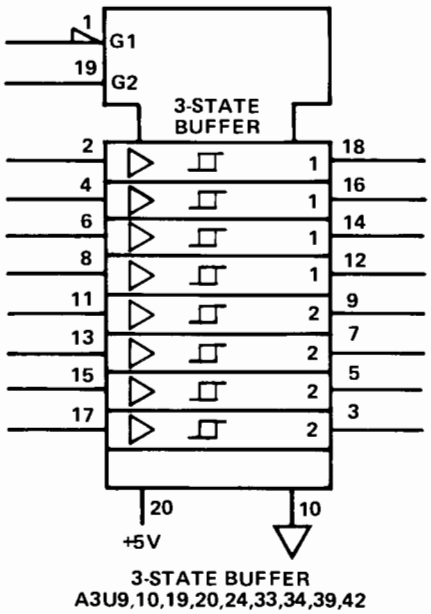
Register control block used to illustrate a quad D-type latch. There is a common active-low reset (R), and a common edge-triggered control input (C). Since there is only one dependency relationship, the controlling input is not numbered and the controlled functions (D) are subscripted with a C.

1-A-6-1

Figure 6-10. ANSI Y32.14 Logic Symbols (Page 4 of 7)



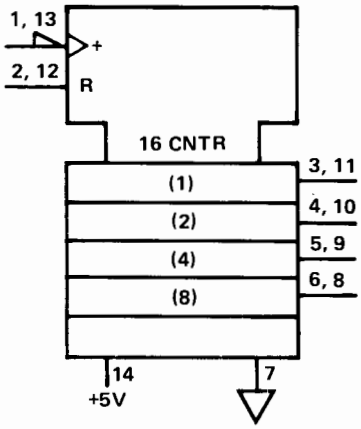
Read Only Memory with 2048 addresses and 8-bit parallel output. Each output byte is selected by the 11-bit address in the upper left portion of the control block. Output is enabled only when gate F1 is low and F2 is high. (In this application, F2 is always high.)



Outputs at pins 12, 14, 16, and 18 are enabled when gate G1 is low, and are high impedance when G1 is high. Outputs at pins 3, 5, 7, and 9 are enabled when G2 is high, and are high impedance when G2 is low. Hysteresis in each buffer improves noise immunity.

1-A-17-1

Figure 6-10. ANSI Y32.14 Logic Symbols (Page 5 of 7)

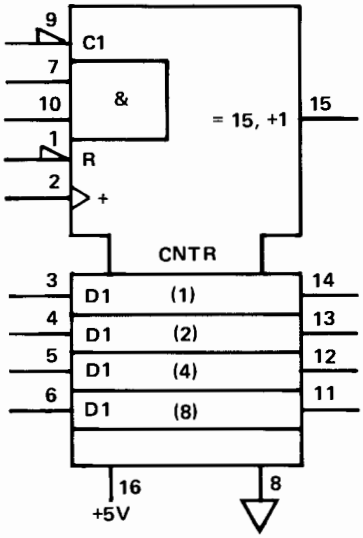


DUAL BINARY COUNTER
A3U2, 31

This IC contains two separate binary counters, as indicated by the two numbers at each signal pin. The control block shows the following common inputs:

+ : Count up by 1 on high to low transition.

R : High level resets all outputs to 0.



PRESETTABLE
BINARY COUNTER
A3U12, 13

The control block shows the following common inputs:

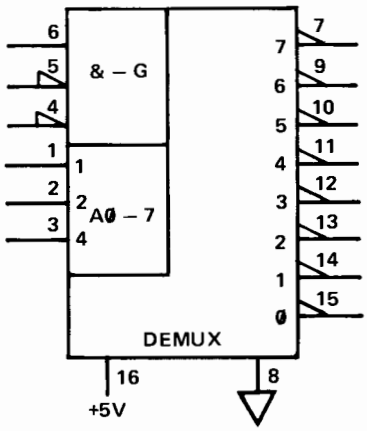
C1 : Low input loads all four flip-flops in parallel.

& : Both inputs must be high to enable counting.

R : Low input resets all outputs to 0.

+ : Count up by one on low to high transition.

The = 15, +1 output goes high for the duration of approximately one clock cycle when the count reaches 15.

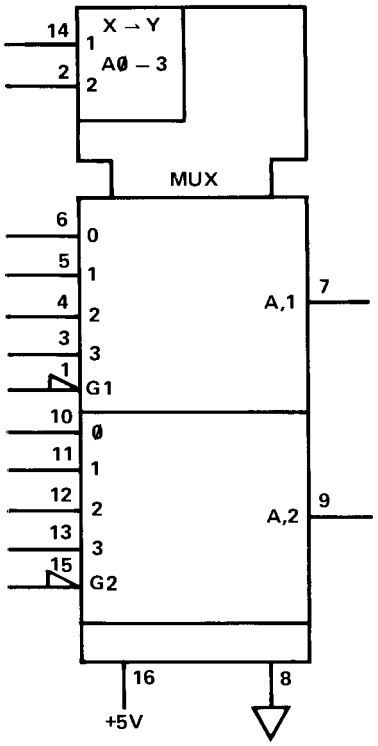


DEMULTIPLEXER
A3U8, 25

Outputs are enabled when all three gate inputs are active. Output selected by the address is low. All other outputs are high.

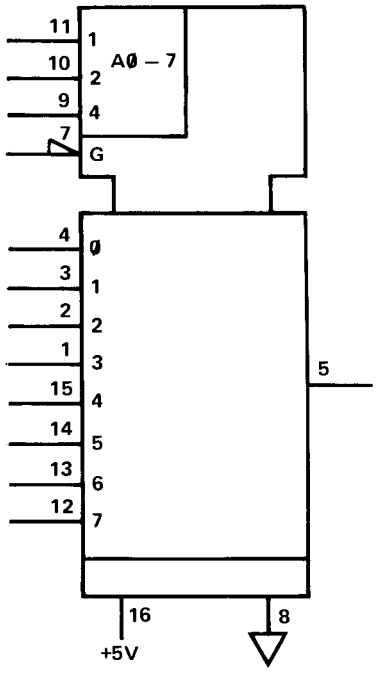
1-A-16-1

Figure 6-10. ANSI Y32.14 Logic Symbols (Page 6 of 7)



MULTIPLEXER
A3U30

Output is selected from the input lines by the address in the upper left corner of the control block. Output is enabled when the gate input (G1, G2) is low. In this application, both gates are always low.



MULTIPLEXER
A3U3

Output is selected from the input lines by the address in the upper left corner of the control block, and is enabled when gate G is low. In this application, G is always low.

1-A-19-1

Figure 6-10. ANSI Y32.14 Logic Symbols (Page 7 of 7)

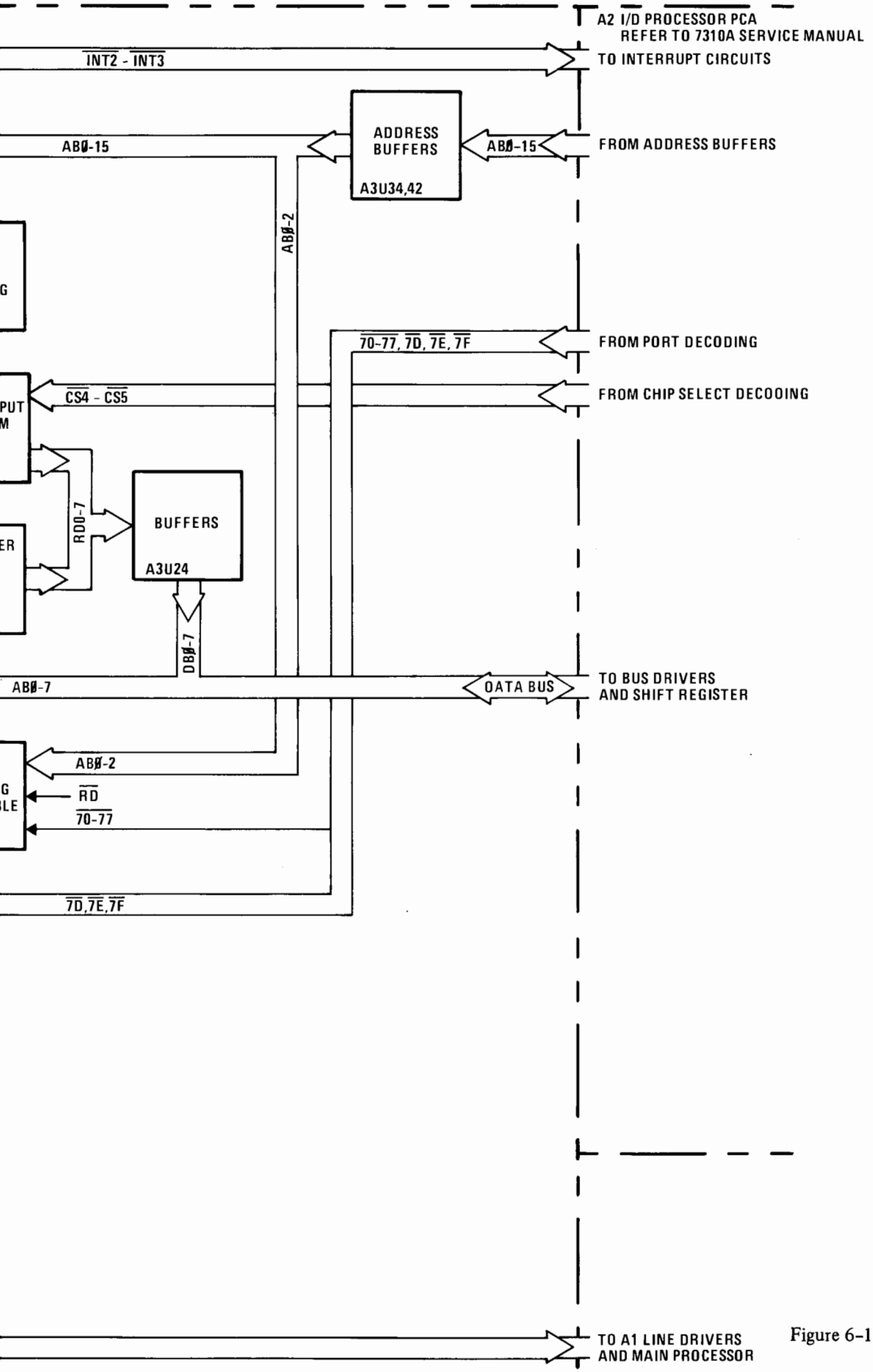
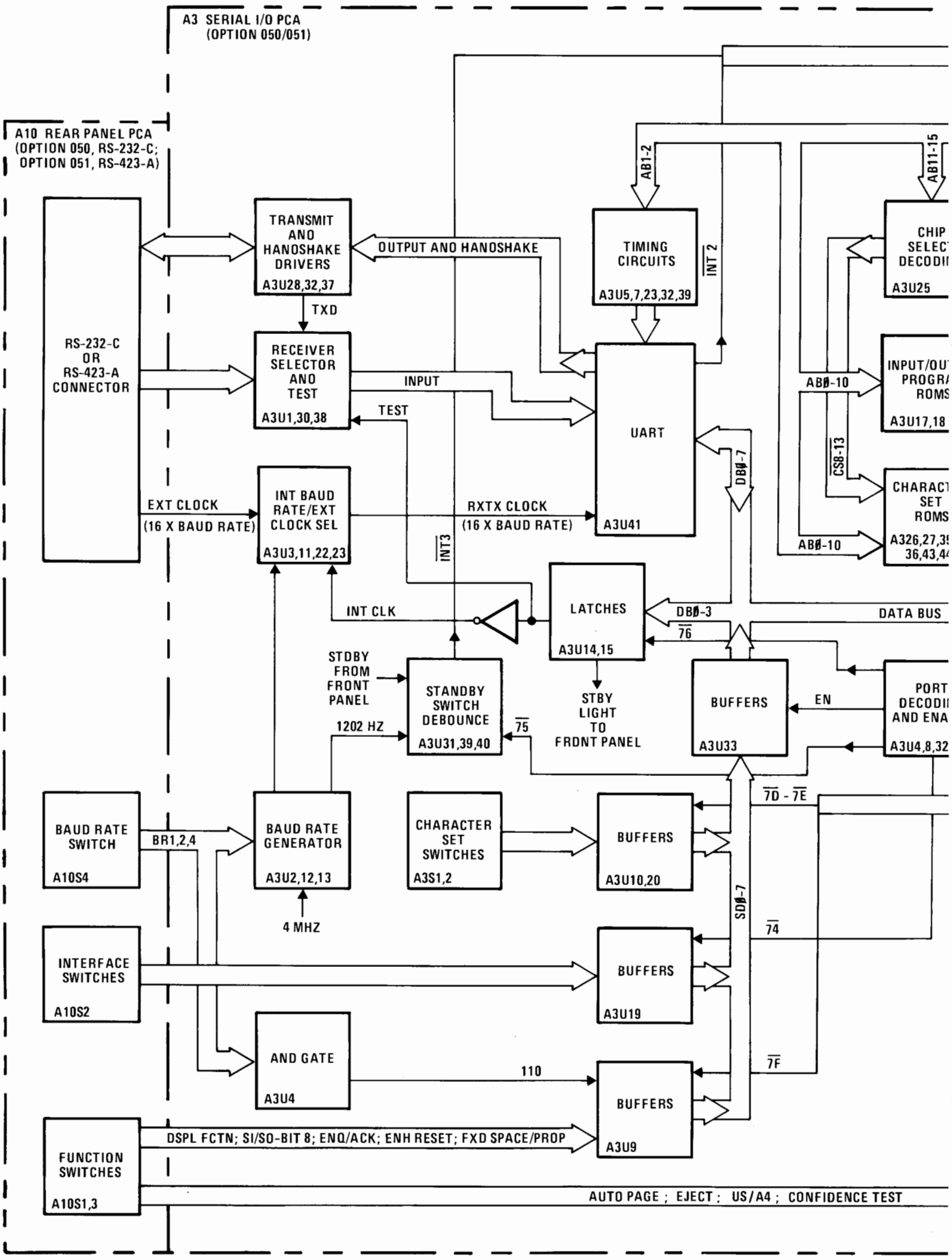


Figure 6-11. Functional Block Diagram, Options 050 and 051


A3 SERIAL I/O PCA
(OPTION 050/051)
A10 REAR PANEL PCA
(OPTION 050, RS-232-C;
OPTION 051, RS-423-A)
RS-232-C
OR
RS-423-A
CONNECTOR
TRANSMIT
AND
HANDSHAKE
DRIVERS
A3U28,32,37
OUTPUT AND HANDSHAKE
TXD
RECEIVER
SELECTOR
AND
TEST
A3U1,30,38
INPUT
TEST
TIMING
CIRCUITS
A3U5,7,23,32,39
INT 2
AB1-2
AB11-15
CHIP
SELEC
DECODI
A3U25
UART
A3U41
DBØ-7
ABØ-10
INPUT/OU
PROGRA
ROMS
A3U17,18
CS8-13
CHARACT
SET
ROMS
A326,27,3
36,43,4
EXT CLOCK
(16 X BAUD RATE)
INT BAUD
RATE/EXT
CLOCK SEL
A3U3,11,22,23
RXTX CLOCK
(16 X BAUD RATE)
INT3
INT CLK
LATCHES
A3U14,15
DBØ-3
DATA BUS
76
STDBY
FROM
FRONT
PANEL
STANDBY
SWITCH
DEBOUNCE
A3U31,39,40
1202 HZ
75
STBY
LIGHT
TO
FRDNT PANEL
BUFFERS
A3U33
EN
PORT
DECODI
AND ENA
A3U4,8,32
7D - 7E
BAUD RATE
SWITCH
A10S4
BR1,2,4
BAUD RATE
GENERATOR
A3U2,12,13
4 MHZ
CHARACTER
SET
SWITCHES
A3S1,2
BUFFERS
A3U10,20
SDØ-7
74
INTERFACE
SWITCHES
A10S2
BUFFERS
A3U19
AND GATE
A3U4
110
7F
BUFFERS
A3U9
FUNCTION
SWITCHES
A10S1,3
DSPL FCTN; SI/SO-BIT 8; ENQ/ACK; ENH RESET; FXD SPACE/PROP
AUTO PAGE ; EJECT ; US/A4 ; CONFIDENCE TEST

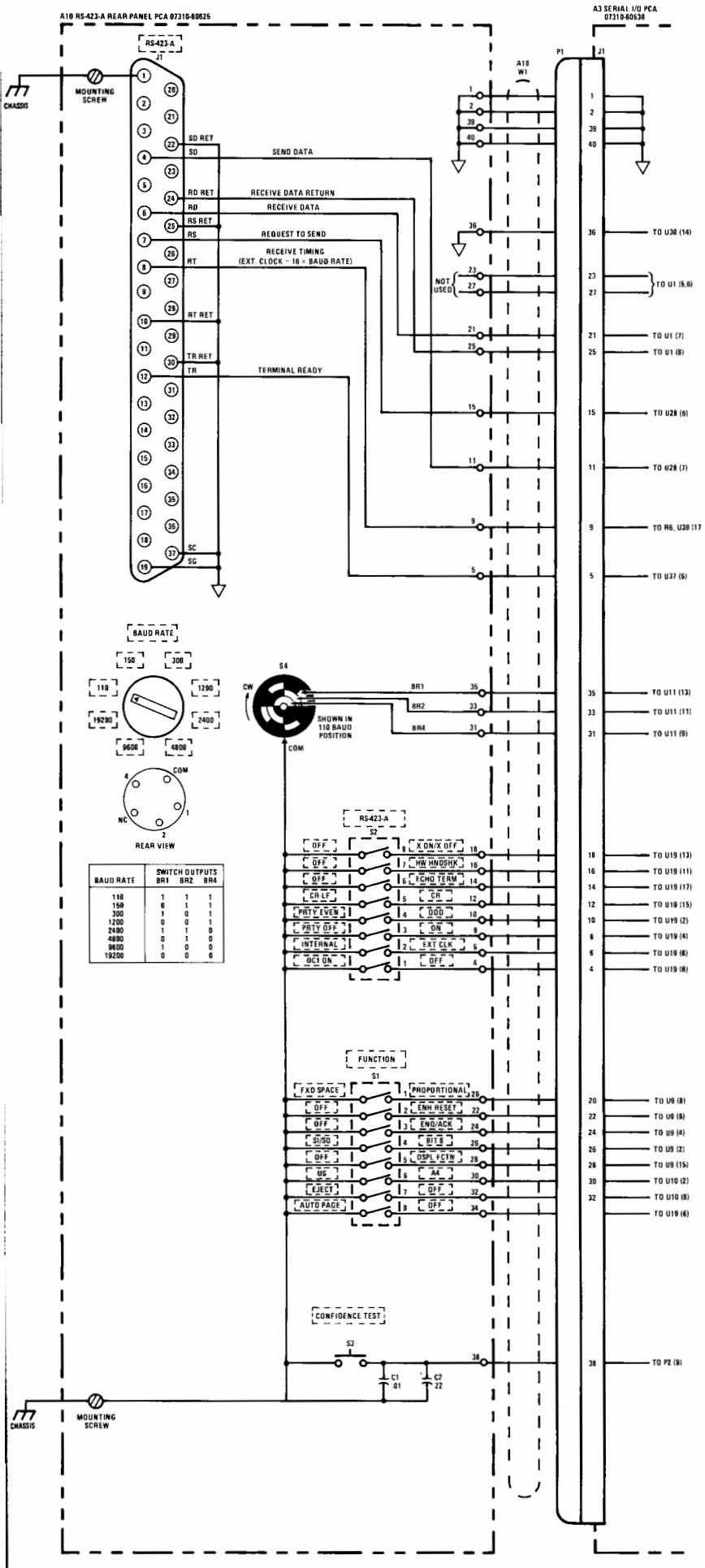
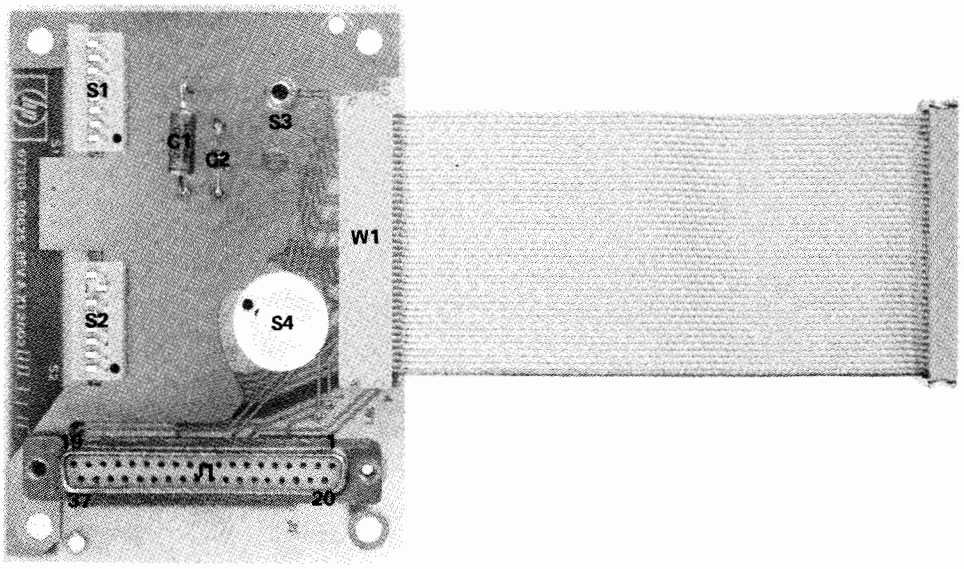
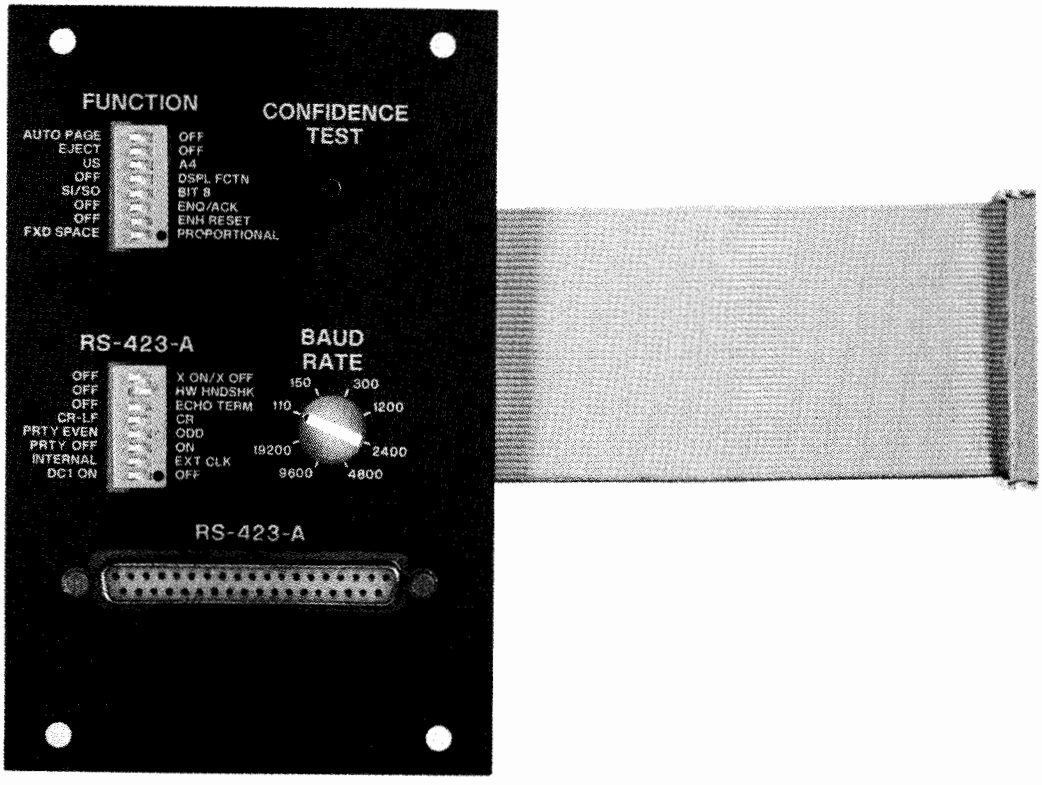


Figure 6-12. Schematic Diagram, Rear Panel PCA, A10, Option 051 (RS-423-A)



A10 (OPTION 051)
07310-60625



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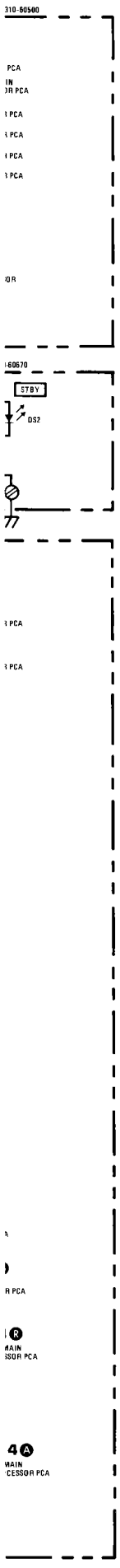
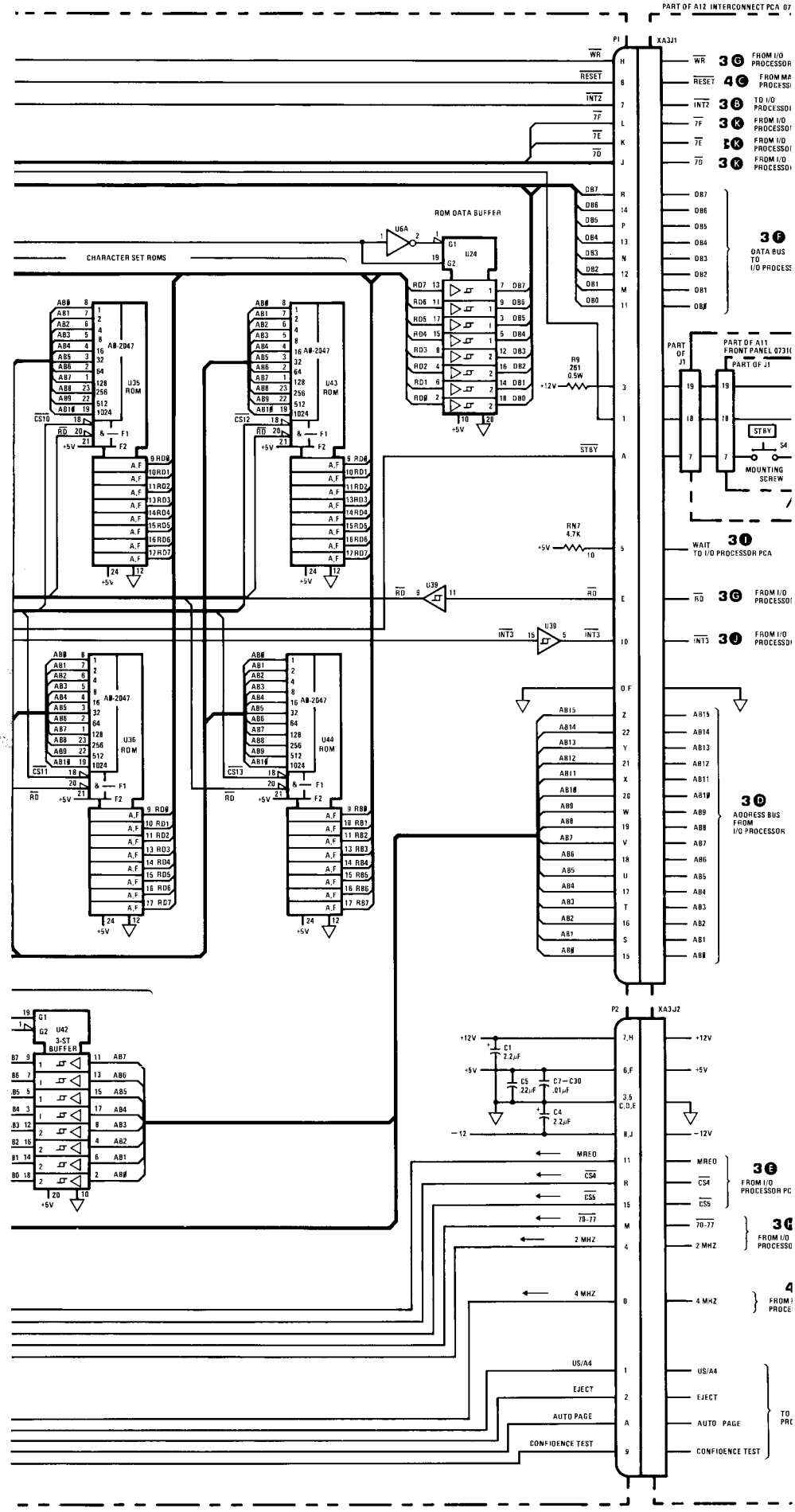
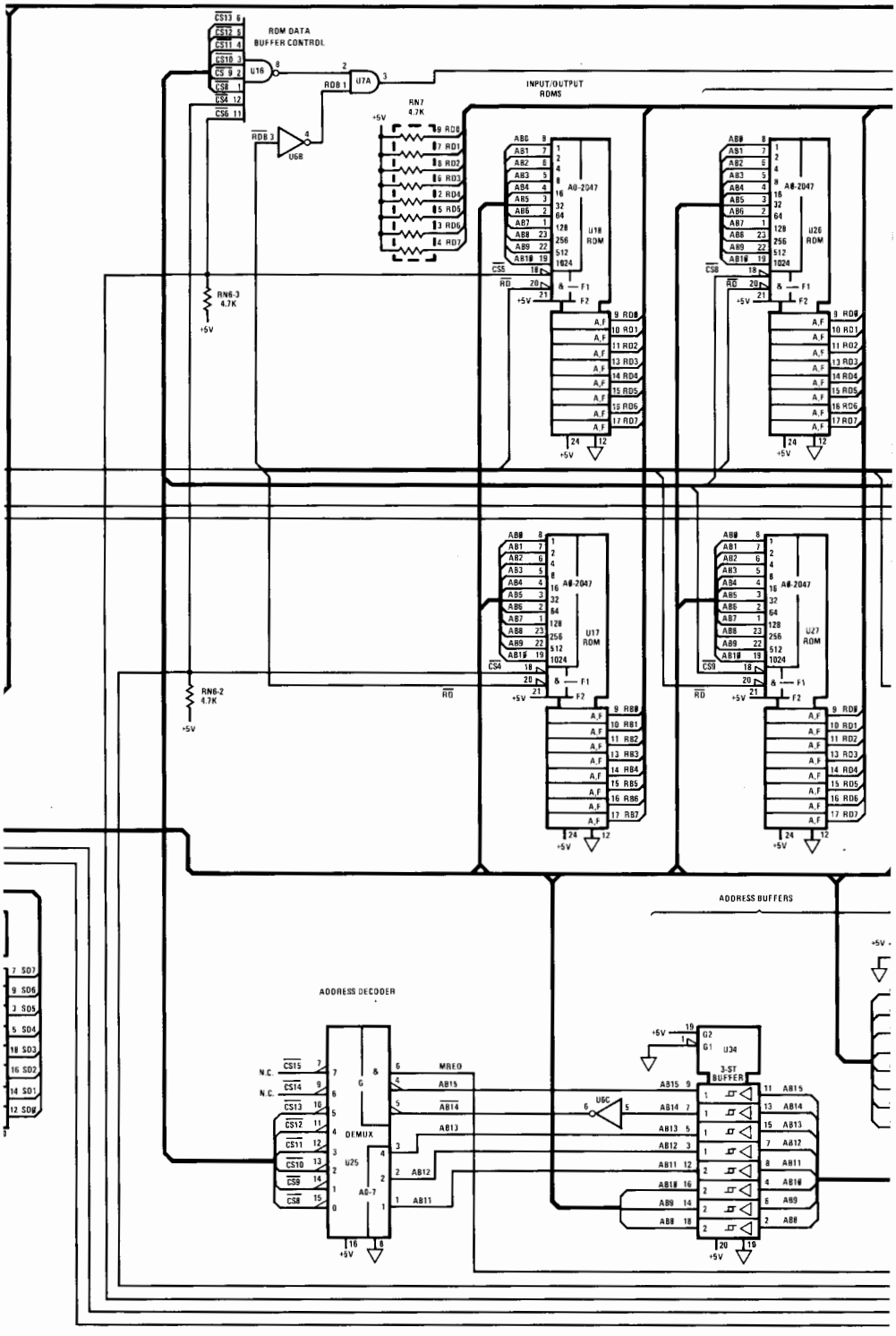
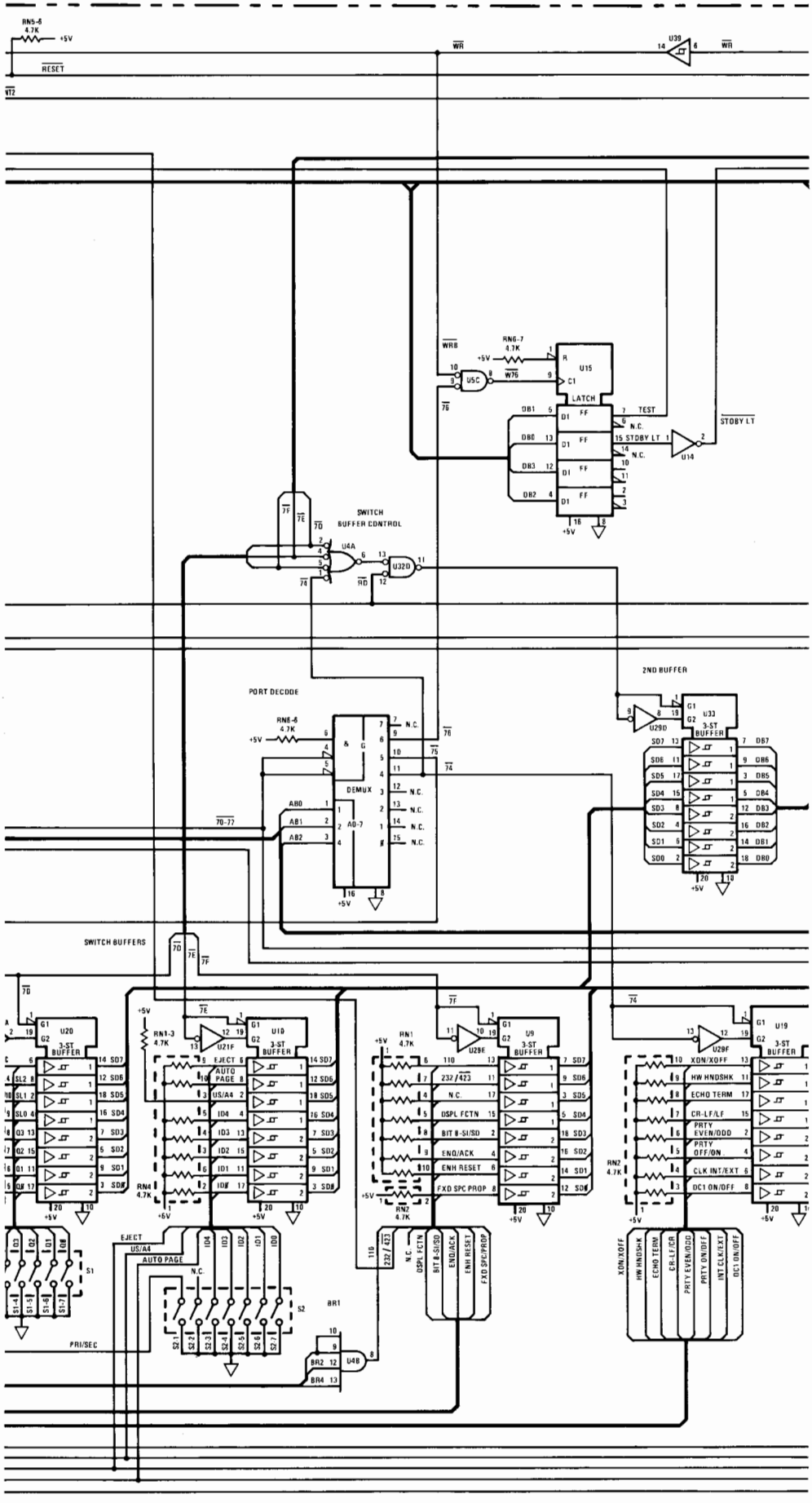
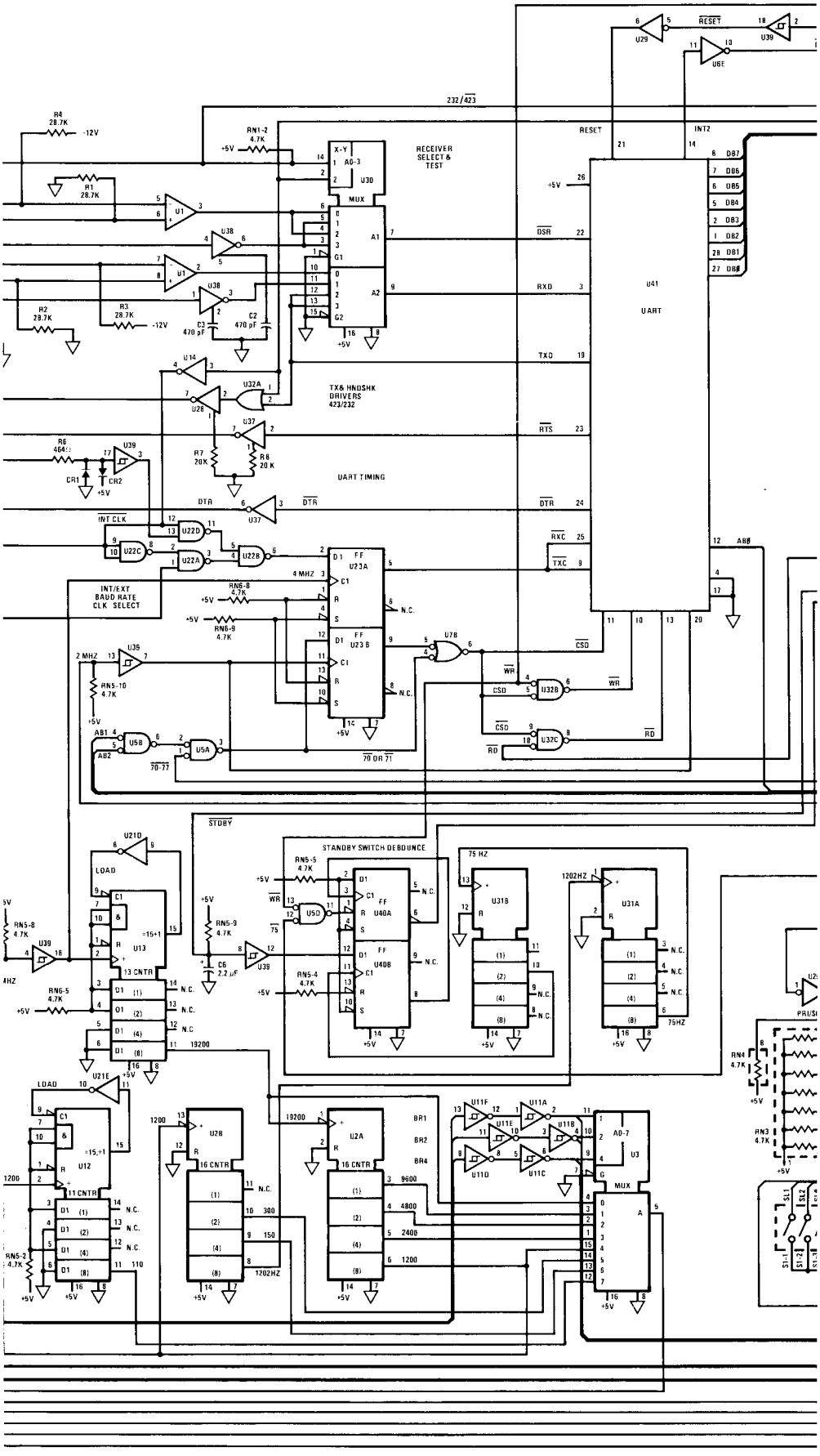


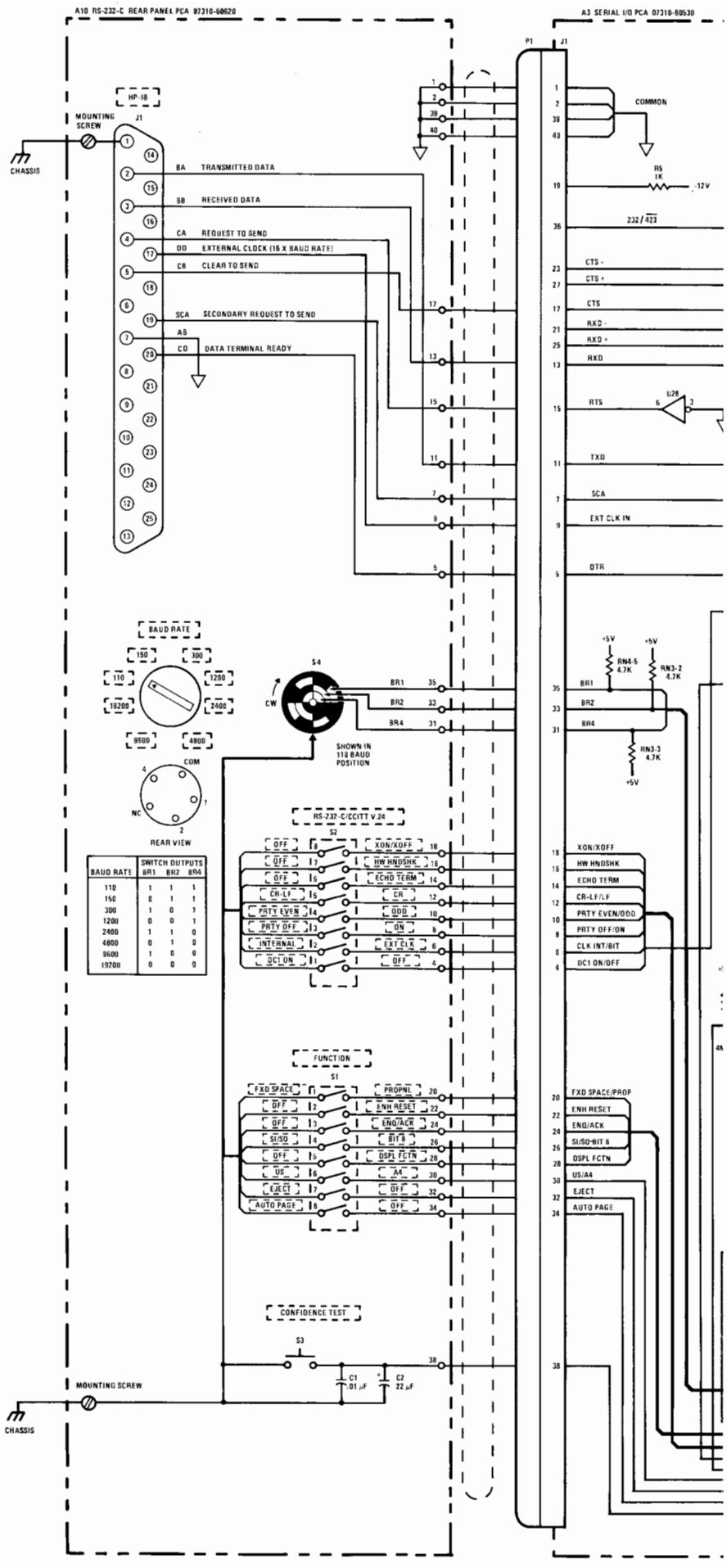
Figure 6-13. Schematic Diagram, Rear Panel PCA, A10 (RS-232-C) and Serial I/O PCA, A3, Option 050


PART OF A12 INTERCONNECT PCA 07
P1
XA3J1
ROM DATA BUFFER
CHARACTER SET ROMS
U6A
U24
U35 ROM
U43 ROM
U36 ROM
U44 ROM
U42 3-ST BUFFER
U39
AB-2047
R9 Z61 0.5W
RN7 4.7K
PART OF A11 FRONT PANEL 07310
PART OF J1
STBY
S4
MOUNTING SCREW
WAIT TO I/O PROCESSOR PCA
FROM I/O PROCESSOR
ADDRESS BUS FROM I/O PROCESSOR
DATA BUS TO I/O PROCESS
FROM I/O PROCESSOR PC
TO PRC
P2
XA3J2
C1 2.2µF
C5 22µF
C7–C30 .01µF
C4 2.2µF
+12V
+5V
-12V
MREQ
2 MHZ
4 MHZ
US/A4
EJECT
AUTO PAGE
CONFIDENCE TEST


ROM DATA BUFFER CONTROL
INPUT/OUTPUT ROMS
ADDRESS BUFFERS
ADDRESS DECODER
RN7 4.7K
RN6-3 4.7K
RN6-2 4.7K
U16
U7A
U68
U18 ROM
U26 ROM
U17 ROM
U27 ROM
A0-2047
U25
DEMUX
A0-7
U34
3-ST BUFFER
U8C
MREQ
AB15
AB14
AB13
AB12
AB11
+5V
RD

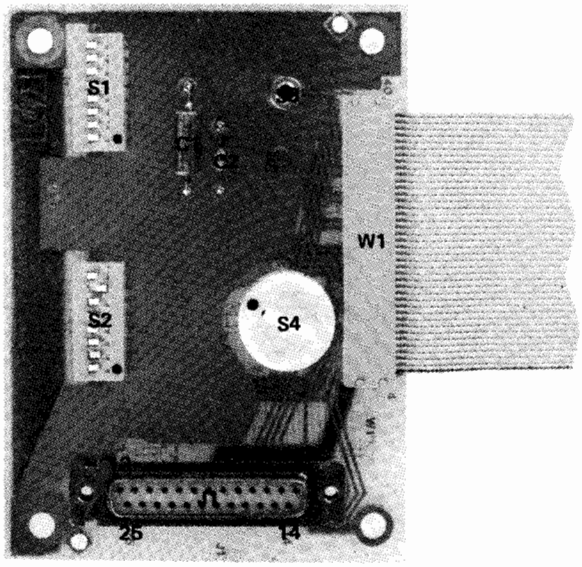

RESET
WR
WR8
W76
LATCH
TEST
STDBY LT
SWITCH BUFFER CONTROL
PORT DECODE
DEMUX
2ND BUFFER
SWITCH BUFFERS
3-ST BUFFER
AUTO PAGE
EJECT
US/A4
PRI/SEC
XON/XOFF
HW HNDSHK
ECHO TERM
CR-LF/LF
PRTY EVEN/ODD
PRTY ON/OFF
CLK INT/EXT
DC1 ON/OFF
232 / 423
N.C.
DSPL FCTN
BIT 8-SI/SO
ENQ/ACK
ENH RESET
FXD SPC/PROP


RESET
232/423
RECEIVER SELECT & TEST
TX& HNDSHK DRIVERS 423/232
UART TIMING
UART
INT/EXT BAUD RATE CLK SELECT
STANDBY SWITCH DEBOUNCE
LOAD
STDBY
INT CLK
4 MHZ
2 MHZ
1200
1202HZ
9600
4800
2400
1200
300
150
110
19200
75HZ

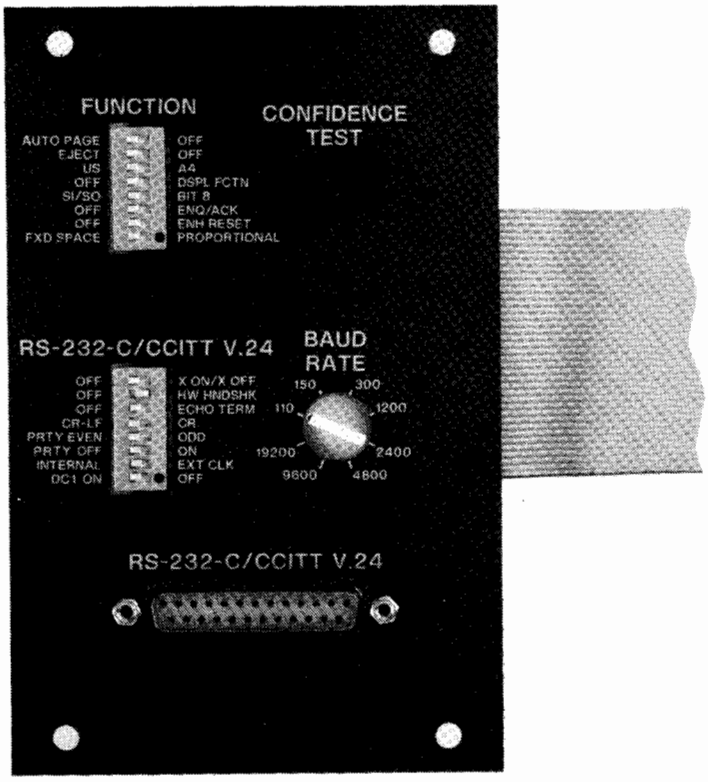


BAUD RATE	SWITCH OUTPUTS BR1	BR2	BR4
110	1	1	1
150	0	1	1
300	1	0	1
1200	0	0	1
2400	1	1	0
4800	0	1	0
9600	1	0	0
19200	0	0	0

7310-J-136-1



A10 (OPTION 050)
07310-60620



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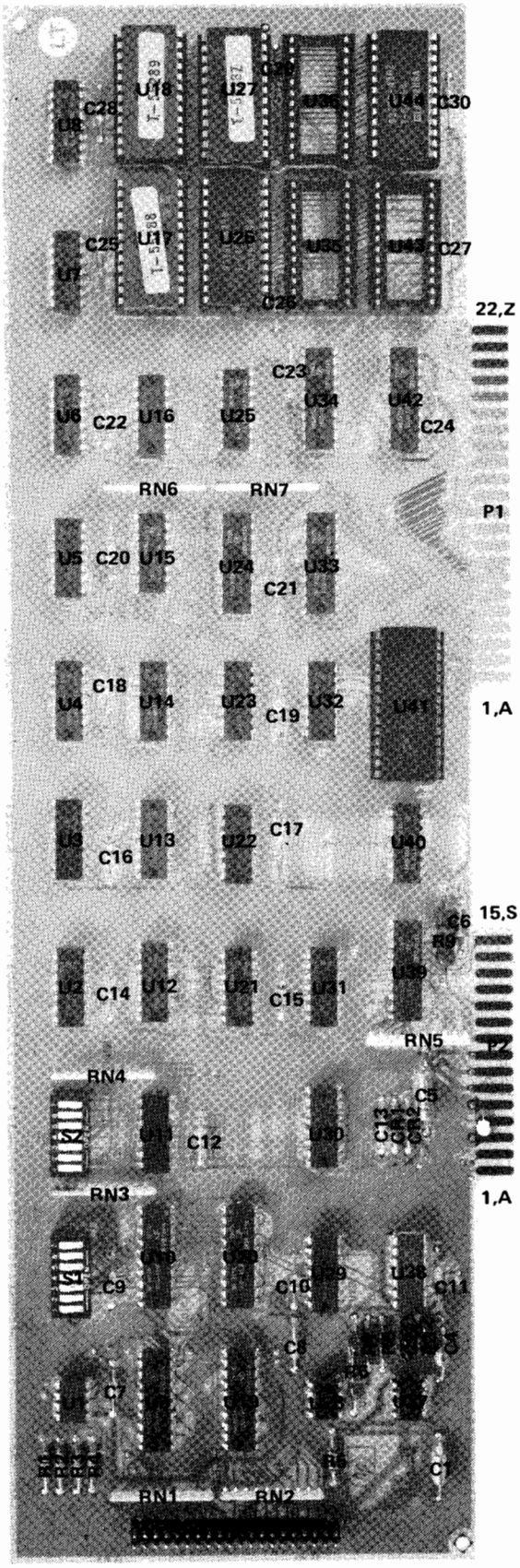

A3 (OPTION 050/051)
07310-60530

07310-90003

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