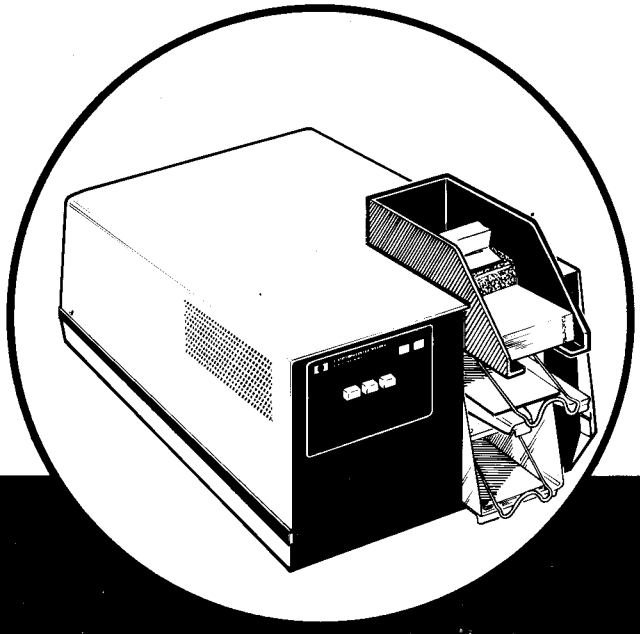
HP7261A-016
INTERFACE



7261A OPTION 016

INTERFACE MANUAL

HEWLETT-PACKARD 7261A OPTICAL MARK READER

HP7261A-016
INTERFACE

OPERATING AND SERVICE MANUAL

7261A OPTICAL MARK READER
OPTION 016
INTERFACE KIT

for

7261A-016 Optical Mark Readers and 12986A Optical Mark Reader Subsystems

Printed-Circuit Assembly:
17200-60001, Series 1330A

NOTE

This manual should be retained with applicable computer documentation.

07261-90006

Printed: SEPTEMBER 1973

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides instructions for interfacing the Hewlett-Packard 7261A Optical Mark Reader to Hewlett-Packard computer systems using the HP 7261A Option 016 Interface Kit. Specifications, installation instructions, programming considerations, principles of operation, and maintenance information of the Kits' interface hardware (PC assembly, cable, and connectors only) are covered in this manual. All driver and diagnostic software tapes in the Kit are independently covered in their own manuals. Refer to the 7261A operating manual (P/N 07261-90000) or the 7261A operating and service manual (P/N 07261-90001) for a discussion of the Reader Hardware.

1-3. DESCRIPTION.

1-4. The HP 7261A Option 016 HP-Computer Interface Kit provides for the transferring of commands, data, and status, bidirectionally between the HP 7261A Reader and the 2100 Series HP Computer. The Kit is included as part of all HP 7261A-016 Readers. The HP 7261A-016 Readers are also defined as HP 12986A Optical Mark Reader Subsystems for Hewlett-Packard computer systems. The Kit includes all necessary interface hardware, driver software tapes, and diagnostic software tapes as listed in Table 1-1. The necessary documentation for all components of the Kit is listed in Table 1-2.

1-5. The 17200-60001 Interface PCA provided in this Kit permits the bidirectional interfacing of the Reader to the computer. The PCA includes two independent 16-bit data registers which allow a two-way flow of information between computer and Reader. The data signals are used for Reader commands and status as well as for card data, and are ground-true/positive-false-logic levels.

1-6. The 17200-60001 PCA uses bits 1, 2, and 3 of its 16-bit output register for transferring commands from the computer to the Reader, bits 0 through 11 of its 16-bit input register for transferring data from the Reader to the computer, and remaining bits 12 through 15 of the input register for transferring status from the Reader to the computer. A Device Command signal from the PCA to the Reader causes the Reader to pick cards. A Device Flag signal, generated by the Reader causes the PCA to gate data bits 0 through 11 into the computer-input register and to generate an interrupt signal to the computer. Control signal and data lines are all compatible with DTL/TTL logic levels and speeds.

1-7. The 17200-60001 Interface PCA is a modified version of the standard ground-true 12566-60001 Interface PCA of the general-purpose HP 12566 Microcircuit Interface Kit. Differences between the two are that the 17200-60001 PCA is hardwired so that both Device Flag and status-input Bit 15 signals are required to generate the Service Request (SRQ) signal for Direct Memory Access (DMA) whereas the 12566-60001 PCA only requires the Device Flag.

1-8. The 24-pin printed-circuit board (PCB) connector provided in this kit shorts each cable-connector contact on the component side of the PCA to the adjacent contact on the circuit side. This shorts each data-input line to the equivalent data-output line, and is used for the interface PCA diagnostic test. For proper operation pins 22, 23, AA, and Z of this connector must be connected before use.

1-9. PRODUCT VERSION IDENTIFICATION.

1-10. Hewlett-Packard printed-circuit assemblies (PCA's) are specifically identified as to version with series numbers. Series numbers are five characters wherein the first four characters are date-code numbers designating the date of the last significant design change. (In the series number "1330" - the "13" represents 1973 and the "30" represents week 30, the week of July 23rd.) The fifth character in the series number is a letter designating the country of manufacture (the letter "A" designates being built in America). If the series number of your PCA is numerically higher than the series number on the title page of this manual, your PCA is a revised version of the PCA covered in this manual and a yellow Manual Change supplement should accompany this manual to cover your version.

1-11. Driver software tapes are specifically identified with their part numbers only. If a driver program is revised, a new part number is given to the new version. An updating supplement should accompany the appropriate Small Programs Manual to cover any new part number.

1-12. Diagnostic software tapes are specifically identified with revision letters. The revision letter appears in a parenthesis next to the program's part number. Revisions to the program's tape will have ascending-order letters from earlier versions. An updating supplement should accompany the appropriate Manual of Diagnostics to cover the latest revision.

1-13. If the supplements to cover revised information to your products' manuals are missing or not up-to-date, consult your nearest Hewlett-Packard Sales and Service Office for assistance. These offices are listed at the back of this manual.

TABLE 1-1. HP 7261A OPTION 016 HP – COMPUTER INTERFACE KIT COMPONENTS

PART NUMBER	DESCRIPTION
	Interface Hardware
17200-60001	OMR-to-HP Computer Interface PCA
07261-60350	Card Reader Interface Cable Assembly
1251-0332	24-Pin OCB Connector
	Driver Software
20520-60001 Rev. C	4K SIO Card Reader Driver Tape
20521-60001 Rev. C	8K SIO Card Reader Driver Tape
20522-60001 Rev. C	16K SIO Card Reader Driver Tape
20819-60001 Rev. C	BCS Card Reader Driver Tape
20821-60001 Rev. B	RTE Card Reader Driver Tape
20823-60001 Rev. C	DOS Card Reader Driver Tape
	Diagnostic Software
24296-60001 Rev. A	Diagnostic Configuration Binary Tape
72010-60001 Rev. A	HP 7261 Diagnostic Tape
02760-9067	Clock-After-Data Test Card Set (50 each)
07261-90140	80-Column No Clock Test Card Set (50 each)
09869-90120	40-Column No Clock Test Card Set (50 each)
09869-90130	Clock-On-Data Test Card Set (50 each)

NOTE: The software revision level indicates the earliest version which is intended to work with the HP 7261A rather than the current revision level. For information on revised versions of this software, contact your HP Sales Office.

TABLE 1-2. HP 7261A OPTION 016 HP – COMPUTER INTERFACE KIT MANUALS

MANUAL NUMBER	TITLE
	Interface Hardware Manual
07261-90006	INTERFACE MANUAL
	HP 7261A Option 016 HP – Computer Interface Kit
	Driver Software Manuals
12602-90021	SMALL PROGRAMS MANUAL
	HP 20819-60001 BCS Card Reader Driver Tape (D.15)
12602-90022	SMALL PROGRAMS MANUAL
	HP SIO Card Reader Driver Tapes
12602-90023	SMALL PROGRAMS MANUAL
	HP 20821-60001 RTE and HP 20823-60002 DOS Card Reader Driver (DVR 15) Tapes
07261-90005	MANUAL OF DIAGNOSTICS
	HP 7261A Optical Mark Reader Diagnostic
02100-90157	MANUAL OF DIAGNOSTICS
	Diagnostic Configurator

1-14. SPECIFICATIONS.

1-15. Specifications for the interface PCA are listed in Table 1-3.

TABLE 1-3. INTERFACE PRINTED-CIRCUIT ASSEMBLY SPECIFICATIONS

GENERAL SPECIFICATIONS

Card Dimensions:

Width: 7-3/4 in. (196,8 mm)
Height: 8-11/16 in. (220,7 mm)

Weight:

Net: 18 oz. (511,2 gm)
Shipping: 2 lb (2,27 kg)

Power Requirements (Computer-Supplied):

+4.5V Supply: 1.1A
-2V Supply: 50 mA

PERFORMANCE SPECIFICATIONS

Signal Levels:

SIGNAL REQUIREMENT		"0" LEVEL	"1" LEVEL
DATA AND FLAG INPUTS	Voltage	+2.4 to +5V*	0 to +0.5V
	Bias and Impedance	+3V, 300 ohms to +5V**	
	Current Required		15 mA
DATA AND COMMAND OUTPUTS	Voltage	+2.4 to +5V†	0 to +0.5V
	Impedance	1k	
	Current Sink (maximum)		31 mA

*OR, open circuit capable of withstanding +5V.
**+5V on 2114 Computer; +4.5V on 2115 and 2116.
†+5V maximum; impedance determined by external circuit.

Minimum Pulse Widths:
Flag and Data (Gated Input to Input Register): 300 ns (Flag and Data are simultaneously applied).
Flag and Status (Ungated Input to Input Register): 200 ns (Input Register follows input data).

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspection, installation and reshipment of the HP 7261A Option 016 Interface Kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping container is damaged, request that the carrier's agent be present when the equipment is unpacked. Inspect the kit for damage (scratches, cracks, loose components, etc. on the Interface Card; bent pins, broken covers, and cut insulation on the Cable Assembly; and crushed or torn Program Tapes.) If the Kit is damaged or fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for repair or replacement of the damaged materials without waiting for any claims against the carrier to be settled.

2-5. After the interface kit has been unpacked and inspected, proper operation should be verified. Proper operation is verified by performing the diagnostic procedures described in the Manual of Diagnostics (07261-90005).

2-6. INSTALLATION.

2-7. To install the Interface Kit, proceed as follows:

a. Verify all jumper connections on the Interface PCA (17200-60001). The proper connections of all the nine jumpers for this PCA are given in Table 2-1. For additional information about these jumpers, refer to section IV.

b. If the computer is in RUN (the run switch is lighted, press the HALT switch.)

c. Turn the power off at computer.

d. Open the computer and plug the Interface Card into the desired I/O slot in the card cage. If the HP Reader is to be used with the interrupt system enabled, as when using one of the BCS drivers supplied, then all higher priority I/O slots should contain either an I/O card or a Priority Jumper Card.

NOTE

Press the Interface PCA firmly into the I/O slot in the card cage to assure proper seating. Often the 80-pin connectors in previously unused I/O slots are stiff and require heavy pressure for proper seating. If this is the case, it is wise to check that both edges of the card are in the guide slots provided before proceeding. When installing the interface card in an HP 2100 Computer, the red puller is toward the back of the computer and the component side to the left. Be sure to check before power-up of the computer because there is no keying.

e. Pass the 48-pin connector on Cable Assembly (P/N 07261-60350) into rear of the computer and to the front of the card cage.

f. Press the 48-pin connector onto the installed PCA and close computer.

g. When the Reader has been unpacked, inspected, and prepared for operation as described in the 7261A Operating Manual, packed with the card reader (07261-90000), connect the 36-pin connector on the Cable Assembly to the Card Reader. (NOTE: Jumper DEV in position N and Jumper RH in position S.)

h. Power up the Computer and the Reader and verify proper operation of the Reader by performing the Card Reader Diagnostic as described in the Manual of Diagnostics.

i. When the proper operation has been verified, the Reader is installed. At this time, any relevant software or operating systems can be configured and the Reader placed in operation.

TABLE 2-1. 17200-60001 PCA JUMPER CONNECTIONS REQUIRED TO OPERATE THE HP 7261A READER

JUMPER	CONNECTION	FUNCTION
W1	A	Provides ground true Device Command signal
W2	B	Clears Device Command FF on negative going edge of Device Flag signal
W3	B	Sets Flag Buffer FF and strobes new data into input register on the negative-going edge of Device Flag signals
W4	B	Makes output data continuously available
W5, W6, W7	Connected	Device Flag signal latches twelve data lines into input data register
W8	Disconnected	Input data register follows four status lines
W9	A	Device Command FF cleared by CLC, CRS, and Device Flag signals

SECTION III

OPERATION AND PROGRAMMING

3-1. OPTICAL MARK READER OPERATION AND PROGRAMMING.

3-2. Table 3-1 contains a list of pin assignments for the interconnecting cable. Pin assignments for both the 36-pin male connector that connects to the reader and the 48-pin printed-circuit card connector that connects to the interface card are listed.

3-3. The Optical Mark Reader reads punched or marked tab cards under computer control at a rate of up to 300 cards per minute. Each card contains up to 80 columns of data arranged in 12 rows and each row represents 12 bits of data. Card reading is initiated by a feed (Device Command) signal from the interface card to the reader (initiated by a STC, C instruction). The Device Command causes the reader to pick a card from the hopper and pass it under the photosensors of the read head. The card moves past the read head without stopping and all 80 columns of data are read out and transferred, one column at a time, to the input register on the interface card. Transfer of the columns of data is controlled by clock marks printed along the bottom edge of the card. A clock mark determines when a column of data marks (or punched holes) is positioned under the photosensors of the read head and generates a flag (Device Flag) signal which is sent to the interface card. The Device Flag signal clocks the column of data into the input storage registers and sets the Flag GG on the interface card to indicate to the computer that data is available in the input register for transfer to the computer memory. Data Flags are spaced 1.6 millisecond (±10%) apart for an 80-column card.

3-4. Transfer of the column of data is accomplished by a LIA/B or MIA/B instruction. After the data transfer instruction, a CLF instruction is issued to clear the Flag FF on the interface card until the next column of data is transferred to the computer memory. This CLF instruction must be executed within 1.5 milliseconds from the time the flag was set to avoid loss of data. After the card clears the read head, another Device Command signal causes the next card to be fed and the process is repeated until the input hopper of the reader is empty or the output hopper (stacker) is full, at which time the reader will no longer be ready.

3-5. In addition to the 12 data bits, the reader sends four status bits to the computer through the input storage registers on the interface card. The status bits indicate the operating condition of the reader and allow the computer to be programmed for control of the Reader. Refer to the Operating and Service Manual (07260-90001) for detailed information on the reader.

3-6. CONTROL AND STATUS SIGNAL TIMING.

3-7. The clear to send line is set high to turn on the motor and cause the feed status to go low providing the input hopper isn't empty and the output hopper isn't full and the ready pushbutton has been operated. If clear to send is low and a Device Command is given, no flag will be returned.

3-8. The timing relationships of the Reader's signals are shown in Figure 3-1. The computer uses these signals to test and control the operation of the Reader through the interface card. The Device Command signal (initiated by the STC, C instruction) triggers the Reader feed mechanism to move a card from the hopper through the read head. The STC instruction also enables the interrupt control logic on the interface card. However, the data bits (0 through 11) cannot be transferred from the interface PCA's input storage register to the computer's A/B register until the Flag FF has been set.

3-9. The computer programs given in Tables 3-3 and 3-4 test the status bits (12 through 15) to determine when the Device Flag signal indicates an end-of-card (EOC) or a no-card condition. These conditions are determined by testing the status bits as explained in paragraphs 3-10 and 3-11.

3-10. When a card is fed through the read head, the computer program tests bit 15 (card-in-gate) if bit 15 is a logic 1, the data being transferred is valid data. At the end of the card, bit 15 changes to a logic 0 and bit 14 (extended card-in-gate) remains a logic 1 for 5 milliseconds. This bit combination indicates an end-of-card condition. Another Device Command is initiated to feed the next card and each card is processed until the input hopper is empty. Figure 2-1 shows an operation with two cards in the input hopper. After the last card is processed, any additional Device Command will cause a no-card flag to be immediately generated by the reader to inform the computer that the input hopper is empty.

3-11. The status bits are tested by the computer program in the order listed in Table 3-2 to determine specific status conditions of the reader. For example, when bits 15 and 14 are logic 0's and bit 12 is logic 1, the indication is that a card has not been fed (bits 15 and 14) although the reader is operating properly to feed (bit 12), so a pick failure condition exists (pick roller slippage, warped card, or input hopper empty). Flow charts illustrating recommended procedures for evaluating status before picking and while reading cards are given in Figures 3-2 and 3-3.

TABLE 3-1. CABLE ASSEMBLY PIN ASSIGNMENTS

WIRE COLOR CODE	CARD READER CONNECTOR PIN	INTERFACE CARD CONNECTOR PIN	FUNCTION		
1	1	1	Data output	Row R	(Bit 0)
2	2	2	Data output	X	1
3	3	3	Data output	0	2
4	4	4	Data output	1	3
5	5	5	Data output	2	4
6	6	6	Data output	3	5
7	7	7	Data output	4	6
8	8	8	Data output	5	7
9	9	9	Data output	6	8
90	10	10	Data output	7	9
91	11	11	Data output	8	10
92	12	12	Data output	9	11
93	13	13	Feed OK status		12
94	14	14	Hoppers OK status		13
95	15	15	Extended CIH status		14
96	16	16	Card-in-head status		(Bit 15)
904	18	24	Ground		
97	19	23	Device Flag		
98	20	B	Clear to send*		(Bit 1)
901	21	C	Select command		(Bit 2)
902	22	D	Bell command		(Bit 3)
903	23	Z	Device command		
Shield	36	BB	Ground		

*All except CTS are ground true

TABLE 3-2. STATUS CONDITIONS

BIT NUMBER				CARD READER CONDITION
15	14	13	12	
0	0	0	0	Hoppers bad
0	0	0	1	2 Hoppers bad, OK to feed
0	0	1	0	Hoppers OK, not OK to feed
0	0	1	1	Hoppers OK, OK to feed
0	1	0	0	EOC, hopper bad (last card)
0	1	0	1	1
0	1	1	0	EOC
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	Data, (last card)
1	1	0	1	1
1	1	1	0	Data
1	1	1	1	1

NOTE: 1 Bit combination not possible

2 Bit combination possible when Card Reader Jumper RH is in position C

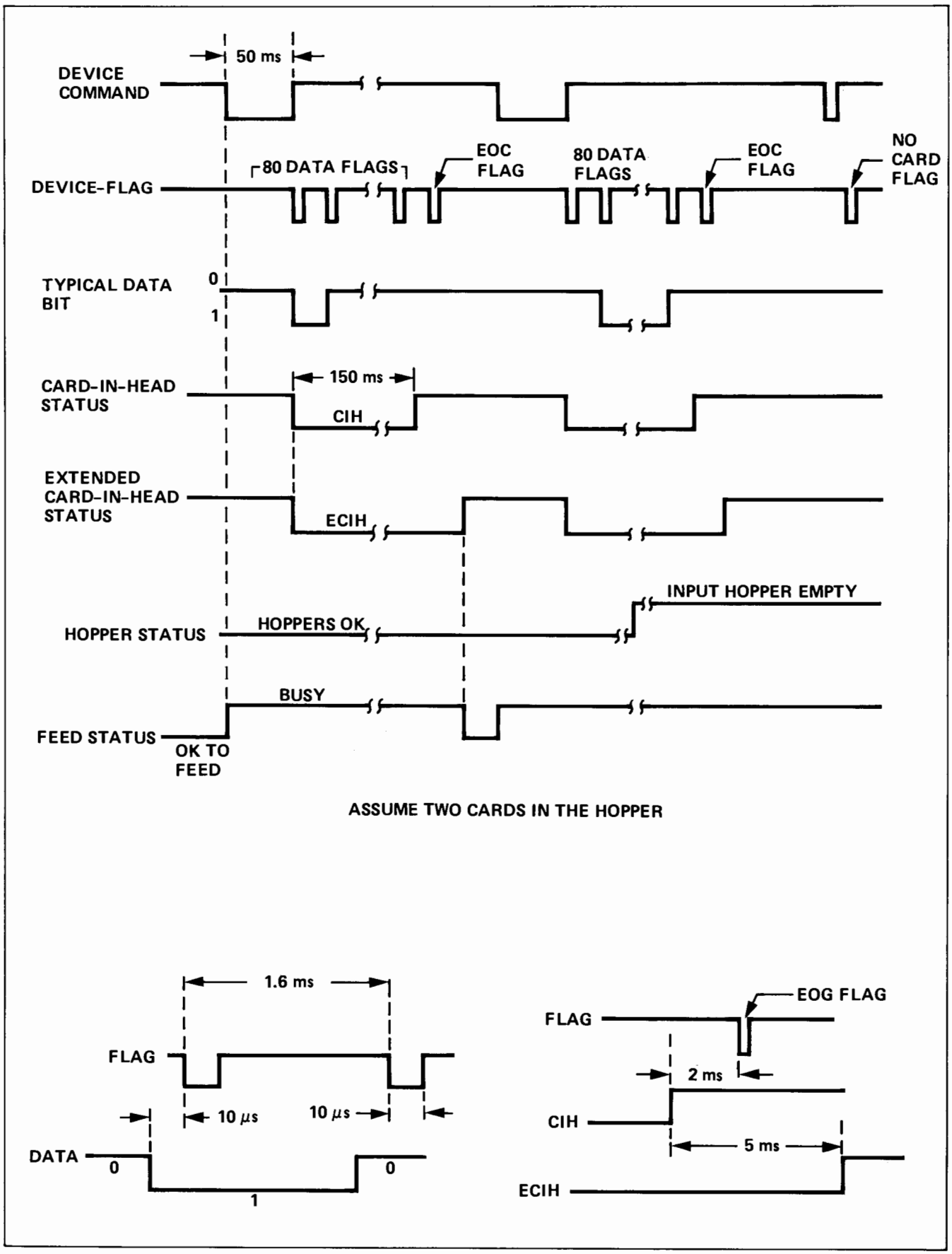


Figure 3-1. Optical Mark Reader Timing

TABLE 3-3. SAMPLE PROGRAM FOR READING 80-COLUMN CARD

```
0001                    ASMB,A,L,B,T
0002*   SAMPLE PROGRAM TO READ  80-COLUMN CARD USING
0003*   OPTICAL MARK READER.
0004*
0005*
0006  01000                 ORG 1000B
0007  01000 002400          CLA             INITIALIZE OUTPUT BUFFER. PRESS
0008  01001 102621          OTA CR           PRESET TO ACCOMPLISH SAME FUNCT
0009  01002 061160          LDA M81         INITIALIZE COLUMN COUNTER TO
0010  01003 071157          STA CNTR         CHECK FOR 80-COLUMN READ.
0011  01004 065036          LDB BUFAD
0012*
0013  01005 103721          STC CR,C        START CARD READER
0014  01006 102321  READ    SFS CR          WAIT FOR FLAG FROM CARD READER
0015  01007 025006          JMP *-1          FLAG SENT UNDER FOLLOWING
0016*                                            CONDITIONS:READER NOT READY
0017*                                                       PICK FAIL
0018*                                                       END-OF-CARD DETECT
0019*                                                       VALID DATA
0020*
0021  01010 103521          LIA CR,C        FLAG SENT; CHECK BUFFER DATA FOR
0022  01011 002021          SSA,RSS          STATUS CONDITION. B15=1?
0023  01012 025021          JMP TEST          NO
0024  01013 011161          AND .7777         YES, VALID DATA IN BUFFER
0025*                                            STRIP OFF STATUS BITS 12-15
0026  01014 170001          STA B,I                AND STORE DATA
0027  01015 006004          INB             INCREMENT BUFFER POINTER
0028  01016 035157          ISZ CNTR        INCREMENT WORD COUNT
0029  01017 025006          JMP READ        READ NEXT COLUMN
0030  01020 025035          JMP BFULL       UNDER NORMAL OPERATION
0031*                                            THIS EXIT SHOULD NOT BE TAKEN
0032*
0033*   THIS PORTION OF THE PROGRAM INTERPRETS STATUS INFORMATION
0034*
0035  01021 001222  TEST    RAL,RAL         TEST B14. IF B14=1, END-OF-CARD
0036  01022 000010          SLA              CONDITION EXISTS
0037  01023 025032          JMP ENDCD       B14=1
0038  01024 001200          RAL              B14=0, TEST B12. IF B12=1, PICK
0039  01025 002020          SSA               FAIL CONDITION EXISTS
0040  01026 025033          JMP PKFAL         B12=1
0041  01027 000010          SLA                TEST B13. IF B13=1, DEVICE
0042  01030 025034          JMP NTRDY           NOT READY, OTHERWISE HOPPER
0043  01031 102010          HLT 10B              EMPTY OR STACKER FULL
0044  01032 102011  ENDCD   HLT 11B         END-OF-CARD HALT
0045  01033 102012  PKFAL   HLT 12B         PICK FAIL HALT
0046  01034 102013  NTRDY   HLT 13B         DEVICE NOT READY HALT
0047  01035 102014  BFULL   HLT 14B         CARD BUFFER FULL HALT CHECK
0048  01036 001037  BUFAD   DEF BUFF
0049  01037 000000  BUFF    BSS 80
0050  01157 000000  CNTR    BSS 1
0051  01160 177657  M81     DEC -81
0052  00021         CR      EQU 21B
0053  00001         B       EQU 1
0054  01161 007777  .7777   OCT 7777
0055                        END
**   NO ERRORS*
```

TABLE 3-4. SAMPLE PROGRAM FOR READING 80-COLUMN CARD USING DMA

```
0001                    ASMB,A,L,B,T
0002*  SAMPLE PROGRAM TO READ 80-COLUMN CARD USING
0003*  OPTICAL MARK READER WITH DMA.
0004*
0005*     DMA INTERCEPTS DATA FLAGS. END-OF-CARD, DEVICE
0006*     NOT READY ,PICK-FAIL, HOPPER/STACKER INTERRUPT
0007*     RECEIVED BY CARD-READER CHANNEL.
0008*
0009  00021I                  ORG 21B
0010  00021 124100            JMP LINK,I     SET TRAP CELL FOR INTERRUPT
0011  00100                   ORG 100B
0012  00100 001015  LINK      DEF TEST       INDIRECT LINKAGE TO TEST
0013  01000                   ORG 1000B
0014  01000 102100            STF 0          TURN ON INTERRUPT SYSTEM
0015  01001 061032            LDA DMACW      INITIALIZE DMA. LOAD THE DMA
0016  01002 102606            OTA DMAH        CONTROL WORD.
0017  01003 106702            CLC DMAL       SWITCH DMA TO LOAD DATA
0018  01004 061033            LDA BUFAD       BUFFER ADDRESS. MAKE SIGN
0019  01005 031154            IOR MSIGN        NEGATIVE TO INDICATE
0020  01006 102602            OTA DMAL          DATA INPUT
0021  01007 102702            STC DMAL       SWITCH DMA TO LOAD WORD-COUNT
0022  01010 061155            LDA M82         REGISTER. END-OF-TRANSMISSION
0023  01011 102602            OTA DMAL         INTERRUPT SHOULD NOT OCCUR
0024  01012 103721            STC CR,C       TURN ON CARD READER
0025  01013 103706            STC DMAH,C     TURN ON DMA
0026  01014 025014            JMP *          WAIT FOR END-OF-CARD INTERRUPT
0027*
0028*   END-OF-CARD INTERRUPT RECEIVED
0029*   PROCESS STATUS
0030*
0031*
0032*   CHECK STATUS TO DETERMINE END-OF-CARD CONDITION,
0033*   DEVICE NOT READY, PICK-FAIL OR HOPPER/STACKER
0034*   CONDITION
0035  01015 102521  TEST      LIA CR
0036  01016 001222            RAL,RAL         AND DETERMINE IF END-OF-CARD
0037  01017 000010            SLA              CONDITION EXISTS. B14=1
0038  01020 025027            JMP ENDCD         B14=1, END-OF-CARD
0039  01021 001200            RAL            TEST B12 FOR PICK FAIL
0040  01022 002020            SSA             CONDITION
0041  01023 025030            JMP PKFAL        B12=1
0042  01024 000010            SLA            TEST B13 FOR NOT READY CONDITION
0043  01025 025031            JMP NTRDY       B13=1, NOT READY
0044  01026 102010            HLT 10B          B13=0, HOPPER EMPTY/STACKER
0045*                                              FULL STATUS
0046  01027 102011  ENDCD     HLT 11B
0047  01030 102012  PKFAL     HLT 12B
0048  01031 102013  NTRDY     HLT 13B
0049  01032 020021  DMACW     OCT 20021
0050  01033 001034  BUFAD     DEF BUFF
0051  01034 000000  BUFF      BSS 80
0052  00006         DMAH      EQU 6B
0053  00002         DMAL      EQU 2B
0054  01154 100000  MSIGN     OCT 100000
0055  01155 177656  M82       DEC -82
0056  00021         CR        EQU 21B
0057                          END
**  NO ERRORS*
```

3-12. The Bell Command activates an audible tone to gain the operator's attention on card readers containing option 004.

3-13. For card readers equipped with option 002, a Select Command may be activated any time between Device Commands. The card picked by the preceding device command will be ejected into the select hopper rather than the output hopper. The Select Command must be deactivated 5 us prior to the next Device Command to avoid selecting the following card. Minimum pulse width is 10 microseconds.

3-14. When a read is being performed using the DMA, every time the Flag is sent and CIH = 1 (bit 15) indicating data, this word will be transferred to core by the DMA and the DMA count will be incremented. If the DMA word count reaches zero, the DMA will set its Flag and possibly generate an interrupt. However, when the Flag is sent and CIH = 0 (bit 15) this data word will not be transferred by the DMA. Instead, the Flag on the Interface PCA is set to request special processing of this word. For this reason, the end-of-card Flag will never be processed by the DMA.

3-15. SAMPLE PROGRAMS.

3-16. Table 3-3 provides a sample assembly language program for reading an 80-column card and Table 3-4 provides a sample assembly program for reading an 80-column card using DMA. Each of these sample programs indicate the operations and instructions required to transfer 80 columns of data (Hollerith characters) from a marked card to computer memory. When standard HP software drivers are used the 12-bit Hollerith characters are converted to ASCII characters (8-bit octal equivalent) and packed two characters to each memory location to conserve available memory.

3-17. The Reader may be programmed in assembly language, FORTRAN and ALGOL. All necessary software required for programming is supplied as part of the computer software package, including detailed programming information.

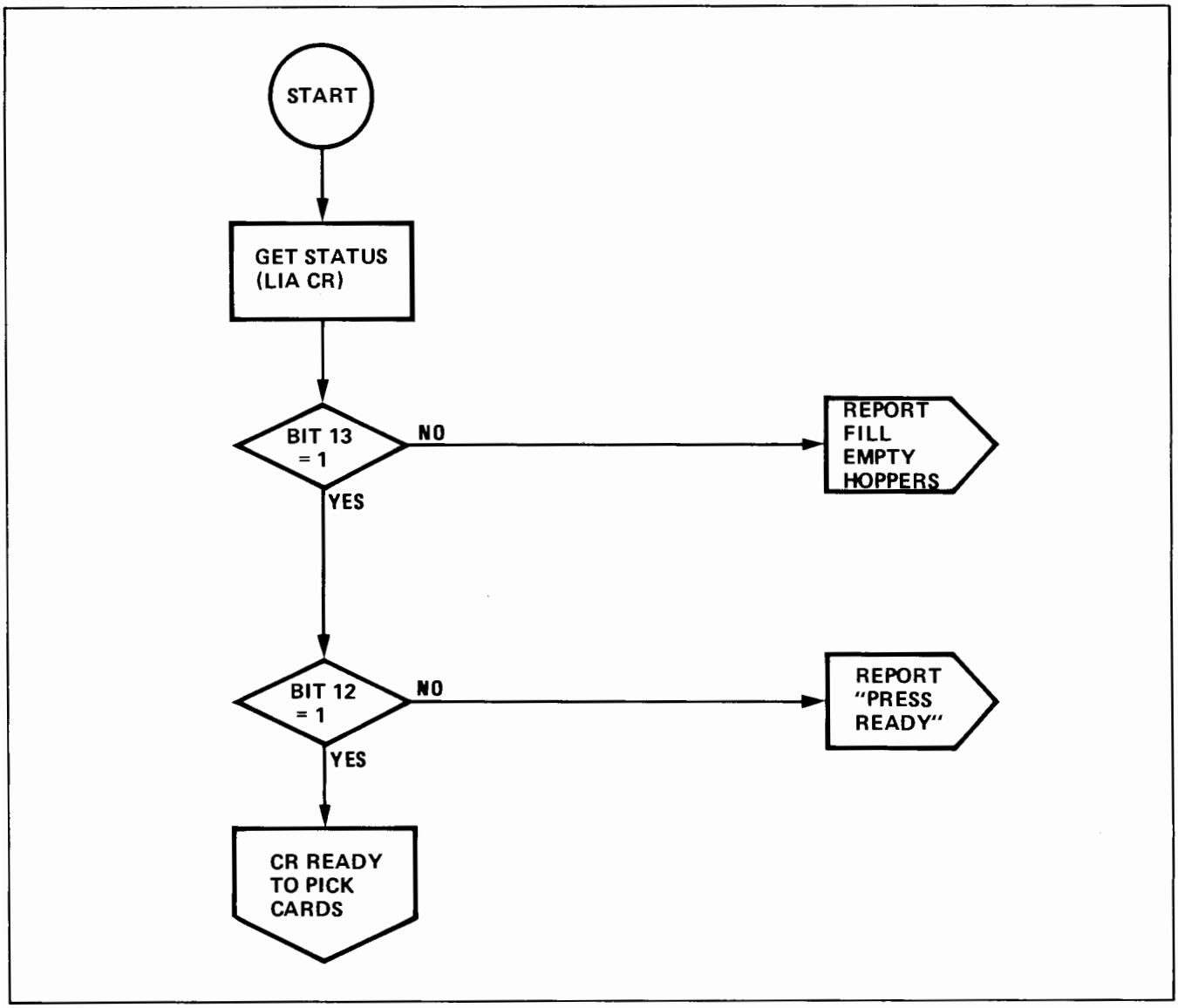


Figure 3-2. Flow Chart for Status Evaluation Prior to Pick

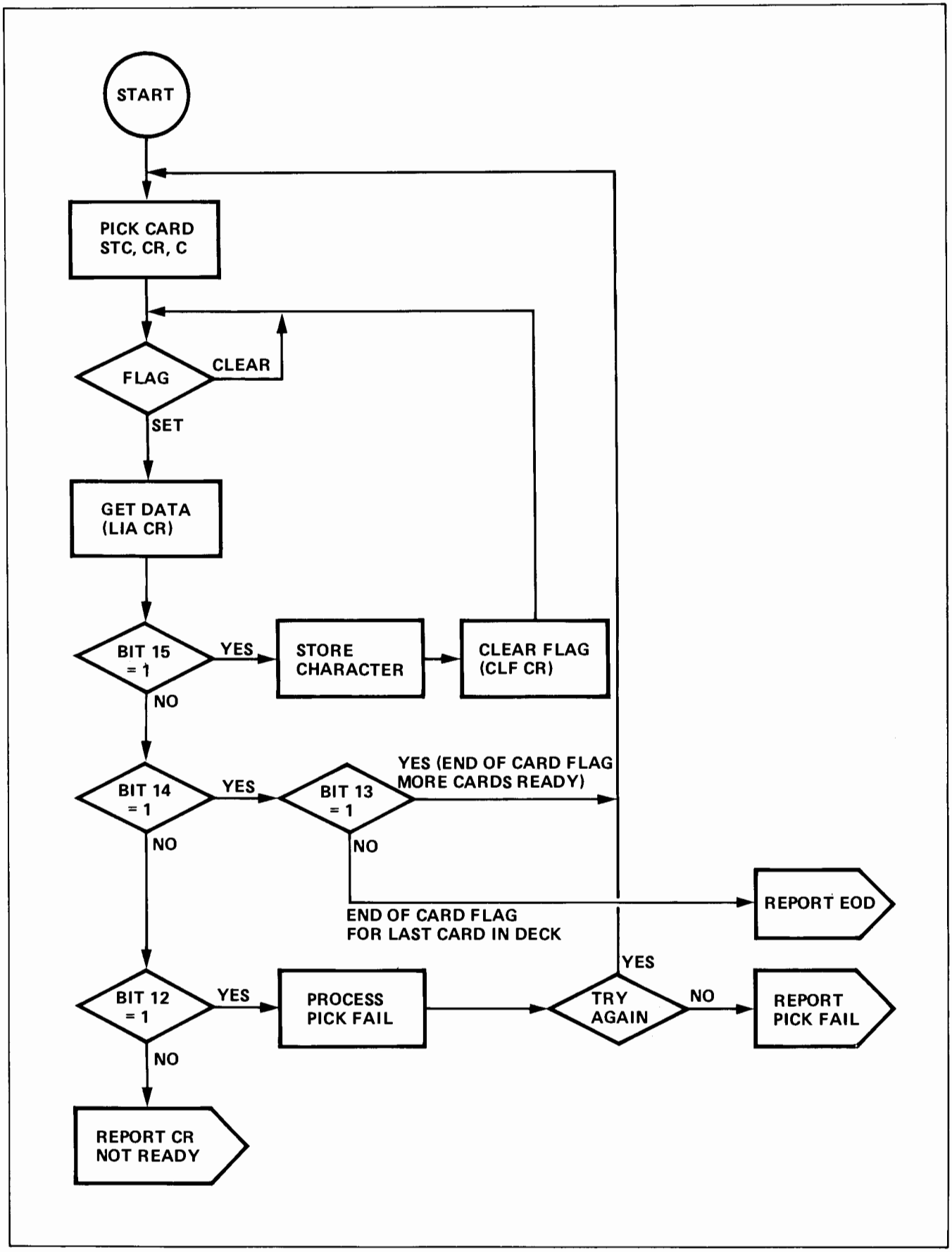


Figure 3-3. Flow Chart for Status Evaluation While Reading Cards

SECTION IV

PRINCIPLES OF OPERATION

4-1. INTRODUCTION.

4-2. This section provides detailed principles of operation for the interface kit.

4-3. OVERALL DESCRIPTION.

4-4. The interface PCA transfers data between an HP computer and an HP 7261A Reader. Two registers are provided on the card. The output storage register provides temporary storage of data sent out by the computer; the input storage register provides temporary storage of data sent to the computer from the Card Reader. Control signals from the computer cause the interface PCA to generate a Device Command signal which picks a card. When data is available, the reader sends a Device Flag signal to the interface card. The computer accepts input data when the Device Flag signal is received or, if the computer interrupt system is in use, when the PCA sends an interrupt signal to the computer. The interface PCA is identical to a Microcircuit Interface Card (12566-60024) with the exception of the Service Request (SRQ) line.

4-5. FUNCTIONAL CIRCUIT DESCRIPTION.

4-6. The following paragraphs describe operation of the various circuits contained on the interface PCA. For further information about the computer input/output system, refer to the instructional manuals supplied with the computer.

4-7. POWER-ON AND PRESET CIRCUIT.

4-8. When computer power is turned on or the PRESET switch is pressed (or EXTERNAL PRESET, depending on computer model), the computer sends POPIO(B) and CRS signals to the interface card. The POIO(B) signal is inverted and sets the Flag Buffer FF; the Flag Buffer FF and the ENF signal set the Flag FF at computer time T2. Inverted again to its original logic level by gate U85A, the POPIO(B) signal clocks the output register. Since the IOBO lines from the computer are low (false) during turn-on or preset, the POPIO(B) signal clears the output register. The inverted CRS signal clears both the Control and Device Command FFs.

4-9. STORAGE REGISTERS.

4-10. The two storage registers on the interface card contain 16 flip-flops each. Integrated circuits U33, U53, U73, and U93 form the output storage register; U23, U43, U63, and U83 form the input storage register.

4-11. The IOO signal from the computer, delayed by the IOO Delay FF, gates computer data from the IOBO lines into the output register. Register contents are present on the output lines to the device at all times, or gated onto the output lines, as determined by the position of jumper W4.

4-12. If jumpers W5 through W8 are disconnected, the input register always contains the data that is present on the input lines from the I/O device. If the four jumpers are connected, a Device Flag signal from the I/O device gates data into the input register. Data from the input register is gated onto the IOBI lines by an IOI signal from the computer.

4-13. FLAG CIRCUIT.

4-14. The Flag FF, Flag Buffer FF, and Device Flag pulse-shaping network comprise the flag circuit. One condition that is required to transfer data between the computer and the I/O device is that the Flag FF be set. The Flag FF is always set at time T2 of the machine cycle following setting of the Flag Buffer FF. The Flag Buffer FF is set by any of three methods: during power turn-on or preset by the POPIO(B) signal, by programming an STF instruction, or by a Device Flag signal from the external device. The Flag and Flag Buffer FFs are both cleared by a CLF program instruction; the Flag Buffer FF is also cleared by an IAK signal from the computer when an interrupt request is acknowledged.

4-15. The Card Reader indicates to the computer that it has transferred data to the computer, by sending a Device Flag signal to the interface card. The output of the Device Flag pulse-shaping network combines with the clear-side output of the Flag FF to provide a low output from gate U87B. This low output sets the Flag Buffer FF. At computer time T2, the set-side output of the Flag Buffer FF and the ENF signal from the computer set the Flag FF. If the computer interrupt system is enabled, a program interrupt occurs after the Flag FF sets; if the interrupt system is disabled, the computer program must check the status of the Flag FF to determine when it sets.

4-16. CONTROL CIRCUIT.

4-17. The computer enables the Card Reader for a data transfer by sending an STC signal to the interface card; the STC signal is the result of an STC program instruction. The Control FF and Device Command FF form the control circuit. Both flip flops are set by the STC signal. The Control FF sets when the first STC signal is sent to the interface card and remains set until CRS or CLC signal is received.

When set, the Control FF fulfills one condition for enabling the interrupt circuit. The Device Command FF, when set, sends a Device Command signal to the I/O device, enabling its operation. In addition to being cleared by a CRS or CLC signal, the Device Command FF is cleared as a result of a Device Flag signal or, at computer time T2, by the ENF signal, depending on placement of jumper W2.

4-18. INTERRUPT CIRCUIT.

4-19. The interrupt circuit, formed by the IRQ FF and associated gating, interrupts computer operation on a priority basis. A data transfer between computer and Card Reader takes place during the interruption of normal program execution. When the Flag and Control FFs are set and an IEN signal is supplied from the computer, initial conditions for an interrupt are met. The resulting low output of U25A provides a low PRL signal to lower priority interface cards. The low PRL signal prevents interrupts from all lower priority devices. At time T5 (SIR signal) the low output of U35A sets the IRQ FF. Setting the IRQ FF provides FLG and IRQ signals which cause the computer to initiate a program interrupt.

4-20. At the next time T2, the ENF signal clears the IRQ FF to allow any higher priority device to request service during the interrupt. If no higher priority device requests service, the PRH signal remains high, as do the other inputs to gate U35A, and at time T5, the SIR signal sets the IRQ FF a second time. The FLG and IRQ signals are then used to indicate the interrupt address.

4-21. The computer sends an IAK signal to the interface card to clear Flag Buffer FF and executes the instruction contained in memory at the interrupt address. At time T2, the ENF signal clears the IRQ FF. Clearing the Flag Buffer FF prevents the IRQ FF from being set again after the requested interrupt is enabled. The Flag FF remains set, however, to maintain the low PRL signal to lower priority devices until processing of the requested interrupt is complete. To clear the Flag FF and enable lower priority devices, a CLF instruction must be programmed.

4-22. SKIP-ON-FLAG CIRCUIT.

4-23. The skip-on-flag circuit allows a data transfer to occur without use of the computer interrupt system. An SKF signal is sent to the computer from the interface card to signal the computer to skip the next program instruction. If an SFS instruction is programmed (SFS signal to the interface card), the SKF signal is generated when the Flag FF is set. If an SFC instruction is programmed (SFC signal to the interface card) the SKF signal is generated when the Flag FF is cleared. When the computer receives the SKF signal, it performs the program instructions necessary to effect the data transfer.

4-24. SELECT CODE DETECTOR.

4-25. When the I/O device is addressed by the computer, the SCM and SCL signals are true (high) at the interface card. The IOG(B) signal is true when a program instruction pertains to any I/O device. These three signals combine at gate U54A to provide an enabling signal for this specific interface card. Thus, the interface card responds only to those program instructions specifying the select code of the I/O slot into which the card is inserted.

4-26. PARTY LINE CIRCUIT.

4-27. The party line circuit, composed of the Party Line FF and associated gating, is used in party line applications in which all devices are connected to a common Device Command signal line. Jumper W1 is placed in position "C". The Party Line FF delays the Device Command signal until time T6. This allows data signals on the output lines to settle before the Device Command signal is sent. The Device Command signal is used by the device to strobe the data from the computer. The Device Command signal is removed when the Party Line FF is cleared at the beginning of time T3 of the next machine cycle.

4-28. GENERATION OF DMA SERVICE REQUESTS.

4-29. The SRQ line provides for generation of DMA Service Requests. If the DMA is assigned to the Card Reader Interface, the SRQ signals the DMA to store the contents of the input buffer in core. The Flag FF and bit 15 of the input register are ended at gate U26B to generate a SRQ. This prevents the generation of service requests when the CIH signal from the card reader is logical 0. In the absence of a service request the setting Flag FF can be detected by the computer and all inputs with C14 (bit 15) a logical 0 must be processed by programmed instructions.

TABLE 4-1. INTERFACE CARD JUMPER FUNCTIONS

JUMPER	POSITION	FUNCTION
W1		DEVICE COMMAND SIGNAL
	A	Provides a ground-true Device Command signal starting at T4.
	B	Provides a positive-true Device Command signal starting at T4.
	C	Provides a pulsed, ground-true Device Command signal starting at T6.
W2		DEVICE COMMAND FF
	A	Device Command FF clears on the positive-going edge of Device Flag signal.
	B	Device Command FF clears on the negative-going edge of Device Flag signal.
	C	ENF signal clears Device Command FF.
W3		DEVICE FLAG SIGNAL
	A	Sets the Flag Buffer FF and strobes input data on the positive-going edge.
	B	Sets the Flag Buffer FF and strobes input data on the negative-going edge.
W4		OUTPUT DATA REGISTER
	A	Output data is gated by the Data FF.
	B	Output data is continuously available to the I/O device.
W5 (bits 0–3) W6 (bits 4–7) W7 (bits 8–11) W8 (bits 12–15)		INPUT DATA REGISTER
	W5, W6, W7, W8 Connected	Device Flag signal latches listed bits of the input data register.
	W5, W6, W7, W8 Disconnected	Listed bits of the input data register follow the input lines from the I/O device.
W9		DEVICE COMMAND FF
	A	Allows the CLC, CRS, and Device Flag signals to clear the Device Command FF.
	B	Allows only the CRS and Device Flag signals to clear the Device Command FF. This action is required for DMA operations.

SECTION V

MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains troubleshooting and diagnostic information for the interface kit. Logic diagrams, component location diagrams, a signal-to-pin index, and replaceable parts lists are included.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are given in the computer system documentation. There are no separate preventive maintenance schedules for the interface kit; however, it is a good practice to remove dust and visually inspect the interface card whenever the card is removed from the computer.

5-5. DIAGNOSTIC TEST.

5-6. Use the Optical Mark Reader Diagnostic to verify proper operation of the interface kit. The Diagnostic Procedure in the Manual of Diagnostics gives operating information for the diagnostic test. The flag, control, and interrupt circuits and the data storage registers are checked for proper operation when the diagnostic test is performed.

5-7. TROUBLESHOOTING.

5-8. Troubleshoot the interface kit by performing the diagnostic test and analyzing any error halts that occur during the test. To further isolate troubles, refer to the signal-to-pin index (Table 5-1), the parts location diagram (Figure 5-2), and the logic diagram for the interface card (Figure 5-2). Replaceable parts lists, in order of reference designations, are provided in Table 5-2.

TABLE 5-1. INTERFACE CARD SIGNAL-TO-PIN INDEX

FROM I/O DEVICE		TO I/O DEVICE	
PIN	SIGNAL	PIN	SIGNAL
1	BIT 0	A	BIT 0
2	BIT 1	B	BIT 1
3	BIT 2	C	BIT 2
4	BIT 3	D	BIT 3
5	BIT 4	E	BIT 4
6	BIT 5	F	BIT 5
7	BIT 6	H	BIT 6
8	BIT 7	J	BIT 7
9	BIT 8	K	BIT 8
10	BIT 9	L	BIT 9
11	BIT 10	M	BIT 10
12	BIT 11	N	BIT 11
13	BIT 12	P	BIT 12
14	BIT 13	R	BIT 13
15	BIT 14	S	BIT 14
16	BIT 15	T	BIT 15
23, AA	DEVICE FLAG	22, Z	DEVICE COMMAND
24	GROUND	BB	GROUND

TABLE 5-2. CARD 17200-60001, REPLACEABLE PARTS

Reference Designation	HP Part No.	Description	Mfr. Code	Mfr. Part No.
C3	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 Vdcw	28480	0160-0153
C4, C5	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 Vdcw	28480	0160-0154
C6 thru C20, C22 thru C30	0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 Vdcw	56289	150D105X-9035A2
R1 thru R16, R52, R63	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F
R17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 50, 59	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8 W	19701	MF4CD3160F
R18, 20, 22, 24, 26, 28 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 60	0757-0420	Resistor, Fxd, Flm, 750 ohms, 1%, 1/8W	28480	0757-0420
R49, R65, R66	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R61, R62	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401
R64	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R67, R73 thru R75	0757-0442	Resistor, Fxd, Flm, 10k, 1%, 1/8W	14674	MF4CD1002F
R68 thru R72	1810-0020	Resistor, Network (7 fxd flm resistors)	28480	1810-0020
U22, 36, 37, 42, 47, 55, 56, 57, 62, 76, 82, 86, 87, 95	1820-0054	Integrated Circuit, TTL	01295	SN7400N
U23, 33, 43, 53, 63, 73, 83, 93	1820-0301	Integrated Circuit, TTL	01295	SN7475N
U24 thru U27, 34, 44, 54, 64, 74, 84, 94	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U31, 32, 51, 52, 71, 72, 91, 92	1820-0348	Integrated Circuit, DTL	01295	SN15844N
U35	1820-0069	Integrated Circuit, TTL	01295	SN7420N
U45, 46, 77	1820-0068	Integrated Circuit, TTL	12040	SN7410N
U67	1820-0077	Integrated Circuit, TTL	01295	SN7474N
U75, 85	1820-0071	Integrated Circuit, TTL	01295	SN7440N
W1 thru W9	8159-0005	Jumper Wire	28480	8159-0005

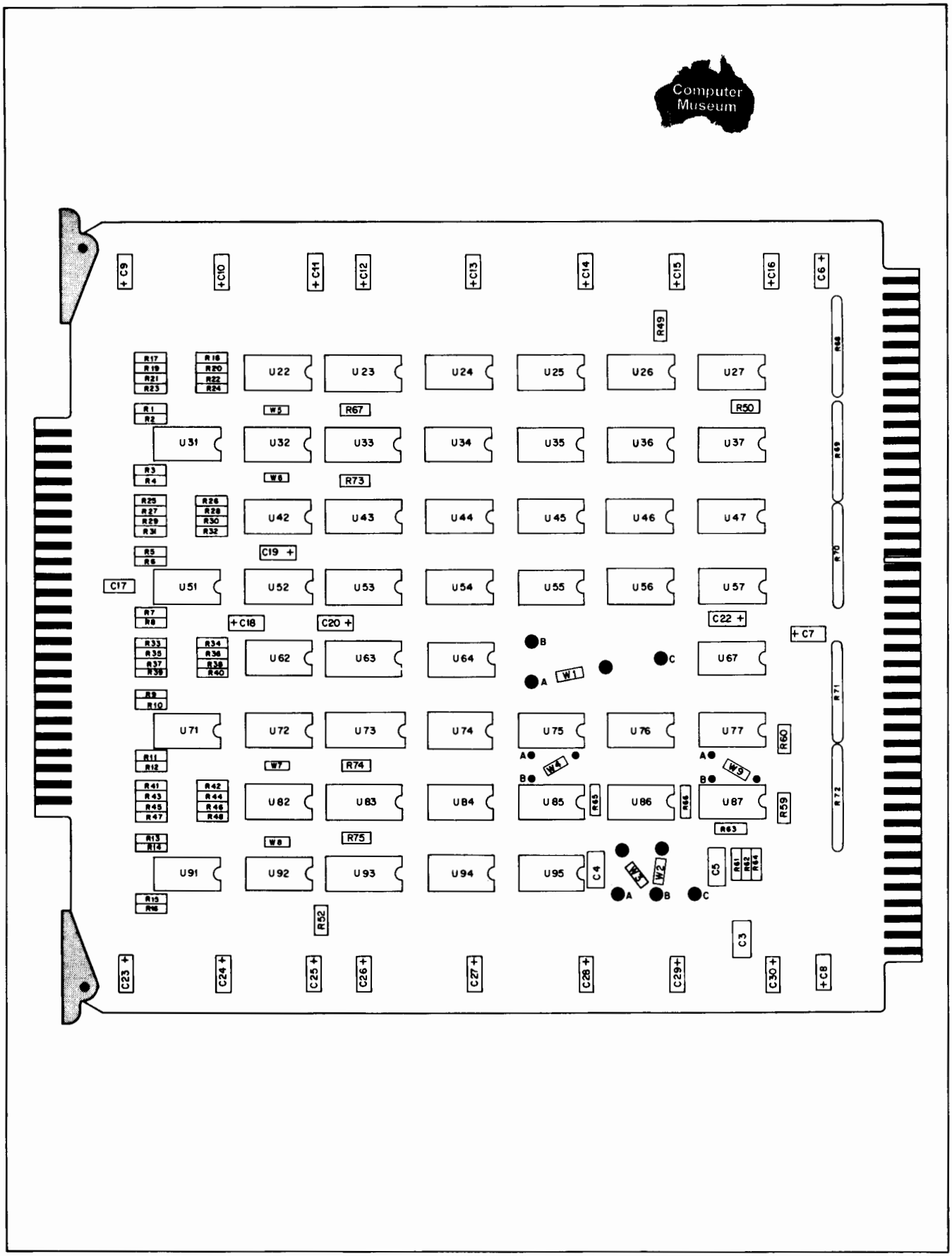


Figure 5-1. OMR-to-HP Computer Interface PCA (17200-60001)

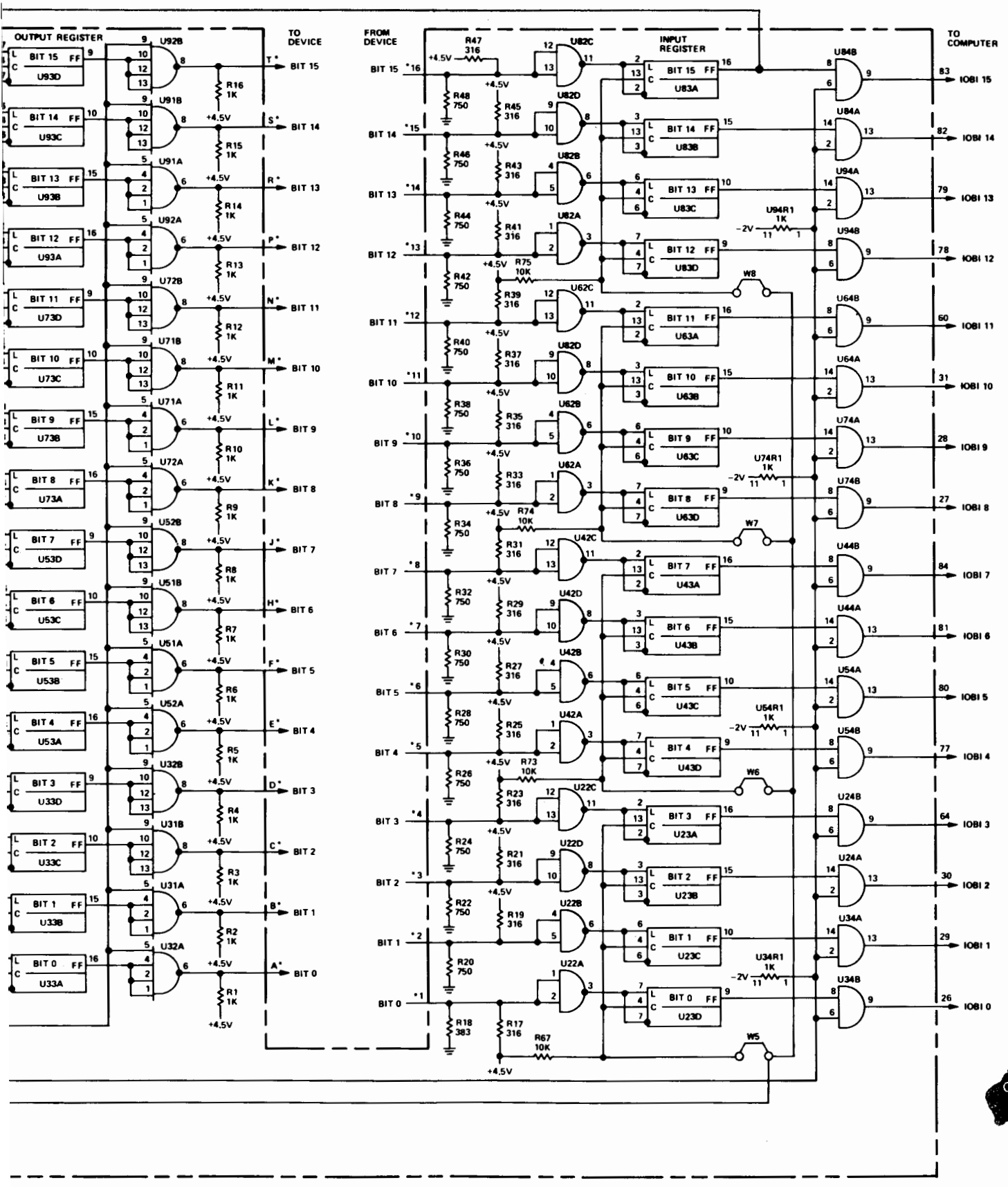
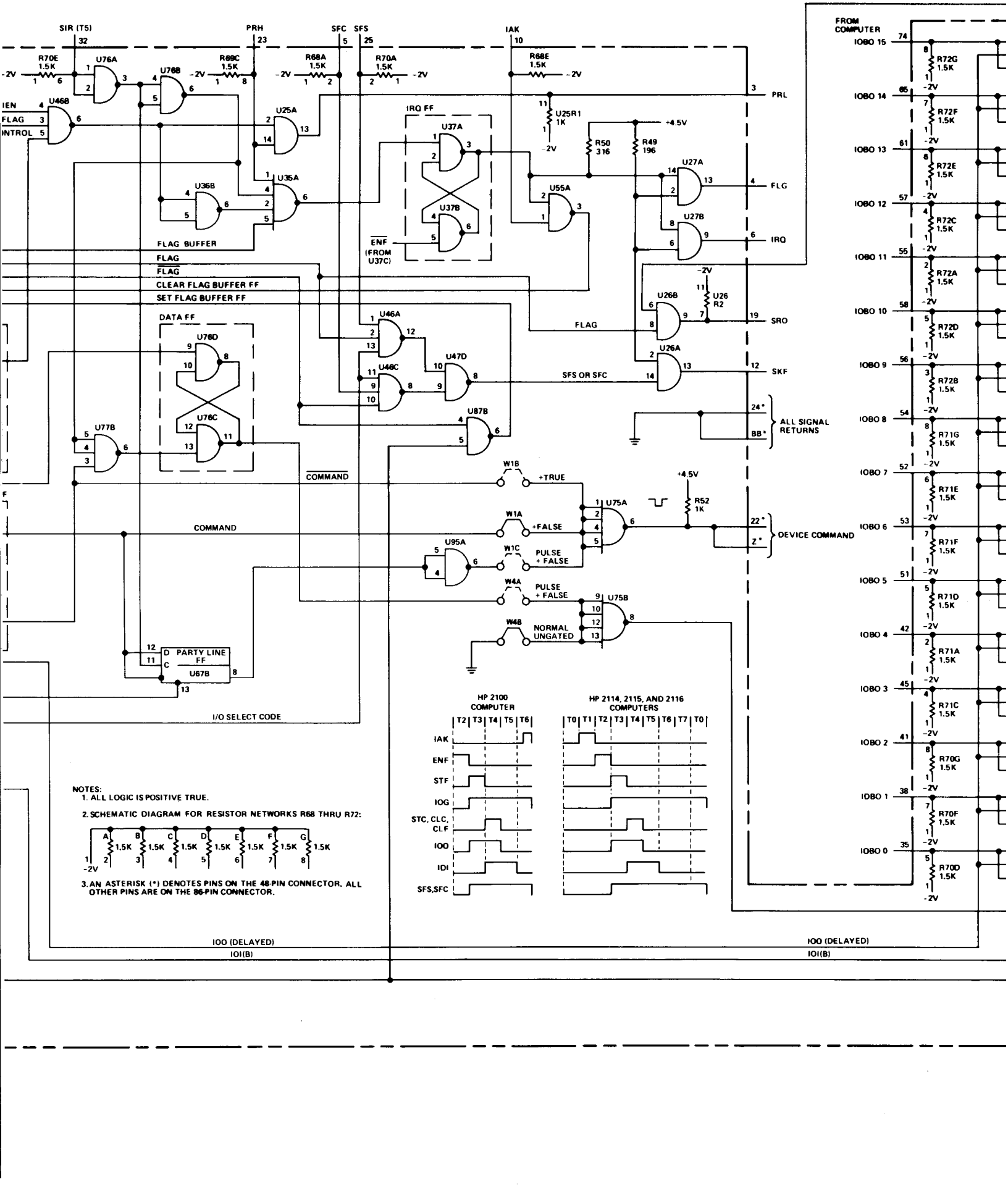
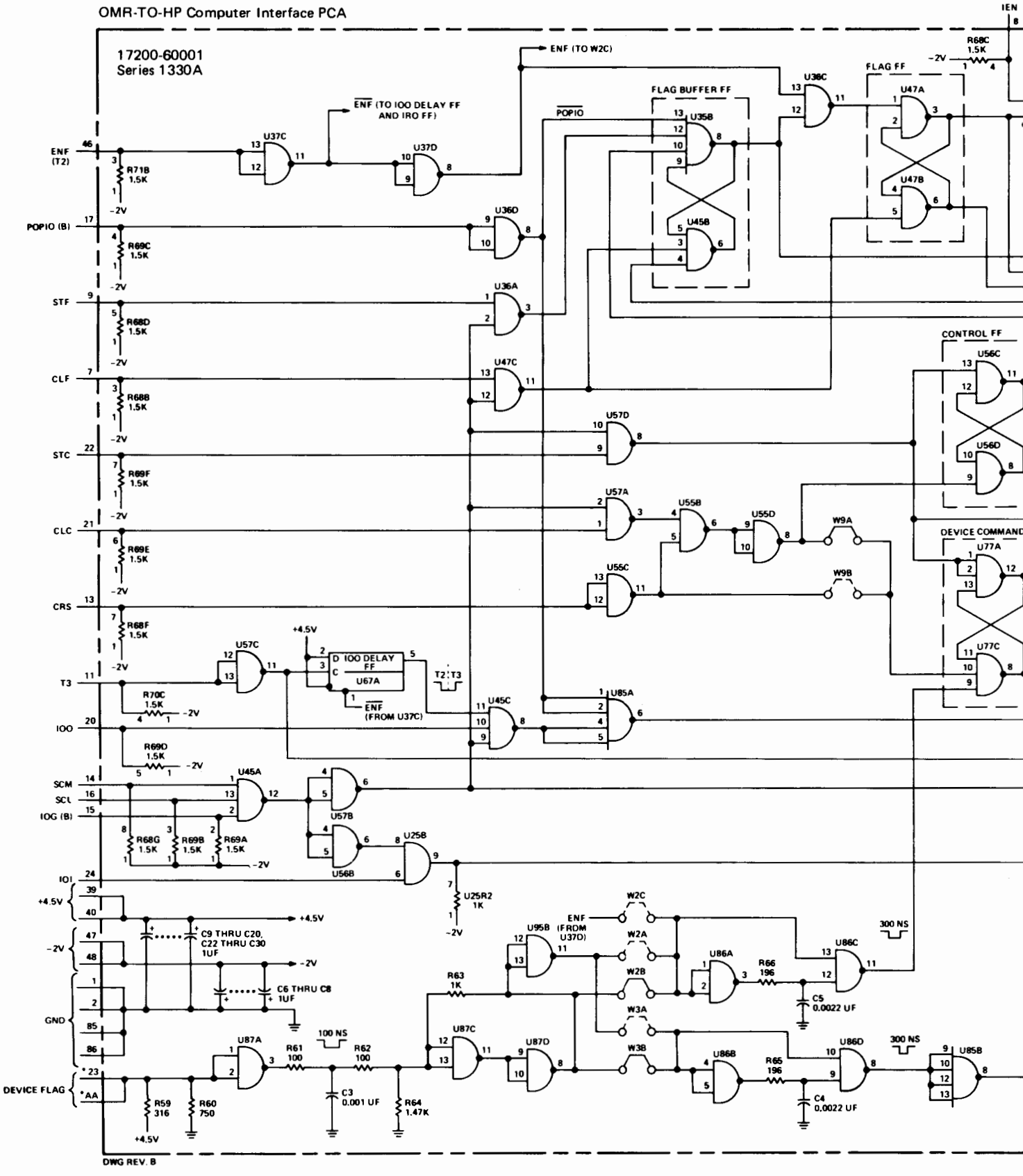


Figure 5-2. OMR-to-HP Computer Interface PCA Schematic Diagram



NOTES:
1. ALL LOGIC IS POSITIVE TRUE.
2. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R68 THRU R72:

3. AN ASTERISK (*) DENOTES PINS ON THE 48-PIN CONNECTOR. ALL OTHER PINS ARE ON THE 86-PIN CONNECTOR.


OMR-TO-HP Computer Interface PCA
17200-60001
Series 1330A
DWG REV. B
ENF (T2)
POPIO (B)
STF
CLF
STC
CLC
CRS
T3
IOO
SCM
SCL
IOG (B)
IOI
DEVICE FLAG
GND
+4.5V
-2V
ENF (TO W2C)
ENF (TO 100 DELAY FF AND IRO FF)
POPIO
FLAG BUFFER FF
FLAG FF
CONTROL FF
DEVICE COMMAND
100 DELAY FF U67A
ENF (FROM U37C)
ENF (FROM U37D)
T2
T3
C9 THRU C20, C22 THRU C30 1UF
C6 THRU C8 1UF
C3 0.001 UF
C4 0.0022 UF
C5 0.0022 UF
100 NS
300 NS
W2C
W2A
W2B
W3A
W3B
W9A
W9B

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