HEWLETT PACKARD

MEMORY CARDS
MODEL 69790B

OPERATING MANUAL

FOR SERIAL NUMBERS 2252A-01436 AND ABOVE.*

*For cards with serial numbers above 2252-01436, a manual change page may be included.

*For 69790B Memory Cards with serial numbers below 2252A-01436 and all 69790A Memory Cards, refer to Appendix A.

Manual Part No. 69790-90003
Microfiche Part No. 69790-90004

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CONTENTS

Section I
GENERAL INFORMATION

1-1 SCOPE OF MANUAL

1-2 This manual covers the installation, Pre-Operation, and Theory of Operation for the Model 69790B Memory Cards. Appendix A in the rear of this manual describes changes that must be made to the manual to make it applicable to Model 69790A Memory Cards. This manual does not include servicing instructions or information on the programming of the card. Programming examples for the Memory cards are shown in Chapter 7 of the 6942A Multiprogrammer User's Guide. Documents that describe specific Memory card applications (e.g. Buffered A/D) are also available. Table 1-1, Related Documentation, lists the HP part numbers for these documents and for additional publications that may be helpful to the Memory card user.

1-3 Any of the documents listed in Table 1-1 can be ordered directly from your local Hewlett-Packard sales office. Give the applicable HP manual part number as indicated in the table.

1-4 DESCRIPTION

1-5 The 69790B Memory provides 4,096 words of CMOS random access memory. Because CMOS memory chips are used, the total current drain is only 1.2A The 69790B Memory consists of two cards designated Card No. 1 and Card No. 2. The cards must be installed side-by-side in the mainframe with Card No. 2 in the higher slot address. A ribbon cable connects the two cards. Data and I/O control signals are routed to the external edge connector of Card No. 1.

1-6 The memory can communicate bidirectionally with the controller and with an external device connected to the edge connector on Card No. 1. External data transfers through 16 input or 16 output lines are controlled by three input or three output handshake lines. Special purpose Memory Input (MI) and Memory Output (MO) instructions allow data transfers to be made between the controller and a memory card assembly without storing the data in mainframe memory.

1-7 Up to eight sets of Memory cards can be installed in the 16 slots of a single 6942A or 6943A mainframe. In a system that contains more than one Memory card assembly, each assembly can handle data transfers to or from the outside world at the same time as the other assemblies.

1-8 The memory can be programmed to operate in one of four modes: FIFO (first-in, first out) Output, FIFO Input, Recirculating Output, or Recirculating Input.

1-9 The FIFO input mode allows an external data source to write on the card. The card can interrupt the computer when some or all of memory is full. This mode is used to gather data in bursts faster than the computer and Multiprogrammer can communicate. The FIFO input mode can improve system efficiency by collecting the data over extended periods of time and transmitting it in a block to the computer.

1-10 The FIFO output mode is used to send a single burst of data to another Multiprogrammer card or external device.

1-11 In the recirculating input mode, the Memory card acts like a circular buffer that an external device writes to continuously. When the memory is full, the external device writes over previously stored data, so that the memory always contains the most recent data. This mode is used when the external outputs of the 69751A Analog to Digital Converter are connected to the inputs of the Memory card for continuous data acquisition with history of up to 4096 readings.

Table 1-1. Related Documentation

Document	HP Part No.
6942A User's Guides:	
User's Guide for HP9825, 9835, and 9845 Controllers	06942-90003
User's Guide for HP85, 83, and 9915 Controllers	06942-90011
User's Guide for HP 9826 Controller	06942-90013
Programming Note: Supplemental Instruction Set for 6942A (Describes 8 new instructions, not covered in above user's Guides).	06942-90015
6942A Application Notes:	
AN316-1 Buffered A/D Conversions	5952-4072
AN316-2 Waveform Digitization	5952-4074
AN316-3 High Speed FET Scanning	5952-4073
6942A Technical Data	5952-4078
6942A Assembly Level Service Manual	06942-90006

1-12 In the recirculating output mode, an external device reads some or all of the memory repetitively. This mode is often used when the outputs of the Memory card are connected to the external inputs of the 69720A Digital to Analog voltage Converter to produce a repetitive analog waveform. A $\overline{\text{RECYCLED}}$ output pulse goes low each time the entire data list is read, and can be used to trigger an oscilloscope for observation of the waveform.

1-13 A lockout feature can be used to prevent an external device from reading or writing data. This feature is used to terminate the recirculating input and recirculating output modes, and can be used to prematurely terminate the FIFO input and FIFO output modes.

1-14 SPECIFICATIONS

1-15 Specifications and supplemental data for the Memory cards are given in Table 1-2.

Table 1-2. Specifications and Supplemental Data

Memory size: 4096 16-bit words
Two I/O slots required for each card pair.
Cycle Time: 8 μs (125 kHz)

Memory Data Output:
Logical 1 = 2.4 V minimum while sourcing 2.6 mA
Logical 0 = 0.5 V maximum while sinking 16 mA

Memory Data Inputs:
Inputs have 10 k ohm pull-ups to +5 volts
Logical 1 = 2.0 to 5.25 V
Logical 0 = 0 to 0.5 V

Input Data Available and Output Data Accepted
These inputs have 10 k ohm pull-ups to 5 V
Logical 0 = 2.0 to 5.25 V
Logical 1 = 0 to 0.5 V

Memory Full, Memory Empty, Recycled, Input Data Accepted, and Output Data Available:
High = 3.8 V minimum while sourcing 200 μA
Low = 0.4 V maximum while sinking 7 mA

Busy, EOP
High = 3.7 V minimum while sourcing 200 μA
Low = 0.5 V maximum while sinking 7 mA

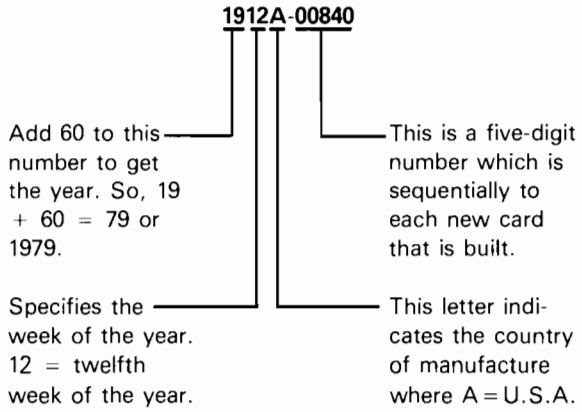
Temperature Range:
From 0 degrees to +70 degrees Centigrade operating in the mainframe (allows 15 degrees C internal rise in in temperature when operating in the mainframe at up to +55 degrees C ambient); From −40 degrees C to +80 degrees C storage.

Card Dimensions:
299.722mm x 132.08mm (11.8in. x 5.2in.)

+5 V Current Requirement:
.2A for both cards combined.

1-16 CARD AND MANUAL IDENTIFICATION

1-17 Hewlett-Packard I/O cards are identified by a two-part serial number. Each card (card no. 1 and card no. 2) comprising 69790B Memory is assigned the same serial number. This number appears on a label affixed to the circuit side of each card. The breakdown of the serial number is explained using the example number 1912A-00840.



1-18 The first part of this serial number (year and week) indicates the last date when a significant design change was made.

1-19 Each I/O card is equipped with a handle that is marked to identify the card type. The handle is located at the card's outer edge and facilitates the removal and installation of the card.

1-20 OPTIONS

1-21 To obtain additional Operating Manuals when the card is shipped, request Option 910 when ordering the card. One additional manual will be shipped with each Option 910 ordered.

1-22 ACCESSORIES

1-23 One external connector is shipped with each I/O card. Order model 14703A when extra connectors are required to fabricate cables for several different applications.

1-24 A deinsertion tool is available to remove the contact from the connector. This tool can be ordered from Hewlett-Packard (HP P/N 8710-0690).

Section II
INSTALLATION

2-1 INSPECTION

2-2 Before the Memory cards left our factory, they were inspected for electrical and mechanical flaws. As soon as you received them, check to make sure that they have not been damaged in shipment. If there is damage, report it to the carrier immediately, and notify the nearest HP Sales Office. Warranty information is printed on the inside cover of this manual. Save the shipping carton and packaging materials. You may need them to ship the card in the future. If the carton is lost, you can order a new one from an HP Sales Office. Ship the card only in a package designed for it. When you ship the card to an HP Service center for repairs, attach a tag to it identifying the owner. On the tag, give the model number and a brief description of the problem.

2-3 In addition to this Operating Manual, check that the following items have been received with the Memory cards:

- I/O card edge connector assembly (HP5060-2806). An instruction sheet that shows how to assemble the connector is provided with the I/O card edge connector assembly. This information is also available in Chapter 2 of the 6942A Multiprogrammer User's Guide.
- Operating Manual (HP 69790-90003) Change sheet. If applicable, one or more manual change sheets may be included with the manual. If a change sheet is included, check to see if the change applies to the serial number of the card you received.
- Ribbon cable assembly (HP69790-60001). The cable is properly connected between Card No. 1 and Card No. 2 before the cards are shipped from the factory.

2-4 INSTALLATION PREREQUISITES

2-5 Before you install the memory cards in a 6942A or 6943A chassis, consider the following:

a. Determine which I/O slots will be used. An I/O card can be installed in slots 0 through 15. The card assumes the address of the slot (and unit) in which it is inserted. Also, a card in slot 0 has the highest priority, slot 1 the next highest priority, and slot 15 the lowest.

NOTE

The memory cards must be installed side-by-side with Card No. 2 in the higher slot address.

b. For the slot positions selected, record the following:
   1. card type.
   2. card's address for Card No. 1 and Card No. 2, where;
      CARD ADDRESS = SLOT NO. + (FRAME NO. X 100) + (SUBADDRESS X 0.1)

      (For example, 205.0 is the card address for a card in slot No. 5, frame number 2, referencing subaddress 0 as in a write operation.)

c. Check that the mainframe power supply will not be overloaded if you are using 69790A cards (refer to Appendix A). There are no mainframe power supply overload considerations for 69790B cards.

2-6 "AS SHIPPED" JUMPER CONNECTIONS (Figures 6-1 and 6-3)

2-7 The memory cards contain jumpers that define the values of the wake-up codes and other jumpers that are used for factory test purposes. The card is shipped with jumpers set to specify the values listed below:

WAKE-UP CODES (on Card No. 2)

Data Type Code = 3 (Unsigned Binary Data) jumpers W24, W26 and W28 installed.
LSB Code = 1 (Unity) jumpers W21, W22, and W23 installed.

NOTE

To change any of these values, refer to Section III, Card jumpers, for further details.

TEST JUMPERS:

Card No. 1 – All the jumpers on Card No. 1 are used for factory test purposes.
Card No. 2 – On 69790B Memory cards, jumpers W1 through W17, and W30 are used for test purposes. On 69790A Memory cards, jumpers W17 and W30 are used for test purposes but W1 through W16 are memory size jumpers (see Appendix A).

2-8 INSTALLATION PROCEDURES

CAUTION

To prevent an accidental short from damaging a card or a mainframe, always turn off Multiprogrammer power before installing or removing I/O cards.

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2-9 As stated previously, the Memory cards must be installed in side-by-side slots (e.g. slot nos. 6 and 7) with Card No. 2 in the higher slot address. To install the cards in the mainframe chassis, perform the following steps:

a. Turn-off mainframe power.

CAUTION

Exercise care when inserting the in line connectors of the ribbon connector assembly. The connector pins will bend if they are not lined up with the sockets on Card No. 1.

b. Connect ribbon cable (see Figure 2-1) to Card No. 1. Cable connectors P3 and P4 mate with sockets J3 and J4, respectively on Card No. 1 (see Figure 6-1).
c. Remove the rear cover of the mainframe by loosening the four quarter-turn fasteners.
d. Position the card so its handle is at the bottom, with the components toward the right.
e. Slide Card No. 1 into the desired slot position until the card just touches the backplane connector.

NOTE

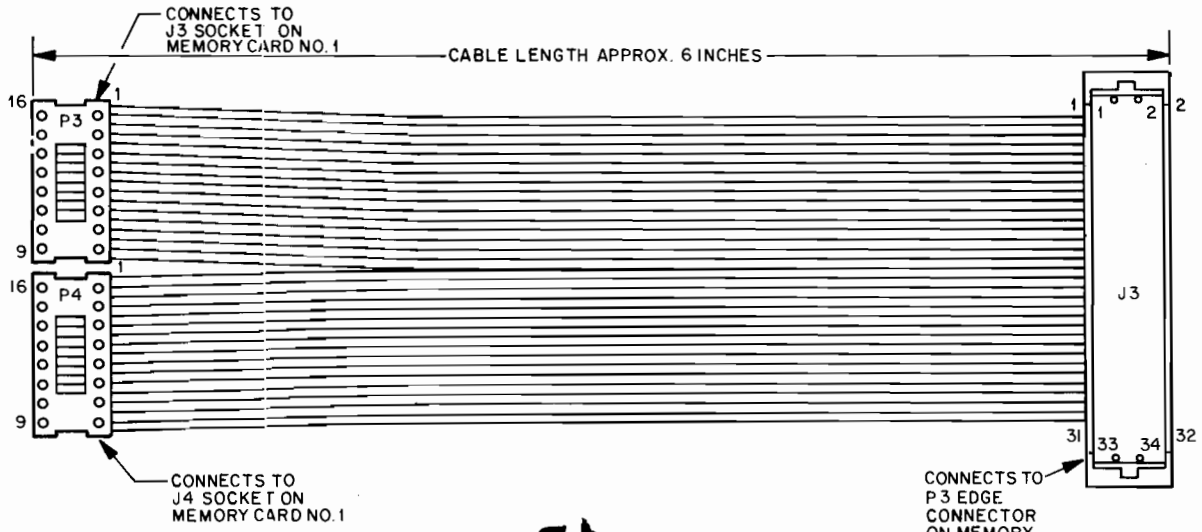
A notch in the card edge and a key in the connector prevent the card from being installed upside down or in an illegal slot position.

f. With the card touching the connector, rotate the card handle downward until it engages the groove at the bottom of the I/O slot. Rotate the handle upward to insert the card into the backplane connector.
g. Install Card No. 2 in next higher slot address by repeating steps d through f.
h. Connect ribbon cable connector J3 to edge connector P3 on Card No. 2 (see Figure 6-3).
i. Replace mainframe rear cover.
j. Perform one or both of the tests described in the next paragraph.

2-10 FUNCTIONAL CHECKOUT

2-11 After the cards are installed, you can run either of two self tests described in the 6942A Multiprogrammer User's Guide. These tests are:

a. The Self-Test Error Detection and Card Identifier Utility Program. This test is described in Chapter 2 of the 6942A Multiprogrammer User's Guide. This test checks the card control chip and the first rank storage register and the first 1k of Memory.
b. Examples 7-42 through 7-47 in Chapter 7 of the 6942A User's guide can be run to test the operation of the Memory Cards in each mode of operation.



RIBBON CABLE WIRING

FROM CARD NO. 1	TO CARD NO. 2	SIGNAL	FROM CARD NO. 1	TO CARD NO. 2	SIGNAL
P3-16	J3-1	A1	P4-16	J3-17	EOP
P3-1	J3-2	A0	P4-1	J3-18	$\overline{\text{IRQ}}'$
P3-15	J3-3	A3	P4-15	J3-19	CLR
P3-2	J3-4	A2	P4-2	J3-20	ARM′
P3-14	J3-5	A5	P4-14	J3-21	EOR′
P3-3	J3-6	A4	P4-3	J3-22	$\overline{\text{CLR}}'$
P3-13	J3-7	A7	P4-13	J3-23	$\overline{\text{T14}}$
P3-4	J3-8	A6	P4-4	J3-24	CLRR
P3-12	J3-9	A9	P4-12	J3-25	$\overline{\text{T12}}$
P3-5	J3-10	A8	P4-5	J3-26	$\overline{\text{ENR}}$
P3-11	J3-11	A11	P4-11	J3-27	$\overline{\text{END}}$
P3-6	J3-12	A10	P4-6	J3-28	INC W
P3-10	J3-13		P4-10	J3-29	INC R
P3-7	J3-14	+5 V	P4-7	J3-30	ALL 0's
P3-9	J3-15	ENW	P4-9	J3-31	">"
P3-8	J3-16	$\overline{\text{RECYCLED}}$	P4-8	J3-32	ALL 1's
			–	J3-33	NOT USED
			–	J3-34	NOT USED

Figure 2-1. Memory Card Ribbon Cable HP Part No. 69790-60001

Section III
PRE-OPERATING INSTRUCTIONS

3-1 INTRODUCTION

3-2 This section contains information on programming the Memory cards' subaddresses, changing the "wake-up" code jumpers, and using the external I/O control signals. The subaddress information explains the function of each subaddress, the operating modes, and the instructions that affect each card (No. 1 and No. 2). The jumper information allows the user to change the data type and LSB wake-up values. The function of each I/O control signal is described to aid the user in making connections to other I/O cards and/or external devices.

3-3 PROGRAMMING THE MEMORY CARDS' SUBADDRESSES

3-4 General

3-5 The Multiprogrammer utilizes an I/O card subaddressing scheme which facilitates programming multifunctioned I/O cards. Four subaddresses are provided for writing data into an I/O card and for reading data from an I/O card. An output instruction, such as a Write First Rank (WF), can be used to write data to a subaddress while an input instruction, such as Read Value (RV), can be used to read data from a subaddress. Memory Card No. 1 uses two (sub 0 and 1) of the write subaddresses and one (sub 0) of the read subaddress. Memory Card No. 2 utilizes all four of the write subaddresses (0-3) and all four of the read subaddresses. The appropriate subaddress number is appended to the card slot number in the instruction syntax. The write subaddresses are programmed using positive decimal numbers and the read subaddresses return positive decimal numbers.

3-6 The 69790B cards' subaddress registers are illustrated in the functional block diagram of Figure 3-1. Table 3-1 gives a brief functional description of each subaddress and the range of values associated with each subaddress. The following paragraphs give a brief description of the operating modes and the instructions that are used to program Card No. 1 and Card No. 2. Detailed programming instructions are provided in the applicable User's Guide (see Table 1-1). Section IV in this manual provides the theory of operation for the subaddress registers on each card and describes the various modes of operation in greater detail.

3-7 Modes of Operation

3-8 As shown in Figure 3-1, memory and mode control circuits are located on Card No. 1. The modes of operation that can be programmed via the mode register are: FIFO input, FIFO output, recirculating input, recirculating output, and external lockout.

- FIFO input mode is used to read and store a list of data words from an external device in the order that the data is received and to allow the controller to read this data in the same order.
- FIFO output mode is used to send a list of data words from the controller to the Memory card and to transfer this list from the Memory cards to an external device in the same order that the data was received.
- Recirculating input mode is used by the controller to read data from selected memory locations on the card. It is also used to read and store data words from an external device into selected locations on the card.
- External lockout mode is usually used in conjunction with one of the other four modes to prevent an external device from reading or writing on a memory card.

3-9 When operating in either of the basic operating modes, FIFO input or FIFO output, and automatic lockout feature prevents data from being overwritten before it has been read or prevents data from being read that has not yet been updated. This is acomplished through the use of a read counter, a write counter, and a differential counter located on Card 2. At all times, the read counter contians a number representing the next memory location to be read, and the write counter contains a number representing the next memory location to be written to. After each read or write takes place, the appropriate counter is incremented by one. In the FIFO input and FIFO output modes, the differential counter contains the difference between the read and writer counters and thus contains the number of memory locations that have been written to but not yet read. An automatic lockout protection feature is provided in both FIFO modes. This lockout feature will prevent an external device from writing over data that has not been read by the controller in the input mode and will prevent the controller from writing over data that has not been taken by the external device in output mode.

3-10 An automatic lockout occurs when the differential counter on Card No. 2 indicates that the memory is empty or full. The effect of an automatic lockout depends upon the card's operating mode.

In the FIFO input mode, an automatic lockout:

1. inhibits the input handshake lines when the memory is full, and
2. causes the card to repeatedly return the value of the word in the current memory location in response to the controller's attempts to read from the card when memory is empty.

Table 3-1. Memory Card Subaddresses

MEMORY CARD	Subaddress	Write Function	Read Function
No. 1	0	Used to send data from the controller to the Memory Card. The card must be in the output mode and the data values must be decimal integers between 0 and 65,535 (see Note 1).	Used to read data from the Memory Card to the controller. The card must be in the input mode and the data values read are decimal integers between 0 and 65,535 (see Note 1).
	1	Used to set operating mode of Memory Cards. Values that can be sent are: 1 = FIFO input mode, no external lockout (Memory Cards "wake-up" with this mode in effect). 21 = FIFO input mode with external lockout 2 = FIFO output mode, no external lockout. 22 = FIFO output mode with external lockout 4 = Recirculate input mode, no external lockout 24 = Recirculate input mode with external lockout 10 = Recirculate output mode, no external lockout 30 = Recirculate output mode with external lockout	N/A
No. 2	0	Used to set reference register to a value from 0 to 4095.	Use to read the value (0 to 4095) in the read counter.
	1	Used to set differential counter to a value from 0 to 4095 (see Note 2).	Used to read the value (0 to 4095) in the differential counter.
	2	Used to set write counter to a value from 0 to 4095 (see Note 2).	Used to read the value (0 to 4095) in the write counter.
	3	Used to set read counter to a value from 0 to 4095 (see Note 2).	Used to read the value (0 to 4095) in the read counter.

NOTES:

1. If you prefer to use a different data format (e.g. 12 or 16-bit two's complement) you may use a Set-Format (SF) instruction to reformat Card No. 1 or permanently select a different format by changing the data type and LSB wake-up code jumpers on Card No. 2 (see paragraph 3-27).

2. Whenever the value in the write or read counters is changed, the differential counter must be programmed to the difference between the values of the read and write counters before returning to operation in the FIFO mode from the recirculate mode.

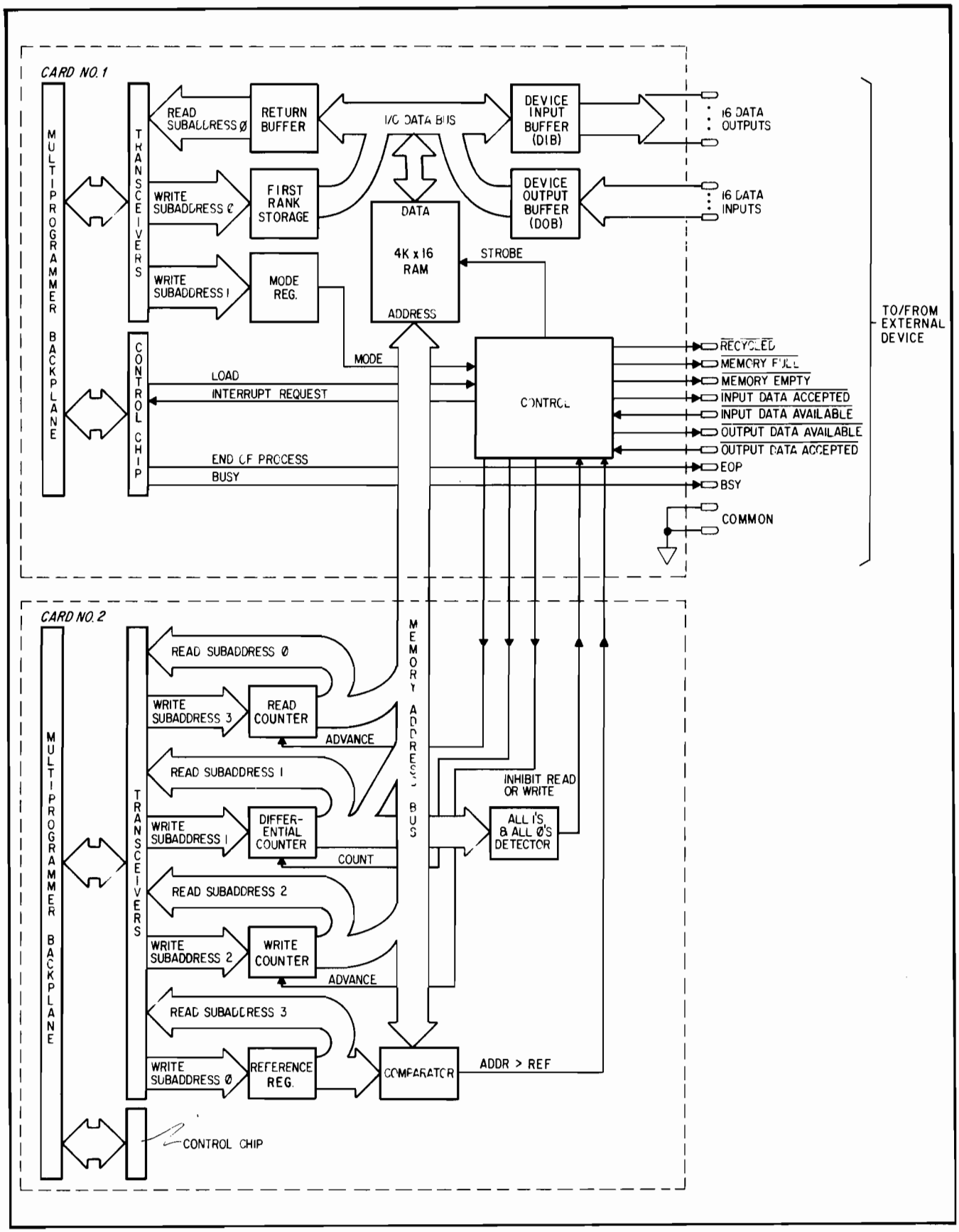


Figure 3-1. 69790B Memory, Block Diagram

In the FIFO output mode, an automatic lockout:

1. inhibits the output handshake lines when the memory is empty, and
2. causes the card to ignore the controllers attempts to write to the card when memory is full.

3-11 The reference register on Card No. 2 can be used in the FIFO input and FIFO output modes to cause the card to generate an interrupt when the number of unread words has increased or decreased to or beyond a specified number. In the FIFO input mode, an armed Memory card interrupts when the number of words stored but not read exceeds the value in the reference word register. In the FIFO output mode, an armed Memory card interrupts when the number of words that remain to be read becomes equal to or less than the value in the reference word register. (The reference register has no function in the recirculate input mode. Its function in the recirculate output mode is described in Paragraph 3-15).

3-12 In any operating mode, FIFO input, FIFO output, recirculating input, or recirculating output, it is possible to program a lockout of just the external interface or to restore it to normal operation. A programmed lockout inhibits the input and output handshake lines.

3-13 The card's operating mode and the status of the programmable lockout of its external interface are both controlled by the data value stored in a mode register on Card 1. At system turn-on or following a Clear Card (CC) instruction (which must be addressed to Card 2), the card is set to the FIFO input mode with no external lockout programmed. The FIFO input or FIFO output mode is automatically selected by programming an MI or MO instruction. Alternately, either of these modes or the recirculate input or recirculate output mode can be established by writing an appropriate value to the mode latch. Four additional data values can be written to the mode latch, each of which combines an external lockout with one of the four operating modes. The card's operating mode and the status of the external lockout remain unchanged until they are reprogrammed by one of these methods.

3-14 There are two primary differences between the way the Memory card functions in the recirculate input and output modes and the way it functions in the FIFO input and output modes. The first is that the automatic lockouts described in Paragraph 3-10 do not function in the recirculate modes. There is nothing to prevent data which has not been read from being written over. As a result, in the recirculate input mode, the memory is continuously written over time after time until one of the following steps is taken: 1) the external data source is stopped, 2) an external lockout of the Memory card is programmed, or 3) the Memory card is programmed to one of its output modes.

3-15 The second difference between FIFO and recirculate operation is that no interrupt can be programmed in the recirculate modes. Instead of controlling the card's interrupt, the data value written to the reference register truncates the size of the memory in the recirculate output mode. In this mode, the external device reads a sequence of words from the word stored in memory location zero to the word stored in the memory location designated by the value in the reference word register, and then continues reading by starting again from word zero. When operating in this mode, which is used to produce a continuously repeating cycle of output words, an output pulse is produced at the **Recycled** terminal of the Card No. 1 edge connector each time the cycle repeats. If the sequence of output words is converted to analog waveform, the **Recycled** pulse can be used to synchronize its display. **Recycled** pulse is produced if the reference word register is loaded with the value of the last available memory location so that memory is not truncated.

3-16 Because proper operation in the FIFO input or output mode depends on the differential counter's containing the difference between the read and write counters, it is always necessary to program the differential counter to equal this difference before returning to one of the FIFO modes from one of the recirculate modes. The usual way to match the differential counter to the difference between the pointers is to program a Clear Card instruction to Card No. 2, which clears all three to zero, but remember that a Clear Card instruction also sets the card to the FIFO input mode.

3-17 Card No. 1 Instructions

3-18 Memory Input (MI) and Memory Output (MO) instructions are addressed to subaddress 0 on Card No. 1. The 4 k x 16 RAM is located on Card No. 1.

3-19 The MO instruction loads a block of data from the controller directly into a memory card. This instruction sets the card to the FIFO output mode. After each data transfer, the card is cycled by advancing the write counter to the next memory location. While the card is in an output mode, its output handshake lines are enabled and its input handshake lines are inhibited. Other types of output instructions, such as a WC instruction, can also be used to transfer data from the controller into a memory card provided that the card is in the FIFO output mode.

3-20 The MI instruction sets the Memory card to the FIFO input mode and specifies the slot address of the Memory card which will be read. The MI instruction links the addressed memory card to extended talk address 05. (The card will remain linked to extended talk address 05 until another MI instruction selects another card.) Data words from the card can then be read via extended talk address 05 into an array or a list of controller variables. The read counter is advanced after each data transfer. Cycling the card in this mode advances the read pointer. The contents of the memory location currently indicated by the read pointer can be read without advancing the pointer by using a Read Value (RV) instruction addressed to subaddress 0 on Card 1. While the card is in an input mode, its input handshake lines are enabled and its output handshake lines are inhibited.

3-21 An MI instruction can include a word count data value that causes the Multiprogrammer to send the controller a carriage return/line feed each time that number of words has been transferred. The inclusion of the word count in an MI instruction is optional for the Multiprogrammer but required by some controllers. See Chapter 6 of the 6942A User's Guide for further information.

3-22 The value in the mode register on Card No. 1 determines the operating mode. Other than by using an MI or MO instruction, the mode register is loaded by addressing a Write First Rank (WF) instruction to subaddress 1 on Card 1.

A Read Format (RF) instruction, addressing Card No. 1, is used to read the card format (card ID, data type, LSB, size, limit). A Set Format (SF) instruction, addressing Card No. 1, can be used to change the card's format (see Paragraph 3-27).

3-23 Card No. 2 Instructions

3-24 The four subaddresses on Card No. 2 can be written to and read from by using Write First Rank (WF) and Read Value (RV) instructions, respectively. These subaddress registers accept and return decimal values. Only three of them are initialized to zero at system turn-on or are cleared by a Clear Card (CC) instruction addressed to Card 2. The read counter, write counter, and differential counter are initialized or cleared but the reference register is not. (After turn-on, the reference register contains the last data value written to it during the system self-test.)

3-25 Data values can be loaded into the read counter or write counter in order to cause subsequent read or write operations to commence at a particular memory location. The differential counter can be loaded with the difference between the values read from the read and write counters, or its value can be read in order to know how many words remain to be taken by the controller or how many empty locations remain to be filled. (If setting up the differential counter to contain the difference between the read and write pointers, it may be necessary to have an external lockout programmed between the time of reading the pointers and of loading the differential counter.) The reference register is used to specify an interrupt point during FIFO input or FIFO output operation or to truncate memory while in the recirculate output mode.

NOTE

The reference register will accept a 16-bit quantity without generating an error, but only the lower-order 12 bits are used or can be read back by the controller.

3-26 The remaining instructions that must be addressed to Card 2 of a memory card pair are 1) the Arm Card (AC) instruction, which arms the card for an interrupt; 2) the Disarm Card (DC) instruction, which disarms it; and 3) the Read Status (RS) instruction, which allows the controller, by reading extended talk address 08, to determine whether the card is armed, whether it is busy, and whether its EOP (End of Process) signal is true. The memory card is defined as being busy if its differential counter is not at zero. Its EOP signal is true in the FIFO input mode when the differential counter's count is greater than the quantity in the reference register. EOP is true in the FIFO output mode when the counter is equal to or less than the quantity in the reference word register. EOP is never true in the recirculate output mode. When a memory card assembly interrupts, it is Card 2 of the assembly that sets $\overline{IRQ}$ and is recognized as the interrupt card.

3-27 WAKE-UP CODE JUMPERS (FIGURE 6-3)

3-28 These jumpers, located on Card No. 2, determine the data type and LSB wake-up codes that are read from the card and stored in Multiprogrammer system memory after power turn on. These codes determine how the Multiprogrammer will process the data it sends to or receives from the subaddresses on Memory Card No. 1. The user can override the values stored in system memory by using a Set Format (SF) instruction addressing Card No. 1. This is useful in applications that require a data format code or LSB value different from the values set at the factory. Any of the data types of Table 3-2 can be used. Programmed LSB values are not limited to those in Table 3-3. Any desired LSB value between 0.001 and 65.535 can be programmed. This allows the user to express programmed data in units appropriate to the process to which the card is dedicated.

3-29 If a new data type or LSB code will always be used, the jumpers on the card can be changed to reflect these new codes. This is more efficient than having the software constantly override the factory set values.

3-30 Data Type Code

3-31 Jumpers, W24 through W29 specify the data type code sent to the Multiprogrammer as part of the wake-up code sequence. Card No. 2 is shipped with jumpers W24, W26, and W28 installed and jumpers W25, W27 and W29 removed. The Multiprogrammer interprets these jumpers as data type code = 3 unsigned binary.

3-32 These jumpers can be changed to specify a different data type code. For example, data type code = 7 could be selected to program a bit pattern in octal form. Table 3-2 shows which jumpers must be in and which jumpers must be removed to select other data type codes.

3-33 LSB Codes

3-34 Card No. 2 is shipped with LSB code jumpers W21, W22, and W23 installed and W18, W19 and W20 removed. These jumpers specify a LSB code 1 (unity). Table 3-3 shows the other valid LSB Codes and required jumpers.

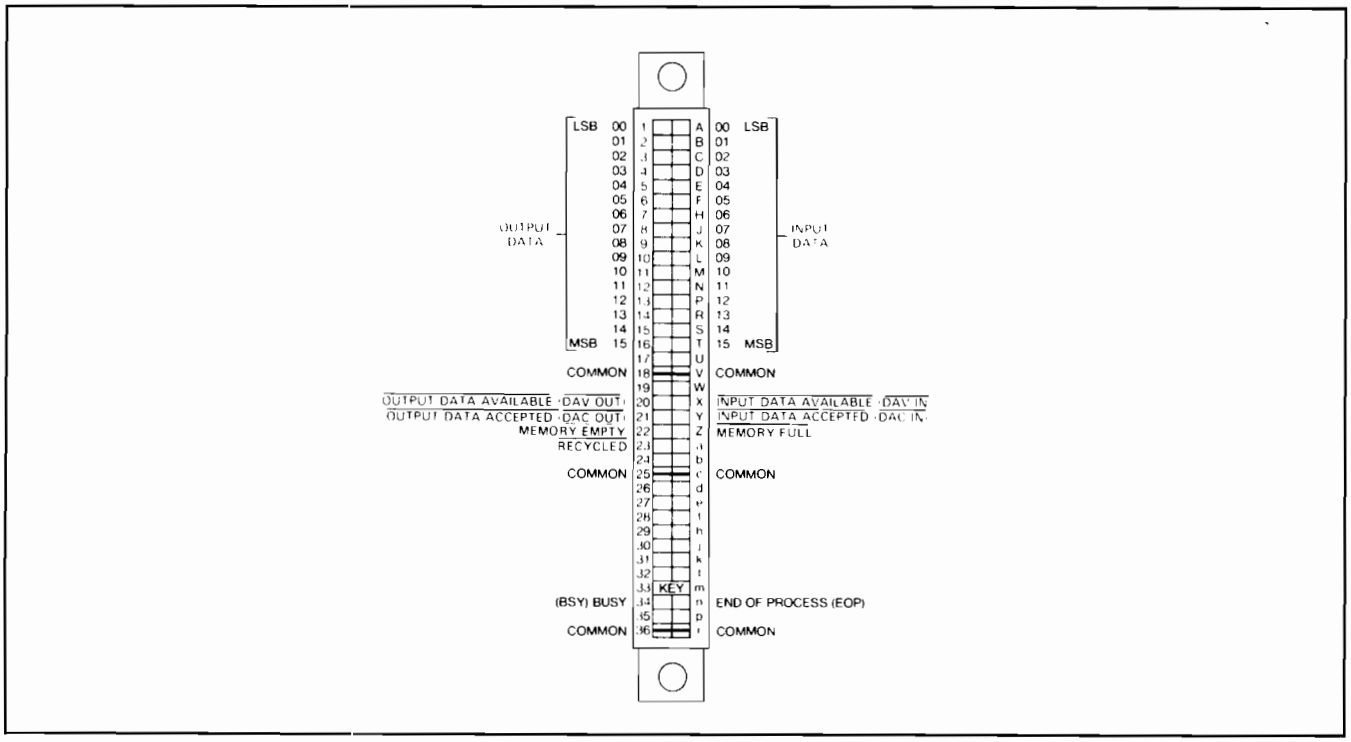


Figure 3-2. Memory Card No. 1, External Edge Connector

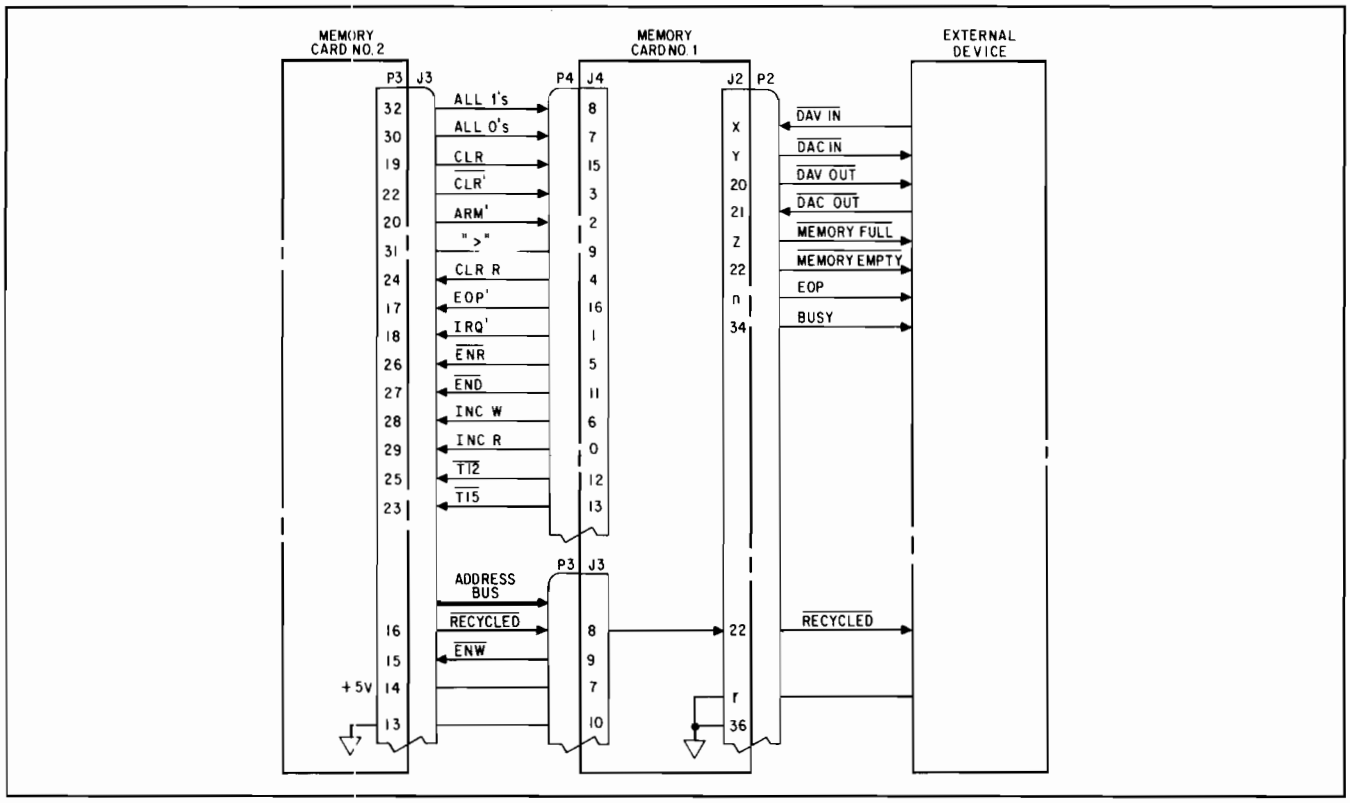


Figure 3-3. External I/O Control Signals

3-35 EXTERNAL I/O CONTROL SIGNALS

3-36 One dual 36-pin connector is supplied with each I/O card for interfacing field wiring to the card. Instructions for making up the mating connector and hood assembly are provided in Chapter 2 of the 6942A User's Guide. The pin assignments of the input and output signals available at the Card No. 1 external edge connector are shown in Figure 3-2. (The lettered pins are on the component side of the card).

3-37 Table 3-4 describes the control signals which interconnect between the Memory Card No. 1 and the Customer's equipment. The electrical specifications for these signals are given in Table 1-1 of Section 1. The direction of the control flow between the Memory Cards and the external equipment is shown in Figure 3-3.

Table 3-2. Data Type Code Jumpers

DATA TYPE CODE	DESCRIPTION	JUMPER ARRANGEMENT					
		W29	W28	W27	W26	W25	W24
1	Programmed positive or negative number is is stored on card in two's complement form.	Out	Out	Out	In	In	In
2	Programmed positive or negative number is stored on card in sign-magnitude form.	Out	Out	In	In	In	Out
3*	Programmed positive number is stored on card in unsigned binary form.	Out	In	Out	In	Out	In
4	(Special Autorange Code Used only with 69736A Timer/Pacer Card)	–	–	–	–	–	–
6	Programmed positive number is stored on card	In	Out	In	Out	In	Out
7	Programmed octal integer is stored on card in unsigned binary form.	In	In	Out	Out	Out	In

* When the card is shipped, its jumpers are arranged to select the starred data type when power is applied to the system.

Table 3-3. LSB Code Jumpers

LSB CODE	LSB VALUE	JUMPER ARRANGEMENT					
		W23	W22	W21	W20	W19	W18
0	0.001	Out	Out	Out	In	In	In
1	0.025	Out	Out	In	In	In	Out
2	0.1	Out	In	Out	In	Out	In
3	0.5	Out	In	In	In	Out	Out
4	0.01	In	Out	Out	Out	In	In
5	0.05	In	Out	In	Out	In	Out
6	0.005	In	In	Out	Out	Out	In
7*	1.0	In	In	In	Out	Out	Out

* When the card is shipped, its jumpers are arranged to select the starred LSB value when power is applied to the system.

Table 3-4. External I/O Control Signals.

I/O Control Signal	Pin No.	Description
$\overline{\text{DAV OUT}}$	20	This line goes low whenever memory contains a data word that has not been read by the device.
$\overline{\text{DAC OUT}}$	21	This line is set low by the device to acknowledge receipt of the data word just read by the device.
$\overline{\text{DAV IN}}$	X	Device sets this line low to transfer a data word to the DOB buffer in memory.
$\overline{\text{DAC IN}}$	Y	Memory sets this line low to acknowledge that memory has received a data word from the device.
$\overline{\text{MEMORY FULL}}$	Z	Goes low during FIFO input mode when the ALL 1's signal is high. This means that the top of memory has been reached. Goes high when ALL 1's signal is low, or during any mode other than FIFO input.
$\overline{\text{MEMORY EMPTY}}$	22	Goes low during FIFO output mode when the ALL 0's signal is high. Goes high when ALL 0's signal is low, or during any mode other than FIFO output.
BUSY also BSY	34	Refer to Paragraph 4-69 in Section IV.
END-OF-PROCESS also EOP	n	Refer to Paragraph 4-71 in Section IV.
COMMON	r, 36	Signal return for all control signals and data lines.

Section IV
THEORY OF OPERATION

4-1 INTRODUCTION

4-2 This section explains the theory of operation for the 69790B Memory Cards. It is assumed that the reader is familiar with the instruction set and operation of the 6942A Multiprogrammer. The Memory can operate in one of four modes as described briefly in Section III. A detailed explanation of each mode is deferred until a later paragraph in this section entitled "Models of Operation." First, it is important for the reader to be familiar with the functional organization of memory and with programming the cards.

4-3 MEMORY ORGANIZATION

4-4 Figure 4-1 shows the basic functions of each memory card. As mentioned in Section II, the two memory cards can be installed in any slots in the mainframe, but the two cards must be located side-by-side with card 2 in the higher slot address. The convention of referring to the memory cards as card 1 and card 2 will be used throughout this section.

4-5 Write Counter

4-6 The write counter is loaded with a 12-bit address word, which acts as a pointer to the next memory location to be written with data. Initially, the write counter is loaded with the first address (usually 0) to be written. Thereafter, as each data word is written to memory, the counter is automatically incremented by one.

4-7 Under certain conditions, the writer counter can be prevented from incrementing. For example, when the counter reaches the top of memory. These conditions are discussed in later paragraphs on "Programmmed Lockout" and "Memory Full".

4-8 To load the write counter with an address, use a WF instruction with subaddress 2, and reference the slot address of card 2.

"WF, slot.2,address T"

To read the address word in the write counter, use an RV instruction with subaddress 2, and reference the slot adress of card 2.

"RV, slot.2T

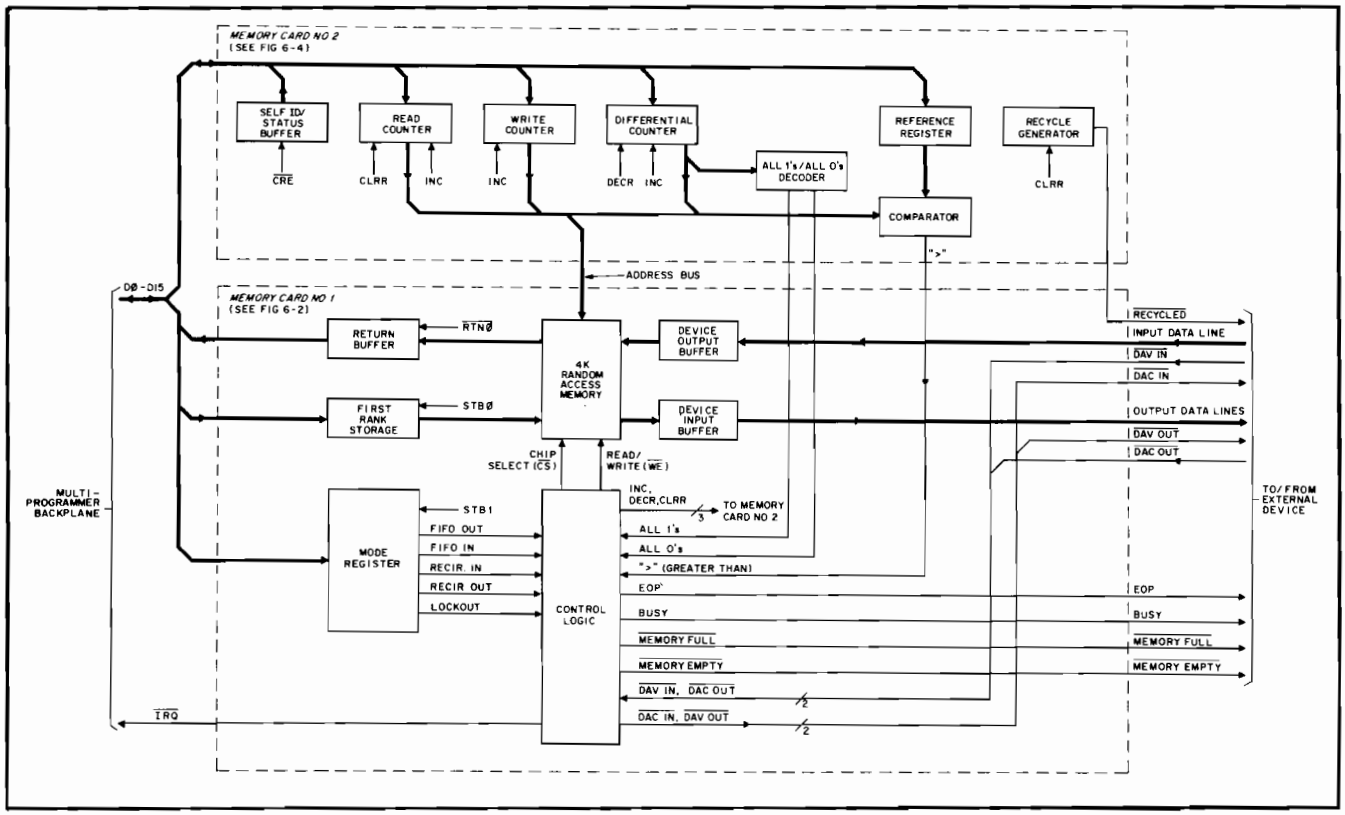


Figure 4-1. 69790B Memory Organization

4-9 Read Counter

4-10 The read counter is loaded with a 12-bit address word, which acts as a pointer to the next memory location to be read. Initially, the read counter is loaded with the address of the first memory location (usually 0) that was written with data. The read counter is automatically incremented after each data word is read from memory.

4-11 Under certain conditions the read counter can be prevented from incrementing, so that any attempt to read data from memory results in the last data word read being returned again and again. Refer to later paragraphs on "Programmed Lockout" and "Memory Empty" for these conditions. During the recirculate Output mode, the read counter is automatically set (or recycled) to zero when the top of memory is reached. This action is explained in the paragraph entitled "Recirculate Output Mode".

4-12 To load the read counter with an address word, use a WF instruction with subaddress 3, and reference the slot address of card No. 2.

"WF, slot.3, address T"

To read the read counter, use an RV instruction with subaddress 0, and reference the slot address of card 2.

"RV, slot.0, T"

4-13 Differential Counter

4-14 The differential counter is used only in the FIFO input and FIFO output modes. It has no application in recirculate modes. The purpose of the differential counter is to keep track of the number of words that have been written to memory but have not yet been read. The differential counter must be set to the difference between the write and read counters before initiating any write or read operation.

Differential Counter = Write Counter – Read Counter

4-15 The value in the differential counter is always an integer value. During read and write operations the differential counter is incremented by one when the write counter is incremented and decremented by one when the read counter is incremented.

4-16 Decoder circuits associated with the differential counter constantly monitor the value in the differential counter.

a. If the value becomes zero (0), an ALL 0's line goes high.
b. If the value becomes all ones, an ALL 1's line goes high.

4-17 The significance of the ALL 1's and ALL 0's conditions will be discussed later in this section. A CC instruction can be used to clear the differential counter to zero. Since CC also clears the read and write counters, it can be used to set all three counters to zero at one time.

4-18 To load the differential counter with an integer value, use a WF instruction with subaddress 1, and reference the slot address of card 2.

"WF, slot.1, value T"

To read the value in the differential counter use subaddress 1, and reference the slot address of card 2.

"RV, slot.1, T"

4-19 Reference Register

4-20 The reference register is used in all modes of operation except in the recirculate input mode. Prior to a read or write operation, the reference register is loaded with a 12-bit word, which, depending on the mode of operation is either:

- an integer value for either the FIFO input or FIFO output modes, or
- an address word for the recirculate output mode.

4-21 Once the Reference Register is loaded, the value is not altered. The value is not incremented or decremented like the other counters. The Clear Card instruction does not clear the reference register.

To load the reference register with an integer or address value, use a WF instruction with subaddress 0, and reference the slot address of card 2.

"WF, slot.0, value T"

To read the value in the reference register, use an RV instruction with subaddress 3, and reference the slot address of card 2.

"RV, slot.3, T"

4-22 Self-ID/Status Buffer

4-23 When the Multiprogrammer performs a self test, or when the controller issues a Read Status (RS) instruction, card No. 2 returns a 16-bit status word to the Multiprogrammer. This word contains information on the operational status (BUSY, EOP, and ARM flags) of the card and shows how the card is configured. The status word is discussed in more detail in the detailed block diagram description.

4-24 Comparator

4-25 The comparator is not programmable. During the FIFO output or FIFO input mode, the content of the differential counter is compared with the integer value in the reference register. During the recirculate output mode, the address word in the read counter is compared with the address word in the reference register. The results of these comparisons are reflected

by a logical high or low condition of the "greater than" output line from the comparator. The significance of these comparisons in each mode of operation is discussed in later paragraphs entitled "End-of-Process" and "Modes of Operation".

4-26 Recycle Generator

4-27 The recycle generator is used only in the recirculate output mode. It is used to send a 1 microsecond $\overline{\text{RECYCLE}}$ pulse to the external device when memory truncation occurs. This is explained in the paragraph entitled "Recirculate Output". A $\overline{\text{RECYCLE}}$ pulse is also generated when a Clear Card (CC) instruction is issued.

4-28 Mode Register

4-29 This register determines the mode of operation for the memory cards. Except for Memory Output (MO) and Memory Input (MI) instructions, which automatically select the FIFO output or FIFO input modes as part of their execution, the mode register must be programmed with a Write First Rank instruction prior to operation. The value entered in the field of the WF instruction determines the mode of operation, as shown here:

Mode of Operation	Set with Instruction
FIFO Output	WF, slot.1, 2T
FIFO Input	WF, slot.1,1T
Recirculate Output	WF, slot.1, 10T
Recirculate Input	WF, slot.1, 4T

Where slot = slot address of card 1.

4-30 In addition to setting the mode of operation, a LOCKOUT flag can also be set when the mode of operation is programmed. The purpose of lockout is covered later under the paragraph entitled "Programmed Lockout." It inhibits I/O handshaking operations so that no data can be sent to or received from the external device. The instructions that set the LOCKOUT flag are shown here:

Mode plus Lockout	Set with Instructions
FIFO Output and Lockout	WF, slot.1, 22T
FIFO Input and Lockout	WF, slot.1, 21T
Recirculate Output and Lockout	WF, slot.1, 30 T
Recirculate Input and Lockout	WF, slot.1, 24T

Where slot = slot address of card 1

4-31 The mode register is automatically set to the FIFO input mode when a Clear Card (CC) instruction is issued (which also clears LOCKOUT, if set). The LOCKOUT flag can be set independently of the mode register at any time with the instruction:

WF, slot.1, 20T

4-32 First Rank Storage

4-33 This register receives the data word sent to memory by an output instruction that references subaddress 0 of Card No. 1. When the card is cycled, the data word in this register is written to the memory location to which the write counter points. An output instruction such as a Write and Cycle referencing sub-address 0 of Card No. 1 can be used to send data to this register and cycle the card.

"WC, slot.0,data T"

4-34 When many data words are to be sent to memory at one time, the Memory Output (MO) instruction should be used. This instruction automatically sets the mode register to FIFO output, then transfers the data one word at a time to first rank storage and cycles the card after each transfer so the data is written to memory.

4-35 Return Buffer

4-36 The Return Buffer always contains a copy of the data word in the memory location to which the read counter points. The data word in this buffer can be read at any time by a Read Value instruction referencing subaddress 0 of Card No. 1.

"RV, slot.0, T"

The RV instruction does not cycle the card, so the content of the return buffer remains unchanged after being read. If an input instruction is used during the FIFO input or recirculate input mode, then data is read from the Return Buffer and the Read Counter is incremented. The return buffer will be updated with the data word from the next memory location.

4-37 A Memory Input (MI) instruction and a read from extended talk address 05 can be used to read data from consecutive memory locations. Each read from extended talk address 05, transfers the data from the Return Buffer and increments the Read counter. The MI specifies the slot address of card 1 and places the card in the FIFO input mode.

4-38 Device Output Buffer (DOB)

4-39 The DOB always contains a copy of the data word currently in the memory location to which the read counter points. In the FIFO output and recirculate output modes, the content of the DOB appears on the 16-data lines to the external device. When the external device sets $\overline{\text{DAC OUT}}$ true, the memory card acknowledges by setting $\overline{\text{DAV OUT}}$ false. After retrieving the next word, the memory card returns $\overline{\text{DAV OUT}}$ to true.

WF, slot.1, 1T

4-40 Device Input Buffer (DIB)

4-41 The DIB is loaded with a data word from the external

device when the device lowers the $\overline{\text{DAV IN}}$ line. The memory card responds by setting $\overline{\text{DAC IN}}$ low. In the FIFO input or recirculate input mode, the data word in the DIB is then written to the memory location to which the write counter points.

4-42 Random Access Memory (RAM)

4-43 The RAM is a series of 16-bit memory locations numbered 0 to 4,096.

4-44 Although the read and write counters can be programmed to any starting address and changed at any time, memory as treated in this section is considered as an FIFO buffer. Once the read, write, and difference counters are set to location 0, the counters are automatically incremented so that the data is read in the same order that it was written to memory (First-In-First-Out buffer).

4-45 The following example is intended to illustrate that memory always acts as a First-In-First-Out buffer provided that (1) the read and write counters are set initially to the same starting address, (2) the differential counter is set equal to the difference between the write and read counters, (3) the value in the counters is not reprogrammed between the time that data is written and the time that it is read.

Example: Assume that 100 words have just been written, so the write counter has the value 100 (Figure 4-2). Since the read counter is still at address 0, the first word written will be the first word read. Eventually, after each data word is read, the read counter is incremented until the last word is read and the read counter value is 100.

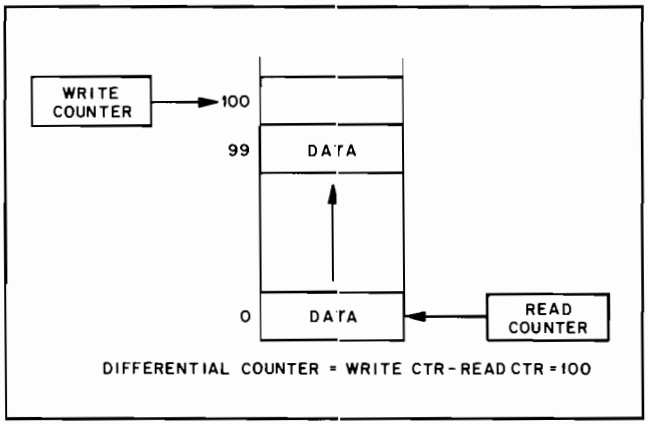


Figure 4-2. Memory After Data is Written but not yet Read.

4-46 Control Logic

4-47 The Control Logic supervises the operations of the memory cards. It establishes the timing, defines the read and write cycles for memory, and controls the input and output handshake lines to the external device. The circuits within the control logic section are described later in the paragraphs entitled "Detailed Functional Diagram Discussion."

4-48 OVERALL OPERATION

4-49 Power Turn-On

4-50 When power is applied to the memory cards, the circuits on the cards are cleared. A self test is then initiated by the Multiprogrammer. The self ID, data type, size and LSB parameters of the card are read and stored in Multiprogrammer memory as part of the wake-up sequence.

4-51 Memory Cycles

4-52 Every 4 microseconds a new memory cycle begins. The following read/write/compare sequence explains a typical memory cycle.

4-53 Read. At the beginning of each memory cycle, the address word in the read counter appears on the address bus and accesses memory. The data word in the accessed location is read out and loaded into both the return buffer and the Device Output Buffer (DOB). The return buffer and the DOB will always contain a copy of the data word currently pointed to by the read counter. The read counter is then incremented if either...

a. The FIFO input mode or recirculate input mode is active, and the card is cycled.
b. The device acknowledges receipt of a data word ($\overline{\text{DAC OUT}}$) just sent to the device during the FIFO output or recirculate output mode.

NOTE

Refer to later paragraphs on Memory Empty and Programmed Lockout for their affect on read operations.

4-54 In the special case of the recirculate output mode, the address in the read counter is compared with the address in the reference register during the read cycle.

4-55 Write. During the middle of a memory cycle, the address word in the write counter appears on the address bus. However, the memory location is not accessed and writing is not permitted unless one of two conditions is met:

a. The card is cycled by an output instruction or by a separate Cycle Card instruction during the FIFO output or recirculate output modes.
b. The external device lowers the $\overline{\text{DAV IN}}$ line to transfer a data word to the DIB during the FIFO input or recirculate input modes ("False" cycle).

4-56 If either of the above occur, a write cycle follows and either the data word in first rank storage or the DIB is written to memory depending on which mode is active. In either case, the write counter is incremented at the end of the write cycle.

NOTE

Refer to the paragraphs entitled "Memory Full" and "Programmed Lockout" for their effect on write operations.

4-57 Compare. At the end of every memory cycle, the value in the Differential Counter is compared with the value in the reference register. The result of these comparisons appears on the ">" comparator output line so that:

The ">" line is	If the
HIGH	Differential Counter > Reference Register
LOW	Differential Counter ≤ Reference Register

4-58 Examples of how these comparisons are used are given later in the paragraphs entitled "End-of-Process" (EOP) and "Modes of Operation."

4-59 Programmed Lockout

4-60 A Lockout flag can be set with the setting of the mode of operation or at any time after the mode is selected (refer to the paragraph on Mode Register). The primary purpose of Lockout is to prevent data from being sent to or received from the external device. Lockout also affects the read and write counters. The chart below shows how memory is affected when Lockout becomes active in each mode of operation.

4-61 Lockout can be cleared by reprogramming the mode register to its current mode but with the lockout value absent. A Clear Card instruction clears Lockout but also clears the read, write, and differential counters and also sets the mode to FIFO input mode. See table below.

4-62 Memory Full

4-63 If during the FIFO output or FIFO input mode, the differential counter should reach all 1's (top of memory), a "memory full" condition exists and the following actions result:

a. The write counter is frozen. No further incrementing of the write counter takes place.
b. If FIFO input mode is active, the $\overline{\text{MEMORY FULL}}$ line to the external device goes low.
c. The input handshake line $\overline{\text{DAV IN}}$ is inhibited so no data words are accepted from the external device.
d. Any attempt to write data to memory by cycling the card in an output instruction is ignored.
e. Memory Full inhibits write operations but does not affect read operations. Data can be read from any memory location and the read counter can be incremented as usual.

4-64 The memory full condition will occur when the read counter = 0 and the write counter reaches 4095.

4-65 Without the "memory full" feature, the write counter would reset to zero after reaching the top of memory. The data previously stored would be overwritten. (This is exactly what does happen in the recirculate modes).

4-66 Memory Empty

4-67 If during FIFO output or FIFO input modes, the difference counter becomes all 0's, a "memory empty" condition exists. Since the differential counter value is equal to the write counter value minus the read counter value, memory empty can occur in one of two ways:

1. Read Counter = write counter = 0; This case occurs when the counters are cleared with a clear card instruction or programmed to zero. This is an idle condition for the memory since no data has been written to memory (Write Counter = 0) no data can be read from memory.
2. Read Counter = write counter = non zero. This case occurs when all the data words that have

Programmed Lockout Actions

FIFO OUTPUT MODE	FIFO INPUT MODE	RECIRCULATE OUTPUT	RECIRCULATE INPUT
Device or Controller can still write data to memory but device can not read data from memory. (i.e. data transfers to device are disabled).	Neither device nor Controller can write data to memory. Write Write Counter is frozen. Data can still be read from memory by device or Controller.	Device or Controller can still write data to memory. Data cannot be read by device (i.e. data transfers to device are disabled). If Controller attempts to read memory, the last word read prior to Lockout is returned.	Same as FIFO Input

been written to memory have been read by the device or Controller.

4-68 When a "memory empty" condition occurs, the following actions take place:

a. The read counter is frozen and cannot be incremented.
b. If FIFO output mode is active, the MEMORY EMPTY line to the device goes low.
c. Requests from the device to read data are not acknowledged (DAV OUT held high).
d. Every attempt by the Controller to read data from memory and cycle the card results in the last data word read before the memory empty occurred being returned.
e. BUSY line to device is low during Memory Empty condition.
f. Write operations are still active and data can be written to memory from the device or Controller. The write pointer can be incremented as usual.

Table 4-1. Conditions Which Affect BUSY

Differential Counter	BUSY	MEANING
All Zero's (Write-Read = 0)	Low	In the FIFO output mode: All the words written to memory by the Controller have been read by the device. In the FIFO input mode: All the words written to memory by the device have been read by the Controller.
Not All Zeros (Write = Read = non 0)	High	In the FIFO output mode: Some data words written to memory by Controller have not yet been read by the device. In the FIFO input mode: Some data words written to memory by the device have not yet been read by the Controller.

NOTE: The BUSY status signal is not generated by the Universal Control Chip (UCC) as is the case in many I/O cards used in the Multiprogrammer.

4-69 Busy Flag

4-70 The BUSY flag is an indication of memory activity. The state of BUSY can be monitored at the edge connector via a separate BUSY status line. The Controller can inspect the state of BUSY by reading the second least significant bit in the status word returned by a Read Status instruction issued to Card No. 2. BUSY is the complement of the ALL 0's line from the difference counter. Since the differential counter is used only in the FIFO output and FIFO input modes, BUSY is interpreted for these modes in the accompanying chart. (See Table 4-1).

Table 4-2. Conditions Which Set EOP

MODE	EOP	MEANING
FIFO output	High	The value in the difference counter is equal to or less than the value in the reference register. This indicates that the controller should send more data to memory to be read by the device. (See Example 1 in Modes of Operation).
	Low	The value in the difference counter is greater than the value in reference register.
FIFO input	High	The value in the difference counter is greater than the value in the reference register. This occurs when the number of words stored in memory by the device but not yet read by the Controller has exceeded the number in the reference register.
	Low	The value in the difference counter is equal to or less than the value in the reference register.

4-71 End of Process (EOP) Flag

4-72 The End of Process flag applies only to the FIFO input and FIFO outut modes. The state of this flag can be monitored:

a. by the external device by monitoring the EOP status line at the external edge connector, or
b. by the Controller by inspecting the least significant bit of the status word returned by a Read Status instruction, issued to the slot address of card no. 2.

4-73 Basically, EOP is high or low depending upon comparisons between the differential counter and reference register. The meaning of the EOP flag for the FIFO output and FIFO input modes of operation are summarized in Table 4-2.

4-74 The EOP flag is cleared by a Clear Card instruction, and most Input and Output instructions. Refer to the next paragraph "Program Interrupt" for the relationship between EOP and interrupt requests.

NOTE

The EOP signal is similar to BUSY in that it is not generated by the UCC chip as in many other Multiprogrammer I/O cards.

4-75 Interrupt Request

4-76 When the End-of-Process (EOP) signal occurs, an Interrupt Request ($\overline{IRQ}$) is returned to the Multiprogrammer if the card is armed. The $\overline{IRQ}$ signal informs the Multiprogrammer that the output instruction has been completed. Output instructions like OI, OP, and OS arm the card when the first rank storage register is loaded. For WF, WC and CY instructions, the card must be armed prior to the execution of the instruction if an interrupt request is to be generated. This can be done with a separate Arm Card (AC) instruction issued at the controller, referencing the card no. 2 slot address. After a program interrupt request is made, the Multiprogrammer will respond by disarming the card and clearing the EOP and group address flag (GAFF).

NOTE

The $\overline{IRQ}$ signal is not generated by the UCC chip as is the case in many other Multiprogrammer I/O cards.

4-77 The GAFF flag is internal to the Universal Control Chip on the card and is set by instructions such as WC, OS, and OP to allow multiple cards to be cycled in parallel. Refer to Chapter 4 in the 6942A Multiprogrammer User's Guide for more information on cycling cards in parallel.

4-78 MODES OF OPERATION

4-79 The memory can be programmed via the mode register to operate in one of four modes:

1. FIFO Output
2. FIFO Input
3. Recirculate Output
4. Recirculate Input

4-80 The operation of memory in each mode is discussed in the following paragraphs.

4-81 FIFO Output Mode.

In this mode of operation, output instructions issued at the Controller transfer one, several, or a block of data words to memory. When memory contains data that has not been read by the external device, a signal is sent to the device ($\overline{DAV\ OUT}$ line goes low) indicating that data is available.

4-82 Data words are read by the device in the same order that they were written to memory. When all the data words have been read, the read counter will equal the write counter and, a memory empty condition exists.

4-83 When data is continuously written to memory and the device does not respond to the data available, it is possible that the memory will become full. No further writing to memory can take place (refer to the paragraph on Memory Full).

4-84 If a Lockout is programmed, data can be written to memory but none can be read by the device from memory until the LOCKOUT flag is cleared.

4-85 This mode is especially suited to storing a block of data words in memory and then having the external device read the data when it is ready. Example 1 in the following paragraph describes such a case.

Example 1: Assume that the FIFO output mode is used to store a block of 100 words in memory beginning at memory location 0. After all the words have been stored in memory, the device begins reading the data. When the device has read all but the last 10 words, an interrupt request should occur to alert the program that only ten words remain to be read. In this example assume that Card 1 is in slot 6 and Card 2 is in slot 7. The following Controller independent instructions are used.

1. "CC,7T"
2. "WF, 6.1, 22T"
3. "WF, 7.0, 10T"
4. Repeat 100 times:
   "WC, 6,",A[n],"T"
5. "AC, 7T"
6. "WF, 6.0, 1T"

Explanation:

1. Clears Card 2 so that the read, write, and differential counters are set to zero. The ARM, EOP, and BUSY flags are also cleared. Thus, the read counter = write counter, and the differential counter = write − read.
2. Sets the mode register to FIFO output mode and sets the LOCKOUT flag. LOCKOUT prevents any data

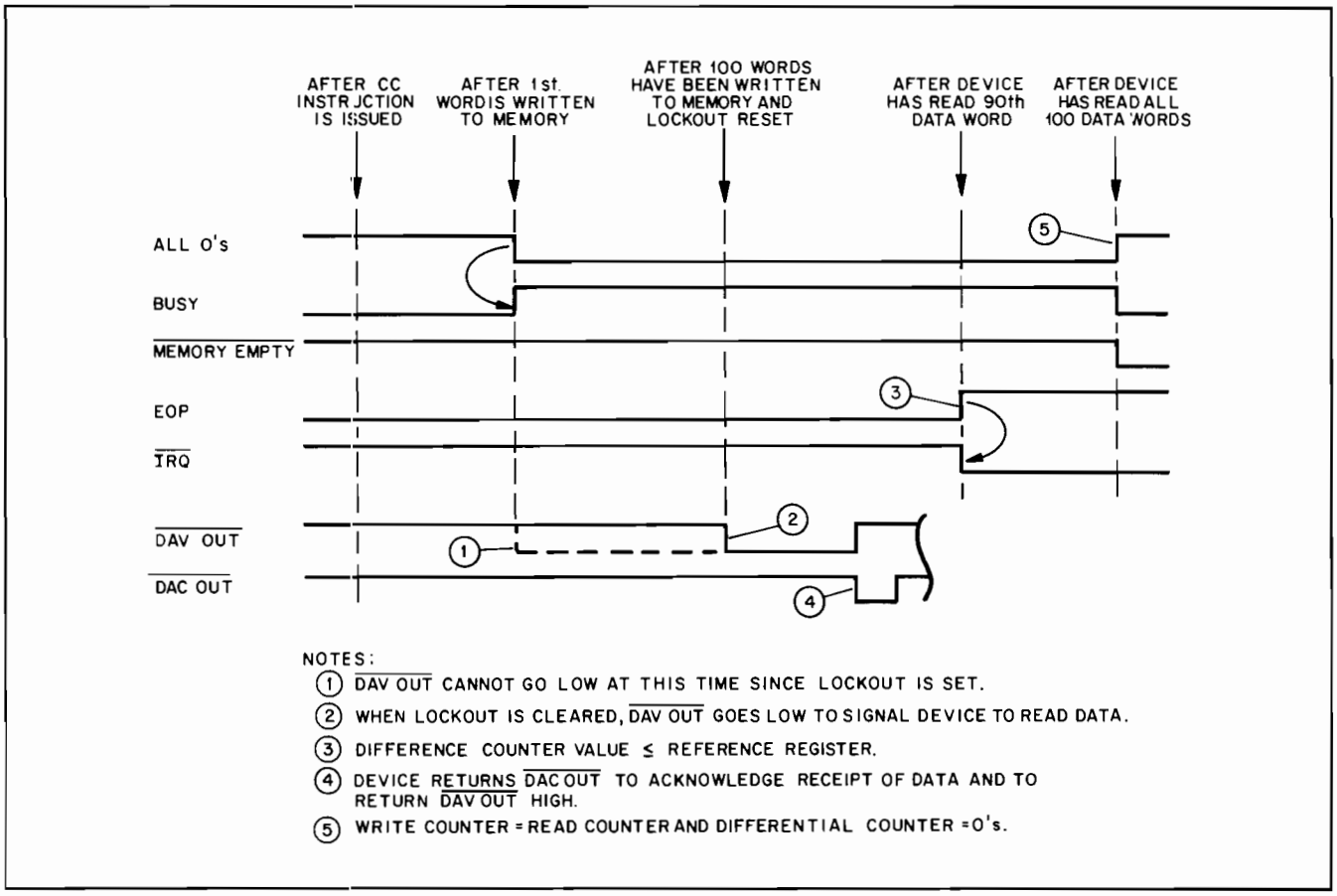


Figure 4-3. FIFO Output, Memory Timing Signals

transfers to or from the device while the 100 locations are being written with data.

3. Loads the reference register with the value 10 which enables an interrupt when ten words remain to be read.
4. Executes a Write and Cycle instruction 100 times. Each time, a data word from array A in the controller is sent to the memory. As each WC instruction is executed the following events take place:

   a. A data word is loaded from the controller into first rank storage in the memory card, the card is cycled, and the data is written into the memory location pointed to by the write counter (initially address 0).
   b. Both the write and difference counters are incremented.
   c. Since the difference counter is now non-zero, the ALL 0's line goes low, the BUSY line and MEMORY EMPTY lines to the device go high (see Figure 4-3).

   d. Normally, the DAV OUT line to the device would go low to indicate that memory contains a data word that has not been read, since LOCKOUT is active, the DAV OUT and DAC OUT lines are disabled, and no data is sent to the device.
   e. After 100 data words are written to memory, the counters have the values as shown in Figure 4-4.

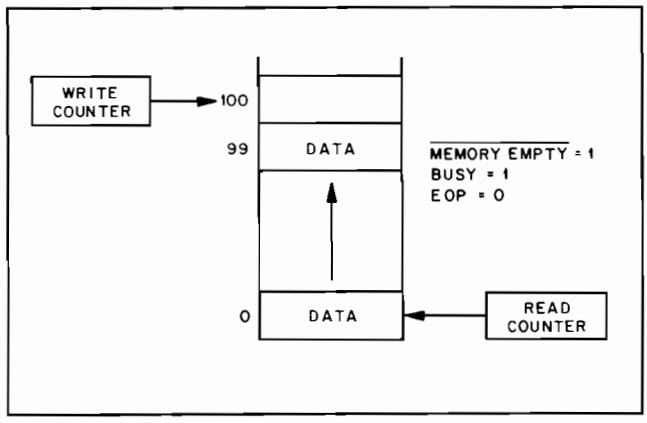


Figure 4-4. Memory after Writing 100 Words and No Words Read.

5. This instruction arms the card so interrupts are enabled as the device begins reading memory.
6. The FIFO output mode is entered again but with LOCKOUT cleared. Now the sequence of events are as follows:

   a. The $\overline{\text{DAV OUT}}$ line goes low, indicating that the external device can read the data word from the DOB. (This is the data word pointed to by the read counter).
   b. When the device reads the data word, it must pull $\overline{\text{DAC OUT}}$ low to acknowledge receipt of the word.
   c. Data words are continually read by the device via the DOB as described in steps (a) and (b).
   d. When the 90th word has been read by the device, the differential counter will have the value 10.
   e. The value in the differential counter is now equal to the value in the reference register so the End-of-Process (EOP) signal goes high. Because the card is armed, an interrupt request ($\overline{\text{IRQ}}$) is sent to the Multiprogrammer (see Figure 4-5).

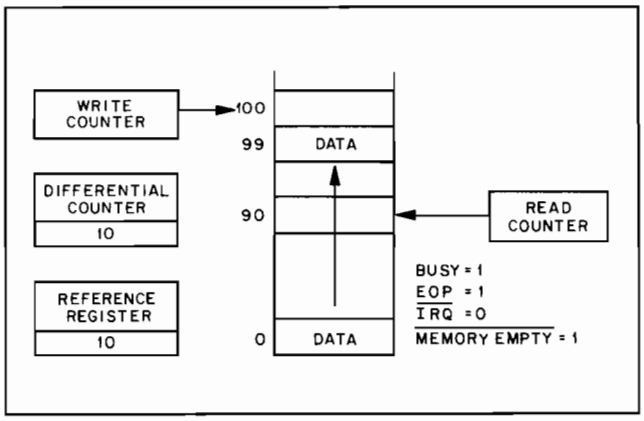


Figure 4-5. Memory After 90 Words Have Been Read By Device.

   f. When all 100 words have been read, the read counter = write counter and the differential counter = 0. The device control lines will have these values:

BUSY	=	0
EOP	=	1
$\overline{\text{MEMORY EMPTY}}$	=	0

4-86 Recirculate Output Mode

4-87 In the Recirculate Output Mode, no interrupt requests can be generated, and the memory full and memory empty conditions are not applicable. The EOP and BUSY flags have no meaning. A Lockout can still be programmed at any time.

4-88 In this mode, data is sent to memory and transferred of the device as in the FIFO output mode. The reference register contains an address word which is used to truncate read operations as follows:

1. As each data word is read by the device from memory, the address word in the read counter is compared with the address word in the reference register.
2. When the read counter address word exceeds the reference register address, memory truncation occurs and
   a. the read counter is automatically recycled to zero, and
   b. a Recycle generator is triggered and a one microsecond $\overline{\text{RECYCLED}}$ pulse is sent to the device.

NOTE

Truncation will not occur if the address word in the reference register is equal to the highest address in memory. This is true because the read counter address can never exceed this value. Should this be the case, when the read counter address reaches the top of memory, the read counter will reset to zero automatically, but no $\overline{\text{RECYCLED}}$ pulse will be sent to the device.

4-89 FIFO Input Mode

4-90 In this mode, the external device inititates the transfer of data words to memory. When the number of words transferred to memory is equal to the value in the Reference Register, EOP goes high and a program interrupt occurs if the device is armed. The data words can then be read by the Controller in the same order that they were sent to memory by the external device.

4-91 In this mode, it is possible for the device to continuously send data to memory until the memory becomes full. The $\overline{\text{MEMORY FULL}}$ line goes low and no futher data can be written to memory (refer to the paragraph on Memory Full).

4-92 This mode is especially useful when the device wishes to send a block of data words to memory and have the Multiprogrammer read the data sometime after the data has been stored. Example 2 describes this application.

Example 2: FIFO Input Mode

One hundred words are to be transferred from the external device into memory locations 0-99. When the words are stored, a program interrupt should occur to alert the Multiprogrammer to begin reading the data. Assume that the memory cards are in slot addresses 6 and 7.

1. "CC, 7T"
2. "WF, 7.0, 99T"
3. "AC, 7T"

4. Repeat 100 times:
   "RV, 6" A[n], "T"
   "CY, 6, T"

Explanation

1. The Clear Card instruction places the Mode Register (card no. 1) in the FIFO input mode, and clears the read, write, and differential counters (card no. 2), and clears the ARM flag. The read counter = write counter, and the differential counter = write − read.
2. Loads the Reference Register with the value 99 so that a program interrupt will occur after the 100th word is written to memory.
3. The AC instruction sets the ARM flag. When the external device is ready to transfer data words to memory, the following events take place:

   a. The $\overline{\text{DAV IN}}$ line goes low and the first data word is sent to the memory location pointed to by the Write pointer.
   b. The Write pointer and the differential counters are incremented.
   c. The write counter is now one greater than the read counter. The differential counter becomes non zero, and the ALL 0's line goes low. BUSY to the device goes high (see Figure 4-6).
   d. The $\overline{\text{DAC IN}}$ line goes low to acknowledge to the device that the data word was stored. The external device must then release the $\overline{\text{DAV IN}}$ line.
   e. The device continues to send data words to memory as described in steps (a) through (d). After the 100th word is written to memory, the memory counters have the values shown in Figure 4-7. With the difference counter equal to 100 the ">" (greater than) line from the comparator goes high and sets EOP. Since the card is armed, an interrupt request ($\overline{\text{IRQ}}$) is sent to the Multiprogrammer.

4. When the Multiprogrammer begins to read the data just stored, the events are:

   a. The data word at the location pointed to by the read counter is also in the Return Buffer.
   b. The data word is read from this buffer by a Read Value instruction.
   c. The read counter is incremented by a Cycle Card (CY) instruction and the difference counter is decremented.

   Steps (a) through (c) are repeated until all 100 words are read, at which time BUSY goes low and the difference counter is zero.

4-93 Recirculate Input Mode

4-94 In this mode, the memory acts as a circular buffer. Data words are transferred continuously from the device to memory. When the top of memory is reached, "memory-wrap-around" occurs automatically and data begins overwriting previously written data, beginning at location 0.

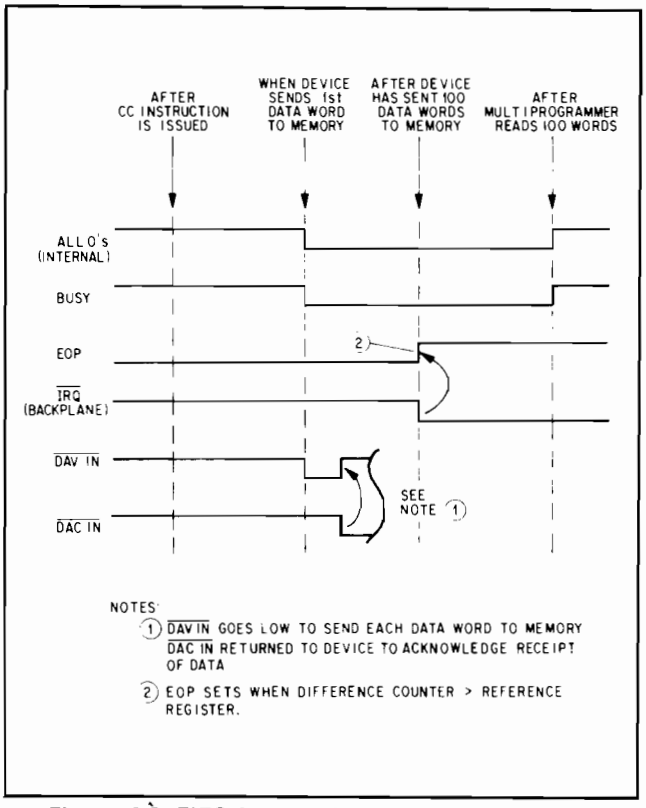


Figure 4-6. FIFO Input, Memory Timing Signals

4-95 In the recirculate input mode, the BUSY, EOP, $\overline{\text{RECYCLED}}$, $\overline{\text{MEMORY FULL}}$, and $\overline{\text{MEMORY EMPTY}}$ signals have no application. In addition, no interrupts can be generated and the differential counter and Reference Register are not used.

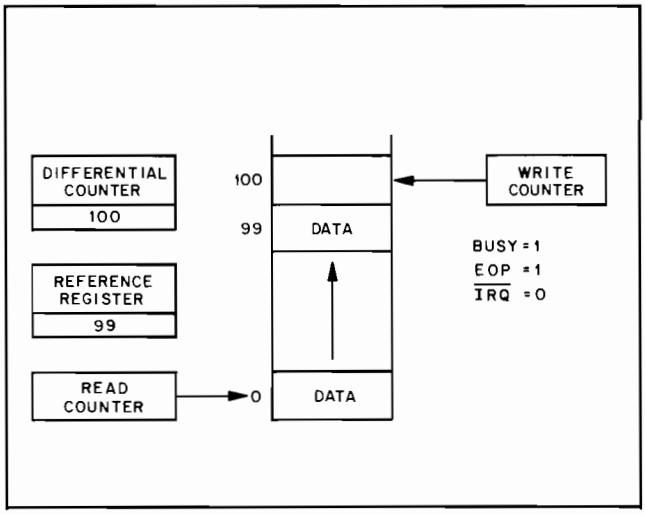


Figure 4-7. Memory After The Device Has Transferred 100 Words To Memory.

4-96 A Lockout can still be programmed at any time to terminate data transfers.

4-97 DETAILED FUNCTIONAL DIAGRAM DISCUSSION

4-98 The remaining paragraphs in this section cover the circuit theory for Card No. 1 and Card No. 2. The functional schematics for the two cards are shown in Figure 6-2 and 6-4 respectively. Each card uses a separate Universal Control Chip (UCC) to decode instructions from the Multiprogrammer and generate the appropriate control signals used by the card. Although the UCC is capable of generating many control signals, only a few of the control signals are actually used by each card.

4-99 Power Turn On

4-100 When power is applied to the Memory cards, a PCR signal on Card No. 2 clears the reference register. CLR and CLR' signals are generated on Card No. 2 and are used as follows:

	Card No. 1	Card No. 2
CLR	Generates a CLRR signal to clear read counter on Card No. 2 (also generates a RECYCLED pulse).	Clears the write and differential counters.
CLR'	Clears the mode register and handshake logic.	Not used

4-101 Overall Timing Diagram

4-102 Figure 4-8 is an overall timing diagram showing the primary control signals generated during the output and input modes of operation. Some of the circuits to be described contribute to the production of one or more of the signals shown.

4-103 Card 1 Functional Circuits

4-104 The functional circuits of Card no. 1 are shown in Figure 6-2. These include:

a. Universal Control Chip.
b. Bidirecitonal Transceivers.
c. Memory Timing Generator.
d. Mode Control Register.
e. Random Access Memory.
f. Chip Select Logic.
g. Read/Write Logic.
h. Read Counter Increment Logic.
i. Read Counter Reset Logic.
j. First Rank Storage.
k. Return Buffer.
l. Device Output Buffer (DOB).

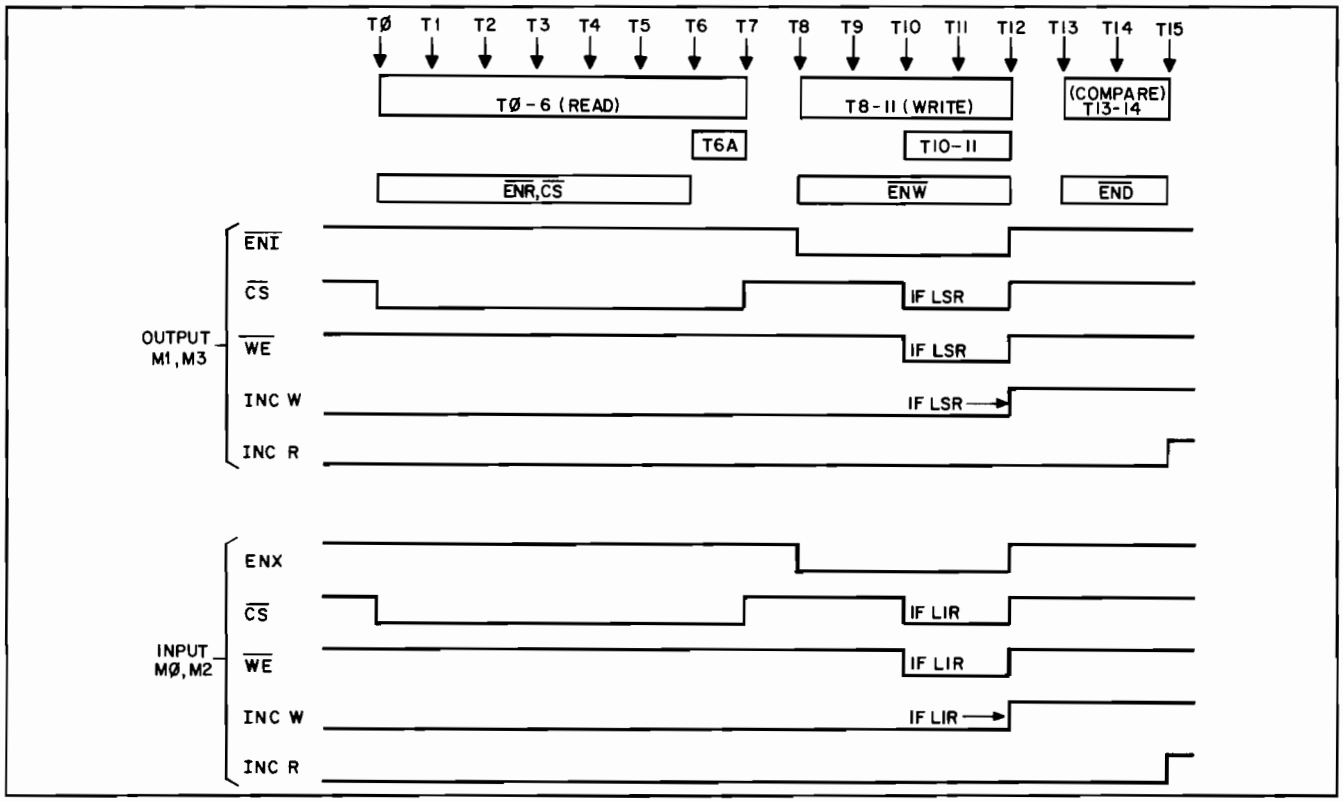


Figure 4-8. Memory Overall Timing Diagram.

m. Device Input Buffer (DIB).
n. EOP and Innterrupt Request Logic.
o. Data FULL/EMPTY Decoders.
p. Memory Input Handshake Logic.
q. Memory Output Handshake Logic.

4-105 In the above list, the first rank storage, return buffer, DOB, DIB, and EOP and Interrupt Request logic circuits were discussed earlier in this section in the paragraphs entitled "Memory Organization." These functions will not be discussed in the following paragraphs.

4-106 Universal Control Chip (UCC). When an instruction is issued at the Controller, the following input lines set up the UCC for a particular operation:

CAD – This is the card address line which goes high when the slot address of Card no. 1 appears in an instruction field.

R/W – This is the read/write line. It is high for read operations and low for write operations.

SAD0, SAD 1 – These two lines supply a subaddress code to the UCC. Depending on the instruction issued, one of the following control signals is decoded: STB0, STB1, $\overline{RTN0}$.

CTL0, CTL1, CTL2 – These lines supply a 3-bit control code to the UCC to indicate the operation to be performed. Depending on the instruction, one or more codes are sent in succession.

4-107 The data values on the above control lines are loaded into the UCC when a data strobe (DST) occurs. The control lines are then decoded to produce the various control signal outputs required for the particular operation.

4-108 Tri-State bidirectional Transceivers. The TRI-state bidirectional transceivers control the direction of the data flow between the card and Multiprogrammer. A UCC generated control signal, (CDE) is used to switch the direction of the data lines. During a write operation, CDE is low and the data lines are connected to the first rank storage register and to the mode register. During a read operation, CDE is high and the data lines (B0-B15) are connected to the output of the return buffer. Although the transceivers are tri-state, logic, jumper W6 establishes pin 19 at ground so that the isolated or high impedance state is never used.

4-109 Memory Timing Generator. All events taking place on the Memory cards are synchronized by timing signals developed by the memory timing generator. When power is applied to the card, a crystal oscillator turns on and produces free-running CLK clock pulses. The CLK pulses are applied to a 4-bit synchronous up counter which counts from 0 to 15 and recycles to zero again. Each count is decoded by a 4-line to 16-line decoder which establishes 16 separate clock phases T0-T16. From these clock phases, four major time states are generated: T0-6, T8-11, T10-11, and T13-14. Figure 4-8 shows this timing.

4-110 Three important control signals occur during the major time states:

a. $\overline{ENR}$ goes low during T0-T6, and is used to place the contents of the read counter on the address bus
b. $\overline{ENW}$ goes low during T8-11, and is used to place the contents of the write counter on the address bus.
c. $\overline{END}$ goes low during T13-14 and is used to place the contents of the difference counter on the address bus.

4-111 When any of these signals is high the output of the buffer associated with the signal is placed in the tri-state, high impedance (or off state).

4-112 Mode Control Register. The Mode Control Register is a five bit register with associated decoders. Depending on the value loaded into the register with a WF instruction, one of the output lines goes high and establishes the mode of operation. The value is loaded into the mode register on the leading edge of STB1 which is decoded from the SAD0, SAD1 lines. On power turn-on or whenever a Clear Card instruction is issued, the register is cleared by CLR making the M0 line go high (FIFO input mode).

Mode Signals

Octal Value Loaded	Mode Selected	Output Mode Signal
1	FIFO input	M0
2	FIFO output	M1
4	Recirculate input	M2
10	Recirculate output	M3
20	Lockout	Lockout

4-113 The $\overline{ENI}$ and $\overline{ENX}$ decoders are enabled during T8-11 and, depending on the mode of operation, one of these signals goes low.

a. $\overline{ENI}$ goes low if the mode is M1 or M3 (output modes) to place the contents of first rank storage on the data bus to memory.
b. $\overline{ENX}$ goes low if the mode is M0 or M2 (input modes) to place the contents of the device input buffer (DIB) on the data bus to memory.

4-114 Random Access Memory Chips. Each memory chip shown is a 1024 x 4 CMOS static memory. Because the chips are static, refresh circuits are not required. The data is read out of memory non destructively and has the same polari-

ty as the input data. All stored data is lost when power is removed. $\overline{CS}$ is the chip select signal that also controls the power-down feature. When $\overline{CS}$ is high, the memory chips are de-selected and the power drain is reduced to a low stand-by current. $\overline{WE}$ is the Write Enable signal. It is high during read cycles and is low for write operations.

4-115 Chip Selection Logic. The 12-bit address word on address lines, A0-A11, is used to access a particular memory location. The two high order bits (A10, A11) of the address word select one of four possible 1k banks of memory via the $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$ signals. The ten low order bits (A0-A9) address a unique location in the selected memory bank.

NOTE

Knowing which bank of memory is selected by a particular address word is important to the service technician when attempting to isolate addressing faults to a particular memory chip.

Example: Assume that the address word 2060_{10} is used to access memory in a memory card having the maximum $4{,}096_{10}$ words. The binary representation of this decimal address is...

1 0 0 0 0 0 0 0 1 1 0 0

BIT 11 BIT 0

Since bit 10 is "0" and bit 11 is "1", the second bank of memory is selected by the $\overline{CS2}$ chip select line. Bits 0-9 address the 12th location in this bank.

Chip Select Decoding

Selected Memory Bank	BITS 11	BITS 10	Chip Select Signal $\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$
4	0	0	1	1	1	0
3	1	0	1	1	0	1
2	1	0	1	0	1	1
1	1	1	0	1	1	1

4-116 Read/Write Logic. The purpose of the read/write logic is to control when the memory chips are enabled for reading and writing and to increment the write counter during write operations. For either a read or write operation, the appropriate Chip Select line ($\overline{CS}$) must be low to enable the memory chips. Then a read or write operation is determined by the logic level of the Write Enable line ($\overline{WE}$).

$\overline{WE}$ is low for write to memory.
$\overline{WE}$ is high for read from memory.

4-117 A read cycle takes place during T0-6 time state. $\overline{ENR}$ is low and makes $\overline{CS}$ low also. Since $\overline{WE}$ is high, the data word in the memory location pointed to by the read counter appears on the data bus and is loaded into the return buffer and into the DOB by the next T6A clock pulse.

4-118 A write cycle occurs during T10-11 time if WRITE INHIBIT is high and either:

1. The card is cycled (LSR) during M1 or M3 modes, or
2. A data word was loaded into the Device Input Buffer (DIB) by an LIR.

4-119 In either case, $\overline{ENW}$, $\overline{CS}$, and $\overline{WE}$ go low and data is written to the memory location pointed to by the write counter. At the beginning of the T12 phase, INC W goes high and increments the write counter.

4-120 Read Counter Increment Logic. The purpose of this logic is to produce a high going INC R pulse to increment the read counter. Whenever the card is cycled (LSR) during the M0 or M2 output modes, or whenever a data word is transmitted to the external device, flip-flop U28A sets provided Read Inhibit is high. At the beginning of T15, U28B sets and INC R goes low. At the beginning of T0 time (start of next memory cycle) INC R goes high to increment the read counter.

4-121 Read Counter Reset Logic. The purpose of the read counter reset logic is to produce a logic high CLR R level when either of the two following conditions is met:

a. a Clear Card (CC) instruction is issued, or a power-up reset occurs.
b. the greater than (>) line from the comparator on card no. 2 is high during Recirculate Output (M3) mode during the T3 (read cycle) phase.

4-122 When CLR R goes high it is routed to card no. 2 to clear the read counter and trigger the RECYCLED generator.

4-123 Data Full/Empty Decoders. These decoders drive two output lines to the external device: $\overline{MEMORY\ FULL}$ and $\overline{MEMORY\ EMPTY}$. In the FIFO Output mode, whenever the ALL 0's line from the decoder goes high the $\overline{MEMORY\ EMPTY}$ line goes low. In the FIFO Input mode, whenever the ALL 1's line from the decoder goes high, the $\overline{MEMORY\ FULL}$ line goes low.

4-124 Memory Input and Output Handshake Logic. The memory card has three handhshake lines for inputs and three for outputs. $\overline{Input\ Data\ Available}$ ($\overline{DAV\ IN}$), $\overline{Input\ Data\ Accepted}$, ($\overline{DAC\ IN}$) and $\overline{Memory\ Full}$ are the input handshake lines; and $\overline{Output\ Data\ Accepted}$ ($\overline{DAC\ OUT}$), $\overline{Output\ Data\ Available}$ ($\overline{DAV\ OUT}$), and $\overline{Memory\ Empty}$ are the output handshake lines. Under various circumstances, one, two or all three input or output handshake lines might be connected to an external device.

1. The $\overline{DAV\ IN}$ and $\overline{DAC\ OUT}$ lines must always be connected in order to handshake data in or out of the card.

2. If the DAC IN and the DAV OUT handshake lines are also connected, then a word can be transferred in or out of the card every 4 microseconds (assuming that delays in the external device do not slow down the handshake).
3. If the card is used with external devices that have a maximum data transfer rate that can never exceed one word every 8 microseconds, then the DAC IN line or the DAV OUT line can be left unconnected if desired.
4. If the Memory card is used in an application that provides some other means of assuring that data will not be lost because the memory became full or empty, then the MEMORY FULL and MEMORY EMPTY lines can be left unconnected.

NOTE

All three input handshake lines are inhibited in both output modes, and all three output handshake lines are inhibited in both input modes. The MEMORY FULL and MEMORY EMPTY output lines are both inhibited in the recirculate input mode and in the recirculate output mode.

The following paragraphs describe the memory card's input and output handshaking requirements in greater detail.

4-125 Memory Input Handshaking. An external device transfers a data word into the memory card by setting the DAV IN line low. If the DAC IN line is also connected, the memory card sets it low to acknowledge the transfer of each data word. The card sets the MEMORY FULL line low to inform the external device when the memory is full. Figure 4-9 shows the timing requirements of the memory input handshake sequence.

When using all three input handshake lines, a data word can be transferred into the memory card as often as every 4 microseconds. Before the external device sets DAV IN low, the input data must have been valid for at least 500 ns; the data must remain valid for at least 500 ns afterward. After the external device sets DAV IN low, the memory card sets the DAC IN line low within 1 microsecond. The external device can then immediately set DAV IN high. Once the memory card responds by setting DAC IN high, the DAV IN line can be can be set low again to make the next data transfer, assuming that the new input data has been valid for at least 500 ns.

4-126 If an external device uses the DAV IN line to initiate transfers of data into the memory card but does not have the DAC IN line connected to allow the card to acknowledge each data word, the maximum data transfer rate is slowed to one word every 8 microseconds. As before, input data must be valid for at least 500 ns before and after the external device transfers a data word into the card by setting DAV IN low. DAV IN must be held low for at least 500 ns, then it must be kept high for at least 6 microseconds before it is set low again to make the next data transfer.

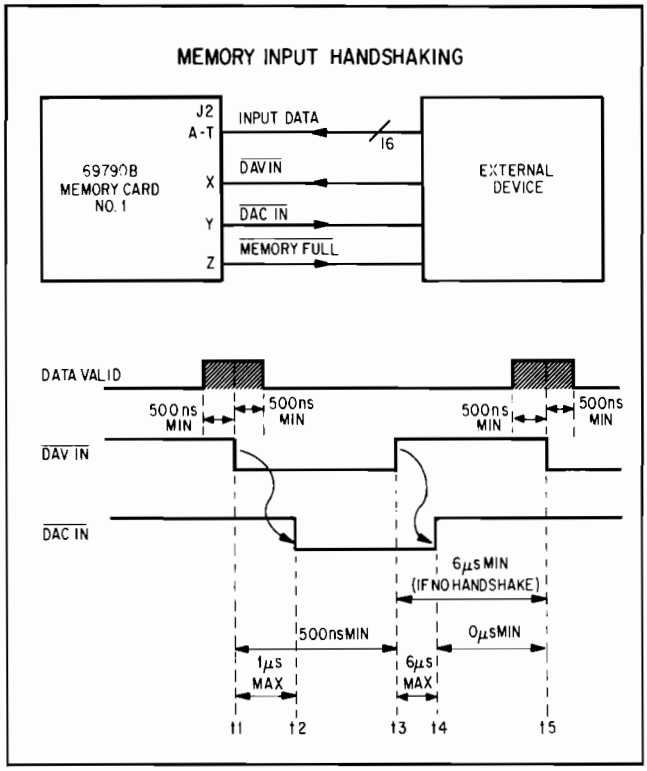


Figure 4-9. Memory Input Handshaking.

4-127 If the DAC IN line is connected, then it is not absolutely necessary to use the MEMORY FULL line, even if the number of words in memory is not being controlled by some other means. If the MEMORY FULL line is not being monitored and the external device attempts to load one more word into a full memory, the fact that the memory is full becomes evident when the card does not complete the handshake sequence. The card sets DAC IN low in response to input DAV IN being set low, but the card does not set DAC IN high again. The extra data word is stored on the card, but not in memory. It remains in the card's input latch until the next read operation by the controller makes a memory location available for it.

4-128 Memory Output Handshaking. If the DAV OUT line is connected, the memory card signals when a data word is ready to be taken by setting this line low. The external device sets the DAC OUT line low each time it accepts a word from the memory card. The card sets the MEMORY EMPTY line low to inform the external device when the memory is empty. Figure 4-10 shows the timing requirements of the memory output handshake sequence.

4-129 When using all three output handshake lines, a data word can be transferred out of the memory card as often as every 4 microseconds. Initially, a data word is present on the memory card's 16 output lines and DAV OUT is set low. After the external device sets DAC OUT low, the card sets the DAV OUT line high within 1 microsecond. (No valid data is then available until DAV OUT is set low again.) Once DAV OUT has

gone high, the external device can immediately set $\overline{\text{DAC OUT}}$ high. Within 6 microseconds of the time that $\overline{\text{DAC OUT}}$ is set high, a new data word becomes available as indicated by the $\overline{\text{DAV OUT}}$ line being set low. At any time after this, this new data word can be taken by the external device. The next new word is obtained by setting $\overline{\text{DAC OUT}}$ low again. The delay between the time that the external device sets $\overline{\text{DAC OUT}}$ high and the time that the memory card makes the next data word available can be as long as 6 microseconds; exactly how long it takes depends on what point in the card's operating cycle the external device sets $\overline{\text{DAC OUT}}$ high. Thus, the time that the external device holds $\overline{\text{DAC OUT}}$ low must be kept short in order that the handshake sequence can be completed within the 4-microsecond cycle of the card's internal clock.

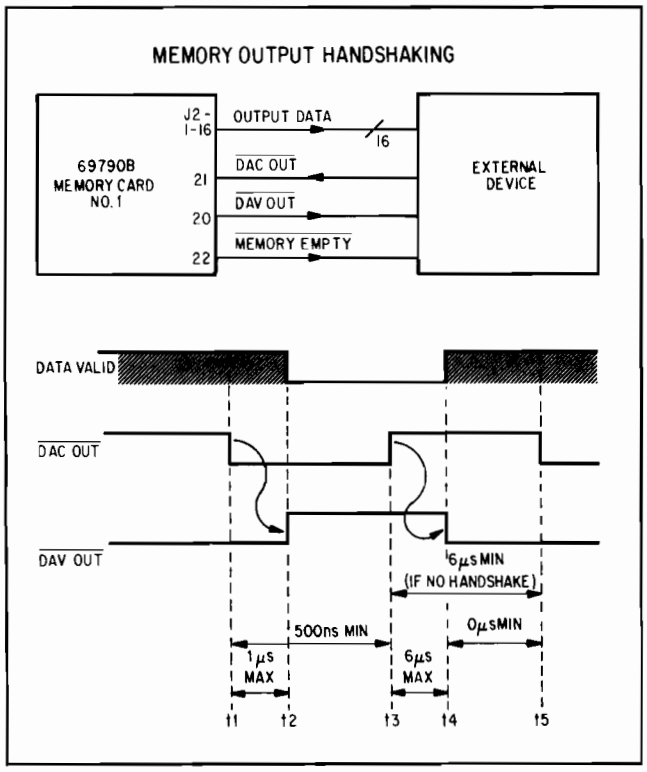


Figure 4-10. Memory Output Handshaking.

4-130 If an external device uses the $\overline{\text{DAC OUT}}$ line initiate transfers of data out of the memory card but does not have the $\overline{\text{DAV OUT}}$ line connected to allow the card to handshake each data transfer, the maximum data transfer rate is slowed to one word every 8 microseconds. in transferring a data word, $\overline{\text{DAC OUT}}$ must be held low for at least 500 ns, then it must be kept high or at least 6 microseconds before it is set low again to make the next data transfer.

4-131 Assuming that no other means is being used to prevent the external device from attempting to read from an empty memory, it is necessary to use the Memory empty line whether the $\overline{\text{DAV OUT}}$ line is connected or not. If the $\overline{\text{MEMORY EMPTY}}$ line is not being monitored and the external device attempts to read a word from an empty memory, an invalid data word will be taken. Even if $\overline{\text{DAV OUT}}$ is connected, the fact that memory is empty is not evident from the state of this line since it goes low even though the available data word is old data. (The word available to be taken from an empty memory is the old data remaining in the next location to be updated; the next controller write operation can update this location at any time.) Even though the card does not complete the handshake sequence (that is, $\overline{\text{DAV OUT}}$ does not go high in response to setting $\overline{\text{DAC OUT}}$ low), this does not prevent one invalid data word from being taken. Thus, in order to avoid reading an invalid word after the memory becomes empty, the $\overline{\text{MEMORY EMPTY}}$ line must be monitored unless some other means is used to prevent attempts to read from an empty memory.

4-132 Card No. 2 Memory Functions

4-133 The following paragraphs describe the circuit functions shown in the schematic diagram in Figure 6-4. Since the counters and registers of Card No. 2 were already discussed in the paragraphs entitled Memory Organization, they will not be repeated in this discussion.

4-134 Universal Control Chip (UCC). When an instruction is issued at the Controller, the following input lines set up the UCC for a particular operation:

CAD – This is the card address line which goes high when the slot address of Card No. 2 appears in the instruction field.

R/W – This is the read/write line. It is high for read operations and low for write operations.

SAD0, SAD1 – These two lines supply a subaddress code to the UCC. Depending on the instruction issued, one of the following control signals is decoded:

Sub-address	Load Strobe	Read Strobe
0	STB0	$\overline{\text{RTN0}}$
1	STB1	$\overline{\text{RTN1}}$
2	STB2	$\overline{\text{RTN2}}$
3	STB3	$\overline{\text{RTN3}}$

CTL0, CTL1, CTL2 – These lines supply a 3-bit control code to the UCC to indicate the operation to be performed. Depending on the instruction, one or more codes are sent in succession.

4-135 The data values on the above control lines are loaded into the UCC when a data strobe (DST) occurs. The control lines are then decoded to produce the various control signal outputs required for the particular operation.

4-136 Tri-State Bidirectional Transceivers. The TRI-state bidirectional transceivers control the direction of data flow between the card and Multiprogrammer. The CDE control signal is used to switch the direction of the data lines. During a write operation, CDE is low and the data lines are connected to the first rank storage register. During a read operation, CDE is high and the data lines (D00-D15) are connected to the output of the return buffer. Although the transceivers are tri-state, logic, jumper W30 establishes pin 19 at ground so that the isolated or high impedance state is never used.

4-137 Self-ID/Status Return Buffers. These buffers are also tri-state and their outputs are held in a high impedance (open) state while the $\overline{CRE}$ control line is high. When a Read Status instruction is issued, $\overline{CRE}$ goes low and the input data applied to this buffer are connected to the data lines going to the Multiprogrammer. The self ID/status word sent to the Multiprogrammer is shown below.

4-138 During system self-test, bits B3-B15 are stored in the Multiprogrammer memory for future use in formatting data sent to the card. When a RS instruction is issued, status bits B0-B2 are read and bits B3-B15 are ignored.

4-139 The self-ID bits B3-B15 specify the "wake-up" values of the LSB, card ID, size, and data type parameters. These values determine how the Multiprogrammer firmware will process the data it sends/receives from the card. The status information is provided by the ARM', BUSY', and EOP, control signals.

NOTE

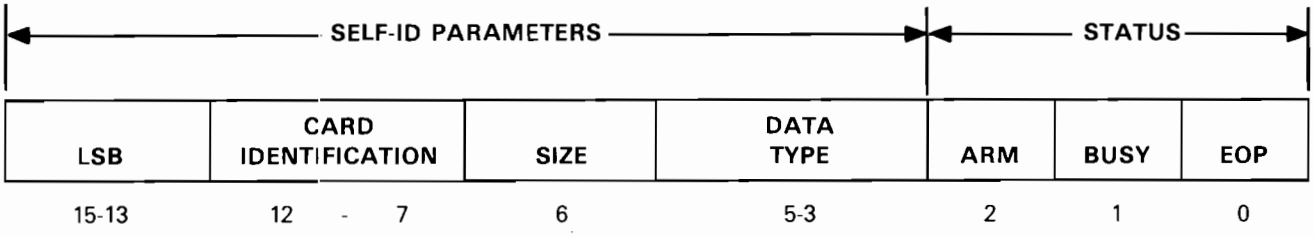
The Multiprogrammer determines the characteristics of Card No. 1 from the status word returned by Card No. 2.

4-140 Address Bus. A 12-bit address bus begins on card no. 2 and connects to the address lines of the memory chips on card no. 1. The address bus is time-shared by the read, write, and difference counter. At the start of a memory cycle, $\overline{ENABLE\ READ}$ goes low and the address word in the read counter is placed on the address bus. In the middle of the memory cycle, $\overline{ENABLE\ WRITE}$ goes low and the address word in the write counter appears on the address bus. At the end of the memory cycle, $\overline{END}$ goes low and the value in the difference counter appears on the address bus. Only the read and write counter address words are used to access memory.

4-141 The Return Buffer Strobe Generator. This generator forces the LRR, LDR and LWR signals low at the beginning of T15 time (end of T14). At the beginning of T13 time, the LOAD READ RETURN (LRR), LOAD DIFFERENCE RETURN (LDR) and LOAD WRITE RETURN (LRW) signals go high if the respective $\overline{RTN0}$, $\overline{RTN1}$, $\overline{RTN2}$ lines are high. This prevents the reading of a register while its contents are being updated.

4-142 ALL 1's and ALL 0's Decoders. These decoders are driven by the output lines from the Difference Counter.

Difference	ALL 1's	ALL 0's
4,095	True	False
0	False	True
$0 < x < 4095$	False	False



Section V
PARTS LIST

5-1 INTRODUCTION

5-2 This section contains information on ordering replacement parts for the Memory Assembly Model 69790B. Table 5-1 lists the electrical and mechanical components of Card No. 1. Table 5-2 lists the parts for Card No. 2. Table 5-3 lists the parts which make-up the external I/O connector assembly supplied with the card. Figure 5-1 illustrates how the parts in Table 5-3 are assembled.

5-3 HOW TO ORDER PARTS

5-4 You can order parts from your local Hewlett-Packard sales office. Refer to the list of sales offices at the end of this manual for the office nearest you. When ordering parts include the following information:

a. the Hewlett-Packard part number.
b. a description of the part.
c. the quantity desired.
d. the model number of the card (69790B).

5-5 If you wish to order a part directly from the manufacturer, locate the manufacturer's supply code in Table 5-1 or Table 5-2 and use this code to find the manufacturer's address in Table 5-4.

Table 5-1. Memory Assembly, Model 69790B, Card No. 1 Parts List.

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
C1-28	0160-4722	28	fxd cer 0.1uf +80-20% 50Vdc	28480	
C29	0180-0291	1	fxd elect 1uf +-10% 35Vdc	24546	150D105X9035A2
R1	0683-1035	6	fxd comp 10K 5% 1/4W	01121	CB1035
R2-5	0683-5125	4	fxd comp 5.1K 5% 1/4W	01121	CB5125
R6-10	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
U1	1820-1997	6	IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED PRL-IN	01295	SN74LS374N
U2,3	1820-1730	2	IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED COM	01295	SN74LS273N
U4	1820-1997		IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED PRL-IN	01295	SN74LS374N
U5	1820-1202	1	IC GATE TTL LS NAND TPL	01295	SN74LS10N
U6	1820-1416	1	IC SCHMITT-TRIGGER TTL LS INV HEX	01295	SN74LS14N
U7,8	1820-1112	7	IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED	01295	SN74LS74AN
U9	1820-1204	1	IC GATE TTL LS NAND DUAL	01295	SN74LS20N
U10	1820-1198	1	IC GATE TTL LS NAND QUAD	01295	SN74LS03N
U11	1820-1208	4	IC GATE TTL LS OR QUAD	01295	SN74LS32N
U12	1820-1203	1	IC GATE TTL LS AND TPL	01295	SN74LS11N
U13	1820-1208		IC GATE TTL LS OR QUAD	01295	SN74LS32N
U14	1820-1201	3	IC GATE TTL LS AND QUAD	01295	SN74LS08N
U15	1820-1112		IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED	01295	SN74LS74AN
U16-19	1818-1330	16	IC CMOS 4096 (4K) STAT RAM	S0545	UPD444C-1
U20	1820-1199	2	IC INV TTL LS HEX	01295	SN74LS04N

Table 5-1. Memory Assembly, Model 69790B, Card No. 1 Parts List (continued)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
U21	1820-1201		IC GATE TTL LS AND QUAD	01295	SN74LS08N
U22	1820-1210	1	IC GATE TTL LS AND-OR-INV DUAL	01295	SN74LS51N
U23	1820-1201		IC GATE TTL LS AND QUAD	01295	SN74LS08N
U24-27	1818-1330		IC CMOS 4096 (4K) STAT RAM	S0545	UPD444C-1
U28-30	1820-1112		IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED	01295	SN74LS74AN
U31-34	1818-1330		IC CMOS 4096 (4K) STAT RAM	S0545	UPD444C-1
U35	1820-1245	2	IC DCDR TTL LS 2-TO-4-LINE DUAL	01295	SN74LS155N
U36	1820-1112		IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED	01295	SN74LS74AN
U37-40	1818-1330		IC CMOS 4096 (4K) STAT RAM	S0545	UPD444C-1
U41,42	1820-1208		IC GATE TTL LS OR QUAD	01295	SN74LS32N
U43	1820-0495	1	IC DCDR TTL 4-TO-16-LINE	01295	SN74154N
U44-47	1820-1997		IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED PRL-IN	01295	SN74LS374N
U48	1820-1196	1	IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED COM	01295	SN74LS174N
U49	1820-1199		IC INV TTL LS HEX	01295	SN74LS04N
U50	0960-0464	1	IC CRYSTAL OSCILLATOR	28480	
U51	1820-1194	1	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U52-53	1820-2239	2	IC DRVR TTL S BUS	27014	DP8304BN
U54	1820-2302	1	IC CONTROL CHIP	28480	
Z1,2	1810-0280	2	NETWORK RESISTOR 10K (9)	01121	210A103
			Mechanical Parts		
	69790-80001	1	CARD EXTRACTOR	28480	
	69790-60001	1	CONNECTOR CABLE		
	1480-0059	1	..PIN ROLL (.062 in.)		
	1200-0552	1	SOCKET-40 CONTACT (U54)	28480	
	1200-0607	2	SOCKET-16 PIN (J3, J4)	28480	
	5060-2806	1	EXTERNAL EDGE CONNECTOR ASSEMBLY (See Table 5-3)	28480	
	9211-3450	1	SHIPPING CARTON	28480	

Table 5-2. Memory Assembly, Model 69790B, Card No. 2, Parts List.

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
C1	0160-4722	21	fxd cer 0.1uf +80-20% 50Vdc	28480	
C2	0160-4801	1	fxd cer 100pf +-5% 100Vdc	28480	
C3,4	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C5	0140-0149	2	fxd mica 470pf +-5% 300Vdc	72136	DM15F471J0300WV1C
C6	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C7	0140-0149		fxd mica 470pf +-5% 300Vdc	72136	DM15F471J0300WV1C
C8-24	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C25	0180-0291	1	fxd elect 1uf +-10% 35Vdc	24546	150D105X9035A2
R1	0698-3269	1	fxd film 23K 1% 1/8W	24546	C4-1/8-T0-2302-F
R2	0683-1015	1	fxd comp 100 5% 1/4W	01121	CB1015
R3,4	0683-5125	2	fxd comp 5.1K 5% 1/4W	01121	CB5125
U1-3	1820-1419	3	IC COMPTR TTL LS MAGTD	01295	SN74LS85N
U4-9	1820-2257	17	IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U10	1820-1199	1	IC INV TTL LS HEX	01295	SN74LS04N
U11	1820-1422	1	IC MV TTL LS MONOSTBL RETRIG	01295	SN74LS122N
U12-14	1820-1194	9	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U15	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U16	1820-0655	2	IC GATE TTL NOR DUAL	01295	SN7425N
U17	1820-1204	1	IC GATE TTL LS NAND DUAL	01295	SN74LS20N
U18-20	1820-1194		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U21	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U22	1820-0655		IC GATE TTL NOR DUAL	01295	SN7425N
U23	1820-1626	1	IC GATE CMOS NAND DUAL	27014	MM74C20N
U24-26	1820-1194		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U27,28	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U29	1820-1195	1	IC FF TTL LS D-TYPE POS-EDGE-TRIGGERED COM	01295	SN74LS175N
U30-32	1820-1544		IC CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U33	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U34	1820-1544		IC CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U35	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U36-38	1820-1544		IC CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U39	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U40	1820-1544		IC CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U41,42	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U43-46	1820-1544		IC CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U47	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U48	1820-1544		IC CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF

Table 5-2. Memory Assembly, Model 69790B, Card No. 2 Parts List (continued)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
U49	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U50,51	1820-2239	2	IC DRVR TTL S BUS	27014	DP8304BN
U52	1820-2302	1	IC CONTROL CHIP	28480	
Z1	1810-0231	3	NETWORK RESISTOR 2.2K (7)	01121	208A222
Z2-6	1810-0205	7	NETWORK RESISTOR 4.7K (7)	01121	208A472
Z7	1810-0231		NETWORK RESISTOR 2.2K (7)	01121	208A222
Z8,9	1810-0205		NETWORK RESISTOR 4.7K (7)	01121	208A472
Z10	1810-0231		NETWORK RESISTOR 2.2K (7)	01121	208A222
			Mechanical Parts		
	69790-80001	1	CARD EXTRACTOR	28480	
	1480-0059	1	..PIN ROLL (.062 in.)		
	69790-90003	1	MANUAL, OPERATION AND INSTRUCTION	28480	
	1200-0552	1	SOCKET-40 CONTACT (U52)	28480	

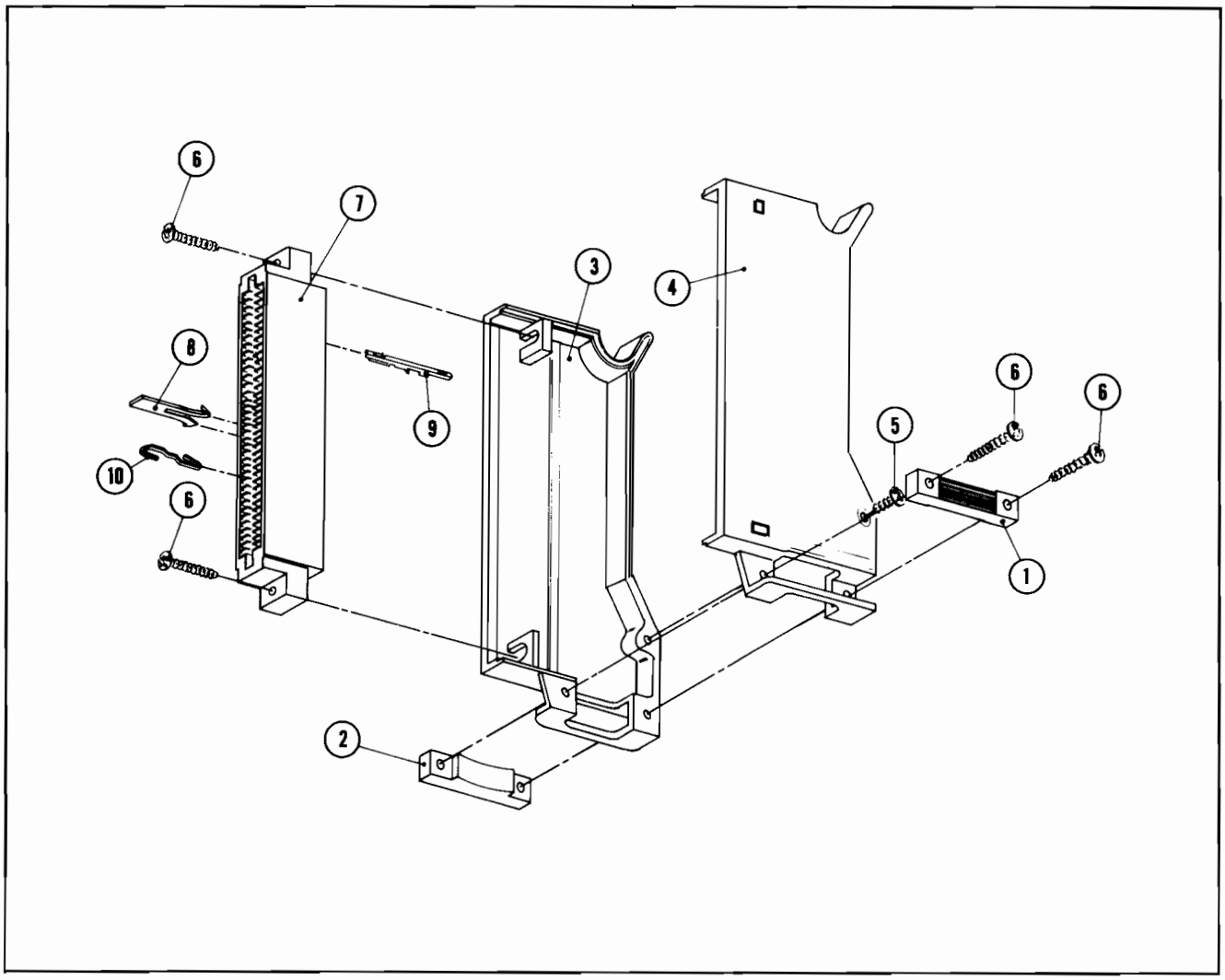


Figure 5-1. External I/O Connector Assembly, (HP P/N 5060-2806) Exploded View

Table 5-3. Parts List for External I/O Connector Assembly (HP Part No. 5060-2806).*

HP PART NO	INDEX NO	DESCRIPTION	QTY
1251-6307		HOOD ASSEMBLY**	
	1	STRAIN RELIEF	
	2	CABLE CLAMPS	
	3	RIGHT HOOD ASSEMBLY	
	4	LEFT HOOD ASSEMBLY	
	5	SCREW, 7/16 INCH	
	6	SCREWS, 11/16 INCH	
1251-6059	7	CONNECTOR PIN HOUSING	1
1251-6056	8	CONNECTOR KEY	1
1251-6183	9	SOLDER PINS, PLATED	45
1251-6380	10	SPRINGS, RETAINING	6

* CAN BE ORDERED AS MODEL 14703A, CARD EDGE CONNECTOR
** ITEM 1251-6307 CONSISTS OF INDEX ITEMS 1 THROUGH 6.

Section VI
DIAGRAMS

6-1 COMPONENT LOCATION

6-2 Figure 6-1 shows Card No. 1 and identifies the location of the components and test points shown functionally on the Card No. 1 schematic diagram, Figure 6-2. The component location and schematic diagrams for Card No. 2 are given in Figures 6-3 and 6-4, respectively.

6-3 SCHEMATIC DIAGRAM

6-4 Figure 6-2 shows the 4 k RAM, first rank storge, return buffer, device input/output logic circuits on Card No. 1. Figure 6-4 illustrates the read counter, write counter, differential counter, reference register, all 1's/all 0's decoder, and comparator circuits on Card No. 2. The diagrams use the ANSI Y32.14 and IEEE Standard 91 for the representations of logic elements. A brief summary of this notation is given in Table 6-1.

Table 6-1. Abbreviated List of ANSI Y32.14 Schematic Symbols

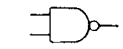
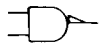
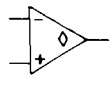
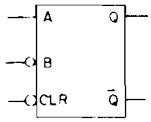
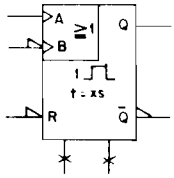
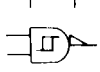
Definitions:

High = more positive
Low = less positive

True = logical "1" state
False = logical "0" state

Indicator and Qualifier Symbols

≥1	OR function
=1	exclusive OR function
&	AND function
▽	3-state output
EN	enable device output
⊏>	(polarity indicator, shown outside logic symbol) Any marked input or output is active low; any unmarked input or output is active high.
⊰	(dynamic indicator) Any marked input is edge-triggered, ie, active during transition between states; any marked input is level sensitive.
⊥⊤	(Schmitt trigger) indicates that hysteresis exists in device.
⁂	(non-logic indicator) Any marked input or output does not carry logic information.)
⟨⟩	open-collector or open emitter output
1⎍	monstable (one-shot) multivibrator
t = xSec	indicates pulse width (usually determined by external RC network)
G	gate input (a number follwing G indicates which inputs are gated); also, astable element
C	control input (clock)
R	reset (clear)
S	set (preset)
D	data input to storage element
▷	buffered element with extra output capacity

OLD SYMBOL	*NEW SYMBOL*	*NOTES*
		
		Output requires external components to achieve logic state.
		A positive-going transition at A or a negative-going transition at B triggers the one-shot. External timing components connect to non-logic inputs.
		Output changes state rapidly regardless of input rate of change.

Appendix A
BACKDATING

A-1 This appendix describes those changes that must be made to this manual to make it applicable to Model 69790B cards with serials from 2120A-00101 to 2120A-01435 and Model 69790A cards with serials from 1910A-00101 to 2110A-0940. To adapt the manual, inspect the following table for your serial number and make the appropriate changes.

SERIAL		MAKE CHANGES
Prefix	Number	
2120A	01435-0101	1
2110A	0940-0821	1,2
1910A	0820-0101	1,2,3

CHANGE 1

In Table 5-1, under Mechanical Parts, change HP Part No. of the 16-pin sockets (J3,J4) to 1200-0507, qty. 2.

CHANGE 2

A. IN SECTION I UNDER THE PARAGRAPH "DESCRIPTION" MAKE THESE CHANGES:

1. Change "Memory Assembly provides 4,096 words of CMOS random access memory" to:

   "Memory Assembly provides up to 4,096 words of random access memory depending on what option is ordered:

   Standard – 1k
   Option 002 – 2k
   Option 004 – 4k

2. In Table 1-1 change "Memory Size from 4,096 16-bit words" to:

   "Memory Size up to 4,096 16-bit words depending on the amount of memory ordered."

B. IN SECTION II ADD THE FOLLOWING PARAGRAPHS:

2-13 Mainframe +5 V Power Restrictions

2-14 The +5 V mainframe power supply has a maximum current capacity of 12.8 amperes. If the User's mainframe chassis already contains one or more cards having a high current drain (in the amperes range), an overload condition could occur if a 69790A Memory Card is installed (the 12.8 ampere current capacity is exceeded).

To determine if such a situation will occur, perform the following test before installing the card into the mainframe:

1. For each I/O card that is currently installed in the mainframe, record the +5 V current drain. To find these values, refer to the Operating Manual on each I/O card and note the value given in Table 1-1 of Section I under "+5 V Current Requirement".
2. Compute the total current drain due to all I/O cards combined. (This is the sum of all the individual values found in step 1).

   Enter this value here:_____

   – If this amount is less than 12.8 amperes, no current restriction applies and the 69790A Memory card may be installed.

   – If this amount is greater than 12.8 amperes, DO NOT install the Memory card as an overload will result.

C. IN SECTION III, AFTER PARAGRAPH 3-9, ADD PARAGRAPH 3-9A AS FOLLOWS:

3-9A Memory Jumpers

3-9B For 69790A cards, the amount of memory available depends on which memory option was ordered. For each memory option, jumpers W1-W16 are arranged at the factory according to the chart on the next page.

D. IN TABLE 5-1, PARTS LIST FOR CARD NO. MAKE THESE CHANGES:

1. For U52 and U53 change the HP part number from "1820-2239" to TPPNR-13483
2. For IC's U16-19, U24-27, U31-34, U37-40 change HP part number from "1818-1330 IC CMOS RAM" to "1818-0443 IC C2114-3",
3. Change model number in table caption from "69790B" to "Model 69790A".

E. IN TABLE 5-2, PARTS LIST FOR CARD NO. 2, CHANGE MODEL NUMBER IN TABLE CAPTION FROM "69790B" TO "MODEL 69790A".

F. IN FIGURE 6-1 AND FIGURE 6-4, CHANGE CAPTION FROM "69790B" TO "69790A."

G. IN FIGURES 6-1 AND 6-2 ADD TO CAPTION "SHOWN WITH FULL COMPLEMENT OF MEMORY (4K)

CHANGE 3:

In Table 5-2, change U23 to HP Part No. 1820-1204, Mfr. Part No. SN74LS20N

69790A Memory Jumper Options

OPTION	MEMORY IC'S INSTALLED ON MEMORY CARD NO.1 (HP PART NO. 1818-0443)	JUMPERS ON MEMORY CARD NO.2															
		W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16
STANDARD (1024 16-BIT WORDS)	U16, 24, 31, 37	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
OPTION 002 (2048 16-BIT WORDS)	U16, 17, 24, 25, 31, 32, 37, 38	0	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0
OPTION 004 (4096 16-BIT WORDS)	U16-19, 24-27, 31-34, 37-40	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	1

1 = JUMPER IN 0 = JUMPER OUT

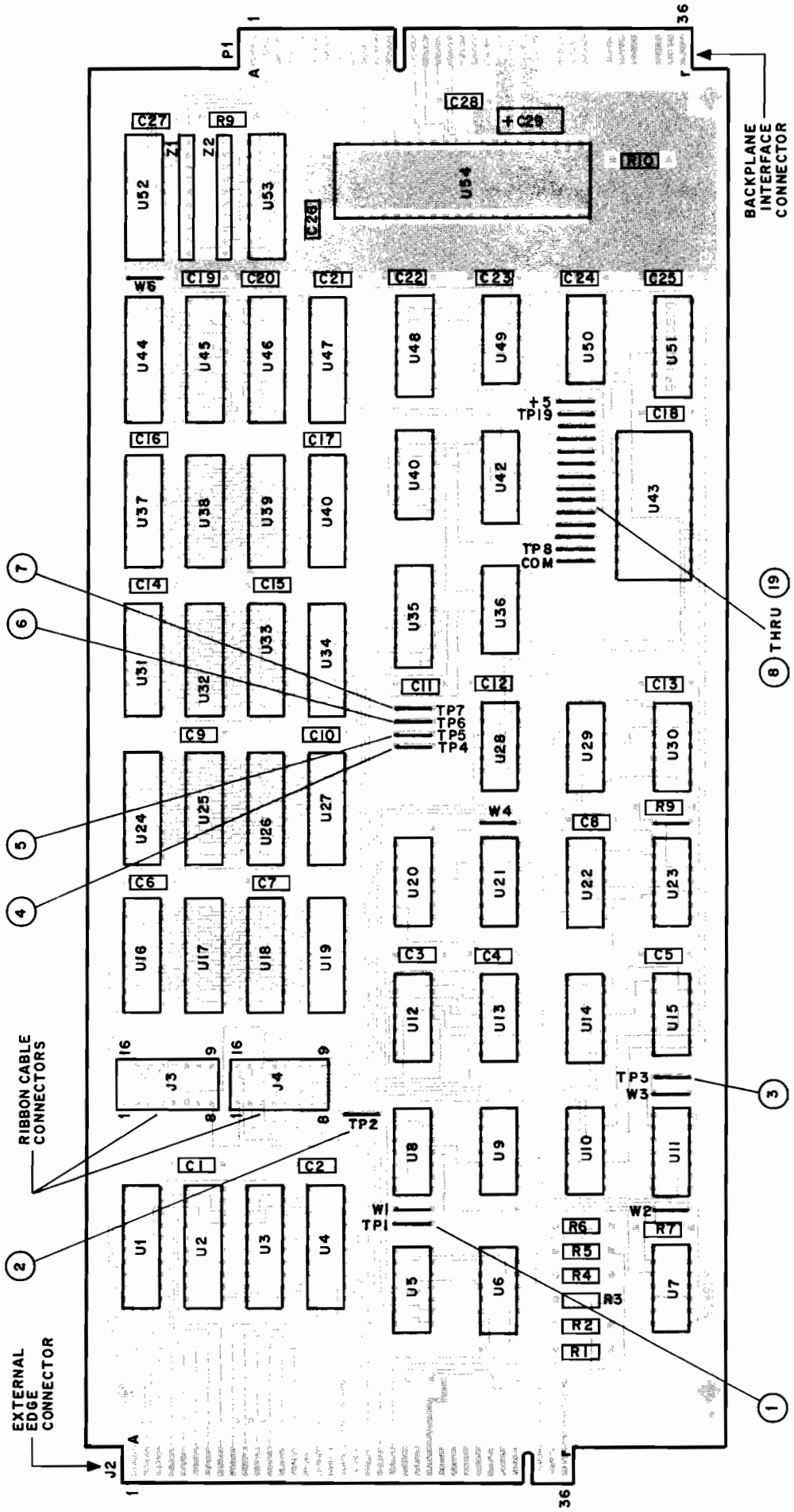


Figure 6-1. 69790B Memory Card No. 1, Component Locations.

P/O 69790B MEMORY CARD NO.1

BIDIRECTIONAL DATA TRANSCEIVER

U52(XCVRS)

U53(XCVRS)

16 DATA LINES

BACKPLANE +5V

P1

R9 10K

W6

FROM UCC CDE

B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15

B7D00 B7D01 B7D02 B7D03 B7D04 B7D05 B7D06 B7D07 B7D08 B7D09 B7D10 B7D11 B7D12 B7D13 B7D14 B7D15

Z1,10K

Z2,10K

RETURN BUFFER

U44

U47

FROM UCC RTN0

FROM MEM. TIMINGGEN T6A

B8D00 B8D01 B8D02 B8D03 B8D04 B8D05 B8D06 B8D07 B8D08 B8D09 B8D10 B8D11 B8D12 B8D13 B8D14 B8D15

FIRST RANK STORAGE

U45

U46

FROM MODE REGISTER EN1

FROM UCC ST80

UNIVERSAL CONTROL CHIP (UCC)

U54

CAD SAD0 SAD1 R/W CTL0 CTL1 CTL2 SYE DST IRQ

CONTROL LINES

ADDRESS DECODER

CONTROL CKTS

HANDSHAKE CKTS

STB0 TO FIRST RANK STORAGE

STB1 TO MODE REGISTER

RTN0 TO RETURN BUFFER

CDE TO BIDIRECTIONAL DATA XCVRS

LSR TO EOP/IRQ LOGIC(SHEET2)& READ COUNTER INCREMENT LOGIC (SHEET 2)

NC

R10 10K +5V

INPUT POWER

C29 1

C1-17, C19-23, C25-28 0.1

COM

MEMORY TIMING GENERATOR

U50 4MHz OSCILLATOR

U51 U43

C24 0.1

C18 0.1

U49 U42 U29 U30

CLK TO MEMORY INPUT/OUTPUT HANDSHAKE LOGIC (SHEET 2)

T0 TO READ COUNTER INCREMENT LOGIC (SHEET 2)

T1 NC

T2 NC

T3 U49-9

T4 NC

T5 NC

T6 U42-13

T7 U29-3, U29-13

T8 TO READ/WRITE LOGIC

T9 U30-3 TO READ/WRITE LOGIC & MEMORY OUTPUT HANDSHAKE LOGIC (SHEET 2)

T10 NC

T11 NC

T12 U29-1, U30-1, U30-11 TO MEMORY INPUT HANDSHAKE LOGIC (SHEET 2) & RIBBON CABLE CONNECTOR J4-12 (SHEET 2)

T13 NC

T14 TO READ COUNTER INCREMENT LOGIC (SHEET 2) & RIBBON CABLE CONNECTOR J4-13 (SHEET 2)

T15 U29-11, U30-13, U49-5

T6A TO RETURN BUFFER & DEVICE INPUT BUFFER (SHEET 2)

T3 TO CLEAR READ COUNTER DECODER (SHEET 2)

T15 TO EOP/IRQ LOGIC (SHEET 2)

ENR TO RIBBON CABLE CONNECTOR J4-5 (SHEET 2)

T0-T6 TO CHIP SELECT LOGIC

ENW TO RIBBON CABLE CONNECTOR J3-9 (SHEET 2)

T8-T11 TO MODE REGISTER

T10-T11 TO READ/WRITE LOGIC

END TO RIBBON CABLE CONNECTOR J4-11 (SHEET 2)

T13,T14 NC

4Kx16 RANDOM ACCESS MEMORY (RAM)

A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 WE CS1

READ/WRITE LOGIC

FROM MEMORY TIMING GEN. T10-T11 T8

WRITE INHIBIT

FROM MEMORY INPUT HANDSHAKE LOGIC(SHEET2) LIR

LSR

FROM MODE REGULATOR REGISTER M1 OR M3

FROM MEM TIMING GEN. T9

FROM RIBBON CABLE CONNECTOR J4-3 (SHEET 2) CLR'

FROM UCC STB1

U11 U23 U14 U15 U1

R7 10K W2 W3

WRITE PENDING TO MEMORY INPUT HANDSHAKE LOGIC (SHEET 2)

INCW TO RIBBON CABLE CONNECTOR J4-6 (SHEET 2)

WE TO 4K x16 RANDOM ACCESS MEMORY (RAM)

MODE REGISTER

U48 U49 U42 U41 U20

B7D00 - B7D04

B7D00 B7D01 B7D02 B7D03 B7D04

M0 OR M1 TO MEMORY INPUT/OUTPUT HANDSHAKE LOGIC (SHEET 2)

M0 M1 TO EOP/IRQ LOGIC (SHEET 2) & DATA FULL/EMPTY DECODER (SHEET 2)

M0 OR M2 TO MEMORY INPUT HANDSHAKE LOGIC (SHEET 2) & READ COUNTER INCREMENT LOGIC (SHEET 2)

M3 TO CLEAR READ COUNTER DECODER (SHEET 2) & MEMORY OUTPUT HANDSHAKE LOGIC (SHEET 2)

M1 OR M3 TO READ/WRITE LOGIC & MEMORY OUTPUT HANDSHAKE LOGIC (SHEET 2)

EN1 TO FIRST RANK STORAGE

ENX TO DEVICE OUTPUT BUFFER (SHEET 2)

LOCKOUT NC

LOCKOUT TO MEMORY INPUT/OUTPUT HANDSHAKE LOGIC (SHEET 2)

FROM MEMORY TIMING GEN. T8-11

CHIP SELECT LOGIC

U14 U35

FROM MEMORY TIMING GEN. T0-6

A11 A10

CS1 CS2 CS3 CS4

TO 4K x16 RANDOM ACCESS MEMORY (RAM)

B2D11 B2D10 B2D09 B2D08

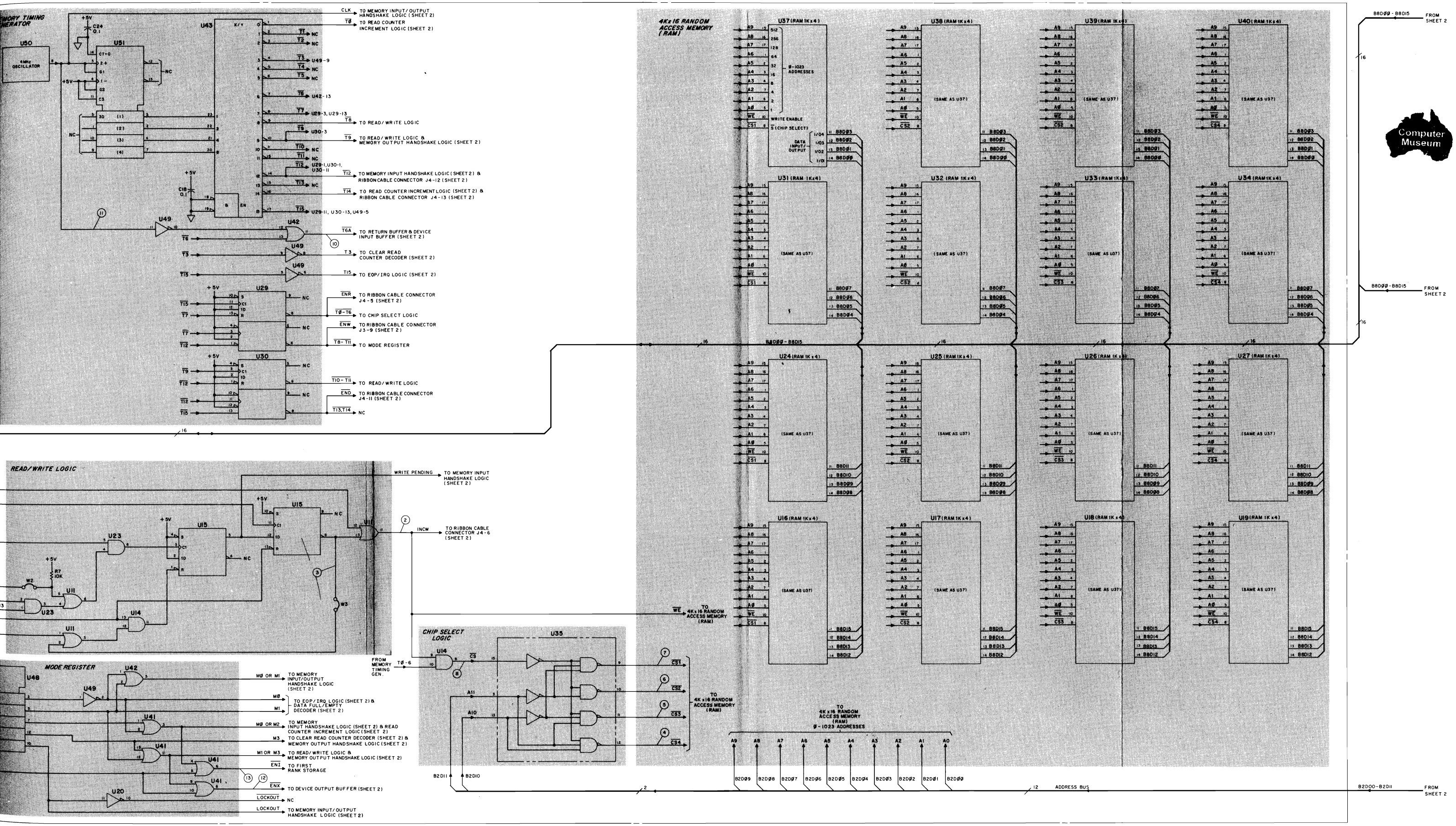


Figure 6-2 (Sheet 1). 69790B Memory Card No. 1, Schematic Diagram.

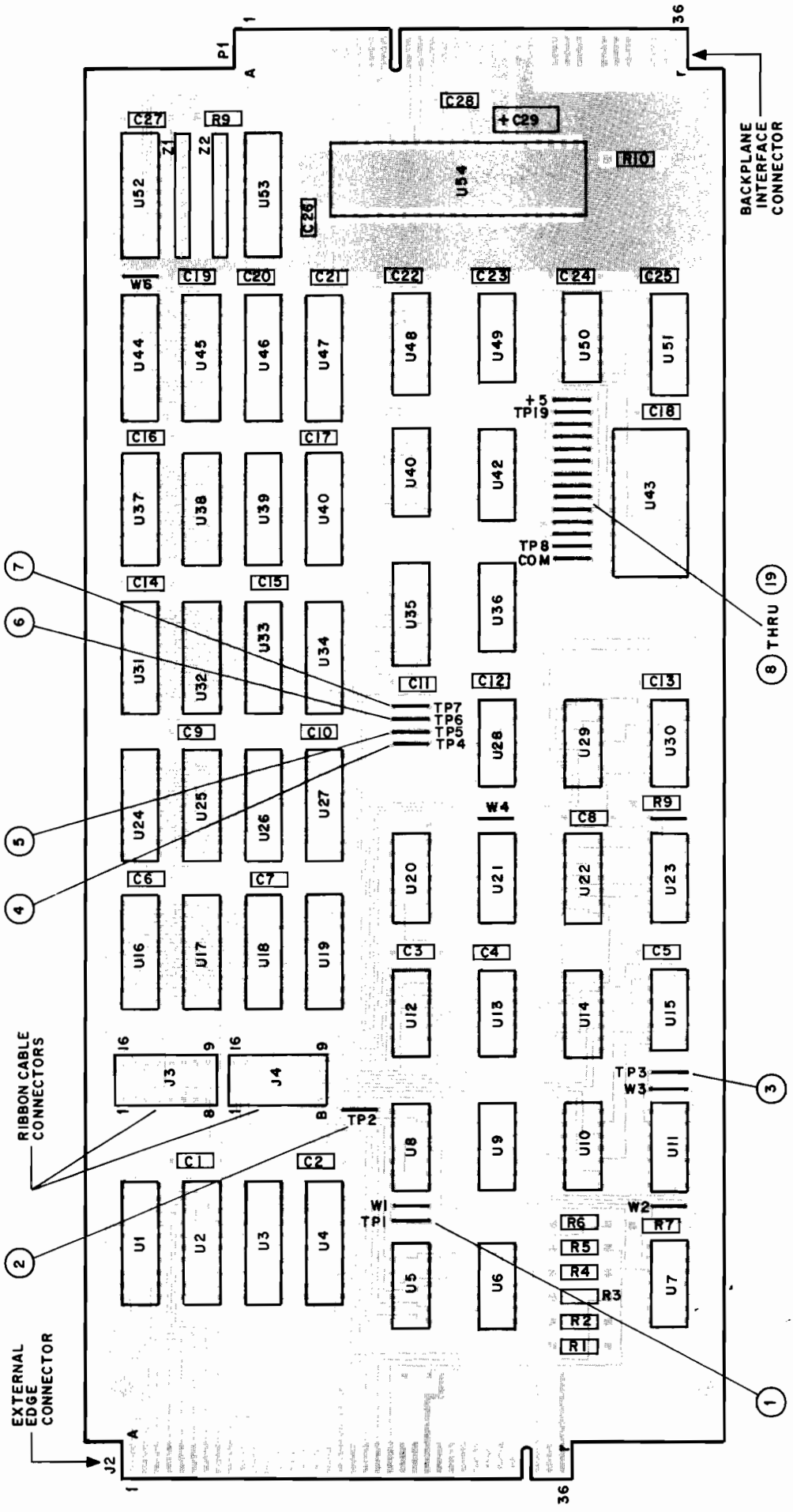


Figure 6-1. 69790B Memory Card No. 1, Component Locations.

P/O 69790B MEMORY CARD NO. 1

TO SHEET 1

B8D00 - B8D15

FROM MODE REG. (SHEET 1) $\overline{ENX}$

FROM MEM. INPUT HANDSHAKE LOGIC LIR

DEVICE OUTPUT BUFFER (D0B)

U1, U4

B8D00 B8D01 B8D02 B8D03 B8D04 B8D05 B8D06 B8D07 B8D08 B8D09 B8D10 B8D11 B8D12 B8D13 B8D14 B8D15

B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15

16 B0 - B15

DEVICE INPUT BUFFER (D1B)

U2, U3

B2D00 B2D01 B2D02 B2D03 B2D04 B2D05 B2D06 B2D07 B2D08 B2D09 B2D10 B2D11 B2D12 B2D13 B2D14 B2D15

FROM MEM. TIMING GEN. (SHEET 1) $\overline{T6A}$

RIBBON CABLE CONNECTORS

J3 P3 P4 J4

TO/FROM MEMORY CARD NO.2 FIG. 6-4 SHEET 2 (SEE NOTE 3)

$\overline{IRQ}'$ EOP' ARM' CLR $\overline{CLR}'$ EOR' CLRR $\overline{T14}$ $\overline{ENR}$ $\overline{T12}$ INCW $\overline{END}$ ALL 0's INCR ALL 1's ">"

TO READ/WRITE LOGIC (SHEET 1) & MODE REG. (SHEET 1)

FROM MEM. TIMING GEN. (SHEET 1)

FROM READ/WRITE LOGIC (SHEET 1)

FROM MEM. TIMING GEN. (SHEET 1)

FROM BACKPLANE CONNECTOR P1 (SHEET 1) +5V COM RECYCLE

TO EDGE CONNECTOR J2-23

FROM MEM. TIMING GEN. (SHEET 1) $\overline{ENW}$

B2D00 - B2D11 12

EOP/IRQ LOGIC

ARM' FROM MEM. TIMING GEN. (SHEET 1) T15 ">" FROM MODE REG. (SHEET 1) M1 MØ EOR' FROM UCC (SHEET 1) LSR $\overline{CLR}'$

U20 U14 U13 U36 U5

$\overline{IRQ}$ EOP' EOP TO EDGE CONNECTOR J2-nn

CLEAR READ COUNTER DECODER

FROM MODE REG. (SHEET 1) M3 FROM MEM. TIMING GEN. (SHEET 1) T3 CLR

U12 U13 CLRR

READ COUNTER INCREMENT LOGIC

FROM MEM. TIMING GEN. (SHEET 1) T14 $\overline{T\emptyset}$ FROM MEM. OUTPUT HANDSHAKE LOGIC READ INHIBIT DATA RCVD FROM UCC (SHEET 1) LSR FROM MODE REG. (SHEET 1) MØ OR M2 $\overline{CLR}'$

U21 U13 U28 W4 INCR READ PENDING

MEMORY INPUT HANDSHAKE LOGIC

ALL 1's FROM MODE REG. (SHEET 1) MØ OR M1 MØ OR M2 LOCKOUT FROM MEM. TIMING GEN. (SHEET 1) CLK FROM READ/WRITE LOGIC (SHEET 1) WRITE PENDING FROM MEM. TIMING GEN. (SHEET 1) $\overline{T12}$ $\overline{CLR}'$

U22 +5V RB 10K

MEMORY OUTPUT HANDSHAKE LOGIC

FROM MEM. TIMING GEN. (SHEET 1) CLK FROM MODE REG. (SHEET 1) LOCKOUT M1 OR M3 $\overline{CLR}'$

U9 W1 U6 $\overline{T9}$ ALL 0's FROM MODE REG. (SHEET 1) MØ OR M1 M3 LOCKOUT READ PAN

DATA FULL DECOD

FROM MODE REG. (SHEET 1) MØ M1 ALL 1's ALL 0's U10 U6

TO SHEET 1

B2D00 - B2D11 12

11 10 6 4 4 2

TEST POINT TABLE

TEST POINT	MNEMONIC	SIGNAL NAME
TP1	DOA	DATA OUT ACCEPTED
TP2	INC W	INCREMENT WRITE
TP3	WRITE	WRITE
TP4	CS4	CHIP SELECT 4
TP5	CS3	CHIP SELECT 3
TP6	CS2	CHIP SELECT 2
TP7	CS1	CHIP SELECT 1
TP8	CS	CHIP SELECT
TP9	RR	READ RESET
TP10	T6A	T6 TIME STATE PULSE
TP11	CLK	4MHz FREE RUNNING CLOCK
TP12	ENX	ENABLE DOB
TP13	ENI	ENABLE FIRST RANK STORAGE
TP14	STB1	STROBE 1
TP15	STB2	STROBE 2
TP16	STB3	STROBE 3
TP17	RTN0	RETURN STROBE

NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTANCE IS IN OHMS, ±5%, 1/4W; CAPACITANCE IS IN MICROFARADS; IC POWER PINS ARE AS FOLLOWS:

IC CONFIGURATION	V_{CC}	GND
14 PINS	14	7
16 PINS	16	8
20 PINS	20	10
40 PINS	40	20

2. Z1, Z2, PIN 1 IS COMMON PIN.
3. MEMORY CARDS 1 AND 2 ARE INTERCONNECTED USING RIBBON CABLE 69790-60001 (SEE FIG. 2-1).

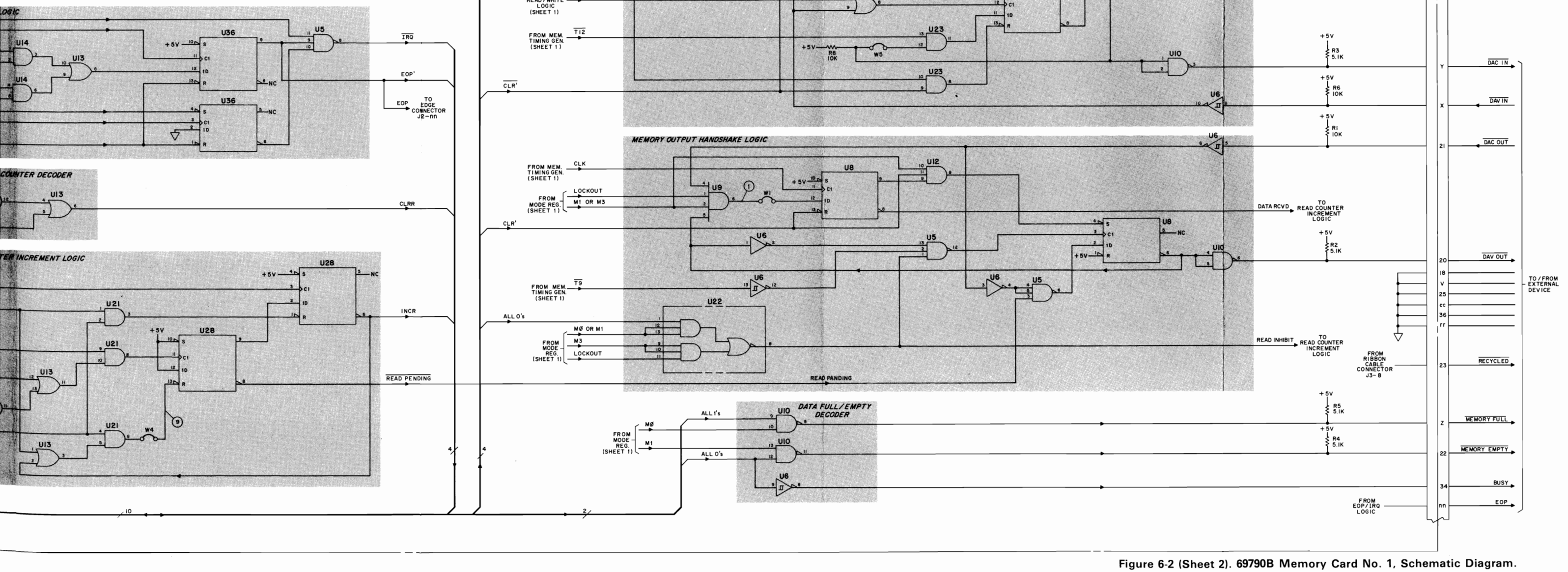
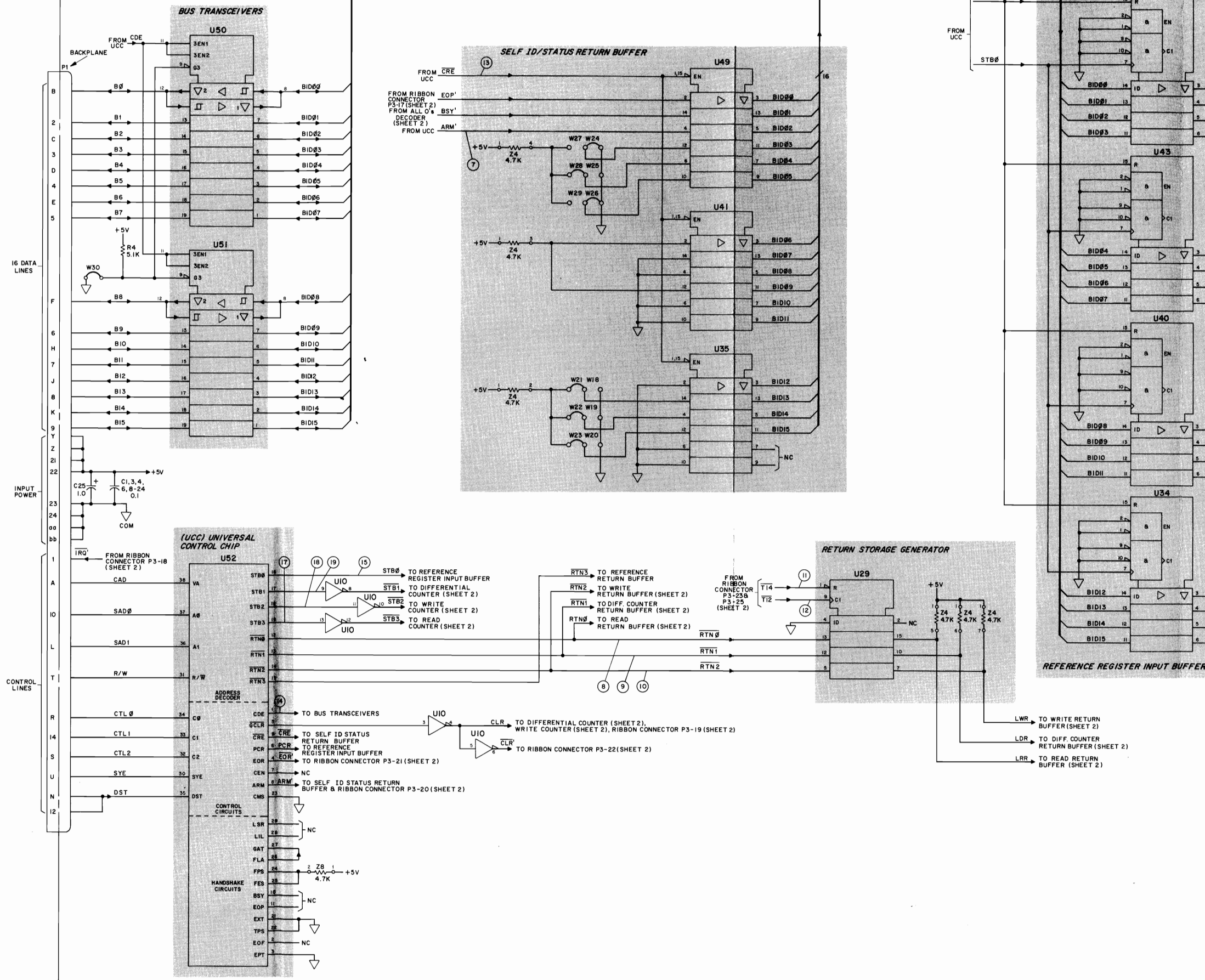


Figure 6-2 (Sheet 2). 69790B Memory Card No. 1, Schematic Diagram.

P/O 69790B MEMORY CARD NO. 2



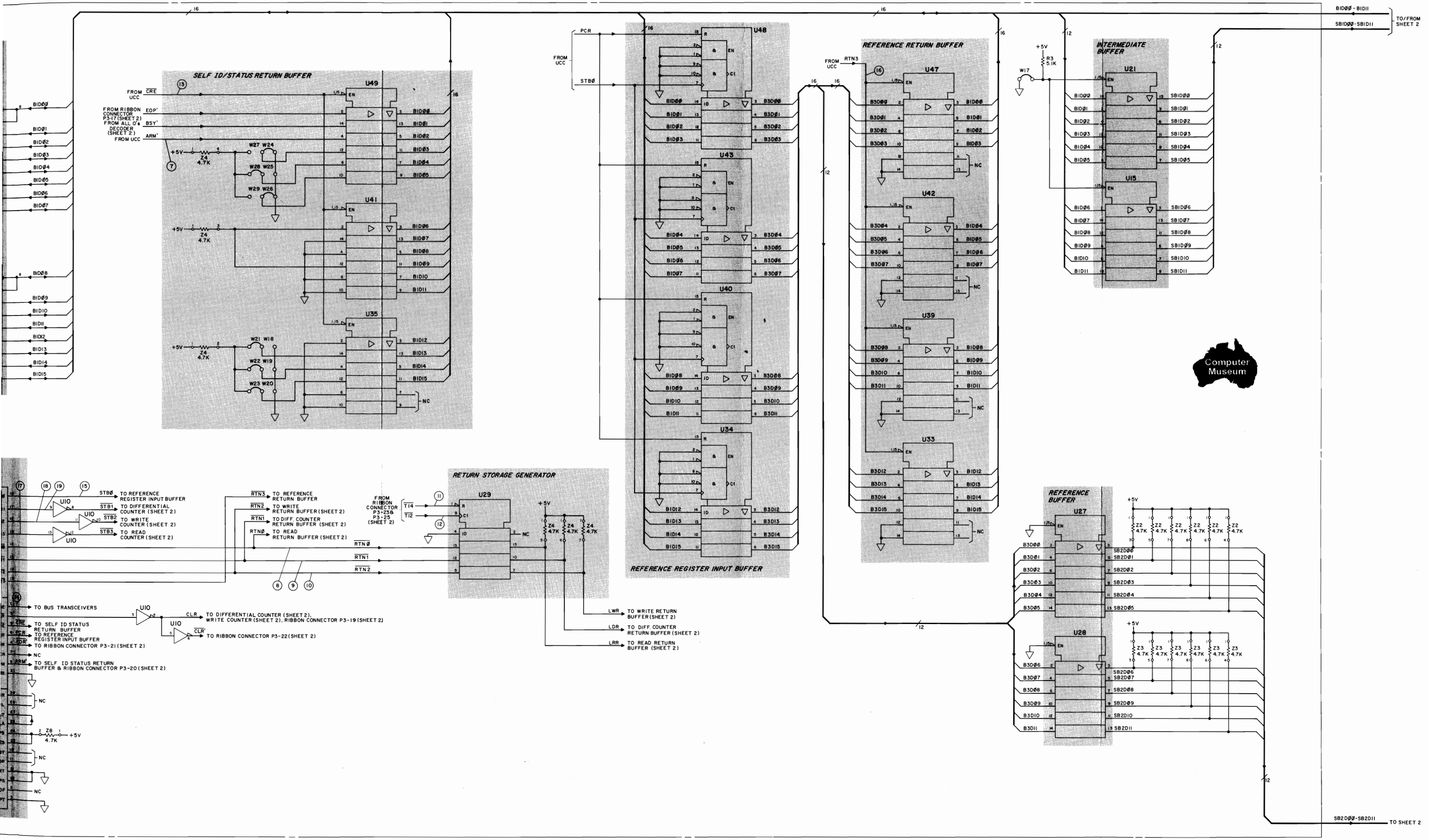


Figure 6-4 (Sheet 1). 69790B Memory Card No. 2, Schematic Diagram

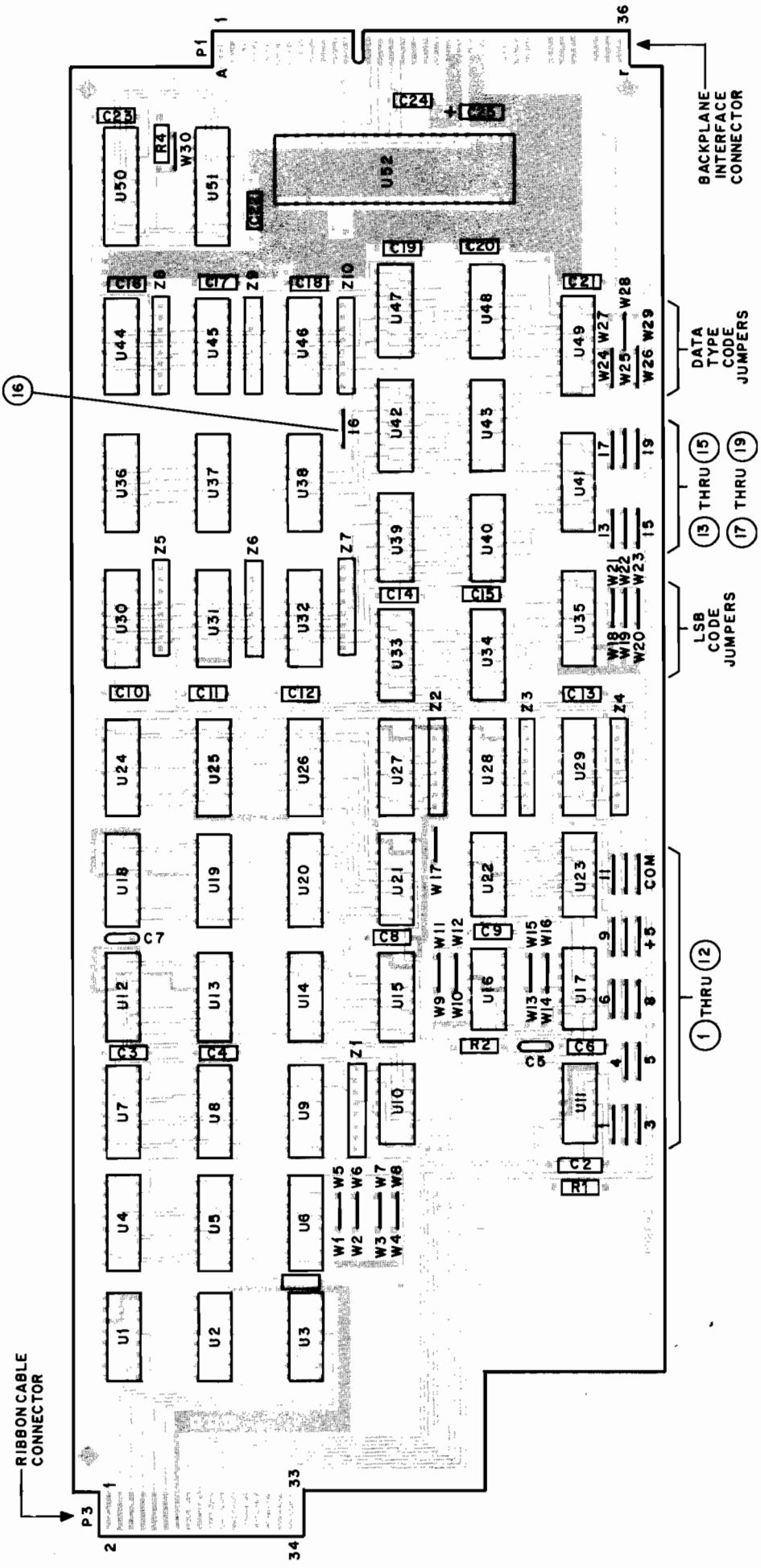


Figure 6-3. 69790B Memory Card No. 2, Component Locations.

P/O 69790B MEMORY CARD NO. 2

TO/FROM SHEET 1

BID00 - BID11 (12)

SBID00 - SBID11 (12)

DIFFERENTIAL COUNTER

FROM UCC (SHEET 1) CLR

FROM RIBBON CONNECTOR P3-28 & P3-29 INCW

INCR

FROM UCC (SHEET 1) STB1

U26 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15, ZCT=0

U20 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15, ZCT=0

U14 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15 (NC), ZCT=0

+5V

Z10 2.2K, Z10 2.2K, Z10 2.2K, Z10 2.2K

Z10 2.2K, Z10 2.2K, Z7 2.2K, Z7 2.2K

Z7 2.2K, Z7 2.2K, Z7 2.2K, Z7 2.2K

SBID00 (1) SBID01 (2) SBID02 (3) SBID03 (4) — 3D

SBID04 (1) SBID05 (2) SBID06 (3) SBID07 (4) — 3D

SBID08 (1) SBID09 (2) SBID10 (3) SBID11 (4) — 3D

B4D00 B4D01 B4D02 B4D03

B4D04 B4D05 B4D06 B4D07

B4D08 B4D09 B4D10 B4D11

DIFFERENTIAL COUNTER RETURN BUFFER

FROM UCC (SHEET 1) RTN1

FROM RETURN STORAGE GEN. (SHEET 1) LDR

U46 — R, a EN, a C1

U38 — R, a EN, a C1

U32 — R, a EN, a C1

1D

BID00 BID01 BID02 BID03

BID04 BID05 BID06 BID07

BID08 BID09 BID10 BID11

WRITE COUNTER

FROM UCC (SHEET 1) CLR

FROM RIBBON CONNECTOR P3-28 INCW

+5V

FROM UCC (SHEET 1) STB2

U25 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15, ZCT=0 (NC)

U19 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15, ZCT=0 (NC)

U13 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15 (NC), ZCT=0

+5V

Z9 4.7K, Z9 4.7K, Z9 4.7K, Z9 4.7K

Z9 4.7K, Z9 4.7K, Z6 4.7K, Z6 4.7K

Z6 4.7K, Z6 4.7K, Z6 4.7K, Z6 4.7K

SBID00 (1) SBID01 (2) SBID02 (3) SBID03 (4) — 3D

SBID04 (1) SBID05 (2) SBID06 (3) SBID07 (4) — 3D

SBID08 (1) SBID09 (2) SBID10 (3) SBID11 (4) — 3D

B5D00 B5D01 B5D02 B5D03

B5D04 B5D05 B5D06 B5D07

B5D08 B5D09 B5D10 B5D11

WRITE RETURN BUFFER

FROM UCC (SHEET 1) RTN2

FROM RETURN STORAGE GEN (SHEET 1) LWR

U45 — R, a EN, a C1

U37 — R, a EN, a C1

U31 — R, a EN, a C1

1D

BID00 BID01 BID02 BID03

BID04 BID05 BID06 BID07

BID08 BID09 BID10 BID11

READ COUNTER

FROM RIBBON CONNECTOR P3-24 & P3-29 CLRR

INCR

+5V

FROM UCC (SHEET 1) STB3

U24 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15, ZCT=0

U18 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15, ZCT=0

U12 CTRDIV16 — CT=0, 2+, 1-, G1, G2, C3, TCT=15, ZCT=0

C7 470 PF

SBID00 (1) SBID01 (2) SBID02 (3) SBID03 (4) — 3D

SBID04 (1) SBID05 (2) SBID06 (3) SBID07 (4) — 3D

SBID08 (1) SBID09 (2) SBID10 (3) SBID11 (4) — 3D

DIFFERENTIAL COUNTER ADDRESS BUFFER

+5V

Z6 4.7K

FROM RIBBON CONNECTOR P3-27 END

U9 — EN

U6 — EN

B4D00 B4D01 B4D02 B4D03 B4D04 B4D05

B4D06 B4D07 B4D08 B4D09 B4D10 B4D11

B2D00 B2D01 B2D02 B2D03 B2D04 B2D05

B2D06 B2D07 B2D08 B2D09 B2D10 B2D11

WRITE COUNTER ADDRESS BUFFER

+5V

Z1 2.2K

FROM RIBBON CONNECTOR P3-15 ENW

U8 — EN

U5 — EN

B5D00 B5D01 B5D02 B5D03 B5D04 B5D05

B5D06 B5D07 B5D08 B5D09 B5D10 B5D11

B2D00 B2D01 B2D02 B2D03 B2D04 B2D05

B2D06 B2D07 B2D08 B2D09 B2D10 B2D11

FROM RIBBON CONNECTOR P3-26 EN

FROM SHEET 1 SB2D00 - SB2D11 (12)

(10) (2) (12)

IC PART NO'S AND SUPPLY VOLTAGE PIN NO'S

NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTANCE IS IN OHMS, ±5%, 1/4W; CAPACITANCE IS IN MICROFARADS; IC POWER PINS ARE AS FOLLOWS:

IC CONFIGURATION	V_{CC}	GND
14 PINS	14	7
16 PINS	16	8
20 PINS	20	10
40 PINS	40	20

2. Z1 THRU Z10, PIN 11 IS COMMON PIN.
3. MEMORY CARDS 1 AND 2 ARE INTERCONNECTED USING RIBBON CABLE 69790-60001 (SEE FIG. 2-1)

TEST POINT TABLE

TEST POINT	MNEMONIC	SIGNAL NAME
TP1	$\overline{ENW}$	ENABLE WRITE
TP2	ENR	ENABLE READ
TP3	END	ENABLE DIFF
TP4	INC W	INCREMENT WRITE
TP5	INC R	INCREMENT READ
TP6	ALL 1's	ALL 1's
TP7	ARM'	ARM
TP8	RTN0	RETURN STROBE 0
TP9	RTN1	RETURN STROBE 1
TP10	RTN2	RETURN STROBE 2
TP11	T14	TIME STATE 14
TP12	T12	TIME STATE 12
TP13	CRE	CONTROL RETURN
TP14	CDE	CONTROL ENABLE
TP15	STB0	STROBE 0
TP16	RTN3	RETURN STROBE 3
TP17	STB3	STROBE 3
TP18	STB2	STROBE 2
TP19	STB1	STROBE 1

Figure 6-4 (Sheet 2). 69790B Memory Card No. 2, Schematic Diagram