HEWLETT PACKARD

DIGITAL INPUT/ANALOG COMPARATOR CARD MODEL 69771A

OPERATING MANUAL

FOR SERIAL NUMBERS 1908A-00101

AND ABOVE.*

*For cards with serial prefixes above 1908A-00101, a manual change page may be included.

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SECTION I
GENERAL INFORMATION

1-1 SCOPE OF MANUAL

1-2 This manual covers the installation, Pre-operation, and Theory of Operation for the Digital Input/Analog Comparator Card, Model 69771A. This manual does not include servicing instructions or information on the programming of the card. Programming examples of the Digital Input/Analog Comparator card are shown in Chapter 7 of the 6942A Multiprogrammer User's Guide. Additional documents that contain general information on I/O cards are:

- 6942A Multiprogrammer User's Guide for HP 9825/35/45 Controllers (HP 06942-90003).
- 6942A Multiprogrammer User's Guide for HP 85 Controllers (HP 06942-90011).
- 6942A Multiprogrammer User's Guide for HP 9826 Controllers (HP 06942-90013).
- 6942A Multiprogrammer Technical Data (HP 5952-4034).
- 6942A Multiprogrammer Installation and Assembly Level Service Manual (HP 6942A-90006).

1-3 Any of these documents can be ordered directly from your local Hewlett-Packard sales office. Give the applicable HP manual part number as indicated above.

1-4 DESCRIPTION

1-5 The Digital Input/Analog Comparator card has 16-input data lines which can be used in any combination to:

a. Monitor switch or relay contact closures with respect to ground.
b. Read TTL or CMOS logic levels.
c. Detect the presence of an analog signal voltage in the range −9.7 V to +9.7 V.

1-6 The input data lines connect to 16-input analog comparators which convert the input signal voltage to TTL logic levels. The TTL logic levels are transferred to the Multiprogrammer when the card is cycled. The card can be cycled by either a programmed instruction or by an External Trigger (EXT) signal.

1-7 As shipped, the input comparators are set to a threshold voltage of 1.2 V. An input voltage 15 mV above this 1.2 V threshold is converted to a logic high. An input voltage equal to or below 1.2 V (e.g. relay closure, or TTL low level) is converted to a logic low. The logic sense of the comparator outputs can be changed from positive true to negative true logic by the insertion of a jumper (W48).

1-8 A four position slide switch (S1) mounted on the card permits the User to select a different comparator reference voltage. One of these switch positions allows the User to set the reference to any value in the range from −9.7 V to 9.7 V by a potentiometer adjustment. Refer to Section III, "Comparator Alternatives" for further information.

1-9 A separate input line to each comparator is available at the edge connector. These lines allow any or all comparators to be referenced to an externally supplied voltage. All comparator outputs (digital word) are available at the edge connector for read back by the external logic.

1-10 A GATE control signal is applied to the edge connector when the card is cycled and can be used by external logic to initiate a "reading". GATE is jumpered to an input control line called FLAG to automatically store the data after it is converted to TTL levels. If the GATE/FLAG jumper is remove, the digital word will not be stored on the card until an external FLAG control signal is applied to the edge connector.

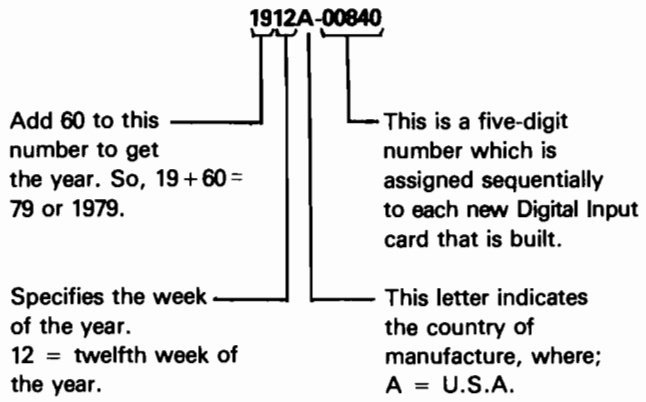
1-11 The Digital Input/Analog Comparator card also contains a separate register called first rank return buffer. This buffer is used soley to verify that data can be written to the card and read back from the card. This permits the Multiprogrammer to check the interface between the card and Multiprogrammer main memory via the backplane.

1-12 SPECIFICATIONS

1-13 Specifications and other supplemental data for the Digital Input Card are given in Table 1-1.

1-14 CARD AND MANUAL IDENTIFICATION

1-15 Hewlett-Packard I/O cards are identified by a two-part serial number, for example, 1912A-00840. This number appears on a label affixed to the component side of the circuit card. The breakdown of the serial number is explained using the example number 1912A-00840.



1-16 The first part of this serial number (year and week) indicates the last date when a significant design change was made.

1-17 Each I/O card is equipped with a handle that is marked to identify the card type (e.g. Digital Input). The handle is located at the card's outer edge and facilitates the removal and installation of the card.

1-18 OPTIONS

1-19 To obtain additional Operating Manuals when the Digital Input card is shipped, request Option 910 when ordering the card. One additional manual will be shipped with each Option 910 ordered.

1-20 ACCESSORIES

1-21 One external connector is shipped with each I/O card. Order model 14703A when extra connectors are required to fabricate cables for several different applications.

1-22 A deinsertion tool is available to remove the contacts from the connector. This tool can be ordered from Hewlett-Packard (HP P/N 8710-0690).

Table 1-1. Specifications and Supplemental Data

Input Switching Threshold: 1.2 V ±100 mV as shipped. Whether an internal or external reference is used, the switching threshold is within 15 mV of the reference voltage.

Logic Sense: Voltages 15 mV above the threshold appear as a logical 1. This logic sense can be reversed by installing **jumper W48** on the card. Installing W48 also inverts the logic sense of the comparator outputs relative to that of the data inputs.

Input Resistance of Data Inputs: 100 kΩ. (The 100 kΩ pull-up resistors at the 16 data inputs are normally connected to +5 volts through **jumper W34.** The supply can be changed to +12 volts by removing W34 and installing **W33.**).

Reference Voltage: An internal or an external supply can be used to establish a reference voltage anywhere within a ±7.7 V range.

Reference Input Current: ±500 nA maximum per input.

Comparator Outputs: In the high state, the outputs source up to 200μA at 3.8 V minimum. In the low state, the outputs sink up to 7 mA at 0.4 V maximum.

Response Time: The maximum time required for an input signal that is at least 20 mV above the switching threshold to appear at the comparator output is 5μs.

For the characteristics of the card's other inputs and outputs, see Section 7.

All output control lines at the Edge Connector are open collector and have these specifications...

Logic High = 3.7 V while sourcing 200 μA.
Logic Low = 0.5 V while sinking 7 mA.

All input control lines at the edge connector are applied to Schmitt trigger circuits and have these specifications...

Logic High = 2.0 V to 5.0 V (or no connection)
Logic Low = 0 V to 0.5 V (short to ground)

TEMPERATURE RANGE:
From 0° to +70° C operating in the mainframe (allows 15°C internal rise in temperature when operating in the mainframe at up to +55°C ambient); from −40°C to +80°C storage.

CARD DIMENSIONS: 299.722mm x 132.08mm (11.8in. x 5.2in.). +5 V Current Requirement: 309 mA.

SECTION II
INSTALLATION

2-1 INSPECTION

2-2 When the Digital Input/Analog Comparator card is received, inspect the card for any obvious defects that may have been incurred during shipment. Save the shipping carton and packing foam in the event that the card may have to be returned to Hewlett-Packard in the future.

2-3 Also check that the following items have been received with the Digital Input card:

- I/O card connector assembly. An instruction sheet is provided with the I/O card connector assembly and shows how to assemble the connector. This information is also available in Chapter 2 of the "6942A Multiprogrammer User's Guide". The parts list in Section V of this manual lists all the parts and the corresponding Hewlett-Packard part numbers for the connector assembly.
- Installation and Operation Manual (HP 69771-90003).
- If applicable, one or more manual change sheets may be included with the manual. If a change sheet is included, check to see if the change applies to the serial number of the card you received.

2-4 AS-SHIPPED JUMPER CONNECTIONS

2-5 The Digital Input/Analog Comparator card contains various jumpers that define the values of the wake-up codes, the logic level of various control signals at the edge connector, and the manner in which the input data lines are operated. Figure 6-1 in Section VI shows the location of these jumpers. The card is shipped with jumpers set to specify the values listed below:

WAKE-UP CODES:

Data Type Code = 3 (unsigned binary data); jumpers W38, W39, and W40 installed

LSB VALUE = 1 (unit); jumpers W42, W43, and W44 installed.

EXTERNAL CONTROL LINES:

Trigger Polarity Select line = logic high (jumper W51 removed).

Flag Polarity Select line = logic high (jumper W50 removed).

Flag Edge Select line = logic high (jumper W49 removed).

FLAG input line = connected to GATE output line (jumper W52 installed).

INPUT DATA LINES ARE CONFIGURED AS:

Positive true logic, (Invert/Invert Gates jumper, W48 removed). TTL logic levels, (+5 V pull-up resistor bias, jumper W34 installed). External comparator reference voltage disconnected, (jumpers W17-32 removed). 1.2 V local comparator reference voltage connected to all comparators (jumpers W1-W16 installed).

INTERNAL +12 V INPUT, jumper W53 installed.

INTERNAL −12 V INPUT, jumper W54 installed.

2-6 A card mounted slide switch, S1, is set to the following positions prior to shipment.

Position	Set To
1	ON (connects local reference voltage to comparators)
2	OFF
3	ON (selects a 1.2 V reference voltage)
4	OFF

2-7 INSTALLATION PREREQUISITES

2-8 Before you install the Digital Input card in a 6942A or 6943A chassis, consider the following prerequisite steps:

a. Determine which I/O slot will be used. An I/O card can be installed in slots 0 through 15. The card assumes the address of the slot (and unit) in which it is inserted. Also, a card in slot 0 has the highest priority, slot 1 the next highest priority, and slot 15 the lowest.

b. For the slot position selected, record the following:

1. card type.
2. card's subaddresses:
   0 (read) = to read input storage register.
   3 (read) = to read first rank return buffer.
   0 (write) = to write data to first rank return buffer.
3. card's address, where;

CARD ADDRESS = SLOT NO. + (FRAME NO. X100) + (SUBADDRESS X 0.1)

(For example, 205.0 is the card address for a card in slot No. 5, frame number 2, referencing subaddress 0 as in a read data operation.)

2-9 Once these prerequisites have been checked, you can proceed to install the card in the mainframe by performing the installation procedure in paragraph 2-10.

2-10 INSTALLATION PROCEDURE

2-11 To install the Digital Input card in the mainframe chassis, perform the following steps:

a. Turn off mainframe power.

CAUTION

To prevent an accidental short from damaging a card or a mainframe, always turn off Multiprogrammer power before installing or removing I/O cards.

b. Remove the rear cover of the mainframe by loosening the four, quarter-turn fasteners.
c. Position the card so its handle is at the bottom, and the component side of the card is toward the right.
d. Slide the card into the desired slot position until the card just touches the backplane connector.

NOTE

A notch in the card edge and a key in the connector prevent the card from being installed upside down or in an illegal slot position.

e. With the card touching the connector, rotate the card handle downward until it engages the groove at the bottom of the I/O slot. Rotate the handle upward to insert the card into the backplane connector. (To remove a card, the handle is rotated downward.)
f. Install mainframe rear cover.
g. After the card is installed, you can proceed to make a partial test of the card by performing the functional test described in the next paragraph.

2-12 FUNCTIONAL CHECKOUT

2-13 After the card is installed, the user can run either of two self tests described in the 6942A Multiprogrammer User's Guide. These tests are:

a. The Self-Test Error Dectection and Card Identifier Utility Program. This test is described in Chapter 2 of the 6942A Multiprogrammer User's Guide. This test checks the card control chip and the first rank storage register.
b. Example 7-33 in Chapter 7 of the 6942A User's Guide can be run to test the logic levels of the input data lines.

SECTION III
PRE-OPERATING INSTRUCTIONS

3-1 INTRODUCTION

3-2 The purpose of this section is to provide the User with additional card information that may be required for any of the following reasons:

- The User wishes to change the card jumpers from their "as shipped" positions to some new positions.
- The User wishes to change the bias voltage at the comparator inputs.
- The User requires additional information on the edge connector I/O signals.

3-3 Since any of the above reasons affect the operation of the card, the information in this section should be read before implementing any card changes. The following topics are covered in the order mentioned:

- Definition of all card jumpers.
- Definition of comparator reference voltage alternatives.
- Card's External Edge Connector.
- External I/O Control Signals.

3-4 CARD JUMPERS

3-5 As mentioned in Section I, the Digital Input card is shipped with certain jumpers in place. When the User wishes to change a jumper(s), the information in the following paragraphs should be referenced to find the location of the applicable jumper(s), and also, to see what other jumper arrangements are possible. The jumpers are shown in Figure 6-1 of Section VI and are described in the following order:

a. Bidirectional Data Transceivers.
b. External I/O control signal jumpers.
c. Input data line jumpers.
d. Comparator reference voltage jumpers.
e. Invert/invert gates jumper.
f. Wake-up code jumpers.
g. External + 12 V and − 12 V jumpers.

3-6 Bidirectional Data Transceivers Jumpers W35

3-7 This jumper is installed at the factory and, normally, is never removed. This jumper establishes pin 9 of tri-state integrated circuits U9 and U25 (see Figure 6-2) at ground. With pin 9 grounded, the open or isolated state of the transceivers is not used. Jumper W35 is temporarily removed during factory testing to allow the outputs of the transceiver to assume an open state for test purposes.

3-8 External I/O Control Signal Jumpers

3-9 The following paragraphs describe those jumpers that affect the control signals at the external edge connector.

3-10 **Trigger Polarity Select Jumper, W51.** This jumper is removed prior to shipment making the Trigger Polarity Select (TPS), control line a logic high. If this jumper is installed, the TPS control line is held at a logic low level. The purpose of the Trigger Polarity Select signal is discussed in Table 3-3.

3-11 **Flag Polarity Select Jumper, W50.** This jumper is removed prior to shipment making the Flag Polarity Select (FPS) control line a logic high. If this jumper is installed, the FPS control line is held at a logic low level. The purpose of this control signal is discussed in Table 3-3.

3-12 **Flag Edge Select Jumper, W49.** This jumper is removed prior to shipment making the Flag Edge Select (FES) control line a logic high. If this jumper is installed, the FES control line is held at a logic low level. The purpose of this control signal is discussed in Table 3-3.

3-13 **Gate/Flag Jumper, W52.** This jumper is installed when the card is shipped. With this jumper installed, the GATE output control line is connected directly to the FLAG input control line. This jumper can be removed by the customer if external handshaking is desired. Further information is given in Table 3-3.

3-14 Input Data Line Jumpers (See Figure 3-1)

3-15 **+5 V Pull-Up Resistor Jumper, W34.** This jumper is installed when the card is shipped and connects all input data line, pull-up resistors to the + 5 V supply voltage.

3-16 **+12 V Pull-Up Resistor Jumper, W33.** This jumper is removed prior to shipment. This jumper can be installed in place of jumper W34 when a + 12 V pull-up bias voltage is required.

3-17 Comparator Reference Voltage Jumpers

3-18 **Local Comparator Reference Voltage.** Jumpers W1 through W16 are all installed when the card is shipped. These jumpers connect the selected local reference voltage to each comparator's reference input. The local reference voltage is selected by card mounted switch, S1 (Refer to paragraph 3-30). The local reference voltage can be removed from any or all comparator inputs by removing the applicable jumper(s).

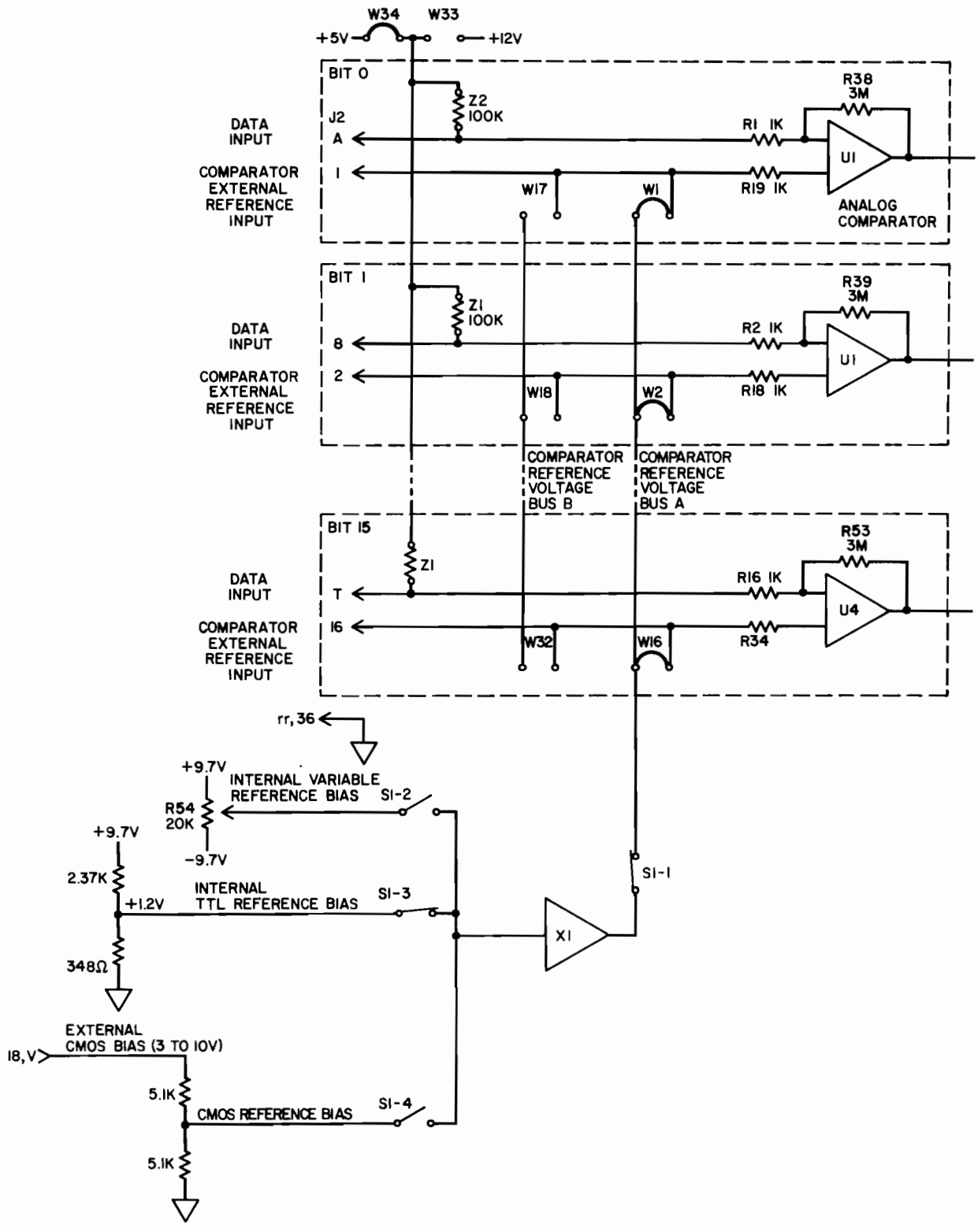


Figure 3-1. Input Data Line Jumpers (As Shipped Configuration)

3-19 **External Comparator Reference Voltage.** An external reference voltage can be applied to any of the input comparator in lieu of the local reference voltage. The external reference voltage is applied to the card at the external edge connector (pins 1 through 16) via a separate input line. Each comparator can have a different external reference voltage, or any number of comparators can share the same external voltage.

3-20 External +12 V and −12 V Jumpers

3-21 The cards input comparators are normally biased by a ±12 V mainframe supply. **Jumpers W53 and W54** make the connections to this supply. If necessary, the permissible range of comparator reference voltages can be widened by using an external ±15 V comparator bias supply. To do so, remove **jumpers W53 and W54** and install W55 and **W56**. Make connections as shown on Figure 3-2.

3-22 Invert/Invert Gates Jumper, W48.

3-23 This jumper is removed when the card is shipped. With W48 removed, the comparator outputs are applied to the external edge connector and to the storage register as positive true TTL logic levels. With jumper W48 installed, the comparator TTL logic levels are converted to negative true logic levels.

3-24 Wake-Up Code Jumpers

3-25 These jumpers determine the data type and LSB wake-up codes that are read from the card and stored in memory after power turn on. The user can override the values stored in memory by using a Set Format (SF) instruction. This is useful in applications that require a data format code or LSB value different from the values set at the factory. Any of the data types of Table 3-1 can be used. Programmed LSB values are not limited to those in Table 3-2. Any desired LSB value between 0.001 and 65.535 can be programmed. This allows the user to express programmed data in units appropriate to the process to which the card is dedicated.

3-26 If a new Data Type or LSB code will always be used, the jumpers on the card can be changed to reflect these new codes. This is more efficient than having the software constantly override the factory set values.

3-27 **Data Type Code Jumpers, W39 through W44.** These jumpers specify the data type code sent to the Multiprogrammer as part of the wake-up code sequence. The Digital Input card is shipped with jumpers W39, W41, and W43 installed and, jumpers W40, W42, and W44 removed. The Multiprogrammer interprets these jumpers as data type code =3 meaning an unsigned binary number.

3-28 These jumpers can be changed to specify a different data type code. For example, data type code = 7 could be selected to program a bit pattern in octal form. Table 3-1 shows which jumpers must be in and which jumpers must be removed to select other data type codes.

3-29 LSB Code Jumpers, W45 through W50. The Digital Input card is shipped with LSB Code jumpers, W48, W49, and W50 installed and W45, W46 and W47 removed. These jumpers specify a LSB code 1 (unity). Table 3-2 shows the other valid LSB Codes and required jumpers.

3-30 Analog Comparator Reference Voltage Alternatives

3-31 As shipped, all analog comparators are referenced to 1.2 V. If a different comparator reference voltage is required, the User can remove the present reference voltage and choose one or a combination of the following alternatives:

A. To select a threshold voltage in the range from −9.7 V to +9.7 V.
   a. Set position 3 of switch S1 to OFF.
   b. Set position 2 of switch S1 to ON.
   c. Adjust card potentiometer R54 to the voltage value desired. This voltage can be measured at any of the numbered pins at the edge connector.

B. To select a reference voltage for CMOS input logic levels.
   a. Set position 3 of switch S1 to OFF.
   b. Set position 4 of switch S1 to ON.
   c. Connect the external CMOS bias supply voltage to pin 18 or V at the edge connector. This voltage is divided in half by a voltage divider network on the card and is then first applied to the comparators.
   d. The input data lines are connected to a +5 V pull-up resistor bias. If a 12 V pull-up resistor bias is required, jumper W34 can be removed and jumper W33 installed to connect the input data lines to the higher 12 V bias.

C. To select an externally supplied reference voltage.
   a. If the external reference voltage is to be applied to all comparators, first set position 1 of switch S1 to OFF (This disconnects the local reference supply from all comparator inputs). Perform step (b) next.

      If only a few comparators are to operate with the externally supplied reference, remove the appropriate jumpers (W1-W16) from those comparators that will receive the external reference. Perform step (b) next.

   b. Apply the external reference voltage to the applicable numbered pins at the edge connector. If more than one comparator is to receive the same external reference voltage, the reference voltage need only be applied to one pin and then jumpers W17-W32 (as applicable) can be installed to distribute this voltage.

Table 3-1. Data Type Code Jumpers

DATA TYPE CODE	DESCRIPTION	JUMPER ARRANGEMENT					
		W8	W7	W6	W5	W4	W3
1	Programmed positive or negative number is stored on card in two's complement form.	Out	Out	Out	In	In	In
2	Programmed positive or negative number is stored on the card in sign-magnitude form.	Out	Out	In	In	In	Out
3*	Programmed positive or negative number is stored Stored on card in unsigned binary form.	Out	In	Out	In	Out	In
4	(Special autorange code used only with 69736A Timer/Pacer Card).						
6	Programmed positive number is stored on card in unsigned BCD form.	In	Out	In	Out	In	Out
7	Programmed octal integer is stored on card in unsigned binary form.	In	In	Out	Out	Out	In

*When the card is shipped, its jumpers are arranged to select the starred data type when power is applied to the system.

Table 3-2. LSB Code Jumpers

LSB CODE	LSB VALUE	JUMPER ARRANGEMENT					
		W42	W43	W44	W45	W46	W47
0	0.001	Out	Out	Out	In	In	In
1	0.025	Out	Out	In	In	In	Out
2	0.1	Out	In	Out	In	Out	In
3	0.5	Out	In	In	In	Out	Out
4	0.01	In	Out	Out	Out	In	In
5	0.05	In	Out	In	Out	In	Out
6	0.005	In	In	Out	Out	Out	In
7*	1.0	In	In	In	Out	Out	Out

*When the card is shipped, its jumpers are arranged to select the starred LSB value when power is applied to the system.

3-32 CARD'S EXTERNAL EDGE CONNECTOR

3-33 One dual 36-pin edge connector is supplied with each I/O card for interfacing field wiring to the card. Instructions for making up the mating connector and hood assembly are provided in Chapter 2 of the 6942A User's Guide.

3-34 The pin assignments of the input and output signals available at the edge connector supplied with the card are shown in Figure 3-2. The lettered pins are on the component side of the card, numbered pins on the opposite side.

3-35 EXTERNAL I/O CONTROL REFERENCE VOLTAGE SIGNALS (Figure 3-3)

3-36 Table 3-3 describes the control signals and bias voltages which interconnect between the Digital Input card and the Customer's equipment. The electrical specifications for these signals are given in Table 1-1 of Section I. The pin numbers given in Table 3-3 correspond to those on the I/O Edge connector shown in Figure 3-2.

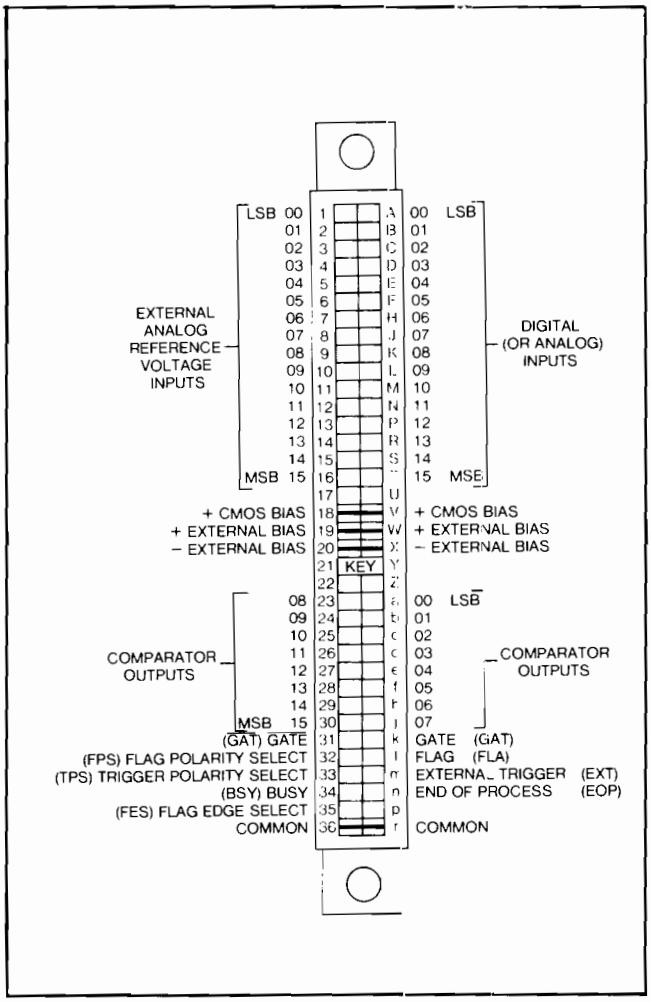


Figure 3-2. Digital Input Card, External Edge Connector

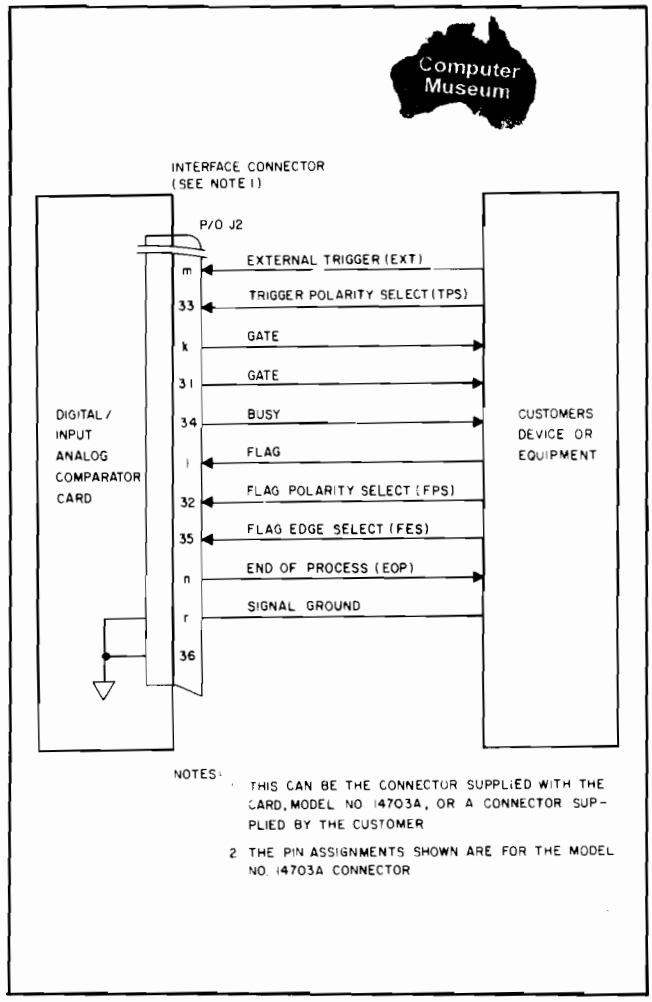


Figure 3-3. External I/O Control Signals, Interface Diagram

Table 3-3. Card's External I/O Control Signals

I/O Control Signal	Pin No.	TTL Level	Description
TRIGGER POLARITY SELECT also TPS (card input)	33	High	With pin 33, at a logic high, a low-to-high transition of the EXTERNAL TRIGGER line cycles the card.
		Low	With pin 33 low (or jumper W51 installed), a high-to-low transition of the EXTERNAL TRIGGER line cycles the card.
EXTERNAL TRIGGER also EXT (card input)	m	edge sensitive	This signal can be used to cycle the card externally. For example, after a Write First (WF) rank instruction is issued at the Controller. The TRIGGER POLARITY SELECT line determines the triggering edge.
BUSY (card output)	34	High	Busy goes high when the card is cycled either by an instruction or externally by the EXT. While BUSY is high, the input data are not reliable.
		Low	Busy goes low when FLAG goes high.
GATE (card output) also GAT	k	High	Goes high when the card is cycled. Can be used to initiate a meter reading operation.
		Low	Goes low when FLAG is received.
$\overline{\text{GATE}}$ (card output) also $\overline{\text{GAT}}$	31		Logical inverse of GATE signal at pin kk.
FLAG POLARITY SELECT also FPS (card input)	32	High	With pin 32 high, a low-to-high transition of the FLAG control signal is required to clear BUSY and set EOP.
		Low	If jumper W50 is installed, or if a low logic level is applied to pin 32, a high-to-low transition of the FLAG control signal is required to set EOP.
FLAG (card input)	1	Edge sensitive trigger	A low-to-high or high-to-low FLAG (determined by FPS) signal sets EOP and clears the GATE and BUSY control lines. FLAG is jumper connected to the GATE control line.
FLAG EDGE SELECT (card input) also FES	35	High	With pin 35 high, a low-to-high transition of the FLAG input line causes a high going LOAD INPUT LATCH (LIL) signal. LIL is generated by the UCC on the card.
		Low	If jumper W49 is installed or if pin 35 is low, a high-to-low transition of the FLAG input line causes a high going LOAD INPUT LATCH (LIL) signal.
END-OF-PROCESS also EOP (card output)	n	High	Goes high when Busy goes low. EOP remains high for a minimum of 2μs and stays high for a time dependent on the program. Pin n going high can be used as an indication that the operation is completed and the data lines can be read.
		Low	EOP is set low by the Multiprogrammer in response to an interrupt request.

Table 3-3. Card's External I/O Control Signals (cont.)

I/O Control Signal	Pin No.	TTL Level	Description
16-External Reference Voltage input lines	1-16	Reference voltage	These lines connect to the 16-input comparators. Any or all lines can be used to supply a reference voltage to the comparators
+ 12 V Reference Voltage (card input)	W, 19	dc	External + 12 V to + 15 V bias.
− 12 V Reference Voltage	X, 20	dc	External − 12 V to − 15 V bias.
+ CMOS Reference Voltage (card input)	V, 18	dc	This input is used when one or more input lines are monitoring CMOS logic levels. The CMOS bias supply voltage is applied to pin V or 18 and a half this voltage will be applied to the comparator threshold input when switch S1 set to position.
COMMON	rr, 36		Signal return for all control signals and data lines.

SECTION IV
THEORY OF OPERATION

4-1 INTRODUCTION

4-2 This section explains the theory of operation for the Digital Input/Analog Comparator card. The theory assumes that the reader is familiar with the instruction set and the basic operation of the 6942A Multiprogrammer. First, a brief description is given covering the basic operation and features of the card. A detailed block diagram discussion then follows. This section concludes with an example of the processing of an input instruction.

4-3 OVERALL OPERATION

4-4 Power Turn-On

4-5 When power is applied to the Digital Input Card, the circuits on the card are first cleared. Then a self test is initiated by the Multiprogrammer to test the circuits of the Digital Input card. The self-ID, data type, size, and LSB parameters of the card are read and stored in the Multiprogrammer memory as part of the wake-up sequence.

4-6 Monitoring and Conversion of Input Voltage Levels

4-7 Immediately after power turn-on, analog comparators begin monitoring the 16-input data lines at the edge connector. As shipped, all input data lines are connected via pull-up resistors to +5 V, and every comparator is referenced to a 1.2 V threshold voltage. With no input voltages applied to the card, the comparator outputs are at high TTL logic levels. A comparator produces a low TTL logic level if the input voltage is equal to or less then the 1.2 V threshold voltage (or below whatever value the threshold voltage is set to if the "as shipped" value of 1.2 V is changed). With 1.2 V as the threshold voltage, any of the following inputs will be converted to a TTL logic low level:

- a switch or relay contact closure with respect to ground.
- a low TTL or low CMOS logic level.
- any analog signal that goes below 1.2 V.

4-8 The comparator outputs comprise a 16-bit data word that always reflects the conversion levels of the input data lines. This data word is applied to the edge connector so the external logic can read the comparator outputs. The 16-bit word is also applied to a storage register but is not loaded into it until after the card is cycled.

4-9 Initiating a New Data Reading

4-10 A new data reading is initiated when the card is cycled by either a Controller issued instruction, or externally, by an EXTERNAL TRIGGER signal. Cycling the card produces high going BUSY and GATE signals (see Figure 4-1) which go to the edge connector.

4-11 BUSY indicates that an operation is currently in progress. GATE and its complement, $\overline{\text{GATE}}$) are ancillary signals that are available to trigger the new data reading. For example, GATE could be used to trigger a "take a reading" operation. When the results of the new data readings are placed on the input data lines to the card, the analog comparators immediately convert the input voltage levels to TTL logic levels forming a 16-bit data word.

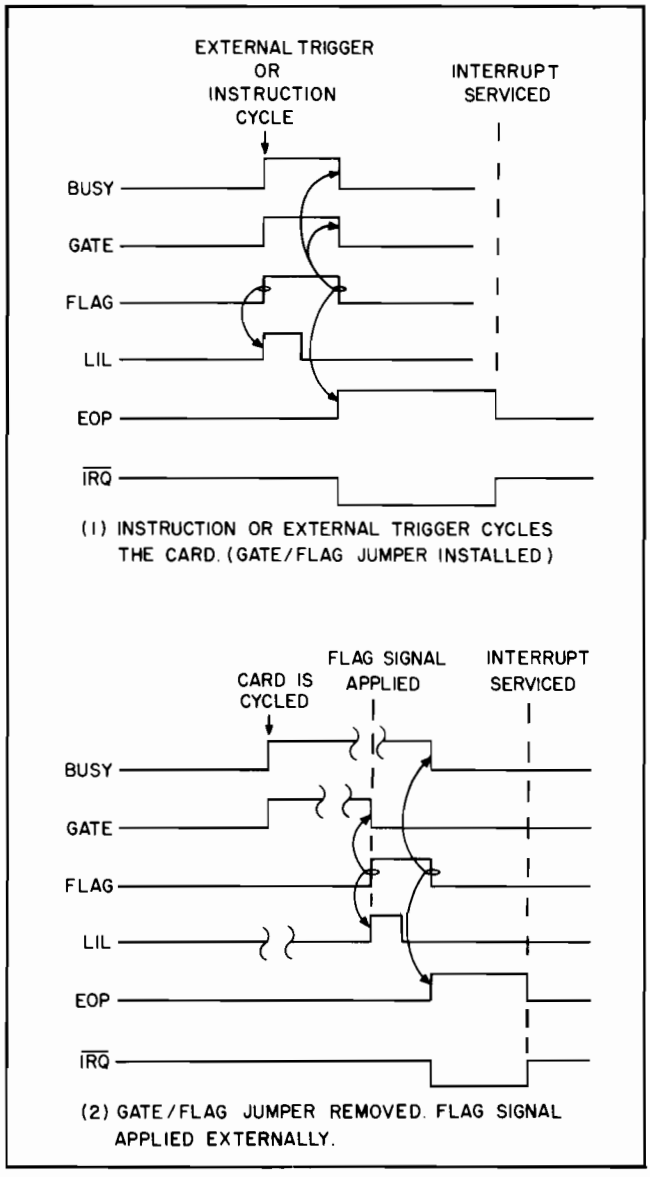


Figure 4-1. Card Cycling and BUSY/EOP Timing

4-12 Storing the Input Data

4-13 The input data word is stored on the card when a FLAG control signal at the edge connector goes high after the card has been cycled. Since the FLAG control line is jumpered (W52) to the GATE control line, data storage takes place automatically when the card is cyled. (If the User removes jumper W52, then the FLAG signal must be applied to the edge connector to initiate data storage). When the FLAG control signal occurs, these events take place simultaneously:

a. The 16-bit data word from the analog comparators is loaded into a storage register for subsequent transfer to the Multiprogrammer.
b. BUSY and GATE signals go low.
c. An End-Of-Process (EOP) signal goes high and is sent to the edge connector. EOP indicates that the operation is completed and the converted input data has been loaded into the storage register.
d. If the card is ARMED, an interrupt request (IRQ) is sent to the Multiprogrammer to alert the program that the card has data to be read by the Multiprogrammer. All input instructions except the Read Value (RV) instruction set ARM when they execute. ARM can be set with a separate Arm Card (AC) instruction.

4-14 When the interrupt request is generated by the card, the Multiprogrammer responds by clearing the ARM, EOP, and GAFF flags. The GAFF flag is internal to the Universal Control Chip on the card and is set by instructions, such as; IP, II, IE, and CY to allow mutliple cards to be cycled in parallel (or simultaneously). Refer to Chapter 4 in the 6942A Multiprogrammer User's Guide for more infromation on cycling cards in parallel.

4-15 Self-ID/Status Word

4-16 When the Multiprogrammer performs a self test, or when the controller issues a Read Status (RS) instruction, the card returns a 16-bit status word to the Multiprogrammer. This word contains information on the operational status of the card and shows how the card is hardware configured. The status word is discussed in more detail in the detailed block diagram discussion.

4-17 DETAILED BLOCK DIAGRAM DISCUSSION (Figure 4-2)

4-18 The Digital Input/Analog Comparator card consists of the following functional circuits:

a. Universal Control Chip (UCC).
b. Data Line Comparators.
c. Local Comparator Reference Voltage Supply.
d. Reference Voltage Selection.
e. Signal Conditioning.
f. Clamping Diodes.
g. Diode Bias.
h. Invert/Invert Gates.
i. Output Buffers.
j. Input Data Storage.
k. Tri-state Bidirectional Data Transceivers.
l. First Rank Return Buffers.
m. Self-ID/Status Return Buffers.

4-19 When the Digtial Input/Analog Comparator card is installed in a slot position in the Multiprogrammer, 6942A, or in the Extender chassis, 6943A, the card is assigned the address of that slot position. Once installed, the card connects to: the data lines (B0-B15), the ocntorl liens, and to the power input lines of the backplane.

4-20 The following paragraphs describe the functional circuits shown in Figure 4-2. The functional schematic in Section VI should also be referenced.

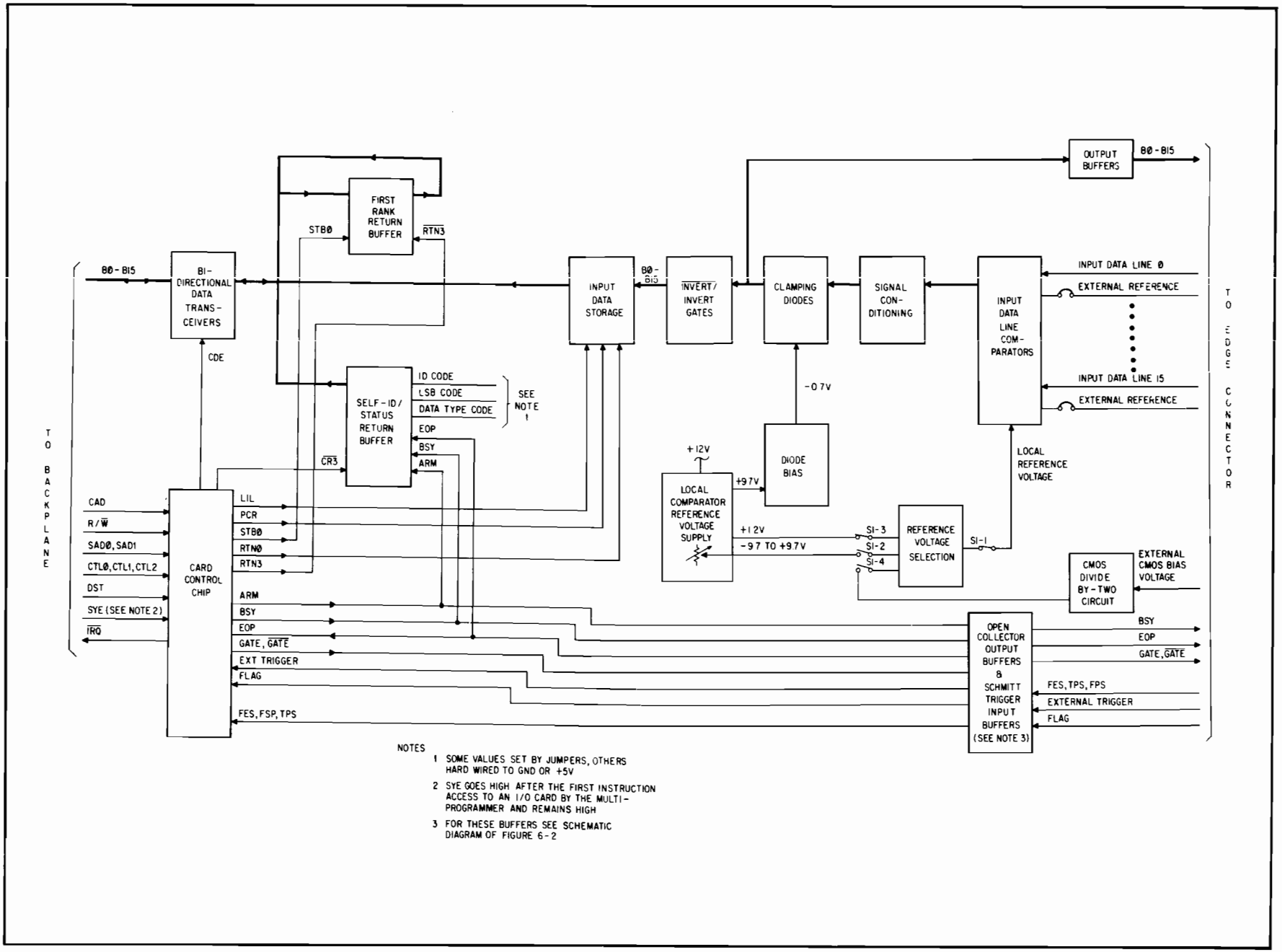
4-21 Universal Control Chip (UCC)

4-22 This control chip (U30) supervises all the operations taking place on the Digital Input/Analog Comparator card. The UCC establishes the timing sequence for the various control signals used on the card.

4-23 When power is applied to the card, a PCR control signal goes high and clears all circuits on the card. The card is then ready to process any instruction issued at the controller that addresses the card. When an instruction is issued, the following input control lines set up the UCC for a particular operation:

a. CAD - This is the card address line which goes high to select the Digital Input card when the card is addressed in an instruction.
b. R/W - This is the read/write line. It is high for a Read Value, Read Status instruction or an input data operation and is low for a write operation.
c. SAD0, SAD1 - These two lines supply a subaddress to the card. For a read data operation , subaddress 0 (binary 00) or 3 (binary 11) is sent. For a write operation, subaddress 0 (binary 00) is sent.
d. CTL0, CTL1, CTL2 - These lines supply a 3-bit control code to the UCC to indicate what operation is to be performed. Depending on the instruction issued, one or more codes are sent in succession.

4-24 The data values on the above control lines are loaded into the UCC when a data strobe (DST) pulse occurs. This data is then decoded to produce the various control signal outputs required for the indicated operation. A description of these control signals as they relate to the function being performed is included in the following paragraphs.



NOTES

1. SOME VALUES SET BY JUMPERS, OTHERS HARD WIRED TO GND OR +5V
2. SYE GOES HIGH AFTER THE FIRST INSTRUCTION ACCESS TO AN I/O CARD BY THE MULTI-PROGRAMMER AND REMAINS HIGH
3. FOR THESE BUFFERS SEE SCHEMATIC DIAGRAM OF FIGURE 6-2

Figure 4-2. Digital Input/Analog Comparator Card, Detailed Block Diagram

4-25 Data Line Comparators

4-26 There are 16 data line comparators. Each comparator has two inputs; one input monitors the data line from the edge connector, the second establishes the threshold voltage for the comparator. When the voltage level on the input data line exceeds the threshold voltage by 15 mV, the comparator output is a logical one. When the input voltage is below the threshold voltage the comparator output is a logic low. The threshold voltage applied to the comparators can originate from one of two sources: (1) an on card local reference supply or, (2) an externally supplied bias applied to the edge connector.

4-27 Local Comparator Reference Supply

4-28 The reference supply circuit consists of zener diode, VR1, operational amplifiers, U6, U7, U5, and a four position slide switch, S1. Zener diode VR1 develops a precise 6.2 V reference voltage from the +12 V supply line. Operational amplifiers, U7 and U6, convert the 6.2 V reference voltage to complementary reference voltages of +9.7 V and −9.7 V respectively.

4-29 Comparator Reference Voltage Selection

4-30 The circuit provides one of three reference voltage alternatives to the user. Regardless of which reference voltage is selected, position 1 of switch S1 (on the card) must be ON to route the voltage to the comparator input. Jumpers W1-W16 at the input data lines determine which comparators receive the reference voltage.

4-31 The 9.7 V reference is applied to voltage divider network R36 and R37 to produce a fixed 1.2 V threshold for the comparators. This voltage is selected when position 3 of switch S1 is set to ON.

4-32 Both the +9.7 V and −9.7 V reference voltages are applied to opposite terminals of potentiometer R54. By adjusting this card mounted pot, the user can set the threshold voltage to any value in the range from −9.7 V to +9.7 V position 2 of switch S1 must be ON to apply this voltage to the comparators.

4-33 CMOS Divide By Two

4-34 When any input data line is operating with CMOS logic, the external CMOS bias supply voltage can be applied to the card at pin 18. This voltage is divided in half by voltage divider network R17 and R18. With position 4 of switch S1 selected, all comparators jumpered to receive the CMOS reference voltage will receive 50% of the externally applied CMOS bias voltage.

4-35 Signal Conditioning

4-36 In series with each comparator output is a parallel network consisting of a resistor and capacitor. The purpose of this network is to improve the switching response time of the TTL logic levels produced by the comparators.

4-37 Clamping Diodes

4-38 Connected in parallel to each comparator output line is a diode which is biased at 0.7 V. The diode acts as a voltage clamp to prevent the comparator outputs from going below zero volts (or negative).

4-39 Diode Bias

4-40 The diode bias is developed by operational amplifier U8 and transistor Q1. This circuit develops a +0.7 V bias at the diode anode to offset the −0.7 V cathode to anode silicon drop across the diode.

4-41 Invert/Invert Gates

4-42 These are exclusive NOR gates which permit the logic sense of the TTL logic levels from the comparators to be inverted before they are applied to the edge connector and to the storage register. Inversion occurs when jumper W48 is installed, otherwise, the comparator outputs are stored in positive true format.

4-43 Output Buffers

4-44 These are open collector AND gates that buffer the comparator outputs before they are applied to the edge connector.

4-45 Input Data Storage

4-46 Initially, this register is cleared on power turn on. It is loaded with the 16-bit TTL data word from the comparators when a load input latch (LIL) control signal occurs. LIL is produced when the FLAG control signal is received after the card has been cycled. If the FLAG EDGE SELECT (FES) line at the edge connector is high, LIL goes high on the leading edge of FLAG. If FES is low, LIL goes high on the trailing edge of FLAG.

4-47 The contents of this register are transferred to the Multiprogrammer by an input instruction which references subaddress zero. Subaddress zero results in a low going $\overline{\text{RTNO}}$ pulse which places the content of the register on the B0-B15 lines to the backplane via the bi-directional transceivers.

Digital Data Word Sent to the Multiprogrammer

Line 15	Line 14	Line 13	Line 12	Line 11	Line 10	Line 9	Line 8	Line 7	Line 6	Line 5	Line 4	Line 3	Line 2	Line 1	Line 0

A bit position can be either a "0" or a "1"

0 = the input voltage level was below the established threshold voltage.
1 = the input voltage level was at least 15 mV above the threshold voltage.

4-48 Tri-State Bidirectional Data Transceivers

4-49 The tri-state bidirectional transceivers control the direction of data flow to and from the card over the B0-B15 data lines. A CDE control signal is used to switch the direction of the data lines. During a write operation, control signal CDE is low and the B0-B15 data lines are connected to the input of the first rank return buffers. During a read operation, CDE goes high and the B0-B15 data lines are connected to the output of the first rank return buffers and to the output of the self-ID/status return buffer. Although the transceivers are tri-state logic, jumper W35 establishes pin 9 at ground so that the isolated or high impedance state is never used.

4-50 First Rank Return Buffers

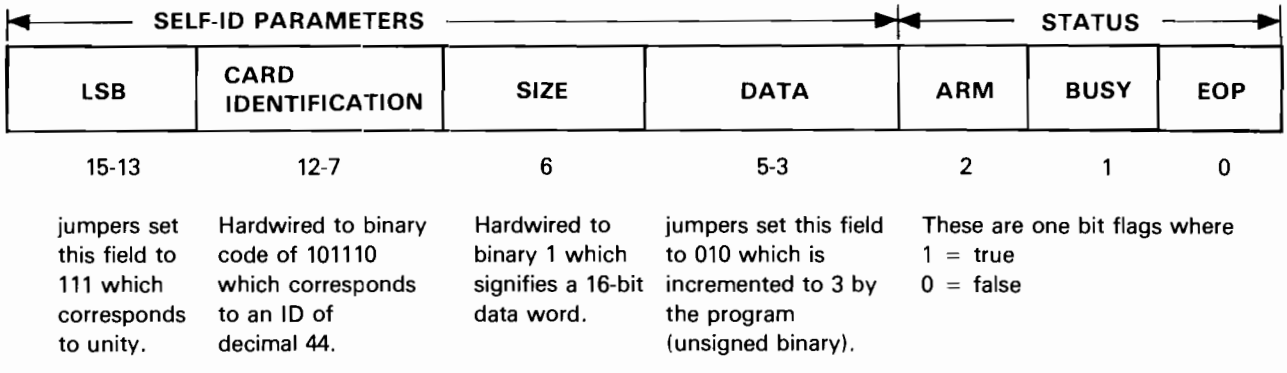
4-51 This buffer is loaded during self test when an Output instruction is issued referencing subaddress 0. STB0 is decoded from the SAD0, SAD1 lines to load the buffer. When a Read Value (RV) instruction is issued referencing subaddress 3, the SAD0, SAD1 lines are decoded to produce a low RTN3 logic level. This control signal enables the tri-state output of the first rank return buffers. CDE is also high and the data word in first rank storage is sent to the Multiprogrammer via the first rank return buffers.

4-52 Self-ID/Status Return Buffers

4-53 These buffers are also tri-state and their outputs are held in an open or isolated condition while the CRE control line is high. When a self-ID status operation is decoded from the control lines, CRE goes low and RTN3 is high. This connects the inputs of the self-ID/status return buffers to the B0-B15 data lines. The self-ID/status word sent to the Multiprogrammer is shown below.

4-54 The 16-bits (B0-B15) are readback during self test or when an RS instruction is programmed. During self-test, bits B3-B15 are stored in the Multiprogrammer memory while status bits B0-B2 are ignored. When a Read Status (RS) instruction is issued, status bits B0-B2 are stored in multiprogrammer memory while bits B3-B15 are ignored.

4-55 The self-ID bits B3-B15 specify the "wake-up" values of the LSB, card ID, size, and data type parameters. The values of the parameters determines how the Multiprogrammer firmware will process the data it sends to or receives from the card. Status bits, B0-B2, are used by the Multiprogrammer to check the status of the card during operation. The status information is provided by UCC outputs, ARM, BSY, and EOP.



4-56 PROCESSING AN INPUT PARALLEL (IP) INSTRUCTION

4-57 This discussion explains the processing of a typical input type instruction. Assume that an Input Parallel (IP) instruction is issued by the controller which addresses a single Digital Input card in slot 2. The format of the controller instruction is...

"IP,2T"

4-58 When this instruction is executed, the following operations occur in the sequence indicated:

a. **Addressing the Digtial Input Card** - the slot position (slot 2) specified by the IP instruction is decoded and the CAD line to the Digital Input card goes high. In addition, the R/W lines, SAD0, SAD1 lines, and the three-bit, control-code lines are decoded. The ARM and GAFF flags are set.

b. **Cycling the card** - next, the Multiprogrammer sends another control code to inititate a cycle operation. BUSY, and GATE signals go high (GATE goes low) and are sent to the external connector. Since FLAG line is connected to the GATE line, a Load Input Latch (LIL) signal goes high. Whatever voltage levels are present at the input data lines are converted to TTL logic levels and are loaded into the Input Storage Register on the leading edge of LIL.

c. **End-of-Process and Interrupt Request** - When FLAG is returned EOP goes high and BUSY and GATE are cleared. Since ARM is also high, a program interrupt request (IRQ) is sent to the Multiprogrammer.

d. **Clearing the UCC** - After servicing the interrupt request, the Multiprogrammer sends a clear control code. The storage registers are not affected, but the ARM, EOP, and GAFF lines are cleared.

e. **Reading the Data Word** - The Multiprogrammer sends the last control code to the card which places the contents of the Input Storage Register on the input data lines to the Multiprogrammer. The data word is then transferred to Multiprogrammer memory. Once the data word from an IP instruction has been read, additional Controller instructions can be issued at the controller to display the data.

SECTION V
PARTS LIST

5-1 INTRODUCTION

5-2 This section contains information on ordering replacement parts for the Digital Input/Analog Comparator Model 69771A. Table 5-1 lists the electrical and mechanical components of the card. Table 5-2 lists the parts comprising the external I/O connector assembly supplied with the card. Figure 5-1 illustrates how the parts in Table 5-2 are assembled.

5-3 HOW TO ORDER PARTS

5-4 You can order parts from your local Hewlett-Packard sales office. Refer to the list of sales offices at the end of this manual for the office nearest you. When ordering parts include the following information :

a. the Hewlett-Packard part number.
b. a description of the part.
c. the quantity desired.
d. the model number of the card (69771A) on which the part is used.

5-5 If you wish to order a part directly from the manufacturer, locate the manufacturer's supply code in Table 5-1 and use this code to find the manufacturer's address in Table 5-3.

Table 5-1. Digital Input/Analog Comparator Card, Parts List

Ref. Desig.	HP Part No.	Qty	Description	Mfr. Code	Mfr. Part No.
C1, C2, C52 C54, C55	0180-0291	5	Capacitor, tantalum 1.0μf, 10%, 35 VDC	56289	150D105X9035A2
C3, C15 C16, C29	0160-0183	4	Capacitor, mica 130pf, 5%, 300 VDC	28480	
C4-14 C17-19, C28, C30 C39-C51, 53	0160-4722	30	Capacitor, ceramic 0.1μf, +80 −20%, 50 VDC	28480	
C20-27, C31-38	0160-0181	16	Capacitor, mica 30pf, 5%, 300 VDC	28480	
R1-16 R19-34	0683-1025	32	Resistor, 1k, 5%, 0.25 W	01121	CB-1025
R17, R18 R80-82, R85, R89-95	0683-5125	13	Resistor,5.1k, 5% 0.25 W	01121	CB-5125
R35, R59	0757-0290	2	Resistor, 6.19k, 1%, 0.125W	19701	MF4C1/8-TO-6191-F
R36	0698-3150	1	Resistor, 2.37k, 1%, 0.125 W	24546	C4-1/8-TO-2371-F
R37	0698-3445	1	Resistor, 348 ohms, 1%, 0.125 W	24546	C4-1/8-TO-348R-F
R38-53	0683-3055	16	Resistor, 3M, 5%, 0.25 W	01121	CB-3055
R54			NOT USED		
R55	0698-7060	1	Resistor, 15.6k, 5%, 0.5 W	28480	
R56, R58	0698-3274	2	Resistor, 10k, 1%, 0.125 W	28480	
R57	0698-6882	1	Resistor, 1.78k, 5%, 0.5 W	28480	
R60-75	0683-2235	16	Resistor, 22k, 5%, 0.25W	01121	CB-2235
R76	0757-0420	1	Resistor, 750Ω, 1%, 0.125 W	24546	C4-1/8-T0-751-F

Table 5.1 Digital Input/Analog Comparator Card, Parts List (Cont.)

Ref. Desig.	HP Part No.	TQ	Description	Mfr. Code	Mfr. Part No.
R77	0698-0092	1	Resistor, 2.61k, 1%, 0.125 W	28480	
R79, R83 R84, R86-88	0683-1035	6	Resistor, 10k, 5%, 0.25 W 5%, 0.25 W	01121	CB-1035
S1	3101-2368	1	Switch	28480	
Q1	1854-0823	1	Transistor, NPN silicon	28480	
U1-4	1826-0306	4	IC, Comparator, GP Quad	27014	LM339AJ
U5-8	1826-0059	4	IC, OP Amp GP-99	27014	LM201AH
U9, U25	1820-2239	2	IC, Misc	27014	DP8304N
U10, U11, U15, U16, U20, U22, U26, U27	1820-1544	8	IC, FF, CMOS, D-type Com Clock Quad	04713	MC14076BCL
U12, U17,	1820-1672	4	IC, Gate, CMOS, Excl-NOR Quad	04713	MC14077BCP
U13, U18, U24, U29, U33	1820-1246	5	IC, Gate, TTL, LS and Quad	01295	SN74LS09N
U14, U19, U21	1820-2257	3	IC BFR, CMOS, BUS Driver, Hex	04713	MC14503BCP
U31	1820-1425	1	IC, Schmitt-Trigger TTL, LS, INV Hex	01295	SN74LS14N
U32	1820-1416	1	IC, Schmitt-Trigger TTL, LS, NAND Quad	01295	SN74LS132N
VR1	1902-0509	1	Zener, 6.2 V, 2%	28480	
Z1, Z2	1810-0281	2	Network Resistors SIP	01121	210A104
Z3, Z4	1810-0280	2	Network Resistors SIP	01121	210A103
Z5-7	1810-0164	3	Network Resistors SIP	01121	CSP09C07-472J
			Mechanical Parts		
	69730-80001	1	Card Extractor		
	1480-0059	1	..Pin-roll (.062in.)		
	69730-90001	1	Manual, Operation and Instruction		

Table 5-2. Parts List for External Connector Assembly*
(HP Part No. 5060-2806)

HP Part No.	Index No.	Description	Qty.
1251-6307		Hood Assembly**	
	1	. . Strain relief	
	2	. . Cable clamps	
	3	. . Right hood assy.	
	4	. . Left hood assy.	
	5	. . Screw, 7/16 inch.	
	6	. . Screws, 11/16 inch.	
1251-6059	7	Connector Pin Housing	1
1251-6056	8	Connector Key	1
1251-6183	9	Solder Pins, plated	45
1251-6380	10	Springs retaining	6

* Can be ordered as Model 14703A, Card Edge Connector
** Item 1251-6307 consists of index items 1 through 6.

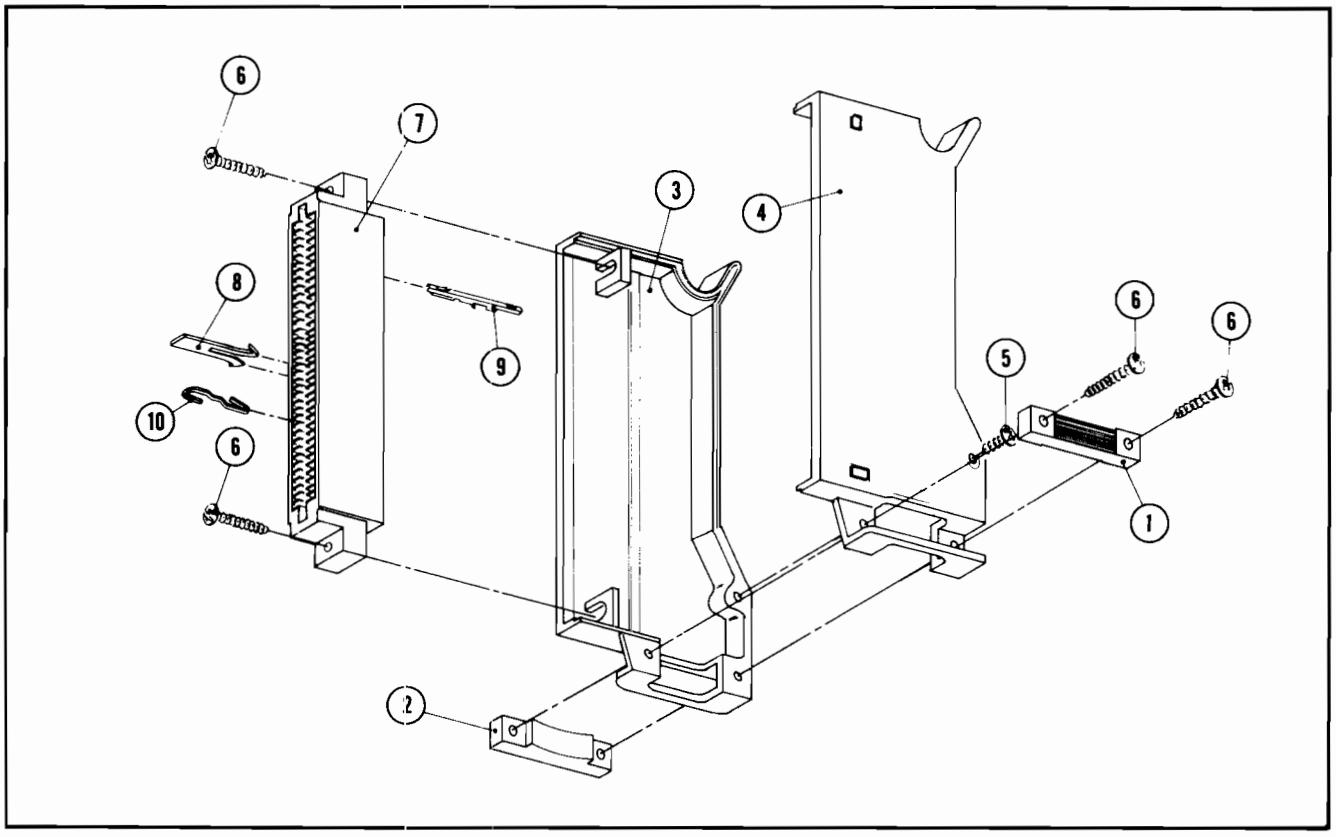


Figure 5-1. External I/O Connector Assembly, (HP, P/N 50600-28069)
Exploded View

Table 5-3. Manufacturer's Federal Supply Codes

Code	Manufacturer	Address
01121	Allen Bradley Co.	Milwaukee, Wis.
01295	Texas Instruments, Inc. Semiconductor-Components Division	Dallas, Texas
04713	Motorola Semiconductor Products Inc. Products Inc.	Phoenix, Arizona
14908	Electronic Instruments and Specialty Corp.	Stonham, Ma
16299	Corning Glass Works, Electronic Component Division	Bradford, Pa.
19701	Mepco/Electra Corporation	Mineral Wells, Texas
27014	National Semiconductor Corp.	Santa Clara. Calif.
28480	Hewlett-Packard Co.	Palto Alto, Calif.
56289	Sprague Electric Co.	North Adams, Ma
91637	Dale Electronics, Inc.	Columbus, NE

SECTION VI
DIAGRAMS

6-1 COMPONENT LOCATION

6-2 Figure 6-1 shows the Digital Input card and identifies the various test points shown in the functional schematic diagram, Figure 6-2, and the jumper locations described in Section III.

6-3 SCHEMATIC DIAGRAM

6-4 The schematic diagram of the Digital Input card is given at the end of this manual. The schematic diagram uses the ANSI Y32.14 and IEEE standard 91 for the representation of logic elements. A brief summary of this notation is given in Table 6-1.

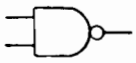
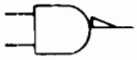
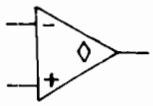
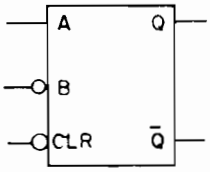
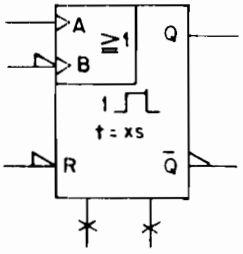
Table 6-1. Abbreviated List of ANSI Y32.14 Schematic Symbols

Definitions

High = more positive
Low = less positive

Indicator and Qualifier Symbols

≧	OR function
▱	(polarity indicator, shown outside logic symbol) Any marked input or output is active low; any unmarked input or output is active high.
⊳	(dynamic indicator) Any marked input is edge-triggered, ie, active during transition between states; any unmarked input is level sensitive.
⊓	(Schmitt trigger) Indicates that hysteresis exists in device.
*	(non-logic indicator) Any marked input or output does not carry logic information.
◊	open-collector or open emitter output
1 ⊓	monostable (one-shot) multivibrator
t = xSec	indicates pulse width (usually determined by external RC network)
G	gate input (a number following G indicates which inputs are gated)
C	control input (clock)
R	reset (clear)
S	set

OLD SYMBOL	*NEW SYMBOL*	*NOTES*
		
		Output requires external components to achieve logic state
		A positive-going transition at A or a negative-going transition at B triggers the one-shot. External timing components connect to non-logic inputs.
		Output changes state rapidly regardless of input rate of change.

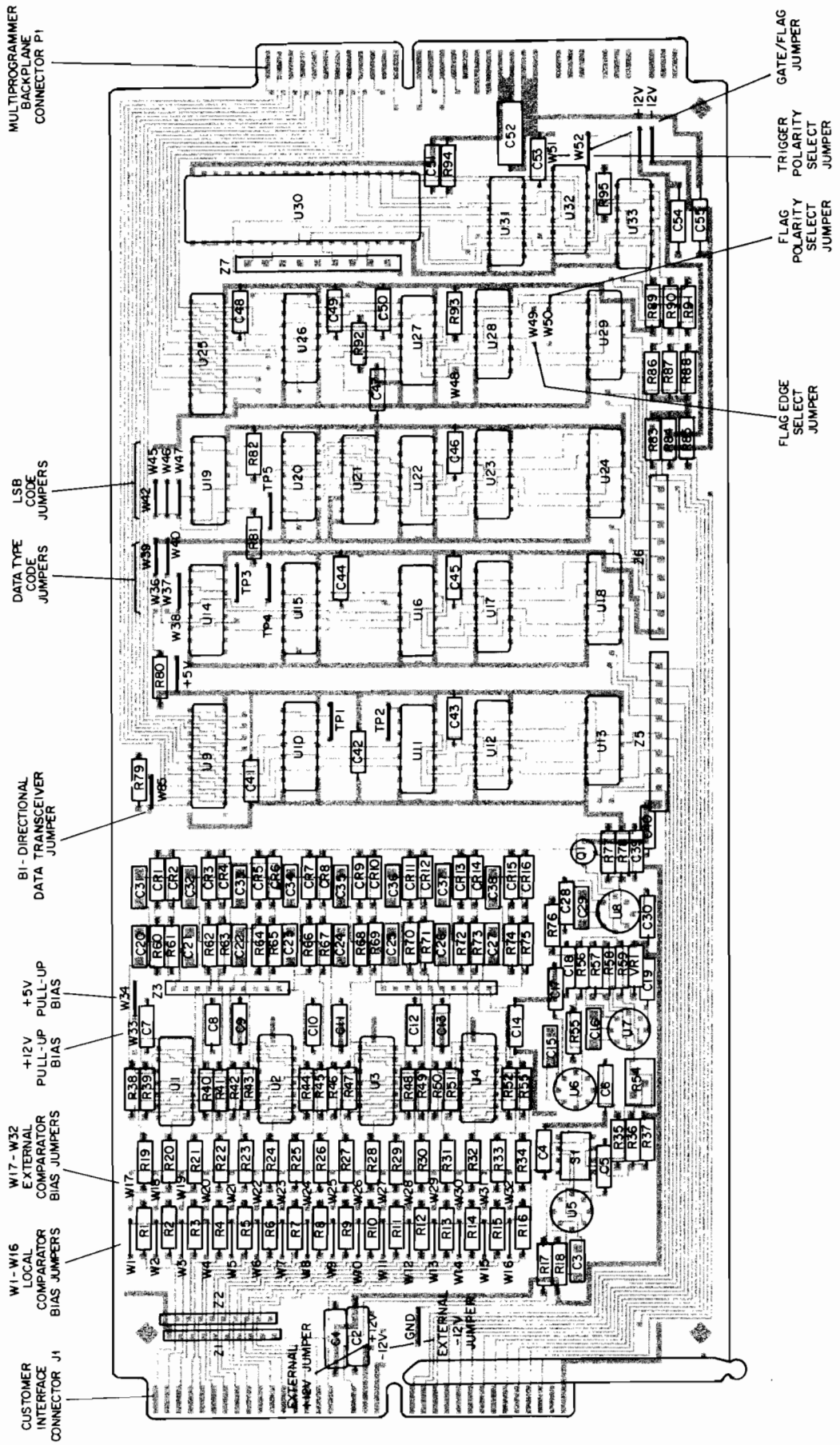


Figure 6-1. Digital Input Card, Component Location

DIGITAL INPUT / ANALOG COMPARATOR CARD MODEL 69771A

NOTES:

1. ALL RESISTORS ARE IN OHMS, ±5%, 1/2W UNLESS OTHERWISE INDICATED. ALL CAPACITORS ARE 50V AND IN MICROFARADS UNLESS OTHERWISE INDICATED.
2. ON IC U9 FILTER CAPACITOR C41 IS CONNECTED FROM PIN 10 TO GROUND.
   ON IC U25 FILTER CAPACITOR C48 IS CONNECTED FROM PIN 20 TO GROUND.
3. ON IC'S U1, U2, U3 AND U4 THE FOLLOWING APPLIES:
   FILTER CAPACITORS C7, C9, C11 AND C13 ARE CONNECTED FROM PIN 3 TO GROUND.
   FILTER CAPACITORS C8, C10, C12 AND C14 ARE CONNECTED FROM PIN 12 TO GROUND.
4. ON IC'S U5, U6, U7 AND U8 THE FOLLOWING APPLIES:
   FILTER CAPACITORS C4, C17, C18 AND C28 ARE CONNECTED FROM PIN 7 TO GROUND.
   FILTER CAPACITORS C5, C6, C19, AND C30 ARE CONNECTED FROM PIN 4 TO GROUND.
5. ON RESISTANCE NETWORKS Z1 - Z4, PIN 1 IS COMMON.
   ON RESISTANCE NETWORKS Z5 - Z7, PIN 9 IS COMMON.

BIDIRECTIONAL DATA TRANSCEIVERS

INPUT DATA STORAGE

INVERT / INVERT GATES

CLAMPING DIODES

SIGNAL CONDITIONING

INPUT DATA LINE C

FIRST RANK RETURN BUFFER

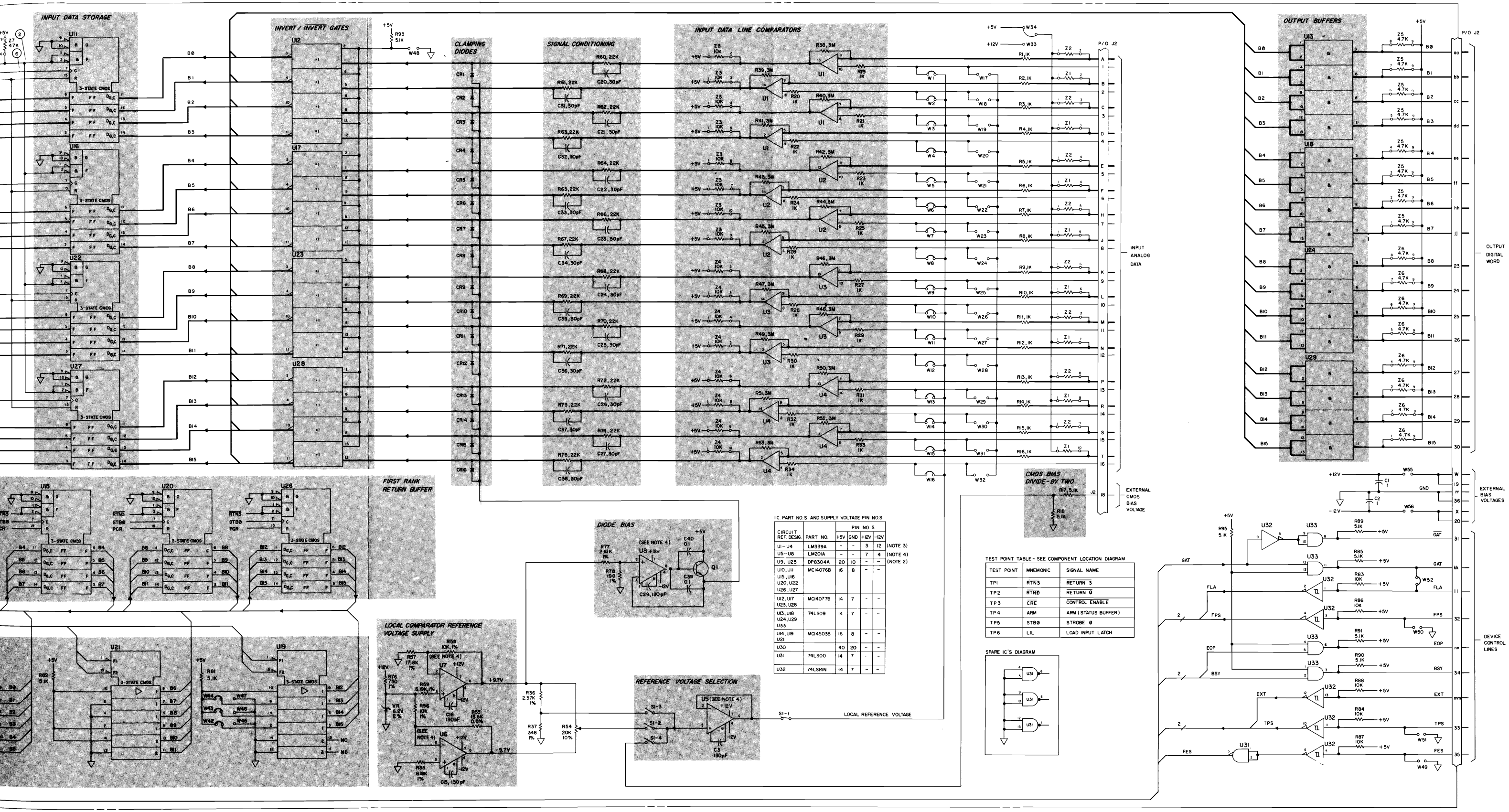
SELF-ID / STATUS RETURN BUFFERS

UNIVERSAL CONTROL CHIP

LOCAL COMPARATOR REFERENCE VOLTAGE SUPPLY

REFERENCE VOLTAGE SELECTION

DIODE BIAS



I.C. PART NO.S AND SUPPLY VOLTAGE PIN NO.S

CIRCUIT REF. DESIG	PART NO.	PIN NO.S +5V	GND	+12V	-12V	
U1-U4	LM339A	-	-	3	12	(NOTE 3)
U5-U8	LM201A	-	-	7	4	(NOTE 4)
U9, U25	DP8304A	20	10	-	-	(NOTE 2)
U10, U11 U15, U16 U20, U22 U26, U27	MCI4076B	16	8	-	-	
U12, U17 U23, U28	MCI4077B	14	7	-	-	
U13, U18 U24, U29 U33	74LS09	14	7	-	-	
U14, U19 U21	MCI4503B	16	8	-	-	
U30		40	20	-	-	
U31	74LS00	14	7	-	-	
U32	74LS14N	14	7	-	-	

TEST POINT TABLE - SEE COMPONENT LOCATION DIAGRAM

TEST POINT	MNEMONIC	SIGNAL NAME
TP1	$\overline{RTN3}$	RETURN 3
TP2	$\overline{RTN0}$	RETURN 0
TP3	$\overline{CRE}$	CONTROL ENABLE
TP4	ARM	ARM (STATUS BUFFER)
TP5	STB0	STROBE 0
TP6	LIL	LOAD INPUT LATCH

SPARE IC'S DIAGRAM

Figure 6-2. Digital Input Card, Fucntional Schematic Diagram