# DIGITAL INPUT CARD

# MODEL 69431A


OPERATING AND SERVICE MANUAL

FOR CARDS DESIGNATED RUN 1 AND ABOVE*

*For Cards above Run 1
a change page may be
included.

HP Part No. 69431-90001

December, 1971

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MANUAL CHANGES

Model 69431A Digital Input Card
Manual HP Part No. 69431-90001

Make all corrections in the manual according to errata below, then check the following table for your card's run or serial number and enter any listed change(s) in the manual.

| RUN NUMBER | | MAKE CHANGES |
|---|---|---|
| ALL | | ERRATA |
| 2 - 13 | | 1 |
| 14 - 15 | | 1, 2 |
| 16 and above | | 1, 2, 3 |
| SERIAL | | |
| Prefix | Number | |
| 1632A | 00693-05754 | 1-4 |
| 2012A | 05755-up | 1-5 |

ERRATA:

On Page 3-4, in Figure 3-2, add the following voltages to the listed pins of the 69431A Input Connector:

Pin A - Bus A
Pin B - Bus B
Pin C - +5V ($V_{CC}$)

On the schematic, Figure 7-1, Sheet 1 add the following references from the power distribution lines (lower left corner near the +5V ALTERNATE SUPPLY) to the P2 Input Connector:

Bus A to P2-A
Bus B to P2-B
+5V to P2-C

The above connections allow the user to provide external power (Bus A and Bus B) to the card for custom interface requirements.

On the schematic, Figure 7-1, Sheet 1, in the 12 Bit Data Storage circuit, interchange the Q and $\overline{Q}$ output pin numbers of each flip-flop (i.e. the Q output for bit 0 is Z1-16 and the $\overline{Q}$ output is Z1-1).

On the schematic, Figure 7-1, Sheet 2, in the Gate Driver circuit, change W3-A from "+15V" to "+5V."

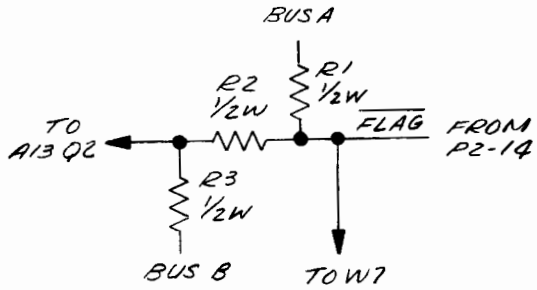
In the replaceable parts table, under Option 070, add the following information for the A4Z17-Z19 Quadruple Hybrid Integrated Circuit:

Mfr. Part No. - 207C17
Mfr. Code - 56289
HP Part No. - 1813-0007

On Figure 7-1, Sheet1, delete the internal connection between P1-A and P1-1. There is no internal connection to P1-1.

On Figure 7-1, Sheet 1 and Sheet 2, change P2 Output connector to P2 Input connector.

On Figure 7-1, Sheet 2, change the A13 Flag Receiver circuit as follows:




On Page 1-3, in the Specification table, add the following power requirements of the input card:

POWER REQUIREMENTS:
+5Vdc at 200mA maximum from Multiprogrammer Main Power Supply.
+12Vdc at 120mA maximum from Multiprogram-Main Power Supply.

CHANGE 1:

On Figure 7-1, Sheet 1, make the following changes:
Reverse the "W9" and "B" reference designations. P1-E now connects to "B" and Bus B connects to "W9."
Add Z20 and Z21 to the +5V Alternate Supply's +5V (ALT) power distribution.

On Page 1-3, in the Specification table and on Page 3-5, in Figure 3-4, for options 069, 070, and 073, change the "LO" Gate output level sink current specification to 15mA maximum.

On Figure 7-1, Sheet 1, change the Address Gate and add output Data Bit Delay circuits as shown on the schematic below.

The Output Data Bit Delay circuits are added in order to eliminate any possibility of generating noise on address bits 15-12 which might be caused if data bits BØØ-B11 were allowed to switch simultaneously. The Delay Circuits delay each associated pair of data bits by approximately 200nsec so that there is a total delay of approximately 1.2μsec (typical) between the time that the card is addressed ($\overline{\text{CARD SEL}}$ goes low) and data bits $\overline{\text{BØØ}}$ through $\overline{\text{B11}}$ appear at the output of the Output Gates (that is, at the multiprogrammer backplane wiring). Total delay time may approach 2.0μsec (maximum).

In the replaceable parts table, make the following changes:

Under 69431A-A4:

A4Z20 and A4Z21: Add Z20 and Z21, Hex Inverters, Low Power, IC, HP Part No. 1820-0586.

A4C20-A4C25: Add capacitors C20-25, fxd, mylar 0.001μF 200Vdc, HP Part No. 0160-0153.

A4C26: Add capacitor C26, fxd, elect. 1.0μF 35Vdc, HP Part No. 0180-0291.

A4Q8: Change Q8 to HP Part No. 1854-0448.

A4R16, A4R24: Change R16 and R24 to 1.5KΩ ±5%, 1/4W, HP Part No. 0683-3025.

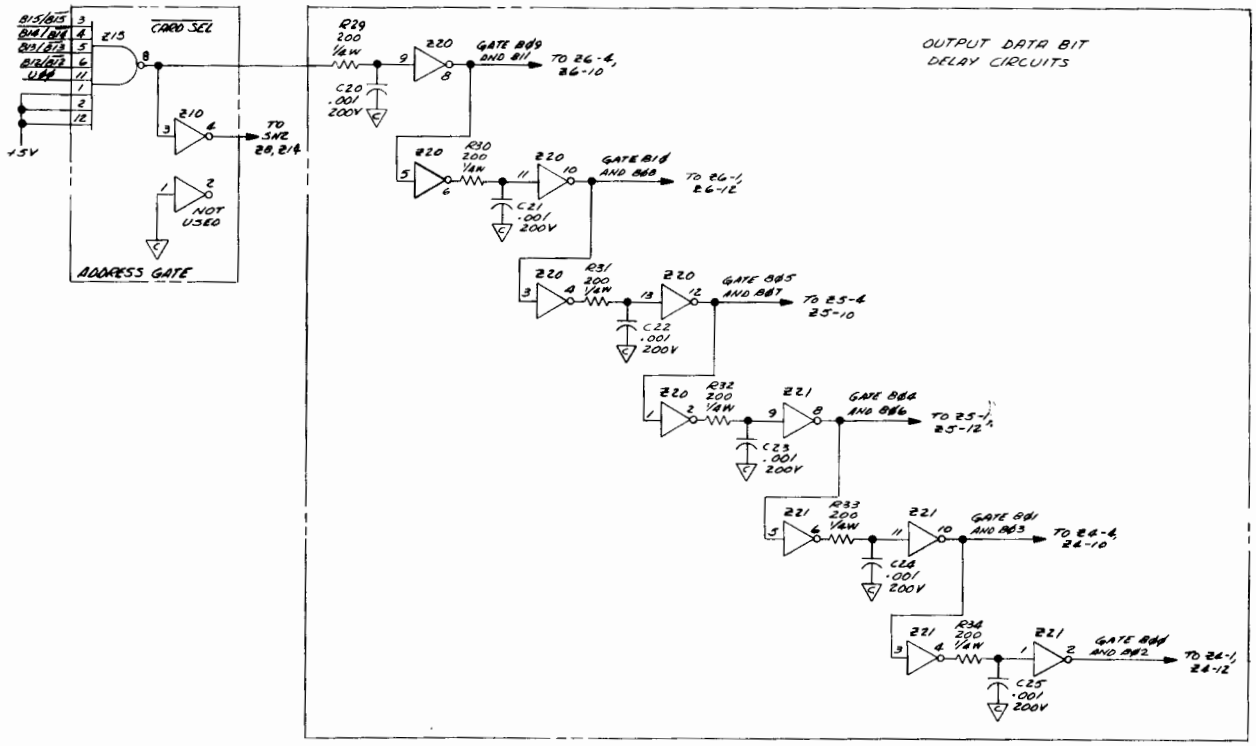
A4R29-A4R34: Add R29-R34, 200Ω ±5%, 1/4W, HP Part No. 0683-2015.

Under Mechanical:

Add IC Socket (2): HP Part No. 1200-0768.

Capacitor A4C26 is connected between +5V (Vcc) and ▽C▽ (see C1-C5 on Figure 7-1, Sheet 1).

A revised component location drawing for Option 069 cards is given on the next page.




In the replaceable parts table, under MECHANICAL, make the following changes:

Change Connector Assembly, Output to HP Part No. 5060-9658. The new assembly consists of the following parts:

Connector, 30-pin-HP Part No. 1251-0159

Hood Assembly, Right-HP Part No. 5060-7981

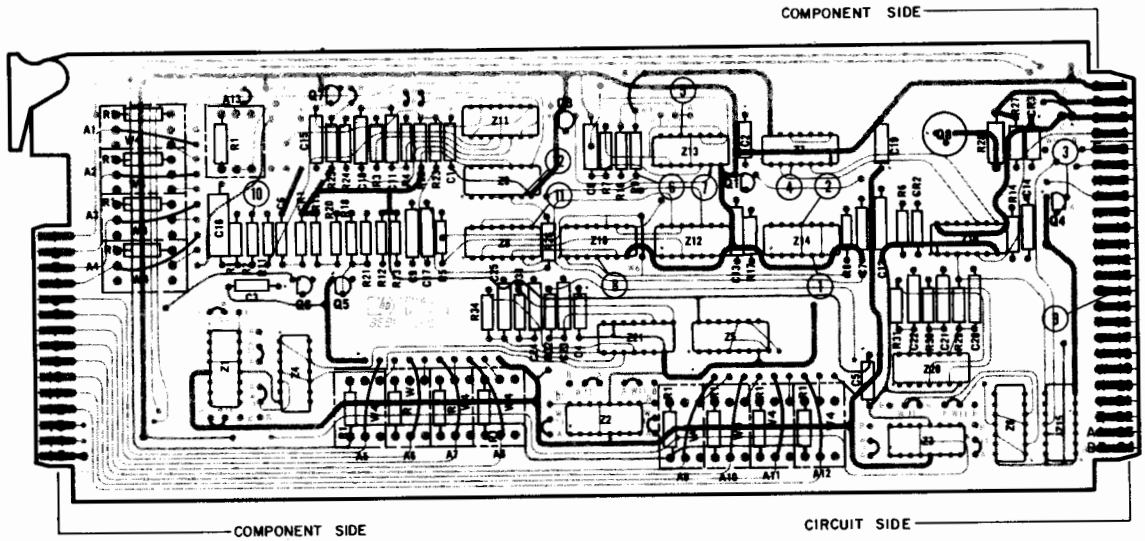
Hood, Right-HP Part No. 4040-0233

Insert, Threaded (4-40)-HP Part No. 0590-1017

Insert, Threaded (2-56)-HP Part No. 0590-1018

Hood, Left-HP Part No. 4040-0232

Clamps, Cable—HP Part No. 1400-0714




OPTION 069 SHOWN

CHANGE 2:

Two more Optional capabilities (Options 095 and 096) have been added to this card. Jumper connections for the added Options are shown below. Add this information to the chart on note 3, Figure 7-1.

OPTION 095: This option is the same as Option 069 (described throughout the manual), except that jumpers W6 and W10 are not connected. With W6 out, the input cards cannot be group activated in the IEN mode, as described in Paragraph 3-21. Instead, each card must be selectively armed for interrupt by programming ISL on and individually addressing the card.
With W10 out, the cards' data storage capability is disabled and data is continuously available at the card as received from the external device.

OPTION 096. This Option is the same as Option 073 except for jumpers W1, W2, W8, and W10 and the omission of R1. Jumper W10 is out, as described for Option 095. The positions of jumpers W1 and W2 affect the timing relationships between the device gate and flag. Table 3-1 (page 3-5) shows the timing for this Option.

| OPTION | A1 through A13 | | | Q2, CR4 | | | | | | | | | | | | LOGIC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | R1 | R2 | R3 | C18, R15 | W1 | W2 | W3 | W4 | W5 | W6 | W7 | W8 | W9 | W10 | W11 | SENSE |
| 095 | 1K | — | — | — | A | B | A | IN | A | OUT | IN | C | OUT | OUT | A | NEG. TRUE |
| 096 | — | — | — | — | B | A | A | IN | A | IN | IN | OUT | OUT | OUT | B | POS. TRUE |

ERRATA:

In the parts list, change the part number of the Z1-3 IC sockets to 1200-0507 and the Z4-16 sockets to 1200-0508.

CHANGE 3:

Change Z11 in the parts list to a quad 2-input Schmitt NAND gate, HP Part No. 1820-1056. Also change C16 in the schematic and parts list to .047μF 200V, HP Part No. 0160-0138

ERRATA:

One page 3-5, add asterisks to Table 3-1 as follows: a single one near (W7 IN) in the top box, and two near (W7 OUT) in the third box.

In Figure 3-2, delete the words GATE OUT and FLAG RETURN from pins P and R. These pins are not used.

In Table 1-1 under FLAG INPUT LEVEL, substitute the following:
Options 069 and 073: HI = 2.4 to 5V LO = 0 to 0.5V
Option 070: HI = 6 to 14V or open contacts
LO = 0 to 1V or closed contacts

CHANGE 4:

Delete all IC sockets from the parts list on page 6-5. To increase reliability the ICs are soldered into the board.

All multiprogrammer plug-in cards are now being marked with serial numbers to keep better control of units out in the field. The serials assigned to this model are given in the table. For an explanation of the serial prefix, see paragraph 1-44 in the multiprogrammer mainframe manual.

ERRATA:

Delete part d of par. 2-10. Current Multiprogrammers do not have an installation record card inside the door.

In par. 3-35, delete the sentence that begins "A 30-conductor cable (28 gauge max . . ." and substitute the following: This connector accommodates up to 15 wires, each with an outside diameter of up to .062 inches.

In the parts list, delete the packing carton or corrugated tray listed and add the part number of the carton with foam liner now used for shipping multiprogrammer cards. Its number is 9211-2603.

CHANGE 5:

In Table 6-1 and in schematic Figure 7-1 (Sheet 2), delete resistors R22 and R23 in the Start/End of Flag Detector circuit.

2-19-80

## TABLE OF CONTENTS (CONTINUED)

# SECTION I
# GENERAL INFORMATION

## 1-1 INTRODUCTION

1-2 This instruction manual contains operating and service instructions for Digital Input Card Model 69431A. The card is designed specifically for use in the 6940A Multiprogrammer and 6941A Multiprogrammer Extender units to receive 12 separate digital logic-level inputs from a user's external device. As shipped from the factory, the inputs to the 69431A card can be either negative-true (Option 069) or positive-true (Option 073) microcircuit logic levels or open collector negative-true (Option 070) logic levels. In addition to the 069, 073, and 070 options, the digital input card can also be modified to satisfy a wide variety of custom interface requirements such as relay contact closure logic inputs as necessary. Input bias networks and/or option jumpers can be selected either at the factory or by the user to interface the user's specific logic sense and voltage polarity input requirements.

1-3 Overall system concepts, including system installation, troubleshooting, and operating considerations are covered in the instruction manual for the 6940A master unit and are not repeated in this manual.

1-4 OPTION 069

1-5 Option 069 is employed for inputs having negative-true logic sense (0 volt input for programmed binary 1) and microcircuit logic levels (0 to +5 volts). As supplied from the factory, the jumper connections on the digital input card are configured such that the logic sense requirements of the input data bits and flag signal as well as the gate signal output are as follows:

$\overline{\text{DATA BIT}}$ INPUTS: LO - TRUE
$\overline{\text{GATE}}$ OUTPUT: HI-to-LO transition
$\overline{\text{FLAG}}$ INPUT: HI-to-LO transition - BUSY
LO-to-HI transition - READY

Other input and output signal senses can be accommodated by adding or removing jumpers on the digital input card (see Section III).

1-6 OPTION 073

1-7 Option 073 is employed for inputs having positive-true logic sense (+5 volt input for programmed binary 1) and microcircuit logic levels (0 to +5 volts). As supplied from the factory, the jumper connections on the digital input card are configured such that the logic sense requirements of the input data bits and flag signal as well as the gate signal output are as follows:

$\overline{\text{DATA}}$ BIT INPUTS: HI - TRUE
$\overline{\text{GATE}}$ OUTPUT: HI-to-LO transition
$\overline{\text{FLAG}}$ INPUT: HI-to-LO transition - BUSY
LO-to-HI transition - READY

Other input and output signal senses can be accomodated by adding or removing jumpers on the digital input card (see Section III).

1-8 OPTION 070

1-9 Option 070 is employed for inputs derived from open-collector output drivers having negative-true logic sense and logic levels up to +14V. As supplied from the factory, the jumper connections on the digital input card are configured such that the logic sense requirements of the input data bits and flag signal as well as the gate signal output are the same as for Option 069. Again, the jumper options allow for other logic senses to be accommodated (see Section III).

1-10 STORAGE DISABLE

1-11 Option jumper W10 is provided to allow input data to be: (1) stored on the input card at the READY transition of the user's FLAG input (trailing edge) or (2) continually available on the input card as received on the input data lines. As shipped from the factory, W10 is installed and input data storage requires the trailing edge of the FLAG input. The user can disable the storage requirement by removing the W10 jumper.

## 1-12 DESCRIPTION

1-13 When installed in a Multiprogrammer System, the digital input card is programmed by a 16-bit address word originating at a remote computer or the 6940A Multiprogrammer control panel. The twelve least significant bits of the programmed bits (bits 0-11) are not relevant to the input card and are not used while the remaining four bits (bits 12-15) contain the slot address of the input card.

1-14 When the input card slot is addressed by the computer or from the control panel, 12-bit input data contained in its storage circuits is transferred to the computer or 6940A multiprogrammer control panel if the multiprogrammer has been previously placed in the input select (ISL) mode.

1-15 With W10 installed, the digital input card stores 12-bit input data from the user's device when the device supplies a Flag ready (trailing edge) input in response to a Gate signal supplied to the device from the digital input card. The input card gate/flag circuit is controlled by the remote computer or from the 6940A control panel and is activated (the gate signal is generated) either: (1) selectively when the input card is addressed and strobed after the Multiprogrammer System has been placed in the ISL mode or (2) in conjunction with other input cards when the multiprogrammer is placed in the IEN mode. The second method of activation (IEN) requires that a jumper option be installed on the input card.

1-16 In addition to processing the device gate/flag signals to control data input, the input card gate/flag circuits also develop, in conjunction with input card control circuits, timing flag and input request signals for application to the computer. The timing flag signal is generated either when the card is addressed and in the data-ready state or when the multiprogrammer has been previously placed in the interrupt enable (IEN) mode and the card is activated and in the data ready state. The timing flag signal is combined in the multiprogrammer with all other input (and output) card timing flag signals into the common (combined) timing flag (CTF) signal used by the multiprogrammer in the timing mode to signal to the computer when data is ready for input (or output). The input request (IRQ) identification signal is generated when the card is addressed, activated, and in the data ready state. Like the CTF signal, the IRQ signal is combined in the multiprogrammer with input request identification signals from all other input cards. Further, the combined IRQ signal is incorporated into bit 15 of the data returned to the computer when an input card is addressed. Note that the common timing flag and IRQ signals are also applied to the 6940A Multiprogrammer control panel during the local programming mode of operation.

1-17 The digital input card also contains a control circuit that is involved (with the gate/flag circuits) in developing the common timing flag and input request identification signals. The control circuit stores the activation status of the input card in that when the card's gate/flag circuits are activated, the control circuit is set to the active state. The control circuits remain active and allow the gate/flag circuits to generate the common timing flag and input request signals. When the card is deactivated, the CTF signal is partially disabled while the IRQ signal is completely turned off. The control circuits are activated when the gate/flag circuits are activated; that is, when the card is addressed and strobed in the ISL mode. The control circuits are deactivated if the card is addressed and strobed when the ISL mode is off. When deactivated, the control circuits inhibit the input card's CTF signal during the IEN mode and, also, inhibit completely the input request signal. Note, however, that CTF can still be generated by addressing the card when it is in the data ready state.

1-18 The data storage and gate/flag operation of the digital input card described above can be modified at the option of the user. For instance, if the user does not have a flag timing circuit, a hardware jumper can be removed from the input card to disable the device flag trailing edge data storage requirement of the input card so that the user's 12-bit input data will be entered into the card storage circuits as received from the device. On the other hand, the storage circuits can be utilized even if the user does not have a flag timing circuit by jumpering the input card gate output and flag input connections.

1-19 The input card is fabricated on a $4\frac{1}{2}$" x 11" printed circuit card. The inner edge of the card contains a dual 24 pin (48 pin total) printed circuit plug that can mate with any connector in slot 400 through 414 of a multiprogrammer unit (6940A or 6941A). A dual 15-pin (30-pin total) printed circuit plug located on the outer-edge of the card connects the 69431A to the external device.

## 1-20 SPECIFICATIONS

1-21 Table 1-1 provides detailed specifications for the Model 69431A.

Table 1-1. Model 69431A Specifications

DATA OUTPUT (To Computer): 12-bit binary
Options 069 and 070: binary 1 = input in LO state
binary 0 = input in HI state
Option 073: reverses above relationships

DATA INPUT (From Device) LEVELS: 12-bit binary
Options 069 and 073: LO = 0 to 0.8V (6mA max. SINK CURRENT)
HI = 2.0V to 5.0V (1kΩ source impedance)
Option 070: (open collector drivers)
LO = 0V to 1.0V (15mA

Table 1-1. Model 69431A Specifications (Continued)

max. sink current)
HI = +6V to +14V
User-Connected Options: receiver input bias network and gate can be modified to accommodate wide range of inputs.

INPUT DATA STORAGE:
Standard (Options 069, 070, 073):
12-bit storage register receives input data at end-of-FLAG transition of external device FLAG input. Data must be at specified level when end-of-FLAG received and remain for 3μsec (min.).

User-Selected Option:
User can disable data storage by removing option jumper. Data available at card as received on input data lines.

DEVICE COMMAND (GATE) OUTPUT:
Standard (Options 069, 070, 073):
One normally HI logic level line. HI-to-LO change in level indicates data is requested by input card. Level normally reverts to original status (HI) at start of external device response (FLAG). User can select option to revert level to HI at end of external device response.

User-Selected Option:
One normally LO logic level line. LO-to-HI change in level indicates data is requested by input card. Level normally reverts to original status (LO) at start of external device response (FLAG). User can select option to revert level to LO at end of external device response.

Gate Output Level:
Options 069 and 073: LO = saturation; 50Ω max. (11mA max. sink current)
HI = cutoff, 1kΩ (max.)
Option 070: LO = saturation; 50Ω max. (40mA max. sink current)
HI = cutoff, 10kΩ (max.)

Should not be set to data requested state twice in succession (i.e. before it is reset by FLAG).

DEVICE SIGNAL (FLAG) INPUT:
Minimum pulse width: 2μsec
Minimum rise and fall times: 0.1V/μsec
Standard (Options 069, 070, 073):
One normally HI input line. HI-to-LO change in level indicates external device is busy processing data in response to device command (gate) output. End-of-FLAG (LO-to-HI transition) indicates device data available to input card.

User-Selected Option: One normally LO input line. LO-to-HI change in level indicates external device is busy processing data in response to device command (gate) output. End-of-FLAG (HI-to-LO transition) indicates device data available to input card.
If external FLAG input not desired, GATE output can be connected directly to FLAG input or left open (see INPUT DATA STORAGE).

FLAG input level: Same as DATA INPUT LEVELS

TEMPERATURE RANGE: 0°C to +80°C operating in mainframe (allows +25°C internal rise when operating in mainframe at up to +55°C ambient).

-40°C to +80°C storage.

OPERATING POSITION:
Any (no restrictions)

INPUT CONNECTOR:
One 15-pin dual (30-pin total) edge connector. Mating female connector assembly supplied (HP Part No. 5060-7934).

DIMENSIONS:
4.5" x 11.0" nominal

WEIGHT:
0.7 lbs.

## 1-22 INTERFACING

1-23 The 69431A Digital Input Card is automatically interfaced with its associated multiprogrammer unit when it is installed in a 400 series slot connector. Once it is assigned to a slot, the card assumes the address of that position and will input data only when the applicable unit and slot are addressed. All operating power and address data for the card are derived from the multiprogrammer unit.

1-24 Interfacing considerations involving the

69431A and the external device are covered in detail in Section III of this Instruction Manual.

## 1-25 OUTPUT CONNECTOR ASSEMBLY

1-26 One 30-pin output connector assembly (HP Part No. 5060-7934) is furnished with each digital input card for interfacing the card with the external system. Additional 30-pin connector assemblies may be ordered from your local Hewlett-Packard sales office (refer to list at rear of manual for addresses).

## 1-27 ORDERING ADDITIONAL MANUALS

1-28 Two manuals are shipped with each 69431A order. Additional manuals may be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). Specify the card model number and HP Part Number shown on the title page.

# SECTION II
# INSTALLATION

## 2-1 INITIAL INSPECTION

2-2 Before shipment, the 69431A Digital Input Card was inspected and found to be free of mechanical and electrical defects. As soon as the card is received, proceed as instructed in the following paragraphs.

2-3 MECHANICAL CHECK

2-4 If external damage to the shipping carton is evident, ask the carrier's agent to be present when the card is unpacked. Check the card for signs of physical damage. If it is damaged, file a claim with the carrier's agent and notify Hewlett-Packard Sales and Service Office as soon as possible. If it appears to be undamaged, perform the electrical check specified in the following paragraph.

2-5 ELECTRICAL CHECK

2-6 Check the electrical performance of the output card as soon as possible after receipt. Section V of this manual contains checkout procedures which will verify operation of the card. Refer to the inside front cover of this manual for Certification and Warranty statements.

## 2-7 REPACKING FOR SHIPMENT

2-8 When shipping an input card, it is recommended that the package designed for it be used. The original packaging material is reusable. If it is not available, contact your local Hewlett-Packard field office to obtain the materials. This office will also furnish the address of the nearest service office to which the input card can be shipped. Be sure to attach a tag to the card specifying the owner, model number, and service required, or a brief description of the trouble.

## 2-9 INPUT CARD INSTALLATION

2-10 Input cards are installed in slots 400 through 414 of a Multiprogrammer unit. To install an input card, proceed as follows:

a. Open the hinged front panel of the Multiprogrammer unit by turning the recessed screw within the knurled handle counterclockwise.

b. With the extractor handle on the top and the card components on the right, slide the card into the desired multiprogrammer slot (400 through 414). Note that all input cards are slotted between pins 4 and 5 and all 400 series connectors of the Multiprogrammer are keyed between the same points. This makes it virtually impossible to plug an input card in upside down or into any slot other than a 400 series slot.

c. Route all wiring from the input cards through the false-bottom channel and out the back of the unit to the external system.

d. As physical installation and wiring are completed for the input card, carefully note and record the following types of information on the installation record card located on the rear of the hinged front panel of the multiprogrammer.

(1) Input card type
(2) Application in external system
(3) Timing flag period, logic sense, etc.

# SECTION III
# OPERATING INSTRUCTIONS



## 3-1 MULTIPROGRAMMER CONNECTIONS

3-2 The Digital Input Card is controlled by the multiprogrammer unit in which it is installed. All dc operating power, address bits, and control signals are supplied to the input card through multiprogrammer main frame connectors in slots 400 through 414. Figure 3-1 illustrates the signals present on all multiprogrammer 400-series connectors. Notice that several signals (i.e. SYE, $\overline{DTE}$, etc.) are used only by multiprogrammer output cards and are not utilized in the Digital Input Card.

## 3-3 PROGRAMMING

3-4 The programming information presented here defines the relationships of programmed data and the 69431A card outputs to the computer. Complete system programming instructions are given in the Operating and Service manual for the 6940A Multiprogrammer. Since the digital input card has been designed to provide a wide range of flexibility in interfacing the user's device to the computer via the multiprogrammer system, no attempt has been made in this programming information to be definitive of all the ways in which an input card can be used in a system. Rather, the intent has been to describe general programming considerations applicable to the card and to indicate the broad flexibility of usage provided by the digital input card.

3-5 Generally, the digital input card is operated in two typical modes of operation as defined in the multiprogrammer by the controlling computer. One mode, the dedicated input mode, is utilized in simple data input sequences and requires that the card be addressed during the data transfer cycle between the card and external device as a condition for allowing the card to signal the computer that data is ready from the external device. The other mode of operation, the interrupt search input mode, is utilized in more complex data input sequences involving many input cards (up to 240, the maximum possible complement of multiprogrammer system input cards) that are simultaneously active in data transfer cycles with their associated external devices. The interrupt search input mode does not require that the computer address the input card during the data transfer cycle as a condition for allowing the card to signal the computer that data is ready for input. Instead, all cards are allowed to signal the computer when the data transfer cycle is over (as soon as data is available) with the computer responding by searching for the card (from among the active group) which signalled that it was ready. The procedures required for programming the digital input card in the two modes of operation are described below.

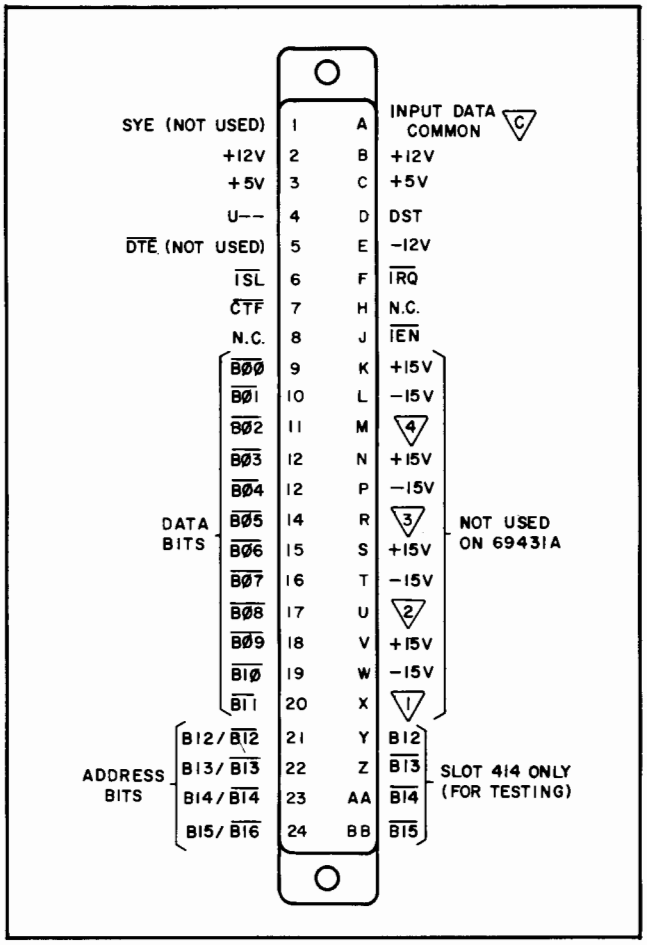



Figure 3-1. Multiprogrammer 400 Series Slot Connector

3-6 DEDICATED INPUT MODE

3-7 There are four general steps involved in programming a digital input card for dedicated input mode of operation:

a. Programming the multiprogrammer into the input select (ISL) mode in order to convert the multiprogrammer into an input device and to enable the input card to be activated. Further, prior to card activation, the multiprogrammer is normally placed

in the timing mode (TME) to allow the input card's flag circuit to control the multiprogrammer flag to the computer. Note that if the card is operated in the handshake mode (TME off) during dedicated input operation, the card should not be activated (Step b. below) twice before the external device has responded with the FLAG ready indication. These initial conditions require a multiprogrammer control word.

b. Activating the input card by addressing and data strobing the card. This will generate a GATE signal to the external system. Note that card addressing actually requires two operations: first, the unit in which the input card is installed must be specified in a multiprogrammer control word. Next, the input card's slot address must be specified in a multiprogrammer address word. Further, the card address must be maintained to allow the card to signal it is ready with data.

c. Inputting card data when the input card signals that it is ready. Since the card address is maintained by the computer to allow the card to signal data ready, the card's data is available to the computer as soon as the data ready signal is received.

d. Activating the card again (Step b.) for the next data input or deactivating the card by first programming the input select mode off and then addressing and strobing the card.

## 3-8 INTERRUPT SEARCH INPUT MODE

3-9 There are seven general steps involved in programming a digital input card for interrupt search input mode of operation:

a. Programming the multiprogrammer into the input select mode as in Step a. (above). However, card activation in the search mode is usually done with the multiprogrammer in the "fast" (handshake) mode (TME is off).

b. Activating all desired input cards by addressing and data strobing each card.

c. Programming the multiprogrammer into the interrupt enable mode (IEN) in which the computer's multiprogrammer I/O channel will wait for one of the activated input cards to signal that data is ready. This step requires a multiprogrammer control word having both IEN and TME programmed on.

d. When an input card completes the data transfer cycle with its external device, it signals the computer that data is ready. The computer should respond by entering the interrupt search routine. First, the computer programs the interrupt enable mode off (to prevent other input cards from signalling data ready) and the input select mode on (in order to communicate with the input cards by turning the multiprogrammer back into an input device). The timing mode is usually turned off also to allow rapid input card data search. This step also requires a multiprogrammer control word.

e. Next, the multiprogrammer searches for the data ready card by addressing the cards (in a software-established priority) one at a time and inputting card data. The data search is usually done without strobing the card so as to avoid reactivating a currently busy card (one that had <u>not</u> signalled data ready).

f. In addition to the 12 data bits received from each input card when addressed, the input cards also return an indication of their data ready status to the computer in the bit 15 line of the data bits returned to the computer from the multiprogrammer. The computer next examines (by software) this bit to determine if the accompanying data bits are valid (i.e. the card had signalled it was ready for data input).

g. After detecting and reading the ready card, the computer should reactivate (Step b.) or deactivate the card (address and strobe the card after turning ISL off) depending on whether or not more data is expected. The computer then can turn the interrupt enable mode back on (Step c.) or not as desired.

3-10 The digital input card includes an optional jumper (W6) that is installed at the factory and allows Steps 3-9a and 3-9b to be bypassed. All cards having the W6 jumper installed are simultaneously activated when the interrupt enable mode is programmed (Step c.). Note that since IEN is turned off (Step d.) and back on (Step h.) again as part of the interrupt search input mode, circuits on the input card prevent a previously-activated and/or still-busy input card from being activated when IEN is programmed. Thus, the input cards can also be activated selectively as described above. Programming data transfers after installing the W6 jumper can be done as follows:

a. Activate all cards with W6 installed by programming the interrupt enable mode (IEN and TME are on).

b. As each card times out, search for the data ready card, read in the data, and deactivate the ready card.

c. After all cards have timed out, been read, and deactivated, reactivate all cards again by repeating Step a. If no more data is expected, leave all cards deactivated. Note that the procedure above treats the input cards as a group so that the W6 jumper provides an especially handy tool for rapidly communicating with devices having similar data transfer rates in which they all will time out at around the same time after activation and can be read at that time after which they all can again be reactivated for the next data cycle.

3-11 It is assumed in the following discussion that the reader is familiar with the definitions and functions of multiprogrammer control and address words. If this is not the case, it is suggested that Section III of the 6940A Instruction Manual be reviewed before proceeding.

3-12 DATA STROBE (DST)

3-13 The DST line is wired to all multiprogrammer 400 series slots. The DST line goes HI when the computer gate input to the multiprogrammer goes true and stays HI for the length of the computer gate. The computer gate is set by the computer but is reset by the multiprogrammer flag back to the computer (when the flag goes busy). If the multiprogrammer is in the timing mode (TME on) and the interrupt enable mode is off (IEN off), the multiprogrammer flag is controlled by a combination of the multiprogrammer timing circuits and the input/output card Common Timing Flag (CTF) circuits. In this case, the multiprogrammer flag goes busy and resets the computer gate (and, thus, resets the DST line) a short time after the DST signal goes HI (the multiprogrammer flag ready state will be entirely controlled by the card Common Timing Flag circuits, however). When the IEN mode is on along with the TME mode, however, the multiprogrammer flag does not go busy after DST to reset the computer gate and DST. Instead, the multiprogrammer flag follows the input cards' CTF line and goes busy to reset the computer gate (and, therefore, DST) only when an input card CTF line goes busy. Note that since all input and output cards generate CTF outputs, all output cards should be allowed to time out before programming the interrupt enable mode (IEN and TME on). If the multiprogrammer is in the fast (handshake) mode (TME off), on the other hand, the multiprogrammer flag to the computer is set busy (as it is for TME on with IEN off) a short time after the DST line goes HI. Thus, depending upon the state of IEN and/or TME, the DST signal is either a short duration pulse used to strobe the input cards or it is a level used to control the input card timing circuits (i.e. in the interrupt enable mode).

3-14 The DST signal is generated for each multiprogrammer control word and notifies the multiprogrammer to store the control word mode of operation specifications. The DST signal is not, however, required for input card address words. If the DST signal is provided in an address word, its affect depends on the state of the multiprogrammer input select (ISL) mode as follows:

a. If ISL was programmed on prior to the address word and DST, the data strobe causes the input card to be activated. This means that the input card GATE to the external device will be generated to notify the device that data is requested and to start the data transfer cycle. In addition, the input card control circuits will be set to store the fact that the input card was activated.

b. If ISL was programmed off prior to the address word and DST, the data strobe resets the input card control circuits and the card is, therefore, deactivated. When deactivated, the input card cannot signal that data is ready in the interrupt enable mode (the card could still signal ready if operated in the dedicated input mode; i.e. if the card is addressed after it is activated and subsequently deactivated).

3-15 INPUT SELECT (ISL)

3-16 The ISL line is wired to all multiprogrammer 400 series slots but is only utilized by cards having input capability. Within the multiprogrammer, ISL reverses the direction of data flow and allows data from an addressed input card to be sent to the computer. In addition, ISL causes the multiprogrammer to combine an addressed input card's input request identification signal (IRQ) with bit 15 of the return data lines for application to the computer. At the input card, ISL enables the card to be activated (if the card is addressed and the data strobe is generated as discussed above).

3-17 CARD ADDRESSING

3-18 An input card is selected to transmit data and/or activate/deactivate when its associated address bits (B12/$\overline{\text{B12}}$ through B15/$\overline{\text{B15}}$ and a unit select line U--) are all HI. Although both the true and complemented forms of the address bits are represented on Figure 3-1, only one of the two states is present on each of the four address gate lines when the card is installed in a multiprogrammer slot. For example, if the input card is installed in slot 405, then bits B12(1), $\overline{\text{B13}}$(2), B14(4), and $\overline{\text{B15}}$(8) will be present on the address lines, and all four lines will be HI when the associated multiprogrammer unit is selected as part of a control word. The unit selection is stored in the 6940A and remains in effect until a different unit is selected by a subsequent control word.

3-19 In addition to enabling data transfer to the computer, the card address is also required during the dedicated input mode of operation to allow the card to signal when it has data ready (assuming, of course, that the card was activated and its external device times out). The card address is also required to enable a data ready card to apply its IRQ signal (which is combined with return data bit 15) to the multiprogrammer main frame providing the input card is ready and the control circuits are in the active state (and ISL is on in the main frame).

3-20 INTERRUPT ENABLE (IEN) MODE

3-21 The IEN line is wired to all multiprogrammer 400 series slots but is only utilized by cards having input interrupt capability. When programmed in a control word, IEN enables previously activated input cards to signal the computer when data is ready (assuming, of course, that the card's control circuits are in the active state). In addition, assuming jumper W6 is not removed, IEN activates

the input card(s) providing the card is not currently busy and had not been previously set to the active state. If the card is busy or its control circuits are already set active, the card is not activated when IEN is programmed and the card's GATE to the device is not set.

3-22 INPUT BITS $\overline{B00}$ THROUGH $\overline{B11}$

3-23 Input Data Transfer. Option jumper W10 is installed on the input card at the factory, so that external device input bits $\overline{B00}$ through $\overline{B11}$ are stored in the digital input card storage register when the card receives the trailing edge of the external device flag input. If ISL and the card address has been programmed, the stored bits will be transferred to the computer (via the multiprogrammer main frame) through the output logic gates. If storage disable jumper W10 is removed, the flag trailing edge is not required so that input data appears at the output logic gates as received from the device. Figure 3-2 shows the pin numbers on the digital input card input connector to which the input bits can be applied.

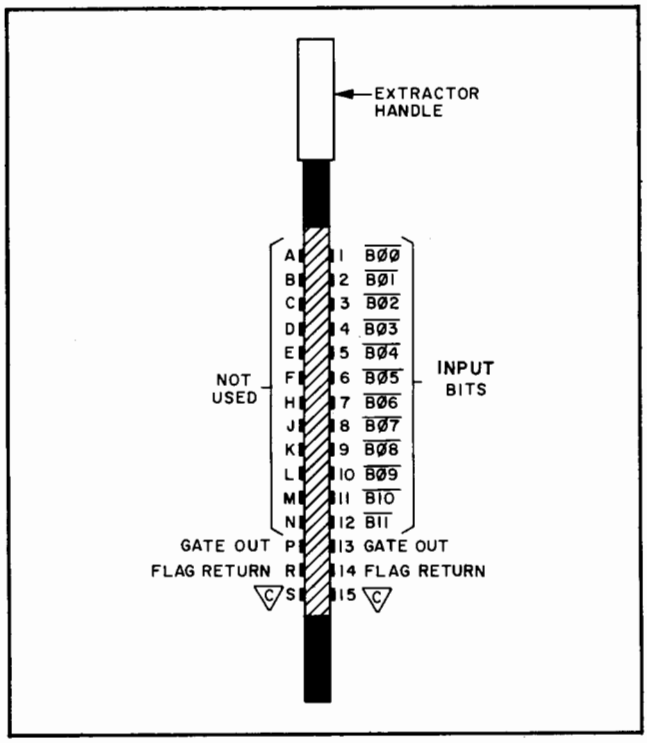



Figure 3-2. 69431A Input Connector

3-24 Input Bit Levels. The digital input card is supplied from the factory to accommodate negative- or positive-true logic sense TTL/DTL microcircuit logic level data inputs (Options 069 and 073, respectively) as well as negative-true open collector data inputs (Option 070). Figure 3-3 depicts the receiver circuits employed for the three options. As shown, for the microcircuit logic level options, a 1k pullup resistor (R1) is provided in the input circuit and the data input is jumpered through W4 (installed for these options) to the storage register. For the 073 option, an input bias network (R1, R2, and R3) is supplied as well as a level conversion gate (hybrid IC) the combination of which changes the open collector logic levels to the microcircuit levels used in the input card and multiprogrammer. Notice that, as required by the user, the input card receiver circuits can be custom modified (at the factory or by the user) to accommodate other logic sense and logic level requirements.

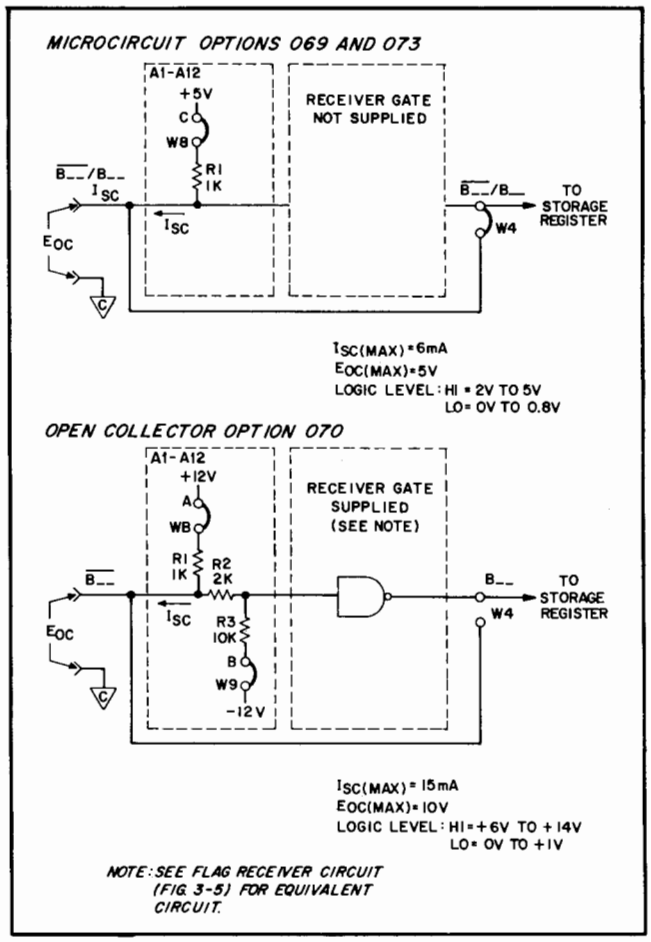


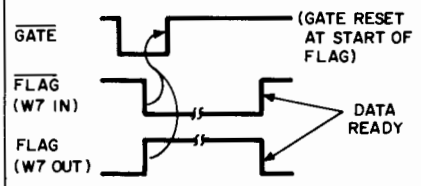
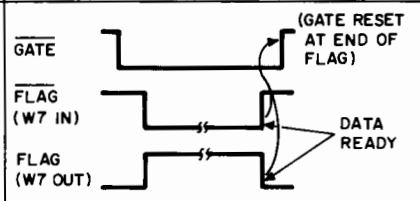
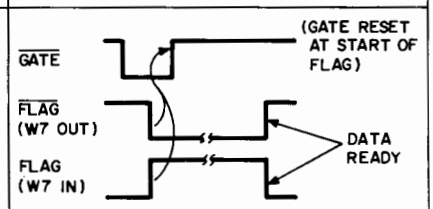
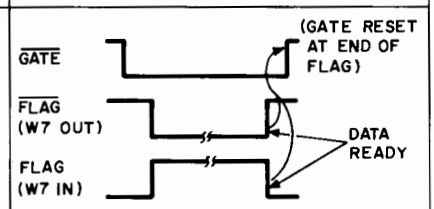

Figure 3-3. Typical Data Bit Receiver Circuit

3-25 GATE

3-26 The input card gate signal notifies the external device that the input card is ready for data. The GATE signal is generated when the input card is activated as discussed previously. Depending upon option jumpers W1 and W2, the GATE signal is reset either when the external device responds to the GATE by setting the FLAG input to the busy

state (leading edge) or at the ready state of the FLAG input (trailing edge). See Table 3-1 for a summary of jumper connections required to select either leading or trailing edge GATE reset. In addition to initiating the data transfer cycle with the external device, the GATE signal, when set, also resets the input card Flag flip-flop. If the input card is in the dedicated input mode (the card address is enabled), the reset state of the Flag flip-flop causes the input card $\overline{CTF}$ output to go LO (which signals the computer that the input card is busy).

Table 3-1. GATE and FLAG Timing Options

| FLAG JUMPER CONNECTIONS | | GATE TIMING RELATIVE TO DEVICE FLAG |
|---|---|---|
| W1 | W2 | |
| A* | B* |   |
| A | A |   |
| B** | A** |   |
| B | B |   |

* JUMPERS CONNECTED IN THESE POSITIONS AT THE FACTORY FOR OPTIONS 069 AND 073.

** JUMPERS CONNECTED IN THESE POSITIONS AT THE FACTORY FOR OPTION 070.

3-27 The $\overline{GATE}$ output of the input card is produced by the driver circuit depicted in Figure 3-4. As shown, two jumpers, W5 and W3, are provided in the driver circuit to allow either negative- or positive-true logic sense (jumper W5) and/or microcircuit or higher logic level output (jumper W3). Jumper W5 is connected at the factory to the A position which selects the positive-true state of the GATE signal for application to the gate driver. After inversion by the driver, the negative-true $\overline{GATE}$ output is applied to the external circuit. If the user desires positive-true GATE output, he must connect the W5 jumper to the B position. Similarly, the W3 jumper is connected to position A to provide microcircuit logic level output. For higher logic level output, the W3 jumper is connected to position B.

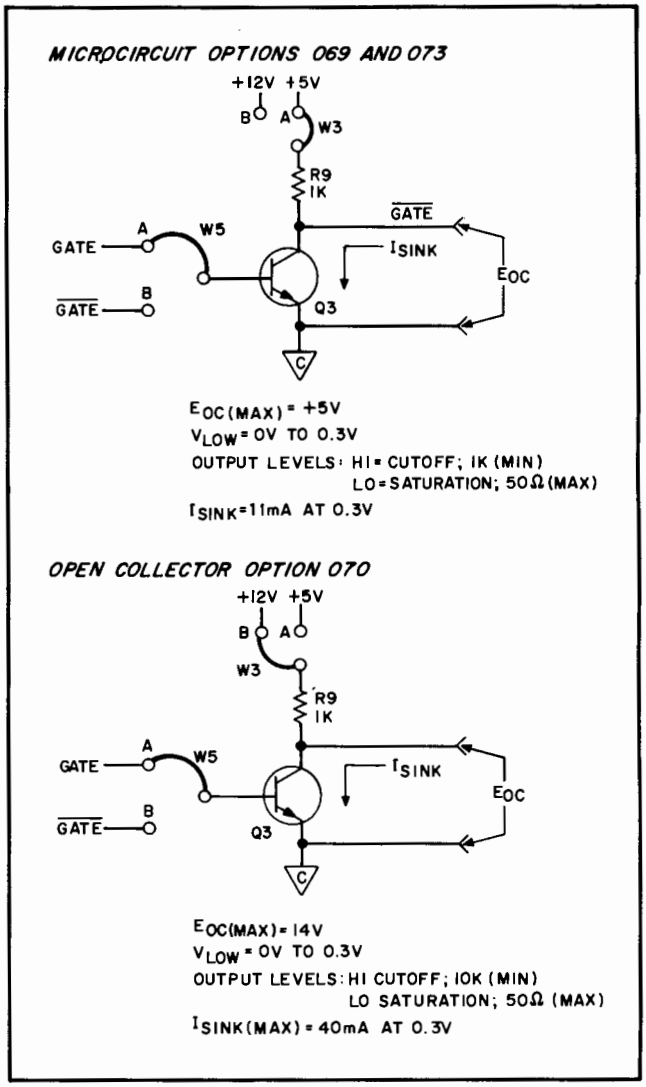



Figure 3-4. GATE Driver Circuit

3-28 FLAG

3-29 The external device signals when it is busy or ready with data via the device FLAG input to the input card. The leading edge of the FLAG signals

the input card that the external device is busy processing data (in response to the input card GATE signal to the device). The busy transition of the FLAG input (leading edge) can be selected to reset the input card GATE output in preparation for the next data transfer cycle (card activation). The GATE can also be reset with the trailing edge (data ready) of the FLAG. Refer to Table 3-1 for a summary of jumper connections required to select either leading or trailing edge GATE reset.

3-30 The trailing edge of the FLAG input is also used to notify the input card that data is available from the external device. If jumper W10 is installed, the ready transition of the FLAG strobes the data into the input card storage circuit. Data must be available on the input connector for 3μsec after the FLAG reaches the ready logic level. Further, the rising and falling edges of the FLAG must be $\geq$ 0.1V/μsec (thus, a 3.5V to 0V FLAG transition must reach approximately 0V within 35μsec). In addition to data strobing, the trailing edge of the FLAG sets the input card Flag flip-flop to the ready state. If the input card is in the dedicated input mode (the card address is enabled), the $\overline{\text{CTF}}$ output is switched to HI at this time to notify the computer that data is ready. If the input card is in the interrupt search input mode (IEN is on, DST is HI and the card has been activated), the ready state of the input card causes the $\overline{\text{CTF}}$ output to go LO. In this mode, the LO state of $\overline{\text{CTF}}$ causes the computer gate to reset which, in turn, resets the multiprogrammer DST signal. When reset, the DST signal switches the input card's $\overline{\text{CTF}}$ output HI to notify the computer that data is ready.

3-31 The device FLAG input passes through a receiver circuit that is comprised of discrete components but has identical specifications as the data bit receiver circuits previously described (see Figure 3-5). The Flag receiver circuit allows negative- or positive-true logic sense $\overline{\text{FLAG}}$ inputs to be utilized as well as open-collector inputs. The W7 jumper (which is comparable to the data bit W4 jumpers) is installed for microcircuit logic level inputs (Option 069 and 073) and applies the $\overline{\text{FLAG}}$ input directly to the input card logic circuits. The W7 jumper is removed for the open collector $\overline{\text{FLAG}}$ input thus allowing an input bias circuit and inverter to be installed in order to convert the input to the microcircuit logic level.

3-32 GATE/FLAG TIMING

3-33 The W1 and W2 jumpers, in conjunction with the W7 jumper, allow the input card GATE to the external device to be reset with either the leading or trailing edge of the device FLAG input. In addition, the W1 and W2 jumpers are selected so that the trailing edge of the FLAG input strobes data into the input card storage circuits (assuming jumper

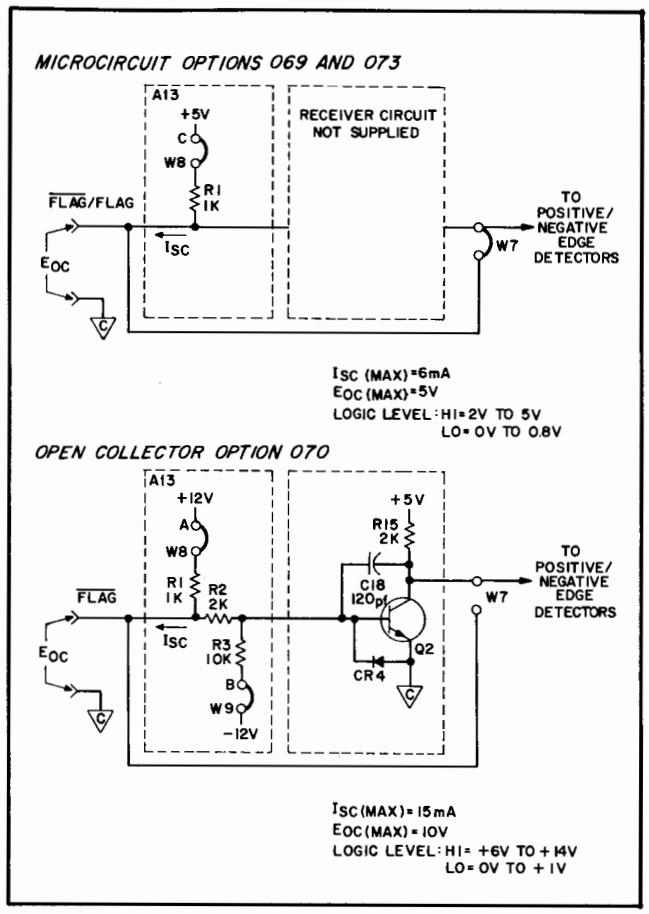



Figure 3-5. Flag Receiver Circuit

W10 is installed so that the data storage strobe is required). Further, the FLAG trailing edge sets the input card Flag flip-flop to the data ready state. Table 3-1 summarizes the GATE/FLAG timing relationships that can be selected by changing the W1 and W2 connections. The table assumes that the negative-true $\overline{\text{GATE}}$ output to the external device is selected (W5 connected to position A). The timing relationships apply equally if positive-true GATE is used (W5 connected to position B). The table lists the W1 and W2 connections required for microcircuit logic level FLAG inputs (W7 is installed) or for other than microcircuit logic level FLAG inputs (i.e. if open collector logic is used in which case W7 is removed and the FLAG receiver circuit is employed). For example, as shown in the table, if a negative-true open collector $\overline{\text{FLAG}}$ input is used and the GATE is to be reset on the trailing edge, the W1 and W2 jumpers must be both connected to position B (the W7 jumper is, of course, removed.).

3-34 CABLE FABRICATION

3-35 Since the Digital Input Card may be used to interface with various external devices, an interconnecting cable must be prepared for the particular

device being used. A 30-pin connector is furnished with each Digital Input Card for this purpose. Figure 3-2 illustrates the signals and associated connector pin numbers of the Digital Input Card. A 30-conductor cable (28 gauge max. wire) is required to interconnect the card and the external device. The cable length should be kept as short as possible.

# SECTION IV
# PRINCIPLES OF OPERATION

## 4-1 INTRODUCTION

4-2 This section contains principles of operation for Digital Input Card, Model 69431A. Theory is presented on both a block diagram and a detailed circuit theory level.

## 4-3 BLOCK DIAGRAM THEORY

4-4 Figure 4-1 is a block diagram of the digital input card. The card consists of three main functional circuit groups: (1) data storage and input circuits which interface 12-bit external device data for input to the computer via the multiprogrammer main frame; (2) gate/flag circuits which exchange control timing signals with the multiprogrammer and external device to synchronize data transfers; and (3) a control circuit that stores the activation status of the digital input card. In addition to the three main functional circuit groups, the input card also includes a power turn-on preset circuit which initializes the digital input card functional circuits when multiprogrammer power is turned on.

4-5 DATA STORAGE AND INPUT CIRCUITS

4-6 The data storage and input circuits consist of an address gate, 12-bit receiver circuits, 12-bit data storage circuits, and 12 output gates. When the input card slot is addressed in a multiprogrammer address word, the slot address bits all go to the HI state. If the unit containing the card was previously addressed in a multiprogrammer mode control word, U-- is also HI. When all address inputs are HI, the card select signal, applied to the data output gates and to the gate/flag circuits, is enabled. The card select signal couples the 12-bit input data from the output gates to the multiprogrammer main frame data bus. If the multiprogrammer is in the input select (ISL) mode, the 12 data bits appear at the return data lines (bits 0 - 11) from the multiprogrammer to the computer.

4-7 Data is entered into the input card storage circuits through the receiver circuits which convert, as necessary, user logic levels to the logic levels employed in the multiprogrammer. Depending upon user requirements, option jumpers and receiver circuit input bias networks are selected to interface the following logic sense and voltage level inputs: (1) negative-true TTL/DTL microcircuit-level input data (Option 069); (2) positive-true TTL/DTL microcircuit-level input data (Option 073); and (3) open collector negative-true input data (Option 070). In addition, the receiver circuits can be modified to satisfy other interface requirements (such as relay contact closure input data). The jumper assignments required for the 069, 073, and 070 options are described completely in Section III.

4-8 With option jumper W10 installed, input data is stored in the data storage circuit when the device flag switches to the ready state (trailing edge). At the trailing edge of the device flag, the outputs of the receiver circuits are strobed into the data storage circuits. Notice that with jumper W10 removed, the flag trailing edge storage requirement is disabled so that the device input data appears at the output gates as received from the device.

4-9 GATE/FLAG CIRCUITS

4-10 The digital input card gate/flag circuits consist of gate and flag flip-flop storage circuits as well as common timing flag (CTF) and input request (IRQ) identification circuits. The gate/flag circuits provide, in conjunction with the input card control circuits, data transfer synchronization among the programming source (via the multiprogrammer main frame, of course), digital input card, and external device. The functions performed by each of the gate/flag circuits are described below.

4-11 Gate Flip-Flop. The gate flip-flop synchronizes the start of data transfers between the computer and the external device. The gate flip-flop is set under program control to notify the device that the input card is ready to accept new data. The output of the gate flip-flop is applied to the external device through option jumper W5 which is used to provide either negative- or positive-true logic sense output. The output of the gate flip-flop is also applied to the flag flip-flop such that when the gate flip-flop is set, the flag flip-flop is reset to the busy state.

4-12 The gate flip-flop can be set (toggled) to begin data transfer operations in two ways, one of which requires that option jumper W6 be installed while the other does not depend on the W6 jumper. The second method of setting the gate flip-flop (the one not requiring the W6 jumper) is the usual way of controlling the flip-flop and requires that the card be selectively addressed. In this method, the gate flip-flop is set when the card is addressed in the ISL mode and in addition, a data strobe is

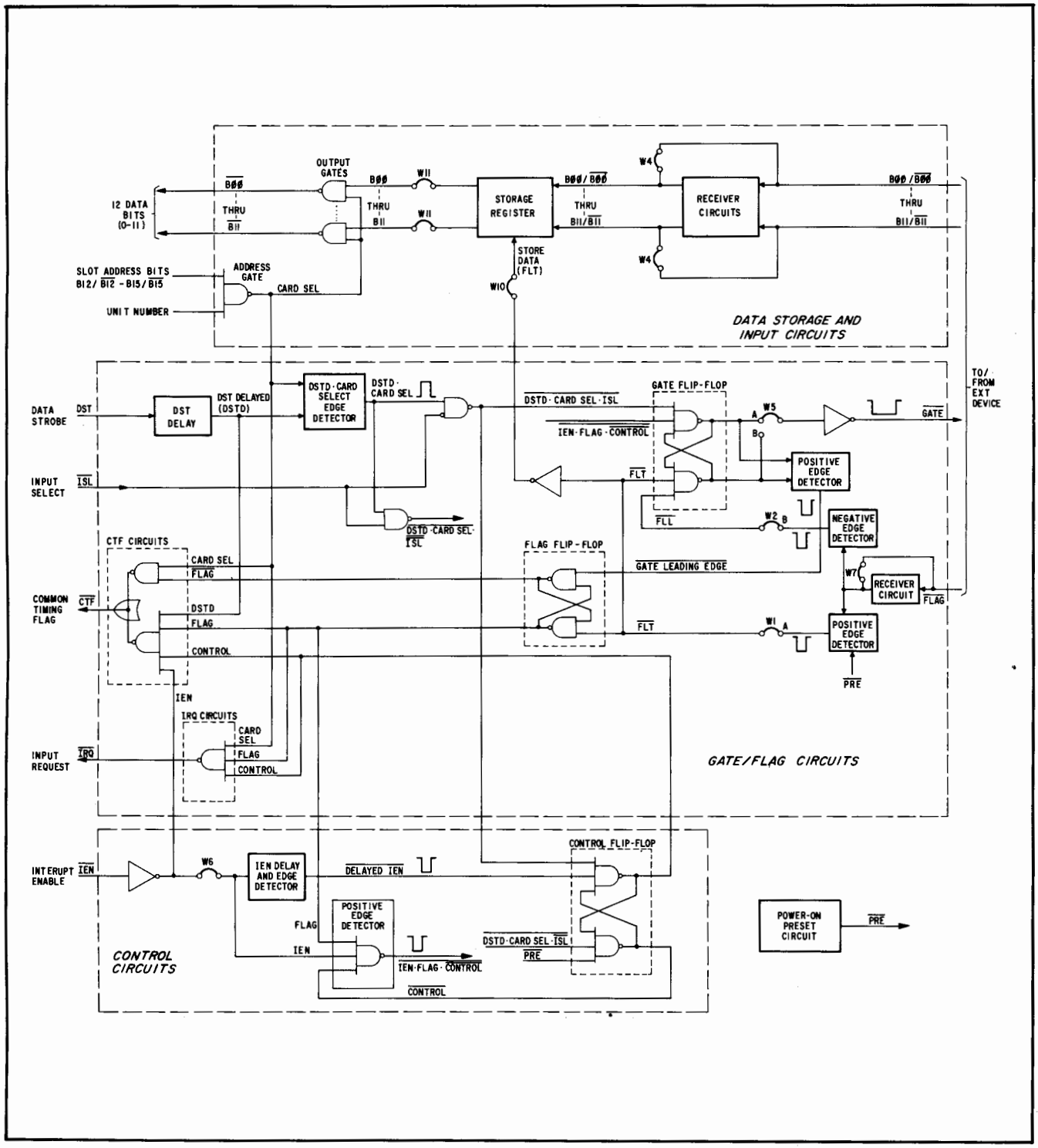



Figure 4-1. Digital Input Card, Model 69431A, Block Diagram

received. If jumper W6 is installed, however, the gate flip-flop can also be set and the input card activated by programming the IEN mode of operation assuming that the card is not busy (the flag flip-flop must be in the ready state) and the card has not been previously activated (the control flip-flop must be reset). Thus, if these conditions are met, the input card (and all input cards having W6 installed) will be activated and begin a data input transfer cycle when the IEN mode is programmed.

4-13 With the W1 and W2 jumpers connected as shown, the gate flip-flop is reset by both the leading edge and the trailing edge of the device flag input. Some time after it receives the gate signal, the device should switch its flag input to the busy state (leading edge). Normally, at this transition, the gate flip-flop will be reset. However, under certain circumstances it may be possible to "hang up" the gate output of the input card. This might occur, for instance, if the input card gate flip-flop is toggled (set) a second time before the device signals that it is ready (trailing edge of device flag). Thus, if the gate flip-flop were reset only with the leading edge of the flag, and the gate flip-flop were set after the leading (busy) edge had been received, the gate line to the device might be locked up. As a precaution against this possibility, the trailing edge of the external device flag input is also used to reset the gate flip-flop. Note that jumpers W1 and W2 can be connected to the same position (A or B) in which case the gate flip-flop will be reset only with the trailing edge of the device flag input. See Section III for details.

4-14 Flag Flip-Flop. The input card flag flip-flop stores the data busy/ready status of the input card (and external device) for use in the common timing flag and input request circuits. The flag flip-flop is reset to the busy state when the gate flip-flop is set. At some time after the gate flip-flop is set, the external device should switch the flag input to the busy state. At a time determined by the specific external device, the device input data is made available to the input card. When data is ready, the device flag input should switch to the ready state (trailing edge). The trailing edge of the device flag causes the input card flag flip-flop to set to the ready state. The flag flip-flop remains in the ready state (set) until it is reset to busy again when the gate flip-flop is set.

4-15 The flag input passes through a receiver circuit that is similar to the data receiver circuits and which allows a variety of input flag logic sense and logic level input specifications to be accepted. Option jumpers W1 and W2 (in conjunction with W7, which allows optional logic level inputs to be used) provide for the reception of either negative- or positive-true logic sense flag inputs from the external device and allow the input card gate to be reset with the ready and/or trailing edge of the device flag.

4-16 Common Timing Flag (CTF) Circuit. The input card's $\overline{\text{CTF}}$ output signal reflects the data readiness status of the input card and is used to signal the computer when data is available. The CTF circuit can be operated in two basic modes of operation. One mode, the dedicated input mode is used for simple data transfer sequences and requires that the input card be addressed before it can signal the computer (through the multiprogrammer main frame) that data is ready. The other mode, the interrupt search input mode, is used in more complex data transfer sequences (sequences in which several — up to 240 — input cards can be active at the same time) and does not require that the card be addressed before it can signal the computer that data is ready. Note that for either mode of operation, the multiprogrammer must be programmed to the timing mode (TME on) in order to allow the input card $\overline{\text{CTF}}$ output to control the multiprogrammer's flag output to the computer. If the multiprogrammer is not in the timing mode, it ignores the $\overline{\text{CTF}}$ line and generates an automatic (handshake) flag to the computer.

4-17 Dedicated Input Mode. In the dedicated input mode, the $\overline{\text{CTF}}$ output of the input card follows the reset output of the flag flip-flop assuming that the input card address is enabled. When the flag flip-flop is reset to the busy state, then the $\overline{\text{CTF}}$ output goes LO to indicate that the input card is busy. $\overline{\text{CTF}}$ stays LO until the flag flip-flop switches to the ready state at which time $\overline{\text{CTF}}$ goes HI to notify the computer that data is available. This data transfer sequence is repeated as long as the input card is addressed.

4-18 Interrupt Search Input Mode. In the interrupt search input mode, the interrupt enable mode (IEN) is on (as well as TME in the multiprogrammer) and the $\overline{\text{CTF}}$ line is controlled by both the input card flag flip-flop (set output) and the data strobe (DST) input to the card. When the flag flip-flop is set to the ready state with IEN and the delayed DST both on, the $\overline{\text{CTF}}$ output goes LO. The LO state of $\overline{\text{CTF}}$ should cause the computer to switch the DST input to the LO state. When DST goes LO, the $\overline{\text{CTF}}$ output goes HI and the computer is notified that data is available. Notice that the computer program entirely controls the operation of the input card gate/flag and CTF circuits and must, in addition, interpret the subsequent data ready/busy reaction of the input card as reflected in the $\overline{\text{CTF}}$ output.

4-19 Input Request (IRQ) Identification Circuit. The IRQ circuits aid the computer in determing the data ready/busy status of the input card (especially in the interrupt search mode which involves many input cards any one of which can signal the

computer that data is ready via the $\overline{CTF}$ line). The $\overline{IRQ}$ output is enabled (LO) when the input card is addressed, the flag flip-flop is set to ready, and the card is activated (control flip-flop is set). When these conditions have been met, the $\overline{IRQ}$ output goes LO and is combined with the $\overline{IRQ}$ output of all other input cards (only the addressed card controls the common $\overline{IRQ}$ line, however) in the multiprogrammer main frame. Further, assuming the ISL mode is on, the multiprogrammer combines the $\overline{IRQ}$ signal with the bit 15 return data line that it sends to the computer. Thus, bit 15 of the data returned to the computer when an input card is addressed in the ISL mode reflects the data ready state of the addressed input card. In the interrupt search mode, then, the computer can interrogate (address) each of the active cards in a software-controlled priority and determine which one is ready with data by examining the state of bit 15 returned with the input card's data bits.

## 4-20 CONTROL CIRCUITS

4-21 The control circuits include a control flip-flop that stores the activation status of the input card. In addition, the control circuits process the IEN input when the W6 jumper is installed. Like the gate flip-flop, the control flip-flop is set when the input card is activated (the card is addressed and strobed in the ISL mode or, if jumper W6 is installed, when IEN is programmed). The control flip-flop remains set until the card is deactivated (the card is addressed and strobed and the ISL mode is off). When set, the control flip-flop enables (along with IEN, the flag flip-flop, and DST) the CTF line during the interrupt search mode of operation. Similarly, the control flip-flop enables (along with the card address and flag flip-flop) the $\overline{IRQ}$ output of the input card.

4-22 If the W6 jumper is installed, the control circuits receive and process the IEN input. When IEN is programmed ($\overline{IEN}$ goes LO), the processing circuits set the control flip-flop after a delay of approximately 0.5μsec. The delay is utilized to prevent the input card's gate flip-flop from being set when IEN is programmed on and the control flip-flop is already set (activated). Further, the gate flip-flop is not set when IEN is programmed if the flag flip-flop is in the busy state (reset). Under these conditions, the card must have been previously activated and then subsequently deactivated with the gate/flag circuits still timing out; therefore, the gate flip-flop is prevented from being re-toggled when IEN is programmed on. Of course, if the card is in the data ready state (flag flip-flop is set) and the control flip-flop is off, the gate flip-flop is set to initiate a data transfer cycle. In addition, the control flip-flop is set after the delay period. Thus, with the W6 jumper installed on several input cards, the program can activate the entire group at one time. Note, however, since it is possible to reactivate a card (set the control flip-flop) that had been previously deactivated, the IEN jumper should be used with discretion in controlling the activation of input cards.

## 4-23 POWER-ON PRESET

4-24 When multiprogrammer power is turned on, the preset circuit initializes the input card. The preset circuit generates a pulse that is used to generate the device flag leading and trailing edge pulses. The simulated device flag pulses, of course, reset the gate flip-flop and set the flag flip-flop to the ready state. In addition, the flag trailing edge pulse strobes the device data lines into the input card data storage circuits. The preset pulse is also applied directly to the control flip-flop where it resets the flip-flop and, consequently, deactivates the input card upon power turn-on.

## 4-25 GATE/FLAG/CONTROL CIRCUIT TIMING

4-26 Timing diagrams of the signals generated by the gate/flag and control circuits in the two basic modes of operation, the dedicated input and interrupt search input modes, are given in Figures 4-2 and 4-3, respectively. The timing diagrams assume that negative-true gate and flag signals are utilized and that the gate signal is to be reset at the leading edge of the flag (this is the 069 option). Further, it is assumed that the W10 jumper is still installed (which means that the device flag trailing edge is required for input data storage).

4-27 Dedicated Input Mode. The timing relationships of signals exchanged among the multiprogrammer, input card, and external device in the dedicated input mode are depicted in Figure 4-2 and described below:

$T_0$ — At $T_0$, the multiprogrammer has been programmed into the ISL mode. The input card was previously initialized (either as a result of the last data transfer cycle or if power were turned on) so that the gate and control flip-flops are reset and the flag flip-flop is set (ready).

$T_1$ — The input card is now activated with the combination of the card (and unit) address and the data strobe. The gate and control flip-flops are set with the LO state of the $\overline{GAT}$ output to the external device signaling the device that the input card can accept data. When set, the gate flip-flop also resets the flag flip-flop to the busy state which causes the $\overline{CTF}$ output to switch LO (card busy). Input data is available to the computer as long as card is addressed.

$T_2$ — In response to the $\overline{GAT}$ signal, the device $\overline{FLG}$ input switches busy (LO). The leading edge of $\overline{FLG}$ resets the gate flip-flop which switches the $\overline{GAT}$ output HI.

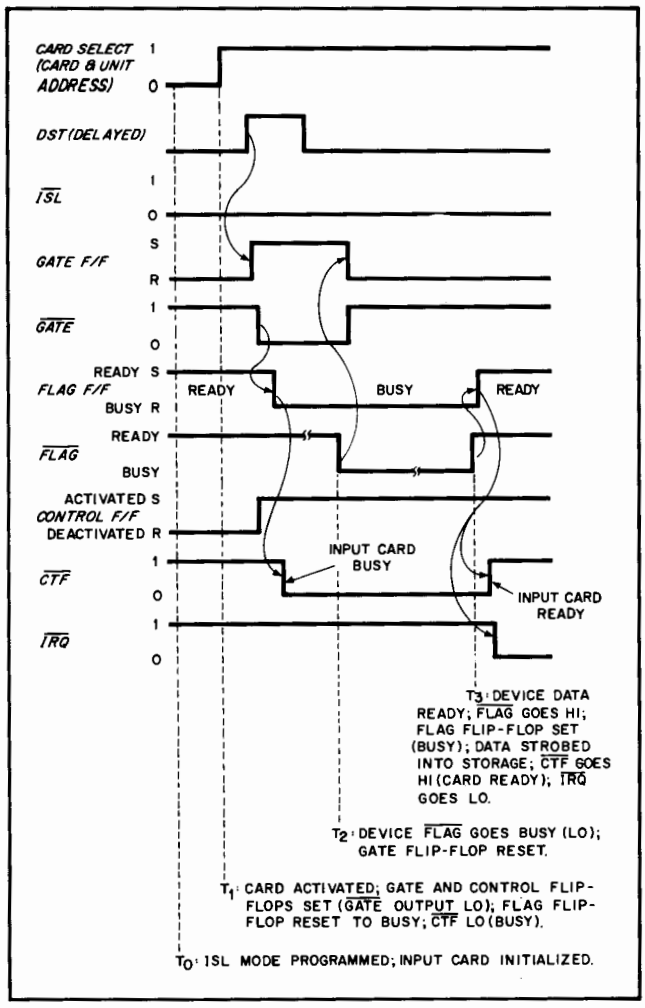



Figure 4-2. Dedicated Input Mode Timing Diagram

T3 — Device times out and is ready with data. The FLG input goes HI; trailing edge of FLG sets flag flip-flop and strobes data into storage. When set (ready) flag flip-flop switches CTF output to HI (card ready). IRQ also goes LO. Notice that the input card's CTF output is used to signal that the card is ready with data for the computer. The card address must be enabled, then, for this output to be generated and, in addition, the multiprogrammer must be in the timing mode (TME on) to allow the CTF line to control the multiprogrammer flag line to the computer. If the multiprogrammer is not in the timing mode (TME is off), the multiprogrammer returns an automatic flag (handshake flag) and ignores the input card CTF flag. Thus, computer software will be required to determine when the card has data ready which it can do by examining bit 15 of the data returned by the card. Bit 15, it will be recalled, contains the data readiness status of the input card as indicated by the IRQ output.

4-28 Interrupt Search Input Mode. The timing relationships of signals exchanged among the

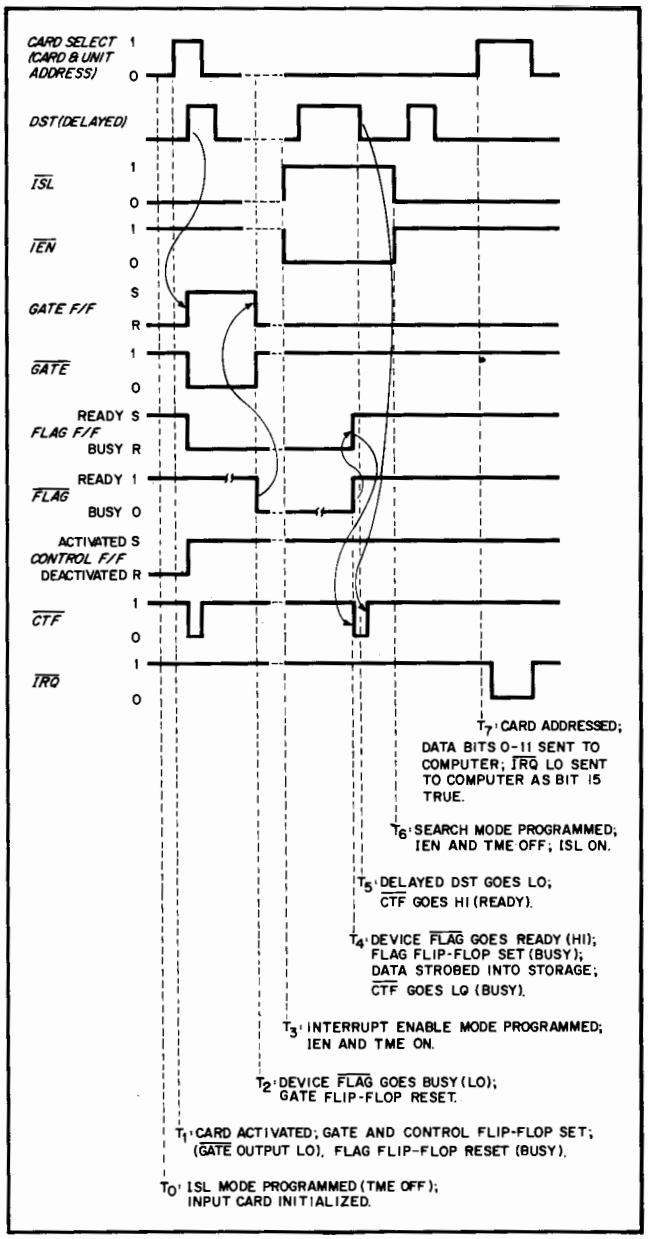



Figure 4-3. Interrupt Search Input Mode Timing Diagram

multiprogrammer, input card, and external device in the interrupt search input mode are depicted in Figure 4-3 and described below:

T0-T2 — The first steps of the interrupt search input mode are similar to the dedicated input mode. The input card is activated in the ISL mode; the external device should respond with a busy FLG (LO) after the input card GAT signal goes LO. Notice that the input card address is not maintained and that the multiprogrammer should be in the handshake mode (TME off) so that the CTF generated during input card activation will be ignored by the multiprogrammer (and computer). After the input card is activated, in addition, the computer can activate all

other desired input cards. It is assumed that during the activation of the other input cards, the external device responds to the $\overline{GAT}$ signal by switching the $\overline{FLG}$ input busy (LO). The device busy flag could, of course, occur at any time after the $\overline{GAT}$ signal goes LO.

$T_3$ - After activating all desired input cards, the multiprogrammer is programmed to the interrupt enable mode in which IEN and TME are on and ISL can be either on or off (it is assumed that the program turns ISL off).

$T_4$ - The system now waits for an external device to time out and signal that data is ready. When ready, the device switches its $\overline{FLG}$ input HI which sets the input card flag flip-flop to the ready state. The setting of the flag flip-flop causes the input card $\overline{CTF}$ signal to go LO ( busy). The trailing edge of the $\overline{FLG}$ input also strobes the device data into storage. Notice that since the ready status of the external device as well as the device input data is stored on the input card, the interrupt enable mode ($T_3$) could actually follow the device ready $\overline{FLG}$ transition and data input (in that case, when IEN is programmed on, $\overline{CTF}$ will go LO). Notice further, that even if the W6 jumper is still installed, IEN will not affect the input card gate flip-flop because the card's control flip-flop was set as a result of selective card activation.

$T_5$ - When $\overline{CTF}$ switches LO, and assuming the multiprogrammer is in the timing mode (TME is on), the multiprogrammer flag to the computer causes the computer interface card to switch the DST input LO (the DST input is derived from the computer gate input to the multiprogrammer). When DST goes LO, the input card $\overline{CTF}$ output switches HI (ready) which is the signal to the computer that data is available from an input card.

$T_6$ - Since any one of the activated input cards could have signalled that data is ready, the computer enters the search mode during which it will interrogate (address) each of the cards (in a software-determined priority) to determine which one is ready. In the search mode, the interrupt enable mode is turned off (to prevent data ready interrupts from other input cards) and the ISL mode is turned on. The timing mode is usually turned off (TME off) also to allow the fastest method (handshake) of communicating with the input cards.

$T_7$ - The computer now searches for the ready card. The card is addressed (without a data strobe in order to prevent reactivation of a busy card) and its data is returned to the computer on the multiprogrammer's return data lines. The computer must examine (by software) bit 15 (which includes the status of the $\overline{IRQ}$ signal) to determine if the card data it received is valid (ready) data. Note that when a ready card is addressed, its $\overline{IRQ}$ output is LO so that the bit 15 return line will be true.

4-29 After identifying the ready input card, the program has several options. It can deactivate the the card (address the card with a data strobe after turning ISL off); it can reactivate it; it can (after deactivating or reactivating the previously ready card) turn the interrupt enable mode back on and wait for the next input card to signal ready, etc. In any case, the program should at least take action with regard to input cards from which it accepts valid data. The card should be either reactivated or deactivated. If no more data is expected from the card, it should be deactivated in order to prevent the card from generating its $\overline{CTF}$ output when the interrupt mode is turned on again for other active cards. Deactivating the input card resets its control flip-flop which disables the $\overline{CTF}$ output during the interrupt enable mode.

## 4-30 DETAILED CIRCUIT ANALYSIS (See Figure 7-1)

4-31 DATA STORAGE AND INPUT CIRCUITS

4-32 Receiver Circuit. The configuration of the receiver circuit depends on the input card option in use. For microcircuit logic level options 069 and 073, only a 1k$\Omega$ pull-up resistor is provided in the input network and data inputs are jumpered directly to the storage register flip-flops. Open collector option 070, however, requires an input bias network and receiver gate as shown in Figure 7-1 in which case the jumpers are configured as listed on the schematic. The operation of the 070 receiver circuit is described below.

4-33 The Option 070 receiver circuit is comprised of a hybrid integrated circuit inverting gate (G1-G12) and an associated input bias network. The three resistors of the input bias network are selected so that a high (positive voltage) input level drives the inverter into full conduction while a low input level cuts the inverter off. Thus, the open collector input logic levels are converted to microcircuit logic levels with the output of the receiver circuit applied to the data storage register.

4-34 Data Storage. The 12-bit data storage register is comprised of three, 4-bit storage flip-flops, Z1 through Z3. Each flip-flop is a D-type, positive-edge triggered circuit. If storage disable jumper W10 is installed, the logical state at the D-input of a flip-flop is transferred to the Q output terminal when the clock terminal (CLK) is strobed by a positive-going device flag trailing-edge pulse. The $\overline{Q}$ output always assumes the state opposite the Q output. If the W10 jumper is removed, the CLK input is held positive and the D-input (data) controls the state of the flip-flop directly. Thus, with W10 removed, data appears at the output of the flip-flops as applied from the receiver circuits.

4-35 The Q or $\overline{Q}$ outputs of the storage flip-flops are selected by jumpers W11 such that, depending

upon the logic sense of the input data and the installation of the W4 receiver circuit jumpers, the binary logic value of input to the data output gates is always the same as the binary logic value of the original data input to the receiver circuits. For example, if the 069 (negative-true microcircuit logic level) option is in use, a binary 1 (LO) is jumpered through W4 to reset the associated storage flip-flop. The output, however, is taken from the reset side and is, thus, a logic one (converted to positive-true). Note, further, that the output gates invert the data bit outputs of flip-flops so that the input to the multiprogrammer is always negative-true data.

4-36 Address and Output Gates. When the slot and unit in which the input card is inserted are addressed, the four address bits and U-- go HI. Data bits BØØ through B11 are transferred through the output gates to the multiprogrammer data bus as data bits $\overline{B00}$ through $\overline{B11}$. If the multiprogrammer has been programmed into the input select (ISL) mode, the data bits are sent to the computer over the multiprogrammer return data lines (bits $\overline{B00}$ - $\overline{B11}$). The card select output of the address gate (G14) is also applied to the gate/flag circuits where it is used for the following functions: (1) enables the $\overline{CTF}$ output during dedicated input mode of operation; (2) enables the $\overline{IRQ}$ output when the card is activated and ready; and (3) used, in combination with the data strobe and ISL inputs, to activate or deactivate the input card.

4-37 GATE/FLAG CONTROL CIRCUITS

4-38 Detailed circuit operation of the gate/flag and control circuits is presented for the following phases of operation:

a. Selective card activation
b. Start-of-gate and $\overline{CTF}$
c. Start-of-flag
d. End-of-flag and $\overline{CTF}/\overline{IRQ}$
e. Card activation with IEN
f. Card deactivation.

4-39 Selective Card Activation. The input card gate/flag and control circuits are selectively activated when the card is addressed (the card select output of G14 is enabled) after the ISL mode has been programmed and the data strobe (DST) is received. The HI DST signal is first applied to inverter G15 the output of which is $\overline{DST}$. The $\overline{DST}$ signal next passes through a delay circuit comprised of resistor R6 and capacitor C12. Before $\overline{DST}$ goes LO, C12 is charged to approximately +3.5V, holding the input to inverter G16 at the logic one level. The inverted (LO) output of G16 holds NAND gate G17 disabled. When $\overline{DST}$ goes LO, C12 starts to discharge towards 0 volts through R6. After approximately 4μsec, C12 discharges to the zero logic level (approximately 0.8 volts). The delayed $\overline{DST}$ ($\overline{DSTD}$) signal is inverted to logic one through G16 to enable NAND gate G17. When the $\overline{DST}$ output of C15 goes HI, capacitor C12 charges rapidly to 3.5 volts through diode CR2 in preparation for the next DST input. Note that DST is delayed in order to prevent the input card from generating an erroneous $\overline{CTF}$ signal when the IEN mode is programmed off as part of the interrupt search mode of operation (see Paragraph 4-52).

4-40 After the 4μsec delay, the logic one DSTD output of inverter G16 is combined with the enabled card select input in NAND gate G17. The output on NAND gate G17, $\overline{CARD\ SELECT \cdot DSTD}$, is applied to a negative edge detector circuit (G18-G20, R8, and C7) which generates a short-duration negative pulse beginning at the leading edge of delayed DST. The negative pulse is used to control the setting of the gate and control flip-flops (it is also used to reset the control flip-flop during card deactivation, see Paragraph 4-55). The operation of the negative edge detector is described in the following paragraphs.

4-41 The negative edge detector circuit makes use of the discharge time of capacitor C7 to generate a negative pulse to set the gate and control flip-flops (card activation) and reset the control flip-flop (card deactivation). At the time $\overline{CARD\ SELECT \cdot DSTD}$ initially goes LO, capacitor C7 begins to discharge, but, since it cannot discharge instantaneously, it temporarily holds one input to G19 HI. G18 inverts $\overline{CARD\ SELECT \cdot DSTD}$ and holds the second input to G19 HI. The resulting LO pulse output of G19 is applied to inverter G20 which produces a short-duration positive pulse for combination with the input select (ISL) input. Note that the pulse width is determined by the discharge time of capacitor C7. When C7 has discharged to the LO logic level, gate G19 is inhibited and its output goes HI.

4-42 During the selective card activation process, the multiprogrammer is in the input mode and input $\overline{ISL}$ is LO. The CARD SELECT • DSTD pulse is combined with ISL to set the gate and control flip-flops. The positive pulse is applied to NAND gate G21 which also receives the HI ISL output of inverter G22. The pulse is coupled through the NAND gate, then, and the resultant negative pulse sets the gate flip-flop (cross-coupled NAND gates Z13) and the control flip-flop (cross-coupled NAND gates Z12). The input card is now activated with the gate and control flip-flops in the set state.

4-43 Start-of-gate and $\overline{CTF}$. The output of the gate flip-flop is inverted by driver Q3 and applied to output pin 13 for application to the external device. Jumper W5 allows either the set side of the gate flip-flop to be applied to Q3 or the reset side depending upon the logic sense requirements of the user's device. The transition (gate flip-flop set) of

the GATE/$\overline{\text{GATE}}$ signal should initiate the timing cycle of the external device which should also respond with a $\overline{\text{FLAG}}$ busy input to the card at some time after the $\overline{\text{GATE}}$ transition.

4-44 The set output of the gate flip-flop is also applied to a positive edge detector which generates a short-duration negative pulse that is used to reset the flag flip-flop when the gate flip-flop is set. The positive edge detector is comprised of NAND gate G22, resistor R7, and capacitor C8 and operates like the negative edge detector previously described in that the positive edge detector also makes use of the discharge time of a capacitor (C8) to generate a negative pulse to reset the flag flip-flop. At the time that the gate flip-flop is set, the reset side goes LO and capacitor C8 begins to discharge. The capacitor cannot discharge instantaneoulsy, however, so that it temporarily holds one input to NAND gate G22 HI. The second input to the gate is instantaneously HI when the gate flip-flop is set. The resulting LO pulse output of G22 is applied to the flag flip-flop and resets the flip-flop to the busy state.

4-45 As described above, the activation of the input card results in the gate and control flip-flops being set and the flag flip-flop reset to the busy state. The flag flip-flop will remain in the busy state until the external device $\overline{\text{FLAG}}$ input switches busy (leading edge) and then back to ready (trailing edge). Note, however, that if the input card is in the dedicated input mode of operation, i.e. the card's address is enabled after the card is activated, the inputs to NAND gate G23 are HI. The LO output of the gate is inverted by NOR gate G24 and again by driver Q4 and applied to output pin 7 for application as the LO $\overline{\text{CTF}}$ signal to the multiprogrammer. If the multiprogrammer is also in the TME mode, the LO $\overline{\text{CTF}}$ signal will control the multiprogrammer flag output to the computer such that the leading edge of the $\overline{\text{CTF}}$ signal notifies the computer that the input card is busy (flag flip-flop reset) processing a data transfer cycle with its external device. In this mode, the card address should be maintained until the device signals ready in order to keep the $\overline{\text{CTF}}$ line LO.

4-46 If the input card is not in the dedicated input mode, the resetting of the flag flip-flop during card acitvation will also set the $\overline{\text{CTF}}$ line LO since the card address will be enabled for a period after the flag is reset. However, the card address is not maintained during the interrupt search mode so that the $\overline{\text{CTF}}$ output will switch HI after the address is removed. Thus, when a card is activated as part of the interrupt search input mode, the toggling of the $\overline{\text{CTF}}$ output should be ignored by the computer (if the multiprogrammer is not in the timing mode, for instance, the $\overline{\text{CTF}}$ signal will be ignored in the multiprogrammer and will not control the multiprogrammer flag to the computer).

4-47 Start-of-flag. When the external device responds to the input card $\overline{\text{GATE}}$ signal, it generates the start-of-flag input by switching the $\overline{\text{FLAG}}$ input to the card to the busy state. The $\overline{\text{FLAG}}$ input passes through a receiver circuit that is functionally identical to the data bit receiver circuits (the FLAG receiver is comprised, however, of discrete components while the data bit receivers employ hybrid integrated circuits). The $\overline{\text{FLAG}}$ receiver includes a jumper, W7, that allows either microcircuit or open collector logic level $\overline{\text{FLAG}}$ inputs to be used.

4-48 After interfacing by the receiver circuit, the $\overline{\text{FLAG}}$ signal in inverted by G25 and applied to a 1μsec delay circuit comprised of resistors R1 and R2 and capacitor C16. The 1μsec delay of the $\overline{\text{FLAG}}$ signal reduces the susceptibility of the input circuits to transients. Resistor R11, connected between the output of G26 and G27, provides hysteresis to prevent oscillation with the increased rise time of Z11.

4-49 The combination of gates G26, G27, and G28 and resistor R3 and capacitor C10 comprise a positive edge detector while G26, G27, G29, and resistor R4 and capacitor C11 comprise a negative edge detector. The operation of the detectors is similar to the edge detectors previously described. The W1 and W2 jumper connections are selected in conjunction with the W7 jumper and the logic sense of the $\overline{\text{FLAG}}$ input such that the short-duration negative $\overline{\text{FLL}}$ and $\overline{\text{FLT}}$ pulses at the output of the positive and negative edge detectors are selected at the leading and/or trailing edges of the $\overline{\text{FLAG}}$ input depending on whether the gate flip-flop is to be reset at the leading or trailing edge of the flag input. For example, if the negative-true TTL/DTL option (069) is desired and the gate is to reset at the flag leading edge, W1 is connected to A and W2 is connected to B (W7 is also installed). Thus, when the $\overline{\text{FLAG}}$ input switches busy (LO), the positive edge detector produces a negative pulse (at the output of G28) that is coupled through W2 as the $\overline{\text{FLL}}$ signal and applied to the gate flip-flop to reset it in preparation for the next input card activation operation. See Section III for complete details on the W1 and W2 (as well as W7) jumper connections required to establish the various $\overline{\text{FLAG}}$ polarity and gate reset configurations.

4-50 End-of-flag and $\overline{\text{CTF}}$/$\overline{\text{IRQ}}$. When the external timing circuit times out, the $\overline{\text{FLAG}}$ input to the input card switches to the ready state (trailing edge). The positive- or negative-edge detector will produce a negative pulse at this time depending upon the logic sense input and corresponding jumper connections as described above. For the 069 option, the negative edge detector produces a negative pulse (at the output of G29) that is coupled through

W1 as the $\overline{FLT}$ signal. The $\overline{FLT}$ pulse is applied to the flag flip-flop to set it to the data ready state. In addition, $\overline{FLT}$ is inverted by driver Q7 which, if storage disable jumper W10 is installed, couples the positive FLT pulse to the 12-bit storage register to strobe the input data into storage. The card is now in the data ready state with the flag flip-flop set and the data stored in the storage register. When the flag flip-flop is set, it controls the $\overline{CTF}$ and $\overline{IRQ}$ outputs of the card as determined by the mode of operation, dedicated input mode or interrupt search input mode, currently in effect.

4-51 If the dedicated input mode has been established, the card address is enabled when the flag flip-flop is set and, therefore, the $\overline{CTF}$ output of driver Q4 goes HI (it went LO when the flag flip-flop was reset). Assuming, further, that the timing mode is in effect (TME is on), the HI transition of the $\overline{CTF}$ output notifies the computer that the card has data ready for the computer. Notice, too, that the $\overline{IRQ}$ output of driver Q1 is also LO at this time and can be used, if necessary, by the computer to determine if the card's data is valid (ready).

4-52 If the interrupt search mode is in progress, the card address is not enabled. Instead, the IEN and delayed DST inputs to NAND gate G30 are enabled as well as the control flip-flop input. Thus, when the flag flip-flop sets, the $\overline{CTF}$ output of Q4 goes LO. This LO transition of $\overline{CTF}$ (assuming TME is on) should cause the computer to disable the multiprogrammer's DST input (which is derived from the computer gate) at which time NAND gate G30 is disabled and the $\overline{CTF}$ output switches back to HI. The HI transition of $\overline{CTF}$ notifies the computer that the input card has data ready. When the computer, in its search mode (IEN off and ISL on) addresses the card, the $\overline{IRQ}$ output of Q1 is returned in bit 15 to the computer (which also, of course, receives the card's 12 data bits at the same time). Bit 15, then, is examined by the computer program to determine the validity of the data it receives from the input card. Notice that before it enters the search routine, the computer programs IEN off to prevent other input cards from generating CTF interrupts during the search process. Thus, DST is delayed on the input card to prevent this same card from again generating the $\overline{CTF}$ output which would occur since DST is used to reset IEN in the multiprogrammer main frame.

4-53 Card Activation with IEN. Jumper W6 allows the input card, along with all other input cards on which the jumper is also installed, to be activated (that is, the gate and control flip-flop set and the flag flip-flop reset) when the IEN mode is programmed in the multiprogrammer. If W6 is not installed, the card must be selectively activated and cannot be activated with IEN. The IEN input from inverter G31 (also used in the CTF circuits as previously described) is applied, through jumper W6, to the delay circuit comprised of resistor R5 and capacitor C9 and to the positive edge detector comprised of G32 and G33 (in conjunction with the delay circuit). When the $\overline{IEN}$ input goes LO, the output of G31 goes HI to enable one input of NAND gate G33. The input to inverter G32, however, remains LO until capacitor C9 can charge to the HI output of G31. Thus, the output of G32 is HI until the delay period (approximately 0.5μsec) expires and enables another input to G33. If the input card is not busy (the flag flip-flop is set) and the card is not already active (the control flip-flop is reset), the other inputs to G33 are enabled and the output goes LO. The output stays LO for the length of the delay period (until C9 charges to the HI output of G31) after which the G32 input to G33 goes LO to disable G33 and switch its output HI. The negative pulse output of G33 is applied to the gate flip-flop to set the flip-flop.

4-54 The delayed LO output of G32 is also applied to the negative edge detector comprised of G34, G35, resistor R26, and capacitor C17. When the delay period is over, the input to G34 goes LO and its output goes HI to enable one input of G35. Since C17 is charged positive, it cannot discharge instantaneously to the LO input from G32. Thus, the other input to G35 is temporarily held HI and the NAND gate produces a negative pulse to set the control flip-flop. Notice that the setting of the control flip-flop is delayed in order to prevent the gate flip-flop from being set if the control flip-flop was already set when IEN was programmed on (NAND gate G33 requires that the control flip-flop be reset during the delay period in order to produce the negative set pulse to the gate flip-flop).

4-55 Card Deactivation. The input card is deactivated when the card is addressed with a data strobe and the multiprogrammer is not in the ISL mode. The enabled card select and delayed DST output of G20 (discussed in Paragraph 4-40) is combined with the HI $\overline{ISL}$ output of G36 in NAND gate G37. When ISL is off, the LO output of G37 causes the control flip-flop to reset to the deactive state. As previously discussed, the control flip-flop must be set before the input card is allowed to signal the computer (via the $\overline{CTF}$ output) that data is ready when the input card is operated in the interrupt search input mode.

4-56 POWER TURN-ON PRESET

4-57 The power turn-on preset circuit (Q5 and Q6 and associated components) initializes the input card when power is turned on at the multiprogrammer control panel. The preset circuit produces a negative pulse to reset the gate and control flip-flops and to set the flag flip-flop. In addition, the preset pulse is used to strobe data on the device input lines into the card storage circuits (assuming

the storage disable jumper W10 is installed; if not, the input data appears at the output of the storage circuits as received).

4-58 When power is turned on, +5 volts is applied across the R-C circuit consisting of resistors R19 and R20 and capacitor C6. Since C6 cannot charge instantaneously, the base of Q6 remains below 5 volts, switching Q6 on. As the collector voltage of Q6 goes positive, Q5 is turned on driving the preset line to the device flag positive and negative edge detectors and to the control flip-flop LO. When capacitor C6 has charged to 3.8 volts (in approximately 50msec) both Q6 and Q5 are cut off, returning the preset line to the HI state. Diode CR1 provides a rapid discharge path for C6 when power is turned off. The negative preset pulse causes the flag edge detectors to generate negative pulses at the negative and positive edges of the preset pulse. The negative pulses are used to initialize the input card as follows: the gate flip-flop is reset, the flag flip-flop is set (ready), and the data storage flip-flops are strobed (receive the data on the input lines). In addition, the negative preset pulse is applied directly to the reset side of the control flip-flop to initialize (reset and, thus, deactivate) the flip-flop.

# SECTION V
# MAINTENANCE

## 5-1 INTRODUCTION

5-2 This section contains preventive maintenance instructions, checkout procedures, and troubleshooting procedures for Digital Input Card, Model 69431A.

## 5-3 TEST EQUIPMENT REQUIRED

5-4 The 6940A Multiprogrammer provides most signal inputs necessary for testing the Digital Input Card. It is assumed that the 6940A, as well as all other test instruments, are functioning properly at the outset of testing. The general purpose test instruments required for maintenance of the Digital Input Card are listed in Table 5-1.

5-5 A coaxial test lead with a 50Ω resistor (nominal) in series with the center conductor provides a handy means of simulating HI logic level (positive) signals. Further, for microcircuit logic levels (Options 069 and 073), the coaxial cable can be fitted with a BNC connector and attached to the multiprogrammer main frame Logic Probe Connector J8 which provides +5V output. To simulate higher logic levels (Option 070), the coaxial test lead can be connected directly to the +12V input of the digital input card (J1-2, B). The ground connection of the coaxial test lead can be left floating.

**NOTE**

If the coaxial test lead used for simulating the HI (positive) logic level is not provided with an isolating resistor, be careful in connecting the test lead to the digital input card test points. If the lead is inadvertently touched to common, the 6940A Multiprogrammer will go into current latch (in which case the positive voltage is reduced towards 0) and erroneous test readings will be produced. The 6940A A3 Logic and Timing board contains an indicating lamp that can be used to verify that the multiprogrammer is not in current latch. The indicator in normally on when the +5 volt output of the 6940A is correct.

## 5-6 PREVENTIVE MAINTENANCE

5-7 The only preventive maintenance necessary is to keep the printed-circuit connector contact fingers clean. A nonabrasive eraser, such as a "Pink Pearl" or a plastic eraser, should be lightly rubbed over the contact fingers to remove any film or foreign material.

## 5-8 CHECKOUT PROCEDURES

5-9 These procedures can be used to check operation of digital input cards when they are initially received, and as an aid in isolating trouble to a general circuit area if a malfunction is noted during operation. The procedures are performed with the input card plugged into an extender card and the extender card plugged into a multiprogrammer unit. It is suggested that the procedures for manually programming the 6940A be reviewed, as necessary, before proceeding. If an input card fails a test, make certain that it was programmed correctly before starting troubleshooting.

Table 5-1. Test Equipment Required

| TYPE | CHARACTERISTICS | USE | RECOMMENDED MODEL |
|---|---|---|---|
| Digital Multi-Function Meter | Voltage Accuracy: ±0.003% of reading. Resistance Accuracy: ±0.01% of reading +0.01% of range. | Voltage and resistance measurements. | HP Model 3450A with Option 002. |
| Logic Probe | Impedance: 10 kilohms Trigger Threshold: +1.4 volts nominal. Minimum Pulse Width: 30nsec. | Logic circuit troubleshooting. | HP 10525A. |

5-10 Checkout is accomplished in two steps. The first set of procedures, Table 5-2, verify operation of the data storage and input circuits, which include the following:

(1) Address Gate
(2) Receiver Circuits
(3) Storage Registers
(4) Output Logic Gates.

5-11 If a malfunction is noted while performing the data storage and input circuits checkout procedures, refer to the referenced troubleshooting table for additional fault isolation.

5-12 The second set of procedures, Table 5-3, verify operation of the gate/flag and control circuits. If a checkout test fails, refer to the referenced test in the gate/flag or control circuit troubleshooting table (Table 5-5).

5-13 The physical and electrical locations of parts referenced in the following procedures are illustrated in Figure 7-1.

Table 5-2. Data Storage and Input Circuits Checkout Procedure

| TEST NO. | EQUIPMENT CONNECTIONS | INSTRUCTIONS | NORMAL INDICATION | EVALUATION |
|---|---|---|---|---|
| 1 | Short Q7 base-to-emitter (not required if W10 removed). | Energize the multiprogrammer system. Select control word (bits 15, 14, 13, and 12, on). Program ISL (bit 7 on). Program unit address. Touch LOAD OUTPUT.<br>Program card slot in address word (bits 15 - 12).<br>Simulate logical 0 for input bits 0-11. Simulate HI inputs for Options 069 and 070 and LO inputs for Option 073.<br>Momentarily apply simulated inputs to corresponding edge connector pins on input card. | 6940A Switch Register bits 0-11 all go off. | If two or more bits are on, check the address gate or Q7 (see Paragraph 5-15).<br>If an individual bit is on, proceed to Test 2. |
| 2 | | Simulate a logical 1 for bit position 0. Simulate LO input for Options 069 and 070 and HI input for Option 073. | 6940A Switch Register bit lit. | If indication abnormal, refer to receiver circuit, storage register, and output gates troubleshooting (see Table 5-5). |
| 3 | | Repeat Test 2 for bit positions 1 through 11. | Same as Test 2. | Same as Test 2. |
| 4 (This step not required if W10 removed.) | | Simulate logical 0 for bit positions 0-11.<br>Remove short from Q7.<br>Simulate a logical 1 for bit positions 0-11. | Bits 0-11 all remain off. | If bits 0-11 come on, check Q7. |

Table 5-3. Gate/Flag and Control Circuit Checkout Procedure

| TEST NO. | EQUIPMENT CONNECTIONS | INSTRUCTIONS | NORMAL INDICATION | EVALUATION |
|---|---|---|---|---|
| 1 | Using logic probe, monitor $\overline{\text{GATE}}$ output at P2-13 | Select control word (bits 15-12 on); program ISL (bit 7 on) and unit address. Touch LOAD OUTPUT.<br>Program card slot in address word (bits 15 - 12). Touch LOAD OUTPUT. | Output level goes from HI to LO (Note 1) | If test fails, refer to gate/flag circuit troubleshooting (Table 5-5, Test 1). |
| 2 | Monitor $\overline{\text{CTF}}$ output at P1-7. | | Output level LO | Same as Test 1. |
| 3 (Note 2) | Monitor $\overline{\text{GATE}}$ output at P2-13. | Simulate start of external device $\overline{\text{FLAG}}$ input to P2-14 by switching $\overline{\text{FLAG}}$ input LO. (If positive FLAG option connected, switch input HI.) | Output goes from LO to HI (Note 1) | If test fails, refer to gate/flag circuit troubleshooting, Test 2. |
| 4 (Note 3) | Monitor $\overline{\text{GATE}}$ output at P2-13 and control panel RETURN DATA lamp. | Simulate end of external device $\overline{\text{FLAG}}$ input to P2-14 by switching $\overline{\text{FLAG}}$ input HI (if positive FLAG option connected, switch input LO). | Output goes from LO to HI (Note 1)<br>RETURN DATA lamp comes on ($\overline{\text{IRQ}}$ LO) | If test fails, refer to gate/flag circuit troubleshooting, Test 3.<br>If test fails, refer to gate/flag circuit troubleshooting, Test 4. |
| 5 | Monitor $\overline{\text{CTF}}$ output at P1-7 and control panel RETURN DATA lamp. | a. If Test 4 executed; check for normal indication.<br>b. If Test 4 skipped, do it now (i.e. simulate end of external device $\overline{\text{FLAG}}$ input). | a. Output level HI<br>b. Output level HI; RETURN DATA lamp comes on ($\overline{\text{IRQ}}$ LO) | a. If test fails, refer to gate/flag circuit troubleshooting, Test 3.<br>b. Same as Test 4. |
| 6 | Monitor $\overline{\text{CTF}}$ output at P1-7. | Select control word (bits 15 - 12 on); program ISL (bit 7 on) and IEN (bit 8 on) and unit address. Touch LOAD OUTPUT. | Output goes LO and then HI | If test fails, refer to gate/flag circuit troubleshooting, Tests 6 and 7. |
| 7 | Monitor control panel RETURN DATA lamp. | Program control word ISL off (bit 7 off) and unit address.<br>Touch LOAD OUTPUT program card slot. | RETURN DATA does not light | If test fails, refer to gate/flag circuit troubleshooting, Test 5. |
| 8 (Note 4) | a. Monitor $\overline{\text{GATE}}$ output at P2-13. | Program control word with ISL (bit 7) and IEN (bit 8) on and unit address. Touch LOAD OUTPUT. | a. Output goes LO (Note 1) | If tests fail, refer to gate/flag and control circuits troubleshooting, Test 8. |

Table 5-3. Gate/Flag and Control Circuits Checkout Procedure (Continued)

| TEST NO. | EQUIPMENT CONNECTIONS | INSTRUCTIONS | NORMAL INDICATION | EVALUATION |
|---|---|---|---|---|
| 8 (Cont'd) | b. Monitor CONTROL flip-flop set output (Z12-Pin 8). | | b. Set output goes HI | |
| 9 | Same as 8a. | a. Reset gate flip-flop by momentarily applying LO reset input (Z13-Pin 9).<br>b. Repeat Test 8 instructions. | a. Output goes HI (Note 1)<br>b. Output remains HI (Note 1) | Check Z16. |
| 10 | Same as 8a. | a. Set flag flip-flop by momentarily applying LO set input (Z8 - Pin 10).<br>b. Repeat Test 8 instructions. | b. Output remains HI (Note 1) | If test fails, check control circuit troubleshooting, Test 10. |
| 11 | Same as 8b. | Program card slot address. Touch LOAD OUTPUT.<br>Program control word with $\overline{ISL}$ (bit 7 off). Touch LOAD OUTPUT.<br>Repeat Test 8 instructions. | Set output goes HI | If test fails, refer to gate/flag circuit troubleshooting, Test 10. |



NOTES:
1. If jumper W5 has been connected to position B, output level will be the reverse of the normal indication.
2. Skip this test if option jumpers W1 and W2 have been connected for FLAG trailing-edge GATE reset (see Section III).
3. Skip this test if option jumpers W1 and W2 are connected for start-of-flag GATE reset.
4. If jumper W6 has been removed, Tests 8 through 11 are not required.

## 5-14 TROUBLESHOOTING

5-15 Faults occuring in the digital input card can be divided into two broad categories: (1) those affecting the input card's ability to input and interface data correctly; and (2) those affecting the card's ability to accomplish the timing and control functions necessary to synchronize data transfers between the external device and the multiprogrammer (computer). The input card's data storage and input circuits provide the first function (data input and interface) while the card's gate/flag and control circuits accomplish the second. Thus, generally, input card data problems can be localized immediately to the data storage and input circuits while card timing and control problems can be localized to the gate/flag and control circuits. However, an exception to the above general philosophy must be considered. That is, when jumper W10 is installed, the reception of data in the data storage circuits is controlled by the gate/flag circuits in that the end-of-flag pulse (FLT) is used to clock the data into the storage circuits. Thus, with W10 installed, data problems cannot be automatically localized to the data storage and input circuits. The following is a procedure for verifying that the end-of-flag pulse is correct:

a. With the input card inserted in the extender and the multiprogrammer energized, address the unit and program the ISL mode on. Next, address the appropriate card slot and then monitor the collector of Q7 with a logic probe (probe should be off).

b. Simulate a HI data bit (any bit from BØØ — B11) input.

c. Simulate the start-of-flag by applying a LO input to $\overline{\text{FLAG}}$ input P2-14 (apply a HI if you have connected the input card jumpers to accept positive level FLAG input).

d. Simulate the end-of-flag by removing the LO input from step (b). (Remove the HI input if positive FLAG used.) The logic probe should flash on when the end-of-flag is simulated. If the logic probe does not flash on, the data problem is in the gate/flag circuits. Similarly, if the probe flashes on and the control panel Switch Register lamp associated with the simulated input bit comes on, then the problem is also in the gate/flag circuits (see paragraph 5-23). On the other hand, if the logic probe does flash on and the Switch Register lamp is not on, then the data problem is in the input card data storage and input circuits.

5-16 If W10 is not installed on the card, or if it is and the end-of-flag pulse has been verified, data interface problems in the input card can be isolated using the procedures given in Paragraphs 5-18 and 5-20. Similarly, input card timing and control problems can be isolated using the procedures given in Paragraph 5-23.

5-17 If a defective component is found in the course of troubleshooting be sure to turn off power at the multiprogrammer and remove the input card from the extender before attempting replacement. When installing an IC, be sure that the notch or dot on the IC is at the same end as the bevel on the IC socket.

5-18 ADDRESS GATE TROUBLESHOOTING

5-19 Assuming the gate/flag circuit has been eliminated as a possible cause of data problems (see Paragraph 5-15), if two or more data bits are incorrect (i.e. the data bit outputs of the output gates do not reflect the data input to the receiver circuits), it is likely that the address gate is defective. Troubleshooting procedures for this circuit are given in Table 5-4.

5-20 RECEIVER CIRCUITS, STORAGE REGISTER, AND OUTPUT CIRCUITS TROUBLESHOOTING

5-21 If a single data bit fails (i.e. the data bit output of an output gate does not reflect the data bit input to the receiver circuit), the problem can be in the associated receiver circuit (if supplied), storage circuit, or output gate. The troubleshooting procedures given in Table 5-5 are typical for a data bit channel. Note that two of the standard options (069 and 073) do not utilize an active receiver circuit (only a 1k pull-up resistor is provided for these options) so that the instructions involving the receiver circuit do not apply. The 073 option receiver circuits do, however, include hybrid integrated circuits to convert the open collector logic level inputs to microcircuit levels and, thus, should be checked as directed in the procedures.

Table 5-4. Address Gate Troubleshooting

| TEST NO. | EQUIPMENT CONNECTIONS | INSTRUCTIONS | NORMAL INDICATION | IF INDICATION ABNORMAL | IF INDICATION NORMAL |
|---|---|---|---|---|---|
| 1 | With logic probe monitor Z15-pin 8. | Program a control word; address the unit. Touch LOAD OUTPUT. Address the card slot. | LO level (probe off) | Replace address gate Z15 | Proceed to Test 2 |
| 2 | Connect logic probe to Z10—pin 2. | Do not change programming. | HI level (probe on) | Replace Z10 | Proceed to Test 3 |
| 3 | Connect logic probe to Z10—pin 4. | Do not change programming. | HI level | Replace Z10 | Check connection to CLK inputs of storage register |

Table 5-5. Data Bit Troubleshooting

| TEST NO. | EQUIPMENT CONNECTIONS | INSTRUCTIONS | NORMAL INDICATION | ABNORMAL INDICATION | IF INDICATION NORMAL |
|---|---|---|---|---|---|
| 1 | With logic probe, monitor the storage register IC output associated with the failed bit according to the W11 option connection in place (i.e., either the Q or $\overline{Q}$ output will be monitored). | Perform applicable checkout procedure (Table 5-2, Tests 2 and 3). | Storage register output normal (HI for simulated logical 1; LO for simulated logical 0). | Proceed to Test 2. | Replace associated output gate IC (i.e. replace Z4 if bit 0 was under test). |
| 2 | Connect logic probe to D-input of storage register associated with failed bit. | Repeat checkout procedure. | Storage register input normal (LO for simulated logical 1; HI for simulated logical 0). | Check receiver circuit (replace receiver circuit IC, if applicable). | Replace associated storage register IC. |

Table 5-6. Gate/Flag and Control Circuits Troubleshooting

| TEST NO. | TROUBLE | ISOLATION PROCEDURE | REMEDY |
|---|---|---|---|
| 1 | a. Both $\overline{GATE}$ and $\overline{CTF}$ fail to set ($\overline{GATE}$ goes LO or HI depending on W5 connection. $\overline{CTF}$ goes LO) normally (set until flag received) when card activated (card addressed in ISL mode and data strobe issued). | a. Disable start- and end-of-flag detectors and preset circuit by applying LO inputs to Z9-pin 9 and Z11-pin 4. Monitor Z7-pin 3 with logic probe. Activate input card. (Program control word with ISL on. Touch LOAD OUTPUT. Program card address. Touch LOAD OUTPUT). Logic probe blinks off when LOAD OUTPUT touched. | a. (1) If pulse present, remove LO inputs to Z9 and Z11 and check output of each gate. If either output (but not both) LO, replace associated gate (Z9 or Z11); if both LO, check preset circuit (Q5 collector should be HI). If both reset inputs to gate flip-flop are HI, replace Z13 (gate flip-flop).<br>(2) If pulse absent, monitor Z14-pin 11. Logic probe flashes on when LOAD OUTPUT again touched. If pulse present, check Z14, Z7, R8, and C7; or Z10 (ISL inverter). If pulse absent, check Z10, Z14, R6, C12, and CR2. |
| | b. $\overline{GATE}$ is set normally but $\overline{CTF}$ is not when card activated. | b. Monitor flag flip-flop output Z8-pin 11 with logic probe. Activate input card (see Step 1a). Logic probe on. | b. If flag flip-flop sets, check Z8, Q4, R14, and C14. If flag flip-flop does not set, check Z8, A13, R7, and C8. |
| | c. $\overline{GATE}$ is not set but $\overline{CTF}$ is when card activated. | | c. Check Q3 and R16. |

Table 5-6. Gate/Flag and Control Circuits Troubleshooting (Continued)

| TEST NO. | TROUBLE | ISOLATION PROCEDURE | REMEDY |
|---|---|---|---|
| 2 | $\overline{\text{GATE}}$ not reset at start-of-flag after card activated. | Jumper P2-13 to P2-14. With a logic probe, monitor Z11-pin 11. Activate input card (Step 1a programming); logic probe goes off or on when LOAD OUTPUT touched (probe goes off if W5 connected to A and W7 installed or W5 connected to B and W7 removed; probe goes on if W5 connected to A and W7 out or W5 connected to B and W7 in). | If Z11-pin 11 does not switch to normal level when LOAD OUTPUT touched, check output at Z16-pin 8. If output LO, replace Z16. If output HI, check Z11, R22, R23, Q2, R15, C15, CR4, and A13 input bias resistor(s).<br>If Z11-pin 11 switches to normal level when LOAD OUTPUT touched, check 1μsec delay circuit (R1, R2, and C16) and positive edge detector (Z9, Z11, R3, R11, and C10) or negative edge detector (Z11, R4, R11 and C11) as applicable according to the W1 and W2 jumper connections in use. |
| 3 | a. $\overline{\text{GATE}}$ and $\overline{\text{CTF}}$ not reset at end-of-flag after card activated | a. Activate input card (Step 1a programming). With logic probe, monitor Z11-pin 11. Simulate start-of-flag by switching $\overline{\text{FLAG}}$ input HI or LO as applicable. Simulate end-of-flag by switching $\overline{\text{FLAG}}$ input back to original level. Logic probe flashes on or blinks off depending on W5/W7 connections (see Step 2). | a. If Z11-11 does not indicate as specified when $\overline{\text{FLAG}}$ simulated, check output of Z16-8. If output LO, replace Z16. If output HI, check Z11, R22, R23, Q2, R15, C15, CR4, and A13 input bias resistor(s). If Z-11 output normal when $\overline{\text{FLAG}}$ simulated, check 1μsec delay circuit (R1, R2, C16) and positive edge detector or negative edge detector as applicable. |
| | b. $\overline{\text{GATE}}$ reset but $\overline{\text{CTF}}$ is not at end-of-flag after card activated | b. Activate input card (Step 1a programming). With logic probe, monitor flag flip-flop set output Z8-11. Simulate start- and end-of-flag (see Step 3a). Logic probe goes off at end-of-flag. | b. If flag flip-flop reset, check Z8, R14, C14, and Q4. If flag flip-flop is not reset, replace flag flip-flop Z8. |
| | c. $\overline{\text{GATE}}$ not reset but $\overline{\text{CTF}}$ is at end-of-flag after card activated | | c. Check gate flip-flop Z13 and gate Z16. |
| 4 | $\overline{\text{IRQ}}$ not set (LO) when activated- and ready-card addressed | Activate input card (Step 1a programming). With logic probe, monitor Z12-pin 6. Simulate end-of-flag by momentarily applying LO input to flag flip-flop Z8-pin 10. Address card (DO NOT touch LOAD OUTPUT). | If logic probe goes off after card addressed, check Z14, R17, C13, and Q1.<br>If logic probe stays on after card addressed, check input at Z12-pin 4. If input LO, check control flip-flop Z12, Z7, |

Table 5-6. Gate/Flag and Control Circuits Troubleshooting (Continued)

| TEST NO. | TROUBLE | ISOLATION PROCEDURE | REMEDY |
|---|---|---|---|
| 4 | (Continued) | | and Z10. If input Z12-pin 4 HI, check input to Z12-pin 5. If Z12-pin 5 HI, replace Z12. If Z12-pin 5 LO, replace flag flip-flop Z8. |
| 5 | a. $\overline{IRQ}$ not reset (HI) when activated- and ready-card not addressed | a. Activate input card (Step 1a programming). Simulate end-of-flag by momentarily applying LO input to Z8-pin 10. Monitor Z14-pin 3. Remove card address. Logic probe goes off when address removed. | a. If logic probe goes off, check Q1, R17, C13.<br>If logic probe stays on, check Z14 and Z12. |
| | b. $\overline{IRQ}$ not reset (HI) when activated- but busy-card addressed | | b. Check that flag flip-flop Z8-pin 8 LO when LO applied to Z8-pin 12. |
| | c. $\overline{IRQ}$ not reset (HI) when deactivated- and ready-card addressed | c. Simulate ready card by applying LO to Z8-pin 10. Deactivate card (program control word with ISL off and unit address. Touch LOAD OUTPUT. Program card address. Touch LOAD OUTPUT).<br>With logic probe monitor Z7-pin 6. Logic probe blinks off when LOAD OUTPUT touched. | c. If logic probe blinks off, check control flip-flop Z12 and IEN reset circuit Z9, R26, C17.<br>If logic probe does not blink off, check Z7 and Z10. |
| 6 | $\overline{CTF}$ not set (LO) when IEN issued and card activated and busy | Activate input card (Step 1a programming). Simulate end-of-flag and DST by applying LO inputs to Z8-pin 10 and Z14-pin 12.<br>Program IEN mode (program control word with bit 8 on. Touch LOAD OUTPUT).<br>With logic probe, monitor Z8-pin 6. Logic probe goes on when LOAD OUTPUT touched. | If logic probe goes on, check Q4, R14, C14.<br>If logic probe stays off, check Z8, Z16, and Z10. |
| 7 | $\overline{CTF}$ not reset (HI) when DST removed | Repeat Step 6 procedures. Remove simulated DST LO input to Z14-pin 12, logic probe goes off. | If logic probe goes off, check Q14, R14, C14.<br>If logic probe stays on, check Z8, Z16, Z10. |
| 8 | With W6 installed, $\overline{GATE}$ is not set (LO or HI depending on W5) when IEN programmed and card deactivated and ready | Deenergize and then energize multiprogrammer. With logic probe, monitor control flip-flop set output Z12-pin 8. | If control flip-flop set, replace Z16. |

Table 5-6. Gate/Flag and Control Circuits Troubleshooting (Continued)

| TEST NO. | TROUBLE | ISOLATION PROCEDURE | REMEDY |
|---|---|---|---|
| 8 | (Continued) | Program IEN mode (see Step 6). Logic probe goes on when LOAD OUTPUT touched. | If control flip-flop reset, check Z9, R5, C9. |
| 9 | With W6 installed $\overline{\text{GATE}}$ is set when IEN programmed and card already activated. | | Check Z16. |
| 10 | With W6 installed $\overline{\text{GATE}}$ and control flip-flop not set when IEN programmed and card ready but deactive. | | Check control flip-flop set circuit Z9, R26, C17. |

## 5-22 GATE/FLAG AND CONTROL CIRCUITS TROUBLESHOOTING

5-23 A failure in the gate/flag or control circuits can affect the $\overline{\text{GATE}}$ output to the external device and/or the $\overline{\text{CTF}}$ and $\overline{\text{IRQ}}$ signals returned to the multiprogrammer. In addition, if W10 is installed, the gate/flag circuits also affect the data interface function of the input card (e.g. if $\overline{\text{FLT}}$ is not produced, data cannot be strobed into the data storage register). Since these circuits are interrelated and produce the above outputs ($\overline{\text{GATE}}$, $\overline{\text{CTF}}$, $\overline{\text{IRQ}}$, and end-of-flag data clock) under various modes of operation, it is important in troubleshooting the circuits that a determination be made of the exact modes of operation that are defective. The check-output procedure given in Table 5-5 can be used to gather symptoms after which the troubleshooting procedures given in Table 5-6 (which are organized according to various combinations of symptoms that can occur) can be used to isolate the malfunction. Notice that some symptoms given in Table 5-6 may not be applicable in that the input card option jumpers may be connected to disable the function (i.e. jumpers W1 and W2 can be connected to cause the $\overline{\text{GATE}}$ output to be reset only at the end-of-flag transition and not at the start-of-flag). Notice, further, that the troubleshooting procedures provided in Table 5-6 form a unified sequence; that is, the procedures used to isolate faults that produce particular symptoms assume that the symptoms isolated in preceding tests are not present (i.e. Test 2 assumes that the $\overline{\text{GATE}}$ output can be set when the input card is selectively activated).

# SECTION VI
# REPLACEABLE PARTS

## 6-1 INTRODUCTION

6-2 This section contains information for ordering replacement parts. Table 6-4 lists parts in alphanumeric order by reference designators and provides the following information:

a. Reference Designators. Refer to Table 6-1.

b. Description. Refer to Table 6-2 for abbreviations.

c. Total Quantity (TQ). Given only the first time the part number is listed except in instruments containing many sub-modular assemblies, in which case the TQ appears the first time the part number is listed in each assembly.

d. Manufacturer's Part Number or Type.

e. Manufacturer's Federal Supply Code Number. Refer to Table 6-3 for manufacturer's name and address.

f. Hewlett-Packard Part Number.

g. Recommended Spare Parts Quantity (RS) for complete maintenance of one instrument during one year of isolated service.

h. Parts not identified by a reference designator are listed at the end of Table 6-4 under Mechanical and/or Miscellaneous. The former consists of parts belonging to and grouped by individual assemblies; the latter consists of all parts not immediately associated with an assembly.

## 6-3 ORDERING INFORMATION

6-4 To order a replacement part, address order or inquiry to your local Hewlett-Packard sales office (see lists at rear of this manual for addresses). Specify the following information for each part: Model, complete serial number, and any Option or special modification (J) numbers of the instrument; Hewlett-Packard part number; circuit reference designator; and description. To order a part not listed in Table 6-4, give a complete description of the part, its function, and its location.

Table 6-1. Reference Designators

| | | | |
|---|---|---|---|
| A | = assembly | E | = miscellaneous electronic part |
| B | = blower (fan) | F | = fuse |
| C | = capacitor | J | = jack, jumper |
| CB | = circuit breaker | K | = relay |
| CR | = diode | L | = inductor |
| DS | = device, signaling (lamp) | M | = meter |

Table 6-1. Reference Designators (Continued)

| | | | |
|---|---|---|---|
| P | = plug | V | = vacuum tube, neon bulb, photocell, etc. |
| Q | = transistor | VR | = zener diode |
| R | = resistor | X | = socket |
| S | = switch | Z | = integrated circuit or network |
| T | = transformer | | |
| TB | = terminal block | | |
| TS | = thermal switch | | |

Table 6-2. Description Abbreviations

| | | | |
|---|---|---|---|
| A | = ampere | mfr | = manufacturer |
| ac | = alternating current | mod. | = modular or modified |
| assy. | = assembly | mtg | = mounting |
| bd | = board | n | = nano = $10^{-9}$ |
| bkt | = bracket | NC | = normally closed |
| °C | = degree Centigrade | NO | = normally open |
| | | NP | = nickel-plated |
| cd | = card | Ω | = ohm |
| coef | = coefficient | obd | = order by description |
| comp | = composition | | |
| CRT | = cathode-ray tube | OD | = outside diameter |
| CT | = center-tapped | p | = pico = $10^{-12}$ |
| dc | = direct current | P.C. | = printed circuit |
| DPDT | = double pole, double throw | pot. | = potentiometer |
| | | p-p | = peak-to-peak |
| DPST | = double pole, single throw | ppm | = parts per million |
| elect | = electrolytic | pvr | = peak reverse voltage |
| encap | = encapsulated | rect | = rectifier |
| F | = farad | rms | = root mean square |
| °F | = degree Farenheit | Si | = silicon |
| | | SPDT | = single pole, double throw |
| fxd | = fixed | | |
| Ge | = germanium | SPST | = single pole, single throw |
| H | = Henry | | |
| Hz | = Hertz | SS | = small signal |
| IC | = integrated circuit | T | = slow-blow |
| | | tan. | = tantulum |
| ID | = inside diameter | Ti | = titanium |
| incnd | = incandescent | V | = volt |
| k | = kilo = $10^{3}$ | var | = variable |
| m | = milli = $10^{-3}$ | ww | = wirewound |
| M | = mega = $10^{6}$ | W | = Watt |
| μ | = micro = $10^{-6}$ | | |
| met. | = metal | | |

Table 6-3. Code List of Manufacturers

| CODE NO. | MANUFACTURER | ADDRESS |
|---|---|---|
| 00629 | EBY Sales Co., Inc. | Jamaica, N.Y. |
| 00656 | Aerovox Corp. | New Bedford, Mass. |
| 00853 | Sangamo Electric Co. S. Carolina Div. | Pickens, S.C. |
| 01121 | Allen Bradley Co. | Milwaukee, Wis. |
| 01255 | Litton Industries, Inc. | Beverly Hills, Calif. |
| 01281 | TRW Semiconductors, Inc. | Lawndale, Calif. |
| 01295 | Texas Instruments, Inc. Semiconductor-Components Div. | Dallas, Texas |
| 01686 | RCL Electronics, Inc. | Manchester, N.H. |
| 01930 | Amerock Corp. | Rockford, Ill. |
| 02107 | Sparta Mfg. Co. | Dover, Ohio |
| 02114 | Ferroxcube Corp. | Saugerties, N.Y. |
| 02606 | Fenwal Laboratories | Morton Grove, Ill. |
| 02660 | Amphenol Corp. | Broadview, Ill. |
| 02735 | Radio Corp. of America, Solid State and Receiving Tube Div. | Somerville, N.J. |
| 03508 | G.E. Semiconductor Products Dept. | Syracuse, N.Y. |
| 03797 | Eldema Corp. | Compton, Calif. |
| 03877 | Transitron Electronic Corp. | Wakefield, Mass. |
| 03888 | Pyrofilm Resistor Co. Inc. | Cedar Knolls, N.J. |
| 04009 | Arrow, Hart and Hegeman Electric Co. | Hartford, Conn. |
| 04072 | ADC Electronics, Inc. | Harbor City, Calif. |
| 04213 | Caddell & Burns Mfg. Co. Inc. | Mineola, N.Y. |
| 04404 | *Hewlett-Packard Co. Palo Alto Div. | Palo Alto, Calif. |
| 04713 | Motorola Semiconductor Prod. Inc. | Phoenix, Arizona |
| 05277 | Westinghouse Electric Corp. Semiconductor Dept. | Youngwood, Pa. |
| 05347 | Ultronix, Inc. | Grand Junction, Colo. |
| 05820 | Wakefield Engr. Inc. | Wakefield, Mass. |
| 06001 | General Elect. Co. Electronic Capacitor & Battery Dept. | Irmo, S.C. |
| 06004 | Bassik Div. Stewart-Warner Corp. | Bridgeport, Conn. |
| 06486 | IRC Div. of TRW Inc. Semiconductor Plant | Lynn, Mass. |
| 06540 | Amatom Electronic Hardware Co. Inc. | New Rochelle, N.Y. |
| 06555 | Beede Electrical Instrument Co. | Penacook, N.H. |
| 06666 | General Devices Co. Inc. | Indianapolis, Ind. |
| 06751 | Semcor Div. Components, Inc. | Phoenix, Arizona |
| 06776 | Robinson Nugent, Inc. | New Albany, Ind. |
| 06812 | Torrington Mfg. Co., West Div. | Van Nuys, Calif. |
| 07137 | Transistor Electronics Corp. | Minneapolis, Minn. |
| 07138 | Westinghouse Electric Corp. Electronic Tube Div. | Elmira, N.Y. |
| 07263 | Fairchild Camera and Instrument Corp. Semiconductor Div. | Mountain View, Calif. |
| 07387 | Birtcher Corp., The | Los Angeles, Calif. |
| 07397 | Sylvania Electric Prod. Inc. Sylvania Electronic Systems Western Div. | Mountain View, Calif. |
| 07716 | IRC Div. of TRW Inc. Burlington Plant | Burlington, Iowa |
| 07910 | Continental Device Corp. | Hawthorne, Calif. |
| 07933 | Raytheon Co. Components Div. Semiconductor Operation | Mountain View, Calif. |
| 08484 | Breeze Corporations, Inc. | Union, N.J. |
| 08530 | Reliance Mica Corp. | Brooklyn, N.Y. |
| 08717 | Sloan Company, The | Sun Valley, Calif. |
| 08730 | Vemaline Products Co. Inc. | Wyckoff, N.J. |
| 08806 | General Elect. Co. Miniature Lamp Dept. | Cleveland, Ohio |
| 08863 | Nylomatic Corp. | Norrisville, Pa. |
| 08919 | RCH Supply Co. | Vernon, Calif. |
| 09021 | Airco Speer Electronic Components | Bradford, Pa. |
| 09182 | *Hewlett-Packard Co. New Jersey Div. | Rockaway, N.J. |
| 09213 | General Elect. Co. Semiconductor Prod. Dept. | Buffalo, N.Y. |
| 09214 | General Elect. Co. Semiconductor Prod. Dept. | Auburn, N.Y. |
| 09353 | C & K Components Inc. | Newton, Mass. |
| 09922 | Burndy Corp. | Norwalk, Conn. |
| 11115 | Wagner Electric Corp. Tung-Sol Div. | Bloomfield, N.J. |
| 11236 | CTS of Berne, Inc. | Berne, Ind. |
| 11237 | Chicago Telephone of Cal. Inc. | So. Pasadena, Calif. |
| 11502 | IRC Div. of TRW Inc. Boone Plant | Boone, N.C. |
| 11711 | General Instrument Corp Rectifier Div. | Newark, N.J. |
| 12136 | Philadelphia Handle Co. Inc. | Camden, N.J. |
| 12615 | U.S. Terminals, Inc. | Cincinnati, Ohio |
| 12617 | Hamlin Inc. | Lake Mills, Wisconsin |
| 12697 | Clarostat Mfg. Co. Inc. | Dover, N.H. |
| 13103 | Thermalloy Co. | Dallas, Texas |
| 14493 | *Hewlett-Packard Co. Loveland Div. | Loveland, Colo. |
| 14655 | Cornell-Dubilier Electronics Div. Federal Pacific Electric Co. | Newark, N.J. |
| 14936 | General Instrument Corp. Semiconductor Prod. Group | Hicksville, N.Y. |
| 15801 | Fenwal Elect. | Framingham, Mass. |
| 16299 | Corning Glass Works, Electronic Components Div. | Raleigh, N.C. |

*Use Code 28480 assigned to Hewlett-Packard Co., Palo Alto, California

Table 6-3. Code List of Manufacturers (Continued)

| CODE NO. | MANUFACTURER | ADDRESS |
|---|---|---|
| 16758 | Delco Radio Div. of General Motors Corp. | Kokomo, Ind. |
| 17545 | Atlantic Semiconductors, Inc. | Asbury Park, N.J. |
| 17803 | Fairchild Camera and Instrument Corp Semiconductor Div. Transducer Plant | Mountain View, Calif. |
| 17870 | Daven Div. Thomas A. Edison Industries McGraw-Edison Co. | Orange, N.J. |
| 18324 | Signetics Corp. | Sunnyvale, Calif. |
| 19315 | Bendix Corp. The Navigation and Control Div. | Teterboro, N.J. |
| 19701 | Electra/Midland Corp. | Mineral Wells, Texas |
| 21520 | Fansteel Metallurgical Corp. | No. Chicago, Ill. |
| 22229 | Union Carbide Corp. Electronics Div. | Mountain View, Calif. |
| 22753 | UID Electronics Corp. | Hollywood, Fla. |
| 23936 | Pamotor, Inc. | Pampa, Texas |
| 24446 | General Electric Co. | Schenectady, N.Y. |
| 24455 | General Electric Co. Lamp Div. of Consumer Prod. Group | Nela Park, Cleveland, Ohio |
| 24655 | General Radio Co. | West Concord, Mass. |
| 24681 | LTV Electrosystems Inc Memcor/Components Operations | Huntington, Ind. |
| 26982 | Dynacool Mfg. Co. Inc. | Saugerties, N.Y. |
| 27014 | National Semiconductor Corp. | Santa Clara, Calif. |
| 28480 | Hewlett-Packard Co. | Palo Alto, Calif. |
| 28520 | Heyman Mfg. Co. | Kenilworth, N.J. |
| 28875 | IMC Magnetics Corp. New Hampshire Div. | Rochester, N.H. |
| 31514 | SAE Advance Packaging, Inc. | Santa Ana, Calif. |
| 31827 | Budwig Mfg. Co. | Ramona, Calif. |
| 33173 | G.E. Co. Tube Dept. | Owensboro, Ky. |
| 35434 | Lectrohm, Inc. | Chicago, Ill. |
| 37942 | P.R. Mallory & Co. Inc. | Indianapolis, Ind. |
| 42190 | Muter Co. | Chicago, Ill. |
| 43334 | New Departure-Hyatt Bearings Div. General Motors Corp. | Sandusky, Ohio |
| 44655 | Ohmite Manufacturing Co. | Skokie, Ill. |
| 46384 | Penn Engr. and Mfg. Corp. | Doylestown, Pa. |
| 47904 | Polaroid Corp. | Cambridge, Mass. |
| 49956 | Raytheon Co. | Lexington, Mass. |
| 55026 | Simpson Electric Co. Div. of American Gage and Machine Co. | Chicago, Ill. |
| 56289 | Sprague Electric Co. | North Adams, Mass. |
| 58474 | Superior Electric Co. | Bristol, Conn. |
| 58849 | Syntron Div. of FMC Corp. | Homer City, Pa. |
| 59730 | Thomas and Betts Co. | Philadelphia, Pa. |
| 61637 | Union Carbide Corp. | New York, N.Y. |
| 63743 | Ward Leonard Electric Co. | Mt. Vernon, N.Y. |

| CODE NO. | MANUFACTURER | ADDRESS |
|---|---|---|
| 70563 | Amperite Co. Inc. | Union City, N.J. |
| 70901 | Beemer Engrg. Co. | Fort Washington, Pa. |
| 70903 | Belden Corp. | Chicago, Ill. |
| 71218 | Bud Radio, Inc. | Willoughby, Ohio |
| 71279 | Cambridge Thermionic Corp. | Cambridge, Mass. |
| 71400 | Bussmann Mfg. Div. of McGraw & Edison Co. | St. Louis, Mo. |
| 71450 | CTS Corp. | Elkhart, Ind. |
| 71468 | I.T.T. Cannon Electric Inc. | Los Angeles, Calif. |
| 71590 | Globe-Union Inc. Centralab Div. | Milwaukee, Wis. |
| 71700 | General Cable Corp. Cornish Wire Co. Div. | Williamstown, Mass. |
| 71707 | Coto Coil Co. Inc. | Providence, R.I. |
| 71744 | Chicago Miniature Lamp Works | Chicago, Ill. |
| 71785 | Cinch Mfg. Co. and Howard B. Jones Div. | Chicago, Ill. |
| 71984 | Dow Corning Corp. | Midland, Mich. |
| 72136 | Electro Motive Mfg. Co. Inc. | Willimantic, Conn. |
| 72619 | Dialight Corp. | Brooklyn, N.Y. |
| 72699 | General Instrument Corp. | Newark, N.J. |
| 72765 | Drake Mfg. Co. | Harwood Heights, Ill. |
| 72962 | Elastic Stop Nut Div. of Amerace Esna Corp. | Union, N.J. |
| 72982 | Erie Technological Products Inc. | Erie, Pa. |
| 73096 | Hart Mfg. Co. | Hartford, Conn. |
| 73138 | Beckman Instruments Inc. Helipot Div. | Fullerton, Calif. |
| 73168 | Fenwal, Inc. | Ashland, Mass. |
| 73293 | Hughes Aircraft Co. Electron Dynamics Div. | Torrance, Calif. |
| 73445 | Amperex Electronic Corp. | Hicksville, N.Y. |
| 73506 | Bradley Semiconductor Corp. | New Haven, Conn. |
| 73559 | Carling Electric, Inc. | Hartford, Conn. |
| 73734 | Federal Screw Products, Inc. | Chicago, Ill. |
| 74193 | Heinemann Electric Co. | Trenton, N.J. |
| 74545 | Hubbell Harvey Inc. | Bridgeport, Conn. |
| 74868 | Amphenol Corp. Amphenol RF Div. | Danbury, Conn. |
| 74970 | E.F. Johnson Co. | Waseca, Minn. |
| 75042 | IRC Div. of TRW, Inc. | Philadelphia, Pa. |
| 75183 | *Howard B. Jones Div. of Cinch Mfg. Corp. | New York, N.Y. |
| 75376 | Kurz and Kasch, Inc. | Dayton, Ohio |
| 75382 | Kilka Electric Corp. | Mt. Vernon, N.Y. |
| 75915 | Littlefuse, Inc. | Des Plaines, Ill. |
| 76381 | Minnesota Mining and Mfg. Co. | St. Paul, Minn. |
| 76385 | Minor Rubber Co. Inc. | Bloomfield, N.J. |
| 76487 | James Millen Mfg. Co. Inc. | Malden, Mass. |
| 76493 | J.W. Miller Co. | Compton, Calif. |

*Use Code 71785 assigned to Cinch Mfg. Co., Chicago, Ill.

Table 6-3. Code List of Manufacturers (Continued)

| CODE NO. | MANUFACTURER | ADDRESS |
|---|---|---|
| 76530 | Cinch | City of Industry, Calif. |
| 76854 | Oak Mfg. Co. Div. of Oak Electro/Netics Corp. | Crystal Lake, Ill. |
| 77068 | Bendix Corp., Electrodynamics Div. | No. Hollywood, Calif. |
| 77122 | Palnut Co. | Mountainside, N.J. |
| 77147 | Patton-MacGuyer Co. | Providence, R.I. |
| 77221 | Phaostron Instrument and Electronic Co. | South Pasadena, Calif. |
| 77252 | Philadelphia Steel and Wire Corp. | Philadelphia, Pa. |
| 77342 | American Machine and Foundry Co. Potter and Brumfield Div. | Princeton, Ind. |
| 77630 | TRW Electronic Components Div. | Camden, N.J. |
| 77764 | Resistance Products Co. | Harrisburg, Pa. |
| 78189 | Illinois Tool Works Inc. Shakeproof Div. | Elgin, Ill. |
| 78452 | Everlock Chicago, Inc. | Chicago, Ill. |
| 78488 | Stackpole Carbon Co. | St. Marys, Pa. |
| 78526 | Stanwyck Winding Div. San Fernando Electric Mfg. Co. Inc. | Newburgh, N.Y. |
| 78553 | Tinnerman Products, Inc. | Cleveland, Ohio |
| 78584 | Stewart Stamping Corp. | Yonkers, N.Y. |
| 79136 | Waldes Kohinoor, Inc. | L.I.C., N.Y. |
| 79307 | Whitehead Metals Inc. | New York, N.Y. |
| 79727 | Continental-Wirt Electronics Corp. | Philadelphia, Pa. |
| 79963 | Zierick Mfg. Co. | Mt. Kisco, N.Y. |
| 80031 | Mepco Div. of Sessions Clock Co. | Morristown, N.J. |
| 80294 | Bourns, Inc. | Riverside, Calif. |
| 81042 | Howard Industries Div. of Msl Ind. Inc. | Racine, Wisc. |
| 81073 | Grayhill, Inc. | La Grange, Ill. |
| 81483 | International Rectifier Corp. | El Segundo, Calif. |
| 81751 | Columbus Electronics Corp. | Yonkers, N.Y. |
| 82099 | Goodyear Sundries & Mechanical Co. Inc. | New York, N.Y. |
| 82142 | Airco Speer Electronic Components | Du Bois, Pa. |
| 82219 | Sylvania Electric Products Inc. Electronic Tube Div. Receiving Tube Operations | Emporium, Pa. |
| 82389 | Switchcraft, Inc. | Chicago, Ill. |
| 82647 | Metals and Controls Inc. Control Products Group | Attleboro, Mass. |
| 82866 | Research Products Corp. | Madison, Wis. |
| 82877 | Rotron Inc. | Woodstock, N.Y. |
| 82893 | Vector Electronic Co. | Glendale, Calif. |
| 83058 | Carr Fastener Co. | Cambridge, Mass. |
| 83186 | Victory Engineering Corp. | Springfield, N.J. |
| 83298 | Bendix Corp. Electric Power Div. | Eatontown, N.J. |
| 83330 | Herman H. Smith, Inc. | Brooklyn, N.Y. |
| 83385 | Central Screw Co. | Chicago, Ill. |
| 83501 | Gavitt Wire and Cable Div. of Amerace Esna Corp. | Brookfield, Mass. |
| 83508 | Grant Pulley and Hardware Co. | West Nyack, N.Y. |
| 83594 | Burroughs Corp. Electronic Components Div. | Plainfield, N.J. |
| 83835 | U.S. Radium Corp. | Morristown, N.J. |
| 83877 | Yardeny Laboratories, Inc. | New York, N.Y. |
| 84171 | Arco Electronics, Inc. | Great Neck, N.Y. |
| 84411 | TRW Capacitor Div. | Ogallala, Neb. |
| 86684 | RCA Corp. Electronic Components | Harrison, N.J. |
| 86838 | Rummel Fibre Co. | Newark, N.J. |
| 87034 | Marco & Oak Industries a Div. of Oak Electro/netics Corp. | Anaheim, Calif. |
| 87216 | Philco Corp. Lansdale Div. | Lansdale, Pa. |
| 87585 | Stockwell Rubber Co. Inc. | Philadelphia, Pa. |
| 87929 | Tower-Olschan Corp. | Bridgeport, Conn. |
| 88140 | Cutler-Hammer Inc. Power Distribution and Control Div. Lincoln Plant | Lincoln, Ill. |
| 88245 | Litton Precision Products Inc, USECO Div. Litton Industries | Van Nuys, Calif. |
| 90634 | Gulton Industries Inc. | Metuchen, N.J. |
| 90763 | United-Car Inc. | Chicago, Ill. |
| 91345 | Miller Dial and Nameplate Co. | El Monte, Calif. |
| 91418 | Radio Materials Co. | Chicago, Ill. |
| 91506 | Augat, Inc. | Attleboro, Mass. |
| 91637 | Dale Electronics, Inc. | Columbus, Neb. |
| 91662 | Elco Corp. | Willow Grove, Pa. |
| 91929 | Honeywell Inc. Div. Micro Switch | Freeport, Ill. |
| 92825 | Whitso, Inc. | Schiller Pk., Ill. |
| 93332 | Sylvania Electric Prod. Inc. Semiconductor Prod. Div. | Woburn, Mass. |
| 93410 | Essex Wire Corp. Stemco Controls Div. | Mansfield, Ohio |
| 94144 | Raytheon Co. Components Div. Ind. Components Oper. | Quincy, Mass. |
| 94154 | Wagner Electric Corp. Tung-Sol Div. | Livingston, N.J. |
| 94222 | Southco Inc. | Lester, Pa. |
| 95263 | Leecraft Mfg. Co. Inc. | L.I.C., N.Y. |
| 95354 | Methode Mfg. Co. | Rolling Meadows, Ill. |
| 95712 | Bendix Corp. Microwave Devices Div. | Franklin, Ind. |
| 95987 | Weckesser Co. Inc. | Chicago, Ill. |
| 96791 | Amphenol Corp. Amphenol Controls Div. | Janesville, Wis. |
| 97464 | Industrial Retaining Ring Co. | Irvington, N.J. |
| 97702 | IMC Magnetics Corp. Eastern Div. | Westbury, N.Y. |
| 98291 | Sealectro Corp. | Mamaroneck, N.Y. |
| 98410 | ETC Inc. | Cleveland, Ohio |
| 98978 | International Electronic Research Corp. | Burbank, Calif. |
| 99934 | Renbrandt, Inc. | Boston, Mass. |

Table 6-4. Replaceable Parts

| REF. DESIG. | DESCRIPTION | TQ | MFR. PART NO. | MFR. CODE | HP PART NO. | RS |
|---|---|---|---|---|---|---|
| 69431A-A4 | Digital Input Card | | | | | |
| | STANDARD COMPONENTS (All Options) | | | | | |
| A4C1-5 | fxd, elect. 1.0μF 35Vdc | 6 | 150D105X9035A2 | 56289 | 0180-0291 | 2 |
| C6 | fxd, elect. 0.47μF 35Vdc | 1 | 150D474X9035A2 | 56289 | 0180-0376 | 1 |
| C7-11 | fxd, mylar 0.0022μF 200Vdc | 6 | 192P22292 | 56289 | 0160-0154 | 2 |
| C12 | fxd, mylar 0.0047μF 200Vdc | 1 | 192P47292 | 56289 | 0160-0157 | 1 |
| C13,14 | fxd, mylar 0.001μF 200Vdc | 2 | 192P10292 | 56289 | 0160-0153 | 1 |
| C16 | fxd, mylar 0.01μF 200Vdc | 1 | 192P10392 | 56289 | 0160-0161 | 1 |
| C17 | fxd, mylar 0.0022μF 200Vdc | | 192P22292 | 56289 | 0160-0154 | |
| C19 | fxd, elect. 1.0μF 35Vdc | | 150D105X9035A2 | 56289 | 0180-0291 | |
| CR1,2 | Diode, Si. 250mW 200V | 2 | | 28480 | 1901-0033 | 2 |
| CR3 | Diode, Si. 250mA 75V | 1 | | 28480 | 1901-0050 | 1 |
| Q1,3-5 | SS NPN Si. | 5 | | 28480 | 1854-0071 | 5 |
| Q6 | SS PNP Si. | 1 | | 28480 | 1853-0099 | 1 |
| Q7 | SS NPN Si. | | | 28480 | 1854-0071 | |
| Q8 | SS NPN Si. | 1 | | 28480 | 1854-0271 | 1 |
| R1,2 | fxd, comp 100Ω ±5% ¼W | 2 | CB-1015 | 01121 | 0683-1015 | 1 |
| R3-8 | fxd, comp 200Ω ±5% ¼W | 7 | CB-2015 | 01121 | 0683-2015 | 2 |
| R9,11-13 | fxd, comp 1kΩ ±5% ¼W | 6 | CB-1025 | 01121 | 0683-1025 | 2 |
| R14 | fxd, comp 3kΩ ±5% ¼W | 3 | CB-3025 | 01121 | 0683-3025 | 1 |
| R16 | fxd, comp 2kΩ ±5% ¼W | 1 | CB-2025 | 01121 | 0683-2025 | 1 |
| R17 | fxd, comp 3kΩ ±5% ¼W | | CB-3025 | 01121 | 0683-3025 | |
| R18 | fxd, comp 20kΩ ±5% ¼W | 1 | CB-2035 | 01121 | 0683-2035 | 1 |
| R19-21 | fxd, comp 100kΩ ±5% ¼W | 3 | CB-1045 | 01121 | 0683-1045 | 1 |
| R22 | fxd, met. film 316Ω ±1% 1/8W | 1 | Type CEA T-0 | 07716 | 0698-3444 | 1 |
| R23 | fxd, met. film 750Ω ±1% 1/8W | 1 | Type CEA T-0 | 07716 | 0757-0420 | 1 |
| R24 | fxd, comp 3kΩ ±5% ¼W | | CB-3025 | 01121 | 0683-3025 | |
| R25 | fxd, comp 1kΩ ±5% ¼W | | CB-1025 | 01121 | 0683-1025 | |
| R26 | fxd, comp 200Ω ±5% ¼W | | CB-2015 | 01121 | 0683-2015 | |
| R27 | fxd, comp 1kΩ ±5% ¼W | | CB-1025 | 01121 | 0683-1025 | |
| R28 | fxd, comp 27Ω ±5% ½W | 1 | EB-2705 | 01121 | 0686-2705 | 1 |
| Z1-3 | Low Power, Quad 4-Bit Bistable Latch | 3 | SN74L75N | 01295 | 1820-0876 | 3 |
| Z4-6 | Quad 2-Input NAND buffer, open collector | 3 | SN7438N | 01295 | 1820-0621 | 3 |
| Z7-9 | Quad 2-Input NAND gate, IC | 5 | SN7400N | 01295 | 1820-0054 | 5 |
| Z10 | Hex Inverter, IC | 1 | SN7404N | 01295 | 1820-0174 | 1 |
| Z11 | Quad 2-Input NAND gate, IC | | SN7400N | 01295 | 1820-0054 | |
| Z12,13 | Triple 3-Input positive NAND gate | 2 | SN7410N | 01295 | 1820-0068 | 2 |
| Z14 | Quad 2-Input NAND gate, IC | | SN7400N | 01295 | 1820-0054 | |
| Z15 | 8-Input NAND gate, IC | 1 | SN7430N | 01295 | 1820-0070 | 1 |
| Z16 | Dual 4-Input NAND gate, IC | 1 | SN7420N | 01295 | 1820-0069 | 1 |
| | MECHANICAL (All Options) | | | | | |
| | IC Socket, Z1-3 | 3 | 316-AG5D-3R | 91506 | 1200-0767 | 3 |
| | IC Socket, Z4-16 | 13 | 314-AG5D-3R | 91506 | 1200-0768 | 7 |
| | Heat Dissipator, Q8 | 1 | 2227-B | 13103 | 1205-0206 | 1 |
| | Extractor Handle, with Roll Pin | 1 | 6100 | 31514 | 0403-0180 | |
| | Connector Assembly, Output | 1 | | 28480 | 5060-7934 | 1 |
| | Connector, 30-pin | 1 | 251-15-30-261 | 71785 | 1251-0159 | 1 |

| REF. DESIG. | DESCRIPTION | TQ | MFR. PART NO. | MFR. CODE | HP PART NO. | RS |
|---|---|---|---|---|---|---|
| | Hood, Connector | 1 | | 28480 | 5040-0051 | |
| | Clamp, Cable | 1 | | 28480 | 0562A-12B | |
| | Screw, Pan Head 4-40 x 3/8 | 1 | | 28480 | 2200-0143 | |
| | Box Corrugated | 1 | | 28480 | 9211-0418 | |
| | OPTION 069 ONLY | | | | | |
| 69431A-A4 | Digital Input Card | 1 | | 28480 | 69431-60021 | |
| | Data Bit and Flag Receiver Circuits | | | | | |
| A4A1R1 | fxd, comp 1kΩ ±5% ½W | 1 | EB-1025 | 01121 | 0686-1025 | 1 |
| A4A2-A4A13 | Same as A4A1 | 12 | | | | |
| | OPTION 070 ONLY | | | | | |
| 69431A-A4 | Digital Input Card | 1 | | 28480 | 69431-60022 | |
| | Data Bit Receiver Circuits | | | | | |
| A4Z17-Z19 | Quadruple Hybrid Integrated Circuit | 3 | | 28480 | | 3 |
| A4A1R1 | fxd, comp 1kΩ ±5% ½W | 1 | EB-1025 | 01121 | 0686-1025 | 1 |
| R2 | fxd, comp 2kΩ ±5% ½W | 1 | EB-2025 | 01121 | 0686-2025 | 1 |
| R3 | fxd, comp 10kΩ ±5% ½W | 1 | EB-1035 | 01121 | 0686-1035 | 1 |
| A4A2-A4A13 | Same as A4A1 | 12 | | | | |
| | Flag Receiver Circuit | | | | | |
| A4C18 | fxd, mica 120pF ±5% 300Vdc | 1 | RDM15F121J3C | 00853 | 0160-2205 | 1 |
| CR4 | Diode, Si. 250mW 200V | 1 | | 28480 | 1901-0033 | 1 |
| Q2 | SS NPN Si. | 1 | | 28480 | 1854-0071 | 1 |
| R15 | fxd, comp 2kΩ ±5% ½W | 1 | EB-2025 | 01121 | 0686-2025 | 1 |
| | OPTION 073 ONLY | | | | | |
| 69431A-A4 | Digital Input Card | 1 | | 28480 | 69431-60023 | |
| | Data Bit and Flag Receiver Circuits | | | | | |
| A4A1R1 | fxd, comp 1kΩ ±5% ½W | 1 | EB-1025 | 01121 | 0686-1025 | 1 |
| A4A2-A4A13 | Same as A4A1 | 12 | | | | |

# SECTION VII
# CIRCUIT DIAGRAMS

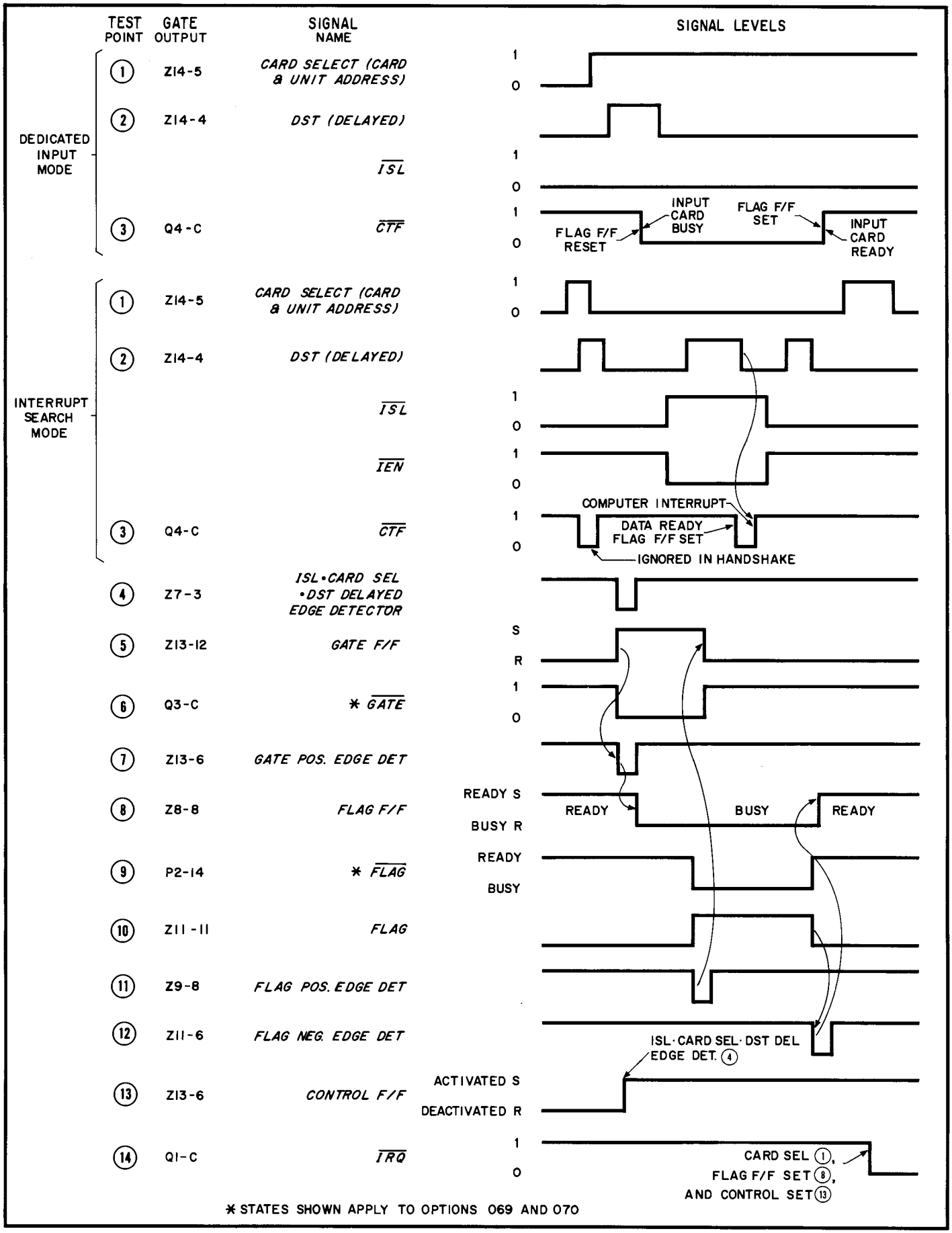
## 7-1 COMPONENT LOCATION ILLUSTRATION

7-2 The component location illustration for the Model 69341A is given in Figure 7-1, Sheet 1. The illustration shows the physical location and reference designations for parts mounted on the printed circuit card.

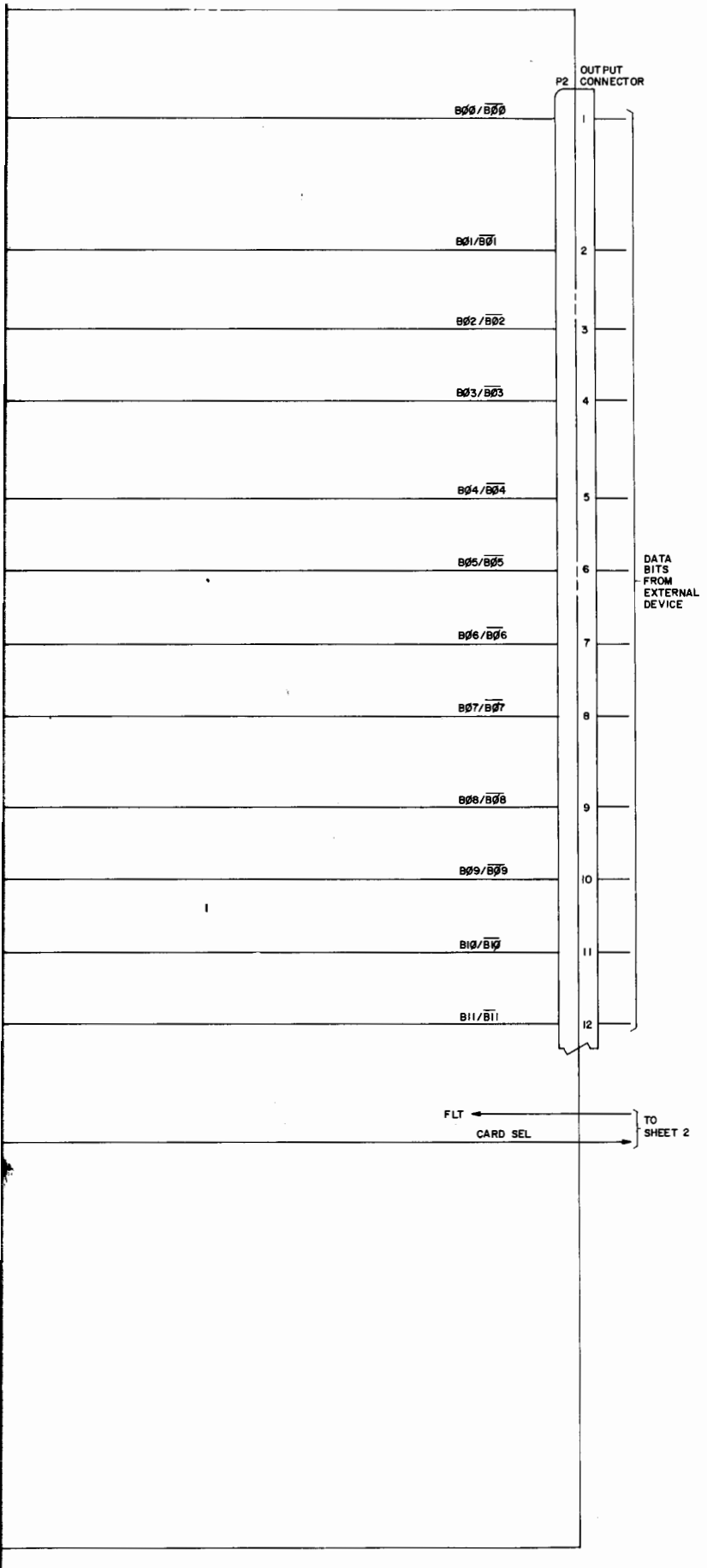
## 7-3 SCHEMATIC DIAGRAM

7-4 The schematic diagram of the Model 69341A is also presented on Figure 7-1, Sheets 1 and 2. The test points (encircled numbers) shown on the schematic diagrams coincide with test points on the component location illustration.

## GATE / FLAG CIRCUIT WAVEFORMS




* STATES SHOWN APPLY TO OPTIONS 069 AND 070

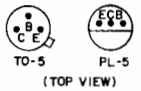



NOTES:

1. ALL 1/2W RESISTORS ARE ±5%, UNLESS OTHERWISE INDICATED, ALL 1/8W RESISTORS ARE ±1%, UNLESS OTHERWISE INDICATED, ALL 1/4W RESISTORS ARE ±5%, UNLESS OTHERWISE INDICATED.
2. ALL CAPACITORS IN MICROFARADS, UNLESS OTHERWISE INDICATED.
3. JUMPER CONNECTIONS SHOWN ARE FOR OPTION 069. SEE TABLE BELOW (AND SECTION III) FOR 070 AND 073 OPTION JUMPER CONNECTIONS.

| OPTION | AI THRU AI3 | | | Q2, CR4 C18, RI5 | WI | W2 | W3 | W4 | W5 | W6 | W7 | W8 | W9 | WIO | WII |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RI | R2 | R3 | | | | | | | | | | | | |
| 069 | IK | - | - | - | A | B | A | IN | A | IN | IN | C | OUT | IN | A |
| 070 | IK | 2K | IOK | SUPPLIED | B | A | B | OUT | A | IN | OUT | A | B | IN | B |
| 073 | IK | - | - | - | A | B | A | IN | A | IN | IN | C | OUT | IN | B |

4. DATA BIT AND FLAG RECEIVER CIRCUITS SHOWN FOR 070 OPTION. ONLY RI(IK) SUPPLIED FOR 069 AND 073 OPTIONS. SEE TABLE ABOVE.
5. PIN LOCATIONS FOR TRANSISTORS ARE AS FOLLOWS:




6. PIN LOCATIONS FOR INTEGRATED CIRCUIT ARE AS FOLLOWS:

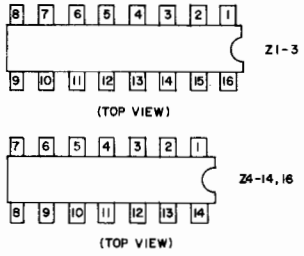
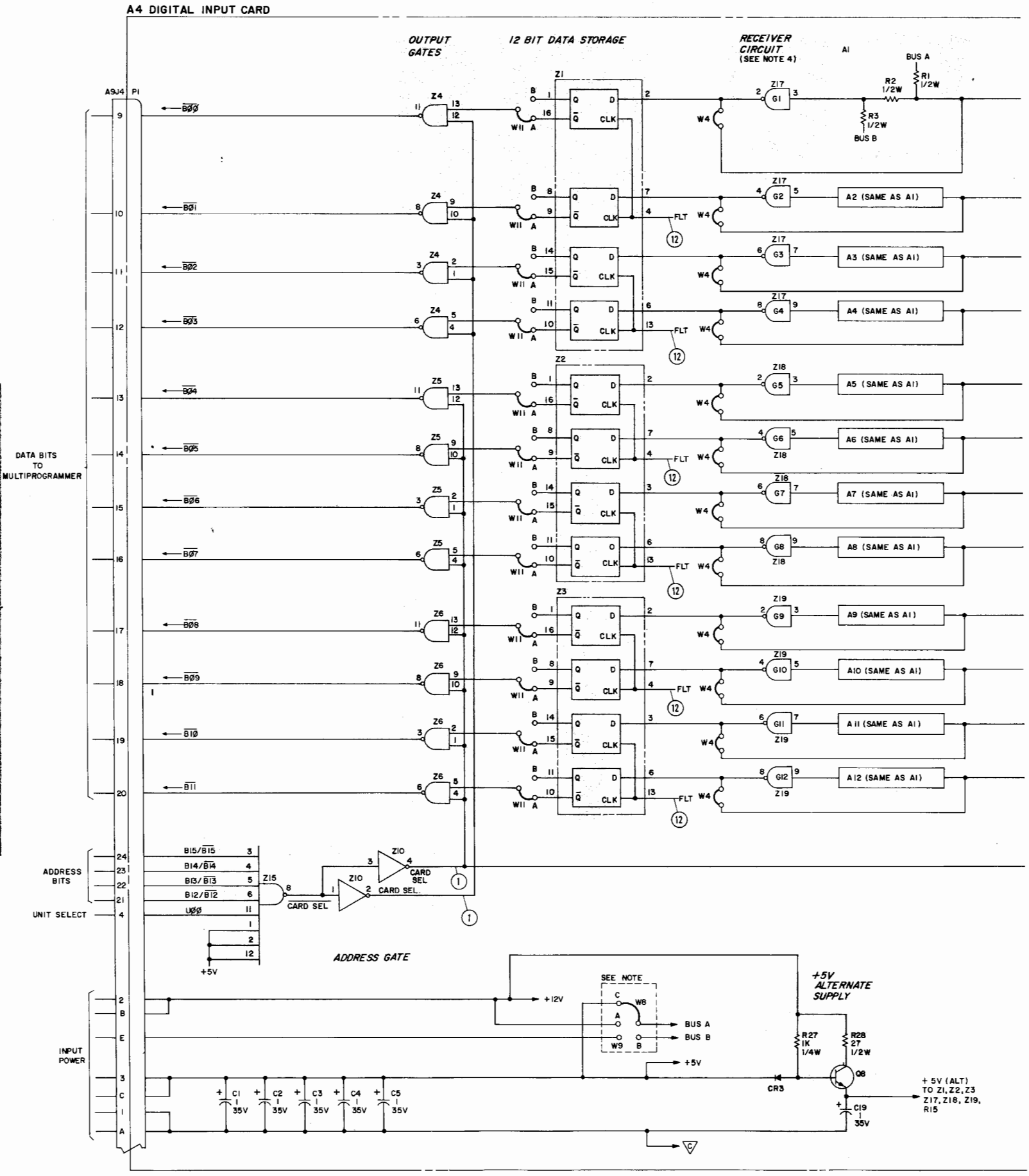
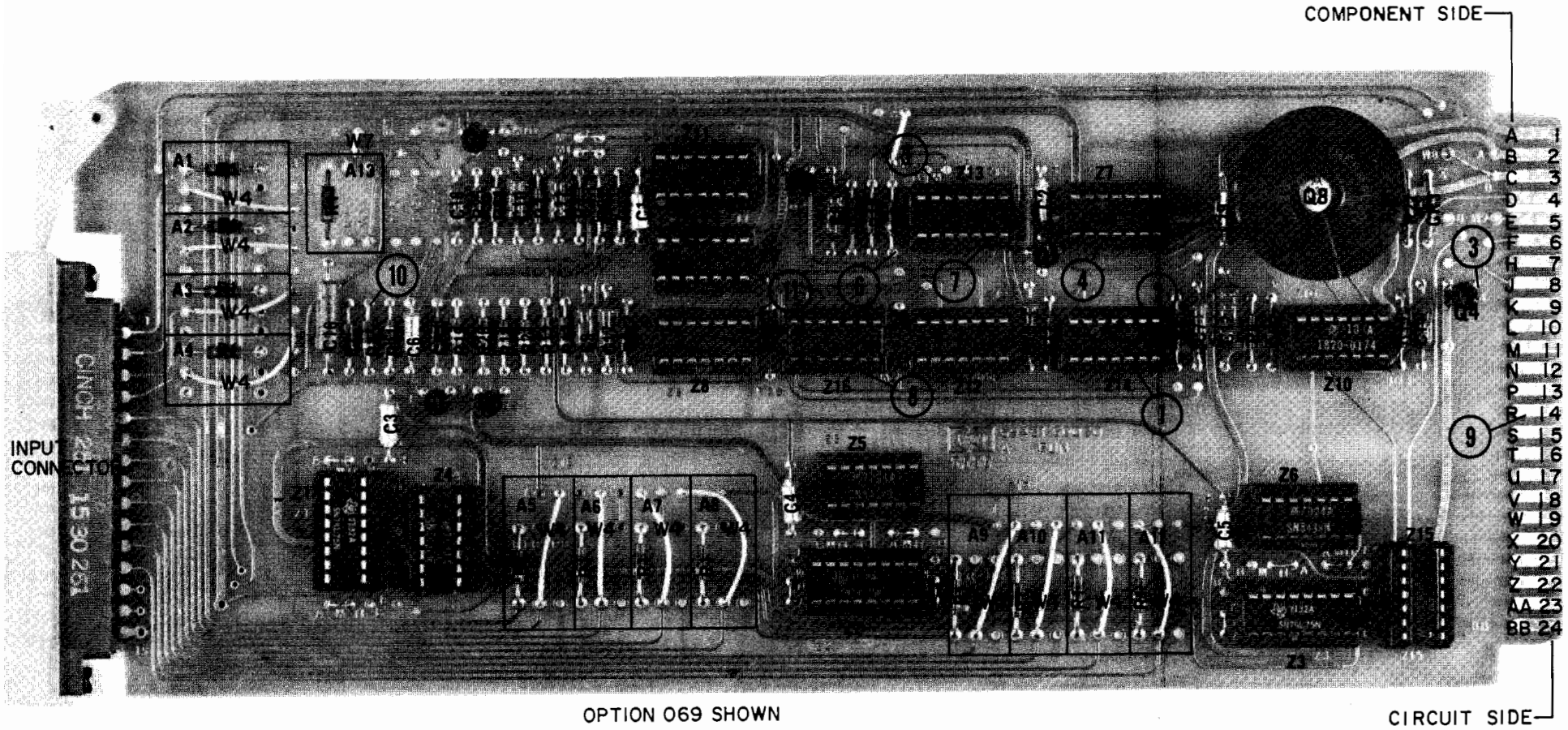



Figure 7-1 (Sheet 1). Digital Input Card, Schematic Diagram


A4 DIGITAL INPUT CARD
OUTPUT GATES
12 BIT DATA STORAGE
RECEIVER CIRCUIT (SEE NOTE 4)
A1
BUS A
BUS B
R1 1/2W
R2 1/2W
R3 1/2W
ASJ4 P1
DATA BITS TO MULTIPROGRAMMER
ADDRESS BITS
UNIT SELECT
INPUT POWER
ADDRESS GATE
CARD SEL
+5V
+12V
SEE NOTE
+5V ALTERNATE SUPPLY
R27 1K 1/4W
R28 27 1/2W
Q8
CR3
C1 35V
C2 35V
C3 35V
C4 35V
C5 35V
C19 35V
+5V (ALT) TO Z1, Z2, Z3 Z17, Z18, Z19, R15
A2 (SAME AS A1)
A3 (SAME AS A1)
A4 (SAME AS A1)
A5 (SAME AS A1)
A6 (SAME AS A1)
A7 (SAME AS A1)
A8 (SAME AS A1)
A9 (SAME AS A1)
A10 (SAME AS A1)
A11 (SAME AS A1)
A12 (SAME AS A1)
FLT




Digital Input Card, Component Locations

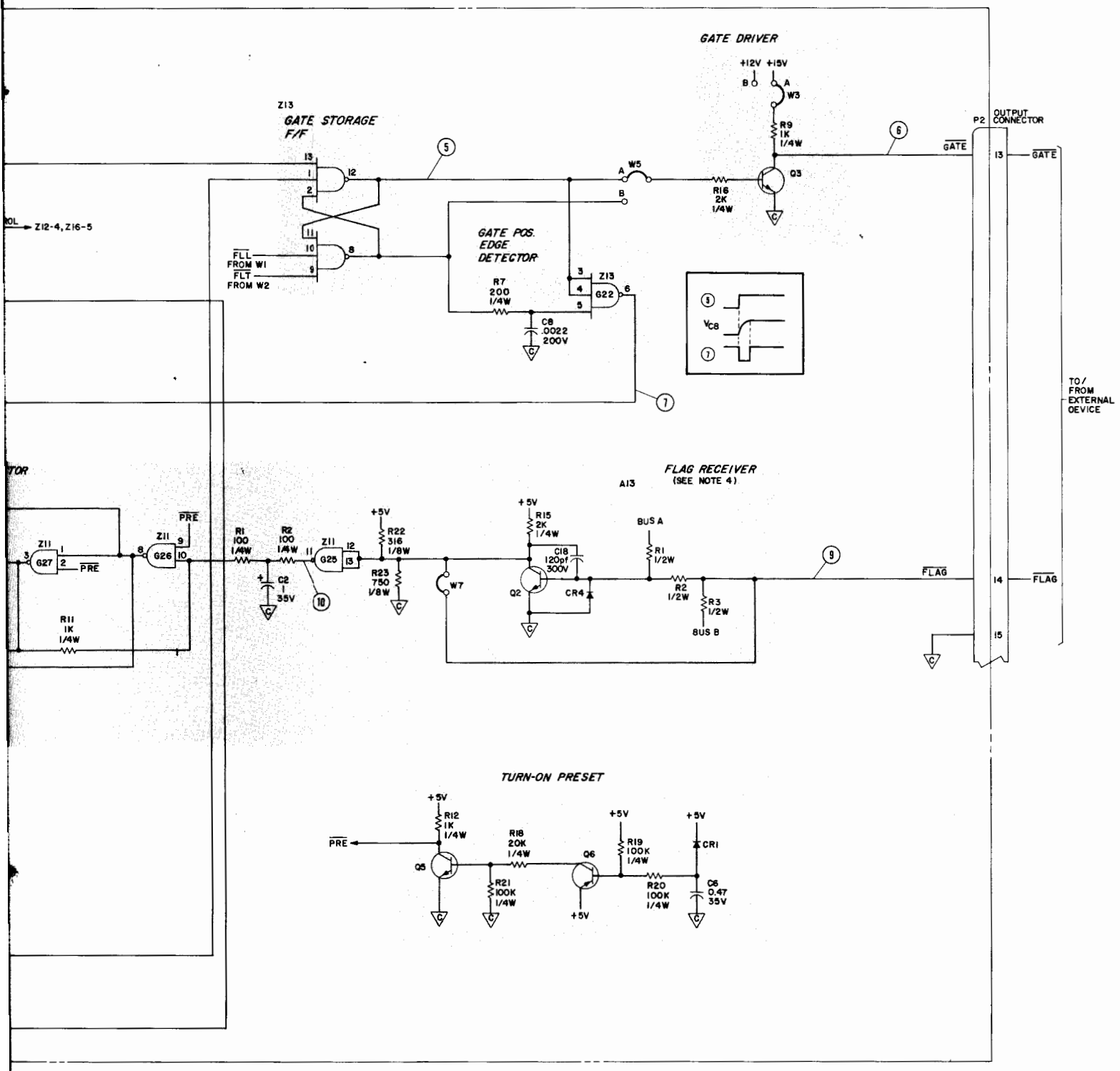
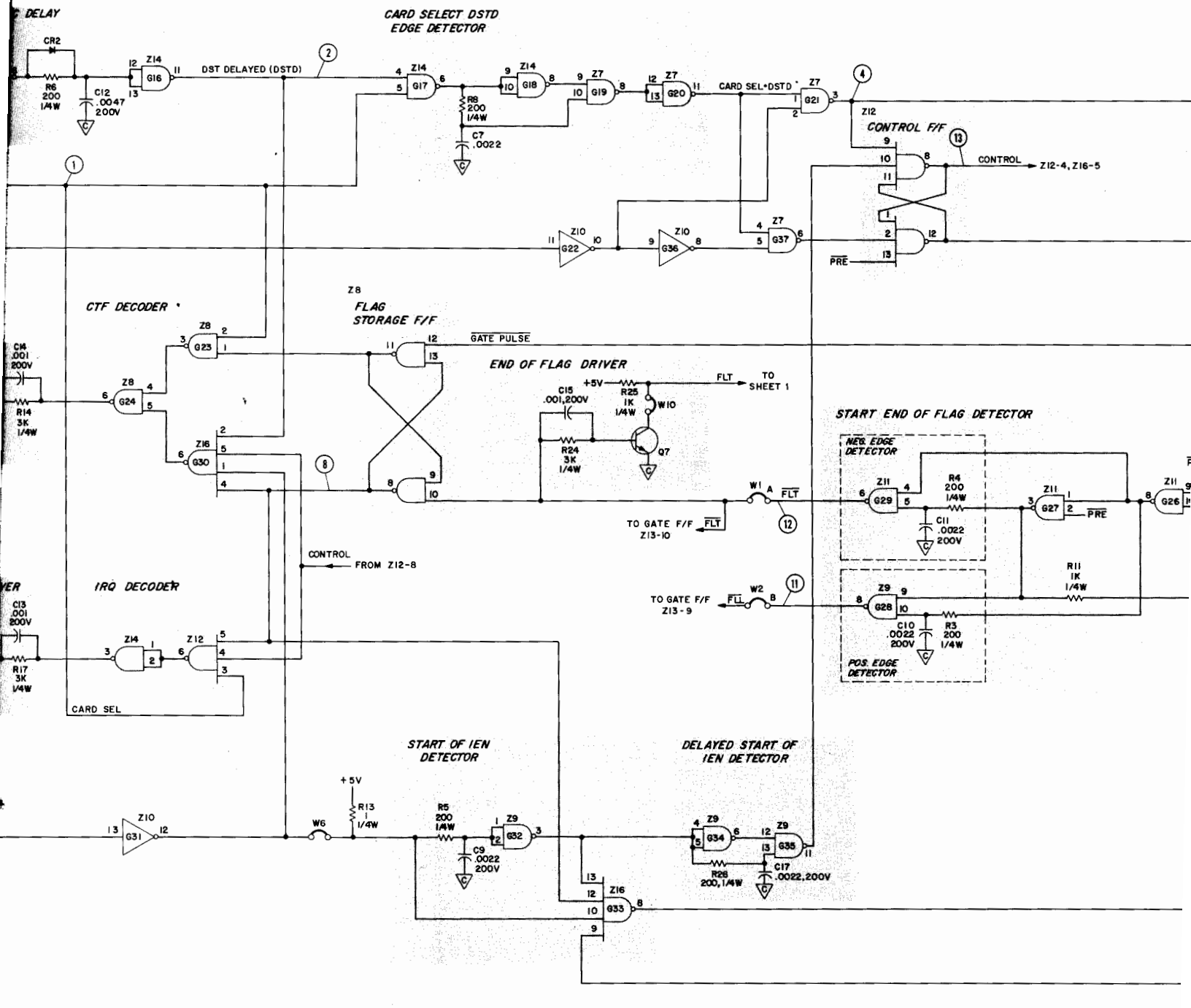
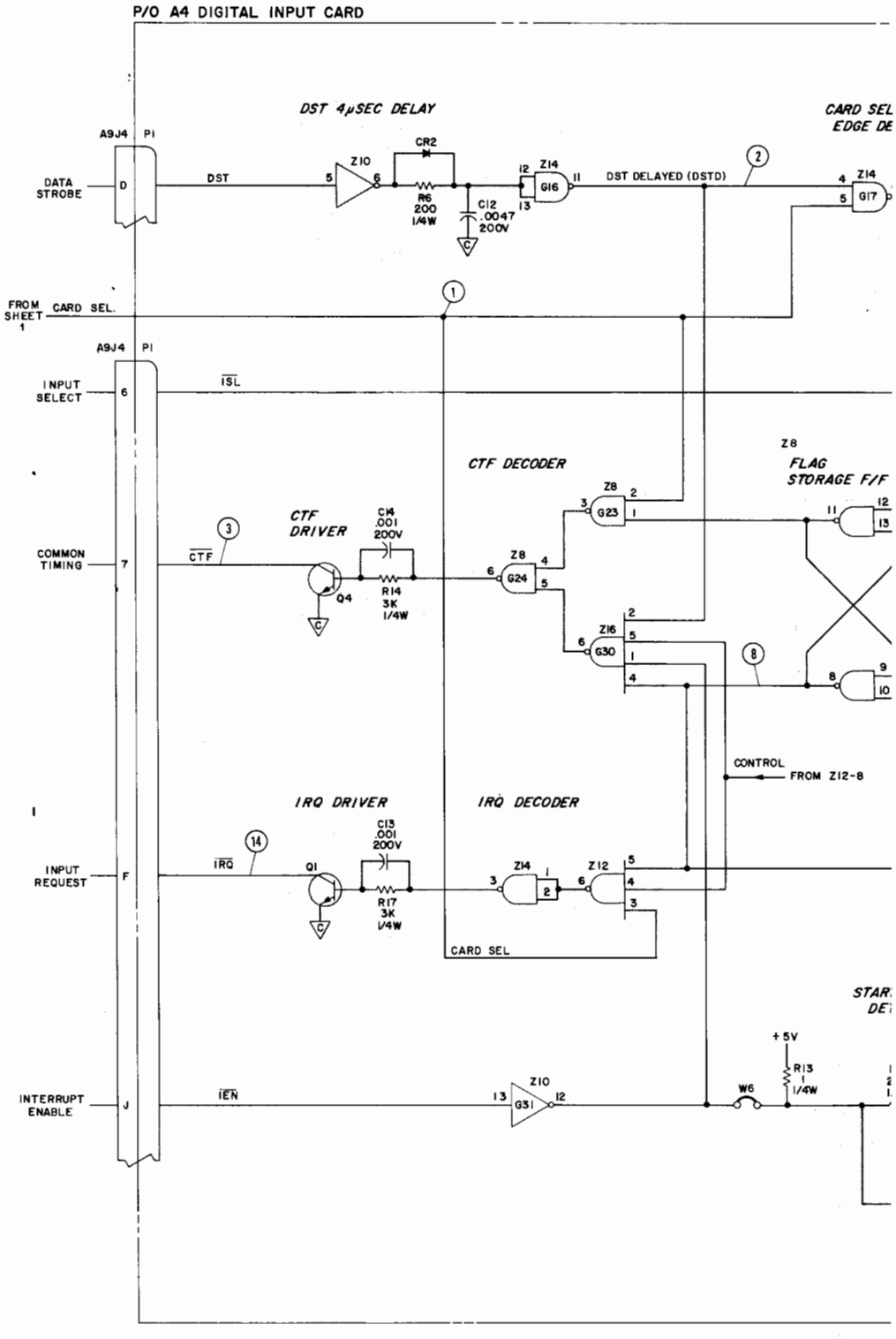
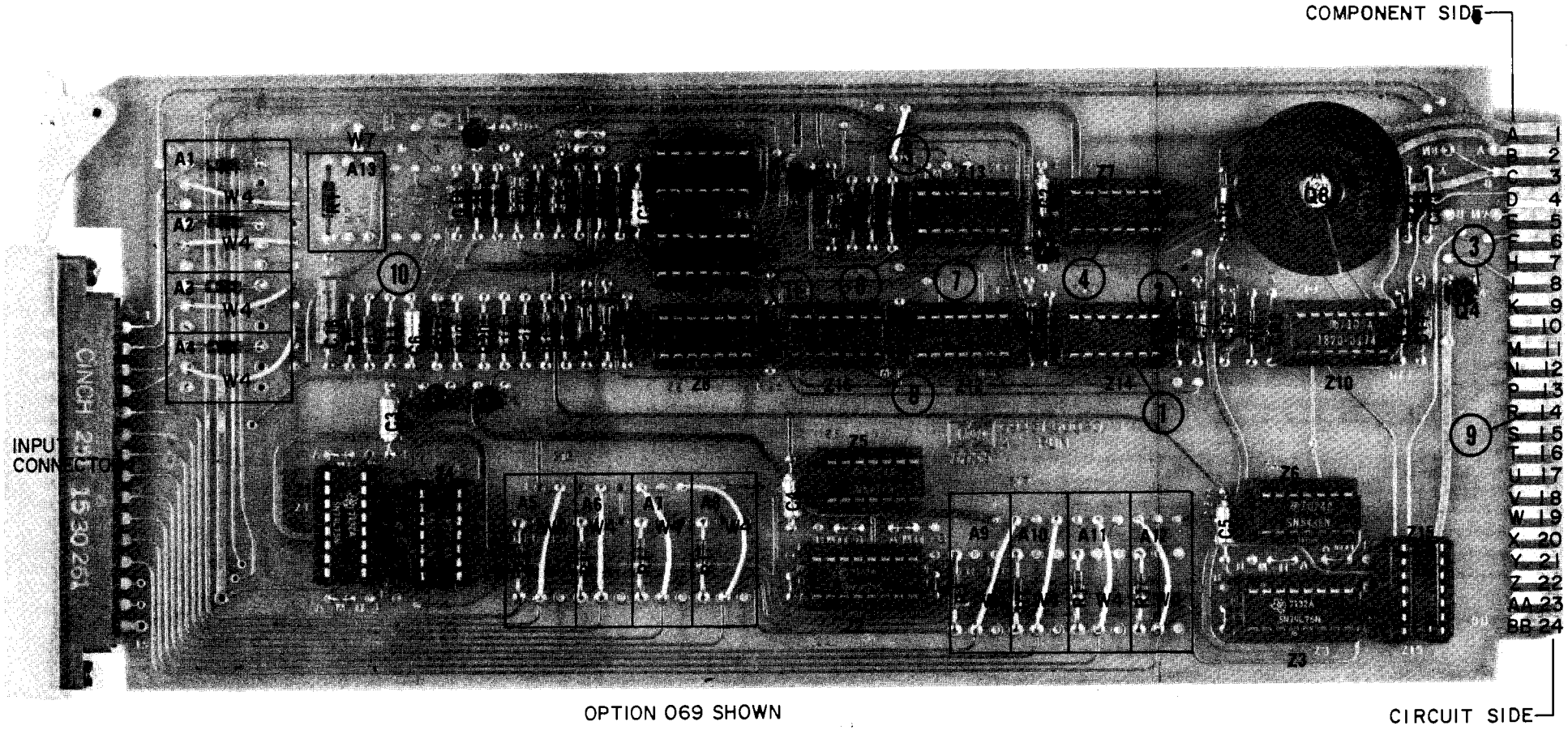



Figure 7-1 (Sheet 2). Digital Input Card, Schematic Diagram


DELAY
CR2
R6 200 1/4W
C12 .0047 200V
Z14 G16
DST DELAYED (DSTD)
CARD SELECT DSTD EDGE DETECTOR
Z14 G17
R8 200 1/4W
C7 .0022
Z14 G18
Z7 G19
Z7 G20
CARD SEL•DSTD
Z7 G21
Z12
CONTROL F/F
CONTROL
Z12-4, Z16-5
Z10 G22
Z10 G36
Z7 G37
PRE
CTF DECODER
Z8
FLAG STORAGE F/F
Z8 G23
Z8 G24
Z16 G30
C14 .001 200V
R14 3K 1/4W
GATE PULSE
END OF FLAG DRIVER
+5V
C15 .001,200V
R25 1K 1/4W
W10
R24 3K 1/4W
Q7
FLT
TO SHEET 1
W1
TO GATE F/F Z13-10
START END OF FLAG DETECTOR
NEG. EDGE DETECTOR
Z11 G29
R4 200 1/4W
C11 .0022 200V
Z11 G27
Z11 G26
R11 1K 1/4W
W2
TO GATE F/F Z13-9
Z9 G28
C10 .0022 200V
R3 200 1/4W
POS. EDGE DETECTOR
CONTROL
FROM Z12-8
IRQ DECODER
C13 .001 200V
R17 3K 1/4W
Z14
Z12
CARD SEL
START OF IEN DETECTOR
DELAYED START OF IEN DETECTOR
+5V
Z10 G31
W6
R13 1/4W
R5 200 1/4W
Z9 G32
C9 .0022 200V
Z9 G34
Z9 G35
R26 200,1/4W
C17 .0022,200V
Z16 G33


P/O A4 DIGITAL INPUT CARD
DST 4μSEC DELAY
CARD SEL EDGE DE
A9J4 P1
DATA STROBE
D
DST
Z10
CR2
R6 200 1/4W
C12 .0047 200V
Z14 G16
DST DELAYED (DSTD)
Z14 G17
FROM SHEET 1 CARD SEL.
A9J4 P1
INPUT SELECT
6
ISL
CTF DECODER
Z8
FLAG STORAGE F/F
CTF DRIVER
C14 .001 200V
COMMON TIMING
7
CTF
Q4
R14 3K 1/4W
Z8 G23
Z8 G24
Z16 G30
CONTROL
FROM Z12-8
IRQ DRIVER
IRQ DECODER
C13 .001 200V
INPUT REQUEST
F
IRQ
Q1
R17 3K 1/4W
Z14
Z12
CARD SEL
+5V
R13 1/4W
W6
INTERRUPT ENABLE
J
IEN
Z10 G31




Digital Input Card, Component Locations