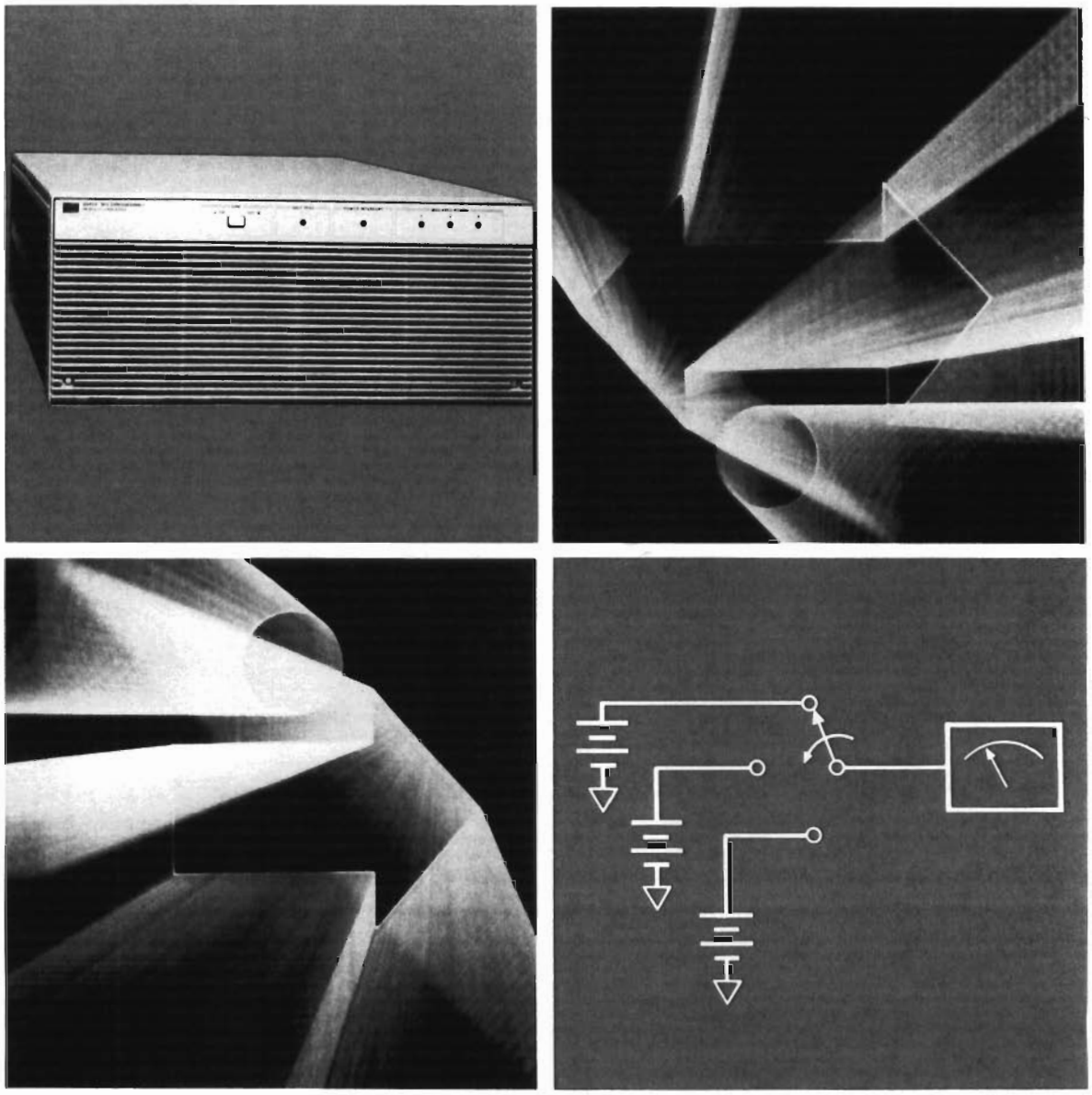
HEWLETT PACKARD

APPLICATION NOTE 316-3

High Speed FET Scanning

with the 6942A Multiprogrammer



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HP Part Number 5952-4073

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CHAPTER 1
INTRODUCTION

1-1 OVERVIEW-SCANNING

Scanning is one method of routing signals from several sources to a single destination. Scanning is generally used when one source at a time must be connected to the destination. The sources can be selected by the scanner and routed to the destination either sequentially or randomly. For sequential applications, the sources are assigned numbers and then routed to the destination in numerical order. In random scanning, the sources may be selected in any sequence. The destination is usually an A/D converter, a voltmeter, or some other signal processor. Most applications which involve data acquisition for process control can use scanning to control signal flow. A typical scanner configuration is shown in Figure 1-1.

A number of factors affect the design and operation of this or any scanning system:

1. The number of signal sources and destinations
2. Voltage and current levels of the signals
3. The series resistances of closed switches
4. Input and output leakage currents
5. Feedthrough characteristics of open switches
6. Crosstalk between signal paths
7. Bandwidth restrictions on the signals
8. The scanning rate
9. The scanning sequence (random or ordered)
10. Settling time of all system components
11. Signal and data processing time

The first factor determines the system configuration. The others are determined by the configuration and by the specifications of the instruments used to build it. Values for each of these factors are given in each of the configuration descriptions in this Application Note. Specifications for the instruments used in each application are in their Operating Manuals, listed in Appendix C.

1-2 SCANNING SYSTEMS

1-3 69750A Family of Cards

High speed scanning applications are handled well by the 69750A Scan Control/Pacer card and at least one of these cards:

69752A 64-channel FET card
69755A 16-channel FET card

Figure 1-2 shows a general 69750A-family scanning system with a 69751A A/D Converter and a system controller. The scanner card connects sources 0 to 63 one at a time to the destination, a 69751A A/D Converter card. If there were sixteen of fewer sources, the 69752A 64-channel FET card could be replaced by a 69755A card. If there were more than 64 sources, then 69752A and 69755A cards could be combined, all controlled by a single 69750A card. The A/D converter changes incoming analog signals to digital data for formatting and storing by the Multiprogrammer. The system controller coordinates these operations, and retrieves the formatted data for additional processing or storage.

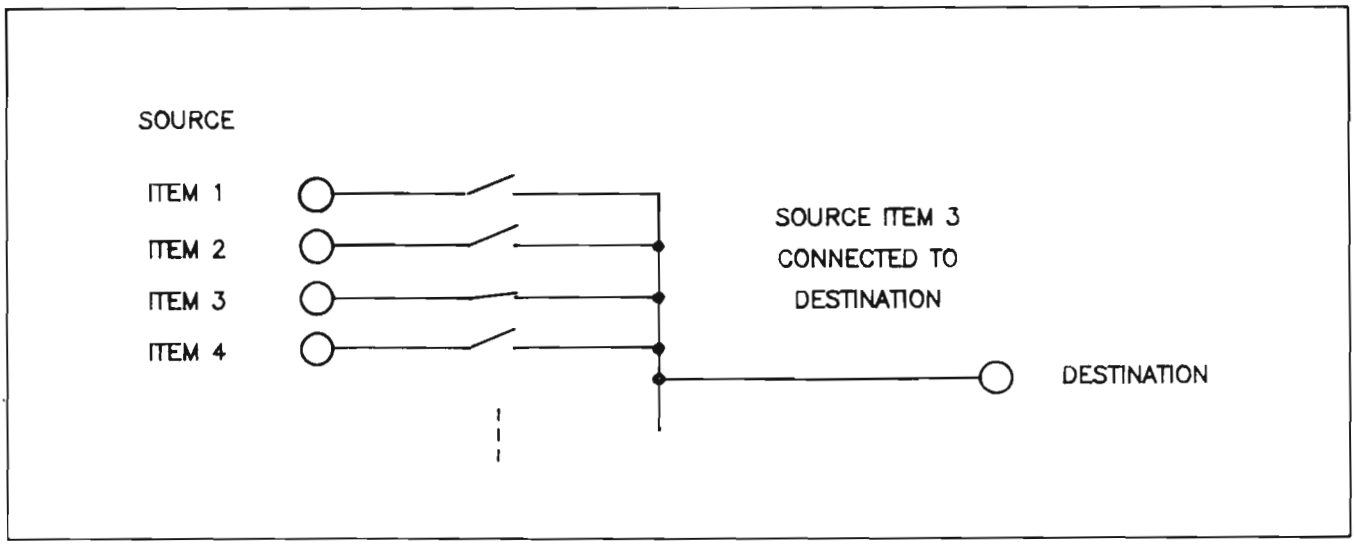


Figure 1-1. Scanner Configuration

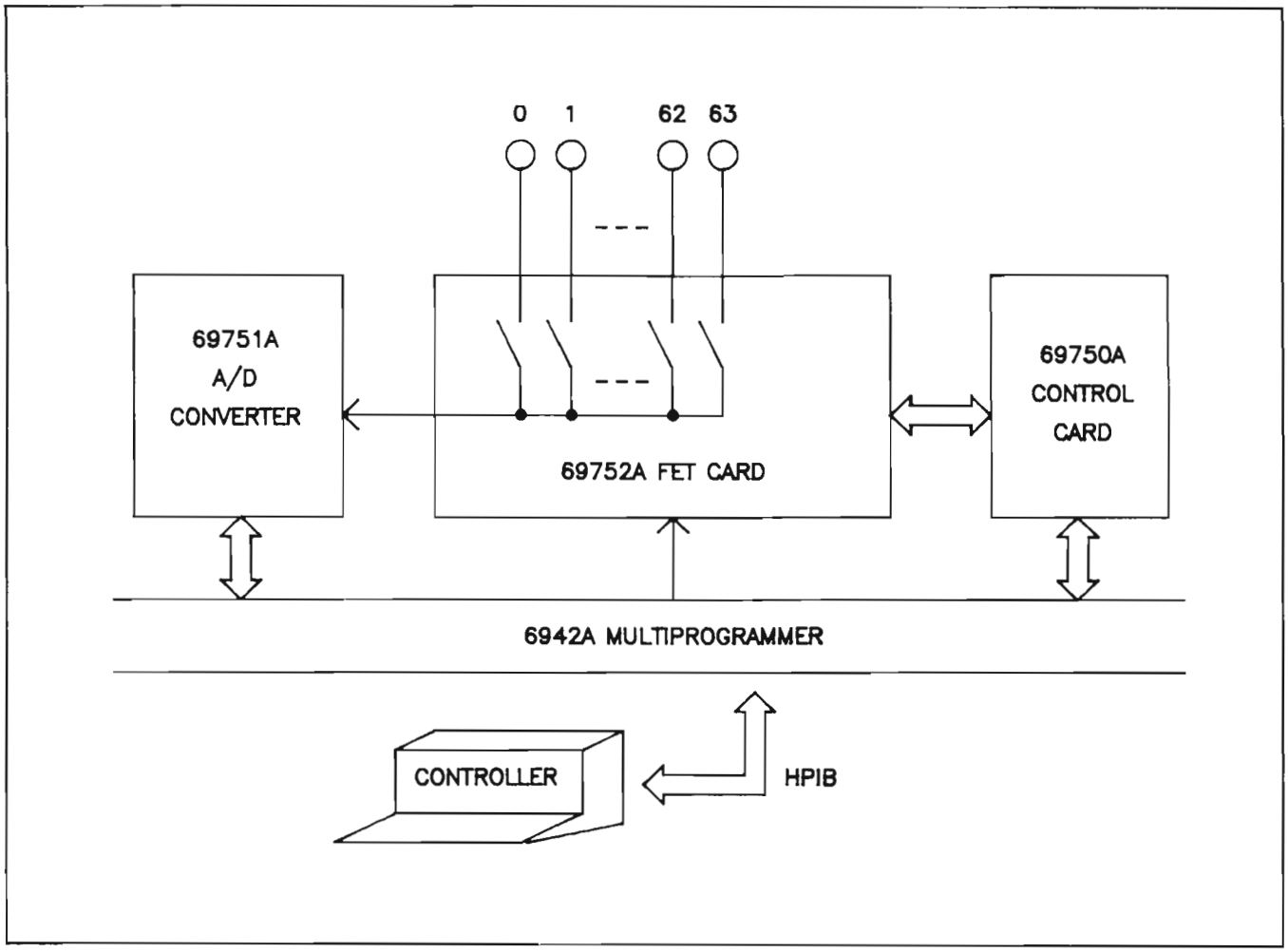


Figure 1-2. Multiprogrammer Scanning System

1-4 Card Descriptions

1-5 **69750A Scan Control/Pacer Card.** The control/pacer card contains logic and drive circuitry to operate up to 32 cards, scanning a maximum of 1024 channels. You may mix 69752A and 69755A cards so that the total number of channels is not more than 1024. A single 69750A can control up to 32 69755A 16-channel FET cards (32 x 16 channels = 512), up to 16 69752A 64-channel FET cards (16 x 64 channels = 1024), or any combination of cards that totals 1024 channels or less.

The number of cards in a system also depends on your Multiprogrammer system. One 6942A mainframe can support up to seven 6943A extenders, and each mainframe or extender can contain up to 16 cards. The 69752A and 69755A scanner cards are not addressable through the Multiprogrammer backplane. All communications between them passes through the control/pacer card.

1-6 **69752A 64-Channel FET card.** This card is used in high-speed scanning applications where the signal voltages are less than ±10.24 volts maximum, with reference to isolated common. The settling time of the FET switches is less than 10 microseconds. This card is best suited to applications with moderate specifications on closed switch offset voltage and "ON" resistance.

1-7 **69755A 16-Channel FET card.** This card is similar to the 69752A in all specifications, but there are fewer channels.

1-8 Modes of Operation

1-9 **Sequential Scanning.** Before the scanning operation is begun, the start and stop channels for the scan are programmed to the control/pacer card. Each time the system controller requests a reading from the A/D converter, the control/pacer card selects the channel to be read next. The scanning rate in this system is determined by how often the controller requests A/D conversions, and by the Multiprogrammer's instruction processing time. After the stop channel is read through the A/D, the start channel is selected as the next channel to be read, and the sequence begins again. Think of the scanner as a rotary switch, with the next position selected automatically after each A/D conversion completes.

1-10 Random Access. When the system is operating in the Random mode, the next channel to be selected may be determined either by the system controller or by external data inputs to the control/pacer card. The system controller determines the next channel directly, by sending the number of the next channel to the control/pacer card. The external inputs to the 69750A could be connected to the data outputs of a 69790B Memory card, with the channel sequence stored in the memory card. This method of operation is described in Chapter 3.

1-11 Internal/External Pacing and Buffered Input. The scan rate can be controlled either by the programmable pacer on the control/pacer card, or by an external timer. Because the scan rates can be high enough so that the system controller does not have enough time to transfer data from the A/D converter card to its memory after each reading, data may be written directly from the A/D converter card to a 69790B Memory card. The data can then be transferred in blocks to the controller. The overall data transfer rate may be faster when using the memory card as an intermediate storage buffer. This type of operation is described in Chapter 3.

1-12 Crosspoint Mode. Normally, only one channel in the system can be selected at a time. The previous channel connection is broken before the next channel is selected, so that only one switch is closed at a time. This can be partially overridden in the crosspoint mode, which lets more than one card in the system be enabled at a time. One channel per enabled card can be selected, so there can be as many channels selected at a time as there are cards in the system.

1-13 Card Enable/Disable. All switches on a scanner card may be disabled (opened) either by an external signal or by a code programmed to the control/pacer card.

1-14 Single Ended Operation. When several sources share a common signal return path, the high side of each source may be switched to the high side of the destination as each channel is scanned. The returns for all the sources can then be connected together at the isolated signal common of the destination.

1-15 Double Ended Operation. There may be some special applications which require double ended operation. Consult the 69752A and 69755A Operating Manuals for details of double-ended operation.

1-16 SCANNER APPLICATIONS

1-17 Circuit Characterization

The 69752A 64-channel FET scanner card is used when many points in a circuit must be repetitively checked to verify proper operation. In circuit characterization, the test set must measure voltages at several points in the circuit. This type of test is used for design verification, final production tests, and incoming inspection of purchased circuits. For example, suppose that you had to test the operation of several power supplies during a burn-in test.

A 69752A 64-channel FET card controlled by a 69750A Scan Control/Pacer card can be used to scan the power supply circuit test points in this application, as long as the test point voltages never exceed the ± 10.24 volt operating limits of the FET card. The 10 microsecond FET switching times let the test system check each point frequently, for high test accuracy. The scanning rate for each test point is limited by the A/D converter settling time and the system controller data transfer rates. Chapters 2 and 3 contain more information on these limits.

The configuration in Figure 1-2 could be used for the power supply test system described above. The scanner system is set for sequential scanning.

1-18 Transducer Measurement

Sequential scanning does not work for all applications. In a processing plant, suppose that there are 20 pressure tranducers and 20 flowmeters. The process is divided into four stages, with five transducers and five flowmeters monitoring each stage. The priority assigned to checking each transducer and flowmeter will probably vary as the processing continues. If there is a problem anywhere in the process, the controlling system will have to pay more attention to the measurement devices in that area. Suppose that the system requires that the transducers and flowmeters normally be checked in this order: 0 to 9, 20 to 29, 10 to 19, 30 to 39, and then back to 0 to 9.

If the scanning sequence is fixed--if the priorities never change--then the sequence should be hardwired, and the scanner system should be set for sequential scanning. Because the sequence in the example must change in response to process conditions, then the scanner should be set to the random mode, and the scanning sequence should be set through the controlling software. The sequence can be constantly updated to follow the needs of the process under control. Figure 1-3 shows a random scanning system.

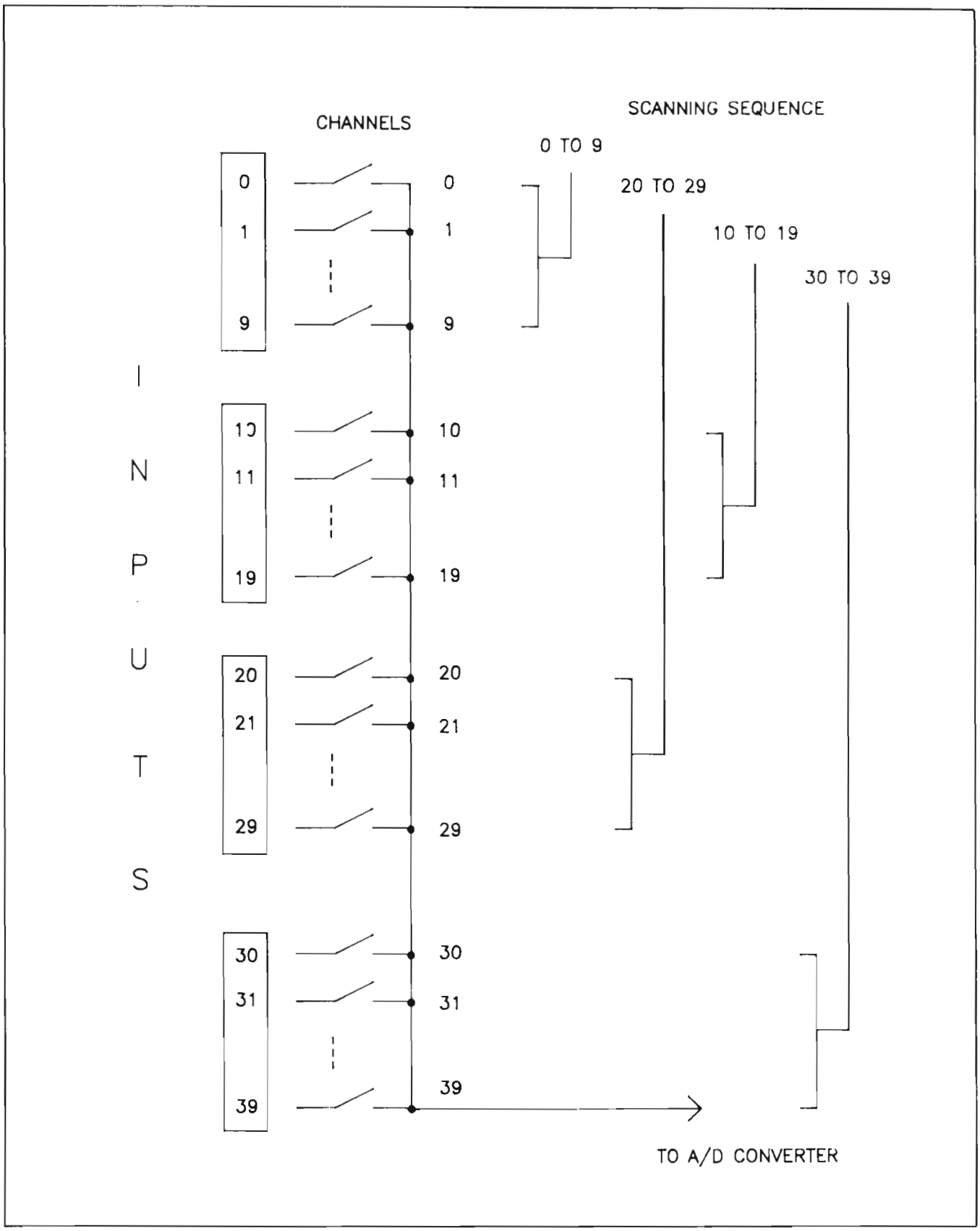


Figure 1-3. Random Channel Selection

CHAPTER 2
APPLICATIONS

2-1 BASIC OPERATING TECHNIQUES

2-2 Sequential Scanning

The power supply test set described in Paragraph 1-17 consists of a scanner, its control card, A/D, a 6942A mainframe, and a system controller. The test set uses a single-ended sequential scan of 41 points in the circuit under test.

Some of the specifications that make a FET scanner card suitable for high-speed, moderate-accuracy circuit measurements are:

- ± 10.24 volt input signal range.
- 0.026% full-scale accuracy with 1k ohms or less source resistance. Each additional card degrades this by specification 0.0063%. These figures must be added to the A/D converter specifications to obtain system accuracy.
- 4k ohms "on" resistance per switch.
- 10 microsecond settling time to within 0.05% of final value, with 1k ohms or less source resistance.

These specifications are accurate for temperatures between 0° C and +70°C at a relative humidity less than 60%. Consult the operating manual for a complete set of specifications.

The operating speed of the power supply test set is determined by the system controller, the A/D converter, and the FET card. Each conversion takes 30 microseconds. If there is a full-scale voltage difference between any two channels, the sample-and-hold amplifier needs up to 15 microseconds to settle. The FET switches settle in 10 microseconds. The End-of-Conversion signal (EOC) from the A/D converter triggers the selection of the next channel, which synchronizes channel selection with conversion time. The system controller software accounts for A/D and FET switch settling time.

2-3 Control Card Subaddresses. The 69750A is a multifunction I/O card. Its input and output functions are accessed through the Read and Write subaddresses, which are added to the card address on the right side of the decimal point. Examples of instructions using subaddresses are in Paragraph 2-29. Depending on the I/O card, the instruction type, and the function of the subaddresses, data may be written to or read from them. Table 2-1 lists the subaddresses and their functions. The zero preceding the subaddresses in the table is the address of a card in slot 0.

Use the Write First Rank (WF) output instruction to write data to the control card subaddresses. Use the Read Value (RV) input instruction to read data from the control card. These instructions do not cycle the card. Normally, the card should not be cycled with the same instruction that programs it. If you must cycle the card immediately after programming a subaddress, then use the Output Parallel (OP) and Input Parallel (IP) instructions, which cycle the card as part of their operation.

Table 2-1. Read & Write Subaddress

Subaddress	Function	Data Format
Write		
0.0	Sequential mode: start channel Random mode: next channel	Decimal
0.1	Sequential mode: stop channel	Decimal
0.2	Pacer period (μs or ms)	Decimal
0.3	Control register	Decimal
Read		
0.0	Present channel	Decimal
0.1	Start channel	Decimal

2-4 Control Card Mode Selection. The control card is set to the Sequential Scan mode by writing a decimal 1 to the Mode Select Register (subaddress 3). Writing a 0 to the Register puts the card in the Random Access mode. The control card "wakes up" with the Mode Select Register reset to all zeroes. The function of each control register bit is shown in Table 2-2. The card functions are programmed by writing ones or zeroes to the Mode Select Register.

Table 2.2 Mode Select Register Bits

Register Bit	Programmed Value	
	0 (Wake-up)	1
0	Random access mode	Sequential scan mode
1	Switches enabled	Switches disabled
2	Triggered externally or by software	Triggered internally by pacer
3	Not used	External trigger lockout
4	Not used	Lockout reset
5	Crosspoint mode off	Crosspoint mode on
6	No interrupt on stop channel	Interrupt on stop channel
7	No interrupt on lockout	Interrupt on lockout
8	1 μsec pacer timebase	1 msec pacer timebase
9	Internal Start channel address source	External start channel address source
10-13	Not used	Not used

The Mode Select Register has the following format:

Bit 13			Bit 2	Bit 1	Bit 0
0	...	...	0	0	1

Bit 0 represents $2^0 = 1$ if bit 0 = 1.
Bit 1 represents $2^1 = 2$ if bit 1 = 1.
Bit 2 represents $2^2 = 4$ if bit 2 = 1.

.
.
.

Bit 13 represents $2^{13} = 8192$ if bit 13 = 1.

To program the Mode Select Register, add the decimal values of the bits you want to program to 1, and program the sum to subaddress Write 3.

To set the card for internal triggering by the on-board pacer, program bit 2 to 1 by sending the decimal value $2^2 = 4$ to subaddress 3. To set the card for internal pacer triggering, with the card in the sequential scan mode, program bits 0 and 2 to 1. Send the sum of their decimal values, $2^0 + 2^2 = 5$, to subaddress 3.

2-5 Start/Stop Channels. The first channel to be selected when scanning begins is programmed by writing the decimal number representing the channel to control card subaddress 0. The last channel in the scanning sequence is programmed by writing the decimal number representing the channel to control card subaddress 1. After the Stop channel is selected, a recycle signal (EQ) is generated, which causes the Start channel to be re-selected the next time the scan control card is cycled.

2-6 Cycling the Control Card. In the power supply test example, the A/D converter controls the cycling of the control card. When the control card is cycled, the next channel is selected. Figure 2-1 shows the system, and Figure 2-2 shows its sequence of operation.

The system controller requests the A/D converter to take a reading at time A, Figure 2-2, and the A/D starts a conversion. After the conversion is complete, the A/D card generates an End-of-Conversion (EOC) signal, which is connected to the External Trigger (EXT) input of the scan control card. The EOC signal cycles the Scan Control/Pacer card at time B, causing it to select the next channel.

The settling time of the FET switches and the A/D input stage is measured in microseconds, and program run time is measured in milliseconds, so settling time is not significant. The digital output of the A/D card is passed to the 6942A after the end of the BUSY pulse from the A/D. The system controller can then read the data from the Multiprogrammer and process it as described in paragraph 2-28. The next channel in the sequence is read by the A/D converter at time C. The control card may be cycled by a software instruction as well as by an external trigger, but this example uses the external trigger only. See the 69750A Scan Control/Pacer card Operating and Service Manual, listed in Appendix C.

2-7 Isolated 6942A 18 Volt Supplies. The 6942A has three ±18 volt power supplies which are isolated from data common (GND) and from each other. The isolation permits analog cards to be isolated from one another and from all data circuits. All 6942A system cards that use the isolated power supplies are shipped from the factory with jumpers set so the card uses isolated Power Supply No. 1. The 69752A and 69755A FET cards are used as shipped, with isolated power Supply No. 1 connected. The 69751A A/D converter is also used with isolated Supply No. 1, which ensures that the A/D converter and the FET card share the same isolated common. Appendix A explains isolated power supply allocation and power supply selection jumper configurations.

2-8 Trigger and Gate/Flag Switches. The 69750A control card is shipped from the factory with S1-1 open, S1-2 closed, and S1-3 closed. The setting of S1-1 and S1-2 permits both software and external triggers to cycle the card. S1-3 connects the card's Gate output to the Flag input, since Gate/Flag handshaking is not used in the scanner system. S1-4 is not used.

2-9 FET Card Size Select Jumpers. The power supply testing example uses a 69752A FET card set up for 64-channel single-ended operation, which is how the card is shipped from the factory. All 64 inputs are routed to Analog Output 1.

2-10 FET Card Start Address Selection. S1 is a dual in-line switch which sets the first channel address of the card. There are seven slide switches on S1; each switch sets one bit of the address. The "1" position is marked by the numbers across the top of S1. The switch on the end of S1 next to the dot sets the MSB (bit 1). S1 can be set to represent the numbers 0 to 127. The card is shipped with all seven switches off, for a first channel address of 0. There should normally be only one channel selected for each address, so if there are several FET cards in the system, then the first channel address of the cards must be different. The first channel address of a card is equal to eight times the number represented by S1. The addresses are multiples of eight so that 64-channel 69752A and 16-channel 69755A FET cards can be combined in a scanner system.

Suppose that a scanner system consists of two 69752A cards and one 69755A card. The first 69752A card scans channels 0 to 63, the 69755A scans channels 64 to 79, and the second 69752A scans channels 80 to 143. The first channel address of the first card is 0, so the switches of S1 are left set to 0000000, as the card is shipped from the factory. The first channel address of the second card is 64, which is 8x8. S1 should be set to represent the number 8; its switches should be set to 0001000. The third card's first channel address is 80, or 8x10. Set S1 to represent the number 10 by setting the switches to 0001010.

CAUTION

Static electricity can damage the FET scanner cards. Always observe standard static electricity precautions when handling the FET Scanner cards.

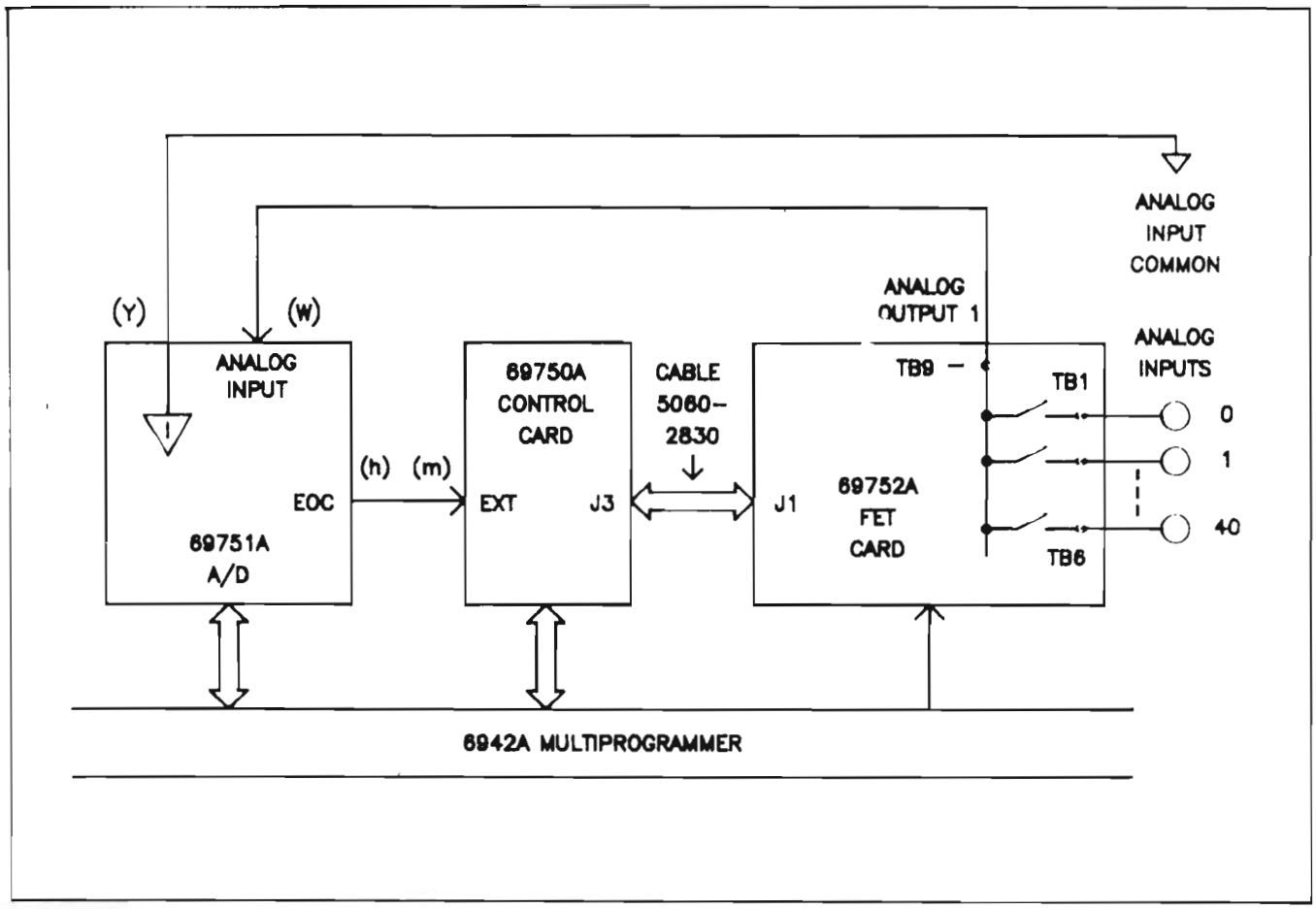


Figure 2-1. System Set-Up

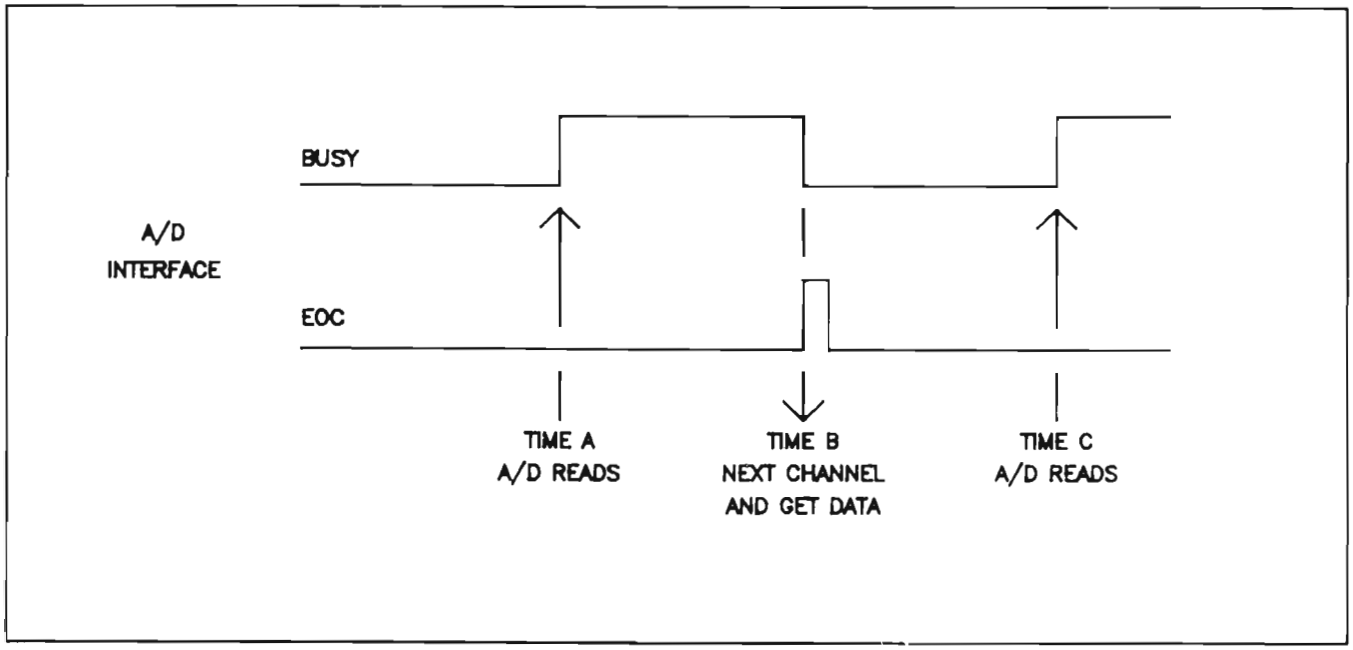


Figure 2-2. Sequence of Operation, Sequential Scanning

2-11 Analog Connections to the FET Card. Input connections to the 69752A FET card are made on the removable terminal blocks TB-1 through TB-8. Each input channel is marked on the printed circuit card. Inputs 0 through 40 are used in the power supply test example. All unused input connections should be wired to the signal return common to all sources. Output connections are made on TB-9. Only Analog Output 1 is used in the example.

NOTE

The signal returns for all of the sources should be connected to the isolated signal common on the A/D converter.

All input and output cables should be routed through the plastic cable clamps on the card for convenient access from the rear of the 6942A.

2-12 Digital Connections to the FET Card. The control and FET scanner cards are connected by the chaining cables which come with the cards. The scanner cards are connected to the control card by HP Part No. 5060-2830. The scanner cards are chained to each other by HP Part No. 5060-2829.

2-13 Interface to A/D Converter. The EOC output for the A/D converter card is connected to the EXT input of the control card as shown in Figure 2-1. The edge connector for the A/D converter is shown in Appendix B.

2-14 A/D Converter Card Configuration. At the factory, the A/D converter's S1-1 and S1-3 are opened, and S1-4 is closed, so the card can accept input signals which range from −10.24 to +10.235 volts. S1-2 is not used. For other input voltage ranges, the switch settings must be changed. Refer to the instruction manual for the A/D card for the input ranges and switch settings. In addition, the S2-1 switch is closed, and S2-2 and S2-3 are opened when the card is shipped. This allows both software instructions and external triggers to cycle the A/D, and causes a 13 to 17 microsecond delay from trigger to start of conversion.

The power supply test set is now ready. Programming instructions are given in Paragraph 2-25.

2-15 Random Channel Access

The process control system described in Paragraph 1-18 uses the random channel access mode to scan 40 channels, addresses 0 through 39. All timing signals come from the system controller. The scanning sequence is determined by the system controller.

2-16 Control Card Mode Selection. The control card is set to the random access mode by programming bit 0 of the Mode Select register to 0, as described in Paragraph 2-4. The card wakes up in the random access mode, so it is only necessary to program the random access mode if the card was used in the sequential mode since power-up.

2-17 Next Channel Selection. The next channel to be selected is determined by writing the address of the channel to subaddress 0 of the scan control card. (This is the subaddress used to program the start channel in the sequential scan mode).

NOTE

This system is the same as Figure 2-1, except that the EOC signal from the A/D converter is not connected to the control card EXT input.

2-18 Sequence of Operations. The sequence of operation of this system is determined entirely by the system controller. The system controller signals the scanner to select a channel at time A, Figure 2-3. The controller then triggers the A/D at time B. The A/D output data is sent to the Multiprogrammer and is read by the system controller at time C.

The A/D conversion time, the settling time of the A/D input amplifier and the settling time of the FET switches are measured in microseconds. These delays are not significant because the program run time is measured in milliseconds.

2-19 Isolated 6942A 18 Volt Supplies. The 69752A FET card and the 69751A A/D converter card are used as shipped from the factory, powered by isolated Supply No. 1. This insures that the FET card and A/D card isolated commons are connected, as described in Paragraph 2-7.

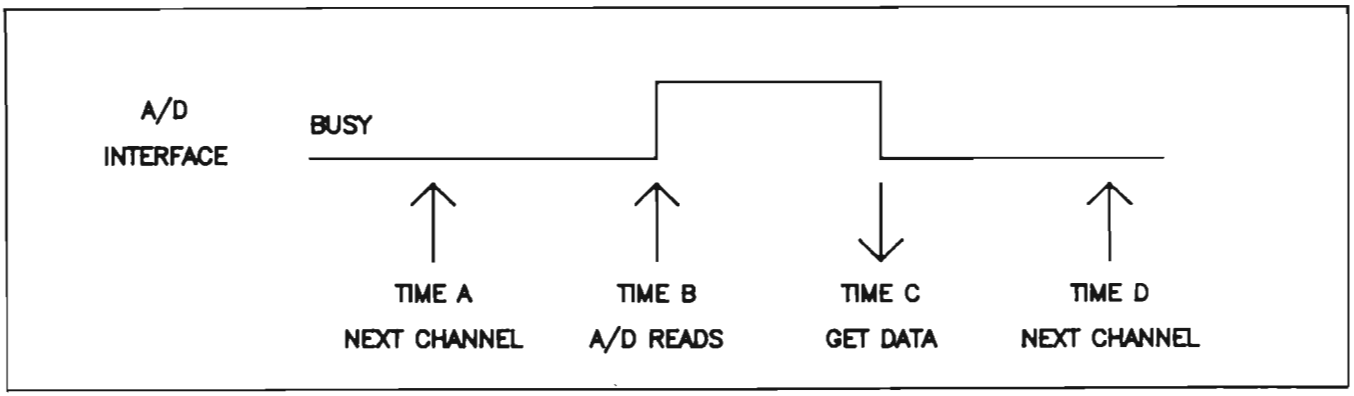


Figure 2-3. Sequence of Operation, Random Access

2-20 FET Card Set-Up. The transducer measurement example uses a single-ended scan of the first 40 channels of the 64-channel 69752A FET card. Follow the set-up instructions in Paragraphs 2-9 through 2-11.

2-21 Control Card Set-Up. No changes need to be made to the control card for this example, if it has not been changed from the factory settings. The card is shipped so it can be cycled by software triggers and external triggers, as in Paragraph 2-8.

2-22 Digital Connections to the FET Card. All connections between the control card and the FET card are made with the standard chaining cable.

2-23 Interface to A/D Converter. There are no digital connections between the A/D converter and the control card. The analog connections are shown in Figure 2-1. The A/D card's edge connector is shown in Appendix B.

2-24 A/D Converter Card Configuration. The A/D card is used as shipped from the factory, with an input range of −10.24 to +10.235 volts, and software triggering enabled.

The transducer measurement system is now ready to be programmed.

2-25 PROGRAMMING TECHNIQUES

2-26 Programming in BASIC

The programs in this chapter are written in the BASIC programming language on a 9826/36 system controller. The 9826/36 supports the BASIC, HPL, and PASCAL languages. This section uses only BASIC, because it is simple and widely used.

2-27 Sequential Scanning

2-28 Flow charts. It is usually helpful to use a flow chart to help organize a sequence of operations before programming. This is especially true when programming real-time data acquisition systems, where the order of the operations and the system timing requirements are extremely important. The flow chart in Figure 2-4 outlines the operations of a sequential scanner system. The rectangular boxes are action blocks, which represent operations such as I/O or data transfer, which do not require decisions by the system controller. The diamond boxes are decision blocks. At the decision blocks, the controller must make a yes-no decision. Such decisions are typically comparisons of input data with known limits. The program usually continues on a "yes" decision, and branches to a subroutine on a "no" decision. The subroutine may stop or return to the main program after taking corrective action. In the flow chart of Figure 2-4, the system reads all the data for the circuit test, and then prints out any values which are not within specifications.

2-29 Programming Examples. The 9826/36 is one of many Hewlett-Packard system controllers which transfer data to and from their peripherals via HP-IB. The data may be either instructions for a peripheral or data transferred to or from an I/O or storage device.

The following BASIC commands, which program a 69750A card in slot 13 of a Multiprogrammer, are in Example 2-1A. All of the commands begin with BASIC program line numbers from Example 2-1A.

```
100 OUTPUT 723;"CY13T"
```

When the Multiprogrammer is powered up or reset by an HP-IB Device Clear command, the control card is disabled. It must be enabled before programming, or the FET switches on the 69752A or 69755A cards will not turn on. Line 100 cycles the control card, which enables it.

723	HP-IB select code 7 and Multiprogrammer address 23
CY13	Multiprogrammer Cycle instruction for card in slot 13
T	Multiprogrammer instruction terminator

```
110 OUTPUT 723;"WF13.0,0T"
```

Line 110 programs the start channel to 0 by writing the number 0 to subaddress 0 of the control card. The FET switch for the start channel 0 is closed as soon as the channel number is written to subaddress 0, even though the card has not been cycled.

WF13.0,0 Writes first channel address 0 to card slot 13, subaddress 0

```
120 OUTPUT 723;"WF13.3,1T"
```

Line 120 programs bit 0 of the Mode Select Register (subaddress 3) to 1, which puts the card in the sequential mode.

WF13.3,1 Writes a decimal 1 to slot 13, subaddress 3.

```
130 OUTPUT 723;"WF13.1,40T"
```

Line 130 programs the stop channel to 40 by sending the decimal number 40 to control card subaddress 1.

WF13.1,40 Writes decimal 40 to slot 13, subaddress 1

```
150 OUTPUT 723;"IP15T"
```

Line 150 signals the A/D to take a reading. The digital output of the converter is stored in Multiprogrammer memory so the controller can retrieve it later. When the A/D reading is complete, the A/D generates an End-of-Conversion (EOC) pulse. EOC is connected to the control card External Trigger (EXT) input, so the pulse cycles the control card, which selects of the next channel.

```
160 ENTER 72301;I(K)
```

Line 160 reads the A/D converter output data from the Multiprogrammer through HP-IB extended talk address 01, and stores it in array I, element K .

72301	HP-IB Select code 7, Multiprogrammer address 23, extended talk address 01
I(K)	Array I, element K will contain the next reading

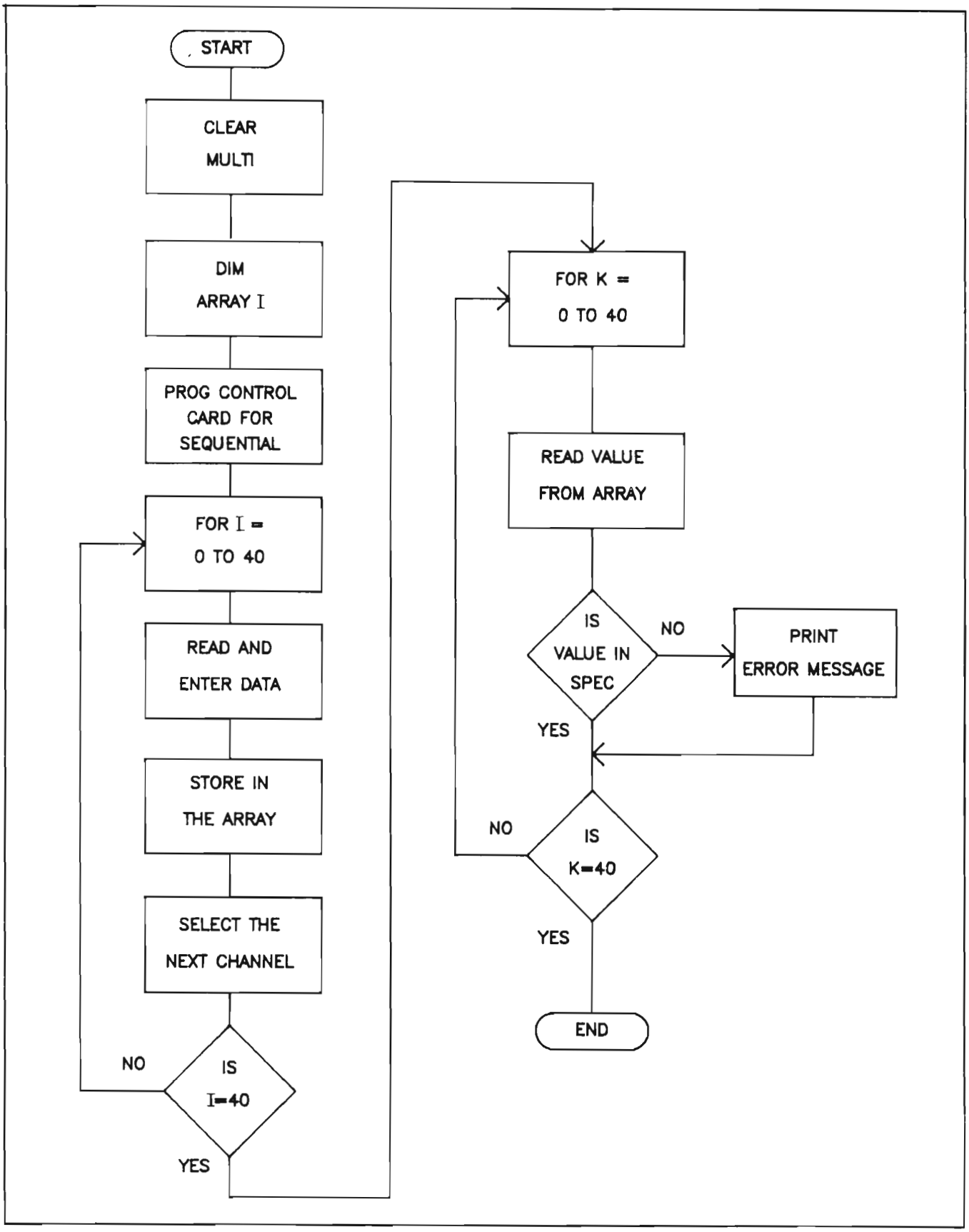


Figure 2-4. Flow Chart, Sequential Scanning

Example 2-1A. System Program, Sequential Scanning

```
10    ! THIS PROGRAM SETS UP A SEQUENTIAL SCAN
20    ! USING THE 69750A CONTROL CARD,69752A FET
30    ! AND THE 69751A A/D CARD.
40    !
50    !
60    OPTION BASE 0
70    CLEAR 723                                    !CLEARS THE MULTI FRAME
80    WAIT 4                                       !WAIT FOR SELF TEST TO END
90    DIM I(40)                                    !DIMINSIONS ARRAY I
100   OUTPUT 723;"CY13T"                           !ENABLES THE CONTROL CARD
110   OUTPUT 723;"WF13.0,0T"                       !SELECTS START CHANNEL
120   OUTPUT 723;"WF13.3,1T"                       !SETS THE MODE TO SEQUENTIAL
130   OUTPUT 723;"WF13.1,40T"                      !SETS THE STOP CHANNEL
140      FOR K=0 TO 40                             !LOOP TO READ 41 CHANNELS
150        OUTPUT 723;"IP15T"                      !INSTRUCTS THE A/D TO READ
160        ENTER 72301;I(K)                        !ENTER READING TO CONTROLLER
170   !                                             AND STORE READING IN ARRAY I
180      NEXT K                                    !NEXT READING
190        LET X=10.00                             !LINES 190 TO 230 CHECK THAT
200      FOR K=0 TO 40                             ! THE VOLTAGES ARE IN SPEC
210        IF I(K)<(X-.05) OR I(K)>(X+.05) THEN GOSUB Error
220        X=X-.50                                 ! IF NOT THEN PRINT ERROR
230      NEXT K                                    ! MESSAGE
240        PRINT                                   !PLACES SPACE BETWEEN THE ERROR
250        !                                         MESSAGE AND END STATEMENT
260        PRINT "END OF SCAN"                     !END OF SEQUENTIAL SCAN
270        STOP
280        !
290        !
300 Error: !                                       !ERROR MESSAGE ROUTINE
310         PRINT
320         PRINT "ERROR DETECTED ON CHANNEL";K
330         PRINT "VOLTAGE READ";I(K)
340         RETURN
350 END
```

Example 2-1B. System Program, Sequential

```
10    ! THIS PROGRAM SETS UP A SEQUENTIAL SCAN
20    ! USING THE 69750A CONTROL CARD,69752A FET
30    ! AND THE 69751A A/D CARD.
40    !
50    !
60    OPTION BASE 0
70    CLEAR 723                                    !CLEARS THE MULTI FRAME
80    WAIT 4                                       !WAIT FOR SELF TEST TO END
90    DIM I(40)                                    !DIMINSIONS ARRAY I
100   OUTPUT 723;"CY13T"                           !ENABLES THE CONTROL CARD
110   OUTPUT 723;"WF13.0,0T"                       !SELECTS START CHANNEL
120   OUTPUT 723;"WF13.3,1T"                       !SETS THE MODE TO SEQUENTIAL
130   OUTPUT 723;"WF13.1,40T"                      !SETS THE STOP CHANNEL
140   !                                            !THIS SECTION INSTRUCTS THE
150   OUTPUT 723;"IP,R41,15T"                      !A/D TO TAKE 41 READINGS THEN
160   ENTER 72301;I(*)                             !ENTER INTO THE CONTROLLER
170   !                                             AND STORE THEM IN ARRAY I
180   !
190   LET X=10.00                                  !LINES 190 TO 230 CHECK THAT
200   FOR K=0 TO 40                                ! THE VOLTAGES ARE IN SPEC
210     IF I(K)<(X-.05) OR I(K)>(X+.05) THEN GOSUB Error
220     X=X-.50                                    ! IF NOT THEN PRINT ERROR
230   NEXT K                                       ! MESSAGE
240   PRINT                                        !PLACES SPACE BETWEEN THE ERROR
250   !                                             MESSAGE AND END STATEMENT
260   PRINT "END OF SCAN"                          !END OF SEQUENTIAL SCAN
270   STOP
280   !
290   !
300 Error: !                                       !ERROR MESSAGE ROUTINE
310         PRINT
320         PRINT "ERROR DETECTED ON CHANNEL";K
330         PRINT "VOLTAGE READ";I(K)
340         RETURN
350 END
```

Example 2-1A is one of two recommended ways to program this system. It uses a FOR... NEXT loop (lines 140 to 180) to step through the 40 test points in the power supply circuit under test. The A/D reading from each test point is transferred from Multiprogrammer memory into array I after each reading.

Example 2-1B shows a faster way to program the test set. The FOR... NEXT loop is replaced by one program line:

```
150  OUTPUT 723;"IP,R41,15T"
```

The line is identical line 150 of Example 2-1A, except for the repeat instruction R41, which modifies the "IP15" instruction. The instruction makes the IP repeat 41 times. The 41 readings are stored in Multiprogrammer memory. The system controller reads them into 41 elements of array I in line 160:

```
160  ENTER 72301;I(*)
```

Example 2-1B is much faster than Example 2-1A, because only one OUTPUT and one ENTER instruction are executed--Example 2-1A executes each instruction 41 times. The scanning rate in Example 2-1A is approximately 10 milliseconds per channel. The scanning rate in Example 2-1B is approximately 3 milliseconds per channel.

NOTE

Example 2-1B uses the Multiprogrammer's internal Memory, which can store up to about 450 readings. If you use the repeat instruction to take more than 450 readings, you may lose data. Read the 6942A User's Guide for additional information on memory size and the repeat instruction.

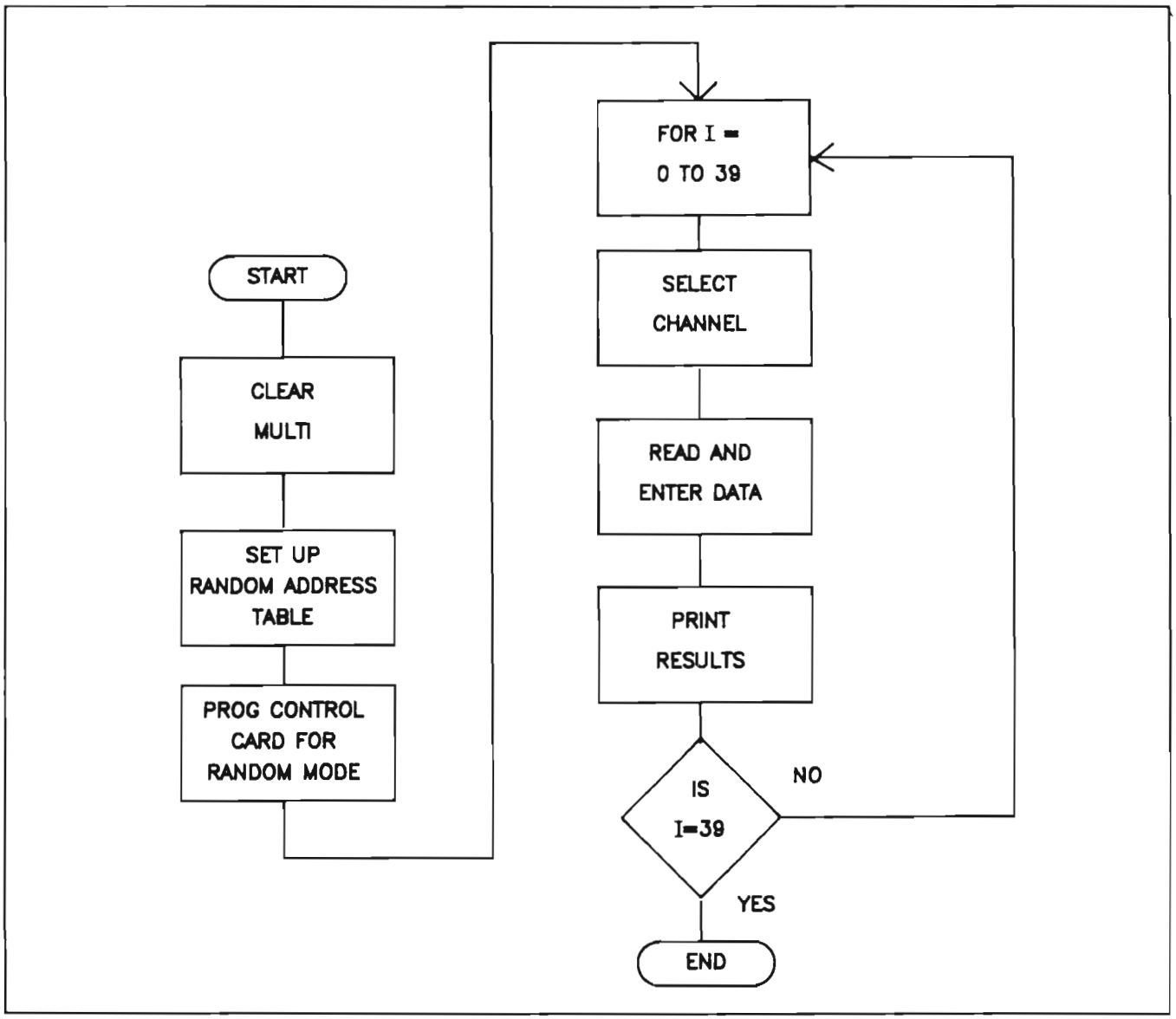


Figure 2-5. Flow Chart, Random Access

2-30 Random Channel Access.

The flow chart for the random access software is shown in Figure 2-5.

2-31 Program Examples. As with the sequential mode examples, these examples include program line numbers. The lines are exerpted from Example 2-2.

```
22 OUTPUT 723;"OP13.3,0T"
```

Line 22 puts the control card in the random access mode. The Output Parallel (OP) instruction writes decimal 0 to subaddress 3, and cycles the card. The instruction programs bit 0 of the Model Select Register to 0. This instruction sets the mode and enables the control card by cycling it. Remember that the card is disabled after power-up or an HP-IB device clear command. The FET switches will not turn on unless the card is enabled. The card wakes up in the random access mode, so it is not necessary to program the random access mode unless the card has been programmed to the sequential scan mode since power-on or a Multiprogrammer Clear.

723	HP-IB select code 7, Multiprogrammer address 23
OP13.3	Writes a 0 to card slot 13, subaddress 3
0	Sets Bit 0, subaddress 3 to 0 for random access mode
T	Multiprogrammer instruction terminator

```
25 OUTPUT 723; "WF13.0,";ADDR(I);"T"
```

Line 25 selects the channel number stored in the array Addr at element (I). The WF instruction writes the number to subaddress 0, which is used to program the next channel in the random access mode. The FET switch for the channel is closed as soon as a number is programmed to subaddress 0.

WF13.0	Writes number to card slot 13, subaddress 0
Addr(I)	Element (I) of the array Addr contains the channel number to be selected.

NOTE

The comma delimiter within the quotes surrounding the command "WF13.0," must be included to separate the command from the data in Addr(I).

```
26 OUTPUT 723;"IP15T"
```

Line 26 signals the A/D converter in slot 15 to take a reading. The digital output of the A/D is stored in the Multiprogrammer memory, so that the system controller can read it back later.

```
27 ENTER 72301;Data(I)
```

Line 27 transfers one A/D reading from the Multiprogrammer memory at HP-IB extended talk address 01 to the arrray Data, element (I).

Example 2-2 scans the 40 transducers at a rate of about 25 milliseconds per channel.

Example 2-2. System Program, Random Access

```
1     !THIS PROGRAM SETS UP A TABLE OF RANDOM
2     !CHANNEL ADDRESSES IN AN ARRAY.THE
3     !PROGRAM THEN SELECTS A CHANNEL TO BE READ
4     !
5     !
6     OPTION BASE 0
7     CLEAR 723                                   !CLEAR MULTI FRAME
8     WAIT 4                                      !WAIT FOR SELF TEST TO END
9     DIM Addr(39),Data(39)
10    FOR I=1 TO 9                                !
11      Addr(I)=I                                 !
12    NEXT I                                      !
13    FOR I=10 TO 19                              !
14      Addr(I)=I+10                              !THIS SECTION FORMS THE TABLE
15    NEXT I                                      !OF RANDOM CHANNEL ADDRESSES
16    FOR I=20 TO 29                              !
17      Addr(I)=I-10                              !
18    NEXT I                                      !
19    FOR I=30 TO 39                              !
20      Addr(I)=I                                 !
21    NEXT I                                      !
22    OUTPUT 723;"OP13.3,0T"                      !ENABLES THE CONTROL CARD AND
23    !                                           !SETS MODE TO RANDOM ACCESS
24    FOR I=0 TO 39                               !LOOP TO READ THE SELECTED
25      OUTPUT 723;"WF13.0,";Addr(I);"T"          !CHANNEL ADDRESSES
26      OUTPUT 723;"IP15T"                        !INITIATE AN A D READING
27      ENTER 72301;Data(I)                       !ENTER READING TO CONTROLLER
28      NEXT I
29      FOR I=0 TO 39
31      PRINT "CHAN";Addr(I),Data(I)              !PRINT THE RESULTS
32      NEXT I
34    !
35    END
```

Example 2-2. Program Results

```
CHAN 0      10.01
CHAN 1      9.51
CHAN 2      9.01
CHAN 3      8.51
CHAN 4      8.01
CHAN 5      7.51
CHAN 6      7.01
CHAN 7      6.505
CHAN 8      6.005
CHAN 9      5.505
CHAN 20     0
CHAN 21    -.505
CHAN 22    -1.005
CHAN 23    -1.505
CHAN 24    -2.01
CHAN 25    -2.51
CHAN 26    -3.015
CHAN 27    -3.515
CHAN 28    -4.02
CHAN 29    -4.52
CHAN 10     5.005
CHAN 11     4.505
CHAN 12     4.005
CHAN 13     3.505
CHAN 14     3.005
CHAN 15     2.505
CHAN 16     2
CHAN 17     1.5
CHAN 18     1
CHAN 19     .5
CHAN 30    -5.025
CHAN 31    -5.525
CHAN 32    -6.03
CHAN 33    -6.53
CHAN 34    -7.035
CHAN 35    -7.535
CHAN 36    -8.04
CHAN 37    -8.54
CHAN 38    -9.04
CHAN 39    -9.545
```

CHAPTER 3
ADVANCED OPERATING TECHNIQUES

3-1 SEQUENTIAL SCANNING WITH BUFFERED A/D

FET scanning systems with high-speed A/D converters can scan at high speed. The system controller may limit the maximum speed of such a system because program run time can be much longer than channel selection and A/D conversion time.

Both scanning systems in the previous chapters depend on the system controller to initiate the scan sequence and read data into the controller memory. Example 2-1B is faster than 2-1A, but still does not take full advantage of the speed of the cards.

When a 69790B Memory card is added to a scanning system, the system controller can transfer the A/D output data to its memory much less often. Instead of transferring data after each A/D reading, or after up to 450 readings, as in Example 2-1B, the controller can wait until up to 4095 conversions have been recorded. Channel selection and A/D conversions can be triggered by the 69750A internal pacer, so the system is independent of program run time between data transfers.

Memory-buffered systems can scan at up to 25kHz when the burst method of data acquistion is used. In the burst method, readings are taken in groups of up to 4095 A/D conversions. Between bursts, the system controller transfers the

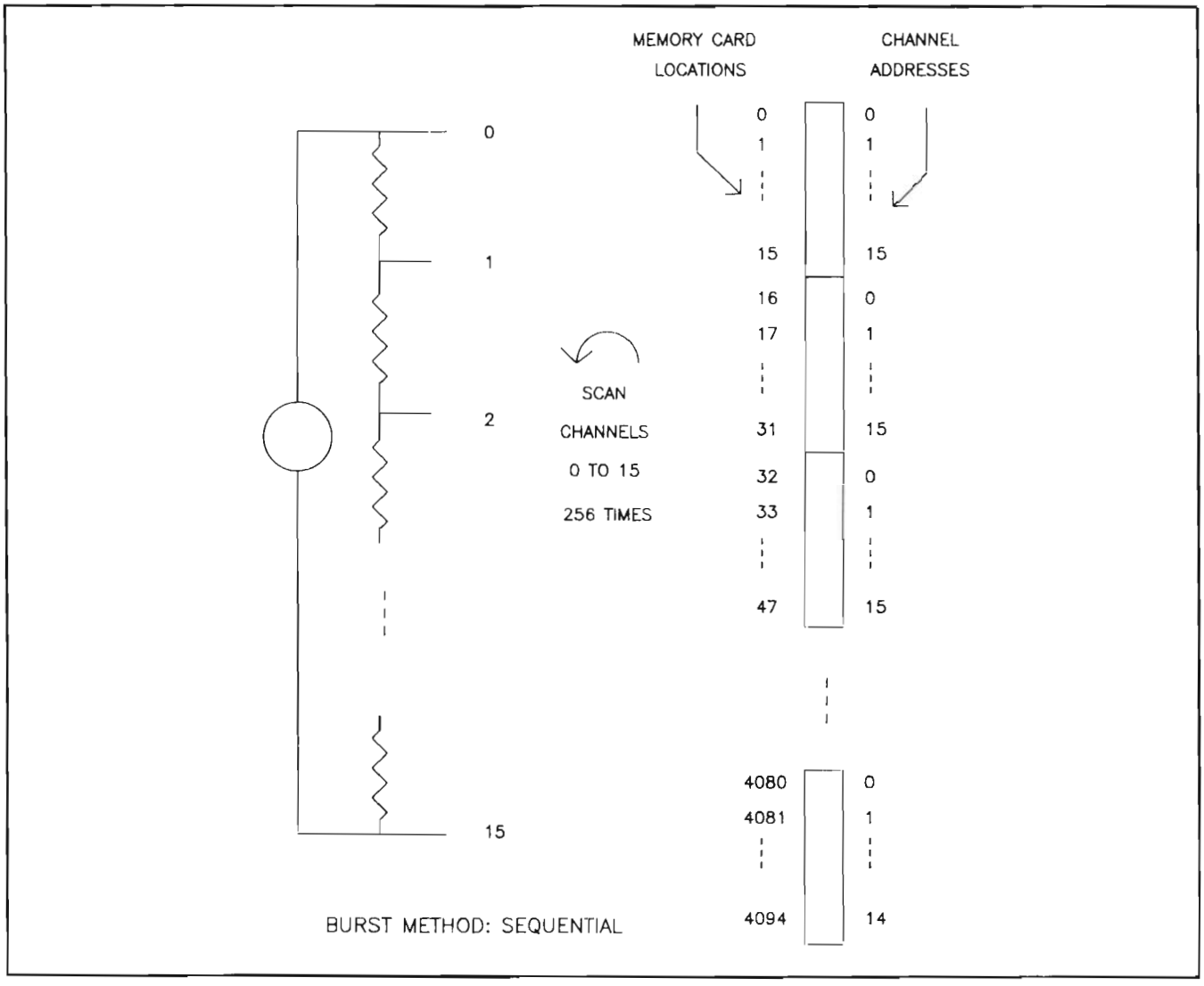


Figure 3-1. Channel Address Allocation, Sequential Scanning

data into its memory. The time between readings in each burst is usually fixed, but the time between bursts can vary, and usually depends on the type of measurement and the system controller readback rate. The number of readings per burst is limited to 4095 by the storage capacity of the 69790B Memory card.

Application Note 316-1 describes the burst mode of data acquisition in more detail. It also describes the continuous mode, which also uses a 69790B card. A memory-buffered A/D in the burst mode is used in the scanning system example in this section. Figure 3-1 shows the scan sequence; Figure 3-2 is a block diagram of the scanner system. The scan control card is set up for sequential scanning with a 64-channel FET card. The memory card is used in the FIFO mode. Channels 0 to 15 are scanned 256 times for a total of 4096 readings in each burst. Memory location 4095 is not available in the FIFO mode, so the last reading (channel 15) of the last scan (number 256) is lost.

3-2 System Considerations

3-3 A/D Converter Set-Up. The 69751A A/D converter is set to accept −10.24 to +10.235 volt input signals. Switches S2-1 and S2-3 are open, and S2-2 is closed, which sets the trigger bypass mode. The card is shipped with S2-1 closed, and S2-2 and S2-3 open. The trigger bypass mode reduces the 13-17 microsecond delay from an external trigger input to the start of a conversion to 1 microsecond. Only external triggers are possible when using the trigger bypass mode.

3-4 Control/Pacer, FET, and Memory Card Set-Up. The 69750A control card, the 69752A FET card, and the 69790B Memory card are used as they are shipped from the factory.

3-5 Sequence of Operations. When it is cycled, the control card pulses the start conversion output which is con-

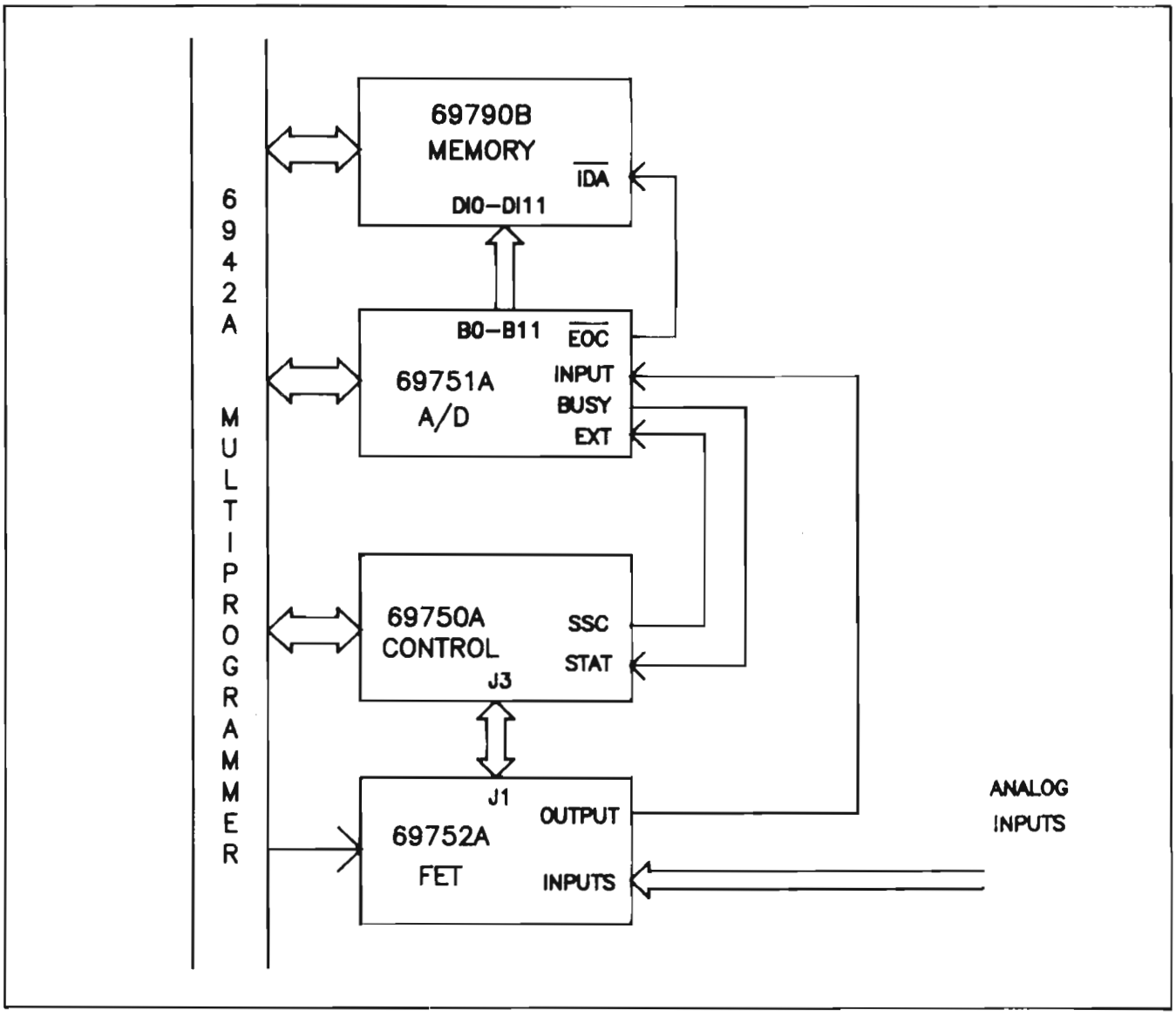


Figure 3-2. Buffered A/D, Sequential Scanning

nected to the A/D converter. The converter then sends a BUSY signal to the control card, which triggers selection of the next channel. The $\overline{EOC}$ output of the converter, connected to the $\overline{Input\ Data\ Available}$ ($\overline{IDA}$) input of the memory card, causes digital output of the A/D to be stored after each conversion. Figure 3-3 shows the timing of each select-convert-storage operation.

3-6 Timing. The programmed pacer period must be long enough for the FET switches and the A/D sample-and-hold amplifier to settle, and for the A/D conversion to complete. The FET switches settle in 10 microseconds, the amplifier settles in 10 microseconds (for this application), and the A/D conversion takes 30 microseconds.

The FET switch settling time can overlap A/D conversion time as shown in Figure 3-3, because the next channel is selected during the conversion. The A/D BUSY signal triggers selection of the next channel after the sample-and-hold amplifier has acquired the signal from the previous channel. The sample-and-hold amplifier settling time does not overlap conversion time because the amplifier samples the next signal only after the previous conversion is complete.

The settling time of the A/D sample-and-hold amplifier is determined by the size of the voltage step between readings, and the accuracy required. As the voltage step and the required accuracy increase, the settling time becomes longer. The A/D converter Instruction Manual gives a settling time of 15 microseconds for a 10 volt step, with an accuracy of 0.01% of the final value. In the example, if a typical accuracy of 0.1% is acceptable, 10 microseconds of settling time is enough. The settling time must be increased if the resistance of any source is higher than 1k ohms.

The pacer period for the example is 40 microseconds (30μs conversion + 10μs settling time). This results in a scanning rate of 25kHz.

3-7 Programming Considerations

3-8 Control Card. The start channel is programmed by writing a decimal 0 to subaddress 0. The stop channel is programmed by writing a decimal 15 to subaddress 1. The on-board pacer is enabled by setting bit 2 of the Mode Select Register to 1. The card is put in the sequential scan mode by

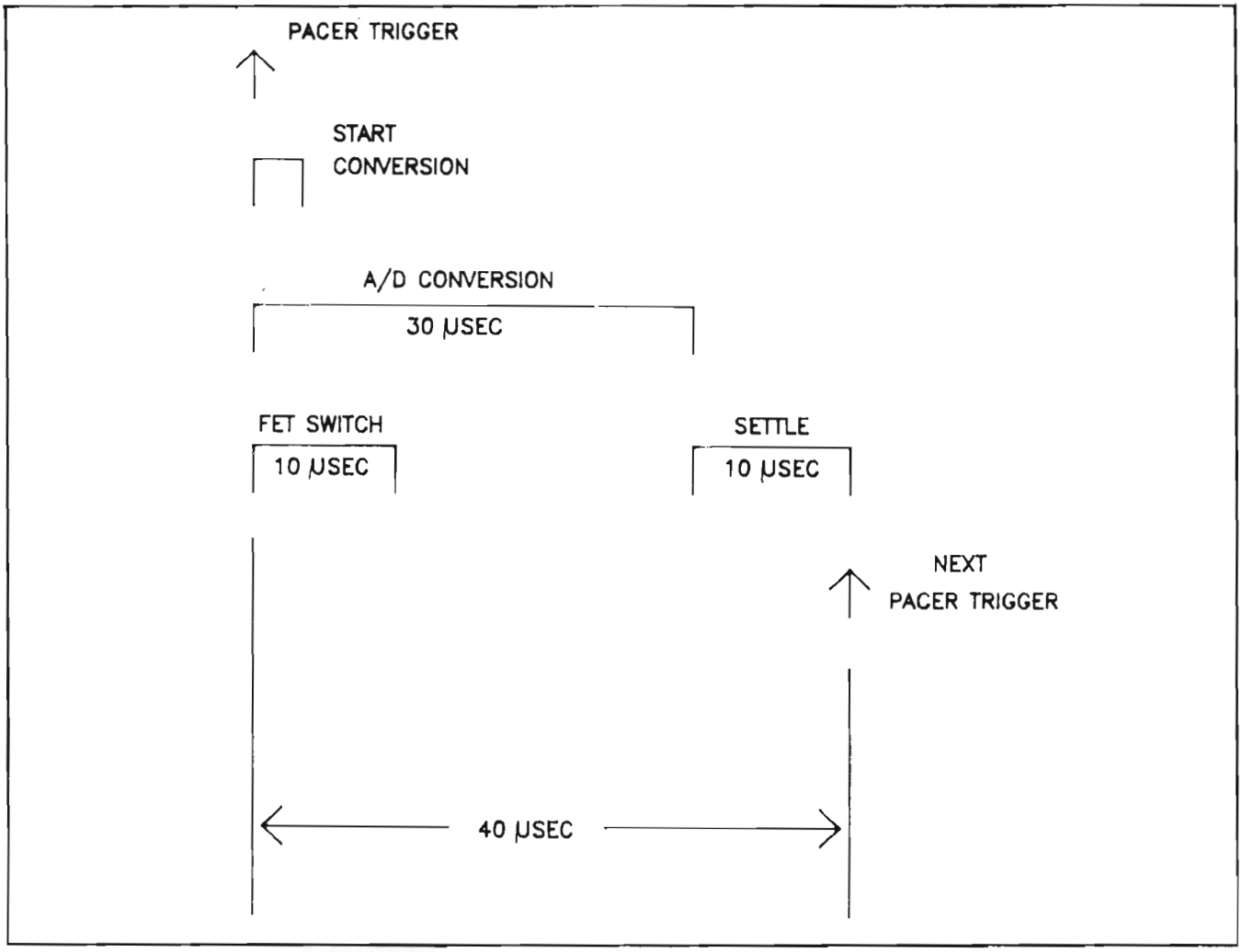


Figure 3-3. Sequence of Operation

setting bit 0 of the Mode Select Register to 1. Bits 0 and 2 of the register are programmed by writing a decimal 5 ($2^0 + 2^2$) to subaddress 3. The pacer is programmed for a 40 microsecond period by writing a decimal 40 to subaddress 2. The pacer period can be programmed in microseconds or milliseconds. The card wakes up with the unit set to microseconds.

The scanning sequence is started when the control card pacer is triggered by the controller with a CY instruction.

3-9 Memory Card. The memory card is described in its Instruction Manual and in Application Note 316-1. The 69790B actually consists of two cards. Sometimes the cards are programmed independently, but most of the time they can be considered one card.

The card can store 4096 16-bit data words in the recirculating mode, and 4095 words in the FIFO mode. The example uses the card in the FIFO mode, which means that the system controller reads data from the card in the same order that it is stored on the card from the A/D converter. For example, 1000 data words (a1, A2,... A1000) are stored in locations 1,2,...1000. When the controller reads them from the card, it reads a1 first, then a2, and so on.

If more than 4095 readings will be stored, then the controller must read data words from memory at least as fast as they are stored, or the memory will become full. When it is full, no new data can be stored. Any data sent to the card is lost. The memory card can be programmed to generate an interrupt when the number of stored data words is greater than the number programmed to the reference register. The Arm Card (AC) instruction programs the card to interrupt. The differential counter keeps track of the difference of the number of words stored and the number of words read back. An interrupt can be generated when the number in the differential counter is greater than the number in the reference register.

In this application the memory card is used in the FIFO input mode. Programming a Clear Card, (CC), instruction to the memory card will reset the read pointer, write pointer and differential counter, and will put the card in the FIFO input mode. In the input mode, data placed on the external memory data lines from the A/D will be stored on the card when the $\overline{EOC}$ output of the A/D strobes the $\overline{IDA}$ input of the memory card.

The reference register is programmed by writing decimal number 4094 to subaddress 0 of memory card 2. The memory card will generate an interrupt when the write pointer is set to 4095 if no words have been read from the card. The last word will be written to location 4095 during the time it takes for the controller to respond to the interrupt.

3-10 MR Instruction. The MR instruction may be used to speed up the transfer rates from the memory card to the controller. The instruction requires that a special program be loaded into Multiprogrammer memory prior to running the system program. The file is described in the system program shown in Example 3-1.

3-11 Interrupt Routine. The Multiprogrammer is polled to determine whether or not it generated an interrupt. Its status is read to see if the memory card generated an armed card interrupt.

The card is then disarmed and set to the FIFO input mode with external lockout. The external lockout mode, which inhibits handshakes and stops the memory card from accepting new data from the A/D, is set by writing a decimal 21 to subaddress 1 of memory card 1. If the card is not placed in the lockout mode, and data is read from memory such that the memory card is no longer in the full condition, then any handshaking will cause the memory card to take in new data. This could disrupt the readback sequence. The card is disarmed by the Disarm Card (DC) instruction, which prevents any interrupts until the card is armed again at the start of a new sequence.

Next, the pacer on the 69750A control card is turned off by writing 0 to subaddress 2. This stops the scanning sequence and ensures that there will be no handshakes between the control card and A/D or between the A/D and memory card until the control card is cycled.

The Memory Read (MR) instructions sets the system up for rapid transfer of data from the memory card to the controller. The data is read from the memory card by entering the data into the controller in two's complement format as it was stored by the A/D converter. Since the A/D converter has a 12-bit resolution, the decimal representation extends from -2048 to $+2047$. The controller stores the decimal representation of each data word in an array.

The A/D converter is used in the ± 10 volt range, so the least significant bit is equal to 0.005 volts. The system program shown in Example 3-1 multiplies the data in the input array by 0.005 to convert to voltage values, and stores it in another array. The data is then plotted and the program returns to the main routine. In this case, a softkey labeled "CONTINUE" allows additional runs of the program.

Figure 3-4 is the flow chart for the system program, and Example 3-1 is the program. Figure 3-5 is a plot for a sample scan.

3-12 BUFFERED A/D WITH RANDOM CHANNEL ACCESS

The high speed buffered A/D system from Paragraph 3-1 may be expanded to include another memory card which contains a table of channel addresses. Such a system is used where sequential scanning is not convenient. For example, it may be necessary to change the scanning order for part of the scan, while keeping the rest of the scan the same. It is easier to change software than to change a hard-wired system configuration.

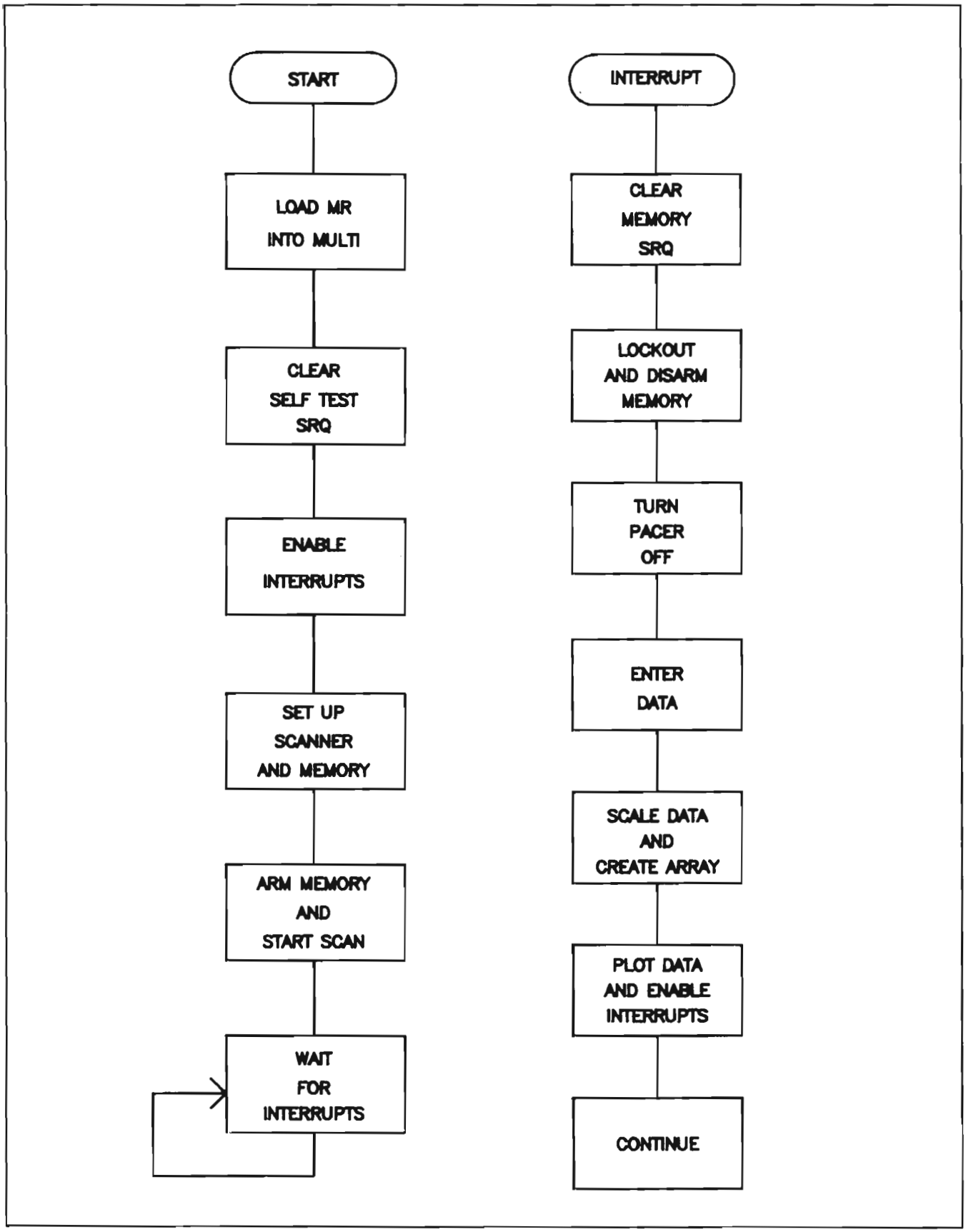


Figure 3-4. Flow Chart, Buffered A/D, Sequential Scanning

Example 3-1. System Program, Buffered A/D, Sequential Scanning

```
10    ! THIS PROGRAM DOES A HIGH SPEED SEQUENTIAL
20    !   FET SCAN USING THE BUFFERED A/D TO TAKE
30    !   A BURST OF READINGS
40    !
50    !
60    OPTION BASE 0
70    DIM Data_scan(4094),Volts(4094)
80    ASSIGN @Multi TO 723
90    CLEAR 723                                    !CLEARS MULTI FRAME
100   WAIT 4                                       !WAIT FOR SELF TEST TO END
110   ALLOCATE Ascii$[80] !*********************!
120   ASSIGN @Disc TO "MRZ"                        !
130   ON END @Disc GOTO Eof                        !
140 Rd_file:  ENTER @Disc;Ascii$                   !THIS ROUTINE TRANSFERS THE
150           OUTPUT @Multi;Ascii$                 !MRZ FILE FROM THE DISC
160           GOTO Rd_file                         !TO MULTI MAINFRAME MEMORY
170 Eof:   OFF END @Disc                           !
180        ASSIGN @Disc TO *                       !
190        DEALLOCATE Ascii$                       !
200   G=SPOLL(723)  !***************************!PERFORMS AN HPIB SERIAL POLL
210   IF G<>64 THEN                                !THEN CHECKS TO SEE IF THE
220      PRINT "MULTI DIDN'T INTERRUPT"            !MULTI SET SRQ ,IF NOT PRINT
230      PAUSE                                     !ERROR MESSAGE AND PAUSE
240   END IF
250      ENTER 72310;A                             !READ SRQ STATUS TO SEE IF SELF
260   IF A<>16384 THEN                             !TEST SET SRQ,IF NOT PRINT
270      PRINT "SELF TEST DIDN'T SET SRQ"          !ERROR MESSAGE AND PAUSE
280      PAUSE
290   END IF
300   ON INTR 7 GOTO Interrupt                     !SET UP INTERRUPT BRANCH
310   ENABLE INTR 7;2                              !ENABLE INTERRUPT
320   OUTPUT @Multi;"CY2T"                         !ENABLE CONTROL CARD
330 Continue:   !*********************************!
340   OFF KEY                                      !
350   OUTPUT @Multi;"WF2.0,0T"                     !SELECT START CHAN
360   OUTPUT @Multi;"WF2.1,15T"                    !SET STOP CHANNEL
370   OUTPUT @Multi;"WF2.3,5T"                     !SET MODE REGISTER
380   OUTPUT @Multi;"WF2.2,40T"                    !SET PACER DELAY IN us
390   OUTPUT @Multi;"CC8T"                         !CLEAR MEMORY REGISTERS
400   OUTPUT @Multi;"WF8.0,4094T"                  !SET INTERRUPT WORD
410   OUTPUT @Multi;"AC8T"                         !ARM THE MEMORY CARD
420   OUTPUT @Multi;"CY2T"                         !START PACER
430 Wait:   !************************************!WAIT FOR INTERRUPT
440         DISP "WAITING FOR INTERRUPT"
450         GOTO 430
460 Interrupt: !*********************************!INTERRUPT ROUTINE
470      G=SPOLL(723)                              !PERFORMS AN HPIB SERIAL POLL
480      IF G=64 THEN                              !THEN CHECKS TO SEE IF MULTI
490         ENTER 72310;A,B,C                      !SET SRQ (ALSO CLEARS SRQ)
500         IF C<>0 THEN                           !READ SRQ STATUS TO SEE THAT A
510            ENTER 72312;Address                 !CARD CAUSED THE INTERRUPT
520            IF Address<>8 THEN                  !CHECK THE ADDRESS OF THE CARD
530              PRINT "NOT A MEMORY ADDRESS"      !IF NOT THE RIGHT ADDRESS THEN
540              PAUSE                             !PRINT ERROR MESSAGE AND PAUSE
550            END IF
560            OUTPUT @Multi;"WF7.1,21T"           !SET FIFO IN MODE WITH EXTERNAL
570            !                                    LOCKOUT TO STOP HANDSHAKES
580            OUTPUT @Multi;"DC8T"                !DISARM CARD TO AVOID INTERRUPT
590            OUTPUT @Multi;"WF2.2,0T"            !TURN OFF THE PACER
600            OUTPUT @Multi;"MR7,4095T"           !MR COMMAND TO GET THE DATA
610            ENTER 72305 USING "%,W";Data_scan(*)!ENTER AND FORMAT THE DATA
620         ELSE !
630           PRINT "SRQ NOT SET BY ARMED CARD"
640           PAUSE
650         END IF
660      ELSE!
```

Example 3-1. System Program, Buffered A/D, Sequential Scanning (cont.)

```
670         PRINT "MULTI DIDN'T INTERRUPT"
680         PAUSE
690       END IF
700     DISP "UPDATING ARRAY"
710     FOR P=0 TO 4094 !*************************CONVERTS THE DATA TO A VOLTAGE
720     Volts(P)=.005*Data_scan(P)                 !MULTIPLY BY THE LSB VALUE
730     NEXT P
740 Plot: !*************************************PLOT ROUTINE
750     ALPHA OFF                                  !THIS PORTION OF THE PLOT
760     GINIT                                      !ROUTINE SETS UP THE CRT WITH
770     GRAPHICS ON                                !AXIS,LABELS AND LEAVES SPACE
780     GCLEAR                                     !FOR THE SPECIAL FUNCTION
790     MOVE 0,95                                  !KEY LABELS
800     CSIZE 4,.6
810     LABEL "VOLTS"
820     MOVE 100,20
830     CSIZE 5,.6
840     LABEL "TIME"
850     VIEWPORT 0,125,25,95
860     WINDOW 0,133,0,100
870     AXES 10,10,0,50
880     FOR I=0 TO 15 !****************************!THIS PORTION OF THE PLOT
890       X=0                                      !ROUTINE SCALES THE DATA AND
900       Y=Volts(I)*5                             !SORTS EACH CHANNEL FROM THE
910       PEN -1                                   !ARRAY. EACH CHANNEL IS
920       MOVE X,Y                                 !PLOTTED USING ALL OF THE
930       PEN 1                                    !256 DATA POINTS, EXCEPT THE
940       FOR J=0 TO 255                           !LAST CHANNEL WHICH USES 255
950         X=J/2                                  !DATA POINTS.
960         IF I<>15 OR J<>255 THEN
970           Y=Volts(J*16+I)*5
980           DRAW X,Y+50
990         END IF
1000      NEXT J
1010    NEXT I
1020    ENABLE INTR 7;2                            !RE-ENABLE INTERRUPT
1030 Done:  !INTERRUPT ROUTINE COMPLETE
1040    ON KEY 0 LABEL "CONTINUE" GOTO Continue
1050 Idle: GOTO Idle
1060 !
1070 END
```

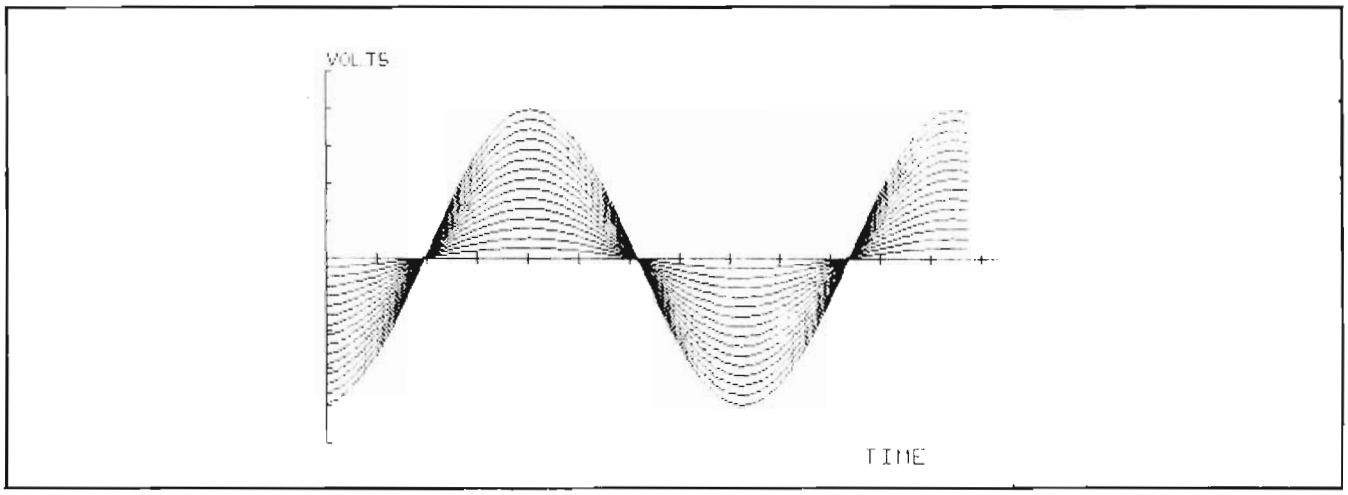


Figure 3-5. Plotted Data

This system uses the burst method of operation with the random access scanning mode. The system configuration is similar to the system described in Paragraph 3-1, but for the additional memory card, which contains the list of addresses for channel selection.

The control card is set to select the next channel address from the external input lines. The memory card which holds the table of addresses is loaded with 64 words representing channel addresses 0 through 31 and then 31 through 0. The memory card read pointer returns to location 0 after location 63 has been read. The data from the A/D is stored in the other memory card in the order it is scanned (channels 0 through 31, 31 through 0, 0 through 31, and so on) until 4095 locations have been filled. Figure 3-6 shows the scanning sequence and the relation between the storage memory card locations and the data from each channel address. Figure 3-7 is the system block diagram.

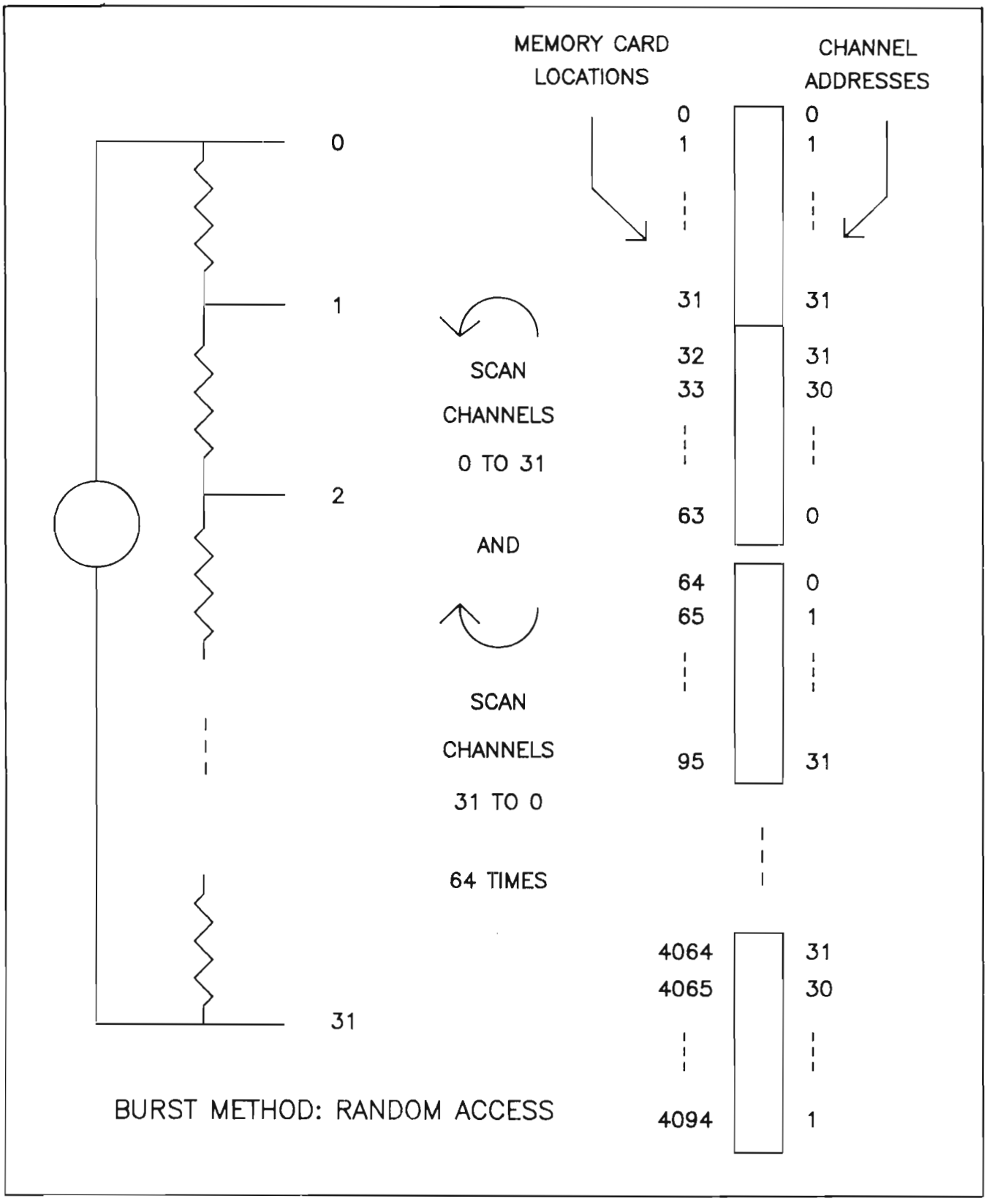


Figure 3-6. Channel Address Allocation, Random Access

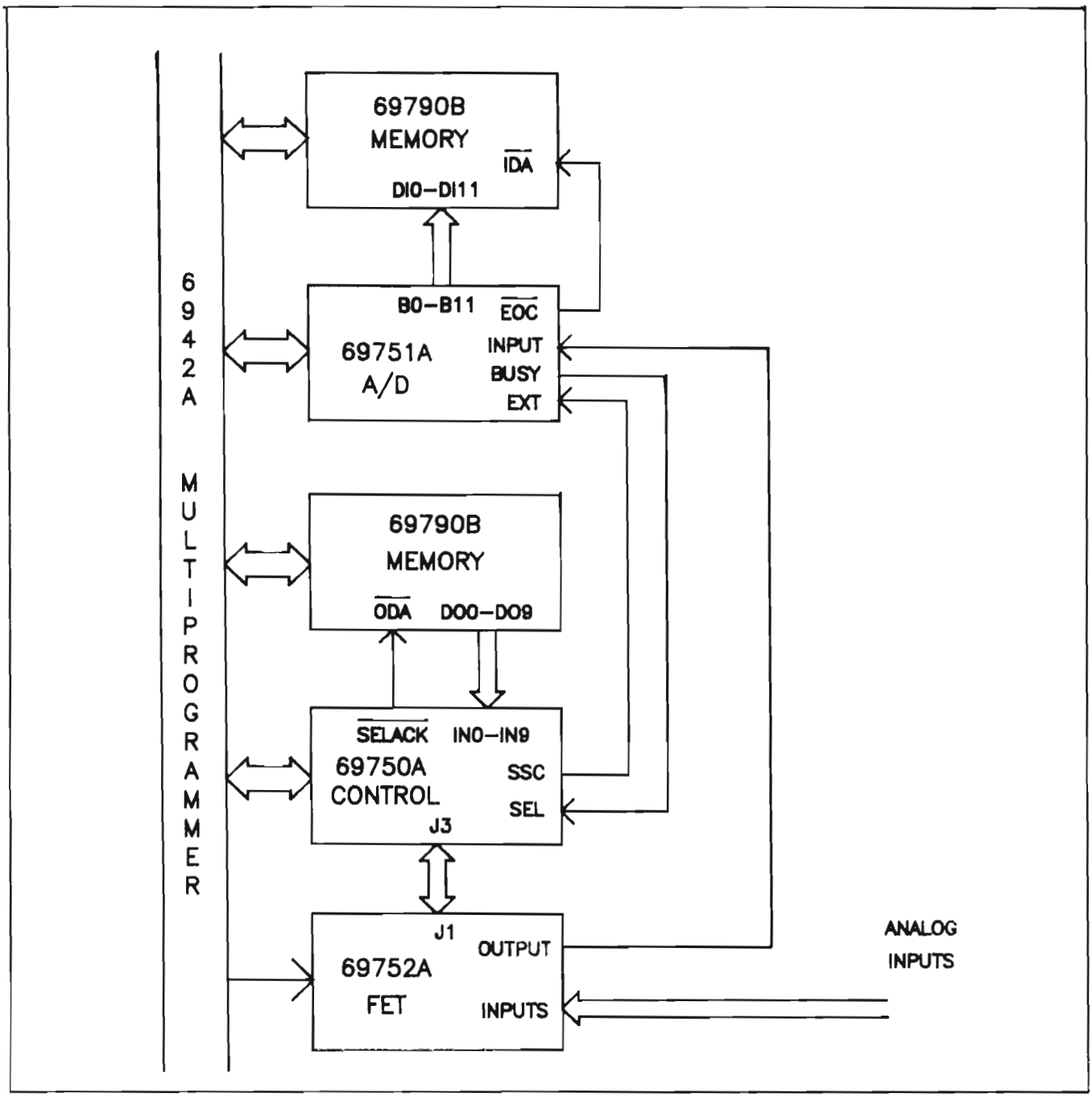


Figure 3-7. Buffered A/D, Random Access

3-13 System Considerations

3-14 **Set-Up.** The system configuration is shown in Figure 3-7. The only differences between this system and the one described in Paragraph 3-1 are the additional memory card and its connections, and the BUSY line from the A/D converter, which is connected to the SELECT (SEL) input of the control card instead of the STATUS (STAT) input.

The Select Acknowledge (SELACK) output of the control card is connected to the Output Data Accepted (ODA) input of the address table memory card. The 10 least significant bits of memory card output are connected to the 10 external address selection inputs of the control card.

The control card, FET card and memory cards are used as shipped from the factory. The A/D converter card is used in the trigger bypass mode described in Paragraph 3-3.

3-15 **Timing Considerations.** The timing considerations are similar to those in Paragraph 3-6. The only difference is that an additional 6 microseconds is required for transferring channel address data from the memory card to the control card. Referring to Figure 3-3, the additional time must be add-

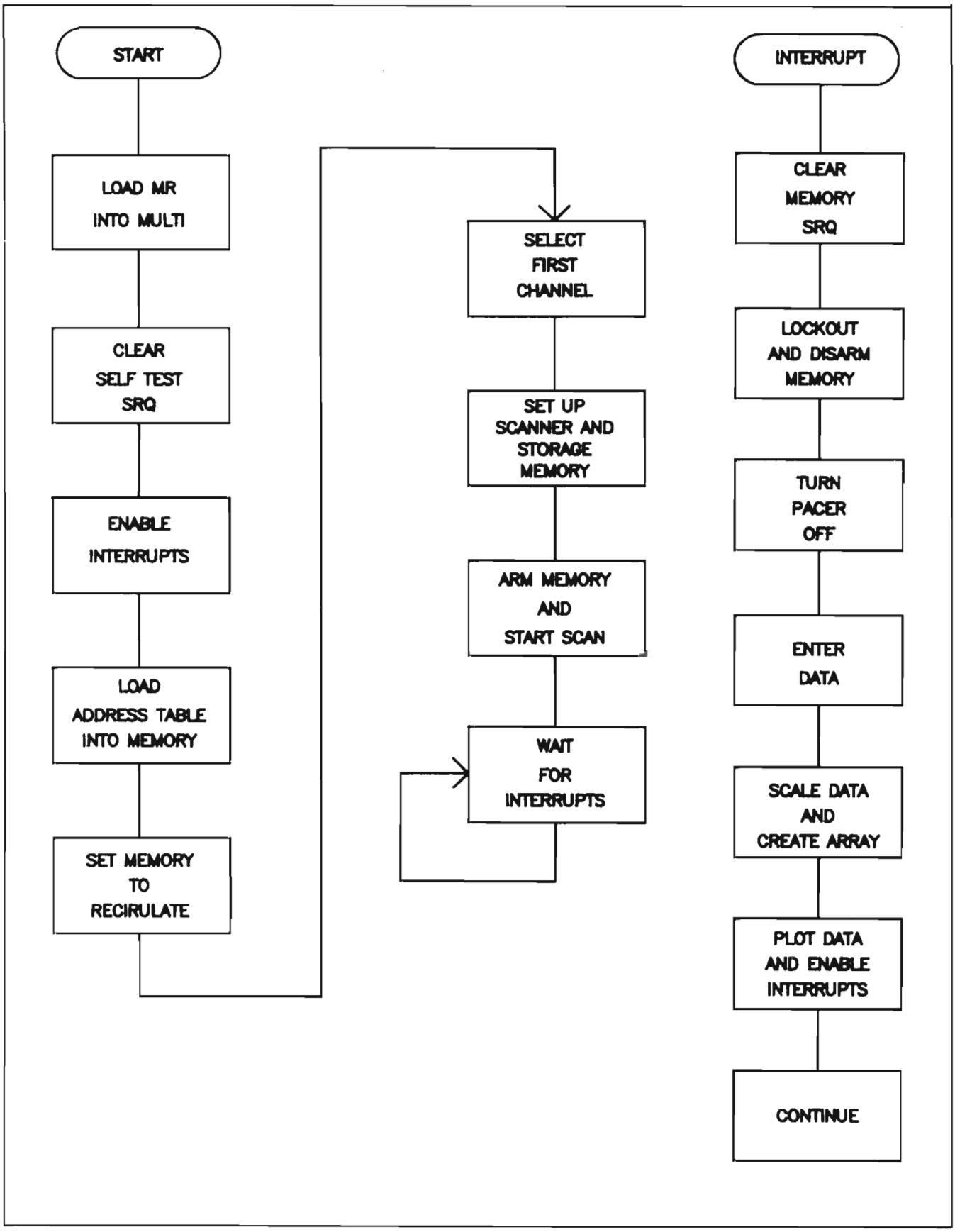


Figure 3-8. Flow Chart, Buffered A/D, Random Access

ed to the FET switch settling time of 10 microseconds to obtain a total of 16 microseconds. The 16 microsecond total is still within the A/D conversion time of 30 microseconds, so the switch and memory settling times can overlap the conversion time as described in Paragraph 3-6. This system uses a pacer period of 40 microseconds.

3-16 Programming Considerations

3-17 Control Card. The control card is enabled by cycling it with a CY instruction. Then the internal channel select mode is programmed by writing a 0 to the Mode Select Register (subaddress 3). The first channel to be selected is programmed by writing its decimal address to subaddress 0. The control card is then put in the random access mode with external address select and the internal pacer mode is set, by programming bit 2 (internal pacer mode) and bit 9 (external address select) of subaddress 3 to logic 1. Subaddress 3 is programmed by writing decimal 516 (2^2+2^9) to subaddress 3. The pacer period of 40 microseconds is programmed by writing decimal 40 to subaddress 2.

3-18 Storage Memory Card. The memory card used to store data from the A/D converter is programmed as described in Section 3-9. It is set to the FIFO input mode by a Clear Card (CC) instruction. Its reference register is programmed to interrupt after 4094 values have been stored by writing 4094 to subaddress 0 of memory card 2.

3-19 Address Table Memory Card. The memory card used to supply channel addresses to the control card contains an array for storing the addresses. The array has 64 elements, which hold the numbers 0 through 31 and 31 through 0 (the channel address numbers in the order of the scan). The read and write pointers are set to 0 and the card is set to the FIFO input mode (use a Clear Card (CC) instruction). The data is stored in the array with the Memory Output (MO) instruction, which also sets the card to the FIFO output mode.

Next, the card is programmed for recirculating output, with the reference word programmed to truncate the memory at 63 words. This causes the read pointer to return to 0 after location 63 has been read. The table of addresses stored in locations 0 to 63 will repeat until all 4095 locations of the storage memory card have been filled. The card is set to the recirculating output mode by sending decimal 10 to subaddress 1 of memory card 1. The reference word is programmed by writing decimal 63 to subaddress 0 of memory card 2.

The read pointer must be initially set to 1, which causes the second channel address to be selected after the sequence is initiated. This is because the first channel has been selected before the sequence begins. After the A/D converter takes the first reading, the BUSY signal triggers selection of the next channel. The flow chart for the system program is shown in Figure 3-8, and the system program is shown in Example 3-2.

A plot of the results of the scanning sequence is shown in Figure 3-9. The voltage dividers which were scanned were supplied with a dc voltage of +8 and −7.5 volts.

Example 3-2. System Program, Buffered A/D, Random Access

```
10    ! THIS PROGRAM DOES A HIGH SPEED RANDOM FET SCAN USING THE
20    !  BUFFERED A/D TO TAKE A BURST OF READINGS
30    !  THE RANDOM CHANNELS ARE PROGRAMMED IN AN ARRAY
40    !
50    ! MEMORY CARDS IN SLOTS 4&5 ARE USED FOR STORAGE OF ADDRESS SELECTIONS
60    ! MEMORY CARDS IN SLOTS 7&8 ARE USED FOR DATA ACQUISITION
70    !
80    !
90    OPTION BASE 0
100   DIM Data_scan(4094),Volts(4094)
110   INTEGER Address(63)
120   ASSIGN @Multi TO 723
130   CLEAR 723                                  !CLEARS THE MULTI
140   WAIT 4                                     !WAIT FOR SELF TEST TO END
150   ALLOCATE Ascii$[80] !**********************!
160   ASSIGN @Disc TO "MRZ"                      !
170   ON END @Disc GOTO Eof                      !
180 Rd_file:  ENTER @Disc;Ascii$                 !THIS ROUTINE TRANSFERS THE
190           OUTPUT @Multi;Ascii$               !MRZ FILE FROM THE DISC TO
200           GOTO Rd_file                       !MULTI MAINFRAME MEMORY
210 Eof:  OFF END @Disc                          !
220       ASSIGN @Disc TO *                      !
230       DEALLOCATE Ascii$                      !
240   G=SPOLL(723)  !****************************!PERFORMS AN HPIB SERIAL POLL,
250   IF G<>64 THEN                              !THEN CHECKS TO SEE IF THE
260      PRINT "MULTI DIDN'T INTERRUPT"          !MULTI SET SRQ, IF NOT PRINT
270      PAUSE                                   !ERROR MESSAGE AND PAUSE
280   END IF
290   ENTER 72310;A
300   IF A<>16384 THEN                           !READ SRQ STATUS TO SEE IF SELF
310      PRINT "SELF TEST DIDN'T SET SRQ"        !TEST SET SRQ,IF NOT PRINT
320      PAUSE                                   !ERROR MESSAGE AND PAUSE
330   END IF
340   ON INTR 7 GOTO Interrupt                   !SET UP INTERRUPT BRANCH
350    ENABLE INTR 7;2                           !ENABLE INTERRUPT
```

Example 3-2. System Program, Buffered A/D, Random Access (cont.)

```
360   !*****************************************!THIS SECTION SETS UP THE
370    FOR J=0 TO 31                            !MEMORY WITH ADDRESS DATA
380      Address(J)=J                           !ADDRESSES 0-31,THEN 31-0 WILL
390      Address(32+J)=31-J                     !BE LOADED INTO MEMORY
400    NEXT J
410    OUTPUT @Multi;"CC5T"                     !CLEAR MEMORY CARD
420    OUTPUT @Multi;"M0,4,";Address(*);"T"     !SET FIFO OUTPUT MODE AND LOAD
430    !                                        !THE TABLE OF ADDRESSES
440    OUTPUT @Multi;"CC5T"                     !RESET THE READ,WRITE POINTERS
450    OUTPUT @Multi;"WF4.1,10T"                !SET TO RECIRC OUTPUT MODE
460    OUTPUT @Multi;"WF5.0,63T"                !SET REF WORD TO LAST LOCATION
470    !                                        !BEFORE RECIRCULATING
480    !*****************************************!THIS SECTION SETS UP SCAN AND
490    !                                        !MEM CARD FOR DATA ACQUISITION
500    OUTPUT @Multi;"CY2T"                     !ENABLE CONTROL CARD
510 Continue: !                                 !
520   OFF KEY                                   !
530   GCLEAR                                    !CLEAR GRAPHICS
540   OUTPUT @Multi;"WF2.3,0T"                  !ENABLE INTERNAL CHAN SELECT
550   OUTPUT @Multi;"WF2.0,";Address(0);"T"     !SELECT THE FIRST CHAN ADDRESS
560   OUTPUT @Multi;"WF2.3,516T"                !SET MODE REGISTER
570   OUTPUT @Multi;"WF2.2,40T"                 !SET PACER DELAY IN uS
580   OUTPUT @Multi;"CC8T"                      !CLEAR MEMORY REGISTERS
590   OUTPUT @Multi;"WF8.0,4094T"               !SET INTERRUPT WORD
600   OUTPUT @Multi;"WF5.3,1T"                  !SET READ PTR FOR 2ND CHAN ADDR
610   OUTPUT @Multi;"AC8T"                      !ARM THE MEMORY CARD
620   OUTPUT @Multi;"CY2T"                      !START PACER
630 Wait:  !*************************************!WAIT LOOP
640        DISP "WAITING FOR INTERRUPT"
650        GOTO Wait
660 Interrupt: !*********************************!INTERRUPT ROUTINE
670     G=SPOLL(723)                             !PERFORMS AN HPIB SERIAL POLL
680     IF G=64 THEN                             !THEN CHECKS TO SEE IF MULTI
690        ENTER 72310;A,B,C                     !SET SRQ (ALSO CLEARS SRQ)
700        IF C<>0 THEN                          !READ SRQ STATUS TO SEE THAT A
710           ENTER 72312;Card_slot              !CARD CAUSED THE INTERRUPT
720           IF Card_slot<>8 THEN               !CHECK THE ADDRESS OF THE CARD
730             PRINT "NOT THE MEMORY CARD"      !IF NOT THE RIGHT ADDRESS THEN
740             PAUSE                            !PRINT ERROR MESSAGE AND PAUSE
750           END IF
760           OUTPUT @Multi;"WF7.1,21T"          !SET FIFO IN MODE WITH EXTERNAL
770           !                                  !LOCKOUT TO STOP HANDSHAKES
780           OUTPUT @Multi;"DC8T"               !DISARM CARD TO AVOID INTERRUPT
790           OUTPUT @Multi;"WF2.2,0T"           !TURN OFF THE PACER
800           OUTPUT @Multi;"MR7,4095T"          !GET DATA USING THE MR COMMAND
810           ENTER 72305 USING "%,W";Data_scan(*)! ENTER AND FORMAT THE DATA
820        ELSE !
830          PRINT "SRQ NOT SET BY ARMED CARD"
840          PAUSE
850        END IF
860     ELSE!
870       PRINT "MULTI DIDN'T INTERRUPT"
880       PAUSE
890     END IF
900   DISP "UPDATING ARRAY"
910   FOR P=0 TO 4094 !*************************!CONVERTS THE DATA TO A VOLTAGE
920   Volts(P)=.005*Data_scan(P)                 !BY MULTIPLYING BY THE LSB
930   NEXT P                                     !VALUE
940 Plot: !*************************************!PLOT ROUTINE
950   ALPHA OFF                                  !THIS PORTION OF THE PLOT
960   GINIT                                      !ROUTINE SETS UP THE CRT WITH
970   GRAPHICS ON                                !AXIS,LABELS AND LEAVES SPACE
980   GCLEAR                                     !FOR THE SPECIAL FUNCTION KEY
990   MOVE 0,95                                  !LABELS
1000  CSIZE 4,.6
1010  LABEL "VOLTS"
1020  MOVE 100,20
1030  CSIZE 5,.6
1040  LABEL "SEQUENCE"
1050  VIEWPORT 0,125,25,95
```

Example 3-2. System Program, Buffered A/D, Random Access (cont.)

```
1060  WINDOW 0,133,0,100
1070  AXES 10,10,0,50
1080  FOR I=0 TO 127 !*************************!THIS PORTION OF THE PLOT
1090   X=I*.75                                  !ROUTINE SCALES THE DATA AND
1100   Y=Volts(I*32)*5                          !SORTS EACH CHANNEL FROM THE
1110   PEN -1                                   !ARRAY.EACH CHANEL IS PLOTTED
1120   MOVE X,Y+50                              !USING ALL OF THE 256 DATA
1130   PEN 1                                    !POINTS, EXCEPT THE LAST
1140    FOR J=0 TO 31                           !CHANNEL WHICH USES 255 DATA
1150     X=I*.75+J                              !POINTS.
1160     IF I<>127 OR J<>31 THEN
1170      Y=Volts(32*I+J)*5
1180      DRAW X,Y+50
1190     END IF
1200    NEXT J
1210  NEXT I
1220  ENABLE INTR 7;2                          !RE-ENABLE INTERRUPT
1230 Done:  !INTERRUPT ROUTINE COMPLETE
1240  ON KEY 0 LABEL "CONTINUE" GOTO Continue
1250 Idle:  GOTO Idle
1260  END
```

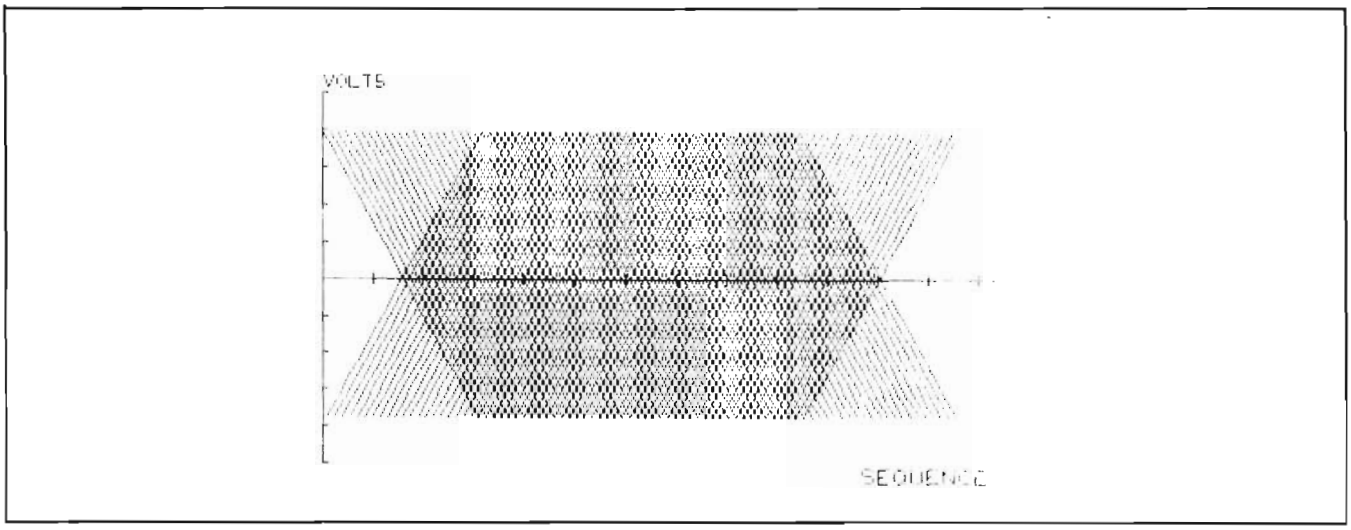


Figure 3-9. Plotted Data

APPENDIX A
POWER BUDGET CONSIDERATIONS

The 6942A mainframe and 6943A extender each have unisolated +5 volt and ±12 volt power supplies, and three isolated ±18 volt power supplies for use in systems requiring isolation between the I/O cards. The current available to the I/O cards from these power supplies is shown in Table A-1.

Table A-1. Mainframe Power Availability

Power Supply	Currently Available To I/O cards
+5 V	12.8 A
+12 V −12 V	2.0 A 1.5 A
+18 V No. 1 −18 V No. 1	1.0 A 0.6 A
+18 V No. 2 −18 V No. 2	0.4 A 0.25 A
+18 V No. 3 −18 V No. 3	0.2 A 0.15 A

Table A-2. I/O card +5 Current Requirements

I/O Card	+5 V Current
69770A Isolated Digital Input 69771A Digital Input/Comparator	350 mA
69720A D/A Voltage Converter 69721A D/A Current Converter 69731B Digital Output 69751A A/D Converter 69755A 16 Channel FET 69776A Interrupt	400 Ma
69752A 64 Channel FET	425 mA
69700A Thru 69706A Resistance Output	650 mA
69709A Power Supply Control 69735A Pulse Train Output 69736A Timer/Pacer 69775A Counter/Totalizer	750 mA
69790B Memory (Standard, 4K) (Each memory card occupies 2 slots)	1.2 A
69750A Control	1.6 A

The current required by each I/O card from the +5 V supply is listed in Table A-2. The total current load drawn from the +5 V supply by any combination of I/O cards must not exceed 12.8 A. Card slots must be left vacant, if necessary, to ensure this. The 69750A Scan Control/Pacer card draws 1.6 A which is twice the current allocated for each card slot (12.8A/16 slots = 0.8A/slot).

The current drawn by each of the I/O cards from the ±18 volt supply is shown in Table A-3. The currents drawn from any of the supplies must not exceed the limits given in Table A-1. Since all cards are shipped from the factory with Supply No. 1 connected by jumpers, some cards may have to be changed to Supply No. 2 or No. 3 to meet these current constraints. If several cards must be isolated, then they should be connected to different supplies.

Table A-3. I/O Card ±18 V Current Requirements

I/O Card	±18 V Current	−18 V Current
69755A 16 Channel FET	45 mA	20 mA
69752A 64 Channel FET	60 mA	40 mA
69720A D/A Voltage Converter	80 mA	40 mA
69721A D/A Current Converter	110 mA	60 mA
69751A A/D Converter	150 mA	80 mA
69775A Counter/Totalizer *	120 mA	15 mA

* This card is shipped from the factory with the unisolated ±12 V supply connected. Jumpers on the card can select one of the isolated ±18 V supplies if required.

Figure A-1 shows how the ±18 V supplies may be selected with the jumper options.

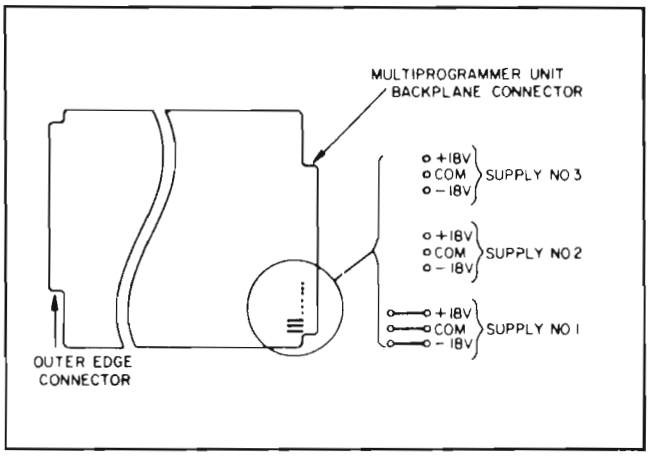


Figure A-1. I/O ±18 V Supply Selection

APPENDIX B
EDGE CONNECTORS AND WIRING

Connections to the A/D converter card are made on the edge connector shown in Figure B-1. The connections to the A/D converter card for the FET scanner application described in Paragraph 2-2, Figure 2-1 are also shown.

The edge connector of card 1 of the pair of 69790B Memory cards is shown in Figure B-2. The connections between the memory card and the A/D converter for the application described in Paragraph 3-1, Figure 3-2 are shown in Figure B-3.

Bits 12 through 15 are connected to bit 11 to allow data transfer in the 2's complement format from the 12 bit A/D converter output to the 16 bit memory card input.

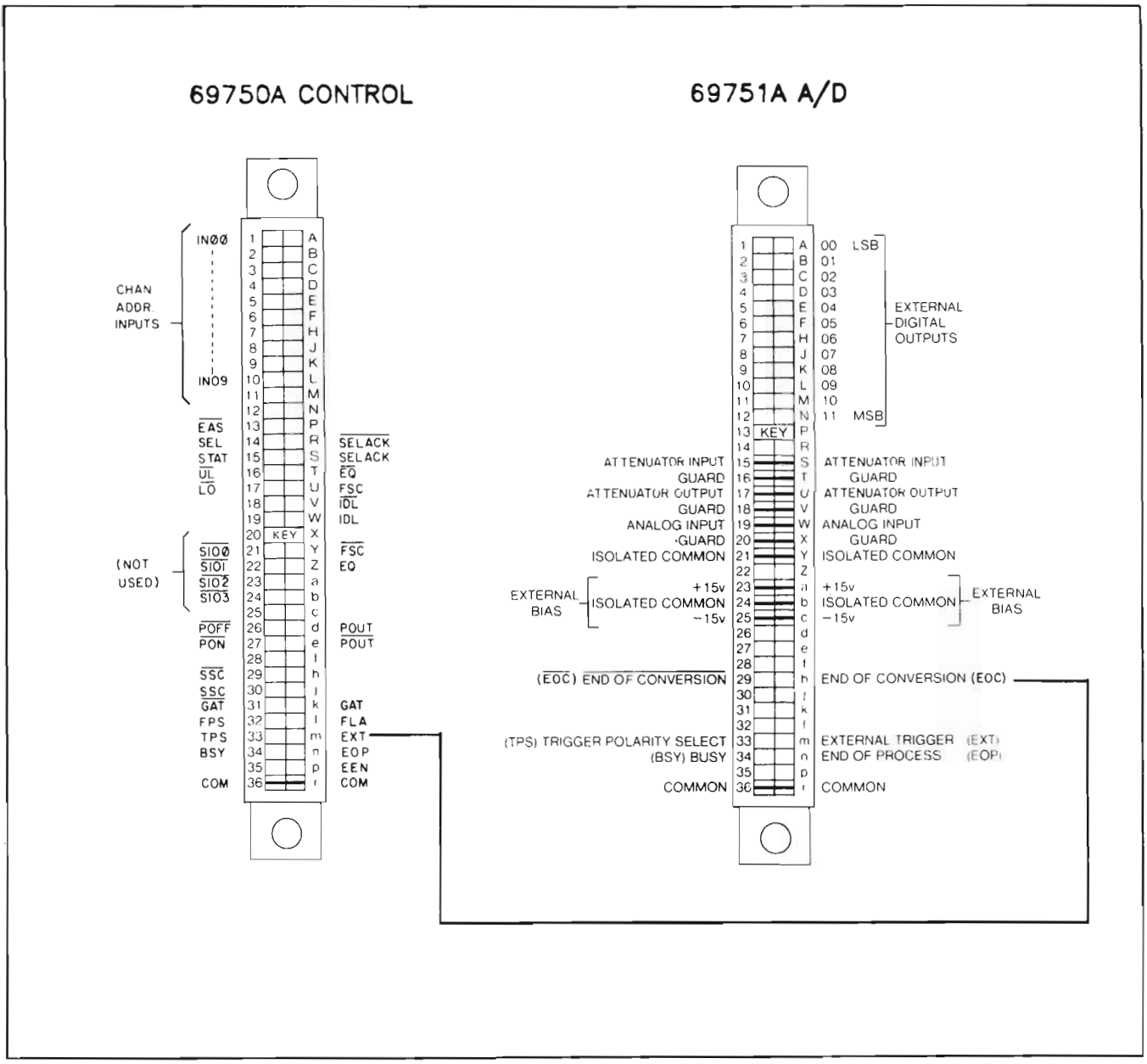


Figure B-1. 69750A Control Card and 69751A A/D Converter

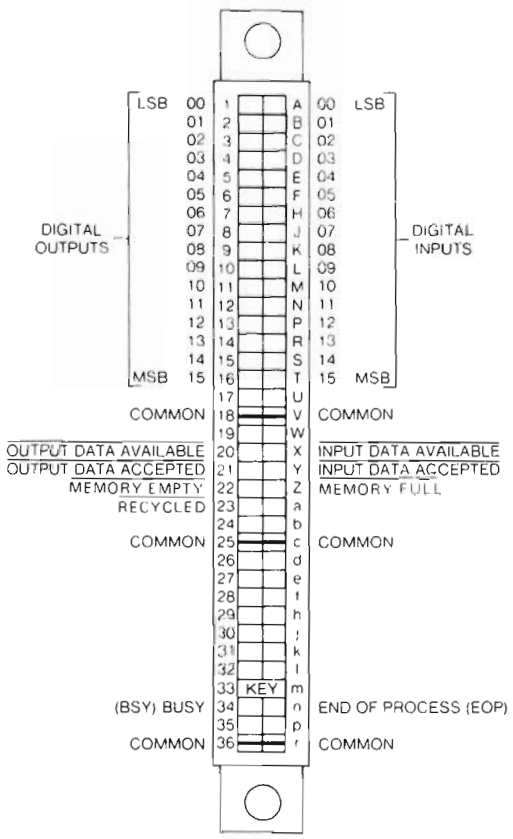
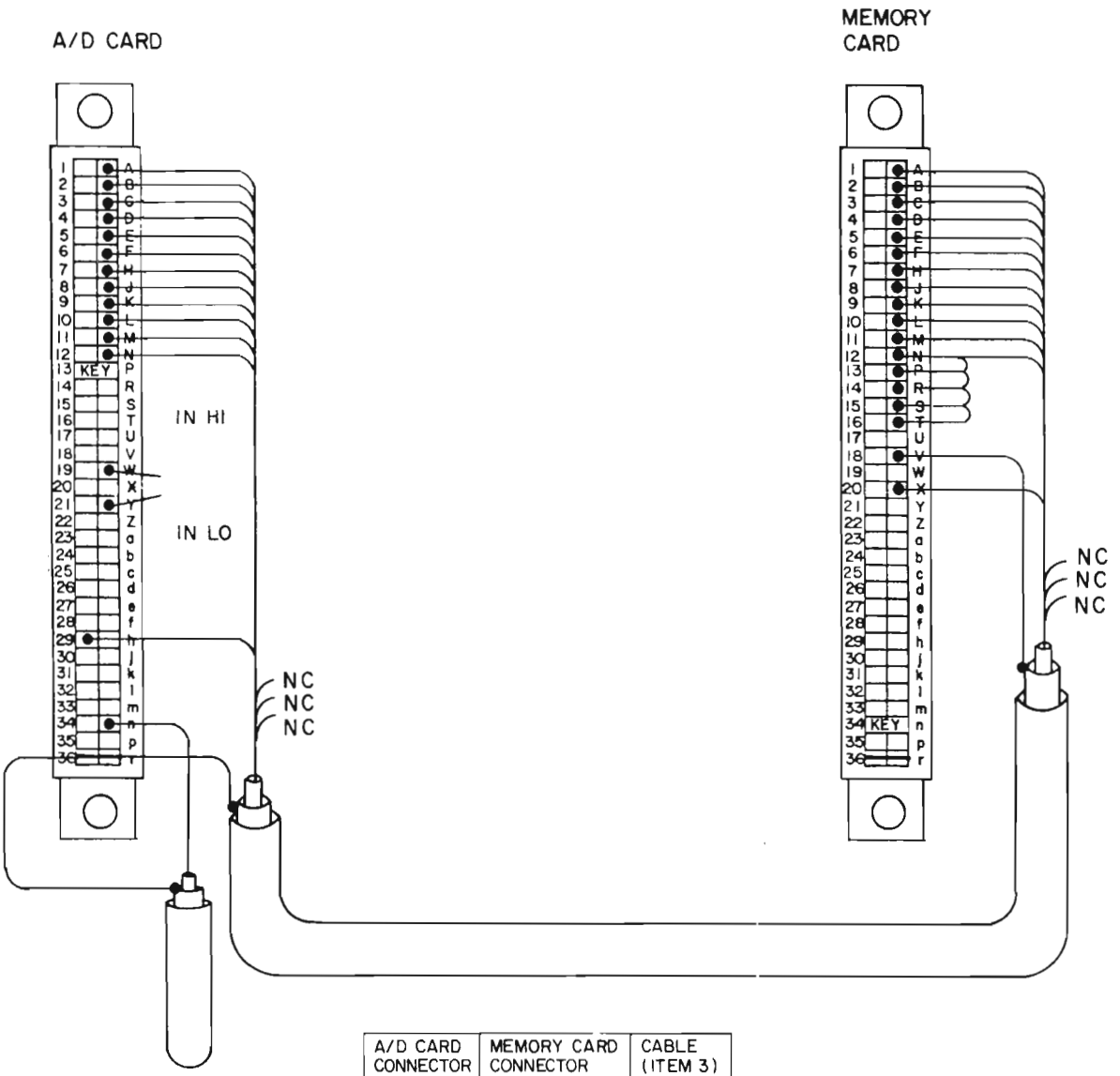


Figure B-2. 69790B Memory Card



A/D CARD CONNECTOR		MEMORY CARD CONNECTOR		CABLE (ITEM 3)
PIN	SIGNAL	PIN	SIGNAL	COLOR
A	OUTPUT BIT ø	A	INPUT BIT ø	BLK
B	BIT 1	B	BIT 1	BRN
C	BIT 2	C	BIT 2	RED
D	BIT 3	D	BIT 3	ORA
E	BIT 4	E	BIT 4	YEL
F	BIT 5	F	BIT 5	GRN
H	BIT 6	H	BIT 6	BLU
J	BIT 7	J	BIT 7	VIO
K	BIT 8	K	BIT 8	GRY
L	BIT 9	L	BIT 9	WHT
M	BIT 10	M	BIT 10	WHT/BLK
N	BIT 11	N	BIT 11	WHT/BRN
29	$\overline{EOC}$(4)	X	$\overline{IDA}$(5)	WHT/RED
36	COMMON	18	COMMON	SHIELD
r	COMMON	V	COMMON	SHIELD

Figure B-3. Connections to 69751A A/D Converter

APPENDIX C
RELATED DOCUMENTS

The manuals in this list will help you to design and install a scanner system for your application.

Scan Control/Pacer Card Model 69750A
Operating Manual, HP Part No. 69750-90001

64-Channel FET Scanner Card Model 69752A
16-Channel FET Scanner Card Model 69755A
Operating Manual, HP Part No. 69752-90001

Analog-to-Digital Converter Card Model 69751A
Instruction Manual, HP Part No. 69751-90001

Memory Card Model 69790B
Instruction Manual, HP Part No. 69790-90001

Buffered A/D Conversion Application Note No. AN 316-1

Multiprogrammer Model 6942A
User's Guide, HP Part No. 06942-90013

Multiprogrammer Model 6942A
Installation and Assembly Level Service Manual,
HP Part No. 06942-90006

BASIC Language Reference for the HP 9826 Computer
HP Part No. 09826-90055

BASIC Interfacing Techniques for the HP 9826 Computer
HP Part No. 09826-90020.

BASIC Programming Techniques for the HP 9826
and 9836 Computers
HP Part No. 09826-90010

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