RELAY OUTPUT CARD

MODEL 69330A

OPERATING AND SERVICE MANUAL

FOR CARDS DESIGNATED RUN 1 AND ABOVE*

*For Cards above Run 1
a change page may be
included.

100 Locust Avenue, Berkeley Heights, New Jersey 07922

HP Part No. 69330-90001

Printed: November, 1970

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MANUAL CHANGES
Model 69330A Relay Output Card
Manual HP Part No. 69330- 90001

Make all corrections in the manual according to errata below, then check the following table for your card's run or serial number and enter any listed change(s) in the manual.

RUN NUMBER		MAKE CHANGES
All		Errata
6		1
7-10		1,2
11-16		1,2,3
17 and above		1,2,3,4
SERIAL		
Prefix	Number	
1637A	01190-01269	1 thru 5
1637A	01270-up	1 thru 6

CHANGE 1:

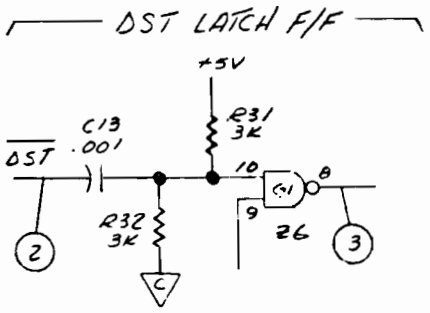
In the Replaceable Parts Table under Mechanical Parts, delete Extractor Handle with Roll Pin, HP Part No. 0403-0180 and add Extractor Handle, Lettered ("Relay Output"), HP Part No. 5081-4916.

CHANGE 2:

In the Replaceable Parts Table, make the following changes:

Relay Output Card: Change to HP Part No. 69330-60021
Add C13: 0.001μF, 500V, HP Part No. 0160-3398
Add R31, 32:3k, 1/4W, HP Part No. 0683-3025

On the schematic diagram, sheet 2, add new differentiating network (C13, R31, R32) as shown below:



CHANGE 3:

In the Replaceable Parts Table, make the following changes:

R2: Change R2 to 1.5KΩ±5%, 1/4W, HP Part No. 0683-1525.
Z1-Z3: Change Z1-Z3 to HP Part No. 1820-0876.

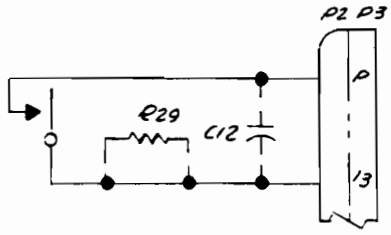
ERRATA:

In Table 1-1, under CONTACT RATINGS, make the following changes:

1.0 amp switching (maximum)
28 VA maximum

In Figure 3-2, in all of the Relay Output Card illustrations (four), add a connection from the junction of J5 and J7 (at the coil of Flag relay K3) to the output connector, pin R.

In Figure 7-1, sheet 2, change the placement of the recommended arc suppression resistor and capacitor (R29 and C12) as shown below:



Each arc suppression resistor can safely dissipate 1W as described in paragraphs 3-31 and 3-32. However, the maximum power dissipation of the multiprogrammer mainframe must be considered in determining the power consumption of the arc suppression resistors. That is, the mainframe can dissipate 36W maximum of external power so that, if 1W is to be dissipated in each arc suppression resistor, only 36 (maximum) resistors can be utilized and, in addition, no other external power dissipation is allowed for any other input/output cards.

CHANGE 4:

An SYE control circuit has been added to the relay card to control the output data relays in a similar manner as the Preset Circuit controls the Gate and $\overline{CTF}$ outputs. That is, the SYE control circuit disables the data relays when power is turned on, if power fails, or if SYE is programmed off. In addition, the card must be addressed and SYE programmed on before the data relays are enab ed. Thus, after power is turned on (or restored after a failure), the card must be addressed and SYE turned on (the order is not important) before the data relays can be energized. Note that the Preset Circuit has also been modified as shown below. These changes, of course, change the component locations so that the component location illustrations do not reflect the latest board layout. Change Figure 7-1, Sheet 1 according to the drawing below.

In the replaceable parts table, make the following changes:

C13: Change C13 to .001μF, 200V, HP Part No. 0160-0153.

C14-16: Add C14-16, 1μF, HP Part No. 0160-0291. (C14 and C15 are connected between C and +5 on the card).

CR7, 8: Add CR7, 8 Diodes, Si. 250mW, 200V, HP Part No. 1901-0033.

CR9: Add CR9 Stabistor, Si. 10 prv, HP Part No. 1901-0460.

Q10: Delete Q10.

Q13-15: Add Q13-15 SS NPN Si, HP Part No. 1854-0071.

Q16: Add Q16 SS PNP Si, HP Part No. 1853-0037.

R25: Change R25 to 20K Ω±5%, 1/4W, HP Part No. 0683-2035.

R26: Delete R26.

R27: Change R27 to 20KΩ ±5%, 1/4W, HP Part No. 0683-2035.

R33: Add R33 fxd, comp 2KΩ ±5%, 1/4W, HP Part No. 0683-2025.

R34: R34 fxd, comp 51KΩ ±5%, 1/4W, HP Part No. 0683-5135.

R36: Add R36 fxd, comp 4.7KΩ ±5% 1/4W, HP Part No. 0683-4725.

R37, 38: Add R37, 38 fxd, comp 3KΩ ±5% 1/4W, HP Part No. 0683-3025.

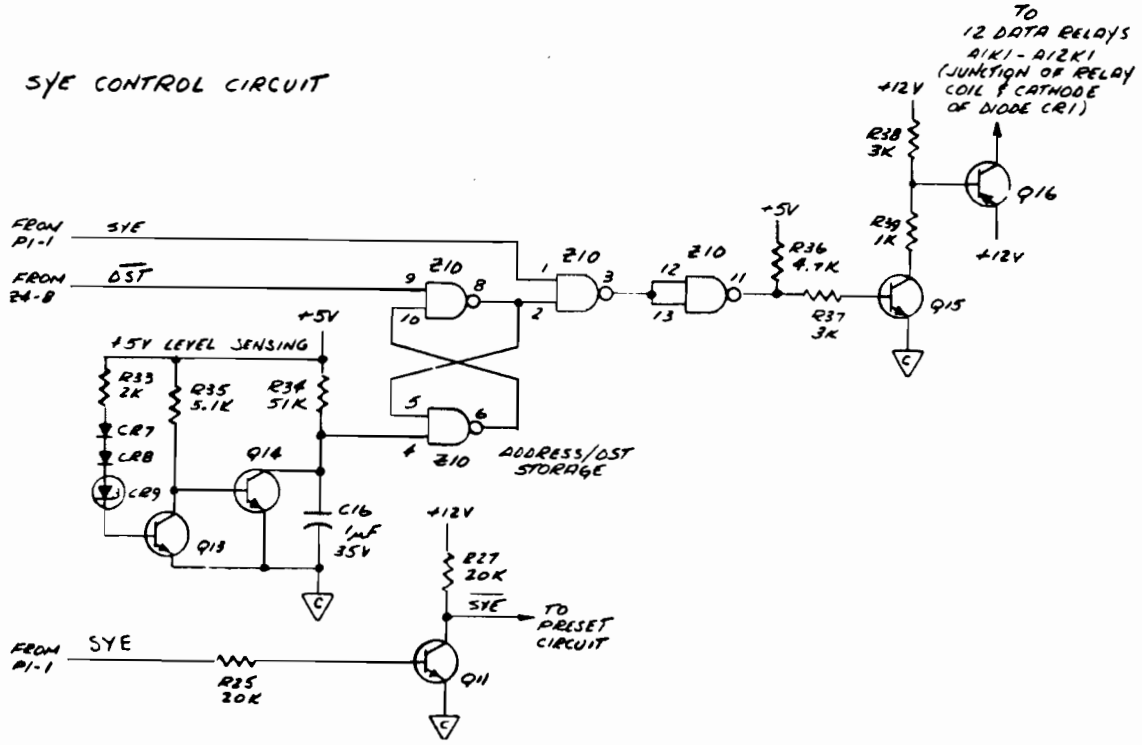
R39: Add R39 fxd, comp 1KΩ ±5% 1/4W, HP Part No. 0683-1025.

Z10: Add Z10 Quad 2-input NAND Gate, IC HP Part No. 1820-0583.

Under Mechanical, Change IC Socket, HP Part No. 1200-0768 to quantity of 10.

ERRATA:

In the parts list, change the part number for the 16-pin IC socket to 1200-0507 and the 14-pin IC socket to 1200-0508.

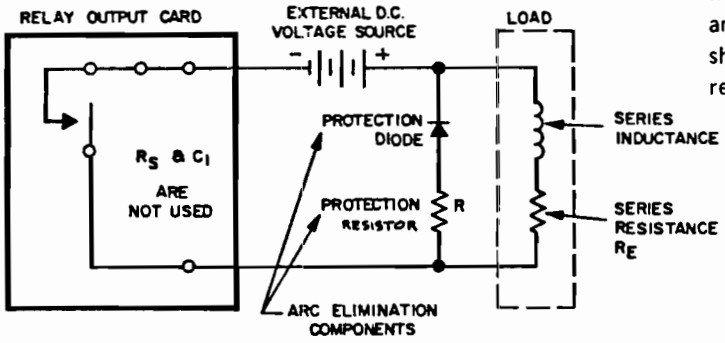


ERRATA:

In the replaceable parts table, under MECHANICAL make the following changes:
Change Connector Assembly, Output to HP Part No. 5060-9658. The new assembly consists of the following parts:

Connector, 30-pin-HP Part No. 1251-0159
Hood, Left-HP Part No. 4040-0232
Clamps, Cable -HP Part No. 1400-0714
Hood Assembly, Right-HP Part No. 5060-7981
Hood, Right-HP Part No. 4040-0233
Insert, Threaded (4-40)-HP Part No. 0590-1017
Insert, Threaded (2-56)-HP Part No. 0590-1018

Arc Suppression Information. The following arc suppression procedure replaces the R-C arc suppression procedure described in paragraph 3-30 when the load is inductive and is operated from a D. C. voltage source:



1. Select a carbon composition resistor R with a value equal to R_E, the equivalent series resistance of the load.
EXAMPLE: a 28V, 1 amp solenoid load has an equivalent series resistance of 28V/1 amp=28 ohms.

2. The power rating of this protection resistor R must be at least $2 (I_{MAX}/6)^2 R_E$ watts.
EXAMPLE: For a 28V, 1 amp solenoid, R has a power rating of at least $2 (1 \text{ amp}/6)^2 28$ ohms = 2 (28/36 watts = 1.56 watts.

3. Connect this resistor in series with a small signal diode that has a peak reverse voltage rating of 200 volts and a power rating of 200 milliwatts, and locate the diode-resistor protection network as close as possible to the load.

The above procedure not only protects the 69330A contacts, but also minimizes radiated electromagnetic fields and voltage spikes, improves solenoid drop-out time (release time), and eliminates excessive heat dissipation in the Multiprogrammer mainframe.

ERRATA:

In Table 1-1, change the Breadkown Voltage Specification to read: "Do not apply voltages in excess of 100Vdc or 100V rms on the output fingers of the card"

ERRATA:

In Table 1-1, change the release time specification to read "3.5 milliseconds maximum.
Vibration during shipment sometimes causes the pool of mercury in mercury-wetted relays A1K1 through A12K1 to become trapped between the relay contacts by capillary action. Once trapped, the mercury makes the contacts appear closed regardless of the coil drive current. To remedy this problem, hold the card in the upright position (as if installed in the 6940B) and gently tap it on its bottom or allow it to drop approximately 2 inches. This gentle impact dislodges the mercury from between the contacts and deposits it in the bottom of the relay capsule. Excessive shock may cause damage to the internal glass capsule of the relay.

Add the following notice to paragraph 1-14: "Effective December 1, 1975, extra manuals may be obtained by ordering Option 910 when ordering your instrument. The number of extra manuals depends on the number of Option 910s ordered".

CHANGE 5:

All multiprogrammer plug-in cards are now being marked with serial numbers to keep better control of units out in the field. The serials assigned to this model are given in the table. For an explanation of the meaning of the serial prefix, see paragraph 1-44 in the multiprogrammer mainframe manual.

CHANGE 6:

To permit mechanized IC insertion, all IC sockets on this board have been deleted.

ERRATA:

Add the model numbers 6940A and 6940B wherever references are made to the 6936A Multiprogrammer, and add the model numbers 6941A and 6941B wherever references are made to the 6937A Extender Unit.

The jumpers designated as J2, J3, etc, on the schematic are actually marked W2, W3, etc. on current circuit boards.

In Table 1-1 on page 1-2, change the Contact Resistance specification to read: 500 millohms maximum at full loading over rated life (10^8 operations).

In the parts list, delete the packing carton or corrugated tray listed and add the part number of the carton with foam liner now used for shipping multiprogrammer cards. Its number is 9211-2603.

In Table 1-1, add the following:
Relay Data Specifications:
Thermal Offset: ±100 microvolts maximum per relay.
Channel Capacitance: 10pF open, 25pF closed, 20pF Channel to Channel, where a channel is any two adjacent relay contacts.
Frequency Response: Flat to within ±0.2dB from DC to 1 MHz.
Cross Talk: −60dB DC to 1MHz with 50 ohm termination; −30dB DC to 1MHz with 1 megohm termination.

Temperature Range Specification: 0°C to +70°C

In paragraph 1-13 and in the parts list (page 6-5), change HP Part No. of the Output connector Assembly to 14555A.

In part two of Change 3 of this change sheet, Z1-Z3 are no longer HP Part No. 1820-0876, but HP Part No. 1820-1411.

1-20-82

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LIST OF TABLES

LIST OF ILLUSTRATIONS

SECTION I
GENERAL INFORMATION

1-1 INTRODUCTION

1-2 This instruction manual contains operating and service instructions for Relay Output Card Model 69330A. The 69330A is designed specifically for use in 6936A Multiprogrammer and 6937A Multiprogrammer Extender units to provide 12 separate form A (SPST, normally open) mercury-wetted contact outputs that reflect the status of 12 programmed data bits.

1-3 Overall system concepts, including system installation, troubleshooting, and operating considerations are covered in the instruction manual for the 6936A Master unit and will not be repeated in this manual.

1-4 DESCRIPTION

1-5 When installed in a multiprogrammer system, the output card is programmed by a 16-bit word originating at a remote computer or the 6936A Multiprogrammer control panel. Twelve of the programmed bits represent data while the remaining four contain the slot address of the output card. The 12 data bits are stored on the output card (when it is addressed) and either energize or de-energize an associated relay. When a logical 1 is programmed in a specific bit position, it energizes its associated relay which in turn produces an output contact closure. (Facilities are provided on the output card for reversing this relationship.)

1-6 The card also contains a system enable (SYE) circuit which holds the 12 output relays in the de-energized state (contacts open) until the SYE function is programmed; and a gate/flag circuit which allows the status of the flag line returned to the computer to be controlled by the external system. The detailed functions of these circuits are covered in Sections III and IV of this instruction manual.

1-7 The output card is fabricated on a $4\frac{1}{2}$" x 11" printed circuit card. The inner end of the card contains a dual 24 pin (48 pin total) printed circuit plug that can mate with any connector in slot 400 through 414 of a multiprogrammer unit (6936A or 6937A). The contact outputs are taken from a dual 15-pin (30 pin total) printed circuit plug located on the outer-end of the card.

1-8 SPECIFICATIONS

1-9 Table 1-1 provides detailed specifications for Model 69330A.

1-10 INTERFACING

1-11 The 69330A relay output card can be installed in any 400 series slot of a 6936A Multiprogrammer or 6937A Multiprogrammer Extender. Once it is assigned to a slot, it assumes the address of that position and will receive programmed data only when that unit and slot are addressed. All operating power and programmed data is derived from the multiprogrammer unit.

1-12 OUTPUT CONNECTOR ASSEMBLY

1-13 One 30-pin output connector assembly (HP Part No. 5060-7934) is furnished with each relay output card for interfacing the output card with the external system. Additional 30-pin connector assemblies may be ordered from your local Hewlett-Packard sales office (refer to list at rear of manual for addresses).

1-14 ORDERING ADDITIONAL MANUALS

1-15 Two manuals are shipped with each 69330A order. Additional manuals may be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). Specify the card model number and HP Part Number shown on the title page.

Table 1-1. Specifications

DATA INPUT:
12-bit binary: Logic 1; relay energized
Logic 0; relay deenergized
The logic states may be reversed by the customer, by a simple modification to the PC card (see Figure 7-1).

SWITCHING CAPABILITY:
12 mercury-wetted reed relays. One Form A per relay (SPST-N.O.). All contact connections are brought separately to fingers on the outer edge of the card.

OPERATING POSITION:
The card is mounted in the mainframe with the relays vertical. Tilt is limited to 30°C maximum displacement from the vertical in any direction.

CONTACT RATINGS:
100Vdc maximum
100Vrms maximum
1.0 amp switching
20 watts maximum

CONTACT RESISTANCE:
50 milliohms maximum, initial (typically 10-20 milliohms).
50 milliohms after rated life.

CONTACT LIFE:
Over 100 x 10^6 operations at full rating.
Contact life greatly increased when used with "dry-circuit" loads.

PULL-IN TIME:
3.5 milliseconds maximum. No contact bounce.

RELEASE TIME:
1 millisecond maximum.

BREAKDOWN VOLTAGE:
Do not apply voltages in excess of 300Vdc on the output fingers of the card.

POWER REQUIREMENT:
+5Vdc, 160mA typical, 260mA maximum from multiprogrammer main power supply.
+12Vdc, 8.5mA/energized relay, 120mA maximum from main power supply.

DIMENSIONS:
4.5" x 11.0" (nominal).

OUTPUT CONNECTOR:
One 30-pin dual contact edge connector.

SAFETY FEATURE:
System enable relay contacts hold all data relays in deenergized state until system enable bit (SYE) is programmed. Following system enable the relays respond to programmed data.

SECTION II
INSTALLATION

2-1 INITIAL INSPECTION

2-2 Before shipment, the 69330A Relay Output Card was inspected and found to be free of mechanical and electrical defects. As soon as the card is received, proceed as instructed in the following paragraphs.

2-3 MECHANICAL CHECK

2-4 If external damage to the shipping carton is evident, ask the carrier's agent to be present when the card is unpacked. Check the card for signs of physical damage. If it is damaged, file a claim with the carrier's agent and notify Hewlett-Packard Sales and Service Office as soon as possible. If it appears to be undamaged, perform the electrical check specified in the following paragraph.

2-5 ELECTRICAL CHECK

2-6 Check the electrical performance of the output card as soon as possible after receipt. Section V of this manual contains checkout procedures which will verify operation of the card. Refer to the inside front cover of this manual for Certification and Warranty statements.

2-7 REPACKING FOR SHIPMENT

2-8 When shipping an output card, it is recommended that the package designed for it be used. The original packaging material is reusable. If it is not available, contact your local Hewlett-Packard field office to obtain the materials. This office will also furnish the address of the nearest service office to which the output card can be shipped. Be sure to attach a tag to the output card specifying the owner, model number, and service required, or a brief description of the trouble.

2-9 OUTPUT CARD INSTALLATION

2-10 Output cards are installed in slots 400 through 414 of a Multiprogrammer unit. To install an output card, proceed as follows:

a. Open the hinged front panel of the Multiprogrammer unit by turning the recessed screw within the knurled handle counterclockwise.

b. With the extractor handle on the top and the card components on the right, slide the card into the desired output slot (400 through 414). Note that all output cards are slotted between pins 4 and 5 and all 400 series connectors of the Multiprogrammer are keyed between the same points. This makes it virtually impossible to plug an output card in upside down or into any slot other than a 400 series slot.

c. Route all wiring from the output cards through the false-bottom channel and out the back of the unit to the external system. Procedures for selecting arc-suppression components are given in Section III of this instruction manual.

d. As physical installation and wiring are completed for the output card, carefully note and record the following types of information on the installation record card located on the rear of the hinged front panel of the multiprogrammer.

(1) Output card type
(2) Application in external system
(3) Timing flag period, logic sense, etc.

SECTION III
OPERATING INSTRUCTIONS

3-1 DATA INPUT

3-2 The relay output card is controlled by the multiprogrammer unit in which it is installed. All d-c operating power, address and data bits, and control signals are supplied to the output card through multiprogrammer main frame connectors in slots 400 through 414. Figure 3-1 illustrates the signals present on all multiprogrammer 400-series connectors.

3-3 PROGRAMMING

3-4 The programming information presented here defines the relationships between programmed data and the 69330A card outputs. Complete system programming instructions are given in the Operating and Service Manual and the 6936A Multiprogrammer.

3-5 There are four general steps involved in programming a relay output card. They are:

a. Enabling the output card by programming the system enable (SYE) bit to a logical 1.

b. Addressing the multiprogrammer unit and slot containing the output card.

c. Programming a data word that will produce the desired output contact configuration.

d. Programming the data transfer enable (DTE) mode which will generate a GATE signal to the external system.

3-6 It is assumed in the following discussion that the reader is familiar with the definitions and functions of multiprogrammer control and data words. If this is not the case, it is suggested that Section III of the 6936A Instruction Manual be read before proceeding.

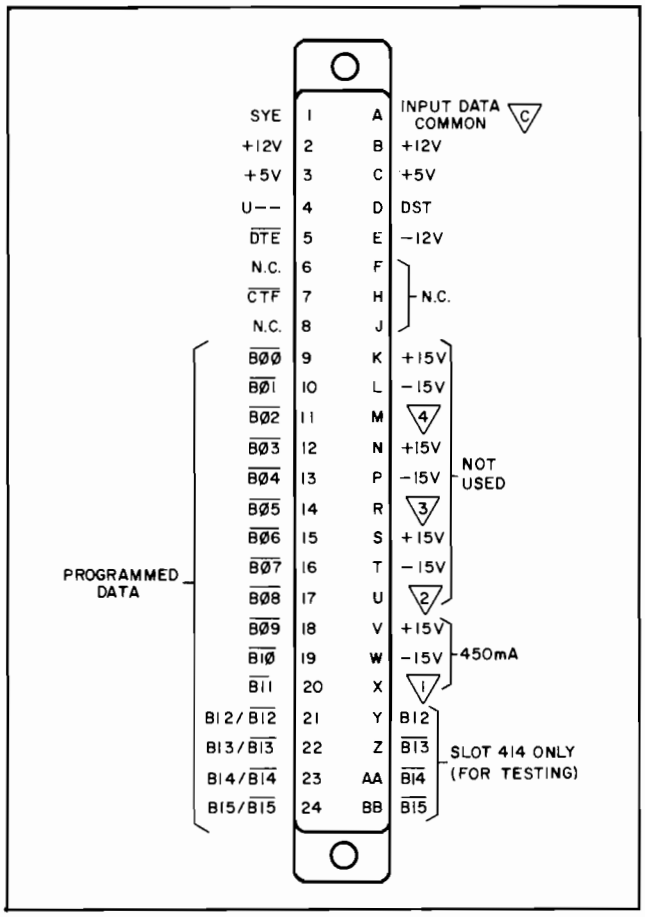


Figure 3-1. Multiprogrammer 400 Series Slot Connector

3-7 SYSTEM ENABLE

3-8 An SYE control line is wired to all multiprogrammer 400 series slots. When the system enable function is programmed as part of a control word, the SYE line goes HI. This energizes the SYE relay which allows the output data relays to respond to programmed data. Prior to SYE being programmed, all the data relays are held in the deenergized state (contacts open).

3-9 The SYE control line has a second function on the 69330A; that is to inhibit the GATE output to the external system until the system enable mode is programmed. This feature prevents a GATE from being generated during initialization.

3-10 ADDRESSING

3-11 An output card is selected to receive new data when its associated address bits (B12/$\overline{B12}$ through B15/$\overline{B15}$) and a unit select line (U--) are all HI. Although both the true and complemented forms of the address bits are represented on Figure 3-1 (e.g. B12 and $\overline{B12}$) only one of the two states is present on each of the four address gate lines when the card is installed in a multiprogrammer slot. For example, if the output card is installed in slot 405, then bits B12 (1), $\overline{B13}$ (2), B14 (4), and $\overline{B15}$ (8) will be present on the address lines, and all four lines will be HI when slot 405 is

addressed. The U-- line is HI when the associated multiprogrammer unit is selected as part of a control word. The unit selection is stored by the 6936A and it remains in effect until a different unit is selected by a later control word.

3-12 RELAY PROGRAMMING

3-13 Data bits $\overline{B\emptyset\emptyset}$ through $\overline{B11}$ are stored on the output card storage registers when the card is addressed. Each stored data bit controls a relay which is energized when a logical 1 ($\overline{B--}$, LO) is programmed. The relay contacts are normally open, and close when the relay is energized. The relays can be made to energize on a logical 0 ($\overline{B--}$, HI) by modifying the printed circuit card and using the Q output of the storage registers to control the relay drivers. (Refer to Figure 7-1 Note 1 for details.)

3-14 DTE MODE

3-15 The primary purpose of the data transfer enable (DTE) mode is to provide a means of generating a GATE signal to the external system under program control. The GATE signal can then be used to strobe the programmed information available on the previously addressed relay output card (or cards) into the external system, and to start a timing flag circuit in the external system that will hold the $\overline{CTF}$ line returned to the multiprogrammer in the busy state until the external circuit times out.

3-16 The purpose, application, and characteristics of the GATE and FLAG signals generated in the DTE mode are described in the following paragraphs. The timing relationships among the various DTE mode signals are covered in Paragraph 3-27.

3-17 GATE Signal. Two conditions must be satisfied in order to generate a GATE to the external system from a single relay output card or from a group of relay output cards: (1) the card (or cards) must be addressed and strobed; (2) the DTE mode must be programmed. The first condition is stored (latched) when it occurs so that when $\overline{DTE}$ is programmed, any previously addressed relay output cards will generate an output GATE signal.

3-18 The external timing flag initiated by the output GATE (and returned to the relay output cards) will reset the strobe latch circuit of the previously addressed and strobed cards, thus clearing them for the next DTE operation. As a back-up, in the event the external timing circuit fails, the data strobe latch and CTF control circuits can be reset by simply programming the DTE mode off.

3-19 A second method of generating an output GATE signal is to keep DTE selected. Then, each time a relay output card is addressed and strobed it will generate an output GATE.

3-20 The GATE output to the external system is a pair of mercury-wetted relay contacts. As supplied from the factory, the GATE relay is normally deenergized and its contacts are normally open. When the two conditions for generating a GATE (latched data strobe and programmed DTE) are satisfied, the GATE relay is energized and its contacts close. If desired, the customer may reverse this relationship (where the relay will deenergize and its contacts will open for the gate conditions) by moving a jumper connection (J2 to A) on the printed circuit card. See Figure 7-1.

3-21 External FLAG Circuit. The timing FLAG circuit in the external system should be started when the GATE relay is first energized (or deenergized when the J2-A jumper option is used) and run for the desired busy period of the external system.

3-22 In applications where an external timing circuit is not required, the GATE relay contacts can be connected directly back to the FLAG relay. In this way the CTF busy period will be approximately 6 to 8msec (the time required for two relay operations).

3-23 Figure 3-2 illustrates four possible connections of the FLAG relay and general requirements for an external timing flag circuit.

3-24 Internal FLAG Circuit. As supplied from the factory, the FLAG relay is normally deenergized and its contacts are open. When the external flag goes to the busy state, the FLAG relay is energized and its contacts close; at the end of the external busy period, the FLAG relay is again deenergized and its contacts open.

3-25 A circuit on the relay output card detects the FLAG relay contact closure and generates a pulse at that time which resets the data strobe latch circuit, and thus the GATE relay. At the end of the external busy period, the detector circuit resets the $\overline{CTF}$ line returned to the multiprogrammer.

3-26 If desired, the customer may have the external timing circuit hold the FLAG relay energized, and its contacts closed, except for the busy period of the external flag. However, since the detector circuit normally interprets a contact closure as the start-of-flag and the next contact opening as the end-of-flag, jumper connections at the output of the detector circuit must be changed so that a contact opening now represents the start-of-flag and the next contact closure represents the end-of-flag. In this way the GATE relay will still be reset at the start-of-flag and the CTF line will be reset at the end-of-flag.

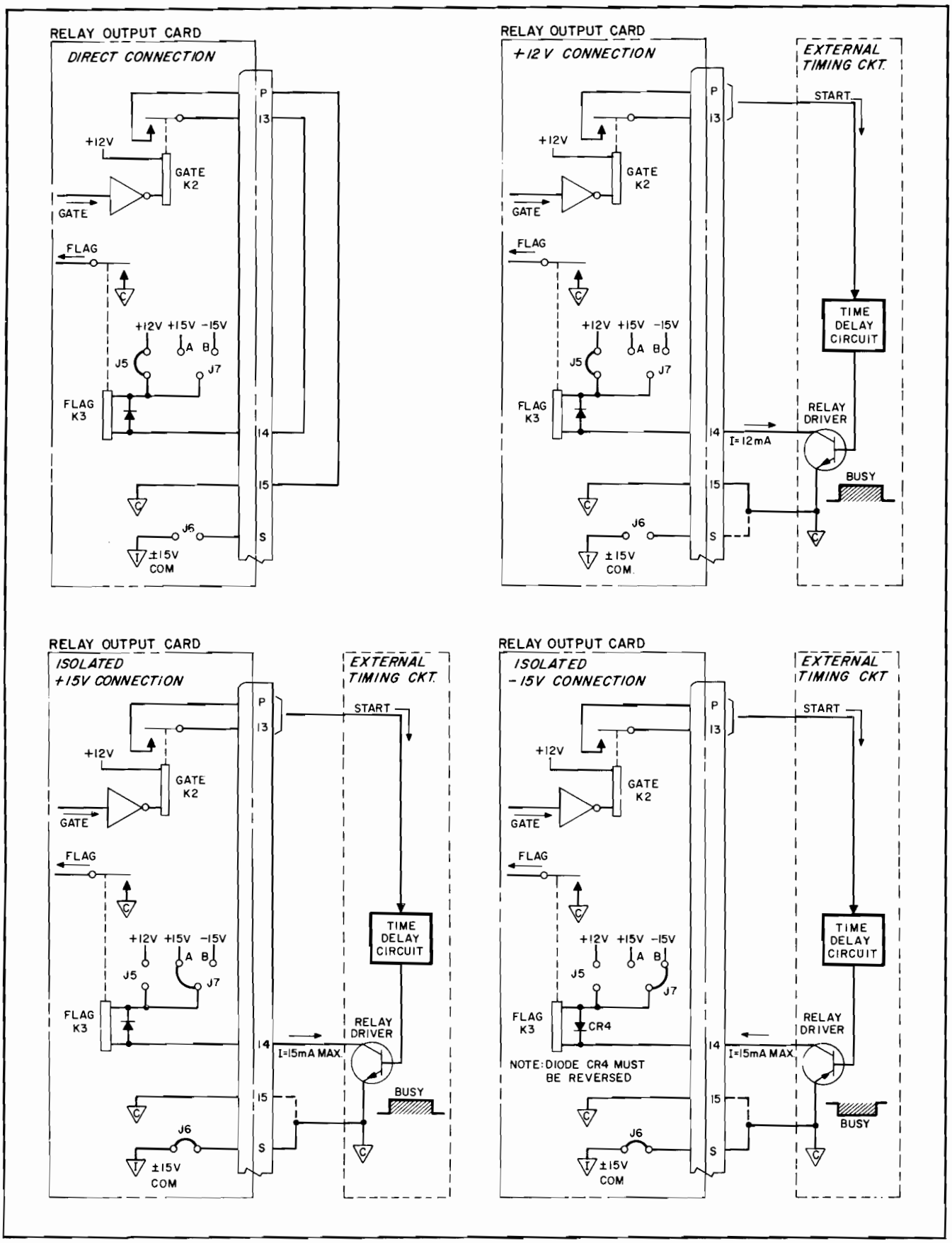


Figure 3-2. External Gate/Flag Connections

The jumper connections for this option are J3 to A and J4 to B. Two additional jumper connections (J3 to A and J4 to A; and J3 to B and J4 to B) allow the FLAG relay to be reset at the end of the busy period of the external circuit. Table 3-1 summarises the functions of the four J3-J4 jumper combinations.

3-28 CABLE FABRICATION

3-29 Since the relay output card may be used to interface with various external devices, an interconnecting cable must be prepared for the particular device being used. A 30-pin output connector is furnished with each relay output card for this

Table 3-1. GATE/FLAG Relay Jumper Options

FLAG RELAY OPERATION	GATE/CTF CIRCUIT OPERATION	JUMPER CONNECTIONS	
		J3	J4
FLAG relay energized by external circuit for BUSY period.	GATE relay reset at start of BUSY period. $\overline{CTF}$ reset at end of BUSY period.	B*	A*
FLAG relay deenergized by external circuit for BUSY period.	GATE relay reset at start of BUSY period. $\overline{CTF}$ reset at end of BUSY period.	A	B
FLAG relay energized by external circuit for BUSY period.	GATE relay reset at end of BUSY period. $\overline{CTF}$ reset at end of BUSY period.	A	A
FLAG relay deenergized by external circuit for BUSY period.	GATE relay reset at end of BUSY period. $\overline{CTF}$ reset at end of BUSY period.	B	B

*Card supplied with this connection

3-27 DTE Mode Timing. A timing diagram of the input and output signals generated in the DTE mode is given in Figure 3-3. The states of the GATE and FLAG relays are shown for the standard strapping options. The timing sequence in this mode is as follows:

a. When the DTE mode is programmed, and data has been previously stored (DST latched), the GATE relay to the external system is energized and the $\overline{CTF}$ line returned to the multiprogrammer is set to the busy (LO) state.

b. The timing flag circuit in the external system should be started when the GATE relay is first energized and run for the desired busy-period of the external system.

c. When the FLAG return relay is first energized, it resets the DST latch circuit and the GATE relay in preparation for the next DTE cycle.

d. When the busy period of the external timing flag circuit is completed, the FLAG return relay is deenergized and resets the $\overline{CTF}$ line to the ready state.

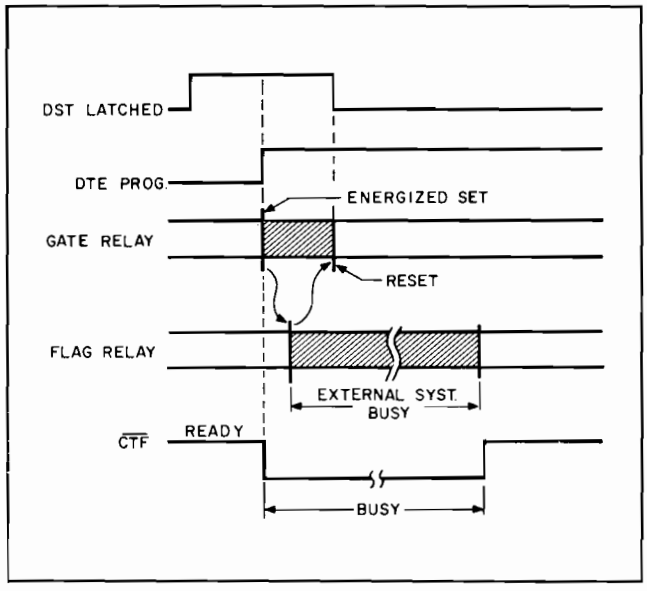


Figure 3-3. DTE Mode, Timing Diagram

Table 3-2. Relay Output Card Pin Connections

CONNECTOR PINS	CONNECT TO CONTACTS OF RELAY	CONTROLLED BY MULTIPROGRAMMER SIGNAL
1, A	A1K1	$\overline{B\emptyset\emptyset}$
2, B	A2K1	$\overline{B\emptyset 1}$
3, C	A3K1	$\overline{B\emptyset 2}$
4, D	A4K1	$\overline{B\emptyset 3}$
5, E	A5K1	$\overline{B\emptyset 4}$
6, F	A6K1	$\overline{B\emptyset 5}$
7, H	A7K1	$\overline{B\emptyset 6}$
8, J	A8K1	$\overline{B\emptyset 7}$
9, K	A9K1	$\overline{B\emptyset 8}$
10, L	A10K1	$\overline{B\emptyset 9}$
11, M	A11K1	$\overline{B1\emptyset}$
12, N	A12K1	$\overline{B11}$
13, P	K2	GATE output
14, R	K3 COIL	FLAG return
15, S	-	5V/12V COM

purpose. Table 3-2 lists the output connector pins for each set of relay contacts.

3-30 ARC SUPPRESSION

3-31 As supplied from the factory, the output relay contacts are directly wired (through jumpers) to the output connector. However, depending upon the nature of the relay contact load, it may be desirable to add arc suppression components to the relay contact circuits. Four printed-circuit pads are provided to mount a resistor and a capacitor in each relay circuit on the card. (See Figure 7-1 for location of these pads.) The selected capacitor and resistor, in conjunction with the external circuit to which the card is connected, must be compatible with the voltage (200V), current (1A), and power rating (20W), of the relay contacts. The maximum physical size of arc suppression resistor R_S (1W) must also be considered.

3-32 An arc suppression circuit is illustrated in Figure 3-4. A procedure for selecting component values of this circuit is given as follows:

(1) Calculate R_S min for 1 amp maximum, through the relay contacts:

$$R_{SMIN} = \frac{V_L}{1\ AMP}$$

(2) With this value of R_S, calculate the maximum current through R_S to limit the power dissipation of R_S to 1 watt:

$$I_{MAX} = \sqrt{\frac{1\ WATT}{R_S}}$$

(3) Now calculate the value of R_L MIN:

$$R_{LMIN} = \frac{V_L}{I_{MAX}} - R_S$$

(4) Calculate C1 to give an R_S C1 time constant of 10 to 24μsec.

3-33 SAMPLE CALCULATIONS

3-34 Sample calculations for three different values of V_L are given below:

For V_L = 50 volts:

(1) $R_{SMIN} = \frac{50V}{1AMP} = 50\Omega$

(2) $I_{MAX} = \sqrt{\frac{1\ WATT}{50V}} = \sqrt{0.02} = 0.1414A$

(3) $R_L = \frac{50V}{0.1414A} - 50\Omega = 300\Omega$

For V_L = 10 volts:

(1) $R_{SMIN} = \frac{10V}{1AMP} = 10\Omega$

(2) $I_{MAX} = \sqrt{\frac{1\ WATT}{10V}} = \sqrt{0.1} = 0.333A$

(3) $R_L = \frac{10V}{0.333A} - 10\Omega = 20\Omega$

For V_L = 100 volts:

(1) $R_{SMIN} = \frac{100V}{1AMP} = 100\Omega$

(2) $I_{MAX} = \sqrt{\frac{1\ WATT}{100V}} = \sqrt{0.01} = 0.1A$

(3) $R_L = \frac{100V}{0.1A} - 100\Omega = 900\Omega$

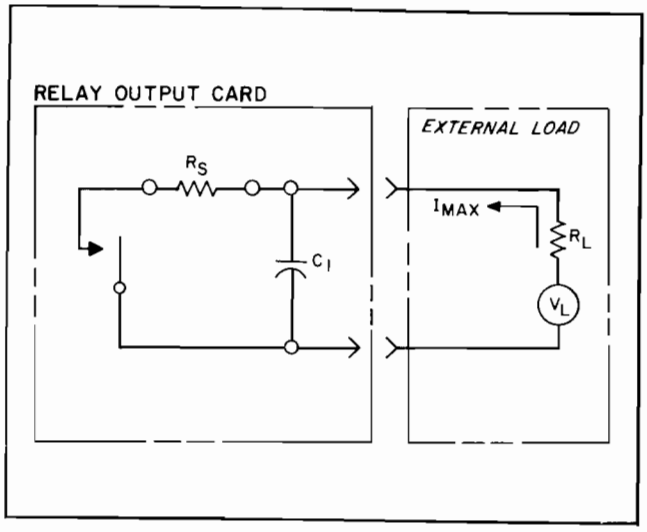


Figure 3-4. Arc Suppression Circuit

SECTION IV
PRINCIPLES OF OPERATION

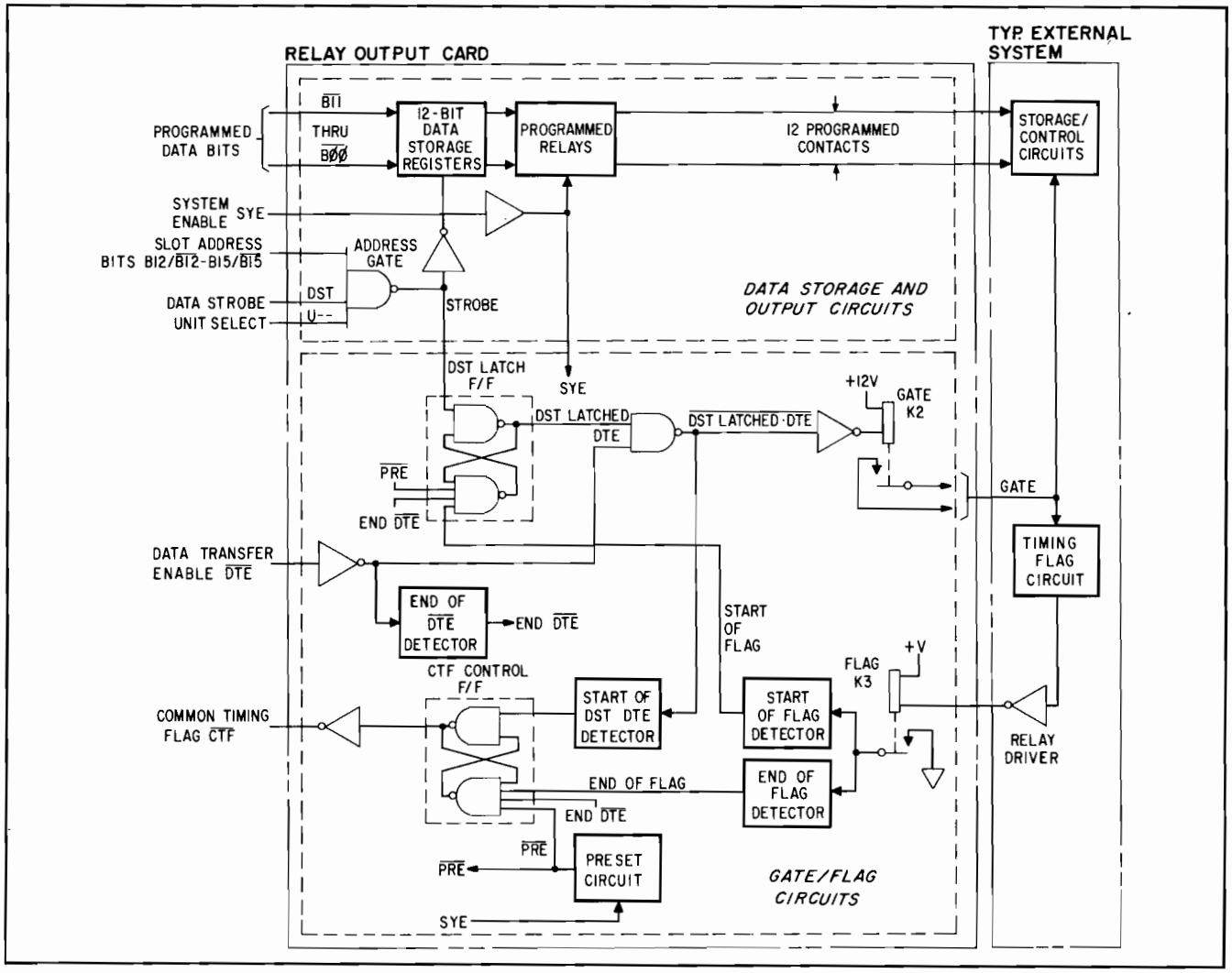


Figure 4-1. Relay Output Card, Model 69330A, Block Diagram

4-1 INTRODUCTION

4-2 This section contains principles of operation for Relay Output Card, Model 69330A. Theory is presented on both a block diagram and a detailed circuit theory level.

4-3 BLOCK DIAGRAM THEORY

4-4 Figure 4-1 is a block diagram of the relay output card. The card consists of two essentially independent circuit groups: a data storage and control circuit group which stores programmed data bits and provides relay contact outputs that reflect the status of the data bits; and a gate/flag circuit group which allows the status of the flag line returned to the computer to be controlled by the external system.

4-5 DATA STORAGE AND OUTPUT CIRCUITS

4-6 This circuit group consists of an address gate circuit, a strobe amplifier, a 12-bit data storage register, programmed output relays and associated drivers, and an SYE circuit. When the output card slot is addressed, the slot address bits

all go to the HI state. If the unit containing the card has been selected by a previous control word, U-- is also HI. When a DST pulse appears, a positive strobe pulse, the width of DST, is generated and applied to the data storage flip-flops and the timing flag circuit. The strobe pulse enters data bits $B\overline{\emptyset\emptyset}$ through $\overline{B11}$ into local storage. The outputs of the storage flip-flops directly control the states of the data relays. The SYE circuit holds the 12 data-output relays in the deenergized state (contacts open) until the SYE function is programmed.

4-7 GATE/FLAG CIRCUIT

4-8 The purpose of the GATE/FLAG circuit is to generate a GATE output to the external system under program control. The GATE signal can then be used to strobe the programmed information available on the previously addressed output card (or cards) into the external system, and to start a timing flag circuit in the external system that will hold the $\overline{CTF}$ line returned to the multiprogrammer in the busy state until the external circuit times out.

4-9 A timing diagram of the signals generated by the GATE/FLAG circuit is given in Figure 4-2 and described as follows:

T_0 - At T_0, the multiprogrammer is initially turned on and SYE has not yet been programmed. The LO PRE output of the preset circuit holds the DST latch and CTF control F/F's in the reset state. This insures that the output GATE relay and CTF lines remain in the reset (off) state until after SYE has been programmed.

T_1 - SYE is programmed. $\overline{PRE}$ goes HI, releasing the DST latch and CTF control F/F's.

T_2 - The card is addressed and strobed. The DST latch F/F is set (DST LATCHED goes HI).

T_3 - DTE is programmed. The two functions (DTE and DST LATCHED) enable a NAND gate, the output of which is amplified and used to energize gate relay K2. The start of this function (DTE · DST LATCHED) is also detected and used to set the CTF control flip-flop. With the CTF control flip-flop set, the $\overline{CTF}$ line goes to the LO (busy) state.

T_4 - The contacts of GATE relay K2 start an external timing flag circuit and this circuit energizes FLAG relay K3. As K3 is first energized, a start-of-flag detector circuit generates a negative pulse. This pulse resets the DST LATCH F/F which in turn deenergizes GATE relay K2 in preparation for the next DTE cycle.

T_5 - As long as the external timing flag circuit is in the busy state, the FLAG relay remains energized and $\overline{CTF}$ is also held in the busy state. When the external circuit times out (T_5) the FLAG relay is deenergized. At this time an end-of-flag pulse is generated which resets the CTF control flip-flop. $\overline{CTF}$ is now returned to the ready state.

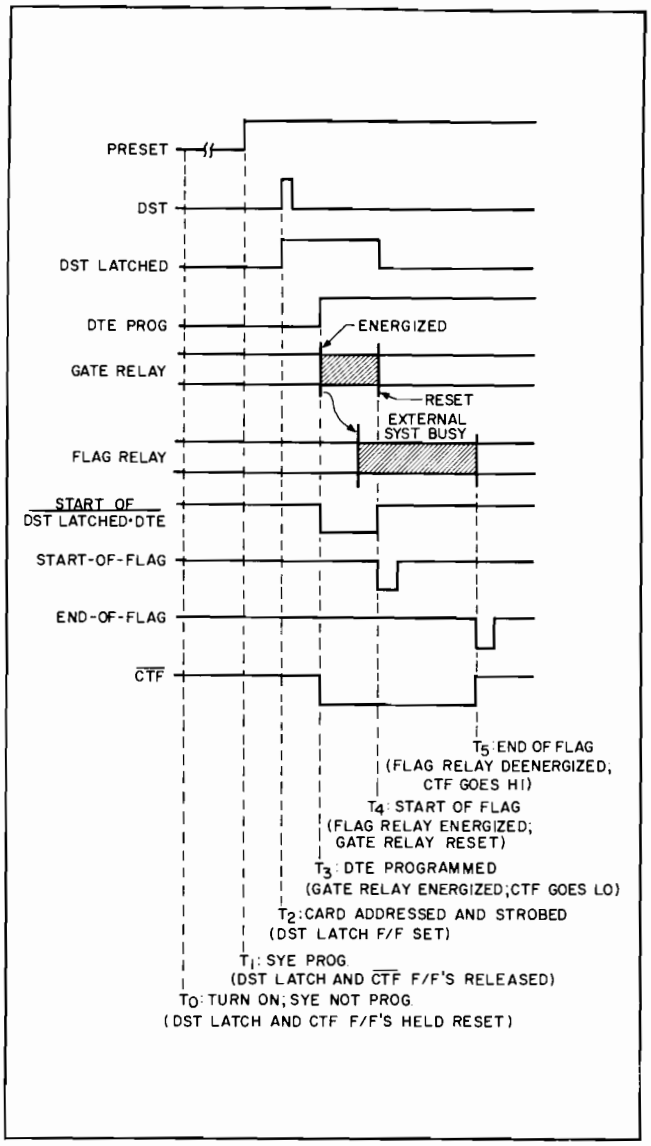


Figure 4-2. GATE/FLAG Circuit, Timing Diagram

4-10 DETAILED CIRCUIT ANALYSIS (See Figure 7-1)

4-11 DATA STORAGE AND CONTROL

4-12 When installed in a multiprogrammer unit, the output card is programmed by a 16-bit word. Twelve of the bits ($B\overline{\emptyset\emptyset}$ through $\overline{B11}$) represent programmed data, while the remaining four (B12/$\overline{B12}$ through B15/$\overline{B15}$) represent the address of the multiprogrammer slot in which the output card is installed. Although both the true and complemented forms of the address bits are represented on Figure 7-1 (e.g., B12 and $\overline{B12}$) only one of the two states is present on each of the four address gate lines when the card is installed in a

multiprogrammer slot. For example, if the output card is installed in slot 405, then bits B12 (1), $\overline{B13}$ (2), B14 (4), and $\overline{B15}$ (8) will be present on the address lines; and all four lines will be HI when slot 405 is addressed. A fifth line, U--, is also part of the addressing scheme and represents a multiprogrammer unit selection.

4-13 A control signal, designated SYE (system enable), is wired to all output card slots and for the relay output cards it either enables or inhibits the data output relays. SYE is programmed as part of a multiprogrammer control word and does not depend on slot addressing. When SYE is HI, driver relays Q11 and Q10 are both switched on and Q10 applies +12 volts to one side of all the data relays.

4-14 Addressing. When the slot and unit in which the output card is housed are addressed, the four address bits and U-- go HI. Data bits $\overline{B11}$ through $\overline{B\emptyset\emptyset}$ are also present at this time but are not yet entered into storage. Approximately 4μsec after the programmed word appears, a data strobe pulse (DST) is received by the output card. The 4μsec delay of DST allows the data lines to settle before the data is stored. When DST appears, it enables NAND gate Z4 which in turn produces a negative pulse the width of DST. Transistor Q2 inverts the negative pulse and applies it to the 12-bit data storage register and the timing flag generator.

4-15 Data Storage. The 12-bit data storage register is comprised of three four-bit storage flip-flops (Z1, Z2, and Z3). The individual stages are D-type, positive-edge triggered flip-flops. The logical state at the D-input of a flip-flop is transferred to the Q output terminal when the clock terminal (CLK) is strobed by a positive-going pulse. ($\overline{Q}$ always assumes the state opposite the Q state.) When a data bit is programmed to a logical 1 at the computer, the corresponding $\overline{B}$-- data lines goes LO. The strobe pulse from Q2 transfers this LO level from the D-input to the Q output ($\overline{Q}$ of course goes HI). Relay driver Q1 is switched on by the HI level at the $\overline{Q}$ output and energizes relay K1. When the relay is energized, its contacts close to the external system.

4-16 GATE/FLAG CIRCUITS

4-17 The gate numbers shown within the logic symbols in Figure 7-1 (e.g. G1) are for reference in tracing circuit operation; they have no physical relationship to the actual parts. The Z numbers adjacent to the gates, however, are the actual reference designations of the IC's and these numbers are etched on the printed circuit card, for physical location of the IC's.

4-18 Detailed circuit operation is described for the following phases of operation:

a. Preset
b. Start of Gate and $\overline{CTF}$
c. Start of Flag
d. End of Flag
e. End of DTE.

4-19 Preset Circuit. When the multiprogrammer system is first turned on, the preset circuit generates an output that stays LO for approximately 50msec after power is applied. This level resets the DST LATCH flip-flop (G1 and G2) and the CTF CONTROL flip-flop (G6 and G7) to insure that the output GATE relay is initially deenergized and the $\overline{CTF}$ line is initially in the ready (HI) state. A second input to the preset circuit from SYE amplifier Q11 holds the two flip-flops in the reset state until the system enable mode is programmed.

4-20 When power is turned on, +5 volts is applied across the R-C circuit consisting of resistors R14 and R15 and capacitor C2. Since C2 cannot charge instantaneously, the base of Q7 remains negative with respect to its emitter, switching Q7 on. As the collector voltage of Q7 goes positive, Q6 is turned on driving the preset line LO. When capacitor C2 has charged to approximately +3.8 volts (in approximately 50msec) both Q7 and Q6 are cut off, returning the turn-on preset line to the HI state. Diode CR2 provides a rapid discharge path for C2 when power is turned off.

4-21 The second input to the preset circuit is taken from the collector of transistor Q11. Before SYE is programmed, Q11 is cut off and its collector voltage is at a HI level. This level is buffered by emitter follower Q12 and applied to the base of Q6, switching Q6 on. The LO collector voltage of Q6 holds the DST LATCH and CTF CONTROL flip-flops in the reset state. Once SYE is programmed the $\overline{PRE}$ line goes HI, releasing the two flip-flops.

4-22 Start of Gate and $\overline{CTF}$. Each time data is strobed into storage, and provided SYE has been programmed, one condition for energizing GATE relay K2 and setting the $\overline{CTF}$ line is satisfied; that of latching the data strobe. The second condition requires that the data transfer enable mode be programmed ($\overline{DTE}$, LO). When the data strobe pulse appears, the output of address gate Z4 goes LO for the period of DST (approximately 1μsec) and sets the DST LATCH flip-flop. The resulting HI output of gate G1 is applied as one input to NAND gate G3. The second input to G3 is derived from $\overline{DTE}$, and is coupled through emitter-follower Q3 and inverter G10 to G3. With DST latched and DTE programmed, both inputs to NAND gate G3 are HI. The LO output of G3 ($\overline{DST\ LATCHED \cdot DTE}$) is inverted by gate G4, amplified by transistors Q4, Q9, and Q8, and used to energize GATE relay K2. Capacitor C8 in the collector-base circuit of Q9 provides a

1.7msec delay on relay pick-up and drop-out. This delay insures that the 12-data relays have time to respond to programmed data before the GATE is applied to the external system. (When the J2-A option is employed K2 is normally deenergized, and energized by $\overline{\text{DST LATCHED} \cdot \text{DTE}}$.)

4-23 The initial negative transition of $\overline{\text{DST LATCHED} \cdot \text{DTE}}$ is detected by the circuit consisting of G4, G5, R9, and C4, and it generates a short-duration negative pulse coincident with this transition. (Operation of the detector circuit is described in the next paragraph.) The negative pulse sets the CTF CONTROL flip-flop and its output goes HI. CTF is inverted by transistor Q5, setting $\overline{\text{CTF}}$ to the LO (busy) state.

4-24 The start of DST and DTE detector makes use of the discharge time of capacitor C4 to generate a negative set pulse for the CTF CONTROL flip-flop. At the time $\overline{\text{DST LATCHED} \cdot \text{DTE}}$ initially goes LO, capacitor C4 begins to discharge, but, since it cannot discharge instantaneously, it keeps one input to NAND gate G5 HI. Gate G4 inverts $\overline{\text{DST LATCHED} \cdot \text{DTE}}$, and this holds the second input to NAND gate G5 HI. The resulting LO output of G5 resets the CTF CONTROL flip-flop. When C4 has discharged to the LO level, NAND gate G5 is inhibited and its output returns HI.

4-25 Start-of-Flag. In response to the GATE relay contact closure, the external system returns a flag relay energizing signal to the relay output card. As the FLAG relay contacts close, they apply a COM (LO) level through the contact-bounce suppressor circuit composed of R7, R13, R12 and C3 to inverter G18. When FLAG relay K3 is first energized, capacitor C3 rapidly discharges to COM through R13. If the relay contacts momentarily bounce, C3 attempts to recharge to +5 volts through both R7 and R13. The charging R-C time constant is long compared to the contact-bounce period thus keeping the voltage across C3, resulting from contact bounce, at a relatively small value. Resistor R3 further minimizes the effects of contact bounce by forcing the input to G18 toward a LO level, thus making it necessary that the input be at approximately 1.6 volts for G18 to switch states. The input LO level from the relay contacts is inverted three times (by G18, G17, and G16) with the resulting HI level (at the output of G16) applied to start-of-flag detector G15, G13, R10, and C6. (The operation of this circuit is similar to that described for the start of DST and DTE circuit in Paragraph 4-24.) The negative start-of-flag pulse at the output of G13 is propagated through gates G8 and G9 and resets the DST latch flip-flop. The output of flip-flop gate G1 now goes LO and inhibits NAND gate G3. The HI output of G3 causes GATE relay K2 to deenergize.

4-26 End-of-Flag. When the external timing circuit times out, the flag relay energizing signal is removed and K2 deenergizes. The end-of-flag circuit consisting of G15, G14, R11, and C7 senses the LO-to-HI transition at the input of G15 and generates a negative pulse which resets the CTF CONTROL flip-flop and returns the $\overline{\text{CTF}}$ line to the ready (HI) state.

4-27 End-of-DTE. When the DTE mode is terminated, the input to the end-of-DTE pulse generator (G11, G12, R8, and C5) makes a transition from a HI to a LO-level. This transition is sensed by the pulse generator and it generates a negative pulse which resets the CTF CONTROL and DST LATCH flip-flops.

SECTION V
MAINTENANCE

5-1 INTRODUCTION

5-2 This section contains preventive maintenance instructions, checkout procedures, and troubleshooting procedures for Relay Output Card, Model 69330A.

5-3 TEST EQUIPMENT REQUIRED

5-4 The 6936A Multiprogrammer provides all signal inputs necessary for testing the relay output card. It is assumed that the 6936A, as well as all other test instruments, are functioning properly at the outset of testing. The general purpose test instruments required for maintenance of the relay output card are listed in Table 5-1.

5-5 PREVENTIVE MAINTENANCE

5-6 The only preventive maintenance necessary is to keep the printed-circuit connector contact fingers clean. A nonabrasive eraser, such as a "Pink Pearl" or a plastic eraser, should be lightly rubbed over the contact fingers to remove any film or foreign material.

5-7 CHECKOUT PROCEDURES

5-8 These procedures can be used to check operation of relay output cards when they are initially received, and as an aid in isolating trouble to a general circuit area if a malfunction is noted during operation. The procedures are performed with the output card plugged into an extender card and the extender card plugged into a multiprogrammer unit. It is suggested that the procedures for manually programming the 6936A be reviewed, as necessary, before proceeding.

5-9 If an output card fails a test, make certain that it was programmed correctly before starting troubleshooting. Also check that the Multiprogrammer SYE interlock jumper (pins 18 and 19 of data input connector) is in place before testing.

5-10 Checkout is accomplished in two steps. The first set of procedures, Table 5-2, verify operation of the data storage circuits, which include the following:

(1) System Enable (SYE) Circuit
(2) Address Gate and Strobe Circuit
(3) Storage Register-Relay Circuits

5-11 If a malfunction is noted while performing the data storage circuit checkout procedures, refer to the referenced troubleshooting table for additional fault isolation procedures.

5-12 The second set of procedures, Table 5-3, verify operation of the gate/flag circuit, including the preset function. If a gate/flag circuit checkout test fails, refer to the correspondingly numbered test in the gate/flag circuit troubleshooting table.

5-13 The physical and electrical locations of parts referred to in the following procedures are illustrated in Figure 7-1.

Table 5-1. Test Equipment Required

TYPE	CHARACTERISTICS	USE	RECOMMENDED MODEL
Oscilloscope	Bandwidth: dc to 50MHz. Sensitivity: 20mV/div.	Monitor short duration pulses.	HP Model 180A with 1804A and 1821A plug-ins.
Digital Multi-Function Meter	Voltage Accuracy: ±0.003% of reading. Resistance Accuracy: ±0.01% of reading +0.01% of range.	Voltage and resistance measurements.	HP Model 3450A with Option 002.
Logic Probe	Impedance: 10k ohms Trig. Threshold: +1.4V nominal Min. Pulse Width: 30nsec.	Logic circuit troubleshooting.	HP 10525A.

Table 5-2. Data Storage Circuits Checkout Procedure

TEST NO.	EQUIPMENT CONNECTIONS	INSTRUCTIONS	NORMAL INDICATION	EVALUATION
1	After performing INSTRUCTIONS (next column to the right) measure the resistance across each pair of data relay contacts. (See Figure 7-1.)	Energize the Multiprogrammer System.	∞ ohms across each pair of relay contacts.	If the indication is abnormal in more than one case, refer to the SYE circuit troubleshooting procedures. If the indication is abnormal in only one case, check the corresponding relay.
2	Same as Test 1.	Select control word (bits 15, 14, 13, and 12 on). Program SYE (bit 5 on). Program unit address. Touch LOAD OUTPUT.	Data relay contacts are open or closed in a random pattern. (At least one pair of contacts are closed.)	If all contact-pairs remain open, turn the multiprogrammer off and on and repeat this test. If the test fails again refer to SYE circuit troubleshooting procedures.
3	Same as Test 1.	Address the unit and output card slot and program logical 1's in alternate bit positions starting with bit 0 (e.g. 0, 2, 4, etc.). Touch LOAD OUTPUT.	Pins of output plug P2 on the card go to the following states: 0* ohms: A - 1, C - 3, E - 5, H - 7, K - 9, M - 11 ∞ ohms: B - 2, D - 4, F - 6, J - 8, L - 10, N - 12	If the data relays do not respond at all to the programmed data, refer to address gate and strobe circuit troubleshooting procedures. If only certain bit positions fail, check the associated storage register and relay circuit.
4	Same as Test 1.	Address the output card slot and program logical 1's in alternate bit positions starting with bit 1 (e.g. 1, 3, 5, etc.). Touch LOAD OUTPUT.	Pins of output plug P2 go to the following states: 0* ohms: B - 2, D - 4, F - 6, J - 8, L - 10, N - 12 ∞ ohms: A - 1, C - 3, E - 5, H - 7, K - 9, M - 11	If only certain bit positions fail, check the associated storage register and relay circuit.

*If arc-suppression resistors are installed, the resistance reading will be the value of the arc-suppression resistor.

Table 5-3. Gate/Flag Circuit Checkout Procedure

TEST NO.	EQUIPMENT CONNECTIONS	INSTRUCTIONS	NORMAL INDICATION	EVALUATION
1	With ohmmeter, measure across GATE relay K2 contacts (pins 13 and P of P2). With logic	Select control word (bits 15, 14, 13, and 12 on). Program SYE (bit 5 on) and DTE (bit 6 on). Program unit address. Touch LOAD OUTPUT. Address	Ohmmeter reading goes from ∞ to 0 ohms. Logic probe goes from on to off.	Check equipment connections and programming and repeat test. If test fails again, refer to gate/flag circuit troubleshooting, Step 1.

Table 5-3. Gate/Flag Circuit Checkout Procedure (Continued)

TEST NO.	EQUIPMENT CONNECTIONS	INSTRUCTIONS	NORMAL INDICATION	EVALUATION
1	probe, monitor $\overline{\text{CTF}}$ line (pin 7 of P1).	the unit and output card slot. Touch LOAD OUTPUT.		
2	Same as Test 1.	Repeat the above except terminate the SYE mode when the control word is entered.	Ohmmeter reading remains ∞ ohms and logic probe remains on.	If test fails, refer to gate/flag circuit troubleshooting, Step 2.
3	Same as Test 1.	Repeat Step 1 programming instructions. Simulate start of external flag by energizing FLAG RET relay K3 (+12 volts across pins R (+) and 14 (COM) of P2). (Energizing voltage must be a definite step change to avoid contact bounce.)	GATE relay is reset; ohmmeter reading goes from 0 to ∞ ohms. $\overline{\text{CTF}}$ remains unchanged; logic probe stays off.	If test fails, refer to gate/flag circuit troubleshooting, Step 3.
4	Same as Test 2.	Do not change programming. Simulate end of external flag by deenergizing FLAG RET relay K3. (Avoid contact bounce.)	Ohmmeter reading remains ∞ ohms. CTF is reset; logic probe goes from off to on.	If test fails, refer to gate/flag circuit troubleshooting, Step 4.
5	Same as Test 2.	a. Touch CLEAR REGISTER. Program control word and DTE and SYE. Touch LOAD OUTPUT. Address unit and output card slot. Touch LOAD OUTPUT. b. Eliminate DTE selection. (Bit 6 to logical 0; touch LOAD OUTPUT.)	a. Ohmmeter reading goes from ∞ to 0 ohms. Logic probe goes from on to off. b. GATE and $\overline{\text{CTF}}$ are reset. (Ohmmeter reading goes to ∞ ohms; logic probe goes on.)	a. Same as Test 2. b. If test fails, refer to gate/flag circuit troubleshooting, Step 5.

5-14 TROUBLESHOOTING

5-15 This paragraph contains troubleshooting procedures covering the four functional circuit areas of the relay output card. The circuit areas are:

(1) System Enable (SYE) Circuit
(2) Address Gate and Strobe Circuit
(3) Storage Register-Relay Circuits
(4) Gate/Flag Circuit.

5-16 If a defective component is found in the course of troubleshooting, be sure to turn off power at the Multiprogrammer and remove the output card from the extender before attempting replacement. When installing an IC, be sure that the notch or dot on the IC is at the same end as the bevel on the IC socket.

5-17 SYE CIRCUIT TROUBLESHOOTING

5-18 If none of the 12 data relays can be energized, the SYE circuit (which provides operating voltage for the relays) is probably defective. Troubleshooting procedures for this circuit are given in Table 5-4.

Table 5-4. SYE Circuit Troubleshooting

TEST NO.	EQUIPMENT CONNECTIONS	INSTRUCTIONS	NORMAL INDICATION	IF INDICATION IS ABNORMAL	IF INDICATION IS NORMAL
1	With voltmeter, monitor the collector of Q10.	Alternately program SYE on and off.	+12 volts with SYE programmed on, and approximately +1 volt with SYE programmed off.	Proceed to Test 2.	Check wiring to relays.
2	With voltmeter or logic probe, monitor the SYE signal input at P1-1.	Alternately program SYE on and off.	HI level with SYE programmed on, and LO level with SYE programmed off.	Fault is in Multiprogrammer or programming. Check programming.	Proceed to Test 3.
3	With voltmeter, monitor the collector of Q11.	Alternately program SYE on and off.	Approximately +1 volt with SYE programmed on and +12 volts with SYE programmed off.	Check Q11, R25, R26, and R27.	Check Q10.

5-19 ADDRESS GATE AND STROBE CIRCUIT TROUBLESHOOTING

5-20 If all storage register stages fail to accept programmed data, it is likely that the address gate and strobe circuit is defective. Troubleshooting procedures for this circuit are given in Table 5-5.

5-21 STORAGE REGISTER-RELAY CIRCUIT TROUBLESHOOTING

5-22 If a storage register, relay driver, or relay associated with a given data bit ($\overline{B\emptyset\emptyset}$ through $\overline{B11}$) fails, the associated contact output will not reflect the state of the programmed bit. The troubleshooting procedures given in Table 5-6 apply to a typical data bit channel.

5-23 GATE/FLAG CIRCUIT TROUBLESHOOTING

5-24 Table 5-7 provides troubleshooting procedures for the gate/flag circuit. The troubleshooting steps are keyed to the same numbered steps in the timing flag circuit checkout procedure.

Table 5-5. Address Gate and Strobe Circuit Troubleshooting

TEST NO.	EQUIPMENT CONNECTIONS	INSTRUCTIONS	NORMAL INDICATION	IF INDICATION IS ABNORMAL	IF INDICATION IS NORMAL
1	Connect logic probe or oscilloscope to collector of strobe amplifier Q2.	Address unit and output card slot and touch LOAD OUTPUT.	Positive-going 1μsec pulse.	Proceed to Test 2.	Check connection to CLK inputs of storage registers.
2	Connect logic probe or oscilloscope to Z4, pin 8.	Same as Test 1.	Negative-going 1μsec pulse.	Proceed to Test 3.	Check Q2, R4, R2, and C1.

Table 5-5. Address Gate and Strobe Circuit Troubleshooting (Continued)

TEST NO.	EQUIPMENT CONNECTIONS	INSTRUCTIONS	NORMAL INDICATION	IF INDICATION IS ABNORMAL	IF INDICATION IS NORMAL
3	Connect logic probe or oscilloscope to Z4, pin 6 (DST).	a. Address unit and output card slot and check logic levels at pins 1, 2, 3, 4, and 5 of Z4. b. Touch LOAD OUTPUT push-button.	a. All HI levels. b. Positive-going 1μsec pulse (DST).	Trouble is in Multiprogrammer or programming. Check programming.	Replace address gate Z4.

Table 5-6. Storage Register-Relay Circuit Troubleshooting

TEST NO.	EQUIPMENT CONNECTIONS	INSTRUCTIONS	NORMAL INDICATION	IF INDICATION IS ABNORMAL	IF INDICATION IS NORMAL
1		Replace the data storage IC associated with the failed bit with a known-good IC of the same type. Repeat applicable checkout procedure.	Operation returns to normal.	Proceed to Test 2.	Permanently replace IC.
2	Monitor voltage at the collector of relay driver Q1.	a. Address the output card and program a logical 1 in the bit position associated with the failure. Touch LOAD OUTPUT. b. Repeat the above, but program a logical 0 in the same bit position.	a. +0.2 volts. b. +12 volts.	Check Q1, CR1, K1, and R1. If Q1 is defective, check CR1 for open.	Check programming.

Table 5-7. Gate/Flag Circuit Troubleshooting

TEST NO.	TROUBLE	ISOLATION PROCEDURE	REMEDY
1	a. Both $\overline{CTF}$ and GATE fail to set when DTE, SYE, and data strobe (DST) are issued.	a. Select control word (Bits 15, 14, 13, and 12 on). Program SYE (bit 5 on) and DTE (bit 6 on). Program unit address. Touch LOAD OUTPUT. Address the unit and output card slot. Touch LOAD OUTPUT. Monitor logic levels present at time T_3 at test points (4), (3), (2), and (1), shown in Figure 7-1. IC's Z6, Z5, and Z9, and transistor Q3 are directly involved in this function.	a. Replace any IC (or transistor Q3) that has proper input levels, but an erroneous output.
	b. GATE is set when DTE, SYE, and DST are issued, but $\overline{CTF}$ is not.	b. With oscilloscope, monitor test point 5, Figure 7-1. Repeat Step (a) programming. Waveform at test point (5) should be a negative voltage spike. (It may be necessary to tap LOAD OUTPUT at a rapid rate in order to observe spike.) IC's Z9 and Z5 and transistor Q5 are directly involved in this function.	b. If spike is absent, check Z9, R9, and C4. If spike is present, check Z9, Z5, and Q5.
	c. $\overline{CTF}$ is set when DTE, SYE, and DST are issued, but GATE relay is not energized.	c. Repeat Step (a) programming. With voltmeter, measure collector voltage of Q4, Q9, and Q8. Voltage should be: Q4-C: +0.2V Q9-C: +12V Q8-C: +0.2V	c. If collector voltages are normal, check K2 and CR6. If collector voltages are abnormal, check the suspected transistor and associated components.
2	GATE relay is not reset (deenergized) at start-of-flag.	Energize FLAG RET relay K3 by connecting +12 volts across P2-R(+) and P2-14(COM). Monitor logic levels present at time T_4 at test points (10), (11), (12), and (3), shown in Figure 7-1. (It may be necessary to energize and deenergize K3 several times in order to observe negative spike at test point (12), on oscilloscope.) IC's Z7, Z8, Z9, Z5, and Z6 are directly involved in this function.	Replace any IC that has proper input levels but an erroneous output.
3	$\overline{CTF}$ line is not reset (HI) at end-of-flag.	With oscilloscope, monitor test point (13), Figure 7-1. Deenergize FLAG RET relay K3 and observe negative spike on oscilloscope when relay is deenergized. (It may be necessary to energize and deenergize relay several times in order to observe negative spike.) IC's Z7,	If spike is absent, check Z7 and Z8. If spike is present, check Z5, Z9, and Q5.

Table 5-7. Gate/Flag Circuit Troubleshooting (Continued)

TEST NO.	TROUBLE	ISOLATION PROCEDURE	REMEDY
3		Z8, Z5, and Z9, and transistor Q5 are directly involved in this function.	
4	Both GATE and $\overline{CTF}$ fail to reset when DTE mode is cleared.	Only one IC, Z8, is involved in this function.	Replace Z8 and repeat test. If test fails again, check R8 and C5.

SECTION VI
REPLACEABLE PARTS

6-1 INTRODUCTION

6-2 This section contains information for ordering replacement parts. Table 6-4 lists parts in alphanumeric order by reference designators and provides the following information:

a. Reference Designators. Refer to Table 6-1.

b. Description. Refer to Table 6-2 for abbreviations.

c. Total Quantity (TQ). Given only the first time the part number is listed except in instruments containing many sub-modular assemblies, in which case the TQ appears the first time the part number is listed in each assembly.

d. Manufacturer's Part Number or Type.

e. Manufacturer's Federal Supply Code Number. Refer to Table 6-3 for manufacturer's name and address.

f. Hewlett-Packard Part Number.

g. Recommended Spare Parts Quantity (RS) for complete maintenance of one instrument during one year of isolated service.

h. Parts not identified by a reference designator are listed at the end of Table 6-4 under Mechanical and/or Miscellaneous. The former consists of parts belonging to and grouped by individual assemblies; the latter consists of all parts not immediately associated with an assembly.

6-3 ORDERING INFORMATION

6-4 To order a replacement part, address order or inquiry to your local Hewlett-Packard sales office (see lists at rear of this manual for addresses). Specify the following information for each part: Model, complete serial number, and any Option or special modification (J) numbers of the instrument; Hewlett-Packard part number; circuit reference designator; and description. To order a part not listed in Table 6-4, give a complete description of the part, its function, and its location.

Table 6-1. Reference Designators

A	= assembly	E	= miscellaneous electronic part
B	= blower (fan)	F	= fuse
C	= capacitor	J	= jack, jumper
CB	= circuit breaker	K	= relay
CR	= diode	L	= inductor
DS	= device, signaling (lamp)	M	= meter
P	= plug	V	= vacuum tube, neon bulb, photocell, etc.
Q	= transistor	VR	= zener diode
R	= resistor	X	= socket
S	= switch	Z	= integrated circuit or network
T	= transformer		
TB	= terminal block		
TS	= thermal switch		

Table 6-2. Description Abbreviations

A	= ampere	mfr	= manufacturer
ac	= alternating current	mod.	= modular or modified
assy.	= assembly	mtg	= mounting
bd	= board	n	= nano = 10^{-9}
bkt	= bracket	NC	= normally closed
°C	= degree Centigrade	NO	= normally open
cd	= card	NP	= nickel-plated
coef	= coefficient	Ω	= ohm
comp	= composition	obd	= order by description
CRT	= cathode-ray tube	OD	= outside diameter
CT	= center-tapped	p	= pico = 10^{-12}
dc	= direct current	P.C.	= printed circuit
DPDT	= double pole, double throw	pot.	= potentiometer
DPST	= double pole, single throw	p-p	= peak-to-peak
elect	= electrolytic	ppm	= parts per million
encap	= encapsulated	pvr	= peak reverse voltage
F	= farad	rect	= rectifier
°F	= degree Farenheit	rms	= root mean square
fxd	= fixed	Si	= silicon
Ge	= germanium	SPDT	= single pole, double throw
H	= Henry	SPST	= single pole, single throw
Hz	= Hertz	SS	= small signal
IC	= integrated circuit	T	= slow-blow
ID	= inside diameter	tan.	= tantulum
incnd	= incandescent	Ti	= titanium
k	= kilo = 10^{3}	V	= volt
m	= milli = 10^{-3}	var	= variable
M	= mega = 10^{6}	ww	= wirewound
μ	= micro = 10^{-6}	W	= Watt
met.	= metal		

Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
00629	EBY Sales Co., Inc.	Jamaica, N.Y.
00656	Aerovox Corp.	New Bedford, Mass.
00853	Sangamo Electric Co. S. Carolina Div.	Pickens, S.C.
01121	Allen Bradley Co.	Milwaukee, Wis.
01255	Litton Industries, Inc.	Beverly Hills, Calif.
01281	TRW Semiconductors, Inc.	Lawndale, Calif.
01295	Texas Instruments, Inc. Semiconductor-Components Div.	Dallas, Texas
01686	RCL Electronics, Inc.	Manchester, N.H.
01930	Amerock Corp.	Rockford, Ill.
02107	Sparta Mfg. Co.	Dover, Ohio
02114	Ferroxcube Corp.	Saugerties, N.Y.
02606	Fenwal Laboratories	Morton Grove, Ill.
02660	Amphenol Corp.	Broadview, Ill.
02735	Radio Corp. of America, Solid State and Receiving Tube Div.	Somerville, N.J.
03508	G.E. Semiconductor Products Dept.	Syracuse, N.Y.
03797	Eldema Corp.	Compton, Calif.
03877	Transitron Electronic Corp.	Wakefield, Mass.
03888	Pyrofilm Resistor Co. Inc.	Cedar Knolls, N.J.
04009	Arrow, Hart and Hegeman Electric Co.	Hartford, Conn.
04072	ADC Electronics, Inc.	Harbor City, Calif.
04213	Caddell & Burns Mfg. Co. Inc.	Mineola, N.Y.
04404	*Hewlett-Packard Co. Palo Alto Div.	Palo Alto, Calif.
04713	Motorola Semiconductor Prod. Inc.	Phoenix, Arizona
05277	Westinghouse Electric Corp. Semiconductor Dept.	Youngwood, Pa.
05347	Ultronix, Inc.	Grand Junction, Colo.
05820	Wakefield Engr. Inc.	Wakefield, Mass.
06001	General Elect. Co. Electronic Capacitor & Battery Dept.	Irmo, S.C.
06004	Bassik Div. Stewart-Warner Corp.	Bridgeport, Conn.
06486	IRC Div. of TRW Inc. Semiconductor Plant	Lynn, Mass.
06540	Amatom Electronic Hardware Co. Inc.	New Rochelle, N.Y.
06555	Beede Electrical Instrument Co.	Penacook, N.H.
06666	General Devices Co. Inc.	Indianapolis, Ind.
06751	Semcor Div. Components, Inc.	Phoenix, Arizona
06776	Robinson Nugent, Inc.	New Albany, Ind.
06812	Torrington Mfg. Co., West Div.	Van Nuys, Calif.
07137	Transistor Electronics Corp.	Minneapolis, Minn.
07138	Westinghouse Electric Corp. Electronic Tube Div.	Elmira, N.Y.
07263	Fairchild Camera and Instrument Corp. Semiconductor Div.	Mountain View, Calif.
07387	Birtcher Corp., The	Los Angeles, Calif.
07397	Sylvania Electric Prod. Inc. Sylvania Electronic Systems Western Div.	Mountain View, Calif.
07716	IRC Div. of TRW Inc. Burlington Plant	Burlington, Iowa
07910	Continental Device Corp.	Hawthorne, Calif.
07933	Raytheon Co. Components Div. Semiconductor Operation	Mountain View, Calif.
08484	Breeze Corporations, Inc.	Union, N.J.
08530	Reliance Mica Corp.	Brooklyn, N.Y.
08717	Sloan Company, The	Sun Valley, Calif.
08730	Vemaline Products Co. Inc.	Wyckoff, N.J.
08806	General Elect. Co. Miniature Lamp Dept.	Cleveland, Ohio
08863	Nylomatic Corp.	Norrisville, Pa.
08919	RCH Supply Co.	Vernon, Calif.
09021	Airco Speer Electronic Components	Bradford, Pa.
09182	*Hewlett-Packard Co. New Jersey Div.	Berkeley Heights, N.J.
09213	General Elect. Co. Semiconductor Prod. Dept.	Buffalo, N.Y.
09214	General Elect. Co. Semiconductor Prod. Dept.	Auburn, N.Y.
09353	C & K Components Inc.	Newton, Mass.
09922	Burndy Corp.	Norwalk, Conn.
11115	Wagner Electric Corp. Tung-Sol Div.	Bloomfield, N.J.
11236	CTS of Berne, Inc.	Berne, Ind.
11237	Chicago Telephone of Cal. Inc.	So. Pasadena, Calif.
11502	IRC Div. of TRW Inc. Boone Plant	Boone, N.C.
11711	General Instrument Corp Rectifier Div.	Newark, N.J.
12136	Philadelphia Handle Co. Inc.	Camden, N.J.
12615	U.S. Terminals, Inc.	Cincinnati, Ohio
12617	Hamlin Inc.	Lake Mills, Wisconsin
12697	Clarostat Mfg. Co. Inc.	Dover, N.H.
13103	Thermalloy Co.	Dallas, Texas
14493	*Hewlett-Packard Co. Loveland Div.	Loveland, Colo.
14655	Cornell-Dubilier Electronics Div. Federal Pacific Electric Co.	Newark, N.J.
14936	General Instrument Corp. Semiconductor Prod. Group	Hicksville, N.Y.
15801	Fenwal Elect.	Framingham, Mass.
16299	Corning Glass Works, Electronic Components Div.	Raleigh, N.C.

*Use Code 28480 assigned to Hewlett-Packard Co., Palo Alto, California

Table 6-3. Code List of Manufacturers (Continued)

CODE NO.	MANUFACTURER	ADDRESS
16758	Delco Radio Div. of General Motors Corp.	Kokomo, Ind.
17545	Atlantic Semiconductors, Inc.	Asbury Park, N.J.
17803	Fairchild Camera and Instrument Corp Semiconductor Div. Transducer Plant	Mountain View, Calif.
17870	Daven Div. Thomas A. Edison Industries McGraw-Edison Co.	Orange, N.J.
18324	Signetics Corp.	Sunnyvale, Calif.
19315	Bendix Corp. The Navigation and Control Div.	Teterboro, N.J.
19701	Electra/Midland Corp.	Mineral Wells, Texas
21520	Fansteel Metallurgical Corp.	No. Chicago, Ill.
22229	Union Carbide Corp. Electronics Div.	Mountain View, Calif.
22753	UID Electronics Corp.	Hollywood, Fla.
23936	Pamotor, Inc.	Pampa, Texas
24446	General Electric Co.	Schenectady, N.Y.
24455	General Electric Co. Lamp Div. of Consumer Prod. Group	Nela Park, Cleveland, Ohio
24655	General Radio Co.	West Concord, Mass.
24681	LTV Electrosystems Inc Memcor/Components Operations	Huntington, Ind.
26982	Dynacool Mfg. Co. Inc.	Saugerties, N.Y.
27014	National Semiconductor Corp.	Santa Clara, Calif.
28480	Hewlett-Packard Co.	Palo Alto, Calif.
28520	Heyman Mfg. Co.	Kenilworth, N.J.
28875	IMC Magnetics Corp. New Hampshire Div.	Rochester, N.H.
31514	SAE Advance Packaging, Inc.	Santa Ana, Calif.
31827	Budwig Mfg. Co.	Ramona, Calif.
33173	G.E. Co. Tube Dept.	Owensboro, Ky.
35434	Lectrohm, Inc.	Chicago, Ill.
37942	P.R. Mallory & Co. Inc.	Indianapolis, Ind.
42190	Muter Co.	Chicago, Ill.
43334	New Departure-Hyatt Bearings Div. General Motors Corp.	Sandusky, Ohio
44655	Ohmite Manufacturing Co.	Skokie, Ill.
46384	Penn Engr. and Mfg. Corp.	Doylestown, Pa.
47904	Polaroid Corp.	Cambridge, Mass.
49956	Raytheon Co.	Lexington, Mass.
55026	Simpson Electric Co. Div. of American Gage and Machine Co.	Chicago, Ill.
56289	Sprague Electric Co.	North Adams, Mass.
58474	Superior Electric Co.	Bristol, Conn.
58849	Syntron Div. of FMC Corp.	Homer City, Pa.
59730	Thomas and Betts Co.	Philadelphia, Pa.
61637	Union Carbide Corp.	New York, N.Y.
63743	Ward Leonard Electric Co.	Mt. Vernon, N.Y.

CODE NO.	MANUFACTURER	ADDRESS
70563	Amperite Co. Inc.	Union City, N.J.
70901	Beemer Engrg. Co.	Fort Washington, Pa.
70903	Belden Corp.	Chicago, Ill.
71218	Bud Radio, Inc.	Willoughby, Ohio
71279	Cambridge Thermionic Corp.	Cambridge, Mass.
71400	Bussmann Mfg. Div. of McGraw & Edison Co.	St. Louis, Mo.
71450	CTS Corp.	Elkhart, Ind.
71468	I.T.T. Cannon Electric Inc.	Los Angeles, Calif.
71590	Globe-Union Inc. Centralab Div.	Milwaukee, Wis.
71700	General Cable Corp. Cornish Wire Co. Div.	Williamstown, Mass.
71707	Coto Coil Co. Inc.	Providence, R.I.
71744	Chicago Miniature Lamp Works	Chicago, Ill.
71785	Cinch Mfg. Co. and Howard B. Jones Div.	Chicago, Ill.
71984	Dow Corning Corp.	Midland, Mich.
72136	Electro Motive Mfg. Co. Inc.	Willimantic, Conn.
72619	Dialight Corp.	Brooklyn, N.Y.
72699	General Instrument Corp.	Newark, N.J.
72765	Drake Mfg. Co.	Harwood Heights, Ill.
72962	Elastic Stop Nut Div. of Amerace Esna Corp.	Union, N.J.
72982	Erie Technological Products Inc.	Erie, Pa.
73096	Hart Mfg. Co.	Hartford, Conn.
73138	Beckman Instruments Inc. Helipot Div.	Fullerton, Calif.
73168	Fenwal, Inc.	Ashland, Mass.
73293	Hughes Aircraft Co. Electron Dynamics Div.	Torrance, Calif.
73445	Amperex Electronic Corp.	Hicksville, N.Y.
73506	Bradley Semiconductor Corp.	New Haven, Conn.
73559	Carling Electric, Inc.	Hartford, Conn.
73734	Federal Screw Products, Inc.	Chicago, Ill.
74193	Heinemann Electric Co.	Trenton, N.J.
74545	Hubbell Harvey Inc.	Bridgeport, Conn.
74868	Amphenol Corp. Amphenol RF Div.	Danbury, Conn.
74970	E.F. Johnson Co.	Waseca, Minn.
75042	IRC Div. of TRW, Inc.	Philadelphia, Pa.
75183	*Howard B. Jones Div. of Cinch Mfg. Corp.	New York, N.Y.
75376	Kurz and Kasch, Inc.	Dayton, Ohio
75382	Kilka Electric Corp.	Mt. Vernon, N.Y.
75915	Littlefuse, Inc.	Des Plaines, Ill.
76381	Minnesota Mining and Mfg. Co.	St. Paul, Minn.
76385	Minor Rubber Co. Inc.	Bloomfield, N.J.
76487	James Millen Mfg. Co. Inc.	Malden, Mass.
76493	J.W. Miller Co.	Compton, Calif.

*Use Code 71785 assigned to Cinch Mfg. Co., Chicago, Ill.

Table 6-3. Code List of Manufacturers (Continued)

CODE NO.	MANUFACTURER	ADDRESS
76530	Cinch	City of Industry, Calif.
76854	Oak Mfg. Co. Div. of Oak Electro/Netics Corp.	Crystal Lake, Ill.
77068	Bendix Corp., Electrodynamics Div.	No. Hollywood, Calif.
77122	Palnut Co.	Mountainside, N.J.
77147	Patton-MacGuyer Co.	Providence, R.I.
77221	Phaostron Instrument and Electronic Co.	South Pasadena, Calif.
77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.
77342	American Machine and Foundry Co. Potter and Brumfield Div.	Princeton, Ind.
77630	TRW Electronic Components Div.	Camden, N.J.
77764	Resistance Products Co.	Harrisburg, Pa.
78189	Illinois Tool Works Inc. Shakeproof Div.	Elgin, Ill.
78452	Everlock Chicago, Inc.	Chicago, Ill.
78488	Stackpole Carbon Co.	St. Marys, Pa.
78526	Stanwyck Winding Div. San Fernando Electric Mfg. Co. Inc.	Newburgh, N.Y.
78553	Tinnerman Products, Inc.	Cleveland, Ohio
78584	Stewart Stamping Corp.	Yonkers, N.Y.
79136	Waldes Kohinoor, Inc.	L.I.C., N.Y.
79307	Whitehead Metals Inc.	New York, N.Y.
79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.
79963	Zierick Mfg. Co.	Mt. Kisco, N.Y.
80031	Mepco Div. of Sessions Clock Co.	Morristown, N.J.
80294	Bourns, Inc.	Riverside, Calif.
81042	Howard Industries Div. of Msl Ind. Inc.	Racine, Wisc.
81073	Grayhill, Inc.	La Grange, Ill.
81483	International Rectifier Corp.	El Segundo, Calif.
81751	Columbus Electronics Corp.	Yonkers, N.Y.
82099	Goodyear Sundries & Mechanical Co. Inc.	New York, N.Y.
82142	Airco Speer Electronic Components	Du Bois, Pa.
82219	Sylvania Electric Products Inc. Electronic Tube Div. Receiving Tube Operations	Emporium, Pa.
82389	Switchcraft, Inc.	Chicago, Ill.
82647	Metals and Controls Inc. Control Products Group	Attleboro, Mass.
82866	Research Products Corp.	Madison, Wis.
82877	Rotron Inc.	Woodstock, N.Y.
82893	Vector Electronic Co.	Glendale, Calif.
83058	Carr Fastener Co.	Cambridge, Mass.
83186	Victory Engineering Corp.	Springfield, N.J.
83298	Bendix Corp. Electric Power Div.	Eatontown, N.J.
83330	Herman H. Smith, Inc.	Brooklyn, N.Y.
83385	Central Screw Co.	Chicago, Ill.
83501	Gavitt Wire and Cable Div. of Amerace Esna Corp.	Brookfield, Mass.
83508	Grant Pulley and Hardware Co.	West Nyack, N.Y.
83594	Burroughs Corp. Electronic Components Div.	Plainfield, N.J.
83835	U.S. Radium Corp.	Morristown, N.J.
83877	Yardeny Laboratories, Inc.	New York, N.Y.
84171	Arco Electronics, Inc.	Great Neck, N.Y.
84411	TRW Capacitor Div.	Ogallala, Neb.
86684	RCA Corp. Electronic Components	Harrison, N.J.
86838	Rummel Fibre Co.	Newark, N.J.
87034	Marco & Oak Industries a Div. of Oak Electro/netics Corp.	Anaheim, Calif.
87216	Philco Corp. Lansdale Div.	Lansdale, Pa.
87585	Stockwell Rubber Co. Inc.	Philadelphia, Pa.
87929	Tower-Olschan Corp.	Bridgeport, Conn.
88140	Cutler-Hammer Inc. Power Distribution and Control Div. Lincoln Plant	Lincoln, Ill.
88245	Litton Precision Products Inc, USECO Div. Litton Industries	Van Nuys, Calif.
90634	Gulton Industries Inc.	Metuchen, N.J.
90763	United-Car Inc.	Chicago, Ill.
91345	Miller Dial and Nameplate Co.	El Monte, Calif.
91418	Radio Materials Co.	Chicago, Ill.
91506	Augat, Inc.	Attleboro, Mass.
91637	Dale Electronics, Inc.	Columbus, Neb.
91662	Elco Corp.	Willow Grove, Pa.
91929	Honeywell Inc. Div. Micro Switch	Freeport, Ill.
92825	Whitso, Inc.	Schiller Pk., Ill.
93332	Sylvania Electric Prod. Inc. Semiconductor Prod. Div.	Woburn, Mass.
93410	Essex Wire Corp. Stemco Controls Div.	Mansfield, Ohio
94144	Raytheon Co. Components Div. Ind. Components Oper.	Quincy, Mass.
94154	Wagner Electric Corp. Tung-Sol Div.	Livingston, N.J.
94222	Southco Inc.	Lester, Pa.
95263	Leecraft Mfg. Co. Inc.	L.I.C., N.Y.
95354	Methode Mfg. Co.	Rolling Meadows, Ill.
95712	Bendix Corp. Microwave Devices Div.	Franklin, Ind.
95987	Weckesser Co. Inc.	Chicago, Ill.
96791	Amphenol Corp. Amphenol Controls Div.	Janesville, Wis.
97464	Industrial Retaining Ring Co.	Irvington, N.J.
97702	IMC Magnetics Corp. Eastern Div.	Westbury, N.Y.
98291	Sealectro Corp.	Mamaroneck, N.Y.
98410	ETC Inc.	Cleveland, Ohio
98978	International Electronic Research Corp.	Burbank, Calif.
99934	Renbrandt, Inc.	Boston, Mass.

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
69330A-A4	Relay Output Card	1		28480	69330-60020	
A4A1	Relay - Driver Circuit					
CR1	Diode, Si. 250mW 200V	1		28480	1901-0033	1
K1	Relay, Reed, 1 Form A 12Vdc	1		28480	0490-0926	1
Q1	SS NPN Si.	1		28480	1854-0071	1
R1	fxd, comp 3kΩ ±5% $\frac{1}{4}$W	1	CB-3025	01121	0683-3025	1
A4A2-A4A12	Same as A4A1	11				
A4C1	fxd, mylar 0.001μF 200V	1	192P10292	56289	0160-0153	1
C2, 3	fxd, elect 1.0μF 35V	5	150D105X9035A2	56289	0180-0291	1
C4-C7	fxd, mylar 0.0022μF 200V	4	192P22292	56289	0160-0154	1
C8-C10	fxd, elect 1.0μF 35V		150D105X9035A2	56289	0180-0291	
C11, 12	Arc Suppression (not supplied)					
CR2-CR6	Diode, Si. 250mW 200V	5		28480	1901-0033	5
K2, 3	Relay, Reed, 1 Form A 12Vdc	2		28480	0490-0926	1
Q2-Q6	SS NPN Si.	9		28480	1854-0071	6
Q7	SS PNP Si.	1		28480	1853-0099	1
Q8, 9	SS NPN Si.			28480	1854-0071	
Q10	SS PNP Si.	1		28480	1853-0037	1
Q11, 12	SS NPN Si.			28480	1854-0071	
R2, 3	fxd, comp 3kΩ ±5% $\frac{1}{4}$W	7	CB-3025	01121	0683-3025	2
R4	fxd, comp 1kΩ ±5% $\frac{1}{4}$W	2	CB-1025	01121	0683-1025	1
R5	NOT USED	-	-	-	-	-
R6, 7	fxd, comp 2kΩ ±5% $\frac{1}{4}$W	2	CB-2025	01121	0683-2025	1
R8-R11	fxd, comp 200Ω ±5% $\frac{1}{4}$W	4	CB-2015	01121	0683-2015	1
R12	fxd, comp 330Ω ±5% $\frac{1}{4}$W	1	CB-3315	01121	0683-3315	1
R13	fxd, comp 51Ω ±5% $\frac{1}{4}$W	1	CB-5105	01121	0683-5105	1
R14-R16	fxd, comp 100kΩ ±5% $\frac{1}{4}$W	3	CB-1045	01121	0683-1045	1
R17	fxd, comp 20kΩ ±5% $\frac{1}{4}$W	2	CB-2035	01121	0683-2035	1
R18	fxd, comp 10kΩ ±5% $\frac{1}{4}$W	3	CB1035	01121	0683-1035	1
R19-R21	fxd, comp 3kΩ ±5% $\frac{1}{4}$W		CB-3025	01121	0683-3025	
R22, 23	fxd, comp 10kΩ ±5% $\frac{1}{4}$W		CB-1035	01121	0683-1035	
R24	fxd, comp 510Ω ±5% $\frac{1}{4}$W	1	CB-5115	01121	0683-5115	1
R25, 26	fxd, comp 3kΩ ±5% $\frac{1}{4}$W		CB-3025	01121	0683-3025	
R27	fxd, comp 1kΩ ±5% $\frac{1}{4}$W		CB-1025	01121	0683-1025	
R28, 29	Arc Suppression (not supplied)					
R30	fxd, comp 20kΩ ±5% $\frac{1}{4}$W		CB-2035	01121	0683-2035	
Z1-Z3	Quad Bistable Latch, IC	3	SN7475N	01295	1820-0301	3
Z4	8-Input NAND Gate, IC	1	SN7430N	01295	1820-0070	1
Z5	Dual 4-Input NAND Gate, IC	1	SN7420N	01295	1820-0069	1
Z6-Z9	Quad 2-Input NAND Gate	4	SN7400N	01295	1820-0054	4
	MECHANICAL PARTS					
	Socket, IC, Z1-Z3	3	316-AG5D-3R	91506	1200-0767	3
	Socket, IC, Z4-Z9	6	314-AG5D-3R	91506	1200-0768	2
	Extractor Handle with Roll Pin	1	6100	31514	0403-0180	
	Connector Assembly	1		28480	5060-7934	
	Connector, 30 Pin	1	251-15-30-261	71785	1251-0159	
	Hood, Connector	1		28480	5040-0051	
	Clamp, Cable	1		28480	00562-00022	
	Screw, Pan Head 4-40 x 3/8	2		28480	2200-0143	
	Box, Corrugated	1		28480	9211-0418	

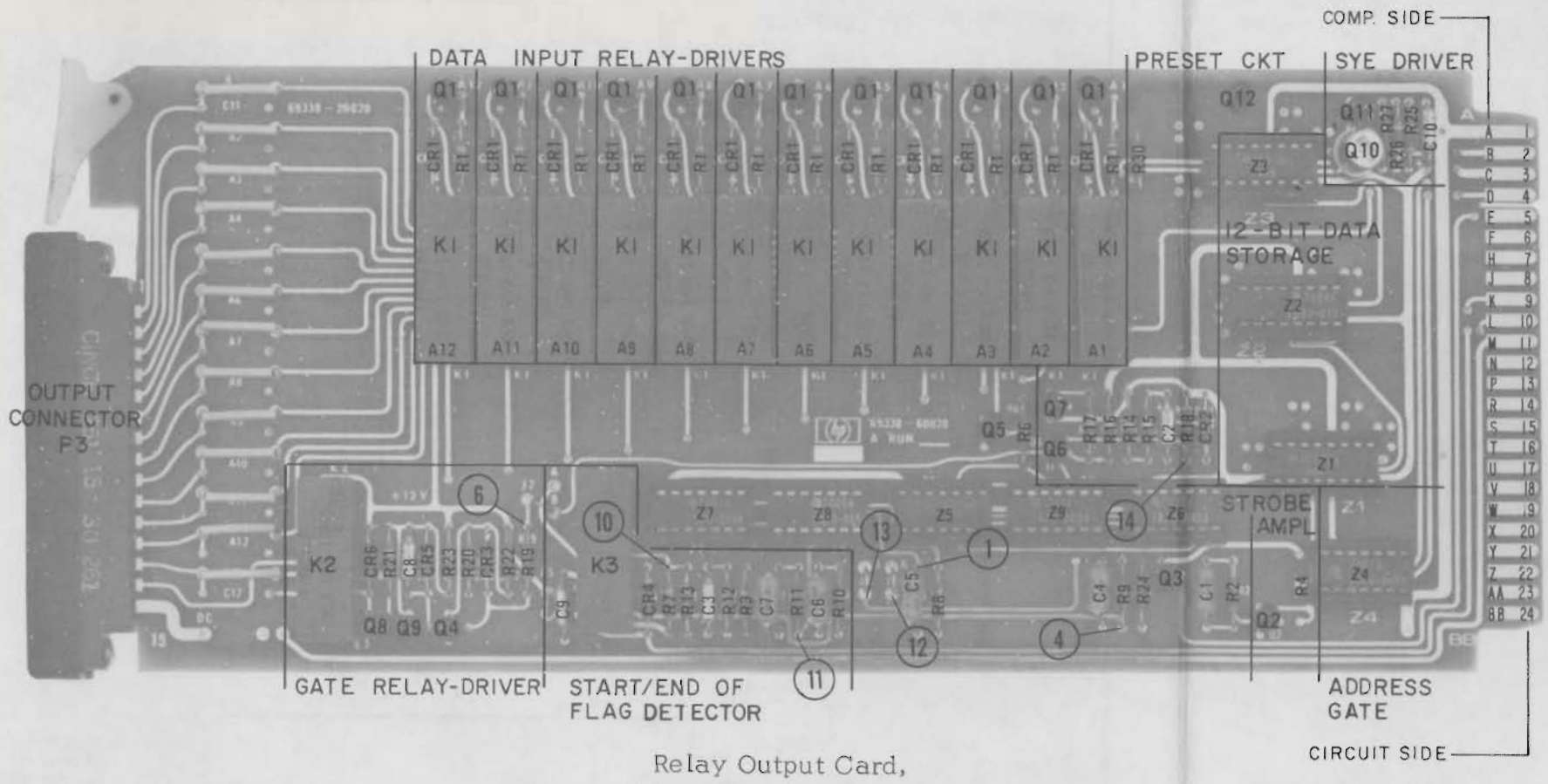
SECTION VII
CIRCUIT DIAGRAMS

7-1 COMPONENT LOCATION ILLUSTRATION

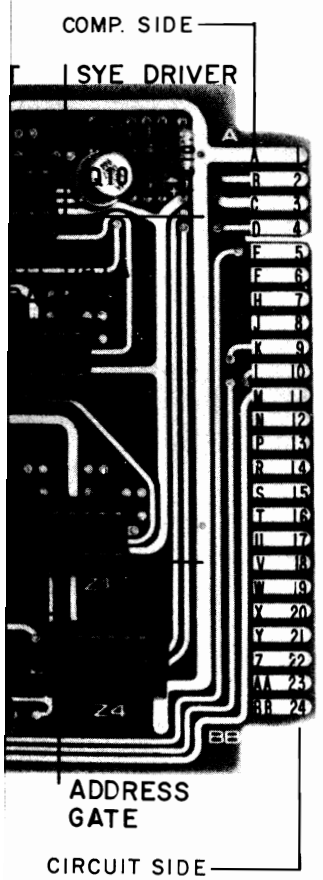
7-2 The component location illustration for the Model 69330A is given in Figure 7-1, Sheets 1 and 2. The illustration shows the physical location and reference designations for parts mounted on the printed circuit card.

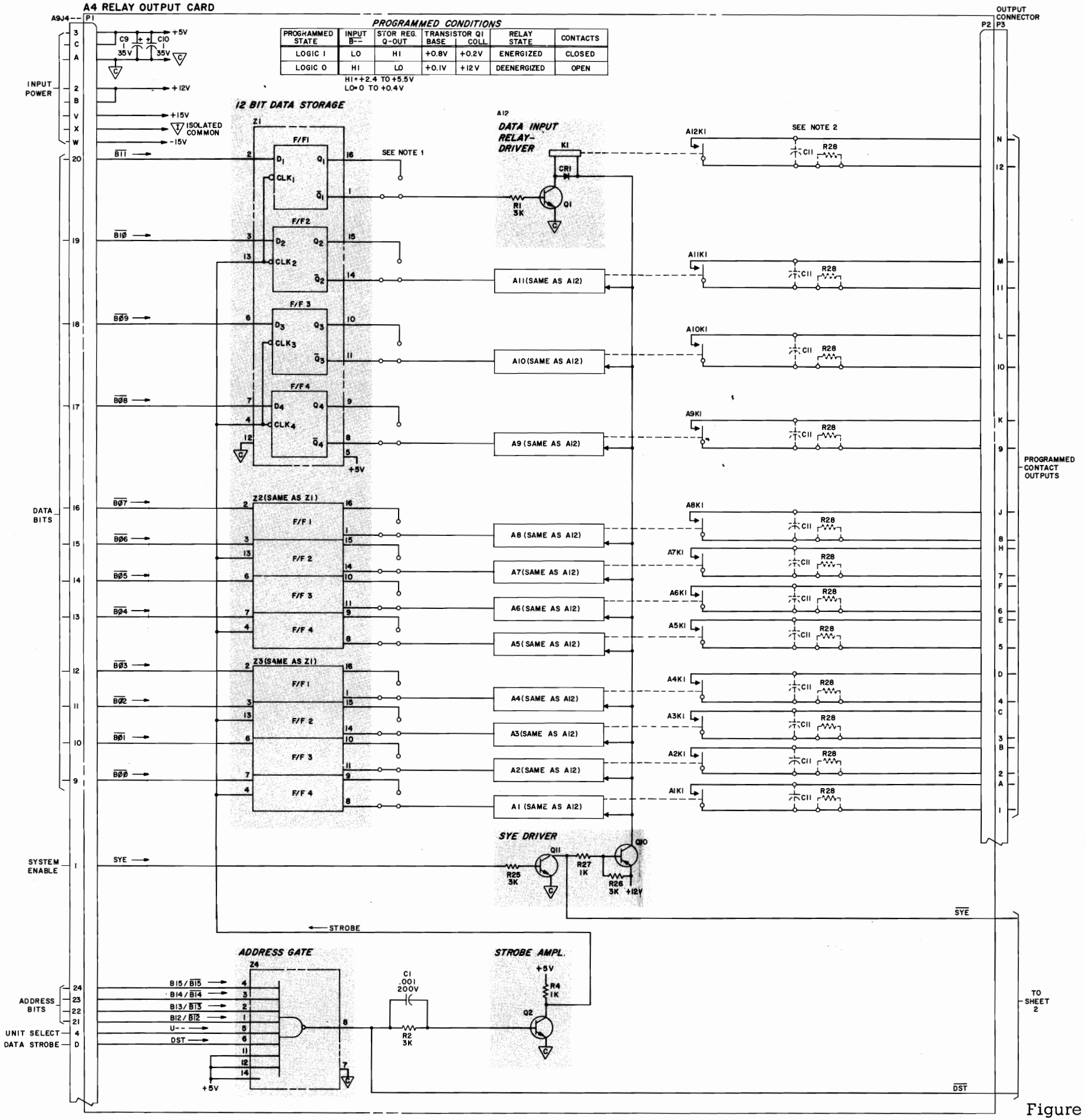
7-3 SCHEMATIC DIAGRAM

7-4 The schematic diagram of the Model 69330A is presented on two sheets of Figure 7-1. Sheet 1 illustrates the data storage and output circuits of the 69330A, while Sheet 2 illustrates the gate/flag circuits of the 69330A. The test points (encircled numbers) shown on the schematic diagrams coincide with test points on the component location illustration.



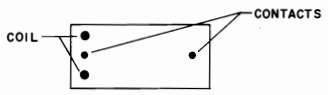
Relay Output Card,
Component Locations



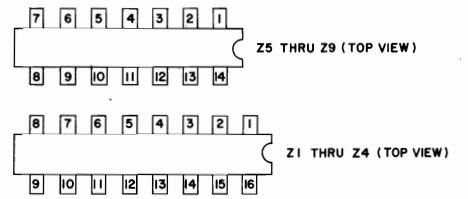


NOTES:

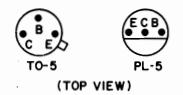
1. THE $\overline{Q}$ OUTPUTS OF THE DATA STORAGE REGISTERS ENERGIZE THE DATA RELAYS WHEN A LOGICAL 1 IS PROGRAMMED. THIS RELATIONSHIP CAN BE REVERSED (WHERE A PROGRAMMED LOGICAL 0 ENERGIZES THE RELAY) BY CUTTING THE TRACK BETWEEN THE $\overline{Q}$ OUTPUT OF THE F/F AND THE RELAY DRIVER INPUT AND CONNECTING A JUMPER FROM THE Q OUTPUT TO THE RELAY DRIVER INPUT.
2. PADS ARE PROVIDED ON THE PRINTED CIRCUIT CARD FOR INSTALLING ARC-SUPPRESSION COMPONENTS IN THE RELAY CONTACT CIRCUIT. REFER TO SECTION III OF INSTRUCTION MANUAL FOR COMPONENT SELECTION DATA.
3. THE JUMPER CONNECTIONS SHOWN ON THE SCHEMATIC DIAGRAM REPRESENT THE STANDARD CONFIGURATION FOR ALL RELAY OUTPUT CARDS. THE PURPOSE AND APPLICATIONS OF ALTERNATE JUMPER CONNECTIONS ARE DESCRIBED IN SECTION III OF THIS MANUAL.
4. DATA RELAY CONNECTIONS ARE AS FOLLOWS:



5. PIN LOCATIONS OF THE INTEGRATED CIRCUITS USED ON THIS CARD ARE AS FOLLOWS:



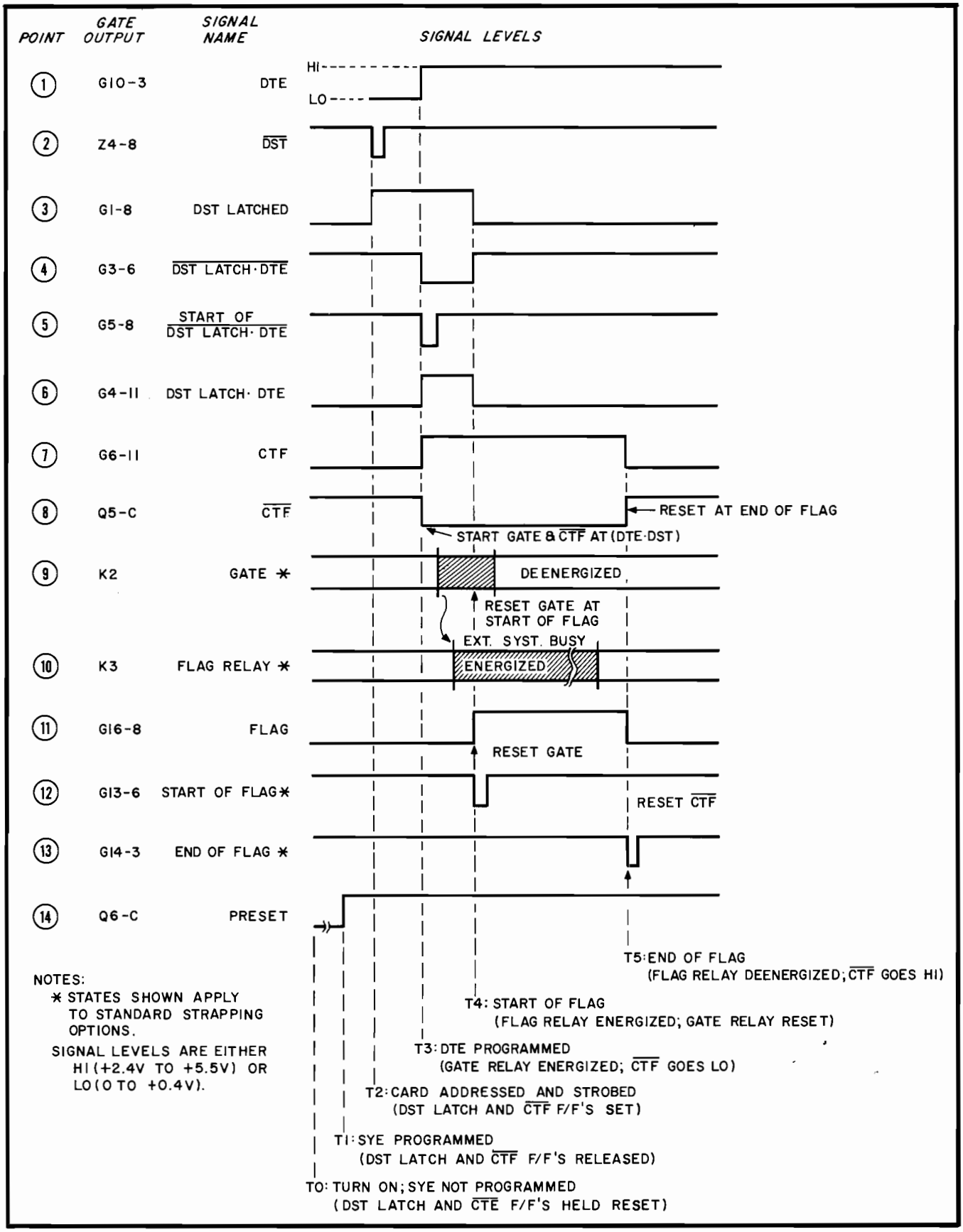
6. PIN LOCATIONS FOR TRANSISTORS ARE AS FOLLOWS:



7. ALL RESISTORS ARE 1/4W, ±5%, UNLESS OTHERWISE INDICATED.
8. ALL CAPACITORS IN MICROFARADS, UNLESS OTHERWISE INDICATED.

Figure 7-1 (Sheet 1). Data Storage and Output Circuits, Schematic Diagram

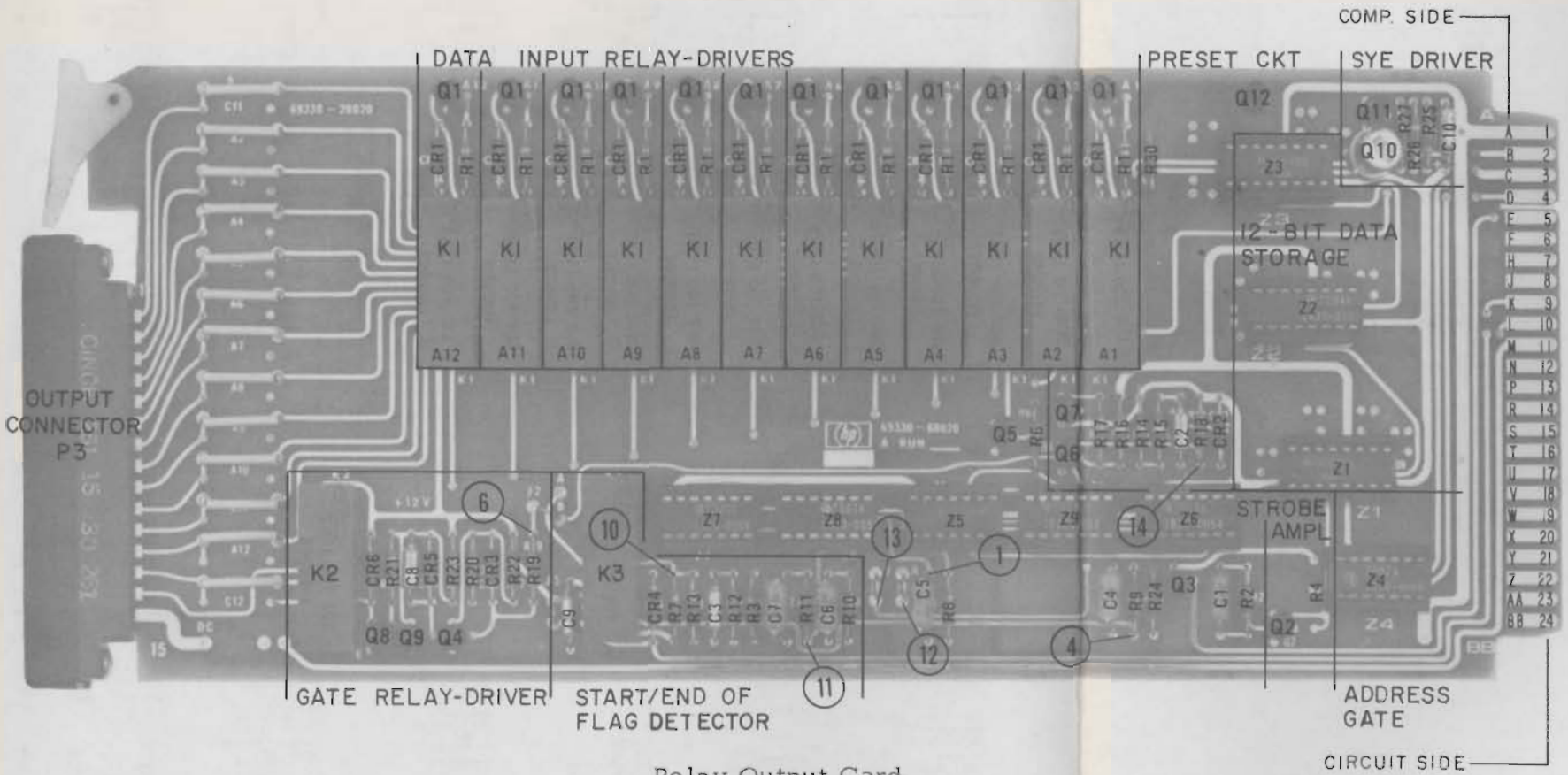
GATE/FLAG CIRCUIT WAVEFORMS



NOTES:

* STATES SHOWN APPLY TO STANDARD STRAPPING OPTIONS.

SIGNAL LEVELS ARE EITHER HI (+2.4V TO +5.5V) OR LO (0 TO +0.4V).



Relay Output Card,
Component Locations

RELAY OUTPUT CARD

OUTPUT CONNECTOR P2 P3

SEE NOTE 2

GATE K2

+12V

CR6

C12

R29

GATE OUTPUT

P

13

TO EXTERNAL TIMING CIRCUIT

9

GATE RELAY DRIVERS

+12V

R23 10K

CR5

C8 35V

R21 3K

Q8

R22 10K

Q9

CR3

R20 3K

Q4

R19 3K

DST LATCHED·DTE

START OF DST·DTE DETECTOR

DST LATCHED·DTE

SEE NOTE 3

A

DTE

Z6 G3

Z6 G4

J2

Z9 G5

R9 200

C4 .0022

DST LATCH F/F

F/F G1

Z6

Z5 G2

DST LATCHED

END DTE

FROM SHEET 1

DST

A9J4-P1

DATA TRANSFER ENABLE

5

DTE

+5V

Q3

Z6 G10

R24 510

END OF DTE DETECTOR

Z8 G11

Z8 G12

END DTE

R8 200

C5 .0022

1

2

3

4

5

6

V_{C4}

START/END OF FLAG DETECTOR

Z8 G13

J3 B

R10 200

C6 .0022

Z8 G14

J4 A

R11 200

C7 .0022

Z7 G15

Z7 G16

Z7 G17

Z7 G18

R3 3K

CONTACT BOUNCE SUPPRESSOR

+5V

R7 2K

R12 330

R13 51

C3 1 35V

K3 CONTACT BOUNCE

+5V

0V

V_{CE}

R13·C3

R7·R13·C3

SEE NOTE 3

+12V +15V -15V

J5

J7

FLAG K3

CR42

J6

R

14

15

S

FROM EXTERNAL TIMING CIRCUIT

CTF CONTROL F/F

COMMON TIMING FLAG

7

CTF

Q5

CTF

R6 2K

F/F G6

START DST·DTE

Z9 G7

END DTE

Z5 9

PRESET CIRCUIT

FROM SHEET 1

SYE

+12V

Q12

+5V

R18 10K

R30 20K

Q6

R17 20K

R16 100K

+5V

+5V

CR2

R14 100K

C2 1 35V

R15 100K

Q7

+5V

Z9 G9

Z9 G8

PRE

8

10

11

12

13

14

Figure 7-1 (Sheet 2). Gate/Flag Circuits, Schematic Diagram