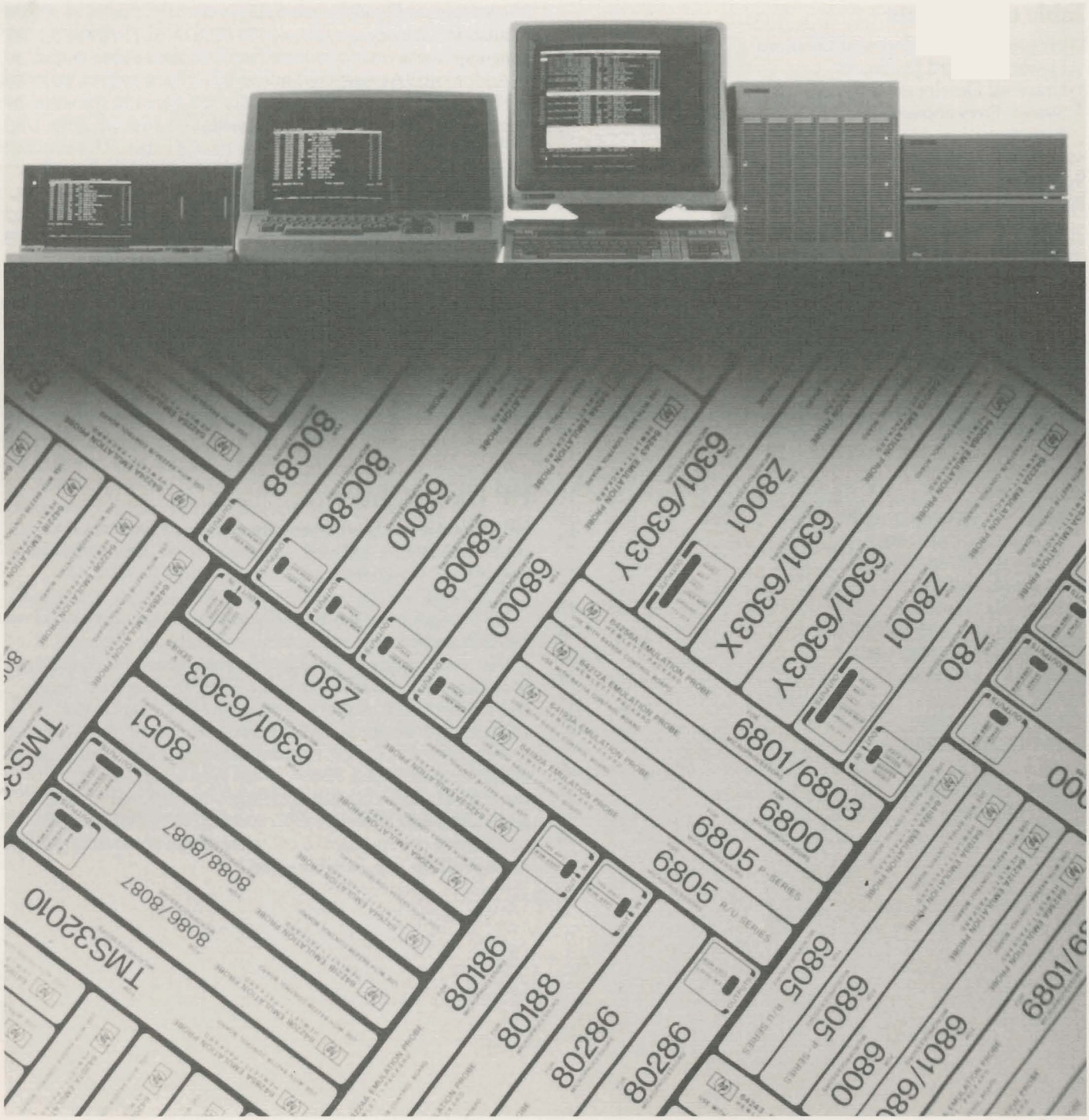
Kenni Rogers.

HEWLETT PACKARD

Real-time Emulators for 8 and 16-bit Microprocessors

HP 64100 Series
HP 64200 Series

Technical Data December 1986



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HP DesignCenter

HP DesignCenter is an integrated design environment that combines systems, software, and support for computer-aided engineering, design, test, and manufacturing (CAE/CAD/CAT/CAM).

HP DesignCenter dramatically boosts the productivity of individual electronic, mechanical, and software engineers within your company. Then it links their efforts for significant company-wide productivity gains. With an integrated design environment such as that provided by HP DesignCenter, engineers can design products faster, with higher quality and fewer errors. At Hewlett-Packard, this is neither a new commitment, nor a new idea. Rather, it has been a continuous commitment to a constant challenge—helping you to design and build better, more reliable products. HP's DesignCenter represents a commitment to complete design automation—from concept all the way to production.

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Microprocessor Development Solutions

Hewlett-Packard Emulators

Hewlett-Packard offers a wide selection of emulators to support microprocessor-based product development. These emulators provide the essential link between software development and hardware/software integration. Code developed on the HP 64000 system or compatible host computers is executed on the emulation subsystem and user's target system, if available, for real-time debugging and logic analysis.

Hewlett-Packard emulators are part of an integrated set of design and development tools that include Teamwork/SA/RT/SD for structured analysis and design; cross compilers and assemblers/linkers for programming at the most efficient level; directed-syntax softkeys and an easy-to-use, responsive editor to streamline software development and documentation; and analysis subsystems which provide powerful measurements to investigate program execution, timing relationships, system performance, and processor activity. Convenience, ease of use, and measurement power help you produce a better product in less time to gain a competitive edge.

Universal Development System

HP 64000 products comprise a universal development system that provides development support for most microprocessor families. Currently, there are emulators for more than 40 microprocessors. When additional emulators are introduced to support popular new processors, they are easily integrated with your existing HP 64000 real-time analysis tools. This flexibility protects the capital investment in instrumentation, since new projects and goals can be accommodated with low-cost add-ons rather than total replacement of development systems and tools.

System Environment

Hewlett-Packard supports the universal development system with two system platforms: a general-purpose, multiuser computer and a dedicated, stand-alone workstation.

The HP 64000-UX Microprocessor Development Environment is based on the HP 9000 Series 300 general-purpose computer, running the HP-UX* operating system. This workstation platform is common to the design engineering tools of HP DesignCenter. The multiuser capability of the Series 300 allows for shared hardware and software resources among system users. Multiple window capability allows integration and debug tasks to be viewed simultaneously, for convenient observation of interactive debug information. The HP-UX operating environment supports user-programmable command files for repetitive and complex test routines. HP 64000-UX systems can be networked and expanded for large design teams, and can be easily connected to other host computers or system resources.

The HP 64000-UX environment is compatible with the dedicated, stand-alone HP 64100A and 64110A Logic Development Stations. The same emulation and analysis card sets for most subsystems are used in both the HP 64000 Logic Development System and the HP 64000-UX Microprocessor Development Environment. In addition, these hardware platforms can be networked via high-speed link or RS-232 for maximum productivity.

Features

- Emulators for 8-bit, 16-bit, and 32-bit microprocessors
- Real-time emulation for evaluating target system performance and critical timing relationships
- Multiple emulation capabilities for multiprocessor product designs
- Display and modify memory, registers, and I/O ports
- Disassembly of microprocessor instruction set
- Source-line referencing
- Symbolic debugging for emulation and analysis operations
- Compatible and interactive high-performance logic analyzers for hardware, software, and software performance analysis
- Run control, single stepping, run from, and run until
- HP 64000 system resources (disc files, printer, development station keyboard, display, and RS-232 port) can be used to simulate target system I/O
- Emulation memory available from 32 kbytes to 1 Mbyte, as appropriate
- Memory assigned by blocks to target system or emulation memory over the microprocessor's entire address space; designated as ROM, RAM, or illegal address space
- User-definable emulator kit for custom emulation support

*HP-UX is Hewlett-Packard's implementation of the UNIX operating system. UNIX is a registered trademark of AT&T in the U.S.A. and other countries.

Measurement System Configuration

An HP 64000 emulation subsystem consists of an emulation control card, emulation pod, and operating software. Most emulators require a separate emulation memory system; others incorporate emulation memory in the emulation subsystem. Refer to the ordering information for a specific emulator or the memory chart on page 38. Up to 1 Mbyte of emulation memory may be added, as appropriate for the target microprocessor, in 32, 64, or 128-kbyte increments.

An emulation bus analyzer is used for tracing activity on the emulation bus in real time. HP 64302A Emulation Bus Analyzer accommodates all 8- and 16-bit processors that are emulated. Trace lists generated by the analyzer may be displayed in the mnemonics of the target processor. Inverse assembler software is included in the emulation software. HP 64856A User Definable Inverse Assembly software package may be used to generate mnemonics for the User Definable Emulator (UDE) and User Definable Preprocessor.

Cross assemblers/linkers are available for all processors supported by an HP emulator. For large software projects, where programmer productivity is critical, there are HP 64000 system C and Pascal cross compilers for many of the general-purpose processors that are supported by HP emulators.

The analytical functions of the emulator can be expanded with Model 64310A Software Performance Analyzer. Input data for the HP 64310A analyzer is collected from activity on the emulation bus. The performance analyzer provides the macro, overview measurements needed for optimizing and modifying code for more efficient software performance.

When complex, detailed logic state analysis is required, the powerful HP 64620S Logic State/Software Analyzer can be integrated directly into the emulator subsystem via HP 64304A Emulation Bus Preprocessor. The added power of software analysis provides traces converted to high-level language source code as well as assembly language or numeric code lists.

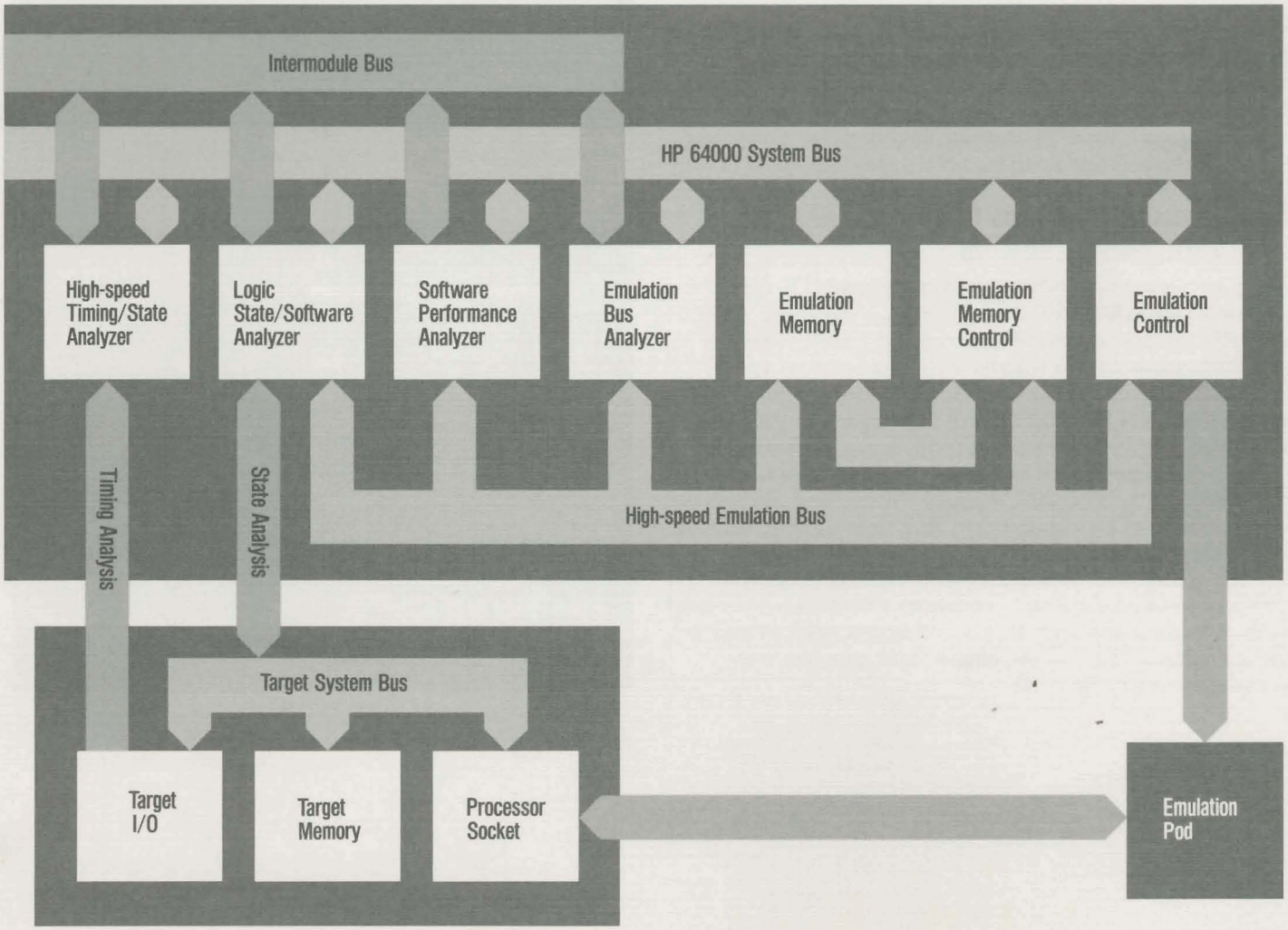
For troubleshooting and debugging software written in C or Pascal languages, the HP 64100A and 64110A development stations support two series of high-level software analyzers, HP 64330 and 64340, for specific microprocessors. These analyzers make measurements on program procedures, functions, statements, local variables, and global variables.

For hardware debugging, the powerful HP 64610S High-speed Timing/State Analyzer checks timing relationships, locates glitches, and identifies marginal signals. For high-speed logic designs, the analyzer functions as a 125 MHz state analyzer.

A new dimension of analysis power can be added with the Intermodule Bus (IMB) which links analyzers and emulators. The IMB communicates with the emulator through the HP 64302A Emulation Bus Analyzer. Other analysis subsystems that can be added to the IMB are the HP 64620S Logic State/Software Analyzer, HP 64310A Software Performance Analyzer, HP 64610S High-speed Timing/State Analyzer, and HP 64340 Real-time High-level Software Analyzer. Cross triggering between analyzers enables the designer to make coordinated measurements that help solve complex hardware/software integration problems.

System Architecture

All emulators of the HP 64000 system use a multiple-bus architecture, thus allowing interactive emulation and analysis. The development station host processor communicates with all installed subsystems using the HP 64000 system bus. A separate high-speed emulation bus carries all transactions required for emulation. Independent operation frees the emulation system from the host system overhead. The intermodule bus controls sophisticated, interactive cross measurements for emulation, state, timing, and performance analysis. Major advantages of the multiple-bus architecture are real-time, transparent emulation and analysis that free the target system for unrestricted execution.



Emulator Application

Control Your System Development

With an HP 64000 emulator, you have direct control over your evolving microprocessor-based system. First, load memory with blocks assigned as ROM, RAM, or guarded. You can display and modify any register, memory location, or I/O port. You also have complete control of the program flow with single-step, run-from, and run-until directives. Run controls initiate or terminate program execution at a specified address or symbol. These functions allow you to thoroughly investigate the details of target system operation in the early design stages.

Register displays are comprehensive, yet easily understood. All registers are clearly identified, and status bits are labeled for easy interpretation (figure 1).

Memory displays show you any location or range of locations in either hexadecimal, binary, real, or mnemonic format (figure 2). Display selections include words and ASCII equivalents, or memory locations translated into the mnemonics of the microprocessor (figure 3). Memory modifications are allowed in the format appropriate to the emulator being used.

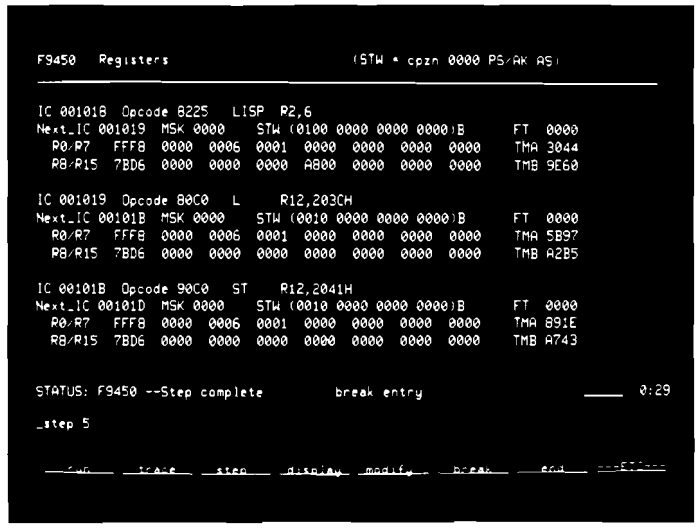


Figure 1. *Register displays show all registers with status bits labeled for easy interpretation.*

Nonintrusive Analysis for Real-time Measurements

Many microprocessor-based products are applied to controlling or monitoring critical real-time processes. With an HP 64000 emulator your development tools support a wide variety of real-time measurements without intruding on target system operation. The analysis system allows you to monitor all memory bus and I/O port activity nonintrusively and in real time, while the target system is operating at full speed.

Information monitored by the emulator is passed to the HP 64302A Emulation Bus Analyzer, where trigger and storage directives are applied. Triggers can be defined for any event and set for the start, center, or end of the trace measurement. Storage qualifiers let you specify which kinds of events are captured and stored in analyzer memory. Commands are entered with easy-to-use softkeys. Trigger and store specifications can include address, data, status, ranges, don't-care bits, and occurrence counts (figure 4).

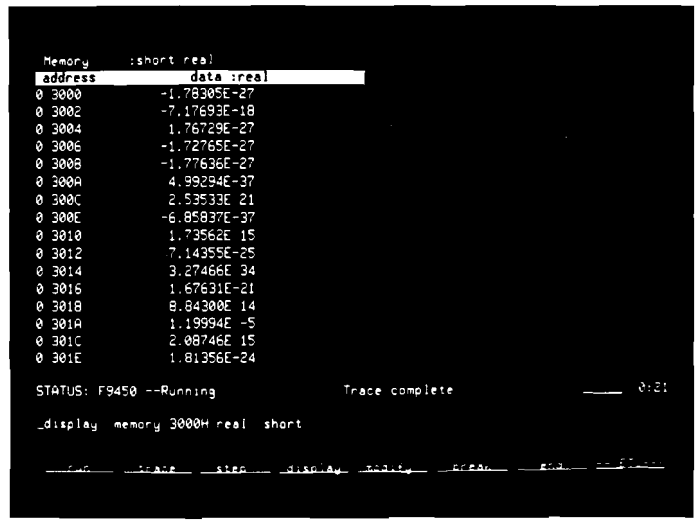


Figure 2. *Memory can be displayed in floating-point, real number format, as well as hexadecimal or mnemonic format.*

Start Analysis and Debugging Without Target System Hardware

Analysis and debugging can begin immediately, with or without functional target system hardware. An internal clock combined with emulation memory provides real-time execution and evaluation as soon as the first code is written. In-circuit emulation may be performed at higher speeds which are determined by the target system clock and the speed capability of the CPU installed in the emulator.

Flexible mapping allows you to assign memory to the emulation or target system in blocks. Blocks are assigned as emulation ROM/RAM, target system ROM/RAM, or guarded access across the full address range of the microprocessor. These block sizes are convenient for efficiently transferring resources from the emulator to the newly developed target system.

Simulated I/O supports concurrent software development and debugging. Program development can continue uninterrupted using the HP 64000 facilities for I/O activities. Your printer, display, keyboard, disc, and RS-232 channel can all be simulated.

Design and Implement Effective Products

HP 64000 emulators offer development support for all phases of microprocessor-based designs. HP 64000 tools have the flexibility, power, and convenience required for designing and implementing effective microprocessor-based products, quickly and efficiently. These interactive tools can be configured into measurement systems for multiple emulation, multiple analysis, and, in the HP 64000-UX environment, multiple users. The powerful measurement subsystems and the friendliness of the microprocessor development environment foster good design practices and complete debugging, from the first design statements to the finished product.

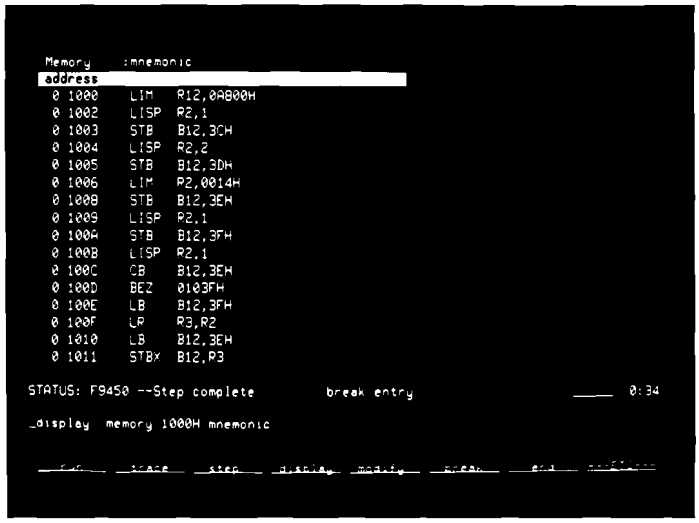


Figure 3. *Memory locations can be displayed in the mnemonics of the target microprocessor.*

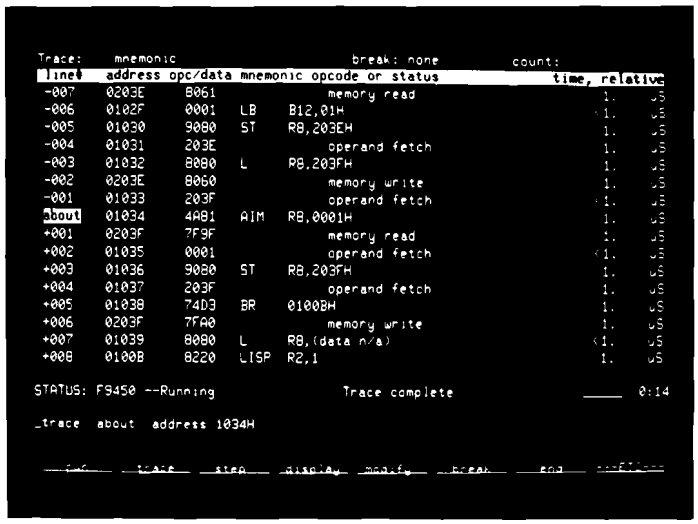
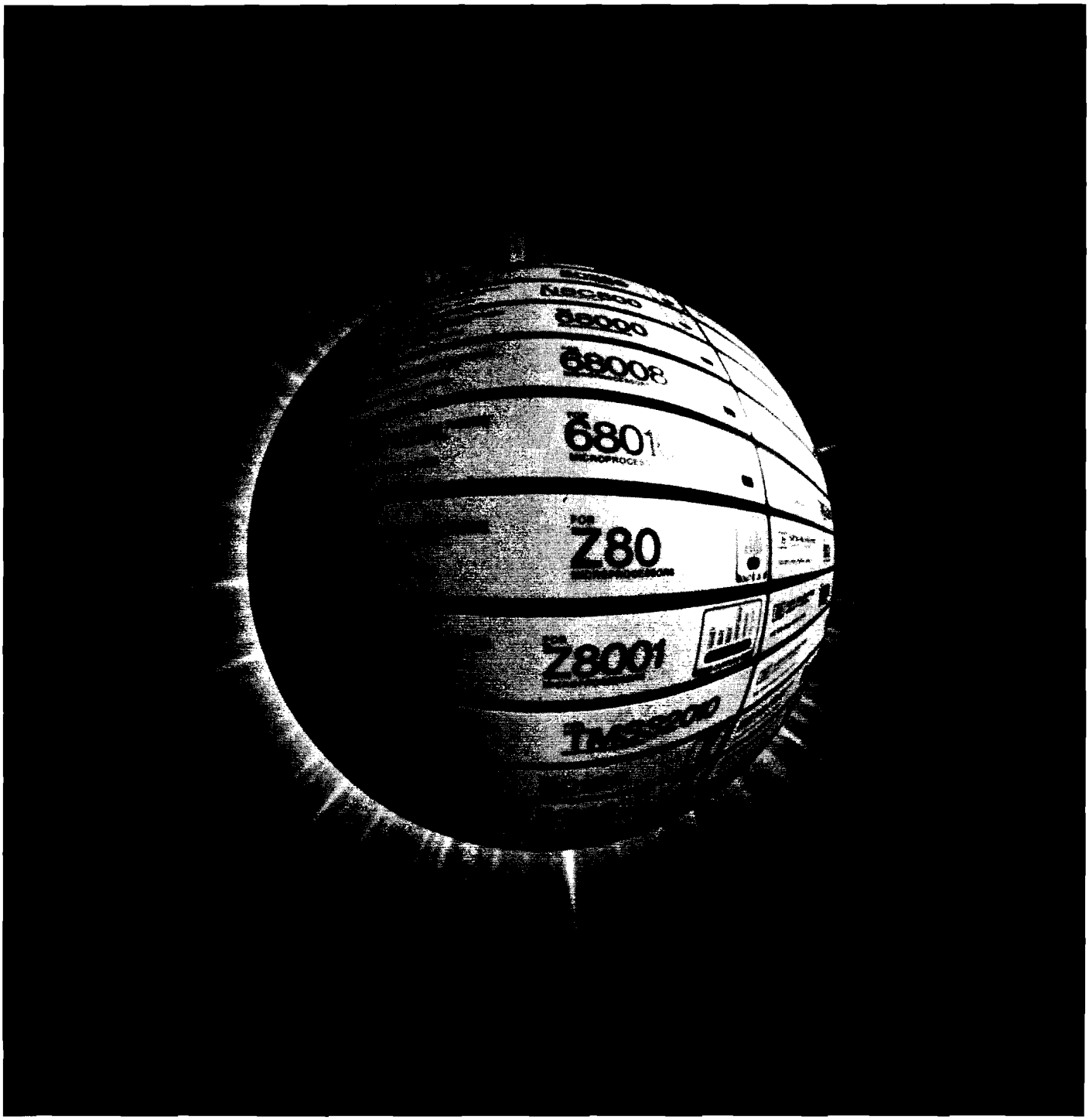


Figure 4. *Nonintrusive, real-time analysis permits evaluation of all target processor memory and I/O activity, including address, data, status, ranges, don't-care bits, and occurrence counts. HP 64302A Emulation Bus Analyzer works with all emulators.*

Emulation Subsystems

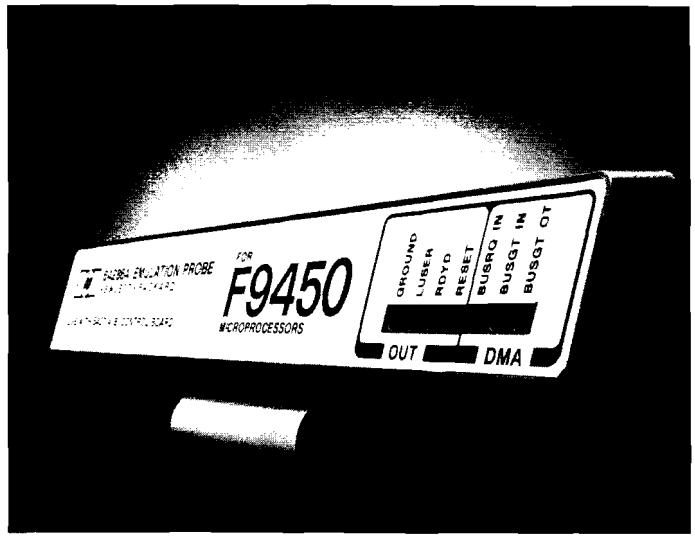
Features, Specifications, Ordering Information



Fairchild F9450
Model 64286SB

Model 64286SB Emulation Subsystem consists of a control board, pod, and operating software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 64-pin probe with 0.050 inch centers. A typical F9450 emulation system includes HP 64286SB Emulation Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64857 Cross Assembler/Linker.



Features

- Real-time execution to at least 15 MHz
- Nonintrusive, real-time tracing of all F9450 cycles including: Memory, DMA, and I/O
- Disassembly of MIL-STD-1750A and IEEE mnemonics
- Up to 448k words of emulation memory
- Expandable to 21 address bits using AS and D/I lines
- Flexible memory mapping for emulator and target systems in 128-word blocks for memory defined by the first 19 address bits; 2k-word blocks for memory defined with address bits 20 and 21
- DMA access allowed into and out of emulation memory
- Supports single- and double-word floating point definitions
- 16 software breakpoints
- Compatible with F9450 peripherals
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another F9450 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speeds: 15 MHz with no wait states required for target system memory; three data wait states for access to emulation memory.

Data inputs: one F TTL load and 40 pF capacitance.

Power: 15 mA drawn from the target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64286SB	**F9450 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 012	Expand to 128 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64857S	**Cross Assembler/Linker for MIL-STD-1750A**

Components

64286AB	**F9450 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64271B	**General Purpose Emulation Control Board**

Hitachi HD6301V/X/Y

Model 64206S
Model 64207S
Model 64208S

HP Model	Hitachi Processor
64206S	6301V/6303R/63P01M
64207S	6301X/6303X/63701X
64208S	6301Y/6303Y/63701Y

Each model consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in either a 40-pin, low-profile probe for the Model 64206S or a 64-pin, low-profile probe for Models 64207S and 64208S. A typical 6301V/X/Y emulation system includes the appropriate emulation subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by HP 64841 Cross Assembler/Linker.

Features

- Real-time execution up to 2 MHz system clock, independent of emulator/target system memory assignment (no wait states)
- Up to 64 kbytes emulation memory available
- Support of all operation modes, 0, 1, 2, 4, 5, 6, and 7 with HP 64206S; and 1, 2, and 3 with HP 64207S and 64208S
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 6301 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: 2 MHz (E CLOCK) with no wait states required for emulator or target system memory; 8 MHz max crystal frequency.

Data inputs: Model 64206S, all inputs meet Hitachi specifications plus 10 kohm pull-up resistor and approx 30 pF capacitance. Models 64207S and 64208S, ports 1 and 3: one HCT load plus 10 kohm pull-up resistor and approx 30 pF capacitance; ports 2, 4, 5, 6, and 7: one LS TTL load plus 10 kohm pull-up resistor and approx 30 pF capacitance; IRQ1, IRQ2, MR, HALT, NMI, RES, STBY, IS (HP 64208S): one HCT load plus 10 kohm pull-up resistor and 30 pF capacitance; HALT tPCS = PWEL + tEf + 20 ns.

Power: HP 64206S, 30 mA drawn from target system; HP 64207S and 64208S, 45 mA drawn from target system; all other power supplied by development station or card cage.

Ordering Information

Model	Description
64206S	**6301V/6303R Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64207S	**6301X/6303X Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64208S	**6301Y/6303Y Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64841S	**Cross Assembler/Linker for 6800 family**

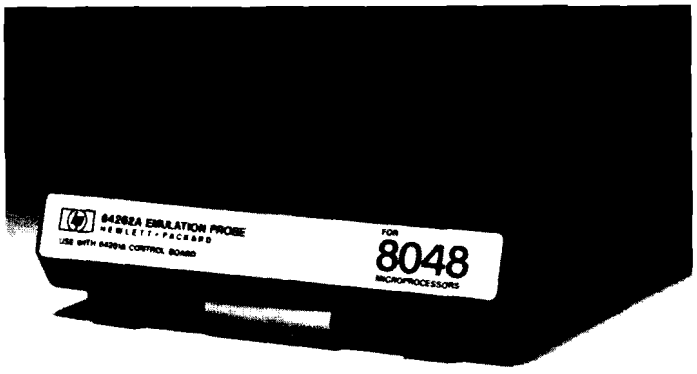
Components

64205B	**6301V/X/Y Emulation Control Board**
64206A	**6301V/6303R Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64207A	**6301X/6303X Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64208A	**6301Y/6303Y Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Intel 8048/8049 Family
Model 64262S

Model 64262S Emulation Subsystem consists of two control boards, pod, and software. Connection to target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 8048/8049 emulation system includes HP 64262S Emulation Subsystem and HP 64302A Emulation Bus Analyzer. High-speed emulation memory is resident on the emulation control boards; no additional emulation memory is needed.

Software development support is provided by Model 64846 Cross Assembler/Linker.



Features

- Real-time execution up to 11 MHz from emulation or target memory
- Flexible memory mapping for emulator and target systems in 1-kbyte blocks of the 4-kbyte program address space; 256 bytes of internal data memory address space
- Symbolic debugging
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 8048/8049 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Specifications

Processor compatibility: compatible with processors that meet the specifications of Intel 8035, 8039, 8040, 8048, 8049, and 8050 microprocessors.

Electrical

Maximum clock speed: up to 11 MHz when operating from emulation or target system memory.

Data input: low-power Schottky TTL loads with capacitance of approx 20 pF.

Clock input: meets Intel 8040 specifications plus capacitance of approx 20 pF; ports P1 and P2 have an additional 10 kohm pull-up resistor.

Power: 50 mA drawn from the target system; all other power supplied by the development station.

Ordering Information

Model	Description
64262S	8048/8049 Emulation Subsystem
64302A	48-channel Emulation Bus Analyzer
64846S	Cross Assembler/Linker for 8048 family

Components

64261A	8048/8049 Emulation Control Board
64262A	8048/8049 Emulation Pod (includes software)

Intel 8051/8751/8031
Model 64264S

Model 64264S Emulation Subsystem consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin, low-profile probe. A typical 8051/8751/8031 emulation system includes HP 64264S Emulation Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64855 Cross Assembler/Linker.

Features

- Real-time execution up to 12 MHz independent of emulator/target system memory assignment
- Nonintrusive, real-time traces of 8051 activity for basic analysis and evaluation, including accesses to
  - Program memory
  - Internal and external data memory
  - Accumulator and special-function registers
  - I/O ports 0, 1, 2, and 3
- Disassembly of 8051 instruction set
- Program and external data memory mapped in 256-byte blocks to emulation or target system memory
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 8051 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: 12 MHz.

Inputs: all inputs meet Intel specifications plus approx 40 pF capacitance; Port 0, low-level input, 0.45 mA; Port 1, Port 2, and Reset, low-level input, 0.1 mA; and EA, low- level input, 0.5 mA.

Power: 20 mA drawn from the target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64264S	**8051/8751/8031 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64855S	**Cross Assembler/Linker for 8051**

Components

64263A	**8051 Emulation Control Board**
64264A	**8051 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Intel 8080/8085
Model 64202S
Model 64203S

Models 64202S and 64203S Emulation Subsystems each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 8080 or 8085 emulation system includes HP 64202S or 64203S Emulation Subsystem, HP 64152A Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64840 Cross Assembler/Linker, Model 64825 Pascal Cross Compiler, and Model 64826 C Cross Compiler.

Features

- Real-time execution for 8080 up to 4 MHz from target memory only, and up to 3.5 MHz when operating from emulation and target system memory (no wait states)
- Real-time execution for 8085 up to 5 MHz from target memory, and up to 4.75 MHz when operating from emulation and target system memory (no wait states)
- Flexible memory mapping for emulator and target systems in 1-kbyte blocks over 64-kbyte address space
- Symbolic debugging capability with assembly language and Pascal and C programs
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 8080 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speeds: HP 64202S, up to 4 MHz with no wait states when operating from target memory only; up to 3.5 MHz with no wait states when operating from both emulation and target system memories (one wait state required when accessing emulation memory between 3.5 MHz and 4 MHz). HP 64203S, up to 5 MHz with no wait states when operating from target memory only; up to 4.75 MHz with no wait states when operating from both emulation and target system memories (one wait state required when accessing emulation memory between 4.75 MHz and 5 MHz).

Data input: low-power Schottky TTL loads with capacitance of approx 20 pF.

Clock input: meets Intel 8080/8085 specifications plus capacitance of approx 20 pF.

Power: 14 mA drawn from the target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64202S	**8080 Emulation Subsystem**
64203S	**8085 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64152S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64840S	**Cross Assembler/Linker for 8080/8085**
64825S	**Pascal Language System for 8080/8085**
64826S	**C Language System for 8080/8085**

Components

64201A	**8080/8085 Emulation Control Board**
64202A	**8080 Emulation Pod** (includes software)
64203A	**8085 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Intel 8086/8088, CMOS 80C86/80C88

Model 64220S
Model 64220S Opt 001
Model 64221S
Model 64221S Opt 001

HP Model	INTEL Processor
64220S	8086/8087
64220S Opt 001	80C86
64221S	8088/8087
64221S Opt 001	80C88

These Emulation Subsystems each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 8086 or 8088 emulation system includes HP 64220S or 64221S Emulation Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64853 Cross Assembler/Linker, Model 64814 Pascal Cross Compiler, and Model 64818 C Cross Compiler.

In addition to tracing the activity of the 8086/8088 target system, the emulator/analyzer combination supports coprocessor functions. Models 64220S and 64221S emulate the 8087 with an on-board 8087 coprocessor that can be selectively enabled or disabled. Instructions and memory cycles of the 8087 numeric coprocessor and a peripheral 8089 I/O coprocessor can be traced and displayed in the processor mnemonics.

Register displays are comprehensive, yet easily understood. All registers are clearly identified, with status bits labeled for easy interpretation (figure 5).

Memory displays can be selected in bytes, words, and ASCII equivalents, or memory locations translated into 8086, 8088 mnemonics.

Features

- Real-time execution up to 8 MHz (no wait states), independent of emulation/target system memory assignment for NMOS 8086/8087 and 8088/8087 emulators
- Real-time execution from dc to 5 MHz (no wait states), independent of emulation/target system memory assignment for CMOS 80C86 and 80C88 emulators
- Real-time instruction dequeueing in MIN and MAX modes (figure 6)
- No MNI restrictions
- Coprocessor compatibility (8087/8089), and expanded coprocessor support with an on-board 8087 in the NMOS 8086 and 8088 emulators
- Up to one Mbyte of emulation memory
- Display of combined 8086/8087 and 8088/8087 registers
- Nonintrusive, real-time tracing of all 8086 and 8088 cycles
- Display of all bus cycles or a dequeued trace of bus activity
- Support of processor bus request/grant activities:
  - DMA transfers
  - Multiple, slave, or coprocessor

- Fully interactive multiprocessor support
- 16 software breakpoints
- Flexible memory mapping for emulation or target system in 256-byte blocks
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 8086/8088 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer
  - HP 64332B/64333B High-level Software Analyzers
  - HP 64341AA/64341CA Real-time High-level Software Analyzers

Electrical Specifications

Maximum clock speeds: 8 MHz with no wait states required for emulation or target system memory for 8086/8087 and 8088/8087 NMOS emulators; dc to 5 MHz for 80C86 and 80C88 CMOS emulators.

Data inputs: one ALS TTL load plus approx 20 pF capacitance

Power: 15 mA at +5V drawn from target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64220S	**8086/8087 Emulation Subsystem**
Opt 001	80C86 Emulation Subsystem
Opt 004	Emulation Software hosted on HP 9000 Series 300
64221S	**8088/8087 Emulation Subsystem**
Opt 001	80C88 Emulation Subsystem
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
Opt 013	Expand to 256 kbytes
Opt 014	Expand to 512 kbytes
Opt 015	Expand to 1024 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64853S	**Cross Assembler/Linker for 8086/88/186/188**
64814S	**Pascal Language System for 8086/88/186/188/286**
64818S	**C Language System for 8086/88/186/188/286**

Components

64223B	**General Purpose Dequeued Emulation Control Board**
64220B	**8086/8087 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64220C	**80C86 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64221B	**8088/8087 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64221C	**80C88 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Figure 5. *The comprehensive register display shows all registers with status bits labeled for easy interpretation.*

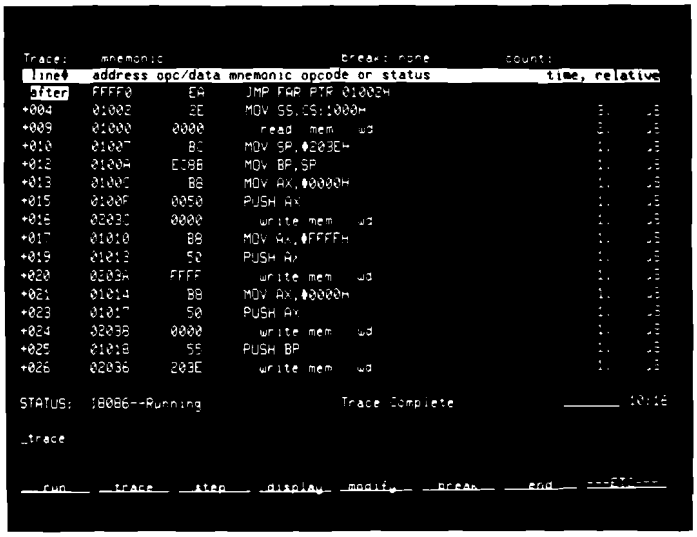
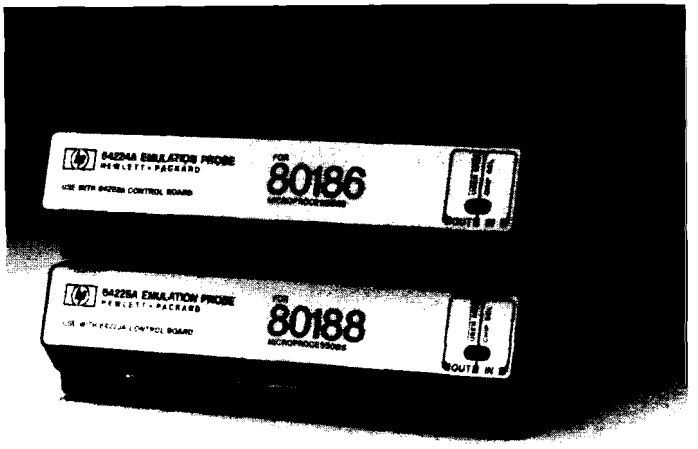


Figure 6. *Nonintrusive, real-time analysis permits evaluation of all 8086/8088 memory activity, including address, data, status, ranges, don't-care bits, and occurrence counts.*

Intel 80186/80188
Model 64224S
Model 64225S

Models 64224S and 64225S Emulation Subsystems each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 68-contact, leadless, chip-carrier probe. A typical 80186/80188 emulation system includes Model 64224S or 64225S Emulation Subsystem, Model 64156S Emulation Memory System, and Model 64302A Emulation Bus Analyzer.

Software development support is provided by HP 64853 Cross Assembler/Linker, HP 64814 Pascal Cross Compiler, and HP 64818 C Cross Compiler.



Features

- Real-time execution up to 8 MHz (no wait states), independent of emulator/target system memory assignment
- Real-time instruction dequeueing in either normal or queue status operating mode
- Flexible memory mapping for emulator and target systems in 256-byte blocks
- Disassembly of 80186/8087 and 80188/8087 or 8089 instruction sets
- Nonintrusive, real-time tracing of all 80186/80188 cycles, including: Memory, DMA, I/O, Coprocessor
- Comprehensive display and modify functions for Internal registers, Peripheral Control registers, memory, and I/O ports
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 80186/80188 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Note: To properly connect and operate either emulator, the target 80186/80188 system must have an AMP® 55162-X socket and AMP 55478-2 lid, and IDT 3M® Textool 68-pin JEDEC socket (part no. 268-5400-52), or equivalent socket assembly.

Maximum clock speeds: 8 MHz (CLKOUT) with no wait states required for emulation or target system memory; 16 MHz max crystal frequency.

Data inputs: one LS TTL load plus approx 40 pF capacitance.

Power: 25 mA drawn from target system; all other power supplied by development station or card cage.

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®Registered, Minnesota Mining and Manufacturing Company

Ordering Information

Model	Description
64224S	**80186 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64225S	**80188 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
Opt 013	Expand to 256 kbytes
Opt 014	Expand to 512 kbytes
Opt 015	Expand to 1024 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64853S	**Cross Assembler/Linker for 8086/88/186/188**
64814S	**Pascal Language System for 8086/88/186/188/286**
64818S	**C Language System for 8086/88/186/188/286**

Components

64223B	**General Purpose Dequeued Emulation Control Board**
64224A	**80186 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64225A	**80188 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Intel 80286
Model 64228S

Model 64228S Emulation Subsystem provides full feature, real-time, transparent emulation for Intel 80286 microprocessor-based systems in both real address mode (compatibility) and protected virtual address mode.

Software development support is provided by Model 64859 Cross Assembler/Linker, Model 64814 Pascal Cross Compiler, and Model 64818 C Cross Compiler. The HP 64859 Assembler/Linker supports protected virtual mode as well as real address mode. In addition, the linker allows linking of mixed-mode code.

Features

- Real-time execution up to 8 MHz with no wait states required, independent of emulation/target system memory assignment
- Full support of real address (compatibility) and protected virtual address modes
- Up to one Mbyte of emulation memory (no wait states required)
- Emulation memory mapped in 4-kbyte blocks, mappable to the full 16-Mbyte physical address space of the 80286
- Dual analysis modes: nonintrusive, real-time tracing of bus cycle activity or executed instruction flow
- Disassembly of 80286 and 80287 instruction sets
- Display of 80286 registers, internal cache, TSS, and 80286-specific system tables including IDT, GDT, and LDTs
- Virtual or physical specification of "run" controls, "display/modify" memory, software breakpoints, and trace specification
- Selection of virtual or physical display formats for memory and analysis
- 16 software breakpoints
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another HP 64228S 80286 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Figure 7. *This display is an example of 80286 protected virtual address mode that contains processor registers with segment descriptor cache registers.*

Protected Virtual Address Mode

The HP 64228S emulator has full, protected virtual address mode support as well as real address mode support. This allows emulation without special emulation-specific table entries for the 80286.

The internal state of the 80286 can easily be determined with the comprehensive register display that includes decoded internal cache information (figure 7). In addition, memory and analysis displays can be in physical or virtual address format. This gives the benefit of allowing displays in the same format as the language tools (linker). Further flexibility is provided by allowing any address, virtual or physical, to be specified symbolically.

Virtual addresses may also be specified via selectors to any memory segment in the system. This gives the ability to access the current active task or any other task. Virtual address specification allows access to segments regardless of their current or future location in physical memory. This support of dynamically relocating systems eliminates the need to manually track segment movement through physical memory.

In addition to comprehensive register displays, the emulator also provides a display of the TSS and 80286 system tables in a decoded format (figure 8). This display includes IDT, GDT, and LDTs. This gives you the ability to easily determine the state of operation of your 80286-based system. Any table in the 80286 environment can be displayed whether it is associated with the current task or not.

Dequeueing

Because the 80286 microprocessor prefetches instructions before executing them, not all instructions which appear on the bus of the processor are executed. This makes it difficult to determine program flow from a trace display. The 64228S emulator provides a significant advantage in this area by dequeueing executed instruction flow in real time. This allows easy determination of executed instruction flow and provides accurate and reliable trigger points for analysis. In addition, the dequeued instruction flow allows analysis traces to be qualified on opcodes as well as instructions.

The HP 64228S also provides an alternate mode which allows analysis of bus cycle information. This gives a complete view of all bus activity which would be of primary importance to system designers.

Electrical Specifications

Note: To properly connect and operate the emulator, the target 80286 system must have an AMP® 55162-X socket and AMP 55478-2 lid, an IDT 3M® Textool 68-pin JEDEC socket (part no. 268-5400-52), or equivalent socket assembly.

Maximum clock speed: 16 MHz maximum CLK frequency; 8 MHz processor operation with no wait states required for emulation or target system memory.

Data inputs: one ALS TTL load plus approximately 40 pF capacitance.

Power: 10 mA drawn from target system; all other power supplied by development station.

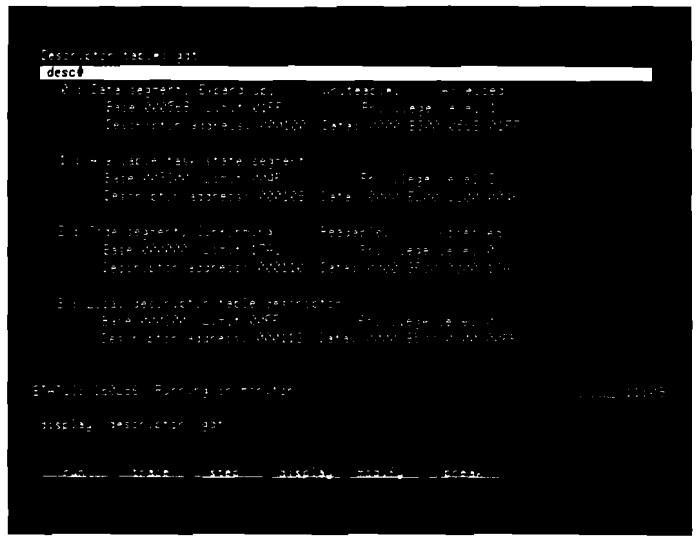


Figure 8. *A decoded display of 80286 system table information makes it easy to identify protected virtual mode attributes.*

Ordering Information

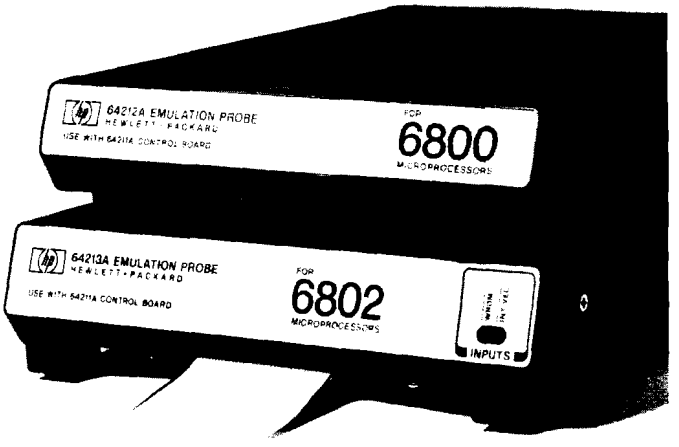
Model	Description
64228S	**80286 Emulation Subsystem**
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
Opt 013	Expand to 256 kbytes
Opt 014	Expand to 512 kbytes
Opt 015	Expand to 1024 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64859S	**Cross Assembler/Linker for 80286**
64814S	**Pascal Language System for 8086/88/186/188/286**
64818S	**C Language System for 8086/88/186/188/286**

Motorola MC6800/6802/6808

Model 64212S
Model 64213S

Models 64212S and 64213S Emulation Subsystems each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 6800 or 6802/6808 emulation system includes HP 64212S or 64213S Emulation Subsystem, HP 64152S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64841 Cross Assembler/Linker, Model 64811 Pascal Cross Compiler, and Model 64821 C Cross Compiler.



Features

- Real-time execution up to 2 MHz from target memory only, and up to 1.9 MHz for the 6800 emulator and up to 1.4 MHz for the 6802/6808 emulator when operating from emulation and target system memory
- Up to 64 kbytes of emulation memory
- Flexible memory mapping for emulator and target system in 1-kbyte blocks over 64-kbyte address space
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 6800 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speeds: HP 64212S, 2 MHz with all memory assigned to target system; 1.9 MHz with any memory assigned to emulation memory, using min phase 2 pulse width (min PW 02H) = 295 ns. HP 64213S, up to 1.4 MHz with no wait states inserted when operating from emulation and target memory; up to 2 MHz with all memory assigned to the target system.

Data input: low-power Schottky TTL loads with capacitance of approx 20 pF.

Clock input: meets Motorola MC6800/6802/6808 specifications plus capacitance of approx 20 pF.

Power: 14 mA drawn from target system; all other power supplied by the development station.

Ordering Information

Model	Description
64212S	**MC6800 Emulation Subsystem**
64213S	**MC6802/6808 Emulation Subsystem**
64152S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64841S	**Cross Assembler/Linker for 6800 family**
64811S	**Pascal Language System for 6800 family**
64821S	**C Language System for 6800 family**

Components

64211A	**MC6800/6802/6808 Emulation Control Board**
64212A	**MC6800 Emulation Pod** (includes software)
64213A	**MC6802/6808 Emulation Pod** (includes software)

Motorola MC6801/6803
Model 64256S

Model 64256S Emulation Subsystem consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 6801/6803 emulation system includes HP 64256S Emulation Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64841 Cross Assembler/Linker, Model 64811 Pascal Cross Compiler, and Model 64821 C Cross Compiler.

Features

- Real-time execution up to 1.25 MHz
- Input mode testing in the target system
- Up to 64 kbytes of emulation memory
- Flexible memory mapping allows 6801/6803 to operate in modes 0, 1, 2, 3, 5, 6, 7
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 6801/6803 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: up to 1.25 MHz with no wait states inserted.

Data input: low-power Schottky TTL loads with capacitance of approx 20 pF.

Clock input: meets Motorola 6801/6803 specifications plus capacitance of approx 20 pF.

Power: 55 mA drawn from target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64256S	**MC6801/6803 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64841S	**Cross Assembler/Linker for 6800 family**
64811S	**Pascal Language System for 6800 family**
64821S	**C Language System for 6800 family**

Components

64255A	**MC6801/6803 Emulation Control Board**
64256A	**MC6801/6803 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Motorola MC6805R/U/P

Model 64192S
Model 64193S

Models 64192S and 64193S Emulation Subsystems each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical MC6805R/6805U or 6805P emulation system includes HP 64192S or 64193S Emulation Subsystem and HP 64302A Emulation Bus Analyzer. All emulation memory is resident on the control board; no additional emulation memory is required.

Software development support is provided by Model 64844 Cross Assembler/Linker.

Features

- Real-time execution up to 4 MHz (no wait states)
- A/D mode fully emulated for 6805R microprocessors
- Memory automatically allocated for the 6805R/U/P microprocessor being emulated
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 6805 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: (no wait states inserted) 4 MHz.

Data Input: low-power Schottky TTL loads with capacitance of approx 20 pF.

Clock input: meets Motorola MC6805R/U/P specifications plus capacitance of approx 20 pF (crystal mask processor option only).

Power: 6 mA drawn from target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64192S	**MC6805R/6805U Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64193S	**MC6805P Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64302A	**48-channel Emulation Bus Analyzer**
64844S	**Cross Assembler/Linker for 6805 and 6809**

Components

64197A	**MC6805 Emulation Control Board**
64192A	**MC6805R/6805U Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64193A	**MC6805P Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Motorola 146805E2
Model 64195S

Model 64195S Emulation Subsystem consists of a control board with self-contained memory, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 146805E2 emulation system includes HP 64195S Emulation Subsystem and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64844 Cross Assembler/Linker.

Memory displays can show any location or range of locations; selectable display formats include words and ASCII equivalents, or memory locations translated into 146805E2 mnemonics. Ports A and B can also be displayed and modified as defined by the 146805E2 specifications. Memory and port addresses can also be referenced symbolically as they are defined in the software symbol table.

Features

- Real-time execution up to 5 MHz independent of emulator/target system memory assignment
- Nonintrusive, real-time traces of all 146805E2 memory activity
- Symbolic addressing for all operations
- Flexible memory for emulator and target systems in 64-byte blocks
- Full complement of emulation memory (8 kbytes) provided on the control board
- Wait/Stop operations displayed as target system status
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 146805E2 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: 5 MHz.

Data inputs: all inputs meet Motorola specifications plus approx 40 pF capacitance; IRQ and Reset, low input, one-half TTL load; Timer, low input, one TTL load.

Power: 60 mA drawn from the target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64195S	**146805E2 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64302A	**48-channel Emulation Bus Analyzer**
64844S	**Cross Assembler/Linker for 6805 and 6809**

Components

64195A	**146805E2 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64197A	**6805 Emulation Control Board**

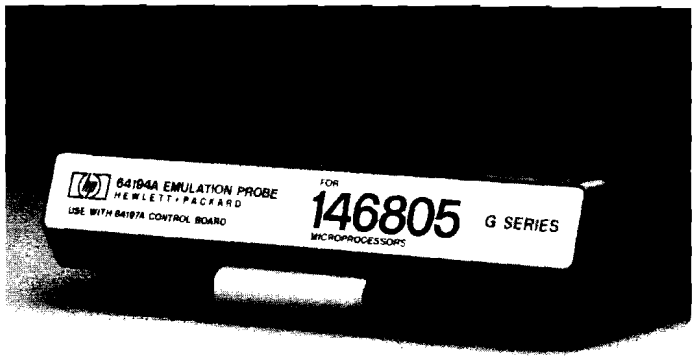
Motorola 146805G2
Model 64194S

Model 64194S Emulation Subsystem consists of a control board with self-contained memory, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 146805G2 emulation system includes HP 64194S Emulation Subsystem and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64844 Cross Assembler/Linker.

Memory mapping is performed automatically with the emulator. The 112 bytes of on-chip RAM and 2106 bytes of on-chip ROM are fully mapped by emulation memory. Additional emulation memory, up to 6 kbytes, is available for prototype software development before the software is optimized and tailored to fit the 2-kbyte, on-chip ROM. The additional emulation memory may also be used as read-only ROM space or read/write RAM equivalent.

Modifications are made by bytes or words. Ports A, B, C, and D can be displayed and modified as defined by the 146805G2 specifications. Memory and port addresses can be referenced symbolically, as they are defined in the software symbol table.



Features

- Real-time execution up to 4 MHz
- Up to 8 kbytes total emulation memory, allowing extra memory to develop prototype software
- Nonintrusive, real-time traces of all 146805G2 memory activity, including internal 112-byte RAM, internal 2-kbyte ROM, and 6-kbyte extra emulation memory
- Symbolic address for all operations
- Wait/stop operations displayed as target system status
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 146805G2 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: up to 4 MHz with no wait states inserted.

Inputs: all port inputs and outputs meet Motorola specifications plus approx 40 pF capacitance; IRQ and Reset, low input, one-half TTL load; Timer, low input, one TTL load.

Power: 60 mA drawn from the target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64194S	**146805G2 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64302A	**48-channel Emulation Bus Analyzer**
64844S	**Cross Assembler/Linker for 6805 and 6809**

Components

64194A	**146805G2 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64197A	**6805 Emulation Control Board**

Motorola MC6809/68A09/68B09 MC6809E/68A09E/68B09E

Model 64215S
Model 64216S

Models 64215S and 64216S Emulation Subsystems each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical 6809 or 6809E emulation system includes HP 64215S or 64216S Emulation Subsystem, HP 64152S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64844 Cross Assembler/Linker, Model 64813 Pascal Cross Compiler, and Model 64822 C Cross Compiler.

Features

- Real-time execution up to 2 MHz independent of emulator/target memory assignment (no wait states)
- Support of processor bus request/grant activities
  - DMA transfers
  - Multiple or slave processors
- Flexible memory mapping in 1-kbyte blocks; 64-kbyte address space
- Up to 64 kbytes of emulation memory available
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 6809 or 6809E emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: up to 2 MHz with no wait states inserted.

Data input: low-power Schottky TTL loads with capacitance of approx 20 pF.

Clock input: meets Motorola MC6809/6809E specifications plus capacitance of approx 20 pF.

Power: 15 mA drawn from target system (HP 64215S only); all other power supplied by the development station or card cage. HP 64216S draws 0.0 mA.

Ordering Information

Model	Description
64215S	**MC6809 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64216S	**MC6809E Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64152S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64844S	**Cross Assembler/Linker for 6805 and 6809**
64813S	**Pascal Language System for 6809**
64822S	**C Language System for 6809**

Components

64214A	**MC6809/6809E Emulation Control Board**
64215A	**MC6809 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64216A	**MC6809E Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Motorola MC68000/68008

Model 64243AA
Model 64243AB
Model 64244AA

HP Model	Cable Connection	Motorola Processor
64243AA	64-pin DIP probe	MC68000
64243AB	68-pin PGA probe	MC68000
64244AA	48-pin DIP probe	MC68008

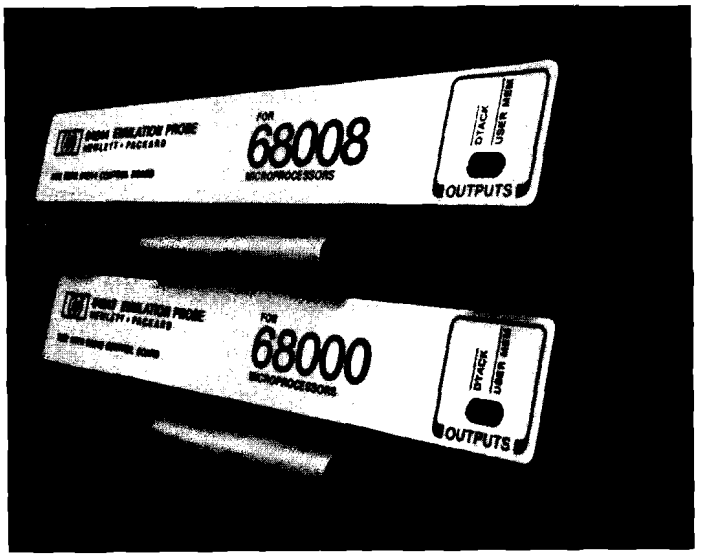
Models 64243 and 64244 Emulation Subsystems each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in either a 64-pin DIP probe for the Model 64243AA, a 68-pin PGA probe for the Model 64243AB, or a 48-pin DIP probe for the Model 64244AA. A typical MC68000 or MC68008 emulation system includes a Model 64243 or 64244 Emulation Subsystem, Model 64156S Emulation Memory System, and Model 64302A Emulation Bus Analyzer.

Software development support is provided by HP 64845 Cross Assembler/Linker, HP 64815 Pascal Cross Compiler, and HP 64819 C Cross Compiler.

Dequeueing

The MC68000/68008 processors have two-word prefetches that allow the processor to fetch instructions before using the information. Normally, a display of all bus activity would include the prefetches along with the executed instructions. This makes it difficult to analyze software execution. Both HP 64243 and 64244 have an execution mode which provides instruction stream dequeueing. This shows the instructions actually executed, for an easy-to-understand display. A bus cycle mode is also available when needed to monitor all bus activity (figure 9).

Figure 9. *A measurement trace of an MC68000 instruction stream shows all activity in bus cycle mode, including memory accesses and instruction prefetches.*



Features

- Real-time execution up to 12.5 MHz for the MC68000 emulator
- Real-time execution up to 10 MHz (no wait states) for the MC68008 emulator
- Up to 896 kbytes of emulation memory
- Real-time instruction execution and bus cycle analysis
- No modification to user vector table for emulator operation
- Flexible memory mapping for the emulator and target system in 4-kbyte blocks with Model 64243, 256-byte blocks with Model 64244
- Both DIP and PGA versions of the MC68000 supported
- Full use of DMA arbitration
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another MC68000 or 68008 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer
  - HP 64331B High-level Software Analyzer for HP 64243AA/AB
  - HP 64337A High-level Software Analyzer for HP 64244AA
  - HP 64341GA Real-time High-level Software Analyzer for HP 64243AA/AB

Electrical Specifications

Maximum clock speeds: 12.5 MHz for the MC68000 emulator. (No wait states when executing from user memory; one wait state from emulation memory above 10 MHz). 10 MHz (no wait states) for the MC68008 emulator.

Data inputs: all inputs meet Motorola specifications plus one ALS TTL load and 40 pF capacitance.

Power: 6 mA drawn from the target system; all other power supplied by the development station or card cage.

Ordering Information

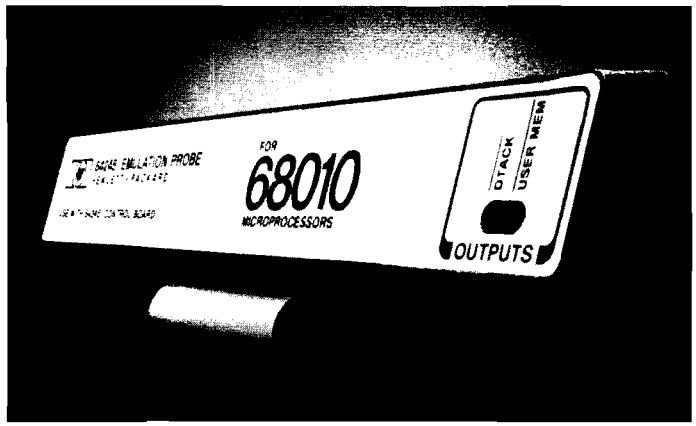
Model	Description
64243AA	**MC68000 Emulation Subsystem** (configured with 64-pin DIP probe)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64243AB	**MC68000 Emulation Subsystem** (configured with 68-pin PGA probe)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64244AA	**MC68008 Emulation Subsystem** (configured with 48-pin DIP probe)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
Opt 013	Expand to 256 kbytes
Opt 014	Expand to 512 kbytes
Opt 015	Expand to 1024 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64845S	**Cross Assembler/Linker for 68000 family**
64815S	**Pascal Language System for 68000 family**
64819S	**C Language System for 68000 family**

Motorola MC68010
Model 64245AA
Model 64245AB

Model 64245 Emulation Subsystem consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in either a 64-pin DIP probe for the HP 64245AA or a 68-pin PGA probe for the HP 64245AB. A typical MC68010 emulation system includes HP 64245 Emulation Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64845 Cross Assembler/Linker, Model 64815 Pascal Cross Compiler, and Model 64819 C Cross Compiler.

The HP 64245 provides additional support for MC68010 systems using function codes to partition memory. Blocks can be assigned to emulation memory as supervisor, user, program, data, CPU space, supervisor program, supervisor data, user program, user data, and functional codes (000, 011, 100, and all).



Dequeueing

The MC68010 processor has a two-word prefetch that allows the processor to fetch instructions before using the information. Normally, a display of all bus activity would include the prefetches along with the executed instructions. This makes it difficult to analyze software execution. The HP 64245 has an execution mode which provides instruction stream dequeueing. This shows the instructions actually executed for an easy-to-understand display. A bus cycle mode is also available when needed to monitor all bus activity.

Features

- Real-time execution up to 12.5 MHz
- Real-time MC68010 instruction execution and bus analysis
- Up to 896 kbytes of emulation memory
- No modification to user vector table for emulator operation
- Function code mapping allows you to assign memory to the emulation or target system in 4-kbyte blocks
- Both DIP and PGA versions of the MC68010 supported
- Full use of DMA arbitration
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another MC68010 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer
  - HP 64334B High-level Software Analyzer
  - HP 64341IA Real-time High-level Software Analyzer

Electrical Specifications

Maximum clock speed: 12.5 MHz. (No wait states when executing from user memory; one wait state from emulation memory above 10 MHz.)

Data inputs: all inputs meet Motorola specifications plus one ALS TTL load and approx 40 pF capacitance.

Power: 6 mA drawn from the target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64245AA	**MC68010 Emulation Subsystem** (configured with 64-pin DIP probe)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64245AB	**MC68010 Emulation Subsystem** (configured with 68-pin PGA probe)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
Opt 013	Expand to 256 kbytes
Opt 014	Expand to 512 kbytes
Opt 015	Expand to 1024 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64845S	**Cross Assembler/Linker for 68000 family**
64815S	**Pascal Language System for 68000 family**
64819S	**C Language System for 68000 family**

National Semiconductor NSC800

Model 64292S

Model 64292S Emulation Subsystem consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable. A typical NSC800 emulation system includes HP 64292S Emulation Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64842 Cross Assembler/Linker, Model 64823 Pascal Cross Compiler, and Model 64824 C Cross Compiler.

Features

- Real-time execution to 4 MHz independent of emulation/target memory assignment (no wait states)
- Flexible memory mapping in 256-byte blocks over 64-kbyte address space
- Up to 64 kbytes of emulation memory available
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another NSC800 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: up to 4 MHz with no wait states inserted; 8 MHz max crystal frequency.

Data input: CMOS B loads at +5 V only, plus capacitance of approx 20 pF.

Clock input: meets National Semiconductor NSC800 specifications plus capacitance of approx 20 pF.

Power: 12.5 mA drawn from the target system; all other power supplied by the development station.

Ordering Information

Model	Description
64292S	**NSC800 Emulation Subsystem**
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64842S	**Cross Assembler/Linker for Z80 and NSC800**
64823S	**Pascal Language System for Z80 and NSC800**
64824S	**C Language System for Z80 and NSC800**

Components

64291A	**NSC800 Emulation Control Board**
64292A	**NSC800 Emulation Pod** (includes software)

NEC 70116/70108
Model 64294S
Model 64295S

Models 64294S and 64295S each consists of a control board, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin, low-profile probe. A typical 70116/70108 emulation system includes an HP 64294S or 64295S Emulation Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64853 Cross Assembler/Linker, Model 64814 Pascal Cross Compiler, and Model 64818 C Cross Compiler.

Features

- Real-time execution up to 8 MHz (no wait states), independent of emulator/target system memory assignment
- Real-time instruction dequeueing in either small or large operating mode
- Disassembly of 70116/70108 instructions with FPP or 8080 mode instructions
- Nonintrusive, real-time tracing of all 70116/70108 cycles, including Memory, DMA, I/O, Coprocessor
- Flexible memory mapping for emulator and target systems in 256-byte blocks
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another 70116/70108 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: 8 MHz (CLK) with no wait state required for emulator or target system memory; 16 MHz max crystal frequency.

Data inputs: All inputs and outputs: ALS TTL load plus approx 40 pF capacitance; LRQ/LAK 1: low level input 1.5 mA; CLK; NEC specifications plus two LS TTL load plus approx 40 pF capacitance.

Power: 25 mA drawn from target system; all other power supplied by development station or card cage.

Ordering Information

Model	Description
64294S	**70116 (V30) Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64295S	**70108 (V20) Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
Opt 013	Expand to 256 kbytes
Opt 014	Expand to 512 kbytes
Opt 015	Expand to 1024 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64853S	**Cross Assembler/Linker for 8086/88/186/188**
64814S	**Pascal Language System for 8086/88/186/188/286**
64818S	**C Language System for 8086/88/186/188/286**

Components

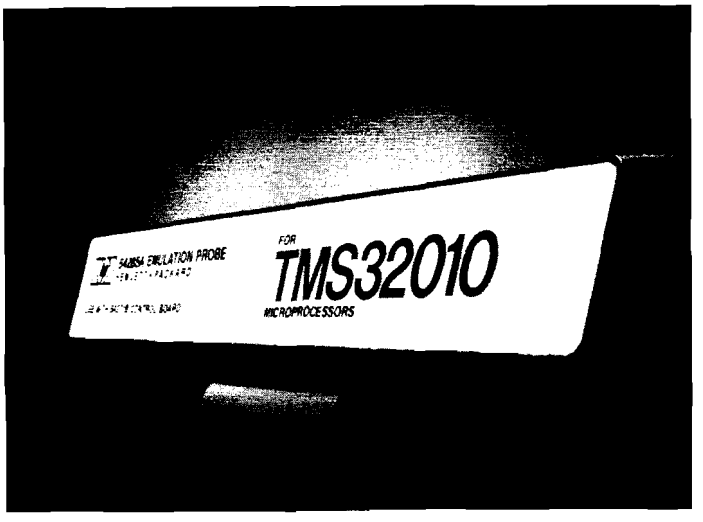
64223B	**General Purpose Dequeued Emulation Control Board**
64294A	**70116 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64295A	**70108 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300

Texas Instruments TMS32010/320M10

Model 64285S

Model 64285S Emulation Subsystem consists of a control board with self-contained memory, pod, and software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 40-pin probe. A typical TMS32010 emulation system includes HP 64285S Emulation Subsystem and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64858 Cross Assembler/Linker.



Features

- Real-time execution up to 20 MHz (no wait states), independent of emulator/target system memory assignment
- Nonintrusive, real-time traces of all TMS32010 memory activity
- Disassembly of TMS32010 instruction set
- Flexible memory mapping for emulator and target systems in 64-word blocks
- 4k words of self-contained memory
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another TMS32010 emulator or another HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: 20 MHz.

Data inputs: all inputs meet Texas Instruments specifications plus 40 pF capacitance.

Power: 25 mA drawn from the target system; all other power is supplied by the development station or card cage.

Ordering Information

Model	Description
64285S	TMS32010 Emulation Subsystem
64302A	48-channel Emulation Bus Analyzer
64858S	Cross Assembler/Linker for TMS32010

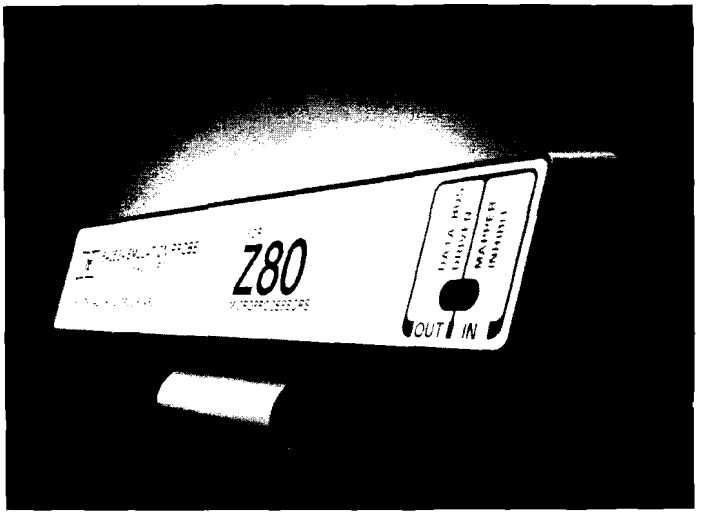
Components

64285A	**TMS32010 Emulation Pod** (includes software)
64271B	**General Purpose Emulation Control Board**

Zilog Z80
Model 64253S

Model 64253S Emulation Subsystem consists of a control board, pod with self-contained memory, and operating software. Connection to the target system is made with a 355 mm (14 in.) cable that terminates in a 40-pin probe. A typical Z80 emulation system includes HP 64253S Emulation Subsystem and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64842 Cross Assembler/Linker, Model 64823 Pascal Cross Compiler, and Model 64824 C Cross Compiler.



Features

- Real-time execution up to 8 MHz (no wait states), independent of emulator/target system memory assignment
- Nonintrusive, real-time tracing of all Z80 cycles, including Memory, DMA, I/O, and Memory Refresh
- Disassembly of Z80 instruction set
- 64 kbytes of self-contained emulation memory
- Flexible memory mapping for emulator and target systems in 256-byte blocks
- DMA access allowed into and out of emulation memory
- Full support of all Z80 interrupt modes
- 16 software breakpoints
- Bank switching for memory systems with more than 64 kbytes of memory
- Software-selectable hardware control options
- Display and Modify functions for Main and Alternate Registers, Memory and I/O Ports; simultaneous display of Main and Alternate Registers
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another Z80 emulator or another HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Specifications

Processor compatibility: compatible with Zilog Z80, Z80A, Z80B, Z80H, Z80L, and any other microprocessors that comply with the specifications of these processors.

Electrical

Maximum clock speed: 8 MHz with no wait states required for emulation or target system memory.

Data inputs: one ALS TTL load plus approx 40 pF capacitance.

Power: 15 mA at +5V drawn from target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64253S	**Z80 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64302A	**48-channel Emulation Bus Analyzer**
64842S	**Cross Assembler/Linker for Z80**
64823S	**Pascal Language System for Z80**
64824S	**C Language System for Z80**

Components

64253A	**Z80 Emulation Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64271B	**General Purpose Emulation Control Board**

Zilog Z8001/Z8002
Model 64232S
Model 64233S

Models 64232S and 64233S Emulation Subsystems each consists of a control board, pod, and operating software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 48-pin probe for Model 64232S and a 40-pin probe for Model 64233S. A typical Z8001 or Z8002 emulation system includes HP 64232S or 64233S Emulator Subsystem, HP 64156S Emulation Memory System, and HP 64302A Emulation Bus Analyzer.

Software development support is provided by Model 64854 Cross Assembler/Linker, Model 64816 Pascal Cross Compiler, and Model 64820 C Cross Compiler.

Features

- Real-time execution to 6 MHz independent of emulation/target memory assignment (no wait states)
- Support of processor bus request/grant activities
  - DMA transfers
  - Multiple, slave, or coprocessor
- 20-bit width mapped in 256-byte blocks over 16-Mbyte address space
- 24-bit width mapped in 4-kbyte blocks over 16-Mbyte address space
- Up to 128 kbytes of emulation memory available
- Status (PROG, DATA, STACK) memory mapping supported in Z8002 emulator
- User-definable monitor program to tailor debugging resources for specific target system
- 16 software breakpoints
- Full disassembly of processor instructions
- Symbolic debugging
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Another Z8001/8002 emulator or any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer
  - HP 64310A Software Performance Analyzer

Electrical Specifications

Maximum clock speed: (no wait states inserted) 6 MHz.

Data input: low-power Schottky TTL loads with capacitance of approx 20 pF.

Clock input: meets Zilog Z8001/Z8002 specifications plus capacitance of approx 20 pF.

Power: 9 mA drawn from target system; all other power supplied by the development station or card cage.

Ordering Information

Model	Description
64232S	**Z8001 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64233S	**Z8002 Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 012	Expand to 128 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64854S	**Cross Assembler/Linker for Z8001/Z8002**
64816S	**Pascal Language System for Z8001/Z8002**
64820S	**C Language System for Z8001/Z8002**

Components

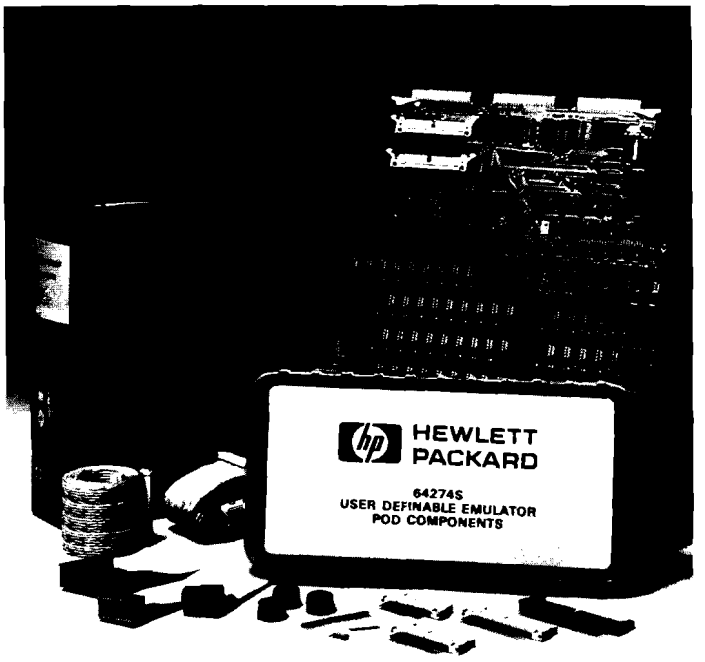
64232A	**Z8001 Emulator Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64233A	**Z8002 Emulator Pod** (includes software)
Opt 004	Emulation Software hosted on HP 9000 Series 300
64271B	**General Purpose Emulation Control Board**

User Definable
Model 64274S

Model 64274S User Definable Emulator (UDE) provides the elements needed to design and build microprocessor emulators for use with the HP 64000 Logic Development System and the HP 64000-UX Microprocessor Development Environment. This opens the full range of HP 64000 system capabilities in developing microprocessor-based systems, even when the target processor is not supported by an HP emulator. Emulation is a powerful technique for accelerating all phases of microprocessor-based product design, development, and maintenance. As a subsystem of the HP 64000 system, Model 64274S also accesses the other sophisticated software and hardware development tools. The User Definable Emulator is suitable for a broad selection of 8-bit and 16-bit microprocessors, including proprietary, low-volume, and older processors.

The User Definable Emulator is used with an HP 64156S Emulation Memory System. Model 64302A Emulation Bus Analyzer is compatible and recommended.

Software development support is provided by Model 64851A User Definable Assembler/Linker and Model 64856A User Definable Inverse Assembler.



Emulator Features and Functions

Each emulator developed with Model 64274S User Definable Emulator can be tailored for the environment in which it will be used. Features and functions are implemented at the designer's discretion to suit the application. A representative set of features of an HP 64274S emulator includes:

- User-definable monitor to
  - Display/modify memory
  - Display/modify internal registers
  - Display/modify I/O ports
- Run-time controls
- Single cycling
- Memory mapping
  - Define 256-byte blocks over 1-Mbyte memory or 4-kbyte blocks over 16-Mbyte memory
  - Assign blocks to emulation or target system memory
- Add up to 1 Mbyte of memory with the emulation memory subsystem
- Memory bus rates to 3.8 MHz without wait states
- An emulation mode that is fully transparent to the target system
- Software breakpoints
- Simulated I/O for emulator access to HP 64000 system resources, including disc files, printer, and development station keyboard, display, and RS-232 ports

Design Examples

Building a specific microprocessor emulator is not a trivial task. Design examples document specific applications of the UDE. The operator's manual includes an implementation of the UDE for the 1802 microprocessor. There are also documents describing UDE designs for 9900 and 9989 processors. HP Sales Representatives can supply any of these design examples, as well as any subsequent UDE designs.

When a UDE is an appropriate answer to a development tool need, the two or three months required to build the new unit are more than offset by the savings in development time, a "cleaner" final product, and an earlier market introduction. The design examples include general principles and specific guidelines and circuits for the subject processor, providing additional information for implementing a UDE design.

Components

- Model 64274A User Definable Emulation Control Board, to be installed in the development station card cage
- Wire-wrapping board, special connectors, and cables
- Software drivers as basis for developing an emulation operating system
- Comprehensive operator's design manual

Microprocessor Compatibility

It is not possible to emulate every microprocessor, nor is it always possible to emulate every feature of microprocessors. Basic criteria that a UDE-compatible microprocessor must meet include:

- Maximum address bus size of 24 bits
- Maximum data bus size of 16 bits
- Access to provide emulator control over the microprocessor through either the highest priority interrupt or jamming in processors that do not prefetch instructions
- Memory cycle rates (NOT clock rates) to a maximum of 1.8 MHz real-time dual access and from 1.8 to 3.9 MHz real-time emulation memory access with no wait states
- Accessible address and data buses
- Specific timing characteristics of the processor must conform to UDE timing constraints as defined in the UDE manual

Time required to implement a UDE varies as a function of the complexity of the target processor emulator features and the designer's level of expertise.

Characteristics

Power Restrictions:

Input Voltage	Current Limit
+12 V	200 mA
+ 5 V	3 A
− 5 V	200 mA

Note: Hewlett-Packard assumes no liability and makes no express or implied warranties of any kind, including, but not limited to, implied warranties of merchantability and fitness for a particular purpose with regard to use of this product for any purpose. Any such use is at the sole risk of the user.

Ordering Information

Model	Description
64274S	**User Definable Emulation Subsystem**
Opt 004	Emulation Software hosted on HP 9000 Series 300
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
64302A	**48-channel Emulation Bus Analyzer**
64851A	**User Definable Assembler/Linker**
64856A	**User Definable Inverse Assembler**

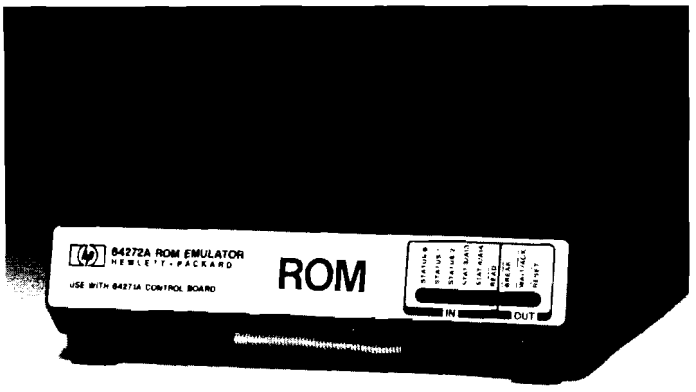
Components

64274A	**User Definable Emulation Control Board**
64274B	**User Definable Emulation Pod Kit** (includes software)
64274C	**User Definable Emulation Software**
Opt 004	Emulation Software hosted on HP 9000 Series 300

ROM Emulator
Model 64272S

Model 64272S ROM Emulator provides real-time, full-speed emulation of a wide range of 24-pin and 28-pin ROMs. It is used with an HP 64156S Emulation Memory System with 32 kbytes or 64 kbytes of memory. Model 64302A Emulation Bus Analyzer is recommended to display emulation activity. The user-definable inverse assembler, Model 64856A, can be used to translate data for memory and trace displays.

The ROM emulator is part of a total, integrated support system for designing and developing ROM-based products. Model 64272S operates interactively with the compilers and assemblers/linkers that are available for many popular microprocessors as well as custom assemblers and inverse assemblers that can be developed for other microprocessors.



Features

- Real-time ROM emulation for most of the popular 24-pin and 28-pin ROMs
- Operation in 8-bit or 16-bit environments
- Up to 64 kbytes of emulation memory
- Memory cycles qualified by chip selects, changes on the address bus, externally-wired READ line
- Emulation/target system synchronization with external reset, break, and wait lines
- Display/modify ROM locations
- Expanded measurement capabilities through interactive operation with other HP 64000 subsystems:
  - Any other HP 64000 emulator
  - HP 64610S High-speed Timing/State Analyzer
  - HP 64620S Logic State/Software Analyzer

ROM Compatibility

Model 64272S ROM Emulator is compatible with most of the ROMs in common use. Additionally, ROMs that are electrically and mechanically identical to the supported ROMs listed are also compatible with HP 64272S.

TI2508	TI2532
Intel 2758	Motorola 68732-0/-01
Intel 2808/2809	Intel 2764
Intel 2716	Motorola 68764
Intel 2816	TI2564
TI TMS2516	Motorola 68766
Hitachi 48016	Intel 3636*
Intel 2732	Signetics 82S190/191*

*Wait states required during emulation

Electrical Characteristics

Minimum access time: 200 ns with Model 64156S Emulation Memory System.

Emulator pod to target system interface: low-power Schottky TTL levels with capacitance of approx 20 pF.

Ordering Information

Model	Description
64272S	ROM Emulation Subsystem
64156S	Emulation Memory System, 32 kbytes
Opt 011	Expand to 64 kbytes
64302A	48-channel Emulation Bus Analyzer
64851A	User Definable Assembler/Linker
64856A	User Definable Inverse Assembler

Components

64271A	General Purpose Emulator Control Board
64272A	ROM Emulation Pod (includes software)

Microprogram Development Subsystem

The HP 64276 Microprogram Development Subsystem and the HP 64320S 25 MHz Logic State/Software Analyzer provide run control and real-time analysis for microprogrammable (bit-slice) systems. As integrated subsystems of the HP 64000 Logic Development System running on the HP 64100A and 64110A stations, the HP 64276 and the HP 64320S add the power of run control and analysis to all phases of the design, development, and maintenance of microprogram-based products.

The Microprogram Development Subsystem consists of three components: a Run Control module, a Writable Control Store (WCS), and a 25 MHz Logic State/Software Analyzer (figure 10). Run Control provides program flow control, clock control, and break event detection. Writable Control Store provides up to 64 kbytes of high-speed RAM for storing the microcode to be executed. A 25 MHz Logic State/Software Analyzer monitors system buses and provides trigger, store, and sequencing functions for locating problems in the microprogram.

The Microprogram Development Subsystem supports software development for a wide variety of microprogrammable processors and sequencers. Integration of the Microprogram Development Subsystem with other powerful HP 64000 analysis and emulation tools allows for interactive, cross-triggered measurements in complex multiprocessor environments.

Features

- The choice of clock control or real-time address jam at break detection offers flexible target system control.
- Address ranging and two-level sequencing provide powerful break event specification.
- Real-time, nonintrusive analysis of microprogrammed system activity reduces software development time.
- Flexible user-definable microassembler provides support for a wide variety of microprogrammable devices.
- Microcode source interleaved with analyzer trace data speeds software debugging.
- Linking of separately assembled microcode modules accelerates software turnaround time.
- MACRO instruction feature of the microassembler improves software engineering productivity.
- Modular architecture permits specific Writable Control Store configurations for customized development tool needs.
- Integration of Run Control and analysis capabilities simplifies operation.
- Interaction with other HP 64000 system emulators and analyzers provides real-time analysis in multiprocessor environments.

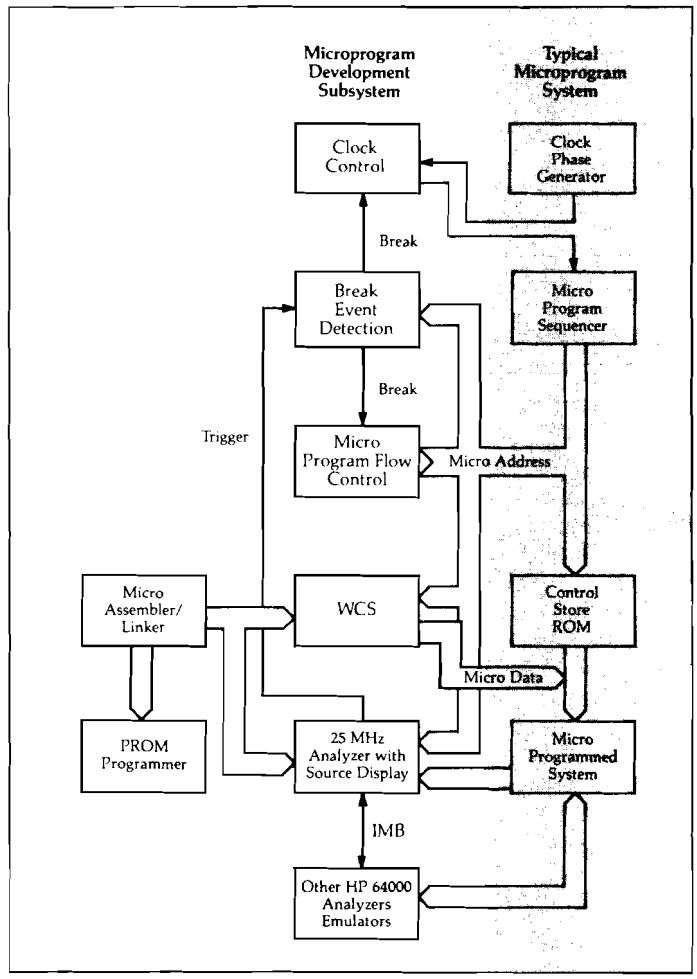


Figure 10. *The Microprogram Development Subsystem consists of a Run Control Module, a Writable Control Store, and a 25 MHz Logic State/Software Analyzer.*

Run Control

Run Control provides system clock control, break event specification, and address jamming. These important features improve debugging of microprogram-based systems.

The Run Control module taps into the clock lines on the target system to obtain the greatest level of clock control. Clock control functions allow you to start and stop the clock, single step, and break on a specific clock edge or pattern (figure 11).

Writable Control Store

The Writable Control Store (WCS), the memory array for the system microcode, consists of a dual port RAM that allows easy microcode downloading from the assembly environment and high-speed access of the microcode by the microprogram target system. Target system development and debugging is more efficient using the WCS instead of the target system control store.

25 MHz Logic State/Software Analyzer

The HP 64320S 25 MHz Logic State/Software Analyzer adds high-speed, real-time, nonintrusive software analysis to the HP 64000 Logic Development System. This flexible analyzer works well in microprogram software analysis, general-purpose software analysis, and system integration.

Measurement results are displayed in source microcode (including MACROs and comment lines) or in user-defined symbols that minimize the need to decode captured data. The analyzer can also reference symbols from the microprogram source files for easy specification and interpretation (figure 12).

Microassembler

The HP 64276 Microprogram Development Subsystem includes a user-definable microassembler and linker (HP 64861) capable of generating microwords up to 1024 bits in width. The microassembler supports a wide range of microprogrammable devices. The linker allows assembly of separate modules, reducing turnaround time for source microcode changes. In addition, a powerful MACRO facility is supported.

A separate data sheet provides more information on the HP 64276 Microprogram Development Subsystem.

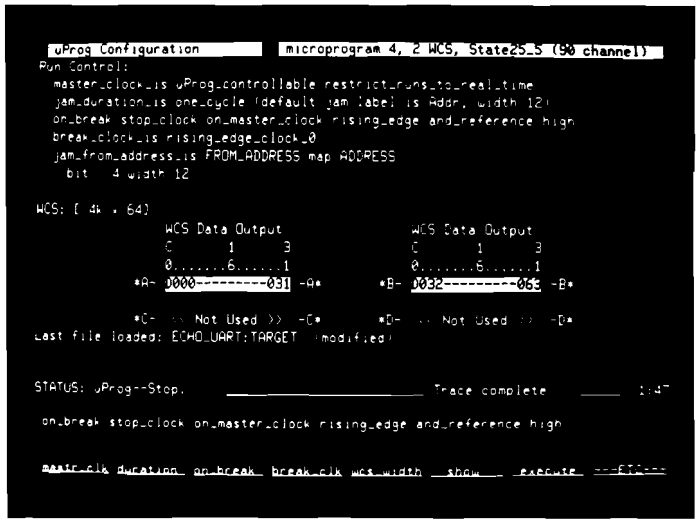


Figure 11. *The Run Control Module allows you to specify complex clock signal characteristics for use in break events.*

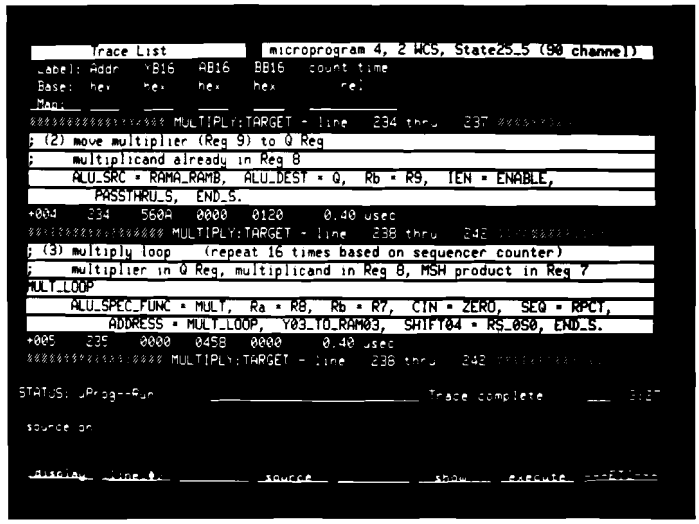


Figure 12. *Microcode source interleaved with trace data provides for very efficient debugging.*

Emulation Memory

Emulation Memory Systems

There are two emulation memory systems, HP 64152S for 8-bit systems and HP 64156S for 8 and 16-bit systems.

HP emulation memory is a dual-port system which allows host access to emulation memory without disturbing emulation. In addition, it is a high-speed universal memory system that works with many different microprocessors and microcontrollers. This provides for real-time emulation and also provides memory display capabilities without stopping emulation. Memory can be mapped as emulation ROM/RAM, target ROM/RAM, or "guarded" access across the full address range of the microprocessor. The following compatibility chart lists the appropriate emulation memory system for each emulation subsystem.

Emulator Model Number	Micro-Processor Supported	Memory Compatible
64192S	6805U/R	N/A*
64193S	6805P	N/A*
64194S	146805G2	N/A*
64195S	146805E2	N/A*
64202S	8080	64152S
64203S	8085	64152S
64206S	6301V/X/Y/6303	64156S
64212S	6800	64152S
64213S	6802/6808	64152S
64215S	6809	64152S
64216S	6809E	64152S
64220S	8086/80C86	64156S
64221S	8088/80C88	64156S
64224S	80186	64156S
64225S	80188	64156S
64228S	80286	64156S
64232S	Z8001	64156S
64233S	Z8002	64156S
64243AA/AB	68000	64156S
64244AA	68008	64156S
64245AA/AB	68010	64156S
64253S	Z80	N/A*
64256S	6801/6803	64156S
64262S	8048	N/A*
64264S	8051	64156S
64272S	ROM	64156S
64274S	User Definable	64156S
64285S	TMS32010	N/A*
64286SB	F9450	N/A*
64292S	NSC800	64156S
64294S	70116	64156S
64295S	70108	64156S

*Emulation memory is provided on the emulation control board.

Ordering Information

Model	Description
64152S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
64156S	**Emulation Memory System, 32 kbytes**
Opt 011	Expand to 64 kbytes
Opt 012	Expand to 128 kbytes
Opt 013	Expand to 256 kbytes
Opt 014	Expand to 512 kbytes
Opt 015	Expand to 1024 kbytes

Language Tools

Additional Assemblers/Linkers

Assemblers/linkers are available for every HP 64000 emulator; in addition, there are assemblers/linkers for selected microprocessors that are not supported with an emulator. With the assembler/linker, the software engineer can write code for the target processor in the assembly language mnemonics to create relocatable modules that can be linked together to form larger programs. Most cross assemblers/linkers are available to execute on a selection of host computer systems. Code can be developed on an HP 64000 station and on the host computer.

To support an even broader base of software development tools, there are two user-definable products to generate assemblers/linkers and inverse assemblers for other microprocessors: Model 64851A User Definable Assembler software and Model 64856A User Definable Inverse Assembler. Experienced programmers can typically write new assemblers/linkers and inverse assemblers in one to two weeks.

Model	Description	Microprocessors
64843*	Assembler/Linker	6502
64847*	Assembler/Linker	9900, 9980, 9985, 9989, 9940
64848	Assembler/Linker	1802
64849	Assembler/Linker	F8, 3870
64850	Assembler/Linker	Z8
64851*	Assembler/Linker	User Definable
64852	Assembler/Linker	HP 1000 L Series
64856	Inverse Assembler	User Definable
64860*	Assembler/Linker	8096
64861*	Microassembler/ Linker	User Definable

*Available for HP 9000 Series 300 Computer System.

High-level Language Support

Hewlett-Packard offers an extensive set of HP 64000 cross compiler tools for microprocessor software development. The cross compilers support many target processors and run on a selection of host computer systems. Code can be developed on an HP 64000 or HP 64000-UX station and on the host computer system.

The HP 64800 Series Pascal and C Cross Compilers are much more than language translators. Not only are the language implementations optimized for microprocessor-based design applications, but the compilers are integrated into the HP 64000 development environment and generate the database needed to operate HP's powerful emulator-based analysis tools.

The following compilers are available on the HP 9000 Series 300 and 500 host computer systems and VAX/VMS host computer system, as well as on Models 64100A and 64110A development stations.

Model	Description	Microprocessor
64811	Pascal Cross Compiler	6800 family
64813	Pascal Cross Compiler	6809
64814	Pascal Cross Compiler	8086/80286 family
64815	Pascal Cross Compiler	68000/68008/68010
64816	Pascal Cross Compiler	Z8001/Z8002
64818	C Cross Compiler	8086/80286 family
64819	C Cross Compiler	68000/68008/68010
64820	C Cross Compiler	Z8001/Z8002
64821	C Cross Compiler	6800 family
64822	C Cross Compiler	6809
64823	Pascal Cross Compiler	Z80/NSC800
64824	C Cross Compiler	Z80/NSC800
64825	Pascal Cross Compiler	8080/8085
64826	C Cross Compiler	8080/8085

Analysis and Interactive Measurements

Strengths of System Solutions

Each of the HP 64000 design and development tools provides special capabilities for software development, emulation, or analysis. But, the primary strength of the HP 64000 system is the capacity for interactive application of measurement and design aids.

Designers and developers appreciate the convenience of moving smoothly between development, emulation, and analysis—all from the familiar, friendly development station environment. Cross-triggering and cross-arming modes automatically transfer control between subsystems contingent on specified conditions. And, most importantly, the added modularity and power of interactive emulation and analysis enable the designer to get the job done right the first time.

Emulation Bus Analyzer

Model 64302A

Model 64302A Emulation Bus Analyzer adds real-time, transparent analysis of activity on the emulator bus. State display listings are in a selected numerical base, or in the microprocessor mnemonics. When analyzing compiled code, source code is displayed*. For most applications, an emulator bus analyzer is an essential part of a complete emulation system.

Model 64302A Emulation Bus Analyzer accommodates addresses as wide as 24 bits. It is compatible with emulators for all the 8-bit and 16-bit microprocessors.

*Available only in HP 64000-UX environment.

Expanded and Interactive Measurement Systems

As your microprocessor system grows, it becomes increasingly more complex. You can add correspondingly more powerful HP 64000 measurement tools as they are needed to serve new levels of analysis. Analyzers are available for the whole spectrum of logic measurements—from a bit-by-bit analysis of individual signal lines to a total system performance analysis.

Any combination of HP 64000 system analyzers can be operated interactively through the Intermodule Bus (IMB). An emulator may be added to an interactive measurement scheme by adding its HP 64302A Emulation Bus Analyzer to the IMB. For multiprocessor applications, the emulator can be used interactively with other HP 64000 system emulators through the IMB. The IMB also supports cross-triggering between analysis tools.

Larger measurement systems made possible by the IMB are not restricted to analysis and emulation subsystems in a single development station; the HP 64303A IMB Extender board* gives you access to measurement tools resident in other development stations. One extender board is installed in each of the stations containing an analysis system that receives the cross-station signals. The development station pairs are connected with up to four BNC-to-BNC coaxial cables. Specifications and applications of Model 64303A IMB Extender are covered in a separate data sheet. In the HP 64000-UX environment, the IMB Extender is resident in the instrumentation card cage.

*Compatible only with HP 64100A and 64110A development stations.

High-speed Timing/State Analyzer
Model 64610S

As target system hardware evolves, a Model 64610S High-speed Timing/State Analyzer can be added to check timing relationships at speeds up to 400 MHz. Model 64610S offers powerful high-resolution, asynchronous and synchronous analysis with extensive postprocessing capabilities in the HP 64000 development environment. Model 64610S consists of a control card (HP 64601B) and acquisition card (HP 64602A) with timing and clock probes. Eight input channels are expandable to 32 channels for timing or state analysis.

With an HP 64610S analyzer, you can examine closely the detail of the executing system. Many triggering modes allow precise positioning of the display window to locate timing margin, state execution, and interaction problems. The analyzer's resources can be allocated to provide wide, fast, glitch, dual-threshold, and externally clocked measurements (figure 13). An external clock mode provides state analysis capabilities at clock speeds up to 125 MHz with up to 32 input channels. Post-processing capabilities allow the user to compare measurements, mark significant signal combinations, and compute means and variances of specified intervals.

Hard copy of the timing diagrams can be obtained using the HP 64050A Graphics Board* and a compatible HP printer or plotter. For more information on this analyzer and graphics board, refer to the data sheet for Model 64610S High-speed Timing/State Analyzer.

*Compatible only with HP 64100A and 64110A development stations.

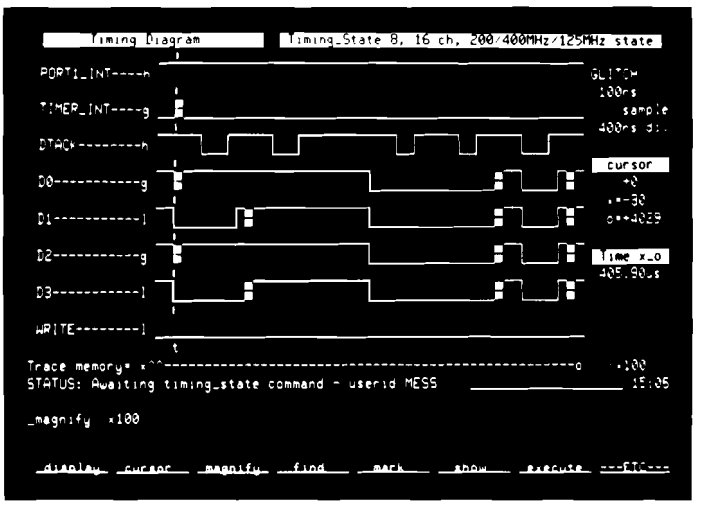


Figure 13. *Timing analysis in glitch mode triggers on, and stores, glitches as short as 3 ns. Each analysis mode features user-defined labels and special display features which make it easy to interpret the trace.*

Logic State/Software Analyzer

Model 64620S

At the next level of measurement, a Model 64620S Logic State/Software Analyzer has the functions to support intricate analysis modes: up to 120 input channels, 15 levels of sequential triggering, broad definitions for storage qualifiers, and measurement window specifications. A modular subsystem, the HP 64620S analyzer can be configured for 20 to 120 input channels using 20-channel and 40-channel data acquisition boards with a control board. Model 64620S can be connected to the emulation subsystem through the HP 64304A Emulation Bus Preprocessor to enhance or replace the HP 64302A Emulation Bus Analyzer.

Key attributes of the HP 64620S are flexibility and power. Configuration of the analyzer may be matched to analysis needs, by channel count and by including or omitting the overview analyzer carried on the 20-channel data acquisition board. Connection set-ups may be internal or external. External connections can be made through the HP 64650A preprocessor and a microprocessor-specific interface or by individual probe leads. Internally, Model 64304A Emulation Bus Preprocessor provides a direct interface to the emulation system.

The added power of software analysis provides traces converted to high-level language source code as well as assembly language or numeric code lists. A mixed display can show high-level statements, with each statement followed by the associated assembly code, similar to an expanded listing (figure 14). Multilayered store functions are well suited to troubleshooting complex and large-scale programs.

For more information on the state/software analyzer and the emulation bus preprocessor, refer to the data sheet for Model 64620S Logic State/Software Analyzer.

Preprocessors

HP Preprocessor Interface Modules provide a quick and convenient interface between microprocessor systems and the HP 64620S Logic State/Software Analyzer. These processor-specific modules are installed in HP 64650A General Purpose Preprocessors for connection to the state analyzer. Measurements are displayed in the target microprocessor's assembly language. This connection system permits the HP 64620S analyzer to probe microprocessors and target systems even when no emulator is present.

The HP 64620S analyzer is automatically configured by the preprocessor interface's inverse assembler which translates the trace lists into the microprocessor's mnemonics. Measurements can be specified using symbols defined in the user program.

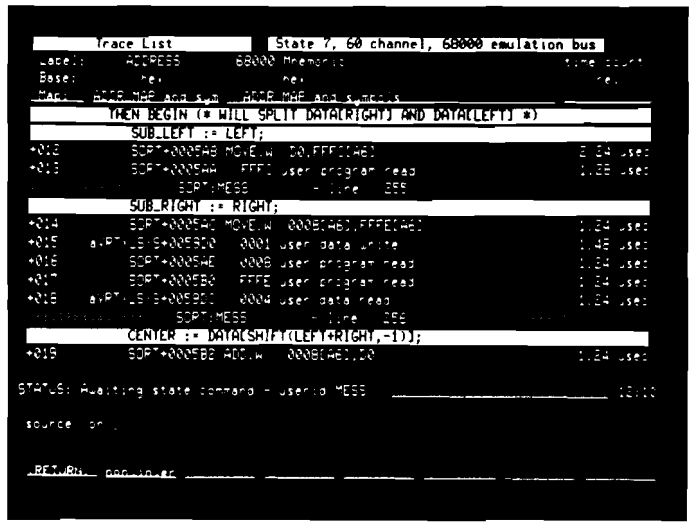


Figure 14. *Symbols are displayed in a state trace, making it easier to determine where the program is executing. For compiled code, source lines can be displayed.*

The following chart lists model numbers of preprocessors for supported microprocessors.

Interface Modules

Model	Microprocessor
64653A	8086/8088
64655A	8085
64657A	80286
64658A	80186/80188
64659A	80386
64671A	6809/6809E
64672B	6800/6802
64673A	68008
64674A	68000/68010
64675A	68020
64680A	Z8001
64681A	Z8002
64683A	Z80
64690A	NSC800
64695A	RS-232C/V.24, RS-449, HP-IB buses

Software Performance Analyzer
Model 64310A

For optimizing and characterizing software performance, the HP 64310A Software Performance Analyzer provides macro views of total system performance by activity, linkage, or duration measurements (figure 15). The performance analyzer becomes an integral part of the emulation system, so you can begin optimizing time-critical software early in the design cycle.

The performance analyzer collects information from the emulator bus, and is integrated into the emulation subsystem. Both high-level and assembly-level code can be analyzed, even when mixed.

Model 64310A Software Performance Analyzer offers six measurement modes to analyze total target system software execution. Two activity measurements—memory activity and program activity—can be used to point out code hot spots. The linkage measurement—intermodule activity—can be used to determine the relative frequency of calls from one module to several others, or vice versa. The duration measurements—module duration, intermodule duration, and module usage—can be used to find modules of code which take too long to execute.

Used in conjunction with an emulator, the Software Performance Analyzer helps the software designer spot design problems as soon as the very first modules are written.

A separate data sheet on Model 64310A Software Performance Analyzer contains detailed information on applications of performance analysis.

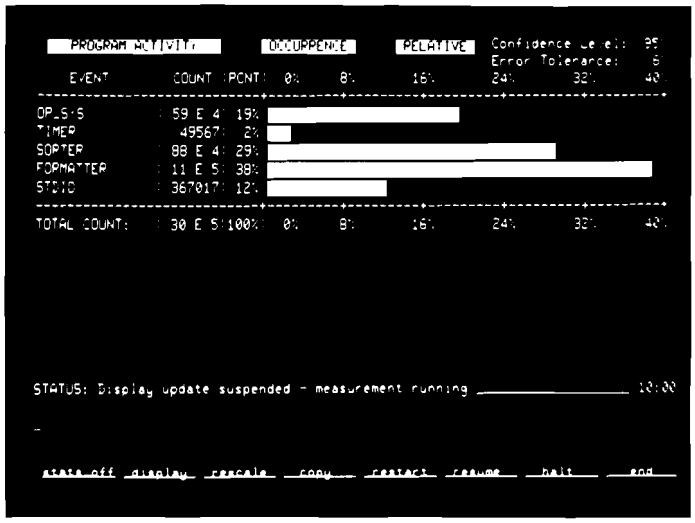


Figure 15. *This measurement indicates overall activity of the program. The display is constantly updated (but can be suspended to make it easier to read) so that changes in activity due to changing stimulus can be measured. This is very useful when tuning microprocessor-based systems.*

High-level Software Analyzers*

Model 64330
Model 64340

Hewlett-Packard High-level Software Analyzers offer HP 64100A and 64110A users an advanced, yet easy-to-use, feature set for analysis of programs written in Pascal or C. The analyzers are processor and emulator specific. Measurements are specified and displayed in the high-level context used in generating the software. Two series of high-level software analyzers are available for the HP 64100A and 64110A development stations: HP 64330 High-level Software Analyzers and HP 64340 Real-time High-level Software Analyzers. The HP 64330 requires the appropriate emulator and the HP 64302A Emulation Bus Analyzer; the HP 64340 requires the appropriate emulator and the HP 64340A hardware.

Both series of analyzers trace program and data flow in executing code. The HP 64330 High-level Software Analyzer adds no extra code to the software under test, but it does stop program execution periodically by inserting software traps to accommodate the analyzer. By contrast, in real-time mode, the HP 64340 Real-time High-level Software Analyzer is fully transparent to the system under test, and it meets all criteria for real-time analysis: the processor is not halted, program execution is not stopped, and additional code and traps are not added to the target software.

Hierarchical measurement modes provide a spectrum of perspectives of software operation. Trace Modules and Trace Data Flow quickly focus analysis on the location of any software problems before applying more detailed debugging at the statement level. Trace Statements (figure 16) and Trace Variables measurements display more detailed information on specific source statements and actual values of selected variables. In addition, the HP 64340 analyzer has Time Modules and Count Statements to measure the absolute time used by an executing module and to count the number of times specified source statements are executed. Determining execution count of a specific statement is particularly helpful in software coverage testing. The HP 64330 and 64340 analyzers improve software engineering productivity with measurements that are relevant and convenient for troubleshooting software written in high-level programming languages.

*Compatible only with HP 64100A and 64110A development stations.

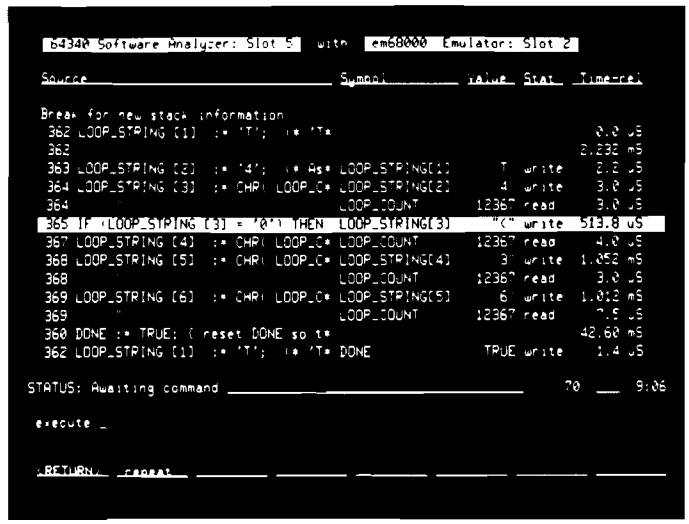


Figure 16. *A "trace statements" measurement shows the order of execution of high-level statements, and even shows the source code from the program. In addition, symbols, or variables, in the statements are evaluated if possible. Finally, when using the real-time analyzer, Model 64340A, time intervals between stored statements and stored variables are measured.*

The high-level software analyzers combine sophisticated software and hardware. A high degree of compatibility with the HP 64000 system cross compilers supports measurements that are closely related to the high-level languages. Measurements may be specified in terms of static and dynamic variables; files, programs, procedures, and function names; as well as source code line numbers. A close link to the HP 64000 emulation subsystem adds the further advantages of displaying/modifying variables and controlling execution of a program under test. Directed-syntax softkeys simplify transitions from software analysis to software synthesis, and back again. After identifying a programming error, it takes only a few keystrokes to correct, recompile, relink, run the modified program, and then return to the software analyzer to verify the modifications.

The following analyzers are available for the appropriate microprocessors and their HP 64000 emulators.

Analyzer Model	Supported Microprocessor	Emulator Model
HP 64330 High-level Software Analyzers		
64331B	68000	64243AA/AB
64332B	8086/80C86	64220S
64333B	8088/80C88	64221S
64334B	68010	64245AA/AB
64335A	80186	64224S
64336A	80188	64224S
64337A	68008	64244AA
64338A	70116 (V30)	64294S
64339A	70108 (V20)	64295S
HP 64340 Real-time High-level Software Analyzers		
64341AA	8086/80C86	64220S
64341CA	8088/80C88	64221S
64341EA	80186	64224S
64341FA	80188	64225S
64341GA	68000	64243AA/AB
64341IA	68010	64245AA/AB
64342AA	70116 (V30)	64294S
64342BA	70108 (V20)	64295S

A separate data sheet on Models 64330 and 64340 High-level Software Analyzers contains detailed information on applications of these analyzers.

General Emulation Subsystem Specifications

Processor compatibility: each emulator subsystem is compatible with the microprocessor for which it is specified as well as any microprocessor which complies with the specifications of that particular microprocessor.

Physical

Cable length: development station to emulation pod, approx 1.5 m (5 ft); emulation pod to target system interface, approx 305 mm (1 ft). (Cables for a few emulators may vary slightly from these dimensions.)

Environmental

Temperature: operating, 0° to 40°C (32° to 104°F); nonoperating, −40° to 75°C (−40° to 167°F).

Altitude: operating, 4600 m (15 000 ft); nonoperating, 15 300 m (50 000 ft).

Relative humidity: 5% to 80%.

Accessories Supplied

Each HP 64000 Emulation Subsystem consists of an emulation pod and emulation control board; appropriate cables for connections from the control board to the pod and from the pod to the target system; operator and service manuals; operating software supplied on flexible disc for HP 64100A and 64110A development stations. When availability is indicated in the ordering information for an emulator, Option 004 adds emulation software hosted on HP 9000 Series 300 Computer Systems. Emulation/analysis bus cables must be ordered separately.

Hardware Accessories

64960A	**2-position Emulation/Analysis Bus Cable**
Opt 001	3-position Emulation/Analysis Bus Cable
Opt 002	4-position Emulation/Analysis Bus Cable

Software Support

Hewlett-Packard offers extended software support for all emulators, analyzers, and language tools with Right-to-copy Licenses and One-time Updates. Software Materials Subscriptions are also available for operating software. See your HP Sales Representative for further information.

HP's Complete Solution for Your Success

Success in today's business environment depends on obtaining high productivity from both people and equipment. Selecting the right measurement and/or computer system is essential to achieving proper results. Achieving the best results from a measurement or computer solution involves more than just purchasing the right equipment; it also involves support of that equipment. Hewlett-Packard is a world leader in customer support and satisfaction.

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- Hardware Support helps minimize productivity interruption for maintenance and calibration, so that you can prolong your system's useful life.
- Software Support ensures that your system software is as current and productive as possible so you can maintain your competitive edge.

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Hewlett-Packard can be your partner in success. From your first consideration of an application solution through the entire life cycle of your system's implementation and use, HP stands behind your success with a complete range of worldwide support services. Choose Hewlett-Packard as your partner in success and you are assured of state-of-the-art hardware, software, and support.

Support Matrix and Index

MICRO-PROCESSOR	EMULATORS	ASSEMBLER/ LINKER*	PASCAL COMPILER*	C COMPILER*	INTERFACE MODULE	PAGE NUMBER
FAIRCHILD						
F9450	64286SB	64857S	—	—	—	9
HITACHI						
6301V/03R	64206S	64841S	64811S	64821S	—	10
6301X/03X	64207S	64841S	—	—	—	10
6301Y/03Y	64208S	64841S	—	—	—	10
64180	—	64864A	—	—	—	—
INTEL						
8048/49	64262S**	64846S	—	—	—	11
8051/31	64264S	64855S	—	—	—	12
8080	64202S**	64840S	64825S	64826S	—	13
8085	64203S	64840S	64825S	64826S	64655A	13
8086	64220S	64853S	64814S	64818S	64653A	14
80C86	64220S Opt 001	64853S	64814S	64818S	64853A	14
8088	64221S	64853S	64814S	64818S	64653A	14
80C88	64221S Opt 001	64853S	64814S	64818S	64853A	14
80186	64224S	64853S	64814S	64818S	64658A	16
80188	64225S	64853S	64814S	64818S	64658A	16
80286	64228S	64859S	64814S	64818S	64657A	17
MOTOROLA						
6800	64212S**	64841S	64811S	64821S	64672B	19
6801/03	64256S	64841S	64811S	64821S	—	20
68HC11	64265A	64865S	—	—	—	—
6802/08	64213S**	64841S	64811S	64821S	64672B	19
6805R/U	64192S	64844S	—	—	—	21
6805P	64193S	64844S	—	—	—	21
146805E2	64195S	64844S	—	—	—	22
146805G2	64194S	64844S	—	—	—	23
6809	64215S	64844S	64813S	64822S	64671A	24
6809E	64216S	64844S	64813S	64822S	64671A	24
68000 (DIP)	64243AA	64845S	64815S	64819S	64674A	25
68000 (PGA)	64243AB	64845S	64815S	64819S	64674A	25
68008	64244AA	64845S	64815S	64819S	64673A	25
68010 (DIP)	64245AA	64845S	64815S	64819S	64674A	27
68010 (PGA)	64245AB	64845S	64815S	64819S	64674A	27
NATIONAL						
NSC800	64292S**	64842S	64823S	64824S	64690A	28
NEC						
70108	64295S	64853S	64814S	64818S	—	29
70116	64294S	64853S	64814S	64818S	—	29
70208	64297S	64853S	64814S	64818S	—	—
70216	64296S	64853S	64814S	64818S	—	—
TEXAS INSTRUMENTS						
TMS32010	64285S**	64858S	—	—	—	30
ZILOG						
Z80	64253S	64842S	64823S	64824S	64683A	31
Z8001	64232S	64854S	64816S	64820S	64680A	32
Z8002	64233S	64854S	64816S	64820S	64681A	32
ROM	64272S**	64851S	—	—	—	35
UDE	64274S	64851S	—	—	—	33
Microprogram (Bit Slice)	64276B**	64861S	—	—	—	36

*Order Option 001 for HP 9000 Series 500 support; Option 003 for VAX/VMS support; Option 004 for HP 9000 Series 300 support.
**Supported only by HP 64100A and 64110A Logic Development Stations.

Printed in U.S.A.
5954-8101

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