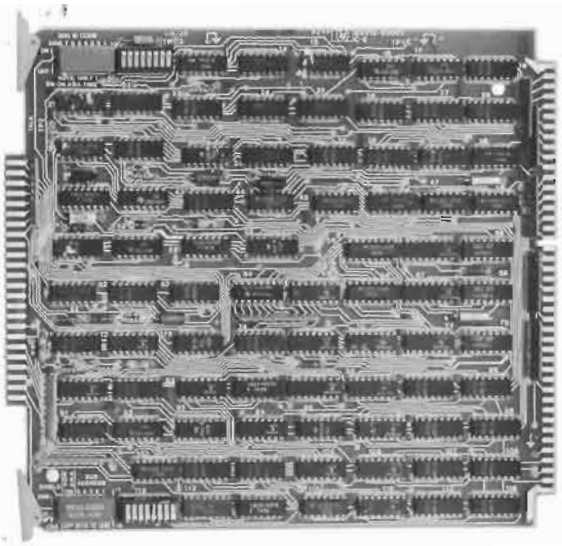
OPERATING AND SERVICE MANUAL

BUS INPUT/OUTPUT INTERFACE KIT

59310A



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59310A/B

BUS INPUT/OUTPUT INTERFACE KIT

OPERATING AND SERVICE MANUAL

UPDATING SUPPLEMENT

12 MAY 1977

MANUAL IDENTIFICATION

Manual Serial No. Prefix: 1348A

Manual Printed: June 1975

Manual Part No.: 59310-90007

Microfiche Part No.: 59310-90008

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to equipment containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left. For any given instrument serial number prefix, all change steps noted for prior serial number prefixes must be incorporated in addition to those for the given prefix.

INSTRUMENT CHANGES

Serial No. Prefix	Change
Not Applicable	

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Series	Changes
A1	Board Assembly, Bus I/O	59310-60101	1606	1 thru 19
A1	Board Assembly, Bus I/O	59310-60101	1716	20 and 21

Changes 1 through 19 dated 12 March 1976.
Change 15 and tables 1-1 and 1-3 revised 4 May 1976.
Changes 20 and 21 dated 12 May 1977.

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CHANGE	DESCRIPTION
1	Change "59310A" to "59310A/B" throughout the manual.
2	Title Page. Add serial prefix: 1606
3	Title Page. Add the following to the serial prefix paragraph: This manual also applies directly to Hewlett-Packard Model 59310B Bus Input/Output card with serial prefix 1606.
4	Page 1-0. Replace table 1-1 with the table 1-1 attached to this supplement.
5	Page 1-4. Replace table 1-3 with the table 1-3 attached to this supplement.
6	Page 2-3, paragraph 2-17. Add the following to paragraph 2-17: On the 59310B Bus I/O Card (59310-60101), DIP switches are permanently installed — no storage positions exist on the card.
7	Page 2-3, Figure 2-1. Replace figure 2-1 with the figure 2-1 attached to this supplement.
8	Page 2-5, paragraph 2-28. Change the paragraph to read: 2-28. To verify proper operation of the 59310A/B, run the diagnostic program as described in the 59310A/B Bus Input/Output Card Diagnostic manual (part number 59310-90061).
9	Page 3-2, paragraph 3-12. Add the following after "Serial Polling": Parallel Polling: Allows the computer to determine the device(s) needing service by sending one Universal Command to all devices and reading the status bits returned on the data lines. If jumper W1 is installed (59310B only) a Parallel Poll response causes a computer interrupt.
10	Page 3-15, paragraph 3-63. After the paragraph, add the following: NOTE Devices transferring data bytes to the computer under DMA control must complete the 3-wire Handshake in less than three microseconds; otherwise each data byte will be duplicated.
11	Page 3-20, Table 3-1. The Data Codes given for the Remote Enable Command and the Local Command functions are erroneously transposed.
12	Page 4-2, paragraph 4-14. After paragraph 4-14, add the following paragraph: 4-14A. The 59310A and the 59310B are electrically identical except for the circuit differences indicated in changes 16 through 18 of this supplement. The added circuits of the 59310B enable it to: 1) detect a Parallel Poll (U101); 2) detect a Parallel Poll response (U55); and 3) cause a Parallel Poll computer interrupt (U112, and W1 installed). If W1 is not installed, the 59310B functions essentially the same as the 59310A.
13	Page 5-1, paragraph 5-4. Change the paragraph to read: 5-4. Refer to the 59310A/B Bus Input/Output Card Diagnostic manual, part number 59310-90061; for diagnostic program use part number 59310-16001. The program is designed to rapidly confirm proper operation of the Bus I/O card and to assist in troubleshooting defective cards.
14	Page 6-4, Table 6-2. Replace Table 6-2 with Table 6-2 of this supplement.

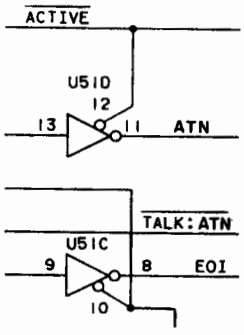
CHANGE **DESCRIPTION**

15 Page 6-6, Table 6-2. Add the following at the end of the table:

	OPTION 422 - 59310B HP INTERFACE BUS COMPUTER I/O KIT INCLUDES:				
	59310-16002	1	TP-RTE DVR37 W/O SRQ	28480	59310-16002
	59310-16003	1	TP-RTE DVR37 W/SRQ	28480	59310-16003
	59310-16004	1	TP-UTILITY SUBROUTINE	28480	59310-16004
	59310-90063	1	MANUAL-RTE DRIVER	28480	59310-90063

	OPTION 423 - 59310B HP INTERFACE BUS COMPUTER I/O KIT INCLUDES:				
	59310-60020	1	TP-DVR D.37A	28480	59310-60020
	59310-60021	1	TP-DVR D.37B	28480	59310-60021
	59310-60050	1	TP-BUS LIBRARY	28480	59310-60050
	59310-90022	1	MANUAL-BCS DRIVER	28480	59310-90022
	59310-90050	1	MANUAL-BCS UTILITY	28480	59310-90050

16 Page 8-9, Figure 8-5 (Sheet 1 of 3). Change the schematic diagram at zones 13, 14, and 1C, 1D as shown below:



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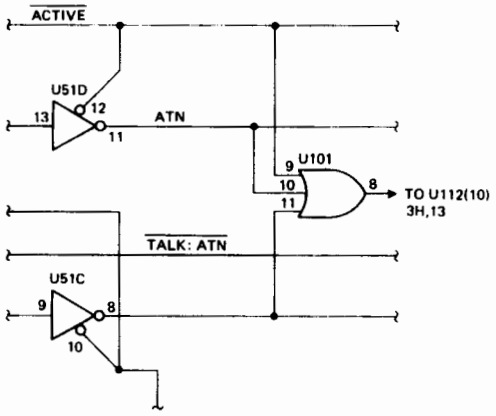
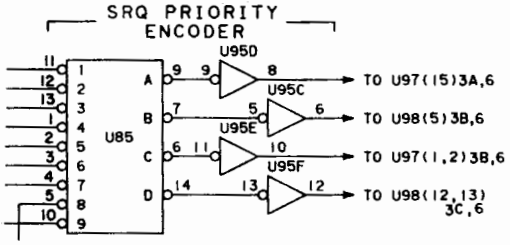


59310B

17 Page 8-11, Figure 8-5 (Sheet 2 of 3). Change the schematic diagram at zones 10, 11, and 2A, 2B as shown below:



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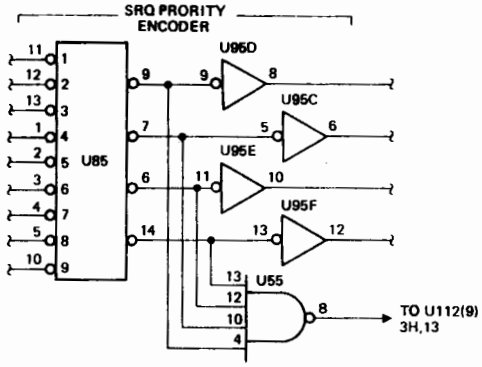
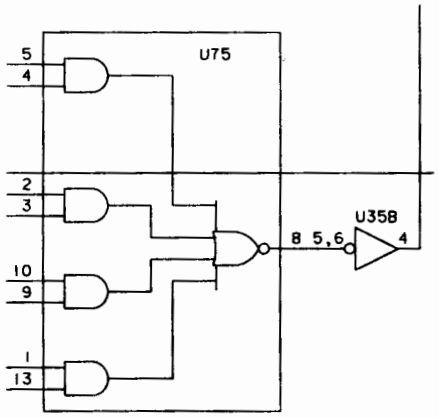


59310B

18 Page 8-18, Figure 8-5 (Sheet 3 of 3). Change the schematic diagram at zones 13, 14, and 3G, 3H as shown below:



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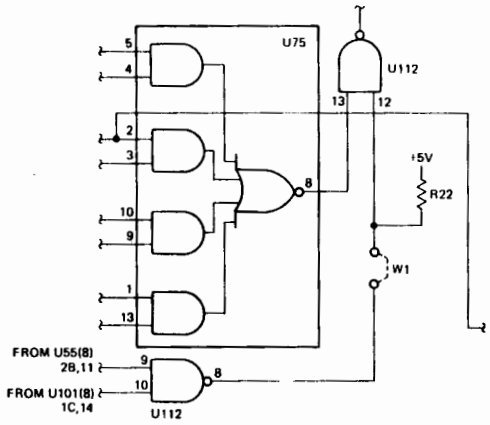
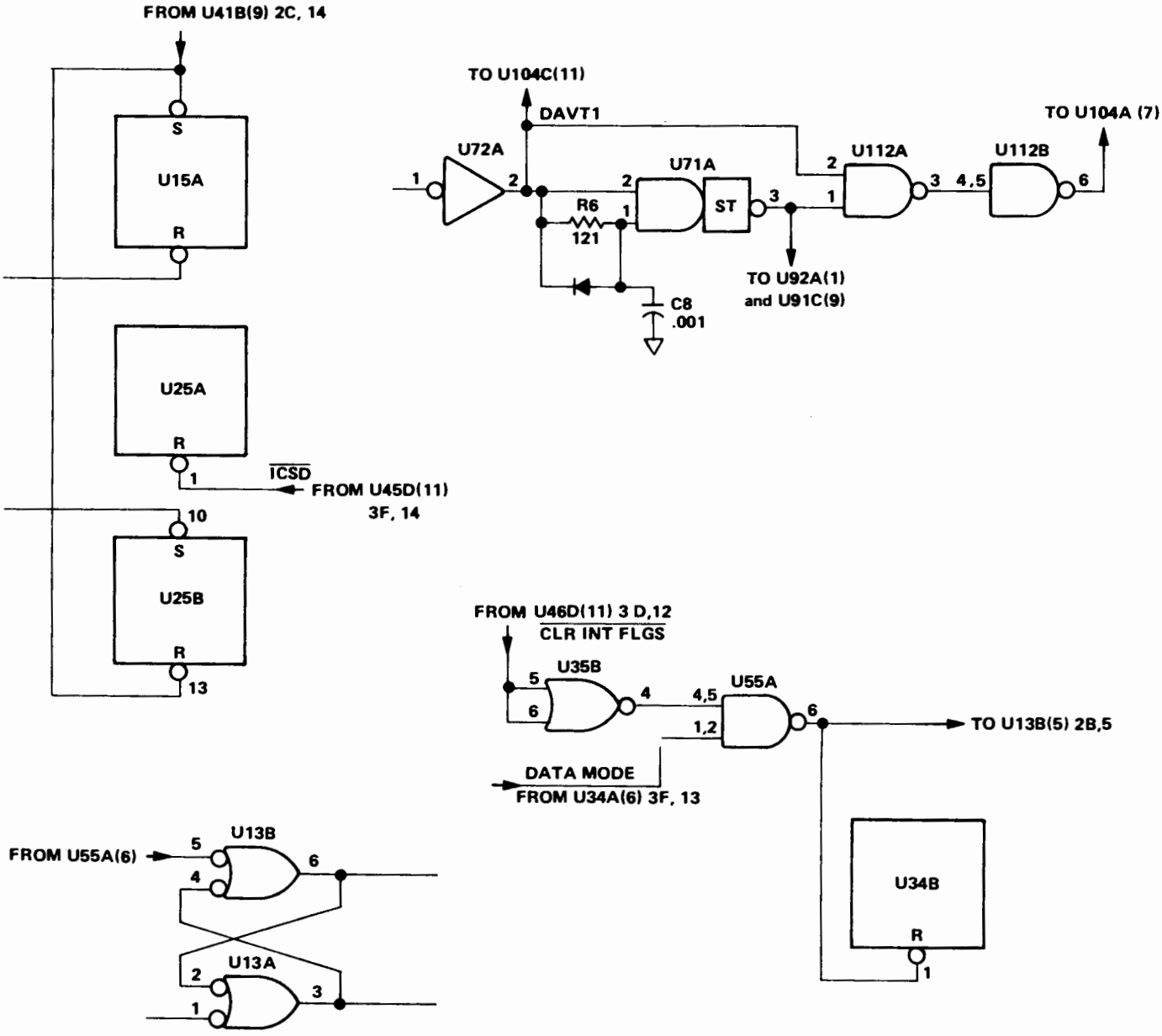


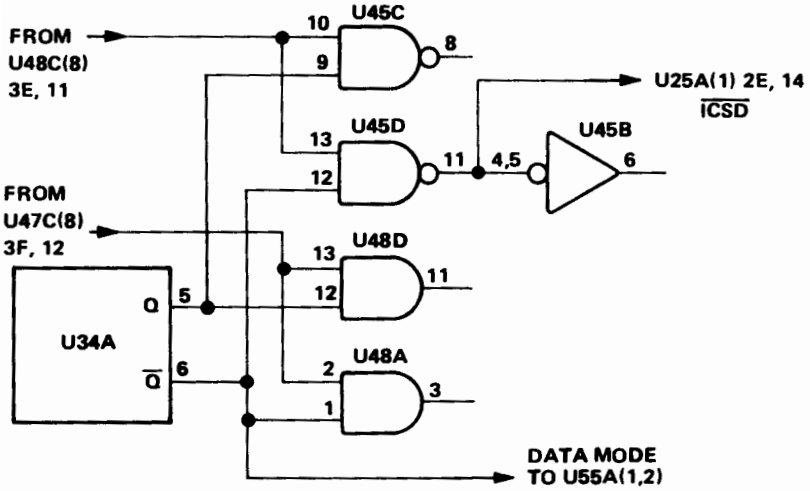
59310B

19 Page 8-9, Figure 8-4. Replace figure 8-4 with figure 8-4 attached to this supplement.

CHANGE	DESCRIPTION
20	Page 8-11, Figure 8-5 (Sheet 2 of 3). Change the schmatic diagram at zones 5A, 11E, 12E, 13E, and 14D,E,F and 14H as shown in the diagrams below. Only the changes are shown.



CHANGE	DESCRIPTION
21	Page 8-13, Figure 8-5 (Sheet 3 of 3). Change the schematic diagram at zones 13F, 14F, 15D and 16D as shown in the diagrams below. Only the changes are shown.



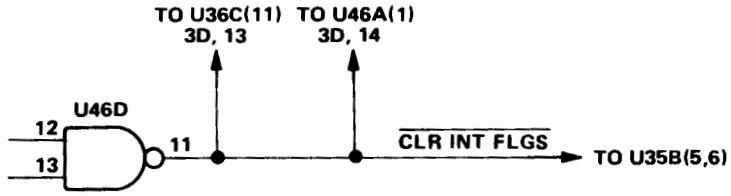


Table 1-1. Equipment Supplied

DESCRIPTION	59310A (HP PART NO.)	59310B		
		STANDARD	OPT. 422	OPT. 423
Bus I/O Card	59310-60001	59310-60101	–	–
Cable Assembly	59310-60002	59310-60002	–	–
Tape Diagnostic	59310-16001	59310-16001	–	–
Operating and Service Manual	59310-90007	59310-90007	–	–
Diagnostic Manual	59310-90061	59310-90061	–	–
Tape, BCS Driver - D.37A (non-DMA)	59310-60020	–	–	59310-60020
User's Guide	–	59310-90064	–	–
Tape, BCS Driver - D.37B (DMA)	59310-60021	–	–	59310-60021
Tape, Bus Library	59310-60050	–	–	59310-60050
BCS Driver Manual	59310-90022	–	–	59310-90022
BCS Utility Subroutines Manual	59310-90050	–	–	59310-90050
Tape, RTE Driver - DVR37 (non-SRQ)	–	–	59310-16002	–
Tape, RTE Driver - DVR37 (SRQ)	–	–	59310-16003	–
Tape, RTE Utility Subroutines	–	–	59310-16004	–
RTE Driver Manual	–	–	59310-90063	–

Table 1-3. 59310A/B Available Software

59310A	59310B	MANUALS	
		PART NO.	DESCRIPTION
X	X	59310-90007	Bus I/O Kit Operating and Service
X	X	59310-90022	Driver Program Procedure (BCS, D.37A/B)
X	X	59310-90050	BCS Bus Utility Subroutine
X	X	59310-90061	Diagnostic Program Procedure
–	X	59310-90063	Real-Time Executive System Driver (DVR37) Programming and Operating
–	X	59310-90064	User's Guide
		SOFTWARE, BINARY PUNCHED PAPER TAPES	
X	X	59310-60020	BCS Bus I/O Card Driver, non DMA (D.37A)
X	X	59310-60021	BCS Bus I/O Card Driver, DMA (D.37B)
X	X	59310-60050	BCS Bus Utility Library (BLIB)
X	X	59310-16001	Bus I/O Card Diagnostic
–	X	59310-16002	RTE Bus I/O Card Driver, non-SRQ (DVR37)
–	X	59310-16003	RTE Bus I/O Card Driver, SRQ (DVR37)
–	X	59310-16004	RTE Bus Utility Library

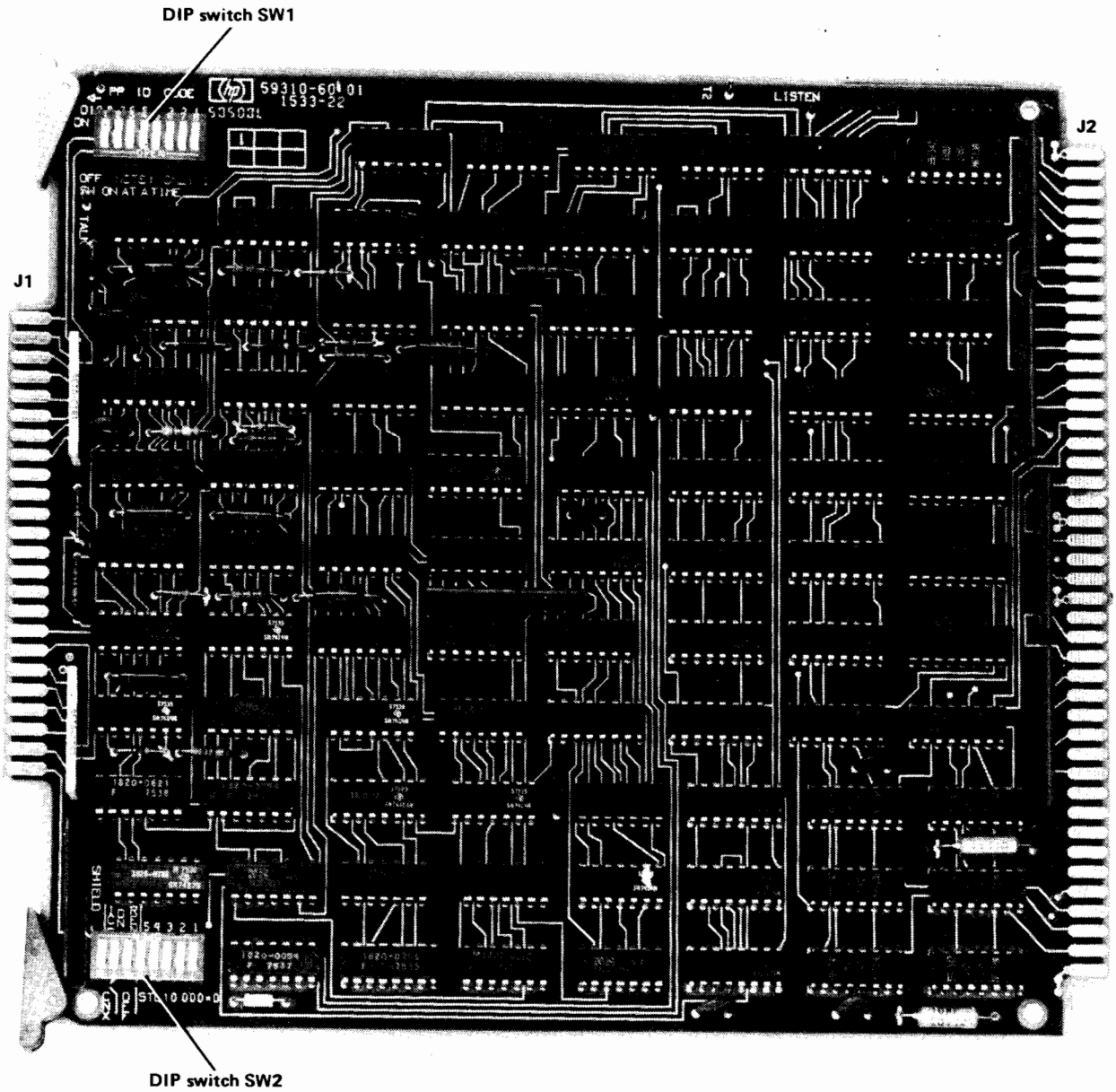


Figure 2-1. Installation Information

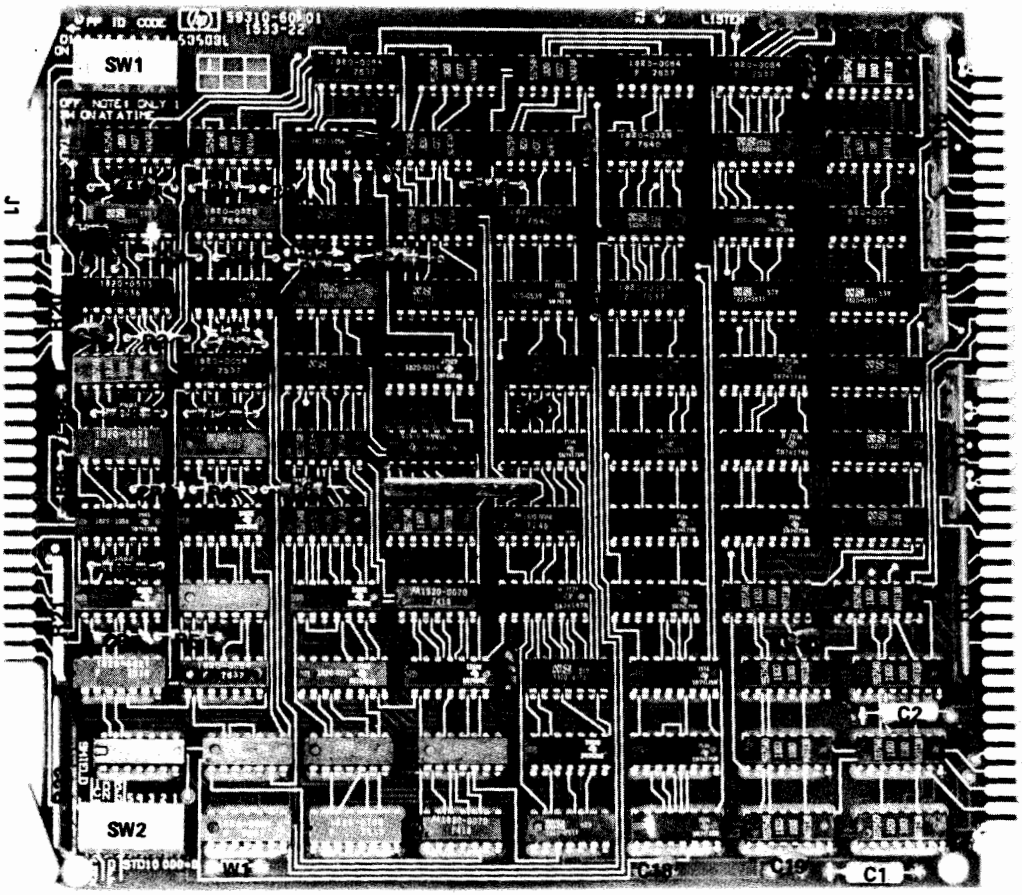


Figure 8-4. Component Locator

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	59310-60101	1	BOARD ASSEMBLY, BUS I/O	28480	59310-60101
C1	0180-0374	2	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C2	0180-0374		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C3	0160-0153	3	CAPACITOR-FXD 1000PF +-10% 200WVDC POLYE	56289	292P10292
C4	0160-0155	1	CAPACITOR-FXD 3300PF +-10% 200WVDC POLYE	56289	292P33292
C5	0160-2640	1	CAPACITOR-FXD .01UF +-20% 50WVDC CER	28480	0160-2640
C6	0160-0157	1	CAPACITOR-FXD 4700PF +-10% 200WVDC POLYE	56289	292P47292
C7	0160-0153		CAPACITOR-FXD 1000PF +-10% 200WVDC POLYE	56289	292P10292
C8	0160-0153		CAPACITOR-FXD 1000PF +-10% 200WVDC POLYE	56289	292P10292
C9	0160-2197	1	CAPACITOR-FXD 10PF +-5% 300WVDC MICA	28480	0160-2197
C10	0160-0154	1	CAPACITOR-FXD 2200PF +-10% 200WVDC POLYE	56289	292P22292
C11	0160-0945	1	CAPACITOR-FXD 910PF +-5% 100WVDC MICA	28480	0160-0945
C12	0160-2055	3	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C18	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C19	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1901-0040	6	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR2	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR3	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR5	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR6	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
R1	0757-0403	7	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-TO-121R-F
R2	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-TO-121R-F
R3	0757-0279	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3161-F
R4	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-TO-121R-F
R5	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-TO-121R-F
R6	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-TO-121R-F
R7	0757-0438	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5111-F
R9	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-TO-121R-F
R10	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-TO-121R-F
R12	0683-1025	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R13	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R14	1810-0121	5	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R15	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R16	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R17	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R18	1810-0041	2	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0041
R19	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R20	1810-0136	2	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	28480	1810-0136
R21	1810-0136		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	28480	1810-0136
R22	1810-0041		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0041
S1	3101-1983	2	SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078
S2	3101-1983		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	81073	76YY2078
U13	1820-0054	8	IC SN74 00 N GATE	01295	SN7400N
U14	1820-0077	7	IC SN74 74 N FLIP-FLOP	01295	SN7474N
U15	1820-0077		IC SN74 74 N FLIP-FLOP	01295	SN7474N
U16	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U17	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U18	1820-1080	11	IC N8T13B DRIVER	18324	N8T13B
U21	1820-0077		IC SN74 74 N FLIP-FLOP	01295	SN7474N
U22	1820-0077		IC SN74 74 N FLIP-FLOP	01295	SN7474N
U23	1820-1056	3	IC SN74 132 N COUNTER	01295	SN74132N
U24	1820-0077		IC SN74 74 N FLIP-FLOP	01295	SN7474N
U25	1820-0077		IC SN74 74 N FLIP-FLOP	01295	SN7474N
U26	1820-0328	3	IC SN74 02 N GATE	01295	SN7402N
U27	1820-0068	7	IC SN74 10 N GATE	01295	SN7410N
U28	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U31	1820-0511	6	IC SN74 08 N GATE	01295	SN7408N
U32	1820-0328		IC SN74 02 N GATE	01295	SN7402N
U33	1820-0174	2	IC SN74 04 N INV	01295	SN7404N
U34	1820-0077		IC SN74 74 N FLIP-FLOP	01295	SN7474N
U35	1820-0328		IC SN74 02 N GATE	01295	SN7402N
U36	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U37	1820-1056		IC SN74 132 N COUNTER	01295	SN74132N
U38	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U41	1820-0515	1	IC MV	07263	9602PC
U42	1820-0537	1	IC SN74 13 N SCHMITT	01295	SN7413N
U43	1820-0068		IC SN74 10 N GATE	01295	SN7410N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
U44	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U45	1820-0539	1	IC SN74 37 N BUFFER	01295	SN7437N
U46	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U47	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U48	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U51	1820-1084	3	IC N8T09B DRIVER	18324	N8T09B
U52	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U53	1820-0069	2	IC SN74 20 N GATE	01295	SN7420N
U54	1820-0214	2	IC:TTL BCD-TO-DECIMAL DECODER	01295	SN7442N
U55	1820-0069		IC SN74 20 N GATE	01295	SN7420N
U56	1820-1100	2	IC SN74 298 N MUXR	01295	SN74298N
U57	1820-0788	2	IC SN74 174 N FLIP-FLOP	01295	SN74174N
U58	1820-1049	3	IC DM80 97N BUFFER	27014	DM8097N
U61	1820-0621	2	IC SN74 38 N BUFFER	01295	SN7438N
U62	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U63	1820-1084		IC N8T09B DRIVER	18324	N8T09B
U64	1816-0188	1	IC 256-BIT ROM TTL	28480	1816-0188
U65	1820-0839	7	IC SN74 175 N FLIP-FLOP	01295	SN74175N
U66	1820-1100		IC SN74 298 N MUXR	01295	SN74298N
U67	1820-0788		IC SN74 174 N FLIP-FLOP	01295	SN74174N
U68	1820-1049		IC DM80 97N BUFFER	27014	DM8097N
U71	1820-1056		IC SN74 132 N COUNTER	01295	SN74132N
U72	1820-1053	5	IC SN74 14 N SCHMITT	01295	SN7414N
U73	1820-1084		IC N8T09B DRIVER	18324	N8T09B
U74	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U75	1820-0084	1	IC SN74 53 N GATE	01295	SN7453N
U76	1820-0839		IC SN74 175 N FLIP-FLOP	01295	SN74175N
U77	1820-0839		IC SN74 175 N FLIP-FLOP	01295	SN74175N
U78	1820-1049		IC DM80 97N BUFFER	27014	DM8097N
U81	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U82	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U83	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U84	1820-0070	2	IC SN74 30 N GATE	01295	SN7430N
U85	1820-1082	1	IC SN74 147 N ENCODER	01295	SN74147N
U86	1820-0839		IC SN74 175 N FLIP-FLOP	01295	SN74175N
U87	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U88	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U91	1820-0621		IC SN74 38 N BUFFER	01295	SN7438N
U93	1820-0214		IC:TTL BCD-TO-DECIMAL DECODER	01295	SN7442N
U93	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U94	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U95	1820-0174		IC SN74 04 N INV	01295	SN7404N
U96	1820-0839		IC SN74 175 N FLIP FLOP	01295	SN74175N
U97	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U98	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U101	1820-0782	1	IC SN74 27 N GATE	01295	SN7427N
U102	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U103	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U104	1820-0068		IC SN74 10 N GATE	01295	SN7410N
U105	1820-1053		IC SN74 14 N SCHMITT	01295	SN7414N
U106	1820-0839		IC SN74 175 N FLIP-FLOP	01295	SN74175N
U107	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U108	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U112	1820-0054		IC SN74 00 N GATE	01295	SN7400N
U113	1820-0706	1	IC COMPTR	07263	9324DC
U114	1820-0070		IC SN74 30 N GATE	01295	SN7430N
U115	1820-0511		IC SN74 08 N GATE	01295	SN7408N
U116	1820-0839		IC SN74 175 N FLIP-FLOP	01295	SN74175N
U117	1820-1080		IC N8T13B DRIVER	18324	N8T13B
U118	1820-1080		IC N8T13B DRIVER	18324	N8T13B
W1	8159-0005	1	WIRE 22AWG W PVC 1X22 80C	00736	L-2007-1
			MISCELLANEOUS PARTS		
	5040-6001	1	EXTRACTOR:PC BOARD	28480	5040-6001
	1480-0116	2	EXTRACTOR PIN:1/16" DIA	73957	GP24-063X250-12
	5040-6065	1		28480	5040-6065
	1480-0116		EXTRACTOR PIN:1/16" DIA	73957	GP24-063X250-12

59310A

BUS INPUT/OUTPUT INTERFACE KIT

SERIAL PREFIX: 1348A

This manual applies directly to Hewlett-Packard Model 59310A BUS INPUT/OUTPUT CARD with series number 1348A. For cards with serial prefixes above 1348A, a manual change sheet is supplied. For cards with serial prefixes below 1348A, refer to Section 7.

NOTE

This manual replaces three previous operating and service manuals of the same title, part number 59310-90001 dated July 1973, and part number 59310-90011 and part number 59310-90006 dated August 1973.

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Manual Part Number: 59310-90007
Microfiche Part Number: 59310-90008

Printed in U.S.A.

HEWLETT hp PACKARD

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SAFETY CONSIDERATIONS

GENERAL

This is a Safety Class I instrument. This instrument has been designed and tested according to IEC Publication 348, "Safety Requirements for Electronic Measuring Apparatus", and has been supplied in safe condition.

OPERATION

BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage and the correct fuse is installed. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

SERVICE

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by qualified service personnel.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

WARNING

IF THIS INSTRUMENT IS TO BE ENERGIZED VIA AN AUTO-TRANSFORMER (FOR VOLTAGE REDUCTION) MAKE SURE THE COMMON TERMINAL IS CONNECTED TO THE EARTHED POLE OF THE POWER SOURCE.

WARNING

BEFORE SWITCHING ON THE INSTRUMENT, THE PROTECTIVE EARTH TERMINALS OF THE INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

CAUTION

BEFORE SWITCHING ON THIS INSTRUMENT:

1. **MAKE SURE THE INSTRUMENT IS SET TO THE VOLTAGE OF THE POWER SOURCE.**

2. **ENSURE THAT ALL DEVICES CONNECTED TO THIS INSTRUMENT ARE CONNECTED TO THE PROTECTIVE (EARTH) GROUND.**

3. **ENSURE THAT THE LINE POWER (MAINS) PLUG IS CONNECTED TO A THREE-CONDUCTOR LINE POWER OUTLET THAT HAS A PROTECTIVE (EARTH) GROUND. (GROUNDING ONE CONDUCTOR OF A TWO-CONDUCTOR OUTLET IS NOT SUFFICIENT.)**

4. **MAKE SURE THAT ONLY FUSES WITH THE REQUIRED RATE CURRENT AND OF THE SPECIFIED TYPE (NORMAL BLOW, TIME DELAY, ETC.) ARE USED FOR REPLACEMENT. THE USE OF REPAIRED FUSES AND THE SHORT-CIRCUITING OF FUSE HOLDERS MUST BE AVOIDED.**

Table 1-1. Equipment Supplied

Description	HP Part No.
Bus I/O Card	59310-60001
Cable Assembly	59310-60002
Tape, Diagnostic	59310-60010
Tape, Driver — D.37A	59310-60020
Tape, Driver — D.37B	59310-60030
Tape, Bus Library	59310-60050

Figure 1-1. 59310A Bus Input/Output Kit

SECTION 1
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This section provides general information on the Hewlett-Packard Model 59310A Bus Input/Output Interface Kit shown in Figure 1-1. Included in this section are a 59310A description, card identification, equipment supplied, specifications and Hewlett-Packard Interface Bus description.

1-3. DESCRIPTION

1-4. The HP 59310A Bus Input/Output Interface Kit (I/O card and cable) interfaces the HP Series 2100 Computers to the HP Interface Bus (HP-IB). The HP-IB provides a two-way digital communications structure for one or more instruments with ASCII-compatible interface. Hardware connection of compatible instruments is a matter of plugging them together with the bus cables. Writing software programs for input/output operations to/from the computer is made easier by hardware features on the card such as packing. Basic Control System (BCS) driver and BCS utility routines are furnished.

1-5. The 59310A I/O card makes bus functions available to the computer: listen and talk functions, serial poll identification, controller clearing and four types of interrupt flagging. Data transfers are byte-serial and bit parallel (8-bit bytes) and packing is available. Direct Memory Access (DMA) can be used for data transfers.

1-6. MICROFICHE

1-7. On the title page of this manual, below the manual part number, is a "Microfiche" part number. This number may be used to order 4x6-inch microfilm transparencies of the manual. The microfiche package also includes the latest Manual Changes supplement as well as all pertinent Service Notes.

1-8. CARD IDENTIFICATION

1-9. Each Model 59310A Bus Input/Output card has a five-character series number (e.g. 1640A). The series number identifies a group of identical printed circuit cards. If the series number on your card is not on the title page of this manual, your card is different from this manual. A change sheet is included with this manual to describe the differences. If the change sheet is missing, request one from the nearest Hewlett-Packard Sales and Service office listed at the back of this manual.

1-10. EQUIPMENT SUPPLIED

1-11. Table 1-1 lists the equipment supplied with the Model 59310A Bus Input/Output Kit. The kit is shown in Figure 1-1.

1-12. SPECIFICATIONS

1-13. Specifications for the 59310A Bus Input/Output card are provided in Table 1-2.

Table 1-2. Specifications

ELECTRICAL CHARACTERISTICS

Bus Signal Lines: The Bus consists of 16 signal lines as follows:

DIO1	Data Input/Output 1
.	
.	
.	
DIO8	Data Input/Output 8
DAV	Data Valid
NRFD	Ready for Data
NDAC	Data Accepted
IFC	Interface Clear (was EOP then BCL)
ATN	Attention (was MRE)
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Logic Levels: High ≥ 2.4V
Low ≤ 0.4V

All signals are Low = True except NRFD and NDAC.

Line Termination: Each of the 16 Bus signal lines is terminated with 3KΩ to Vcc and 6.2KΩ to logic common. The value of Vcc depends on the particular 2100 series model in which the card is installed. It varies between 4.5 to 5.0V.

Line Drivers: The signal lines DIO1 through DIO8, DAV, ATN and EOI are drivers with a circuit having the following characteristics:

Type: Tri-State
Output Voltage Low State: ≤ 0.4V @ 48 mA
Output Voltage High State: ≥ 2.4V @ –40 mA

The signal lines NRFD, NDAC, IFC, REN and SRQ are drivers having the following characteristics:

TYPE: Open Collector
Output Voltage Low State: ≤ 0.4V @ 48 mA
Output Voltage High State: Determined by resistor termination
Leakage Current High State: ≤ 0.250 mA @ 5.5V

Line Receivers: Each of the 16 Bus signal lines is received with a circuit having the following characteristics:

Type: Schmitt Trigger
Threshold Positive Transition: 1.5V
Threshold Negative Transition: 1.1V
Input Current Low State: –1.6 mA @ 0.4V
Input Current High State: 0.04 mA @ 2.4V

Maximum Cable Length: 2 meters per device connected, 20 meters total.

Operating Temperature: 0–55°Celsius

Table 1-2. Specifications (Cont'd)

Power Requirements: The card requires the following amounts of power from the computer's power supply:

Supply	Maximum Current Acquired
+30	None
+12	None
+5*	3.0A
-2	100 mA
-12	None

*Value of supply varies from 4.5 to 5.0V depending on model of computer.

PHYSICAL CHARACTERISTICS

Card Dimensions:
Width: 7-3/4 in. (196,8 mm)
Height: 8-11/16 in. (220,7 mm)

Weight:
Net weight, card and cable: 4 lb. (1,81 kg)
Shipping weight: 5 lb (1,94 kg)

Connector: 48-pin printed circuit board edge connector (cable supplied has standard bus connector on outboard end).

1-14. SOFTWARE AVAILABLE

1-15. Software available for use with the 59310A is listed in Table 1-3.

1-16. HEWLETT-PACKARD INTERFACE BUS CAPABILITIES

1-17. HP-IB provides the capability of connecting from one to 14 compatible devices to the computer via one HP 59310A I/O Card. Data is transferred over the Bus bidirectionally in 8-bit bytes. Data can be transferred from a device to the computer or from the computer to one or more devices simultaneously or from one to other devices under the direction of the computer.

1-18. Some bus features MUST be used while others are optional. For example, ALL instruments must be capable of being addressed, but they may or may not be capable of being operated by remote control. A system may have some instruments operating under remote control while other instruments obey their front and rear panel controls (LOCAL). The same pins of all bus connectors of all instruments are connected in parallel making a parallel communication network. This permits information to flow in any direction on the bus and allows any instrument to talk directly with another without going through a central control unit.

1-19. PROGRAM CODE

1-20. Once a system has been assembled, programming is simplified since almost all HP instruments use the same code set. The seven-bit ASCII (USA Standard for Information Interchange) code set was selected because of its wide acceptance in the communications and data handling fields. The HP-IB itself can transmit full eight-bit binary data however. All of these features make the job of interconnecting instruments into a system simple. The job has been reduced to primarily programming.

Table 1-3. 59310A Available Software

MANUALS		
PART NO.		**DESCRIPTION**
59310-90001		Bus I/O Kit Operating and Service
59310-90022		Driver Program Procedure (BCS, D.37A/B)
59310-90010		Diagnostic Program Procedure
59310-90050		BCS Bus Utility Subroutine
SOFTWARE, BINARY PUNCHED PAPER TAPES		
59310-60020		BCS Bus I/O Card Driver, non DMA (D.37A)
59310-60021		BCS Bus I/O Card Driver, DMA (D.37B)
59310-60050		BCS Bus Utility Library (BLIB)
59310-60010		Bus I/O Card Diagnostic
BCS BUS I/O CARD, DRIVER, NON-DMA VERSION (D.37A)		
PART NO.	**PARTS**	**FORM**
59310-60020	1 of 1	Binary punched paper tape
59310-80020	1 of 1	Source punched paper tape
59310-90020	1 of 1	Printed Listing
BCS BUS I/O CARD DRIVER, DMA VERSION (D.37B)		
59310-60021	1 of 1	Binary punched paper tape
59310-80020	1 of 1	Source punched paper tape
59310-90021	1 of 1	Printed Listing
BCS BUS UTILITY LIBRARY (BLIB)		
59310-60050	1 of 1	Binary punched paper tape
		Source punched paper tape, 7 boxes
59310-80051	1 of 7	(Lib Header)
59310-80052	2 of 7	(REMOT)
59310-80053	3 of 7	(LOCL)
59310-80054	4 of 7	(DEVCL)
59310-80055	5 of 7	(CMD)
59310-80056	6 of 7	(READB)
59310-80057	7 of 7	(CIOC)
59310-90051		Printed Listing, 6 parts
59310-90052		
59310-90053		
59310-90054		
59310-90055		
59310-90056		
59310-90057		
BUS I/O CARD DIAGNOSTIC		
59310-60010	1 of 1	Absolute punched paper tape
59310-60011	1 of 4	(Relocatable)
59310-60012	2 of 4	
59310-60013	3 of 4	Binary punched paper tape, 4 boxes
59310-60014	4 of 4	
		Source punched paper tape, 4 boxes
59310-80011	1 of 4	(BICD)
59310-80012	2 of 4	(BDUS)
59310-80013	3 of 4	(BDTS)
59310-80014	4 of 4	(EQTSC)
59310-80011		Printed Listing, 4 parts
59310-80012		
59310-80013		
59310-80014		

1-21. ADDRESSING-TALKING-LISTENING-HANDSHAKING

1-22. A technique of addressing is used to determine which instrument is to "talk" and those instruments that are to "listen". Data is sent from one instrument to another one character (byte) at a time using an interlocked "Handshake" technique. This technique assures that the sender does not remove data before the receiver has finished using the data. It also insures that data is not lost when instruments having inherently different speeds communicate on the same bus.

1-23. FUNCTIONS OF INSTRUMENTS ON THE BUS

1-24. Instruments connected to the bus may function in one or more of the following ways: (They function only after being addressed.)

TALKER — Any instrument that is capable of sending or transmitting information on the bus. There can be ONLY ONE TALKER at a time on the bus.

LISTENER — Any instrument that is capable of receiving or accepting information on the bus is a listener. There may be up to 14 listeners at the same time on the bus.

TALKER-LISTENER — An instrument has the capability of both sending and receiving information on the bus as defined above is both a talker and a listener. For example: a counter is a talker when sending data to a recorder and it is a listener when it is being programmed.

CONTROLLER — Any device that has been programmed to have the responsibility of managing the flow of information between instruments connected to the bus is a controller. It is capable of addressing one of the instruments as a TALKER and one or more as a LISTENER. It is a TALKER and may be a LISTENER. The HP interface bus permits a system to have more than one controller, but only ONE may be active at any time.

SYSTEM-CONTROLLER — The system designer must designate one instrument as the System Controller at the time the system is configured. This instrument performs all the functions of a Controller plus it has the ability to gain absolute control of the Bus.

1-25. HP-IB BUS LINES

1-26. Sixteen of the twenty-four bus conductors are signal lines, one is ground, one is the cable shield and the remaining six are twisted pair commons for six of the signal lines.

1-27. All sixteen bus lines have been given names and mnemonic acronyms that describe the message being carried on that line. There are three types of lines: Data (8), Transfer (handshake) (3), and Control (management) (5).

Note

All instruments connected to the bus, including the controller, must obey these descriptions.

1-28. CONTROL LINES

1-29. The five control lines are used to manage the flow of information over the data and transfer lines. They communicate control and status information between the active controller and instruments connected to the bus. All instruments MUST use ATN and IFC. An instrument may or may not use REN, SRQ and EOI.

1-30. ATN (Attention) is driven by the active controller to place the bus in either the ADDRESS (Low) or DATA (High) mode. ALL other instruments MUST monitor ATN at all times.

Note

ATN was formerly Multiple Response Enable (MRE).

1-31. When the Controller sets ATN to its low state, the bus is in the Command Mode. The primary purpose of the Command Mode is to permit the Controller to send commands or address those instruments that are to communicate when the bus is placed in the Data Mode. Also, the Controller may send Universal Commands while the bus is in the Command Mode.

1-32. When the controller puts ATN to its high state, the bus is in DATA MODE. The instrument that was addressed to TALK and those that were addressed to LISTEN will now communicate on the Data Lines.

1-33. ATN may be set low or high at any time by the Controller, however, it is usually changed at the end of a transfer (handshake) cycle so that data information is not lost. Timing of the transfer lines with respect to ATN is given below under Transfer Lines.

1-34. IFC (Interface Clear) is used by the System Controller to initialize the bus. Only the System Controller can drive IFC and it MUST be monitored by ALL other instruments. When the System Controller sets IFC low for at least 100 μsec: all talkers and listeners are stopped, serial poll mode is disabled, and control is returned to the bus controller. When IFC is high it has no effect on the bus operation. The System Controller may set IFC low at any time.

Note

IFC was formerly Bus Clear (BCL) and End Output (EOP).

1-35. REN (Remote Enable) is driven by the System Controller and is one of the conditions for operating instruments under Remote Control. Only instruments capable of Remote operation use REN and they monitor it at all times. Instruments that do not use REN terminate the line in a resistor load. The System Controller may change the state of REN at any time.

1-36. SRQ (Service Request) is driven to its low state by an instrument to indicate that it wants the attention of the controller. SRQ may be set low by an instrument at any time except when IFC is in the low state. Only the Controller senses SRQ. Some instruments do not use SRQ but terminate it in a resistor load.

1-37. EOI (End or Identify) may be used to indicate the end of an instruments character string. When the bus is in the Data Mode (ATN is high), the addressed Talker may indicate the end of its data setting EOI low at the same time it places the last byte on the Data Lines.

1-38. DATA LINES (DIO1-8)

1-39. The data lines are used to communicate all data including input, output and program codes, addresses control and status information between instruments connected to the bus. These data are passed one character (byte) at a time (i.e., byte serial and bit parallel) under control of the Transfer Lines. In most instruments these data are based on the 7-bit ASCII code set. Unused data lines terminate in a resistor load.

1-40. TRANSFER LINES

1-41. The three transfer (handshake) lines are used to execute the transfer of each byte of information on the data lines. All instruments use these lines and employ an interlocked "handshake" technique to pass information. This allows asynchronous data transfer without timing restrictions being placed on any instrument connected to the bus. Transfer of each byte is accomplished at the speed of the slowest instrument. The three transfer lines are: NRFD, NDAC, and DAV.

1-42. NRFD (Not Ready for Data) is the transfer (handshake) line that indicates all Listeners are ready to accept information on the data lines. NRFD is driven by all Listeners: all instruments when ATN is low and driven only by those instruments addressed to listen when ATN is high. It is sensed by Talkers: the controller when ATN is low, and the instrument addressed to talk when ATN is high.

1-43. When NRFD is high, all listeners are unconditionally ready for data. The Talker may, at its own time, put a byte of information on the data lines and set DAV low. When NRFD is low, one or more listeners is not ready for data.

1-44. When the controller sets ATN low, all instruments must set NRFD to its high state within 200 nanoseconds, i.e., if an instrument is "Ready for Data" it places NRFD to its high state and if it is "Not Ready for Data" it sets NRFD to its low state. When the controller sets ATN high, all instruments that have not been addressed to listen will not drive NRFD, those addressed to Listen will set NRFD to its high state within 200 ns.

1-45. A listener must not set NRFD low until it senses DAV is low. It may do so before or at the same time that it sets NDAC high. It must not return NRFD high until it senses DAV is high and may do so after, or at the same time that it sets NDAC low.

1-46. NDAC (Not Data Accepted) is the transfer line that indicates the acceptance of information on the data lines.

1-47. NDAC is driven by all Listeners. That is, all instruments when ATN is low and only those instruments addressed to Listen when ATN is high. It is sensed by Talker and the controller when ATN is low and by the instrument addressed to talk when ATN is high.

1-48. When NDAC is high, all Listeners have unconditionally accepted the byte of information that is on the data lines and no longer need it. The Talker may, at its own time set DAV high, remove that byte of information and continue. When NDAC is low, one or more Listeners has not accepted the information on the data lines.

1-49. When the controller sets ATN low, each instrument must set NDAC to its high state within 200 nanoseconds. When the controller sets ATN high, the instruments that have not been addressed to listen will not drive NDAC, those addressed to Listen will set NDAC to its true state within 200 nanoseconds.

1-50. A Listener must not set NDAC low until it senses DAV is high. It may do so before or at the same time that it sets NRFD high. It must not return NDAC high until it senses DAV is low and it may do so after or at the same time that it sets NRFD low.

1-51. DAV (Data Valid) is the transfer line that indicates the validity of information on the data lines.

1-52. DAV is driven by Talkers: the controller when ATN is low and by the instrument addressed to talk when ATN is high. It is sensed by Listeners and by all instruments if ATN is low and by those instruments addressed to listen when ATN is high.

Table 1-4. Relation of ATN and Transfer (Handshake) Lines (NRFD, NDAC and DAV)

Mode	ATN	NRFD		NDAC		DAV	
		LOW	HIGH	LOW	HIGH	LOW	HIGH
ADDRESS	LOW	One or more units not ready for data	All units ready for data	One or more units have not accepted data	All units have accepted data	Controller has valid data on DIO lines	Controllers data is not valid
		1. Driven by all units except controller 2. Sensed by controller 3. All units set NRFD and NDAC to valid state within 200 nanoseconds after ATN goes LOW				1. Driven by controller 2. Sensed by listeners 3. See DAV above for timing	
DATA	HIGH	One or more listeners not ready for data	All addressed listeners ready for data	One or more listeners have not accepted data	All addressed listeners have accepted the data	The addressed talker has valid data on lines	The addressed talker data is not valid
		1. Driven by all units addressed to listen. 2. Sensed by the unit addressed to talk. 3. All units not addressed will not drive. 4. All addressed listeners set both NRFD and NDAC to valid within 200 nanoseconds after ATN goes HIGH.				1. Driven by the instruments addressed to TALK 2. Sensed by ALL instruments addressed to LISTEN 3. See DAV above for timing.	

Table 1-5. Summary of Bus Timing

IFC INTERFACE CLEAR	The System Controller must set IFC low for at least 100 microseconds to clear the bus.
TRANSFER LINES WITH RESPECT TO ATN	When sending an Address or a Universal Command the controller may set DAV low only after sensing that NRFD is high, and ATN has been low for at least once microsecond. When a controller changes ATN from its high to the low state or from low to high, all Listeners (all instruments when ATN is low and those addressed to Listen when ATN is high) put both NRFD and NDAC to their high state in less than 200 nanoseconds.
TRANSFER LINES WITH RESPECT TO THE DATA	After changing the information on one or more Data Lines, the TALKER (the Controller when MRE is low or the instrument addressed to TALK when MRE is high) MUST wait before setting DAV low. It waits 2 ±sec if designed with open-collector circuits and 0.5 microsecond if designed with tri-state integrated circuits.

1-53. When DAV is low, the states of data lines DI01 through DI07 are unconditionally valid and may be accepted by all listeners at their own time. DAV can only be driven low if NRFD and IFC are high. When DAV is high, the information on the data lines is not valid. DAV cannot be set high unless NDAC is high and NRFD is low.

1-54. The Talker has the responsibility of allowing enough time for cable rise time and ringing. It does this with DAV. The controller after placing the bus in the ADDRESS MODE (sets ATN low) must wait at least one microsecond before setting DAV low. Of course it must not do so unless NRFD is high. In either the ADDRESS or DATA MODE, a Talker designed with open-collector circuits must not set DAV low for at least two microseconds after placing valid data at its output connector. Those designed with tri-state integrated circuits must wait at least 500 nanoseconds.

1-55. Data Transfer

1-56. Transfer of data on the bus is asynchronous. It places no restrictions on the data rates of instruments connected to the bus. The timing and levels required to transfer a byte of information on the data lines are shown in Figure 1-2. Transfer is under the control of three lines DAV, NRFD and NDAC. The Talker (sender of data) drives the Data Lines and DAV (Data Valid) and the Listeners (acceptors of data) drive both NRFD (Not Ready for Data) and NDAC (Not Data Accepted).

1-57. The transfer of a byte or data is initiated by all Listeners signifying they are ready for data by setting NRFD high. When the TALKER recognizes NRFD is high and has placed valid data on the data lines it sets DAV low. When the Listener senses that DAV is low and have finished using the data, they set NDAC high. Notice that the assertive or action state of both NRFD and NDAC is high. Since all instruments on the bus have their corresponding lines connected together (e.g. NRFD), all Listeners must be in a high state before that line goes high. This wire-AND situation allows a Talker to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

1-58. Figure 1-2 also shows the timing of the transition to the non-assertive state of these lines. A Listener may set NRFD low as soon it recognizes that DAV has been set low and must do so before or at the same time it puts NDAC high. The Talker may return DAV to its high state after it detects that NDAC is high. A Listener may set NDAC low as soon as it recognizes that DAV is high and must do so before or at the same time it places NRFD in its high state.

1-59. HP-IB ELECTRICAL CHARACTERISTICS

1-60. All 16 bus lines are designed to be compatible with TTL or DTL integrated circuits. Because wire-ANDING is used on some lines the line drivers must be either open collector or tri-state. Each line in every instrument is terminated in a resistor divider consisting of a 3KΩ connected to 5V and a 6.2KΩ connected to ground. Typically receivers are hex inverters and the drivers are open collector NAND gates. These may be put into four groups:

a. Receivers only: They require -3.2 mA max. at 0.4V drive (A Standard Load).

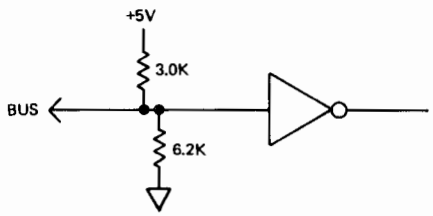
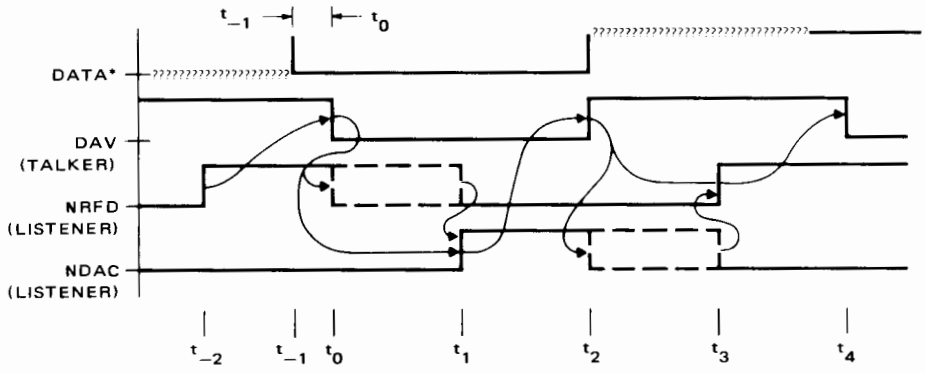


Figure 1-2. Transfer Timing

SEQUENTIAL REQUIREMENTS OF THE THREE WIRE TRANSFER



EVENTS

t_{-2} : Listener becomes ready to accept data.

t_{-1} : Talker has put data on the lines.

t_0 : Indicates data is valid.

t_1 : Listener has accepted the data and no longer requires it held valid.

t_2 : Talker indicates the data is no longer valid and may change it.

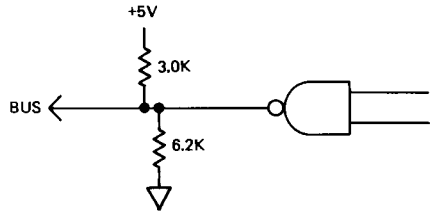
t_3 : Listener indicates it is ready for new data.

t_4 : A new cycle begins (equivalent to t_0).

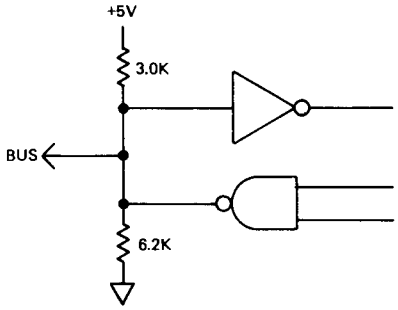
t_{-1} to t_0 : Time that data is put on lines before DAV is set low.

*A composite of the DIO1 through DIO7 lines for illustrative purposes.
(The curved lines indicate interlocked signal sequence.)

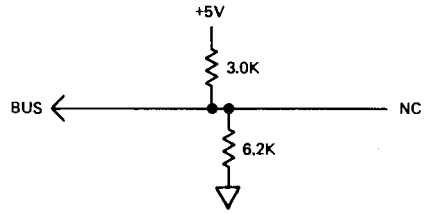
b. Senders only: They are capable of sinking 45 mA at +0.4V (A Standard Driver).



c. Bi-directional Lines: They are a combination of the above, i.e., when a TALKER, capable of sinking 45 mA at 0.4V. When a LISTENER, requires -3.2 mA at 0.4V to drive. Examples are the Data Lines ((DIO1 through DIO7 for instruments using the ASCII code) and the handshake lines (NRFD, NDAC and DAV).



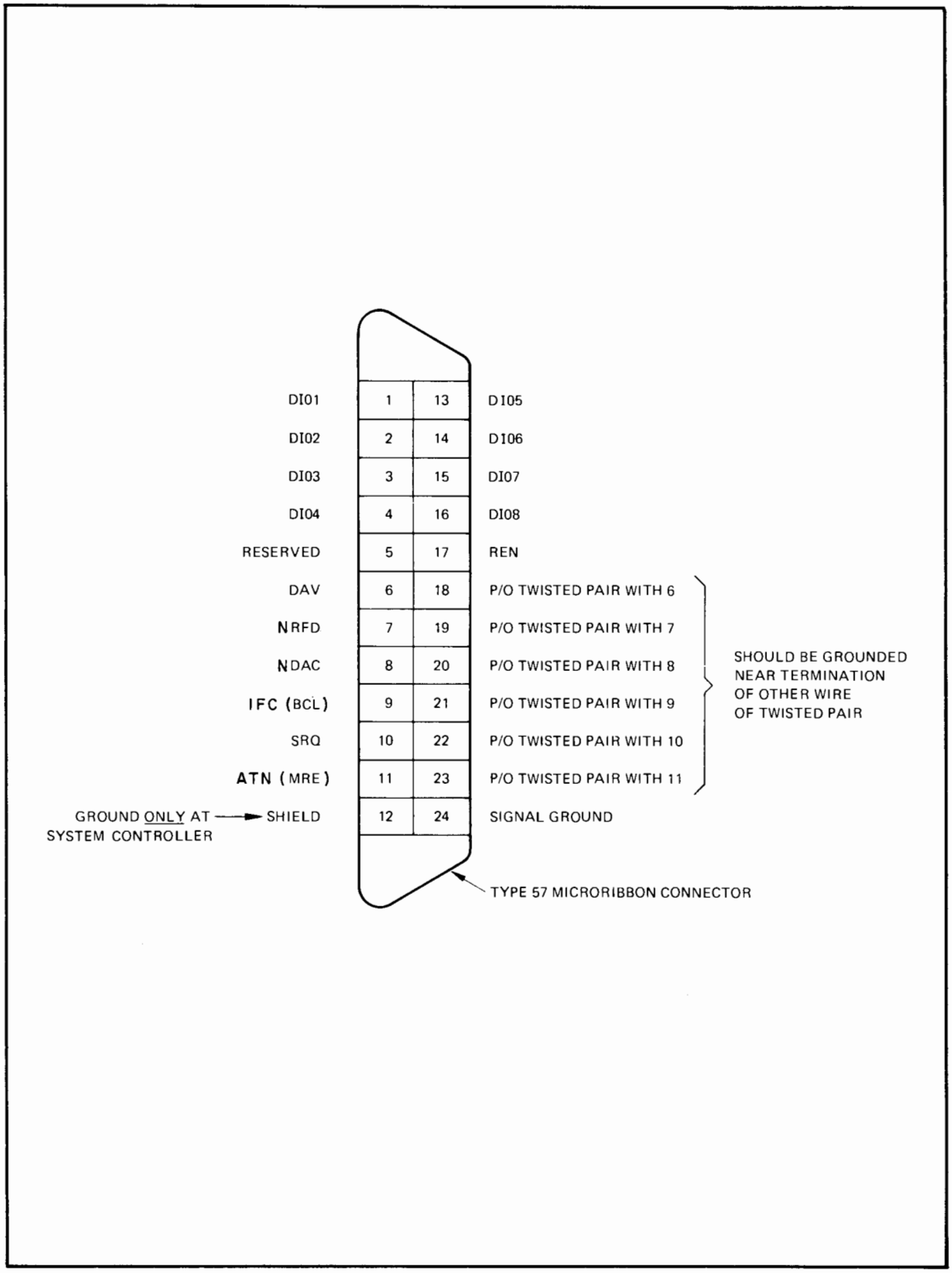
d. Lines not used by an instrument are connected to a 3.0KΩ resistor to +5V, and 6.2KΩ resistor to signal ground (a Standard Termination). For example, DIO8 for instruments using the ASCII code or those not using REN, SRQ or EOI.



1-61. HP-IB PHYSICAL CHARACTERISTICS

1-62. Bus cables are available for connecting instruments into a system. These have one overall shield to reduce susceptibility to external noise. The cables use a mixture of individual wires and twisted pairs to reduce crosstalk. Both ends are identical. They are terminated in two 24-pin piggy back connectors; one male and one female. Pin connections of these connectors are shown in Figure 1-3.

Figure 1-3. Pin Connections of the HP-IB Cables



SECTION II

INSTALLATION

2-1. INTRODUCTION

2-2. This section contains information for unpacking, inspection, repacking, storage, and installation. Information on the performance check and interconnecting cables is also included.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, ask that the carrier's agent be present when the instrument is unpacked. Inspect the instrument for damage. If the instrument is damaged or fails to meet electrical specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Retain the shipping carton and padding material for the carrier's inspection. The sales and service office will arrange for the repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. STORAGE AND SHIPMENT

2-6. To protect the 59310A Bus Input/Output card during storage or shipment, good commercial packing methods should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack an instrument.

Note

Before returning an instrument to Hewlett-Packard, contact the nearest Hewlett-Packard Sales and Service Office for instructions.

2-7. Environment

2-8. Conditions during storage and shipment should normally be limited as follows:

a. Maximum altitude: 25,000 feet.

b. Minimum temperature: -40°F (-40°C).

c. Maximum temperature: +167°F(+75°C).

2-9. INSTALLATION

2-10. The following steps are suggested for preparing and installing the 59310A Bus Input/Output card into the computer:

a. Determine that the computer has sufficient power to support the addition of the Bus Input/Output card. (Refer to paragraph 2-12.)

b. Set up the hardwired options on the card using switches or jumpers for desired system functions. (Refer to paragraph 2-14.)

c. Install printed circuit board assembly in computer. (Refer to paragraph 2-25.)

d. Verify proper operation using the Diagnostic Program. (Refer to paragraph 2-28.)

e. Interconnect system observing cabling restrictions. (Refer to paragraph 2-33.)

2-11. Power Requirements

2-12. Before installing the 59310A Bus Input/Output card in the computer, determine that the additional power consumed by the 59310A card will not overload the computer power supply. The power required by the 59310A card is as follows:

SUPPLY VOLTAGE	MAX. CURRENT REQUIRED
+30	None
+12	None
+5*	3.0 A
-2	100 mA
-12	None
*Nominal value of voltage can vary between 4.5 to 5.0 volts depending on the computer model.	

2-13. Programming of Hardwired Options

2-14. Before installing the 59310A I/O card in the computer, several "jumper options" must be programmed for the desired user application and system function. One of two methods may be used to program these functions. One is by use of DIP switches; the other by jumper plugs. The DIP switches allow easy changing of the card's function to accommodate changing system requirements. The jumper plugs provide a fixed configuration to avoid accidental changing of operating modes.

2-15. The hardwired programmable functions of the 59310A Bus I/O Card are as follows:

a. BUS ADDRESS 5 4 3 2 1 — Defines the lower five bits of the Talk and Listen addresses that the card will recognize as its own. The value set on the switches must be between **ØØ ØØØ** ($Ø_8$) and 11 **11Ø** (36_8). Address 37_8 is reserved for the Unlisten and Untalk addresses. *(Jumper installed in plug programs a Ø.)*

b. REN — When ON, enables the card to drive the BUS signal line REN. When OFF, disables the card from driving the BUS signal line REN. *(Jumper installed in plug programs OFF.)*

c. EOP (IFC is the latest abbreviation) — When the switch is set to ON, enables the I/O card to drive the BUS signal line IFC (EOP). When the switch is set to OFF, disables the I/O card from driving the BUS signal line IFC. *(Jumper installed in plug programs OFF.)*

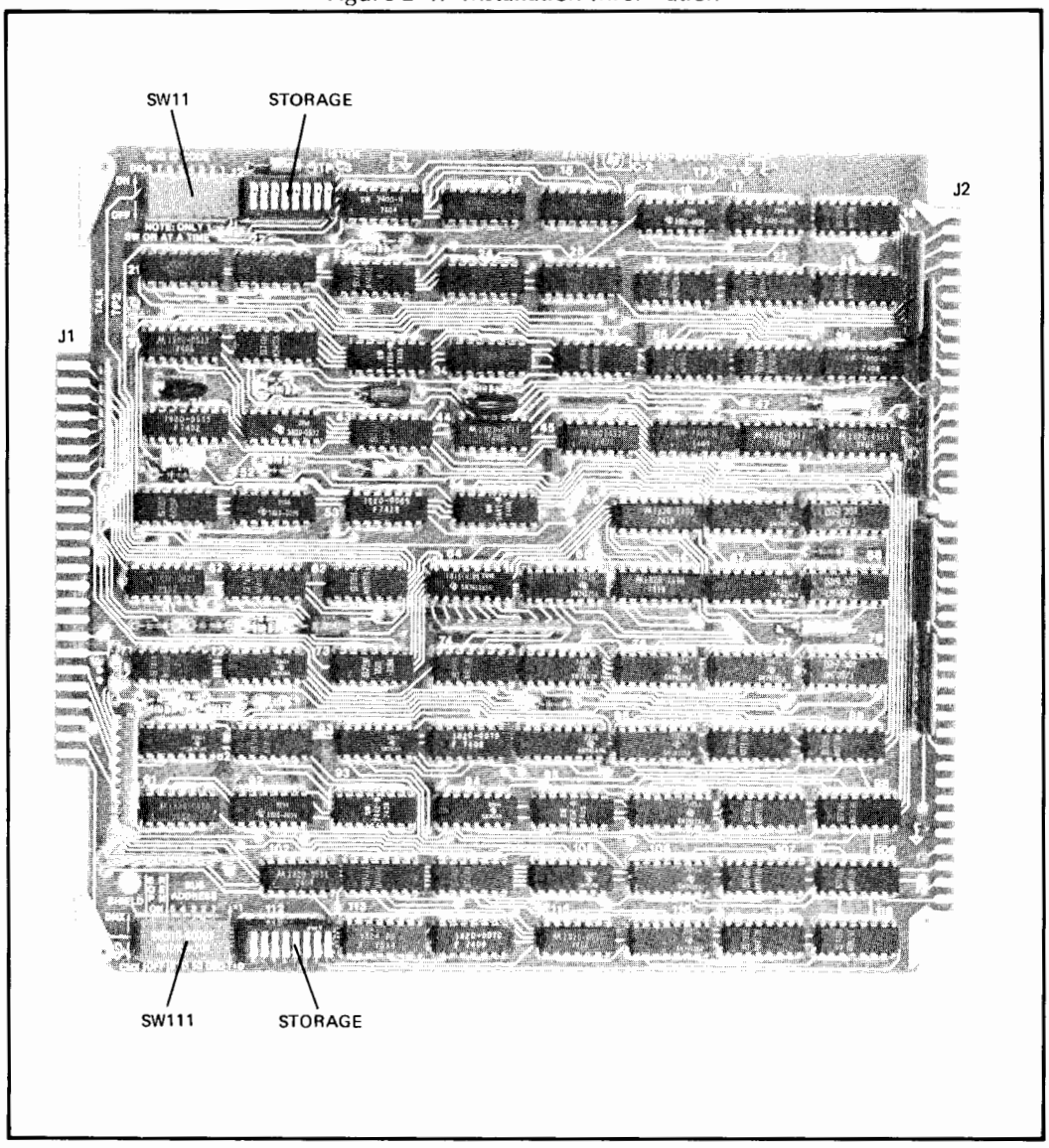
d. SHIELD — When the switch is set to CNX, connects the shield in the bus cable to the logic circuit common. When the switch is set to DNX, disconnects the shield in the bus cable from the I/O cards common. (Unless some other device connects the shield it will remain disconnected.) *(Jumper installed in plug programs a CNX.)*

e. SRQ ID CODE — Defines the code that the 59310A Bus I/O card will send in response to a Parallel Poll. Setting the switch to ON (Jumper installed in plug) will cause the card to use the DIO signal line specified to be used. Note only *one* switch (or jumper installed in plug) may be on at one time.

2-16. Installation of DIP Switches or Jumper Plugs

2-17. There are four locations on the 59310A Bus I/O card (59310-60001) where the DIP switches and jumper plugs may be installed. Two of the locations are active and the other two are storage locations for the unused DIP switches or plugs. The positions are located in the upper left and lower left of the printed circuit board. The active locations are the left hand side of the top and bottom. See Figure 2-1.

Figure 2-1. Installation Information



2-18. The upper left hand location (position 11) defines the identification code to be used by the card in response to a parallel poll. The upper position just to the right of this (position 12) is the storage location for the unused DIP switch or plug.

2-19. The lower left hand location (position 111) defines the BUS ADDRESS, REN and IFC (EOP) enables, and the SHIELD connection. The lower position just to the right of this (position 112), is the storage location for the unused DIP switch or plug.

2-20. If plugs are selected for the hardwired programming, first wire the desired functions as described in paragraph 2-15. Then install the plug in the active location(s) and the DIP switch in the storage location(s). If the DIP switches are selected, first install them in the active location(s) and the plug in the storage location(s). Then select the switch positions of each DIP switch according to the functions desired as described in paragraph 2-15.

2-21. If the DIP switches are installed in the active locations, the arrows associated with the labeling on the printed circuit board indicate which side of the rocker is to be depressed to cause the indicated effect. If plugs are installed, the arrows do not apply.

CAUTION

When installing the DIP switches and plugs in the printed circuit board, be certain that all of the pins are correctly aligned with the sockets before applying force to insert them. Failure to observe this caution may result in the pin being bent or broken off.

2-22. When removing the DIP switch or plug from the printed circuit board, be certain that the extractive force is applied evenly to both ends of the DIP switch or plug. (It is recommended that an IC extractor be used.) Failure to do this may cause one end to be extracted before the other, causing the pins on one end to bend or break off.

2-23. Standard Mode of Operation

2-24. The normal use of the 59310A card is the System Controller function. This requires the switches to be set as follows:

a.	BUS ADDRESS:	5 4 3 2 1 1 Ø Ø Ø Ø (20_8)
b.	REN:	to ON
c.	IFC (was EOP & BCL)	to ON
d.	SHIELD:	to CNX
e.	SRQ ID CODE:	to all OFF

NOTE

A standard DIP plug is supplied (59310-60003) with jumper wires installed to provide the above functions.

NOTE

The BUS ADDRESS may be set to any value between ØØ ØØØ ($Ø_8$) and 11 11Ø (36_8). The value 20 is the preferred address for the computer when it is used as the system controller.

2-25. Installing 59310A Printed Circuit Board in the Computer

2-26. After having selected hardwired options, the 59310A BUS I/O card may then be installed in the computer as follows:

a. Set the computer's power to OFF.

b. Insert the 59310A BUS I/O card into one of the available I/O slots of the computer. (Since the location and position will vary depending on the model of computer, refer to the computer manual for details.)

2-27. PERFORMANCE CHECK

2-28. To verify proper operation of the BUS I/O CARD, run the BUS I/O CARD DIAGNOSTIC program (Part No. 59310-60010). Information regarding the operation and use of the diagnostic is contained in a separate DIAGNOSTIC PROGRAM PROCEDURE manual entitled BUS INPUT/OUTPUT CARD DIAGNOSTIC (59310A) (Part No. 59310-90010).

2-29. INTERCONNECTING CABLES

2-30. Supplied with the 59310A Kit is a 3 meter cable (59310-60002) which contains a printed circuit board edge connector at one end and a piggy-back connector at the other end. The printed circuit board edge connector end is connected to the BUS I/O card (59310-60001) J2. The end of the connector which does not have the ocable protruding must be installed so it is closest to the extractor labeled "BUS INPUT/OUTPUT".

2-31. The piggy-back connector end is connected to the peripheral device. Other devices may be added to the bus by use of the standard bus cable (not supplied), listed in Table 2-1.

Table 2-1. Bus Cables

LENGTH	ACCESSORY NUMBER
1 meter	10631A
2 meters	10631B
3 meters	10631C

2-32. Cabling Length Restrictions

2-33. In order to ensure proper operation of the bus, two rules must be observed regarding the total *length* of bus cables when they are connected together. These are:

a. The total length of cable permitted to be used with one BUS I/O CARD must be less than or equal to two meters times the number of devices connected together. (The Bus I/O card is counted as one device.)

b. The total maximum length of cable must not exceed 20 meters.

2-34. Rule (a.) implies that there may be up to 4 meters of cable between the first two devices (2 units x 2 m./device = 4 m.). Additional units may be added using 2-meter cables up to a total of 10 units (10 units x 2 m./device = 18 meters) using one 4-meter and six 2-meter cables (4 + (8 x 2) = 20). If more than ten devices are to be connected together, cables shorter than two meters must be used between some of the devices. For example, 15 devices can be connected together using one 4-meter and thirteen one-meter cables 4 + (13 x 4) = 17. Other combinations may be used as long as both of the requirements of rule (a.) and (b.) are met. In making calculations, remember to count the BUS I/O Card as one device.

2-35. Cabling Configurations

2-36. There are no restrictions to the ways cables may be connected together. However, it is recommended that no more than 3 to 4 piggy-back connectors be stacked together on one device. The resulting structure can exert great force on the panels of the device where the connector is mounted and could cause mechanical damage.

2-37. The configuration may be linear (all cables connected end to end) or in a star (all cables branching out from a central point) or any combination of the above.

SECTION III

OPERATION AND PROGRAMMING

3-1. INTRODUCTION

3-2. This section explains the operation and programming of the 59310A Bus I/O Card.

3-3. CHANGES* IN HP INTERFACE (HP-IB) BUS LINES

3-4. The HP-IB has 24 lines with 16 signals. The bus lines and changes are listed below:

Abbreviation	Name	Change or Previous Name	Connector Pin
DIO1	Data Input Output 1 thru 8		1
DIO2			2
DIO3			3
DIO4			4
DIO5			13
DIO6			14
DIO7			15
DIO8			16
DAV	Data Valid		6
*NRFD	Ready for Data	(N-prefix added)	7
*NDAC	Data Accepted	(N-prefix added)	8
*IFC	Interface Clear	(Was BCL and EOP)	9
SRQ	Service Request		10
*ATN	Attention	(Was MRE)	11
EOI	End or Identify		5
REN	Remote Enable		17
	Common (Ground)		18-24

NOTE: The starred (*) line functions have not changed with name changes. References to any version of a line name is equivalent to any other version. That is: EOP = BCL = IFC, and ATN = MRE.

3-5. BUS FUNCTIONS AVAILABLE TO THE COMPUTER WITH THE 59310A

3-6. Several functions on the HP-IB are usable by the computer when the 59310A is installed. These functions are described in the following paragraphs.

3-7. Listen Functions

3-8. The computer can input data from the Bus when addressed. The Listen Functions include the following capabilities:

Addressable Listen: The 59310A becomes addressed to Listen when a Controller sends its Listen Address.

Programmable Listen: The 59310A becomes addressed to Listen by the computer via software control.

End of Record Detection: An End of Record (EOR) Flag will be set if the card is addressed to Listen and is receiving data and the EOI line goes Low. In addition, if enabled by software control, an ASCII Line Feed (012) on the data lines will also set the EOR Flag. The EOR Flag can be tested by software or used to generate an interrupt.

Service Requesting: If enabled by software control and not addressed to Listen and ready to receive data, the card will generate a Service Request (SRQ).

3-9. Talk Functions

3-10. The computer can output data to the Bus when addressed. The Talk Functions include the following capabilities:

Addressable Talk: The 59310A becomes addressed to Talk when a Controller Sends its Talk Address.

Programmable Talk: The 59310A becomes addressed to Talk by the computer via software control.

End of Record Signaling: The computer can set EOI Low with the last byte or after the last byte indicating that End of Record has occurred. If enabled by program control, EOI will be set Low if an ASCII Line Feed (012_8) is output.

Service Requesting: If enabled by software control and not addressed to talk and ready to send data, the Bus I/O Card will generate a Service Request (SRQ).

Serial Poll Identification: Allows the computer to respond to a Controller making a Serial Poll. The Controller sending the Serial Poll Enable Command will set the Serial Poll Mode Flag which may be tested via software or used to cause an interrupt. The computer may then send its Status Byte to the Controller when addressed to Talk.

3-11. Controller Functions

3-12. The computer can manage the activities on the Bus by sending Addresses and Universal Commands. The computer can only perform this role if its Active status is set (A Controller becomes "Active" if designated by another Controller or if a System Controller and it activates itself.) The Controller Functions include the following capabilities:

Addressing and Universal Commands: The computer sets ATN Low via program control and sends Address or Commands to devices in the Bus.

Service Request Processing: The computer can monitor for the Service Request line (SRQ) or enable it to cause an interrupt to determine if a device on the Bus is requesting service.

Serial Polling: Allows the computer to determine the device(s) that have caused a Service Request. A Serial Poll is executed via software by sending Universal Commands and Addresses and using the Listen Mode.

3-13. System Controller Functions

3-14. The card performs all of the functions of a Controller including the following additional capabilities:

Interface Clear: Allows the computer to utilize the Bus or regain control by setting the Bus signal line Interface Clear (IFC) Low. (Note: IFC formerly was called BCL and EOP.)

Remote Enable Control: Allows the computer to enable programmable devices to switch from local to remote control by setting the bus signal line Remote Enable (REN) Low.

Automatic Activation of Controller Functions: The Bus I/O Card automatically becomes the Active Controller when powered up or if its sets IFC Low.

3-15. COMMUNICATION FORMS BETWEEN THE I/O CARD AND COMPUTER

3-16. The information that can be transferred between the computer and the 59310A Bus I/O card under program control takes five forms. These include four data types which can be passed between the A/B registers and the I/O card's registers. They are: (1) the Control Word, which establishes the I/O card's operating mode, (2) the Status Word which provides information about the condition of the card and the Bus, (3) Output Data, which is transmitted from the computer to the Bus and (4) Input Data which is received from the Bus. Input Data and Output Data may also be transferred under Direct Memory Access (DMA) control. These are discussed in detail in paragraphs 3-43 to 3-75.

3-17. The fifth type of communication from the I/O card is the flags. There are eight flags, of which seven can be tested by program instructions and one is used with DMA. Operation of the Flags is discussed in paragraphs 3-76 to 3-103. Operations under program control are controlled by use of the various computer I/O instructions.

3-18. CONTROL WORD

3-19. Description

3-20. The Control Word is a 16 bit word (see Figure 3-1) which is output to the I/O Card under program control. It is divided into three parts referred to as Group 1, 2 and 3. Group 2 is further divided into two sub-groups, Group 2A and 2B. The effect on the I/O card of each group is independent from the other groups. Each group may be used individually or in combinations.

3-21. Functions and Modes

3-22. The Control Word is used to select the operating modes and Bus functions that the Bus I/O Card is to perform.

3-23. The operating modes controllable with the Control Word are:

1. Flag selection for interrupt or by testing with the SFS or SFC instructions
2. Packaging enable/disable
3. DMA input or output flag selection
4. Service Request enable/disable
5. ASCII Mode enable/disable
6. Forced input of data (without a handshake cycle)

7. Initialize flags

3-24. The Bus functions controllable with the Control Word are:

1. Remote/Local
2. Active/Inactive Controller Function
3. Enable talker function/disable
4. Enable listener function/disable
5. Controller functions
   a. Data Mode/Command Mode Select
   b. Parallel Poll

3-25. Outputting the Control Word

3-26. The CONTROL WORD is output to BUS I/O card by the following sequence of instructions:

```
              .
              .
              .
              LDA     CTLWD
              STF     SC
              OTA     SC
              .
              .
              .
CTLWD         OCT     <value>
SC            EQU     <select code of BUS I/O card>
```

3-27. The value of the Control Word is a function of the desired operating mode of the I/O card and Bus functions.

3-28. Control Word Group 1 Coding

3-29. Group 1 of the Control Word consists of seven coded commands using bits Ø thru 2. The commands of group 1 are used to control the IFC (BCL-EOP) One-Shot, Remote Enable Flip-Flop, Active Flip-Flop, to force an input cycle and initialize certain I/O Control and Flag Flip-Fops. The coding and function of each of the commands is as follows:

B I T 2	B I T 1	B I T Ø	FUNCTION/OPERATION
Ø	Ø	Ø	NO OPERATION (NOP) Does not affect the I/O Card or the Bus.

Control Word Group 1 Coding (Continued)

B I T 2		B I T Ø	FUNCTION/OPERATION
Ø	Ø	1	INTERFACE CLEAR (IFC) COMMAND
			Causes the IFC one-shot to be triggered. This sets the Bus signal line IFC (Interface Clear) Low for 100 μsec which unaddresses all Talkers and Listeners, clears the Serial Poll Mode and deactivates all other controllers.
Ø	1	Ø	LOCAL COMMAND
			Causes the Remote Enable Flip-Flop to be cleared which causes the Bus signal line Remote Enable (REN) to be set high. This causes all devices, with the possible exception of source devices (i.e., power supplies), to switch to local control, and the local lock out state to be cleared.
Ø	1	1	REMOTE ENABLE COMMAND
			Causes the Remote Enable Flip-Flop to be set which causes the Bus signal line Remote Enable (REN) to be set low. This enables all devices on the Bus to switch to remote control when addressed to Listen to their remote programming codes.
1	Ø	Ø	DEACTIVATE CONTROLLER FUNCTION COMMAND
			Causes the Active Flip-Flop to be cleared. In this state, the I/O Card (and thus the computer) can not perform any of the functions of a Controller.
1	Ø	1	ACTIVATE CONTROLLER FUNCTION COMMAND
			Causes the Active Flip-Flop to be set. Only if the I/O card is in this state may it perform the Bus functions of a Controller.
1	1	Ø	STROBE INPUT DATA COMMAND
			Causes the contents of the Bus Data lines at the time of execution to be strobed into the Input Data Register irrespective of the state of the handshake lines or whether the card is addressed to Listen or not. The Data will go into the upper or lower half of the Input Data Register as a function of the state of Input Byte Counter. The Input Byte Counter will be toggled and the Input Register Loaded FF set if appropriate.
1	1	1	INITIALIZE FLAGS COMMAND

Affects several flags associated with the transfer of data in and out as follows:

1. Causes the Output Word Register Loaded and Output Byte Register Loaded Flip-Flop to be cleared. This initializes the output handshake logic for subsequent output operations and/or terminates an output cycle in progress.

2. Initialized the Output Byte Counter to byte Ø (upper half) so that data output using packing always starts with the upper half word.

3. Causes the DMA Output Request Flip-Flop to be set so that the first DMA Output cycle will be requested when DMA is enabled.

4. Causes the Ready for Data Flip-Flop to be cleared which will set the Bus signal line NRFD (Not Ready for Data) Low if the card is addressed to Listen. This indicates to the Talker device that the card is not able to accept data yet.

3-30. Control Word Group 2 Coding

3-31. Group 2 of the Control Word consists of two sub-groups which control two functions each using bits 3 thru 6. Group 2A is used to control the Controller functions and Group 2B to control the Talker/Listener functions. The two sub-groups may be used independently or in combination. Bits 4 and 5 are used to select Groups 2A and 2B respectively and bits 3 and 4 to control the functions of each sub-group. Group 2 coding and functions are as follows:

B I T 6	5	4	B I T 3	FUNCTION/OPERATION
Ø	Ø	X	X	NO OPERATION (NOP) Does not affect the I/O card or the Bus.
Ø	1	—	—	GROUP 2A FUNCTIONS Accesses ATN (MRE) and EOI FF's.
Ø	1	Ø	Ø	SET DATA MODE Causes the ATN (Attention) and the EOI (End of Identify) Flip-Flops to be cleared which puts the bus into the Data Mode so that the Talker and Listener(s) may transmit data.
Ø	1	Ø	1	SIGNAL END OF RECORD Clears the ATN and sets the EOI Flip-Flops which sets the Bus signal line EOI (End or Identify) Low if addressed to Talk. This indicates that the next byte sent as a Talker is the last in the string.
Ø	1	1	Ø	SET COMMAND MODE Sets the ATN and clears the EOI Flip-Flops which sets the Bus signal line ATN Low and EOI High. This puts the Bus into the Command Mode which enables the computer to send Commands and Addresses.
Ø	1	1	1	PARALLEL POLL COMMAND Sets the ATN and EOI Flip-Flops which sets the Bus signal lines ATN and EOI Low. This initiates a Parallel Poll. Devices so equipped, respond on a preassigned data line.

Control Word Group 2 Coding (Continued)

BIT 6	5	4	BIT 3	FUNCTION/OPERATION
1	Ø	—	—	GROUP 2B FUNCTIONS
				Accesses Talk and Listen Flip-Flops. All Group 2B codes cause the Data Mode to be set simultaneously (i.e., the ATN FF is cleared).
1	Ø	Ø	Ø	DISABLE LISTEN AND DISABLE TALK FUNCTIONS
				Clears both the Talk and Listen Flip-Flops which prevents the I/O card from transmitting or receiving data.
1	Ø	Ø	1	DISABLE LISTEN AND ENABLE TALK FUNCTIONS
				Clears the Listen Flip-Flop and sets the Talk Flip-Flop, thereby enabling the card to send data to the Bus.
1	Ø	1	Ø	ENABLE LISTEN AND DISABLE TALK FUNCTIONS
				Sets the Listen Flip-Flop and clears the Talk Flip-Flop, thereby enabling the card to receive data from the Bus.
1	Ø	1	1	ENABLE LISTEN AND ENABLE TALK
				Sets both the Talk and Listen Flip-Flops, allowing the card to send data to itself. This is generally useful only for diagnostic purposes.
1	1	—	—	COMBINED ACTION OF GROUPS 2A &2B
				Both the functions indicated by bit 3 and 4 in Groups 2A and 2B will be performed.

3-32. Control Word Group 3 Coding

3-33. Group 3 of the Control Word consists of eight mode control functions coded with one bit per function using bits 8 thru 15. Bit 7 enables or disables the effect of the other bits in the group. Group 3 coding and functions are as follows:

Bit 7 — GROUP 3 SELECT

When Bit 7 = 1, enables bits 8 thru 15 to control their specified functions.

When Bit 7 = 0, disables bits 8 thru 15 from having any effect in controlling their designated functions.

Bit 8 — ASCII MODE ENABLE

When Bit 7 = 1, enables the ASCII mode logic (see paragraph 3-122 for details of the operation of the ASCII Mode.)

When Bit 7 = 0, disables the ASCII Mode.

Bit 9	GENERATE SERVICE REQUEST ENABLE When Bit 9 = 1, enables the Bus I/O Card to generate a Service Request (set the Bus signal line SRQ Low) if: 1(a). The Talk Flip-Flop is clear and (b) the Output Byte Register Flip-Flop is set. 2(b). The Listen Flip-Flop is clear and (b) the NRFD Flip-Flop is set. When bit 9 = 0, the Bus I/O card is disabled from driving the SRQ line (it is set to OFF).
Bit 10	DMA FLAG SELECT Selects which flag is to be used to request a DMA cycle. When Bit 10 = 0, the DMA Output Request Flag is selected. When Bit 10 = 1, the Input Register Loaded Flag is selected.
Bit 11	PACKING ENABLE When Bit 11 = 1, enables the packing and unpacking logic for both input and output. When Bit 11 = 0, disables the packing logic.
Bits 12–15	FLAG SOURCE SELECT Selects which flags can be tested by the SFS or SFC instructions or can be used to cause an interrupt.
Bit 12	Enables the End of Record Flag.
Bit 13	Enables the Output Word Register Accepted Flag.
Bit 14	Enables the Input Register Loaded Flag.
Bit 15	If the Active Flip-Flop is set, enables the BUS clear as service Request Flag. If the Active Flip-Flop is clear, enables Serial Poll Mode Flag.

3-34. STATUS WORD

3-35. Description

3-36. The Status Word is a 16 bit word (see Figure 3-2) which is input under program control to obtain information about the operating conditions of the BUS I/O card and the BUS.

3-37. Function

3-38. With the Status Word, the following can be determined:

1. Which one or more of the six flags have occurred (EOR, ORA, IRC, IFC (EOP), SRQ, SPM)*.

*See paragraphs 3-76 to 3-103 for the description of the various flags.

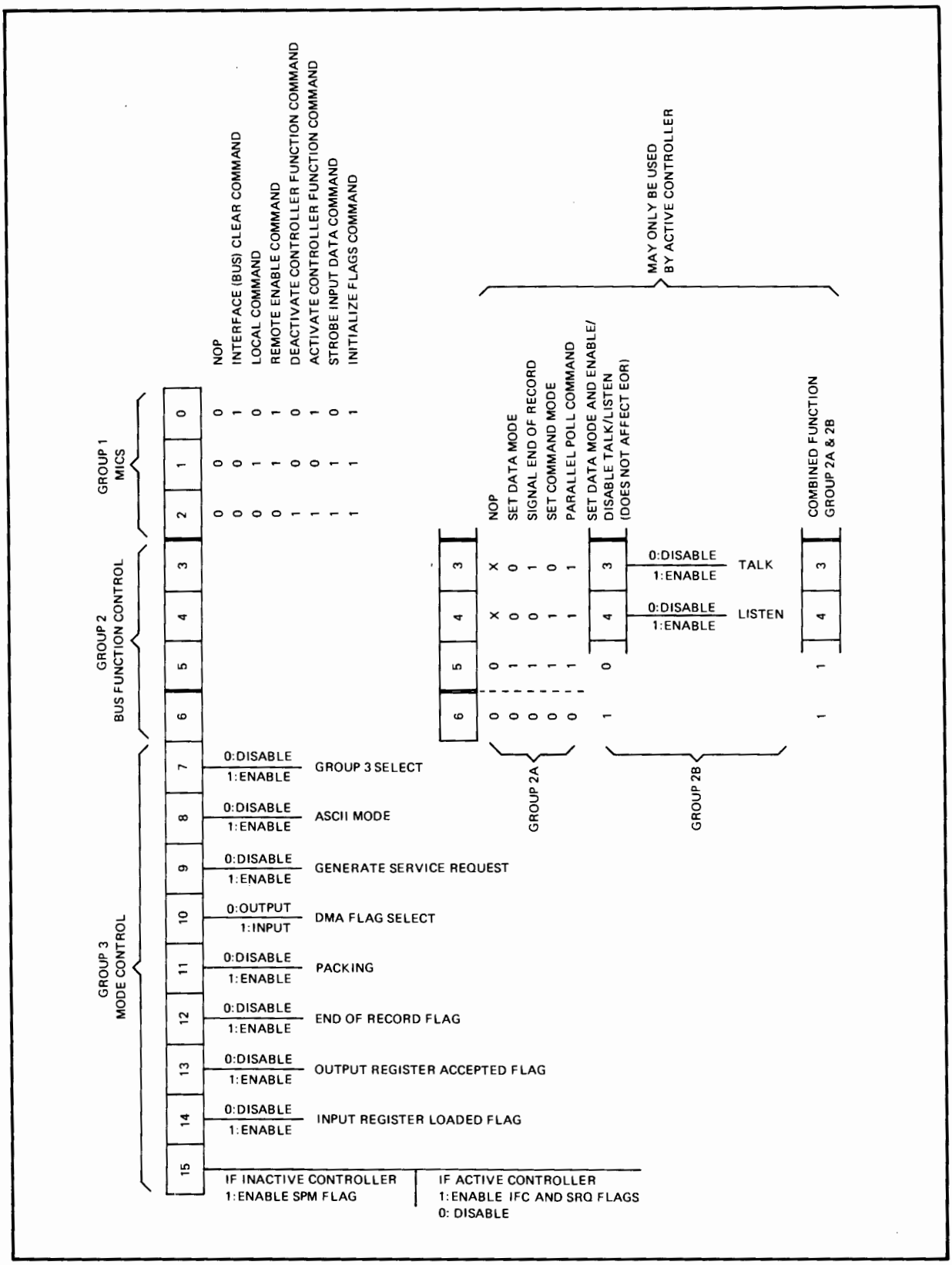


Figure 3-1. Control Word Format

2. The states of five of the BUS signal lines (REN, ATN (MRE), DAV, NRFD and NDAC).

3. Which of the three BUS interface functions the I/O card is currently enabled to perform (Talk, Listen, Active Controller).

4. The highest priority response to a parallel poll.

3-39. Inputting the Status Word

3-40. The Status Word is transferred to the A or B registers of the computer using the following sequence of machine instructions:

```
          .
          .
          .
          STF     SC
          LIA     SC
or
          .
          .
          .
          STF     SC
          LIB     SC
          .
          .
          .
SC        EQU     <select code of BUS I/O card>
```

Note

A OTA/B instruction may not be executed between the STF and LIA/B or inputting of data will result.

3-41. Status Word Coding

3-42. The coding of each of the bits of the Status Word is as follows:

BITS Ø — 3 PARALLEL POLL PRIORITY ENCODED IDENTIFICATION

Indicates the highest priority response to a parallel poll or the occurrence a Bus clear command. Highest priority is assigned to IFC (BCL) followed by DIO8, etc.

The priority encoding scheme is shown in Figure 3-2.

BIT 4 ACTIVE FLIP-FLOP STATUS

Indicates the state of the ACTIVE Flip-Flop.

If BIT 4 = 1, the ACTIVE Flip-Flop is set.

If Bit 4 = Ø, the ACTIVE Flip-Flop is reset.

BIT 5 TALK F STATUS

Indicates the state of the TALK Flip-Flop.

If BIT 5 = 1, the TALK Flip-Flop is set (i.e., the card is addressed to talk).

If BIT 5 = Ø, the TALK Flip-Flop is reset (i.e., the card has not been addressed to talk).

BIT 6 LISTEN FLIP-FLOP STATUS

Indicates the state of the LISTEN Flip-Flop.

If BIT 6 = 1, the LISTEN Flip-Flop is set (i.e., the card is addressed to listen).

If BIT 6 = Ø, the LISTEN Flip-Flop is reset (i.e., the card has not been addressed to listen).

BIT 7 ATN (MRE) LINE STATUS

Indicates the state of the BUS signal line ATN.

If BIT 7 = 1, ATN (MRE) is Low. (BUS in Command Mode)

If BIT 7 = Ø, ATN (MRE) is High. (BUS in Data Mode)

BIT 8 REN LINE STATUS

Indicates the state of the BUS signal line REN.

If BIT 8 = 1, REN is Low. (BUS is Remote Enabled)

If BIT 8 = Ø, REN is High. (BUS is in Local)

BIT 9 NDAC LINE STATUS

Indicates the state of the BUS signal line NDAC.

BIT 10 NRFD LINE STATUS

Indicates the state of the BUS signal line NFRD.

If BIT 10 = 1, NRFD is High.

If BIT 10 = Ø, NRFD is Low.

BIT 11 DAV LINE STATUS

Indicates the state of the BUS signal line DAV.

If BIT 11 = 1, DAV is Low.

If BIT 11 = Ø, DAV is High.

BIT 12 END OF RECORD (EOR) FLAG STATUS

Indicates the state of the End of Record Flag.

If BIT 12 = 1, EOR FLG has been set.

If BIT 12 = Ø, EOR FLG has not been set.

BIT 13 OUTPUT REGISTER ACCEPT (ORA) FLAG

Indicates the state of the ORA Flag.

If BIT 13 = 1, the ORA Flag has been set.

If BIT 13 = Ø, the ORA Flag is clear.

BIT 14 INPUT REGISTER LOADED (IRL) FLAG

Indicates the state of the IRL Flag.

If BIT 14 = 1, the IRL Flag has been set.

If BIT 14 = Ø, the IRL Flag is clear.

BIT 15 INTERFACE CLEAR (IFC), SERVICE REQUEST (SRQ) AND SERIAL POLL MODE (SPM) FLAGS STATUS

If Active (Bit 4 = 1), Bit 15 = 1 indicates that either the IFC (BCL) or SRQ Flags have been set and Bit 15 = Ø indicates that both the IFC (BCL) and SRQ Flags are clear.

If Inactive (Bit 4 = Ø), Bit 15 = 1 indicates that the SPM Flag has been set and Bit 15 = 1 indicates that the SPM Flag is clear.

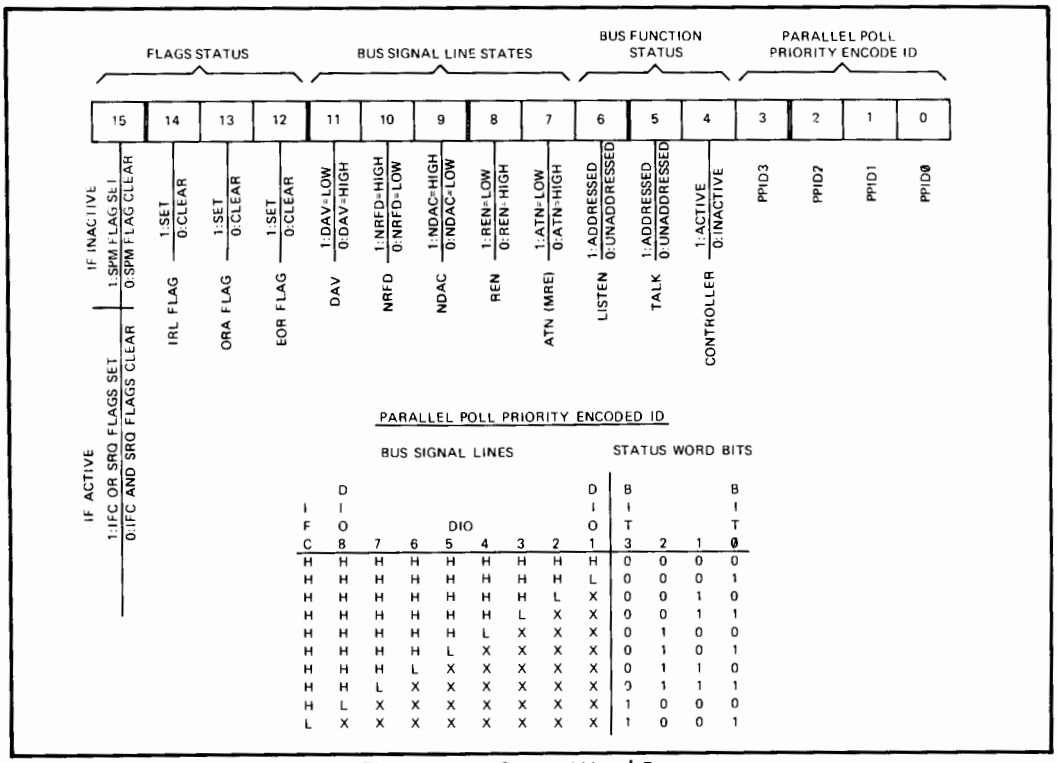


Figure 3-2. Status Word Format

3-43. DATA OUTPUT

3-44. Data Transfer Capabilities

3-45. Data can be transferred from the computer to the Bus via the A or B registers under program control or via memory under Direct Memory Access (DMA) control. Either whole (16 bits) or half words (8 bits) can be output from the computer. If whole words are to be used, the I/O card's packing feature must be enabled by outputting a Control Word.

3-46. Output Data Types

3-47. Data that is outputted can be classified into three types. They are distinguished by the affect they have on the devices on the Bus and the I/O card. Each is output in the same manner, only their affect is different. All data type can be output with or without packing.

3-48. The function of the three data types are:

1. To send information (device data) from the computer to a device(s) on the Bus while the computer is acting as the Talker. Coding and Formatting is a function of the devices.

2. To send Addresses and coded Commands to the Bus while the computer is acting as the Controller. Codes are defined by Bus.

3. To send ASCII data, control codes, Addresses and Commands when the I/O Card is in the ASCII Mode. Some codes are defined by I/O Card.

3-49. Output Data Registers

3-50. There are two registers on the Bus I/O card which store data received from the computer prior to being sent over the Bus. These are the Output Word Register (OWR) and the Output Byte Register (OBR). The OWR is a 16 bit (2 bytes) register which stores the data received from the A or B registers or memory. The OBR is an 8 bit (1 byte) register which stores the data which is being sent via the Bus.

3-51.The OWR is loaded when an OTA/B instruction is executed or simulated by DMA. Its contents are transferred to the OBR by the I/O Card in 8 bit bytes. If packing has been enabled by outputting a Control Word with Bit 11 = 1, then two bytes are transferred from the OWR to the OBR for each OTA/B. If packing is disabled, only one byte is transferred for each OTA/B.

3-52. The contents of the OBR are transferred via the Bus in accordance with the Bus handshake lines. Each time a byte is accepted by the device(s) on the Bus, a new byte is transferred from the OWR to the OBR until all the data in the OWR (one byte without packing, two with) has been accepted.

3-53. When data is being transferred under program control (using OTA/B instructions) only one or two bytes can be stored at a time in the two registers. The acceptance of all bytes is indicated by a flag* that can be tested or used to generate an interrupt. When data is being transferred by DMA, up to three bytes can be stored. A special flag* indicates when the OWR is empty and requests the next DMA output cycle. This allows DMA and Bus cycles to overlap.

*See paragraphs 3-76 to 3-103.

3-54. To Output Data

3-55. Data may be transferred from the A or B register of the computer to a device on the Bus under program control by using the following instruction sequence:

```
        .
        .
        .
    LDA DATA
    OTA SC(,C)
        .
        .
        .
or
        .
        .
        .
    LDB DATA
    OTB SC(,SC)
        .
        .
        .
```

Note

A STF SC instruction may not precede the LDA/B and OTA/B instructions or the data will be interpreted as a Control Word by the I/O card.

3-56. Data may also be transferred from the computer's memory to a device on the Bus by using the Direct Memory Access (DMA) option.

3-57. Output Data Format

3-58. The correspondence between the way the data appears in the A/B registers or Memory and the way it appears when transferred to the Bus is shown in Figure 3-3.

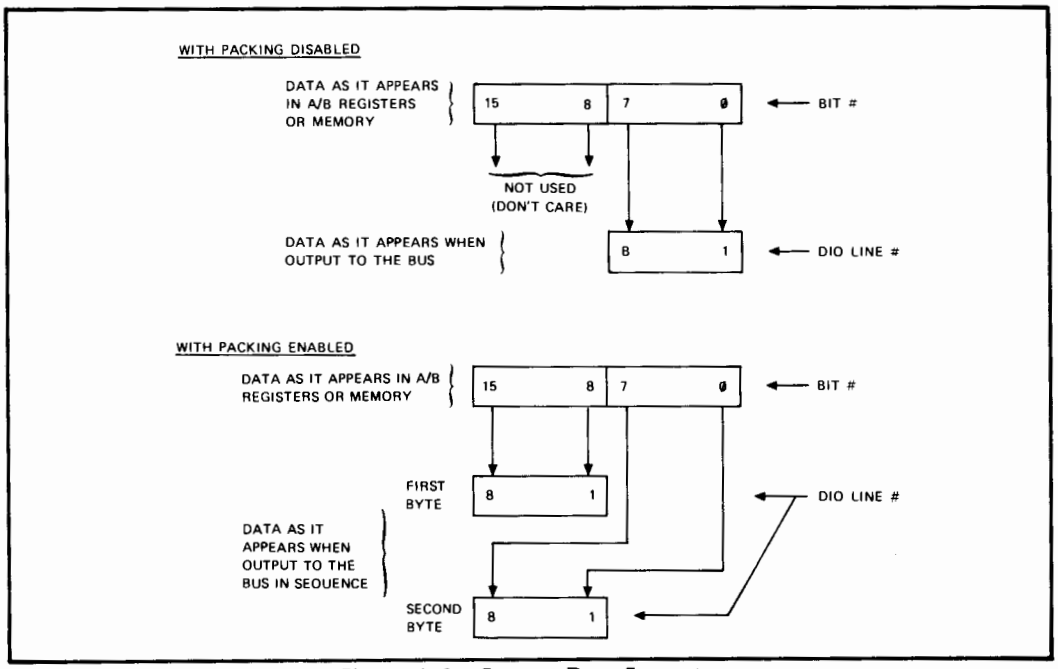


Figure 3-3. Output Data Formats

3-59. With packing disabled, only the lower half of the machine word is transferred (bits Ø-7) to the Bus. The upper half (bits 8-15) is ignored. Bit Ø of the machine word corresponds to DIO1 of the Bus, Bit 1 to DIO2, etc.

3-60. With packing enabled, both the upper and lower half of the machine word are transferred to the Bus. The upper half is output as the first Bus byte, the lower half second. Bits Ø and 7 correspond to DIO1 of the Bus, Bits 1 and 8 to DIO2, etc.

3-61. DATA INPUT

3-62. Data Transfer Capabilities

3-63. Data can be transferred from the Bus to the computers' A or B registers under program control or to the computers' memory under Direct Memory Access (DMA) control. One or two Bus bytes may be packed into one computer word by the I/O card, as selected by outputting a Control Word.

3-64. Input Data Type

3-65. The only type of data that can be input is data received from a device on the Bus while the computer is addressed to Listen and the device to Talk. The coding and formatting of the data is a function of the two devices.

3-66. Input Word Register

3-67. The Input Word Register (IWR) is a 16 bit register on the I/O card which can store one or two bytes of data received from a device on the Bus.

3-68. One byte is loaded into the IWR each time a Bus handshake cycle occurs. It will be loaded with one byte if packing is disabled and two bytes if packing is enabled. When the IWR is full (1 byte without packing, 2 with) a flag* will be set which can be tested, used to cause an interrupt, or used to request a DMA input cycle. The contents of IWR is transferred to the A or B registers when a LIA/B or MIA/B instruction is executed or to memory when a DMA cycle simulates a LIA/B.

3-69. To Input Data

3-70. Data may be transferred to the A or B register under program control by the following sequence of instructions:

```
        .
        .
        .
    LIA sc
    STA DATA
        .
        .
        .
or
        .
        .
        .
    LIB sc
    STB DATA
        .
        .
        .
```

Note

A STF sc instruction may not precede the LIA/B instruction or the inputting of a Status Word will result.

*See paragraphs 3-76 to 3-103.

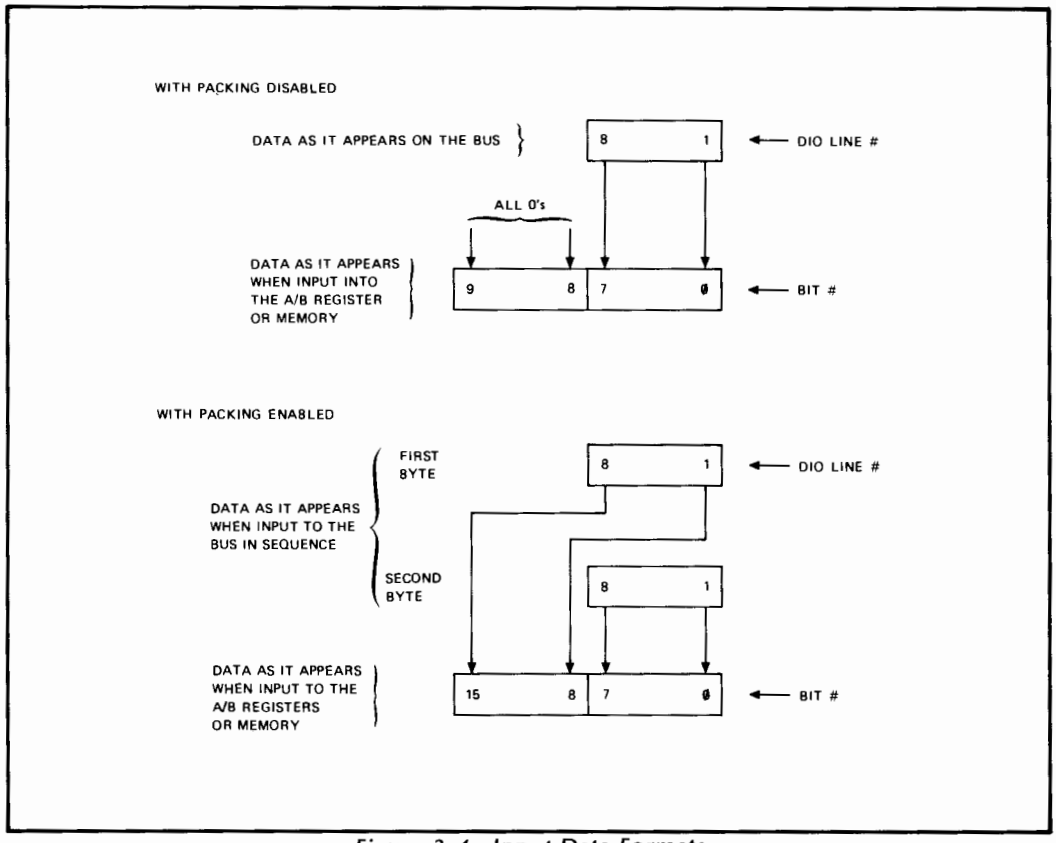


Figure 3-4. Input Data Formats

3-71. Data may also be transferred to the computer's memory using the DMA option. See paragraph 3-101.

3-72. Input Data Format

3-73. The correspondence between the way the data appears on the Bus data lines and the way it appears when it is transferred to the A/B register or memory is shown in Figure 3-4.

3-74. With packing disabled only the lower half (bits Ø-7) of the computer word contains a Bus byte. The upper half (bits 8-15) will contain all zeroes. The Bus signal line DIO1 corresponds to Bit Ø, DIO2 to Bit 1, etc.

3-75. With packing enabled both the upper and lower halves of the computer word will contain Bus bytes. The upper half will contain the first byte received, the lower the second. The Bus signal line DIO1 corresponds to Bit Ø and Bit 8, DIO2 to Bits 1 and 9, etc.

3-76. FLAGS

3-77. Flag Organization

3-78. There are eight flags associated with various aspects of the cards' and the Bus' operation. Six of the flags (EOR, ORA, IRL, IFC (BCL), SRQ and SPM Flags) can be selectable combined to set a seventh flag (Main Flag) which can be tested by the program or used to cause an interrupt. The six flags may also be tested by inputting a Status Word. The eighth flag is used in conjunction with outputting data under Direct Memory Access (DMA) control.

3-79. Main Flag

3-80. The Main Flag indicates that at least one auxiliary flag has been set. It is set if any one of the auxiliary flags selected by the Control Word occurs. It is cleared by a CLF instruction if the Control Flip-Flop* is clear.

3-81. The state of the Main Flag can be tested by the SFS or SFC instructions. It may also be used to cause an interrupt if it is set and the Control Flip-Flop* is set and the interrupt system has been turned on (by a STF Ø instruction).

3-82. End of Record Flag (EOR)

3-83. The End of Record (EOR) Flag indicates that the byte of data received is the last in the string. The EOR Flag is set only if the Bus I/O card is addressed to Listen and the talker signals "End" (EOI is Low) or an ASCII linefeed character ($Ø12_8$) is received and the ASCII Mode has been enabled by the Control Word. The EOR Flag is cleared by a CLF instruction if the Control Flip-Flop** has been cleared.

3-84. The EOR Flag may be tested by inputting a Status Word. If Bit 12 = 1, the EOR Flag is set. The EOR Flag may be enabled to set the Main Flag by outputting a Control Word with Bit 12 = 1.

3-85. Output Register Accepted Flag (ORA)

3-86. The Output Register Accepted (ORA) Flag indicates when set that all data in the Output Word and Output Byte Register has been accepted by the device(s) on the device(s) on the Bus. The ORA Flag will be set if:

1. The Bus I/O card is addressed to Talk and the Bus is in the Data Mode or

2. If the Bus I/O is the Active Controller and the Bus is in the Command Mode and the last byte in the OWR and OBR has been accepted.

3-87. The ORA Flag is cleared by a OTA/B instruction. It can be initially cleared by outputting a Control Word = $XXXXX7_8$.

3-88. Input Register Loaded Flag (IRL)

3-89. The Input Register Loaded (IRL) Flag indicates when set that data has been loaded into the Input Register and is ready to be input into the computer.

3-90. The IRL Flag will be set if the I/O card is addressed to Listen and the Bus is in the Data Mode and a handshake cycle occurs. If the Packing Mode is disabled, the IRL Flag will be set each time a handshake cycle occurs. If the Packing Mode is enabled, the IRL Flag will only be set every other time a handshake cycle occurs. The IRL Flag is cleared by a LIA/B or MIA/B instruction.

3-91. The IRL Flag can be tested by inputting the Status Word and testing bit 14 or it can be used to set the Main Flag by outputting a Control Word with bit 14 = 1 or it can be selected to request DMA cycles by outputting a Control Word with bit 10 = Ø.

3-92. Interface Clear Flag (IFC)

3-93. The Interface Clear Flag (IFC) indicates when set that an Interface Clear command has occurred on the Bus (it may or may not have been generated by the Bus I/O card). The IFC Flag is cleared by a CLF instruction if the Control Flip-Flop** is clear.

Note : IFC was formerly BCL (Bus Clear).

*See paragraph 3-117.
**See paragraph 3-115.

3-94. The IFC Flag can be tested by inputting a Status Word. If the Status Word = X XXX XXX XXX XX1 001, then the IFC Flag is set. It may also be enabled to set the Main Flag if the I/O card is Active by outputting a Control Word with Bit 15 = 1.

Note

This will also enable the SRQ Flag to set the Main Flag.

3-95. Service Request Flag (SRQ)

3-96. The Service Request (SRQ) Flag indicates that some device on the Bus wants service from the controller. The SRQ Flag is set when the first device requests service. It will remain set as long as at least one device still requires service. The SRQ Flag is cleared by executing a Serial Poll to all devices.

3-97. The SRQ Flag may be tested only if the I/O card is Active by inputting a Status Word. If Bit 15 = 1 (and Bit 4 = 1)* and Bits Ø - 3 $\neq 11_8$, then the SRQ Flag is set. If the computer is the System Controller and is not executing an Interface Clear Command, then Bits Ø - 3 need not be tested. The SRQ Flag may also be enabled to set the Main Flag if the I/O card is Active and a Control Word with Bit 15 = 1 is output.

Note

This also enables the IFC (BCL) Flag to set the Main Flag.

3-98. Serial Poll Mode Flag (SPM)

3-99. The Serial Poll Mode (SPM) Flag indicates when set that another controller has entered the Serial Poll Mode to determine the source of a Service Request. The SPM Flag will be set when the Controller sends the Serial Poll Mode Enable command. It will be cleared by the Controller sending the Serial Poll Disable command or the Interface Clear Command.

3-100. The SPM Flag may be tested only if the I/O card is inactive as a controller and a Status Word is input. If Bit 15 = 1 (and Bit 4 = Ø)*, the SPM Flag is set. The SPM Flag can also be used to set the Main Flag if the I/O card is inactive by outputting a Control Word with Bit 15 = 1.

3-101. DMA Output Request Flag

3-102. The DMA Output Request Flag indicates when set that all the data in the Output Word Register has been transferred to the Output Byte Register. It is set at the same time the last byte is loaded into the OBR. This occurs when the previous byte has been accepted from the OBR by the device(s) on the Bus. If packing is used, the DMA Output Request Flag will be set as the second byte is loaded. If packing is not enabled, it will be set for each byte transferred. The DMA Output Request Flag is cleared by a CLF instruction (during DMA operation, it is issued by DMA).

3-103. The DMA Output Request Flag can only be used to request DMA cycles. It must be enabled to do so by outputting a Control Word with Bit 10 = 1. Furthermore, DMA must be initialized with various parameters to operate properly.

*Optional

3-104. MACHINE I/O INSTRUCTIONS OPERATION

3-105. This section describes the operation of each of the computer's I/O instructions with respect to the Bus I/O card. It should be noted that some of them operate somewhat differently than the normal description of each indicates.

3-106. Difference in Use of I/O Instructions

3-107. Specifically, the STF instruction is used differently to set a data type flip-flop, the OTA/B, LIA/B, MIA/B do more (STC's are not used with them), STC does less (only enabling interrupts) and the CLF instruction is qualified by the control flip-flop.

3-108. STF Instruction

3-109. A STF sc instruction prepares the Bus I/O card indicated by sc to receive a Control Word or input a Status Word. Execution of a STF instruction changes the operation of the next OTA/B, LIA/B, MIA/B instruction on the I/O card. Execution of a OTA/B, LIA/B, MIA/B instruction returns them to their normal operation.

3-110. OTA and OTB Instructions

3-111. An OTA sc or OTB sc loads the contents of the A or B registers into the Output Word Register and clears the ORA Flag if preceded by a STF sc instruction, outputs a Control Word to the Bus I/O card indicated by sc.

3-112. LIA, LIB, MIA and MIB Instructions

3-113. A LIA sc or LIB sc instruction transfers the contents of the Input Register or, if preceded by a STF sc instruction, the Status Word of the Bus I/O card indicated by sc to the A or B registers. The MIA sc and MIB sc instructions operate the same except they merge (inclusion "or") the contents into A and B.

3-114. A LIA/B, MIA/B instruction clears the Input Register Loaded Flag, presets the Input Byte Counter to byte Ø (first input) and sets the Not Ready For Data Flip-Flop.

3-115. SFS and SFC Instructions

3-116. A SFS sc (SFC sc) instruction causes the next instruction to be skipped (i.e., P + 2 is executed) if the Main Flag of the Bus I/O card indicated by sc is set (clear).

3-117. STC and CLC Instructions

3-118. A STC sc instruction enables (by setting the Control Flip-Flop) the Bus I/O card indicated by sc to cause an interrupt if the interrupt system is turned on and any one of the six flags selected by the Control Word occurs. In addition, a STC sc prevents any subsequent CLF sc instructions from clearing all but the DMA Output Request Flag.

3-119. A CLC sc instruction prevents (by clearing the Control Flip-Flop) the Bus I/O card indicated by sc from causing an interrupt and enables the CLF sc instruction to clear the Main Flag, EOR Flag and IFC (BCL) Flag.

3-120. CLF Instruction

3-121. A CLF sc instruction clears the DMA Output Request Flag and if the Control Flip-Flop is clear, it will also clear the Main Flag, the EOR Flag and the IFC Flag.

Note

A stand alone CLF SC instruction does not operate the same as a ,C appended to another I/O instruction. The ,C works as described above. The stand alone CLF SC instruction executes as though it were STF SC ,C thus it prepares the I/O to receive a Control Word or send a Status Word. To effectively execute a stand alone CLF, use a CLC SC, C instruction.

3-122. ASCII MODE

3-123. Description

3-124. The ASCII Mode is a special operating mode of the Bus I/O card in which six of the functions of the Control Word may be controlled by outputting reserved data codes. These are listed in Table 3-1. It also enables an ASCII Linefeed ($Ø12_8$) character to set the End of Record Flag when receiving data while addressed to Listen.

Table 3-1. ASCII Mode Codes

FUNCTION	DATA CODE		
	OCTAL	ASCII	TTY
INTERFACE CLEAR COMMAND	Ø33	ESC	ESC
REMOTE ENABLE COMMAND	Ø02	STX	CTRL and B
LOCAL COMMAND	Ø03	ETX	CTRL and C
SET COMMAND MODE	Ø16	SO	CTRL and N
SET DATA MODE	Ø17	SI	CTRL and O
SIGNAL END OF RECORD	Ø12	LF	LINE FEED

3-125. Enabling the ASCII Mode

3-126. The ASCII Mode is enabled by outputting a Control Word with Bit 8 = 1 when Group 3 is enabled.

3-127. Operation When Outputting

3-128. When the ASCII Mode is enabled, any one of the functions shown in Table 3-1 may be executed by outputting the indicated data code. The effect of each on the I/O on the Bus is the same as outputting a Control Word for the same function.

3-129. When in the ASCII Mode, all codes which have control functions defined (per Table 3-1) will not be transmitted to the Bus with one exception; Linefeed ($Ø12_8$). Linefeed causes End of Record to be signaled and is transmitted to the Listener(s). (The card must be

addressed to Talk.) The other ASCII Mode codes cause an internal handshake to occur which operates the same as if a device had accepted the data. That is the ORA Flag will be set, etc.

3-130. An ASCII Mode code (except LF) can be output whether or not the card is addressed to Talk or in the Command Mode. All other codes must be output when appropriate, i.e., device data only when addressed to talk, Address, etc. only when in the Command Mode.

3-131. The ASCII Mode operates the same with or without packing enabled and under program or DMA data transfer or any combination thereof.

3-132. Operation When Inputting

3-133. If the I/O card is addressed to Listen and the ASCII Mode has been enabled, an ASCII Linefeed ($Ø12_8$) will cause the End of Record (EOR) Flag to be set. The Linefeed character will also be loaded into the Input Register. If packing is disabled, the receipt of the Linefeed character will also set the Input Register Loaded (IRL) Flag. If packing is enabled, the IRL Flag will only be set if the Linefeed was the second byte received.

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION

4-2. This section explains the theory of operation of the HP 59310A Bus Input/Output Interface card. The circuit analysis presented in this section is limited to a description of a simplified block diagram and a detailed block diagram.

4-3. GENERAL THEORY

4-4. The purpose of the 59310A is to interface the HP 2100 series computer I/O backplane to the HP Interface Bus (HP-IB). This requires translation of the computer backplane CTL logic levels to the TTL logic level used by the HP-IB. The HP Interface Bus uses 8-bit words which requires the conversion of the computer 16-bit word to two 8-bit words.

4-5. The 59310A Bus Input/Output card performs four major functions; computer control word processing, bus data output, computer data input, and status information input to the computer. These four functions are controlled by the control signals applied from the computer through the I/O backplane to the Control Logic, see Figure 4-1.

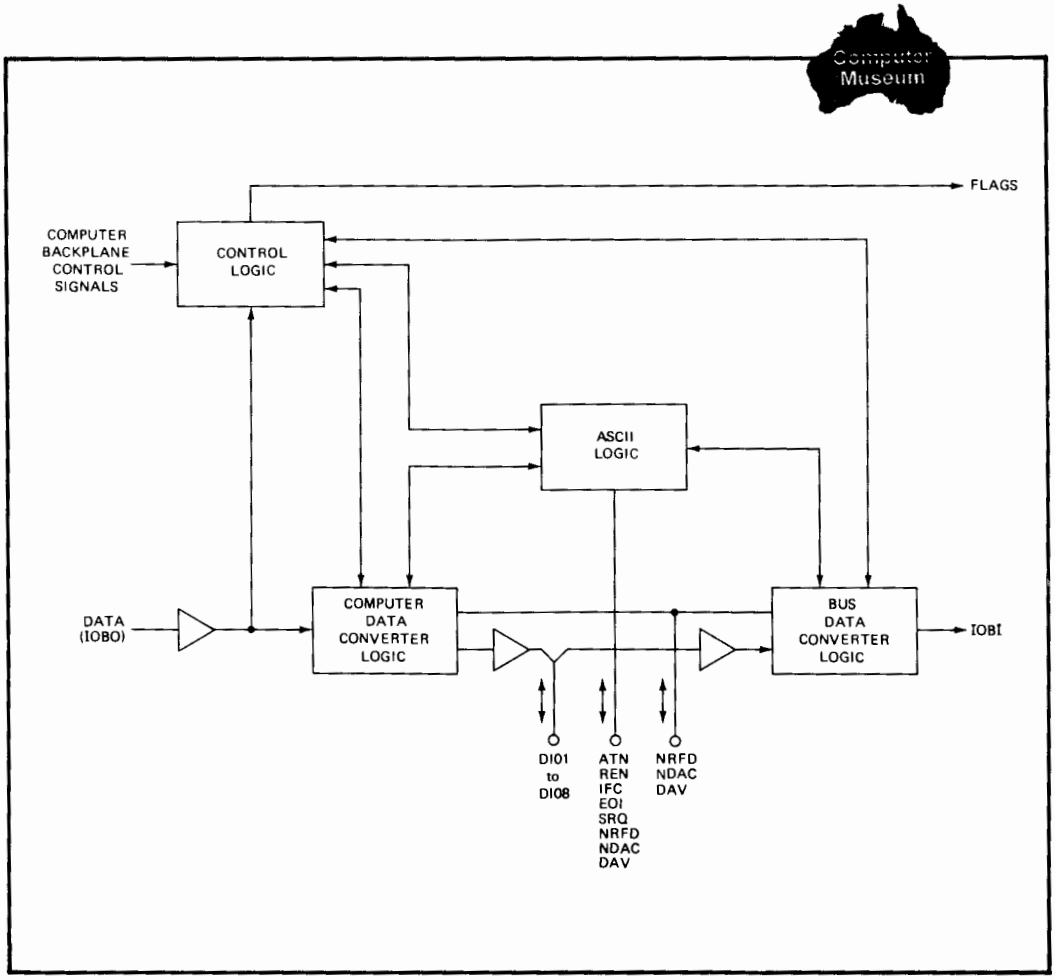


Figure 4-1. Simplified Block Diagram

4-6. Control Word Processing

4-7. The computer control word output, which is applied through the BP DATA RECEIVERS to the CONTROL LOGIC, determines the operating mode of the Bus Input/Output card. When the control word processing function is initiated, the CONTROL LOGIC, in response to the computer backplane CTL signals, inhibits the COMPUTER DATA CONVERTER LOGIC and the BUS DATA CONVERTER LOGIC. The CONTROL LOGIC, in conjunction with the computer control word output, determines if the Bus Input/Output card is either a listener or talker; the state of the ASCII LOGIC; and the logic state of the flag outputs to the computer.

4-8. Bus Data Output

4-9. The 59310A Bus I/O card applies data to the bus lines (DI01 through DI08) when the COMPUTER DATA CONVERTER LOGIC is enabled by the CONTROL LOGIC. The COMPUTER DATA CONVERTER LOGIC stores the 16-bit computer word and, after the handshake sequence is completed, transfers eight bits to the bus data lines. The handshake cycle is repeated and the second eight bits are applied to the bus data lines. The data output of the COMPUTER DATA CONVERTER LOGIC is continuously monitored by the ASCII LOGIC. If the ASCII LOGIC is enabled by the CONTROL LOGIC and the data output is a special ASCII character, the appropriate ASCII command output is activated.

4-10. Computer Data Input

4-11. The Bus Input/Output card applies data to the computer when the CONTROL LOGIC enables the BUS DATA CONVERTER LOGIC. The BUS DATA CONVERTER LOGIC converts two eight bit words into one 16-bit word before outputting to the computer. This accomplished in the following manner. After the completion of the handshake cycle, the first eight bits are transferred from the bus data lines and stored in the BUS DATA CONVERTER LOGIC. The handshake cycle is repeated and the second eight bits are clocked into the appropriate output register of the BUS DATA CONVERTER LOGIC. Two eight bit words, now one 16-bit word, are clocked into the computer.

4-12. Status Information Input

4-13. The fourth major function of the Bus Input/Output card is the outputting of card status information to the computer. The BUS DATA CONVERTER LOGIC applies status information to the computer when the CONTROL LOGIC inhibits the data output and enables the status word output. The status word output is used by the computer to monitor card operation to determine which flag caused an interrupt; to determine the state of the input/output handshake cycle; and to determine the state of the ASCII commands.

4-14. DETAILED THEORY

4-15. Data Input/Output Control

4-16. The four major functions of the Bus Input/Output card are controlled by the DATA INPUT/ OUTPUT CONTROL, see Figure 8-2. The DATA INPUT/OUTPUT CONTROL generates four outputs from the IOI, IOO, and STF inputs. These outputs are the IOI SC status, which puts the card in the computer status information function; the IOI SC data, which puts the card in the computer data input function; the IOO SC control, which puts the card in the control word processing function; and the IOO SC data, which puts the card in the bus data output function.

4-17. Control Word Processing

4-18. CTL WORD REGISTER AND DECODER. The computer control word determines the card operating mode and is processed by the CTL WORD REGISTER AND DECODER. When the card is

in the control word processing function, the transfer of data from the card to either the bus (lines DI01 through DI08) or the computer is inhibited by the DATA INPUT/OUTPUT CONTROL. The control word is a 16-bit word which is divided into three functional groups; groups one, two, and three. Group one consists of bits seven through fifteen. Group two consists of bits three through six and group three consists of bits zero through two. These three groups can be used independently or in combination with each other.

4-19. The group one portion of the control word is loaded into the CTL WORD REGISTER AND DECODER whenever bit seven of the control word is set high. These eight bits control the selection of which flags will cause an interrupt to be tested by a skip flag set or skip flag clear instruction. Group one also sets the ASCII mode in either the address or data mode and sets the DMA in an input or output operation. In addition, these bits determine if the service request (SRQ) is generated on the bus with an input/output operation and if packing is enabled or disabled.

4-20. The group two portion of the control word consists of bits three through six and is subdivided into two groups: groups 2a and 2b. Group 2a controls the ATN and EOI flip-flops and is selected whenever bit five of the control word is set high. Group 2b controls the talk and listen flip-flops and is selected whenever bit six of the control word is set high. Groups 2a and 2b can be used independently or in conjunction with each other.

4-21. The third group of the control word consists of bits zero through two and is decoded by the CTL WORD REGISTER AND DECODER into six control lines. These six control lines, in addition to controlling the REN and ACTIVE flip-flops and the IFC single-shot, also sets the OUTPUT DATA CONTROL and the INPUT DATA CONTROL to their initial state (byte one).

4-22. EOI. The EOI flip-flop, set by the control word, determines the state of the EOI signal output line. The EOI flip-flop is reset by either the control word, an IFC signal from the bus, computer turn on, or when the computer preset push button is engaged.

4-23. REN. The REN flip-flop output is enabled when switch SW111 (position 6) is set to REN ON. When enabled, the REN flip-flop sets the REN output line low when triggered by either the control word, the ASCII MODE LOGIC, computer turn on, or when the computer preset push button is pushed.

4-24. ACTIVE. The output state of the ACTIVE flip-flop is controlled by the control word and the IFC single-shot. When the ACTIVE flip-flop is set, the Bus Input/Output card becomes the bus controller. The bus controller is a device that can send out addresses and universal commands to instruments connected to the HP-IB. The ACTIVE flip-flop is reset by the control word or when some other device on the bus sets EOP low.

4-25. ATN. When the ACTIVE flip-flop is set, the ATN driver is enabled. This allows the ATN flip-flop to control the ATN output line. The ATN flip-flop is set by either the control word or the ASCII MODE LOGIC. It is reset by the following: the control word, ASCII MODE LOGIC, triggering of the IFC single-shot, computer turn on, and when the computer preset button is pushed if the Bus Input/ Output card is the system controller.

4-26. IFC. The IFC single-shot output is enabled when switch SW111 (position 7) is set to IFC ON. In this position, the IFC single-shot produces a 100 microsecond pulse output when triggered by one of the following: an octal one in the lower octal digit of the control word, the ASCII MODE LOGIC, computer turn-on, or when the computer preset push button is pushed.

4-27. IFC BUFFER AND FILTER. The IFC BUFFER AND FILTER, in addition to buffering the IFC signal line from the bus, also filters the IFC line. Filtering is required to eliminate fast transient noise spikes on the bus IFC line to prevent falsely clearing of various flip-flops.

4-28. IFC OFF. The IFC OFF flip-flop, set whenever the IFC bus signal line goes low, is used to generate an interrupt output to the computer. It can be tested by either a skip flag set instruction or by loading the status word into the computer. A clear flag instruction resets the IFC flip-flop.

4-29. Bus Data Output.

4-30. The transfer of data from the computer to the Bus Input/Output card to the bus data lines uses a series of circuits on the Bus Input/Output card. These circuits are the BP DATA RECEIVERS, the DATA INPUT/OUTPUT CONTROL, the OUTPUT WORD REGISTER, the OUTPUT DATA CONTROL, the OUTPUT HANDSHAKE LOGIC, the OUTPUT BYTE REGISTER, and the DIO DRIVERS.

4-31. BP DATA RECEIVERS. The BP DATA RECEIVERS provide signal buffering from the computer IOBO data bus to the Bus Input/Output card internal bus. In addition, the BP DATA RECEIVERS translate the computer backplane CTL logic level to the TTL logic level required by the Bus Input/Output card. The output of the BP DATA RECEIVERS is applied to the CTL WORD REGISTER AND DECODER and to the OUTPUT WORD REGISTER.

4-32. OUTPUT WORD REGISTER. The OUTPUT WORD REGISTER is a 16-bit register which is used to store the input data because the computer applies data to the IOBO lines for only 400 nanoseconds. Data is strobed into the OUTPUT WORD REGISTER by the IOO SC data signal output of the DATA INPUT/OUTPUT CONTROL. The transfer of information from the OUTPUT WORD REGISTER to the OUTPUT BYTE REGISTER is controlled by the OUTPUT DATA CONTROL and the OUTPUT HANDSHAKE LOGIC.

4-33. OUTPUT BYTE REGISTER. The OUTPUT BYTE REGISTER is an eight bit register used to transfer the data from the OUTPUT WORD REGISTER to the DIO DRIVERS in eight bit segments. This operation is controlled by two inputs applied from the OUTPUT DATA CONTROL. One input is the word shift (ws), determining which eight bits of the OUTPUT WORD REGISTER are applied to the DIO DRIVERS. The remaining input is the clock and is used to transfer data into the OUTPUT BYTE REGISTER.

4-34. OUTPUT DATA CONTROL. The OUTPUT DATA CONTROL consists of a series of flip-flops. These flip-flops are used to control the OUTPUT BYTE REGISTER, to generate a DMA flag output, to enable the OUTPUT HANDSHAKE LOGIC, and to inform the computer of the OUTPUT BYTE REGISTER operating state. The IOO SC data signal input sets the output word register loaded flag (OWRA FLG) low and, after a 100 nanosecond delay, clocks data into the OUTPUT BYTE REGISTER. If packing is enabled, which is the ability to convert the computer 16-bit word into two eight bit words, and the OUTPUT DATA CONTROL is in byte one, bits zero through seven are transferred to the OUTPUT BYTE REGISTER. After the handshake cycle, the DMA FLAG output is set high and the OUTPUT DATA CONTROL is set to byte two. The DMA FLAG output requests the next DMA cycle of the computer. The second eight bits of the computer word, bits eight through fifteen, are clocked into the OUTPUT BYTE REGISTER and applied through the DIO DRIVERS to the bus output lines. After the handshake cycle, the OWRA FLG output is set high, indicating to the computer that the device on the bus has accepted both eight bit words. The OUTPUT DATA CONTROL is reset to byte one.

4-35. OUTPUT HANDSHAKE LOGIC. The OUTPUT HANDSHAKE LOGIC consists of a combination of logic functions that are used to control the outputting of data to the required handshake sequence. There is a 500 nanosecond delay incorporated in the OUTPUT HANDSHAKE LOGIC. After an initial 200 nanosecond delay, an enable is applied to the ASCII MODE LOGIC. An additional 300 nanoseconds later, if the NRFD on the bus is high, the DAV bus output line is set low. When the device on the bus has accepted the data, the DAC bus input is set high which resets the DAV output to high.

4-36. ASCII MODE LOGIC. The data output of the OUTPUT BYTE REGISTER is also applied to the ASCII MODE LOGIC. If the ASCII MODE LOGIC is enabled, bit-8 of the control word set high,

and the data is a reserved ASCII character, a low output is applied to the OUTPUT HANDSHAKE LOGIC. This ends the handshake cycle, giving the appearance that the device on the bus has accepted the data. In addition, the reserved ASCII characters are decoded by the ASCII MODE LOGIC, determining the state of the REN flip-flop, the MRE flip-flop, or the triggering of the EOP single-shot.

4-37. DIO DRIVERS. The output of the OUTPUT BYTE REGISTER is applied to the DIO DRIVERS. The DIO DRIVERS provide the drive for the bus data lines. These are tristate drivers and they are enabled only when the card is either addressed to talk or is an active controller with MRE set low.

4-38. Computer Data Input

4-39. The third major function of the Bus Input/Output card is the transferring of data from the INPUT DATA & STATUS WORD MULTIPLEXER to the computer. This is controlled by the INPUT HANDSHAKE LOGIC, the INPUT DATA CONTROL, and the INPUT DATA/WORD REGISTER. The input data is applied through the DIO RECEIVERS to the INPUT DATA/WORD REGISTER. The strobing of data into the INPUT DATA/WORD REGISTER is controlled by the handshake lines (DAV, NDAC, and NRFD) and the listen flip-flop. The listen flip-flop is part of the BUS COMMUNICATOR LOGIC. If the listen flip-flop is set and DAV goes low, the card can accept data into the INPUT DATA/WORD REGISTER. This is controlled by the INPUT HANDSHAKE LOGIC.

4-40. INPUT HANDSHAKE LOGIC. The INPUT HANDSHAKE LOGIC consists of a combination of logic functions that are used to control the strobing of data into the INPUT DATA/WORD REGISTER. There is a 200 nanosecond delay incorporated into the INPUT HANDSHAKE LOGIC. After an initial 100 nanosecond delay, the DAV input from the bus is applied to the INPUT DATA CONTROL and the NRFD bus output line is set high. After an additional 100 nanosecond delay, the NDAC output line is set high.

4-41. INPUT DATA CONTROL. The INPUT DATA CONTROL, consisting of a series of flip-flops and other logic elements, provides a clock output to both the EOR FLAG LOGIC and the upper and lower half of the INPUT DATA/WORD REGISTER. Also, an input register loaded flag (IRL FLG) output is applied to the computer.

4-42. If packing is enabled, the IOI SC data output signal from the DATA INPUT/OUTPUT CONTROL sets the INPUT DATA CONTROL to byte one. The DAV input, applied from the INPUT HANDSHAKE LOGIC, results in a clock applied to the lower half of the INPUT DATA/WORD REGISTER, transferring the contents of the DIO RECEIVERS into the INPUT DATA/WORD REGISTER. The clock is also applied to the EOR FLAG LOGIC and the INPUT DATA CONTROL is set to byte two. The next DAV input clocks the contents of the DIO RECEIVERS into the upper half of the INPUT DATA/WORD REGISTER. In addition, a IRL FLG is applied to the computer, indicating that the card has accepted both words of data and is ready to output.

4-43. If packing is not enabled, data is clocked into only the upper half of the INPUT DATA/WORD REGISTER. The INPUT DATA CONTROL is continuously set to byte two.

4-44. EOR FLAG LOGIC. The EOR FLAG LOGIC will respond to the clock output from the INPUT DATA CONTROL if enabled by either the ASCII MODE LF DETECTOR or the EOI flip-flop. The EOR flag can be used to generate an interrupt and be tested by either a skip flag set instruction or by the control word.

4-45. ASCII MODE LF DETECTOR. If the ASCII MODE LF DETECTOR is enabled by the BUS COMMUNICATOR LOGIC, it monitors the data output of the DIO DRIVERS. If an octal 12 is applied to the bus data lines (DIO1 through DIO7), the ASCII MODE LF DETECTOR will enable the EOR FLAG LOGIC. The EOR FLAG LOGIC, when clocked, will indicate end of record in the ASCII mode.

4-46. BUS COMMUNICATOR LOGIC. The BUS COMMUNICATOR LOGIC, in conjunction with the computer control word or with a bus controller, enables the Bus Input/Output card as either a talker or listener. The LISTEN flip-flop, contained in the BUS COMMUNICATOR LOGIC, is set or reset by either the computer control word or if a controller applies the appropriate Bus Input/Output listen or un-listen address to the data lines. Similarily, the TALK flip-flop is set or reset by either the computer control word or if a controller applies the correct Bus Input/Output talk address to the data lines.

4-47. An additional function in the BUS COMMUNICATOR LOGIC is the STATUS POLL flip-flop. The STATUS POLL flip-flop is set when a controller applies a status poll command to the bus data lines. It is used to cause an interrupt and is tested by the skip flag set instruction. The STATUS POLL flip-flop enables the computer to output a status byte to the controller on request. The status poll flip-flop is reset by either the status poll disable command, generated by the controller, or when EOP is set low.

4-48. ADDRESS COMPARATOR and ADDRESS SWITCH. Switch SW111 consists of eight, two position switches. Five of these switches, labeled BUS ADDRESS on the Bus Input/Output card, correspond to the ADDRESS SWITCH. The position of these switches determine the address of the card. The output of the ADDRESS SWITCH is applied to the ADDRESS COMPARATOR. The ADDRESS COMPARATOR, by comparing the output of the ADDRESS SWITCH to the data applied to the bus input data lines, determines if the Bus Input/Output card is addressed. When the card is addressed, the ADDRESS COMPARATOR applies an output to the BUS COMMUNICATOR LOGIC.

4-49. SRQ REQUEST LOGIC. The SRQ REQUEST LOGIC is used to generate an SRQ output, if enabled by the computer, whenever data is to be outputted or received. When enabled, an SRQ output is generated if the card is not addressed to talk and the output byte register loaded flip-flop (part of the OUTPUT DATA CONTROL) is set. Also, an SRQ output is generated if the card is not addressed to listen and the ready for data flip-flop (part of the INPUT HANDSHAKE LOGIC) is set.

4-50. PARALLEL SRQ I.D. If a SRQ is pending, the controller may execute a parallel service request I.D. sequence by setting both MRE and EOI low. In response, the PARALLEL SRQ I.D. will set the DIO line assigned to the card, line assignment is determined by the SRQ I.D. CODE switch SW11, low. This identifies the Bus Input/Output card as one of the sources of a SRQ.

4-51. SRQ PRIORITY AND ENCODER. The SRQ PRIORITY AND ENCODER is used to execute a PARALLEL SRQ I.D. cycle by encoding the data lines (DI01 through DI08) to the octal equivalent of the eight line code. Line DI08 has the highest priority of the data lines, octal code eight is generated if line DI08 is low. If DI08 is high, line DI07 has the highest priority. This sequence is repeated through line DI01. The EOP flip-flop generates the highest priority code, octal 11. Octal code 11 can be used to distinguish a service request from an EOP interrupt.

4-52. FLAG MULTIPLEXER and FLAGS. The FLAG MULTIPLEXER selects one of seven flag inputs that can be used as a source of interrupt. Any combination of these flags, which are enabled, will set the FLAGS. The output of the FLAGS is used in conjunction with the SFS/SFC LOGIC, enabling testing by these machine instructions. In addition, the FLAGS output is used with the INTERRUPT LOGIC to cause an interrupt if the computer uses the interrupt system.

4-53. INTERRUPT LOGIC. The INTERRUPT LOGIC generates an interrupt output to the computer if the interrupt system in the computer is enabled and a high priority interrupt from another I/O card is not pending. If the FLAGS is set, any other interrupt is locked out until the interrupt from the Bus Input/Output card is processed.

4-54. DMA FLAG MULTIPLEXER. The DMA FLAG MULTIPLEXER selects which flag, the IRL flag or the DMA output request flag, is used to generate a DMA service request. The control word determines flag selection.

4–55. Status Information Input

4–56. The fourth major function of the Bus Input/Output card is the transfer of the status word from the INPUT DATA & STATUS WORD MULTIPLEXER to the computer. The DATA INPUT/OUTPUT CONTROL IOI SC status output inhibits bus data transfer and enables the outputting of the status word. The status word is used by the computer to monitor card operation to determine which flag caused an interrupt; to determine the state of the handshake cycle; and to determine the state of the ASCII commands.

SECTION V

MAINTENANCE

5-1. INTRODUCTION

5-2. This section contains troubleshooting information.

5-3. TROUBLESHOOTING

5-4. Refer to Diagnostic Program Procedure, Bus Input/Output Card Diagnostic (59310A) manual part number 59310-90010 (for diagnostic program use part number 59310-60010). The program is designed to rapidly confirm proper operation of the Bus I/O card and to assist in troubleshooting defective cards.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering replaceable parts.

6-3. Table 6-1 gives the meanings of the abbreviations and reference designations used in the table of replaceable parts.

6-4. Table 6-2 is the list of replaceable parts and is organized as follows:

1. Components in alpha-numerical order by reference designation.
2. Miscellaneous parts.

The information given for each part consists of

1. the Hewlett-Packard part number,
2. total quantity (Qty) in the instrument,
3. description of the part,
4. typical manufacturer of the part in a 5-digit code, and
5. the manufacturer's number for the part.

Total quantity for each part is given only once — at the first appearance of the part number.

6-5. Table 6-3 contains the names and addresses that correspond to the manufacturers' code numbers.

Table 6-1. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	E	= miscellaneous electrical part	P	= electrical connector (movable portion); plug	U	= integrated circuit; microcircuit
AT	= attenuator; isolator; termination	F	= fuse			V	= electron tube
B	= fan; motor	FL	= filter	Q	= transistor; SCR; triode thyristor	VR	= voltage regulator; breakdown diode
BT	= battery	H	= hardware				
C	= capacitor	HY	= circulator	R	= resistor	W	= cable; transmission path; wire
CP	= coupler	J	= electrical connector (stationary portion); jack	RT	= thermistor		
CR	= diode; diode thyristor; varactor			S	= switch	X	= socket
				T	= transformer	Y	= crystal unit–piezoelectric
DC	= directional coupler	K	= relay	TB	= terminal board		
DL	= delay line	L	= coil; inductor	TC	= thermocouple	Z	= tuned cavity; tuned circuit
DS	= annunciator; signaling device (audible or visual); lamp; LED	M	= meter	TP	= test point		
		MP	= miscellaneous mechanical part				

ABBREVIATIONS

A	= ampere	avg	= average	CHAN	= channel	dc	= direct current
ac	= alternating current	AWG	= American wire gauge	cm	= centimeter	deg	= degree (temperature interval or difference)
ACCESS	= accessory			CMO	= cabinet mount only		
ADJ	= adjustment	BAL	= balance	COAX	= coaxial		
A/D	= analog-to-digital	BCD	= binary coded decimal	COEF	= coefficient	...°	= degree (plane angle)
AF	= audio frequency			COM	= common	°C	= degree Celsius (centigrade)
AFC	= automatic frequency control	BD	= board	COMP	= composition		
		BE CU	= beryllium copper	COMPL	= complete	°F	= degree Fahrenheit
AGC	= automatic gain control	BFO	= beat frequency oscillator	CONN	= connector	°K	= degree Kelvin
				CP	= cadmium plate	DEPC	= deposited carbon
AL	= aluminum	BH	= binder head	CRT	= cathode-ray tube	DET	= detector
ALC	= automatic level control	BKDN	= breakdown	CTL	= complementary transistor logic	diam	= diameter
		BP	= bandpass			DIA	= diameter (used in parts list)
AM	= amplitude modulation	BPF	= bandpass filter	CW	= continuous wave		
		BRS	= brass	cw	= clockwise	DIFF AMPL	= differential amplifier
AMPL	= amplifier	BWO	= backward-wave oscillator	cm	= centimeter		
APC	= automatic phase control			D/A	= digital-to-analog	div	= division
		CAL	= calibrate	dB	= decibel	DPDT	= double-pole, double-throw
ASSY	= assembly	ccw	= counterclockwise	dBm	= decibel referred to 1 mW		
AUX	= auxiliary	CER	= ceramic			DR	= drive

Table 6-1. Reference Designations and Abbreviations (Cont'd)

ABBREVIATIONS

DSB	= double sideband
DTL	= diode transistor logic
DVM	= digital voltmeter
ECL	= emitter coupled logic
EMF	= electromotive force
EDP	= electronic data processing
ELECT	= electrolytic
ENCAP	= encapsulated
EXT	= external
F	= farad
FET	= field-effect transistor
F/F	= flip-flop
FH	= flat head
FIL H	= fillister head
FM	= frequency modulation
FP	= front panel
FREQ	= frequency
FXD	= fixed
g	= gram
GE	= germanium
GHz	= gigahertz
GL	= glass
GND	= ground(ed)
H	= henry
h	= hour
HET	= heterodyne
HEX	= hexagonal
HD	= head
HDW	= hardware
HF	= high frequency
HG	= mercury
HI	= high
HP	= Hewlett-Packard
HPF	= high pass filter
HR	= hour (used in parts list)
HV	= high voltage
Hz	= Hertz
IC	= integrated circuit
ID	= inside diameter
IF	= intermediate frequency
IMPG	= impregnated
in	= inch
INCD	= incandescent
INCL	= include(s)
INP	= input
INS	= insulation
INT	= internal
kg	= kilogram
kHz	= kilohertz
kΩ	= kilohm
kV	= kilovolt
lb	= pound
LC	= inductance-capacitance
LED	= light-emitting diode
LF	= low frequency
LG	= long
LH	= left hand
LIM	= limit
LIN	= linear taper (used in parts list)
lin	= linear
LK WASH	= lock washer
LO	= low; local oscillator
LOG	= logarithmic taper (used in parts list)
log	= logarithm(ic)
LPF	= low pass filter
LV	= low voltage
m	= meter (distance)
mA	= milliampere
MAX	= maximum
MΩ	= megohm
MEG	= meg (10^6) (used in parts list)
MET FLM	= metal film
MET OX	= metal oxide
MF	= medium frequency; microfarad (used in parts list)
MFR	= manufacturer
mg	= milligram
MHz	= megahertz
mH	= millihenry
mho	= mho
MIN	= minimum
min	= minute (time)
′	= minute (plane angle)
MINAT	= miniature
mm	= millimeter
MOD	= modulator
MOM	= momentary
MOS	= metal-oxide semiconductor
ms	= millisecond
MTG	= mounting
MTR	= meter (indicating device)
mV	= millivolt
mVac	= millivolt, ac
mVdc	= millivolt, dc
mVpk	= millivolt, peak
mV p-p	= millivolt, peak-to-peak
mVrms	= millivolt, rms
mW	= milliwatt
MUX	= multiplex
MY	= mylar
μA	= microampere
μF	= microfarad
μH	= microhenry
μmho	= micromho
μs	= microsecond
μV	= microvolt
μVac	= microvolt, ac
μVdc	= microvolt, dc
μVpk	= microvolt, peak
μVp-p	= microvolt, peak-to-peak
μVrms	= microvolt, rms
μW	= microwatt
nA	= nanoampere
NC	= no connection
N/C	= normally closed
NE	= neon
NEG	= negative
nF	= nanofarad
NI PL	= nickel plate
N/O	= normally open
NOM	= nominal
NORM	= normal
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NRFR	= not recommended for field replacement
NSR	= not separately replaceable
ns	= nanosecond
nW	= nanowatt
OBD	= order by description
OD	= outside diameter
OH	= oval head
OP AMPL	= operational amplifier
OPT	= option
OSC	= oscillator
OX	= oxide
oz	= ounce
Ω	= ohm
P	= peak (used in parts list)
PAM	= pulse-amplitude modulation
PC	= printed circuit
PCM	= pulse-code modulation; pulse-count modulation
PDM	= pulse-duration modulation
pF	= picofarad
PH BRZ	= phosphor bronze
PHL	= Phillips
PIN	= positive-instrinsic-negative
PIV	= peak inverse voltage
pk	= peak
PL	= phase lock
PLO	= phase lock oscillator
PM	= phase modulation
PNP	= positive-negative-positive
P/O	= part of
POLY	= polystyrene
PORC	= porcelain
POS	= positive; position(s) (used in parts list)
POSN	= position
POT	= potentiometer
p-p	= peak-to-peak
PP	= peak-to-peak (used in parts list)
PPM	= pulse-position modulation
PREAMPL	= preamplifier
PRF	= pulse-repetition frequency
PRR	= pulse repetition rate
ps	= picosecond
PT	= point
PTM	= pulse-time modulation
PWM	= pulse-width modulation
PWV	= peak working voltage
RC	= resistance capacitance
RECT	= rectifier
REF	= reference
REG	= regulated
REPL	= replaceable
RF	= radio frequency
RFI	= radio frequency interference
RH	= round head; right hand
RLC	= resistance-inductance-capacitance
RMO	= rack mount only
rms	= root-mean-square
RND	= round
ROM	= read-only memory
R&P	= rack and panel
RWV	= reverse working voltage
S	= scattering parameter
s	= second (time)
″	= second (plane angle)
S-B	= slow-blow (fuse) (used in parts list)
SCR	= silicon controlled rectifier; screw
SE	= selenium
SECT	= sections
SEMICON	= semiconductor
SHF	= superhigh frequency
SI	= silicon
SIL	= silver
SL	= slide
SNR	= signal-to-noise ratio
SPDT	= single-pole, double-throw
SPG	= spring
SR	= split ring
SPST	= single-pole, single-throw
SSB	= single sideband
SST	= stainless steel
STL	= steel
SQ	= square
SWR	= standing-wave ratio
SYNC	= synchronize
T	= timed (slow-blow fuse)
TA	= tantalum
TC	= temperature compensating
TD	= time delay
TERM	= terminal
TFT	= thin-film transistor
TGL	= toggle
THD	= thread
THRU	= through
TI	= titanium
TOL	= tolerance
TRIM	= trimmer
TSTR	= transistor
TTL	= transistor-transistor logic
TV	= television
TVI	= television interference
TWT	= traveling wave tube
U	= micro (10^{-6}) (used in parts list)
UF	= microfarad (used in parts list)
UHF	= ultrahigh frequency
UNREG	= unregulated
V	= volt
VA	= voltampere
Vac	= volts, ac
VAR	= variable
VCO	= voltage-controlled oscillator
Vdc	= volts, dc
VDCW	= volts, dc, working (used in parts list)
V(F)	= volts, filtered
VFO	= variable-frequency oscillator
VHF	= very-high frequency
Vpk	= volts, peak
Vp-p	= volts, peak-to-peak
Vrms	= volts, rms
VSWR	= voltage standing wave ratio
VTO	= voltage-tuned oscillator
VTVM	= vacuum-tube voltmeter
V(X)	= volts, switched
W	= watt
W/	= with
WIV	= working inverse voltage
WW	= wirewound
W/O	= without
YIG	= yttrium-iron-garnet
Zo	= characteristic impedance

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

6-6. ORDERING INFORMATION

6-7. To order a part listed in the Replaceable Parts table, provide the nearest Hewlett-Packard office with the following information:

1. The Hewlett-Packard part number from the Replaceable Parts table.
2. The quantity required.

6-8. To order a part not listed in the Replaceable Parts table, provide the nearest Hewlett-Packard office with the following information:

1. Instrument model number
2. Complete serial number, including prefix
3. Description and function of the part
4. Quantity required.

6-9. HP PART NUMBER ORGANIZATION

6-10. Following is a general description of the HP part number system.

6-11. Component Parts and Materials

6-12. Generally, the prefix of HP part numbers identifies the type of device. Eight digit part numbers are used, where the four digit prefix identifies the type of component, part, or material and the four digit suffix indicates the specific type. Following is a list of some of the more commonly used prefixes for component parts. The list includes HP manufactured parts and purchased parts.

Prefix	Component/Part/Material
0121--	Capacitors, Variable (mechanical)
0122--	Capacitors, Voltage Variable (semiconductor)
0140--	Capacitors, Fixed } Non-Electrolytic
0150--	Capacitors, Fixed } Non-Electrolytic
0160--	Capacitors, Fixed } Non-Electrolytic
0180--	Capacitors, Fixed Electrolytic
0330--	Insulating Materials
0340--	Insulators, Formed
0370--	Knobs, Control
0380--	Spacers and Standoffs
0410--	Crystals
0470--	Adhesives
0490--	Relays
0510--	Fasteners
0674- thru 0778-	Resistors, Fixed (non wire wound)
0811- thru 0831-	Resistors (wire wound)
1200-	Sockets for components
1205-	Heat Sinks
1250-	Connectors (RF and related parts)
1251-	Connectors (non RF and replated parts)
1410-	Bearings and Bushings
1420-	Batteries
1820-	Monolithic Digital Integrated Circuits
1826-	Monolithic Linear Integrated Circuits
1850-	Transistors, Germanium PNP
1851-	Transistors, Germanium NPN
1853-	Transistors, Silicon PNP
1854-	Transistors, Silicon NPN
1855-	Field-Effect-Transistors
1900- thru 1912-	Diodes
1920- thru 1952-	Vacuum Tubes
1990-	Semiconductor Photosensitive and Light-Emitting Diodes
3100- thru 3106-	Switches
8120-	Cables
9100-	Transformers, Coils, Chokes, Inductors, and Filters

6-13. For example, 1854-0037, 1854-0221, and 1851-0192 are all NPN transistors. The first two are silicon and the last is germanium.

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	59310-60001	1	BOARD ASSEMBLY, BUS I/O	28480	59310-60001
A1C1	0180-0374	2	CAPACITOR-FXD: 10UF+-10% 20VDC TA-SOLID	56289	1500106X902082
A1C2	0160-0153	3	CAPACITOR-FXD 1000PF +-10% 200WVDC POLYE	56289	292P10292
A1C3	0160-0155	1	CAPACITOR-FXD 3300PF +-10% 200WVDC POLYE	56289	292P33292
A1C4	0160-0154	1	CAPACITOR-FXD 2200PF +-10% 200WVDC POLYE	56289	292P22292
A1C5	0160-0207	1	CAPACITOR-FXD .01UF +-5% 200WVDC POLYE	56289	292P10352
A1C6	0160-0157	1	CAPACITOR-FXD 4700PF +-10% 200WVDC POLYE	56289	292P47292
A1C7	0160-0153		CAPACITOR-FXD 1000PF +-10% 200WVDC POLYE	56289	292P10292
A1C8	0160-0153		CAPACITOR-FXD 1000PF +-10% 200WVDC POLYE	56289	292P10292
A1C9	0160-2197	1	CAPACITOR-FXD 10PF +-5% 300WVDC MICA	28480	0160-2197
A1C10	0180-0374		CAPACITOR-FXD: 10UF+-10% 20VDC TA-SOLID	56289	1500106X902082
A1C11	0160-0945	1	CAPACITOR-FXD 910PF +-5% 100WVDC MICA	28480	0160-0945
A1CR1	1901-0040	6	DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1CR2	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1CR3	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1CR4	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1CR5	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1CR6	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1F1	0757-0403	7	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A1R2	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A1R3	0698-3160	1	RESISTOR 31.6K 1% .125W F TC=0+-100	16299	C4-1/8-T0-3162-F
A1R4	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A1R5	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A1R6	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A1R7	0757-0438	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1P8	0683-1525	2	RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
A1R9	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A1R10	0757-0403		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A1R11	1810-0136	2	NETWORK-RES 10-PIN SIP .1-PIN-SPCG	28480	1810-0136
A1R12	0683-1025	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R13	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R14	1810-0020	5	NETWORK-RES 8-PIN SIP .125-PIN-SPCG	28480	1810-0020
A1R15	1810-0020		NETWORK-RES 8-PIN SIP .125-PIN-SPCG	28480	1810-0020
A1R16	1810-0020		NETWORK-RES 8-PIN SIP .125-PIN-SPCG	28480	1810-0020
A1R17	1810-0020		NETWORK-RES 8-PIN SIP .125-PIN-SPCG	28480	1810-0020
A1R18	1810-0020		NETWORK-RES 8-PIN SIP .125-PIN-SPCG	28480	1810-0020
A1R19	0683-1525		RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
A1R20	1810-0041	2	NETWORK-RES 9-PIN SIP .15-PIN-SPCG	28480	1810-0041
A1R21	1810-0041		NETWORK-RES 9-PIN SIP .15-PIN-SPCG	28480	1810-0041
A1R22	1810-0136		NETWORK-RES 10-PIN SIP .1-PIN-SPCG	28480	1810-0136
A1R23	0757-0962	1	RESISTOR 39K 2% .125W F TC=0+-100	24546	C4-1/8-T0-3902-G
A1S1	3101-1797	2		28480	3101-1797
A1S2	3101-1797			28480	3101-1797
A1U13	1820-0054	7	IC SN74 00 N	01295	SN7400N
A1U14	1820-0077	7	IC SN74 74 N	01295	SN7474N
A1U15	1820-0077		IC SN74 74 N	01295	SN7474N
A1U16	1820-0054		IC SN74 00 N	01295	SN7400N
A1U17	1820-0054		IC SN74 00 N	01295	SN7400N
A1U18	1820-1080	11	IC N8T13B	18324	N8T13B
A1U21	1820-0077		IC SN74 74 N	01295	SN7474N
A1U22	1820-0077		IC SN74 74 N	01295	SN7474N
A1U23	1820-1056	3	IC SN74 132 N	01295	SN74132N
A1U24	1820-0077		IC SN74 74 N	01295	SN7474N
A1U25	1820-0077		IC SN74 74 N	01295	SN7474N
A1U26	1820-0328	3	IC SN74 02 N	01295	SN7402N
A1U27	1820-0068	7	IC SN74 10 N	01295	SN7410N
A1U28	1820-1080		IC N8T13B	18324	N8T13B
A1U31	1820-0511	6	IC SN74 08 N	01295	SN7408N
A1U32	1820-0328		IC SN74 02 N	01295	SN7402N
A1U33	1820-0174	2	IC SN74 04 N	01295	SN7404N
A1U34	1820-0077		IC SN74 74 N	01295	SN7474N
A1U35	1820-0328		IC SN74 02 N	01295	SN7402N
A1U36	1820-0068		IC SN74 10 N	01295	SN7410N
A1U37	1820-1056		IC SN74 132 N	01295	SN74132N
A1U38	1820-0054		IC SN74 00 N	01295	SN7400N
A1U41	1820-0515	1	IC MULTIVIBRATOR	07263	9602DC
A1U42	1820-0537	1	IC SN74 13 N	01295	SN7413N
A1U43	1820-0068		IC SN74 10 N	01295	SN7410N
A1U44	1820-0511		IC SN74 08 N	01295	SN7408N
A1U45	1820-0539	1	IC SN74 37 N	01295	SN7437N
A1U46	1820-0054		IC SN74 00 N	01295	SN7400N
A1U47	1820-0511		IC SN74 08 N	01295	SN7408N
A1U48	1820-0511		IC SN74 08 N	01295	SN7408N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1U51	1820-1084	3	IC N8T09B	18324	N8T09B
A1U52	1820-0054		IC SN74 00 N	01295	SN7400N
A1U53	1820-0069	1	IC SN74 20 N	01295	SN7420N
A1U54	1820-0214	2	IC SN74 42 N	01295	SN7442N
A1U56	1820-1100	2	IC SN74 298 N	01295	SN74298N
A1U57	1820-0788	2	IC SN74 174 N	01295	SN74174N
A1U58	1820-1049	3	IC DM80 97N	27014	DM8097N
A1U61	1820-0621	2	IC SN74 38 N	01295	SN7438N
A1U62	1820-0068		IC SN74 10 N	01295	SN7410N
A1U63	1820-1084		IC N8T09B	18324	N8T09B
A1U64	1816-0188	1	IC;DGTL;MEMORY	28480	1816-0188
A1U65	1820-0839	6	IC SN74 175 N	01295	SN74175N
A1U66	1820-1100		IC SN74 298 N	01295	SN74298N
A1U67	1820-0788		IC SN74 174 N	01295	SN74174N
A1U68	1820-1049		IC DM80 97N	27014	DM8097N
A1U71	1820-1056		IC SN74 132 N	01295	SN74132N
A1U72	1820-1053	5	IC SN74 14 N	01295	SN7414N
A1U73	1820-1084		IC N8T09B	18324	N8T09B
A1U74	1820-1080		IC N8T13B	18324	N8T13B
A1U75	1820-0084	1	IC SN74 53 N	01295	SN7453N
A1U76	1820-0839		IC SN74 175 N	01295	SN74175N
A1U77	1820-0839		IC SN74 175 N	01295	SN74175N
A1U78	1820-1049		IC DM80 97N	27014	DM8097N
A1U81	1820-1053		IC SN74 14 N	01295	SN7414N
A1U82	1820-0068		IC SN74 10 N	01295	SN7410N
A1U83	1820-1053		IC SN74 14 N	01295	SN7414N
A1U84	1820-0070	2	IC SN74 30 N	01295	SN7430N
A1U85	1820-1082	1	IC SN74 147 N	01295	SN74147N
A1U87	1820-1080		IC N8T13B	18324	N8T13B
A1U88	1820-1080		IC N8T13B	18324	N8T13B
A1U91	1820-0621		IC SN74 38 N	01295	SN7438N
A1U92	1820-0054		IC SN74 00 N	01295	SN7400N
A1U93	1820-0214		IC SN74 42 N	01295	SN7442N
A1U94	1820-1053		IC SN74 14 N	01295	SN7414N
A1U95	1820-0174		IC SN74 04 N	01295	SN7404N
A1U96	1820-0839		IC SN74 175 N	01295	SN74175N
A1U97	1820-1080		IC N8T13B	18324	N8T13B
A1U98	1820-1080		IC N8T13B	18324	N8T13B
A1U102	1820-0511		IC SN74 08 N	01295	SN7408N
A1U103	1820-0068		IC SN74 10 N	01295	SN7410N
A1U104	1820-0068		IC SN74 10 N	01295	SN7410N
A1U105	1820-1053		IC SN74 14 N	01295	SN7414N
A1U106	1820-0839		IC SN74 175 N	01295	SN74175N
A1U107	1820-1080		IC N8T13B	18324	N8T13B
A1U108	1820-1080		IC N8T13B	18324	N8T13B
A1U113	1820-0706	1	IC COMPARATOR	07263	93240C
A1U114	1820-0070		IC SN74 30 N	01295	SN7430N
A1U115	1820-0511		IC SN74 08 N	01295	SN7408N
A1U116	1820-0839		IC SN74 175 N	01295	SN74175N
A1U117	1820-1080		IC N8T13B	18324	N8T13B
A1U118	1820-1080		IC N8T13B	18324	N8T13B
			A1 MISCELLANEOUS		
	0360-0124	7	.040 040	28480	0360-0124
	1200-0475	80	CONNECTOR:1-CONT SKT .016 DIA	22526	75060-005
	1260-0545	1		28480	1260-0545
	1260-0546	1		28480	1260-0546
	3101-0538	2		28480	3101-0538
	5040-6001	1	EXTRACTOR, P.C. BOARD	28480	5040-6001
	59310-60003	1	HEADER ASSEMBLY	28480	59310-60003
	59310-80001	1	EXTRACTOR, "BUS I/O"	28480	59310-80001
A2	59310-60002	1	CABLE ASSEMBLY, BUS I/O	28480	59310-60002
	8120-1927	1	CABLE ASSEMBLY, 24-PIN	28480	8120-1927
	5060-8339	1	CONNECTOR, P.C. BOARD	28480	5060-8339
			A1 AND A2 MISCELLANEOUS		
	59310-60010	1	TAPE-DIAGNOSTIC	28480	59310-60010
	59310-60020	1	TAPE-DRIVER .037A	28480	59310-60020
	59310-60021	1	TAPE-DRIVER .037B	28480	59310-60021
	59310-60050	1	TAPE-BUS LIB	28480	59310-60050
	59310-90007	1	MANUAL-OPERATING	28480	59310-90007
	59310-90022	1	MANUAL-BCS DRIVER	28480	59310-90022
	59310-90050	1	MANUAL-BCS BUS	28480	59310-90050
	59310-90058	1	MANUAL-DIAGNOSTIC	28480	59310-90058

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			OPTION 801 - 59310A H-P INTERFACE BUS COMPUTER I/O KIT INCLUDES:		
	59310-60011	1	TP-BICOM REL	28480	59310-60011
	59310-60012	1	TP-BDUS	28480	59310-60012
	59310-60014	1	TP-EQTSC	28480	59310-60014
	59310-60051	1	TP-BLIB	28480	59310-60051
	59310-60052	1	TP-REMOT	28480	59310-60052
	59310-60053	1	TP-LOCAL	28480	59310-60053
	59310-60054	1	TP-DEVCL	28480	59310-60054
	59310-60055	1	TP-CMD	28480	59310-60055
	59310-60056	1	TP-READOUT	28480	59310-60056
	59310-60057	1	TP-CIOC	28480	59310-60057
	59310-60013	1	TP-BDTS	28480	59310-60013
			OPTION S01 - 59310A H-P INTERFACE BUS COMPUTER BUS I/O KIT INCLUDES:		
	59310-80011	1	TP-BICOM SOR	28480	59310-80011
	59310-80012	1	TP-BDUS SOR	28480	59310-80012
	59310-80013	1	TP-BDTS SOR	28480	59310-80013
	59310-80014	1	TP-EQTSC SOR	28480	59310-80014
	59310-80020	1	TP-D37A/B SOP	28480	59310-80020
	59310-80051	1	TP-BLIB SOR	28480	59310-80051
	59310-80052	1	TP-REMOTE SOR	28480	59310-80052
	59310-80053	1	TP-LOCI SOR	28480	59310-80053
	59310-80054	1	TP-DEVCL SOR	28480	59310-80054
	59310-80055	1	TP-CMD SOR	28480	59310-80055
	59310-80056	1	TP-READOUT SOR	28480	59310-80056
	59310-80057	1	TP-CIOC SOR	28480	59310-80057

See introduction to this section for ordering information

Table 6-3. Manufacturers Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
01121	ALLEN BRADLEY CO	MILWAUKEE, WI	53212
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS, TX	75231
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW, CA	94040
16299	CORNING GL WK ELEC CMPNT DIV	RALEIGH, NC	27604
18324	SIGNETICS CORP	SUNNYVALE, CA	94086
22526	BERG ELECTRONIC INC	CUMBERLAND, PA	17070
24546	CORNING GLASS WORKS (BRADFORD	BRADFORD, PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA, CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO, CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS, MA	01247

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to older instruments.

7-3. MANUAL CHANGES

7-4. This manual applies directly to Model 59310A having series number 1348A (refer to paragraph 1-8).

7-5. Newer Instruments

7-6. As changes are made, newer instruments may have series numbers that are not listed in this manual. The manuals for these instruments are supplied with a manual change sheet, containing the required information. Contact the nearest Hewlett-Packard Sales and Service Office for information if this sheet is missing.

7-7. Older Instruments

7-8. To adapt this manual to bus I/O cards having series numbers lower than 1348A, refer to Table 7-1 for backdating that applies to your series number.

Table 7-1. Manual Backdating

Series Number	Make Change
1324A	1
1312A	1,2

CHANGE 1

a. Make the following changes to the schematic diagram, Figure 8-3, Sheet 1.

(1) At the lower right side of the diagram, disconnect the enable inputs of U51(2), U63(4,2,12,10), and U73(4,2,12,10) from U31(13) and connect to U31(11). Delete U51B from the diagram.

(2) At the center of the diagram, disconnect U24(3) from U14(11) and connect to U24(11). Delete U102 and transfer its output signal labels to U24(5).

(3) At the upper left of the diagram, on the output of U76(15) add "TO U74(1,2)".

b. Make the following changes to the schematic diagram Figure 8-3, Sheet 2.

(1) At the lower right of the diagram, delete U74 and R15, a 1.5K resistor, connected to the output. Connect U25(9) to U82(9). Remove the connection from U34(8) to U34(10).

c. In Table 6-1, Replaceable Parts, delete R15.

CHANGE 2

a. Make the following changes to the schematic diagram Figure 8-3, Sheet 1.

(1) Disconnect the connection from U24(3) to U14(11) and connect toU24(11). Disconnect the connection from U14(5) to U24(3).

SECTION VIII

SCHEMATIC DIAGRAMS

8-1. INTRODUCTION

8-2. This section contains information for schematic diagram notes, reference designation system, identification markings on PC board, an overall block diagram, schematic simplified logic diagram and component locator. The schematic includes a table of active elements giving HP and vendor part numbers.

8-3. SCHEMATIC DIAGRAM NOTES

8-4. Figure 8-1 shows the symbols used on the schematic diagrams. Notes are also included on each schematic diagram.

8-5. IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS

8-6. HP printed circuit boards (see Figure 8-1) have four identification numbers; an assembly part numbers, a series number, a revision letter, and a production code.

8-7. The assembly part number has 10 digits (such as 05340-60037) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 1548A) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed-circuit board is lower than that on the schematic, refer to Section VII for back dating information. If it is higher, refer to the loose leaf manual change sheets for this manual. If the manual change sheets are missing, contact your local Hewlett-Packard Sales and Service Office. See the listing on the back cover of this manual.

8-8. Revision letters (A,B, etc.) denote changes in printed circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes, the series number is also usually changed. The production code is the four digit, seven segment number used for production purposes.

8-9. Symbols are used on PC boards to aid in identifying pin numbers, diode elements etc. as follows:

Δ OR □	**IDENTIFIES:**	Pin 1 of dip and flat-pack IC's. Tab of TO cases. + side of electrolytic capacitors. Pin 1 of resistor packs. Cathode of diodes. Section 1 of dip switches.

8-10. COMPONENT LOCATORS

8-11. Figure 8-3 component locator for the printed circuit assembly are next to the schematic.

Figure 8-1. Schematic Diagram Notes

SYMBOLS

FRONT PANEL

REAR PANEL

INTERIOR AND PC BOARDS

WIPER MOVES TOWARD "CW" WHEN CONTROL IS ROTATED CLOCKWISE

POWER LINE GROUND

CIRCUIT COMMON GROUND

FLOATING GROUND

CHASSIS GROUND

KNOB CONTROL

SCREWDRIVER ADJUST

MAIN SIGNAL PATH

FEEDBACK PATH

TEST POINT

"AND" GATE

"OR" GATE

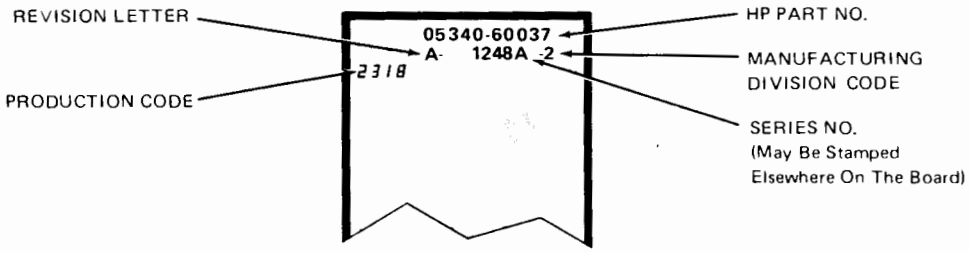
INVERTER

NAND GATE

NOR GATE

EXCLUSIVE NOR

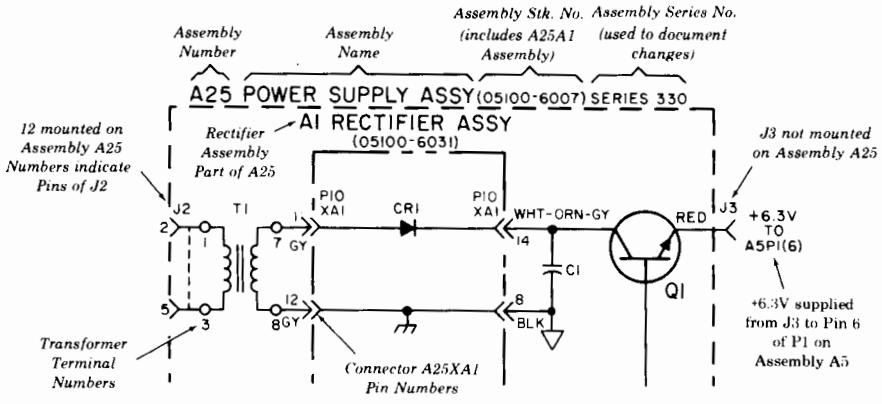
PRINTED CIRCUIT BOARD IDENTIFICATION



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3



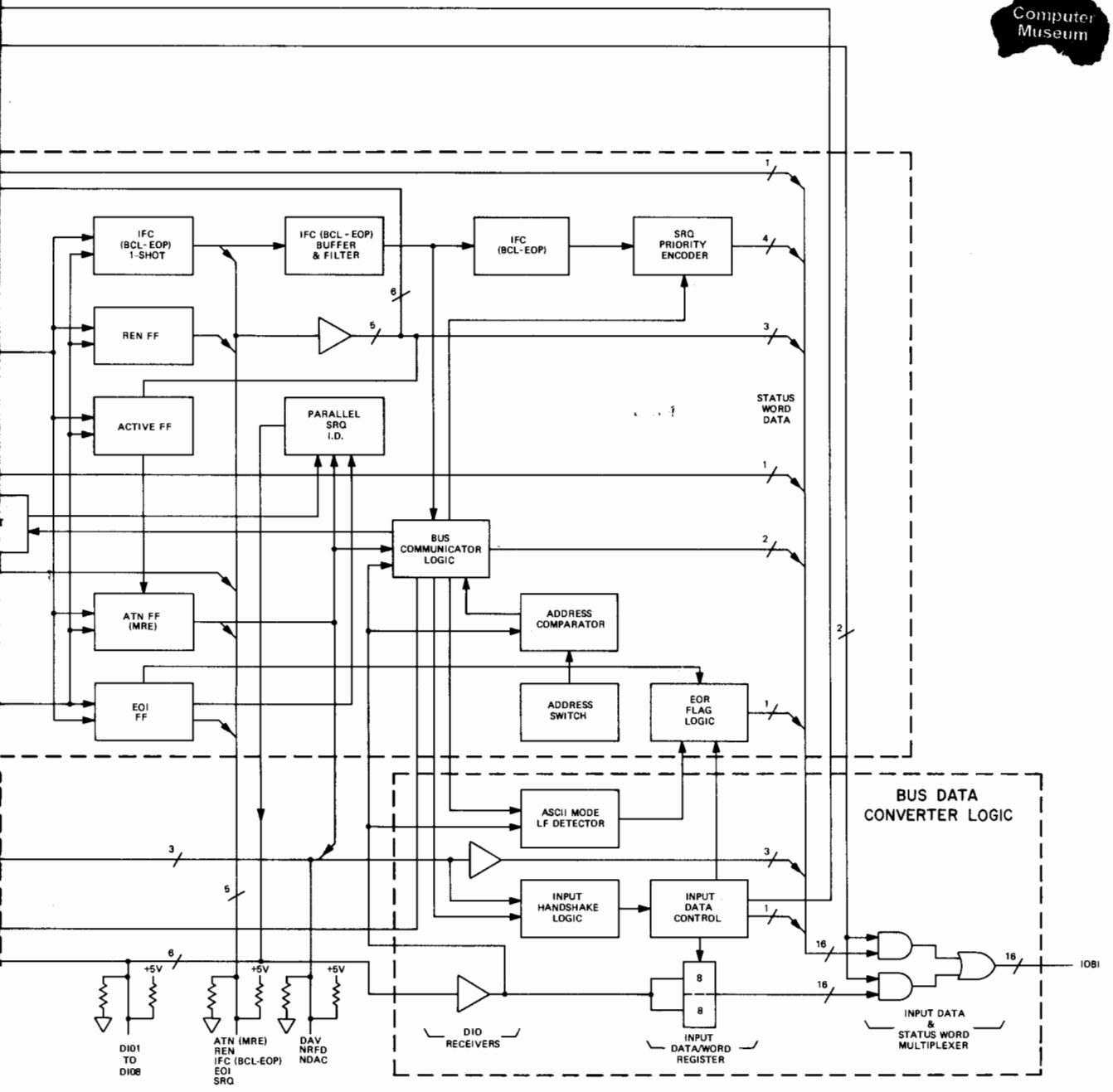
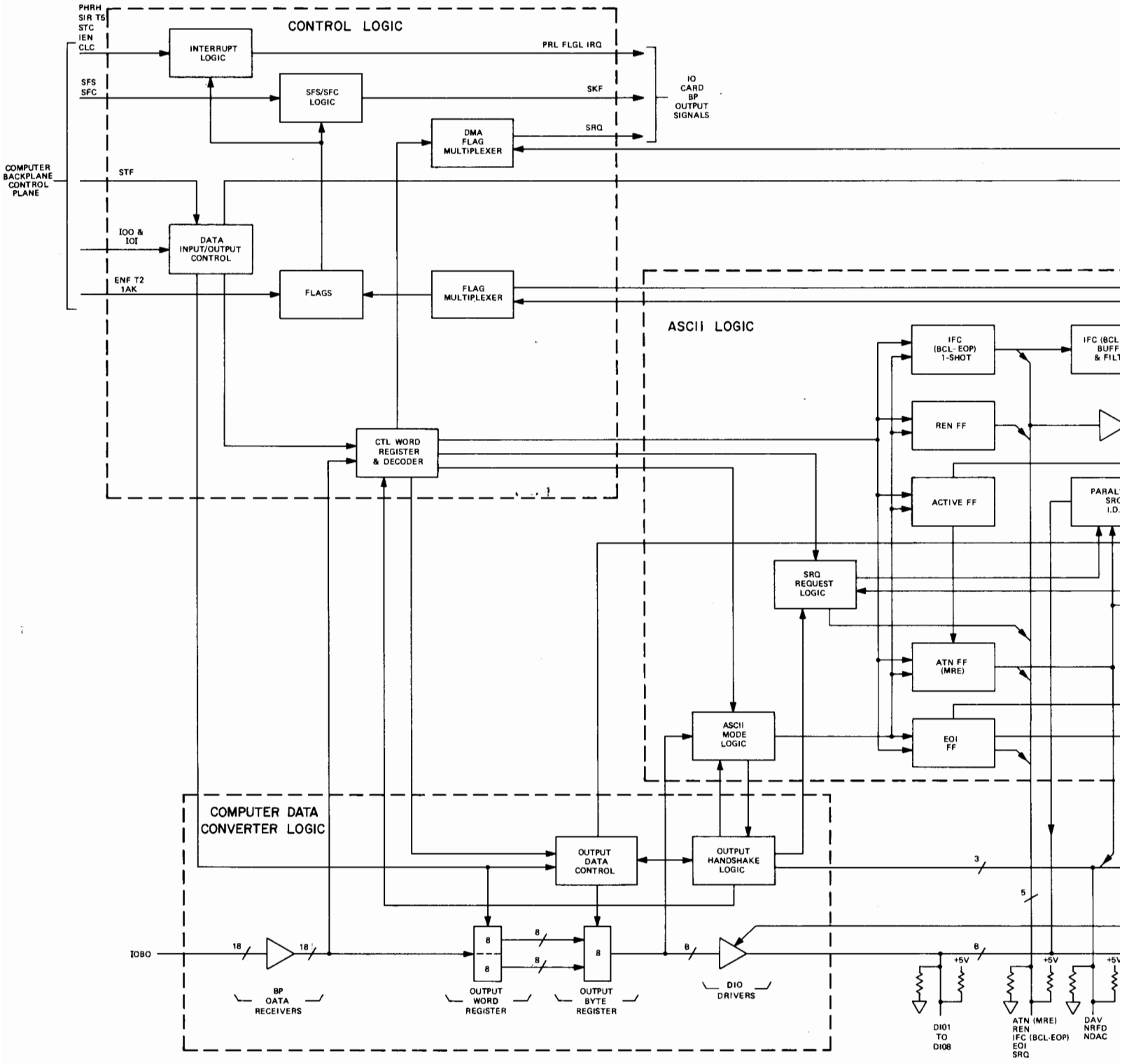
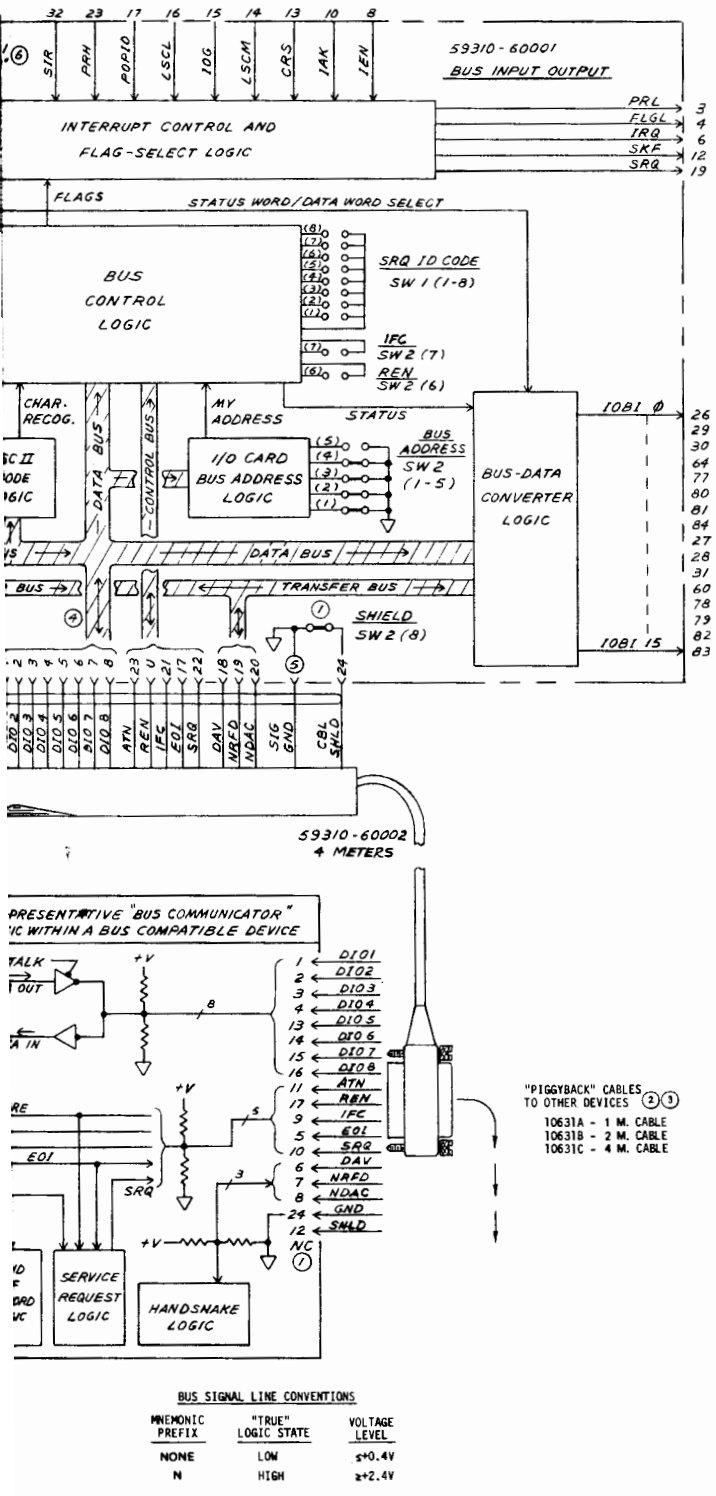


Figure 8-2. 59310A Block Diagram


CONTROL LOGIC
PHRH
SIR T5
STC
IEN
CLC
INTERRUPT LOGIC
PRL FLGL IRQ
SFS
SFC
SFS/SFC LOGIC
SKF
IO CARD BP OUTPUT SIGNALS
DMA FLAG MULTIPLEXER
SRQ
COMPUTER BACKPLANE CONTROL PLANE
STF
IOO & IOI
DATA INPUT/OUTPUT CONTROL
ENF T2 1AK
FLAGS
FLAG MULTIPLEXER
ASCII LOGIC
IFC (BCL-EOP) 1-SHOT
REN FF
ACTIVE FF
CTL WORD REGISTER & DECODER
SRQ REQUEST LOGIC
ATN FF (MRE)
ASCII MODE LOGIC
EOI FF
COMPUTER DATA CONVERTER LOGIC
OUTPUT DATA CONTROL
OUTPUT HANDSHAKE LOGIC
IOBO
18
BP DATA RECEIVERS
8
OUTPUT WORD REGISTER
OUTPUT BYTE REGISTER
DIO DRIVERS
+5V
DI01 TO DI08
ATN (MRE) REN IFC (BCL-EOP) EOI SRQ
DAV NRFD NDAC



BUS SIGNAL LINE CONVENTIONS

MNEMONIC PREFIX	"TRUE" LOGIC STATE	VOLTAGE LEVEL
NONE	LOW	≤+0.4V
N	HIGH	≥+2.4V

TEST-POINTS

I/O CARD CONTROL WORD BIT #'s	CONTROL WORD FUNCTION	TEST-POINT TO VERIFY ACTION: ACCESS PT. ON CARD ⑤	CABLE PIN: I/O	CABLE PIN: BUS	STATUS WD. BIT
2 - Ø	IFC (100µs)	U41 (6) ⊓⊔	21	9	-
	REN	U43 (6) ⊓	U	17	8
	ACTIVE	U21 (9) ⌋	-	-	4
	FORCE INPUT CYCLE	U54 (7) ⊔	-	-	-
	CLEAR I/O CARD	U54 (9) ⊓⊔	-	-	-
6 - 3	ATN	U21 (5) ⌈	23	11	7
	EOI	U22 (6) ⌊	17 ⑦	5 ⑦	-
	TALK	TP-2 ⌈	-	-	5
	LISTEN	TP-3 ⌋	-	-	6
11 - 8 (BIT 7 ENABLES)	ASCII MODE	U65 (10) ⌋	-	-	-
	SRQ ENABLE	U65 (15) ⌋	22 ⑦	10 ⑦	-
	DMA R/W SELECT	U65 (2) ⌈	-	-	-
	PACKING/ UNPACKING	U65 (7) ⌋	-	-	-
15 - 12 (BIT 7 ENABLES)	EOR FLAG EN.	U76 (15) ⌐	-	-	12
	ORA FLAG EN.	U76 (10) ⌐	-	-	13
	IRL FLAG EN.	U76 (7) ⌐	-	-	14
	SEP FLAG EN.	U76 (2) ⌐	-	-	15

NOTES:

① The cable shield is grounded only once, and is done at the System Controller.

② The maximum accumulated cable length (per bus) is 20 meters, total.

③ A bus cable network must not exceed an average of one "standard load" device for each 2 meters of bus cable; i.e.:

$$\frac{\text{TOTAL CABLE LENGTH}}{\text{NUMBER OF DEVICES}} < 2 \text{ meters/device}$$

Remember that the I/O card must be counted as one of the devices.

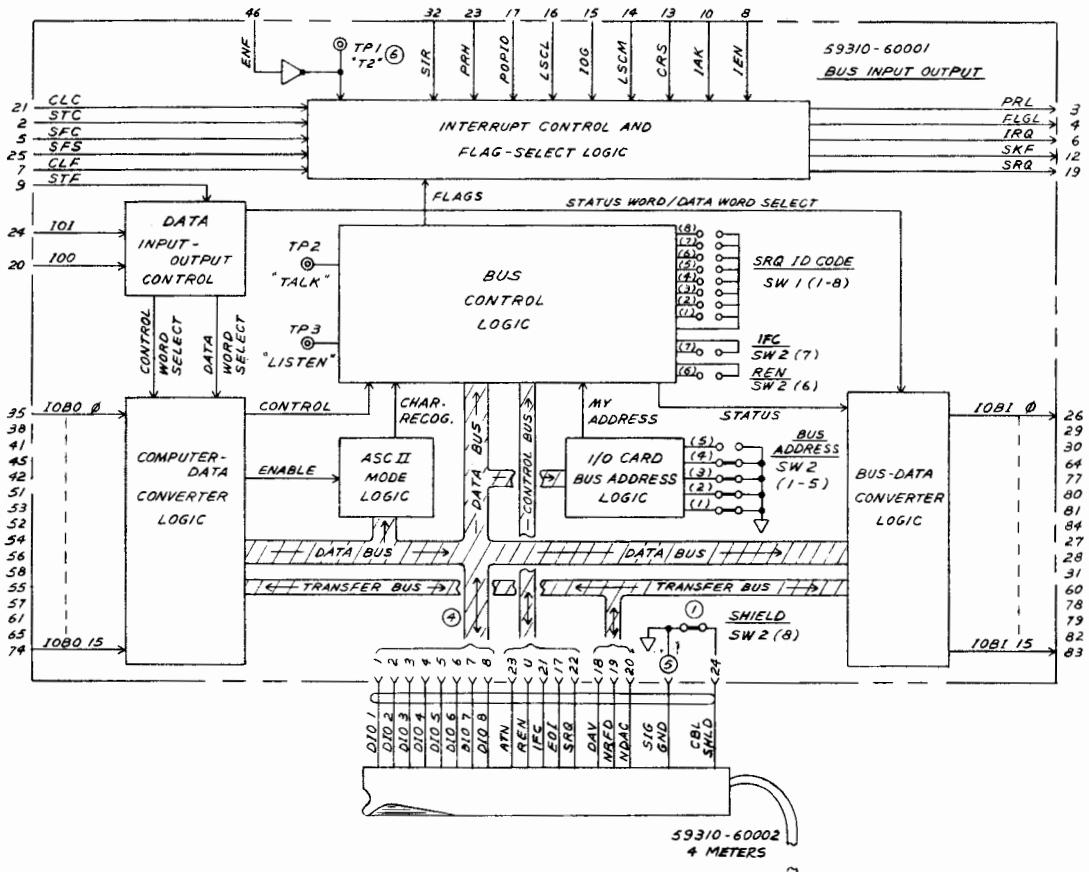
④ The I/O card's circuitry has one "Standard Load" on each bus signal line.

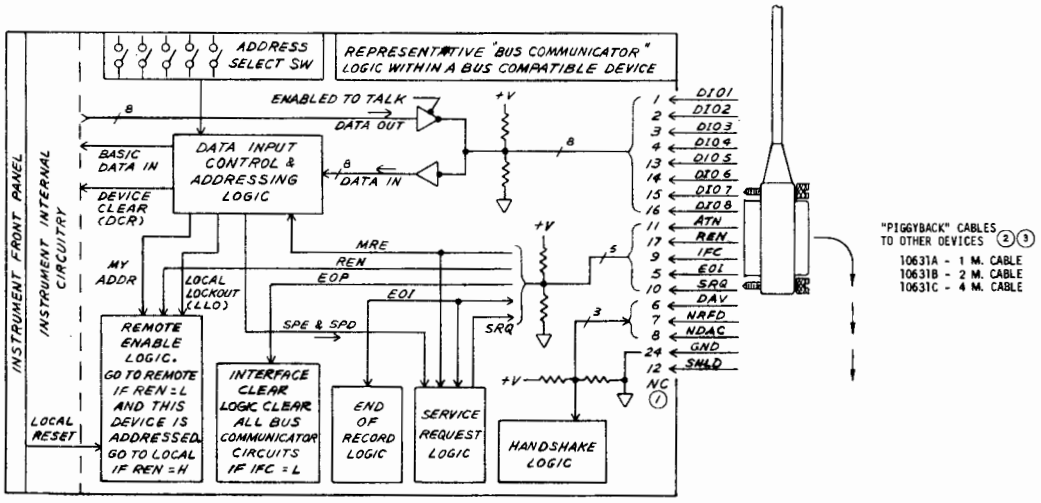
⑤ Bus cable signal grounds are connected to I/O card common at connector pins V,W,X,Y,Z,AA and BB.

⑥ Use TP-1 (2100 time "t2") to sync 'scope for dynamic tests.

⑦ State of these signal lines is dependent on other I/O card functions that are programmed.

Figure 8-3. 59310A Simplified Logic Diagram (Sheet 1 of 2)





BUS SIGNAL LINE CONVENTIONS

MNEMONIC PREFIX	"TRUE" LOGIC STATE	VOLTAGE LEVEL
NONE	LOW	≤+0.4V
N	HIGH	≥+2.4V

I/O CARD CONTROL WORD BIT #'s	CONTROL WORD FUNCTION
2 - Ø	IFC (100us) REN ACTIVE FORCE INPUT CYCLE CLEAR I/O CA
6 - 3	ATN EOI TALK LISTEN
11 - 8 (BIT 7 ENABLES)	ASCII MODE SRQ ENABLE DMA R/W SELE PACKING/ UNPACKING
15 - 12 (BIT 7 ENABLES)	EOR FLAG EN. ORA FLAG EN. IRL FLAG EN. SEP FLAG EN.

NOTES:

(1) The cable shield is grounded only

(2) The maximum accumulated cable leng

(3) A bus cable network must not excee for each 2 meters of bus cable; i.e.:

$$\frac{\text{TOTAL CABLE LENGTH}}{\text{NUMBER OF DEVICES}} \leq 2 \text{ me}$$

Remember that the I/O card must be

(4) The I/O card's circuitry has one "

(5) Bus cable signal grounds are conne V,W,X,Y,Z,AA and BB.

(6) Use TP-1 (2100 time "t2") to sync

(7) State of these signal lines is dep

Figure 8-3. 59310A Simplif

```
PAGE 0002 #01  AMD 59310A GPIB SUBSYSTEM TOGGLE TEST PROGRAM


0001                ASMB,A,B,L
0003  00100             ORG 100B
0004*
0005*       THIS TOGGLE PROGRAM PROVIDES FOR COMPLETE FUNCTION
0006*       PROGRAMMING OF THE 59310-69001 BUS I/O CARD, PLUS
0007*       CONTROL OF INDIVIDUAL SIGNAL LINES WITHIN THE BUS
0008*       CABLE.  IT MAY BE RUN WITH OR WITHOUT INSTRUMENTS
0009*       ON THE BUS.
0010*
0011*       SPECIFIC BIT PATTERNS ARE ENTERED VIA THE COMPUTER'S
0012*       FRONT PANEL REGISTERS, BOTH AS CONTROL WORDS TO THE
0013*       I/O CARD AND AS DATA WORDS TO THE BUS DIO SIGNAL LINES.
0014*
0015*       THE PROGRAM RETURNS THE I/O CARD'S STATUS WORD
0016*       IN THE B REGISTER.
0017*
0018*       ACTION CAUSED BY SPECIFIC CONTROL WORDS CAN BE CHECKED
0019*       AT ACCESS POINTS ON THE I/O CARD, AT THE CABLE
0020*       CONNECTORS AND/OR IN THE STATUS WORD RETURNED IN THE
0021*       B REGISTER.
0022*
0023*       TEST EQUIPMENT FOR CONVENIENCE IN LOGIC LEVEL TESTING:
0024*             LOGIC PROBE      LOGIC CLIP     FIXTURE FOR BUS CABLE
0025*             HP 10529T        HP 10528A      HP P/N 5060-0124
0026*
0027*
0028*       TO USE THIS PROGRAM:
0029*       1. LOAD THE PROGRAM BELOW, USING THE COMPUTER FRONT
0030*          PANEL CONTROLS AND ENTERING THE I/O CARD'S
0031*          SELECT CODE (SC) WHERE REQUIRED.
0032*       2. SET STARTING ADDRESS = 100 OCTAL, AND PRESS
0033*          BOTH PRESET BUTTONS.
0034*       3. SET CONTENTS OF THE REGISTERS AS APPROPRIATE:
0035*             DATA TO THE BUS DIO SIGNAL LINES = - - - B REG.
0036*             CONTROL WORD TO THE BUS I/O CARD = - - - A REG.
0037*
0038*          NOTES: THE FIRST WORD OUTPUT TO THE 59310A
0039*                 FOLLOWING A 'STC SC,C' INSTRUCTION IS
0040*                 ALWAYS CONSIDERED TO BE A CONTROL WORD.
0041*                 ANY SUBSEQUENT WORDS ARE TREATED AS DATA
0042*                 UNTIL ANOTHER 'STF SC' INSTRUCTION IS
0043*                 ENCOUNTERED.
0044*
0045*                 THE DATA IN THE SWITCH REG. IS OFFSET ONE
0046*                 PLACE FROM THE DIO LINES FOR CONVENIENCE IN
0047*                 USING OCTAL FORMAT; I.E., BIT 0 OF THE
0048*                 B REG. = DIO LINE 1, BIT 1 OF B REG. = DIO 2,
0049*                 ETC.
0050*
0051*       4. PRESS 'RUN', THE PROGRAM HALTS.
0052*          OBSERVE I/O CARD'S STATUS WORD = - - - B REG.
0053*       5. NOTE THAT THE DIO LINES ARE SET ONLY IF THE I/O
0054*          CARD IS PROGRAMMED TO 'TALK' OR 'NRE'; IS SET LOW.
0055*       6. OBSERVE OTHER RESULTS, AND REPEAT STEPS 3-6
0056*          AS APPROPRIATE.
0057*
0058*
0059  00100 004114  START LDB 97          SET CLEAR CODE
0060  00101 102177        STF 8C          CLEAR I/O FOR USE W/O HANDSHAKE
0061  00102 106677        OTB 8C
0062  00103 106577        LIB 8C          GET STATUS/READY I/O CARD
0063  00104 102177        STF 8C          RELEASE CARD FROM CLEAR MODE
0064  00105 102677        OTA 8C          SEND A REG AS CONTROL WORD
0065  00106 106501        LIB 1           GET DW REG
0066  00107 107677        OTB 8C,C        SEND DATA TO I/O LINES
0067  00110 102177        STF 8C
0068  00111 106577        LIB 8C          GET STATUS WD FROM I/O CARD
0069  00112 102000        HLT 00          (NOP FOR CONTINUOUS LOOPING)
0070  00113 004100        JMP START
0071*
0072  00114 000007  97    OCT 7           CODE TO CLEAR I/O CARD
0073  00077         8C    EQU 77B         SELECT CODE OF I/O CARD
0074*
0075                      END
**  NO ERRORS: AMD ASMB,B5117-482518
```

NOTES

(A) Data is put on the DIO Signal Lines only if the I/O card is programmed to TALK, or if the ATN line is programmed LOW.

(B) ESCAPE (ESC) Key on HP 2754B (ASR-35) is OCT 176; to get OCT 33, Press CTRL-SHIFT-K.

Figure 8-3. 59310A Simplified Logic Diagram (Sheet 2 of 2)

I/O CARD ASCII-MODE FUNCTIONS			
	CODE		
FUNCTION	ASCII (TTY KEY)	OCTAL	DECIMAL
EOP (100μs)	ESC (ESC) (B)	33	27.
REN = L	STX (CTRL-B)	2	2.
= H	ETX (CTRL-C)	3	3.
ATN = L	SO (CTRL-N)	16	14.
= H	SI (CTRL-O)	17	15.

GENERAL BUS-CODE ALLOCATIONS WITHIN THE ASCII-CODE SET

DIO LINES				UNIVERSAL BUS COMMANDS				DEVICE LISTEN ADDRESS				DEVICE TALK ADDRESS			
8	7	6	5	X [H H] H				X [H H] L				X [L H] H			
				COLUMN → Ø				1				2			
4	3	2	1	ROW	OCTAL	DECIMAL	BUS COMMAND	OCTAL	DECIMAL	BUS COMMAND		OCTAL	DECIMAL	SYMBOLIC ADDRESS	
H	H	H	H	0	Ø	0.		2Ø	16.			4Ø	32.	SP	
H	H	H	L	1	1	1.		21	17.	LLO		41	33.	!	
H	H	L	H	2	2	2.		22	18.	R*		42	34.	"	
H	H	L	L	3	3	3.		23	19.	R*		43	35.	#	
H	L	H	H	4	4	4.		24	20.	DCR		44	36.	$	
H	L	H	L	5	5	5.		25	21.			45	37.	%	
H	L	L	H	6	6	6.		26	22.			46	38.	&	
H	L	L	L	7	7	7.		27	23.			47	39.	'	
L	H	H	H	8	1Ø	8.		3Ø	24.	SPE		5Ø	4D.	(	
L	H	H	L	9	11	9.		31	25.	SPD		51	41.	)	
L	H	L	H	10	12	10.		32	26.			52	42.	*	
L	H	L	L	11	13	11.		33	27.			53	43.	+	
L	L	H	H	12	14	12.		34	28.	R*		54	44.	,	
L	L	H	L	13	15	13.		35	29.	R*		55	45.	-	
L	L	L	H	14	16	14.		36	30.			56	46.	.	
L	L	L	L	15	17	15.		37	31.			57	47.	/	

DEVICE LISTEN ADDRESS				DEVICE TALK ADDRESS			
X [H L] L				X [L L] H			
3				4			
OCTAL	DECIMAL	SYMBOLIC ADDRESS		OCTAL	DECIMAL	SYMBOLIC ADDRESS	
6Ø	48.	D		1ØØ	64.	@	
61	49.	1		1Ø1	65.	A	
62	5D.	2		1Ø2	66.	B	
63	51.	3		1Ø3	67.	C	
64	52.	4		1Ø4	68.	D	
65	53.	5		1Ø5	69.	E	
66	54.	6		1Ø6	70.	F	
67	55.	7		1Ø7	71.	G	
7Ø	56.	8		11Ø	72.	H	
71	57.	9		111	73.	I	
72	58.	:		112	74.	J	
73	59.	;		113	75.	K	
74	60.	<		114	76.	L	
75	61.	=		115	77.	M	
76	62.	>		116	78.	N	
77	63.	?		117	79.	O	
UNLISTEN COMMAND							

DEVICE TALK ADDRESS			
X [L L] L			
5			
OCTAL	DECIMAL	SYMBOLIC ADDRESS	
12Ø	80.	P	
121	81.	Q	
122	82.	R	
123	83.	S	
124	84.	T	
125	85.	U	
126	86	V	
127	87.	G	
13Ø	88.	X	
131	89.	Y	
132	90.	Z	
133	91.	[	
134	92.	\	
135	93.	]	
136	94.	^	
137	95.	_	
UNTALK COMMAND			

H = High State.
L = Low State.
X = Unused when MRE is low.
[ ] = Control Bits.

LLO = Local Lockout.
DCR = Device Clear.
R* = Reserved for future assignment

NOTE THAT ASCII COLUMNS 6 AND 7 ARE NOT USED.

SPE = Status Poll Enable.
SPD = Status Poll Disable.
DIO = Data Input Output Signal Lines, DIO1-8

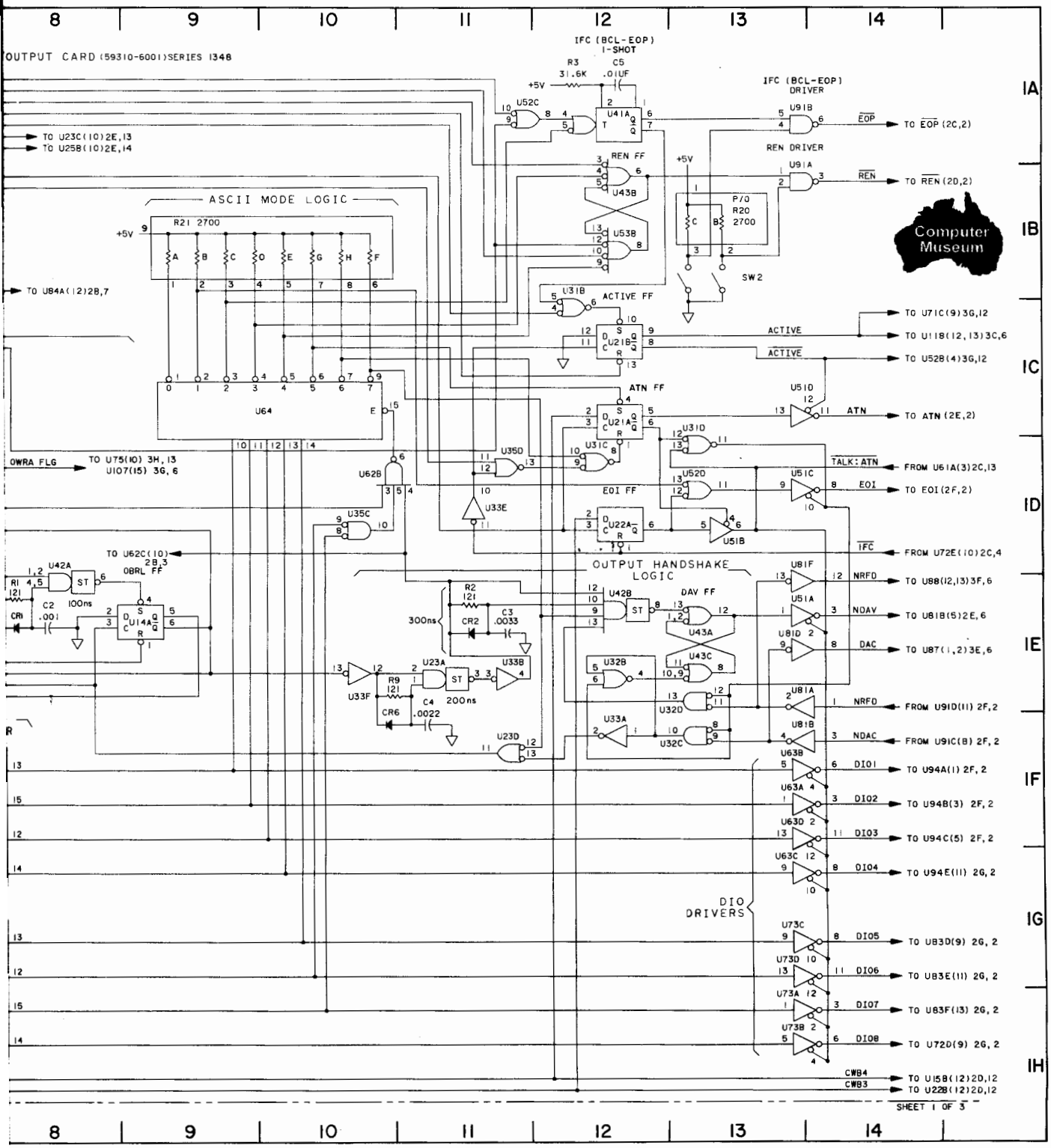
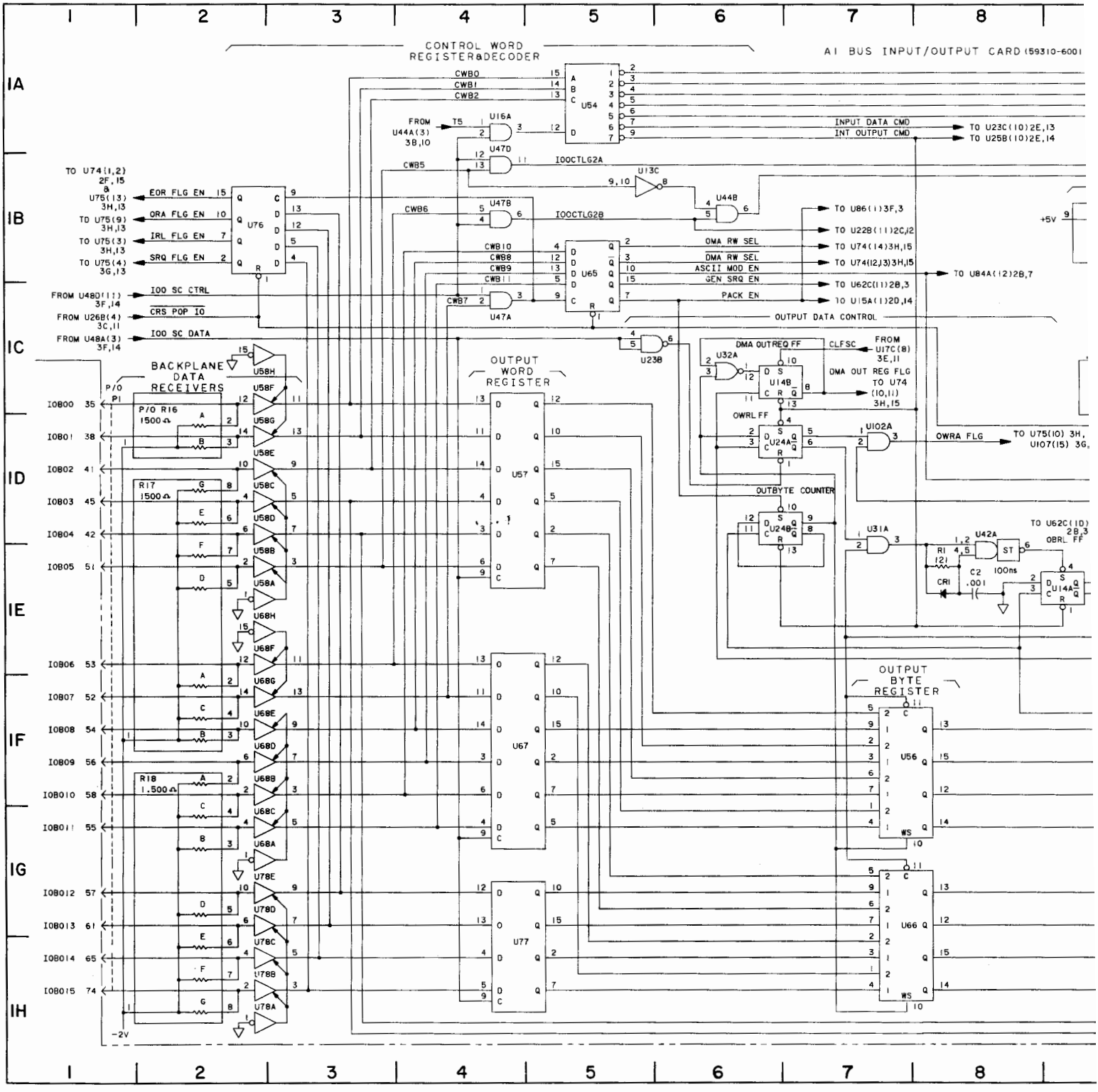


Figure 8–5. 59310A Schematic Diagram (Sheet 1 of 3)



NOTE: "TO-FROM" legends give locations corresponding to numbered grids around schematic edges. "3H, 16" means: sheet 3, row H, column 16.

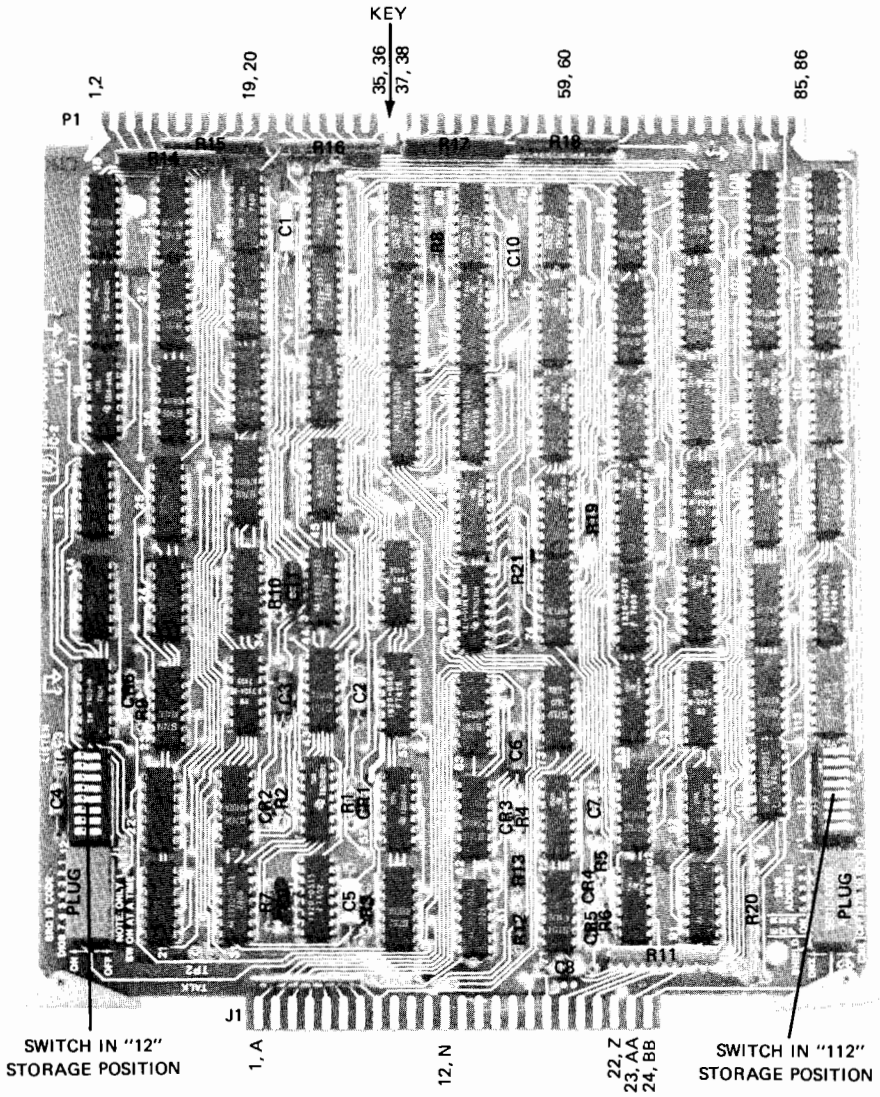


Figure 8–4. Component Locator

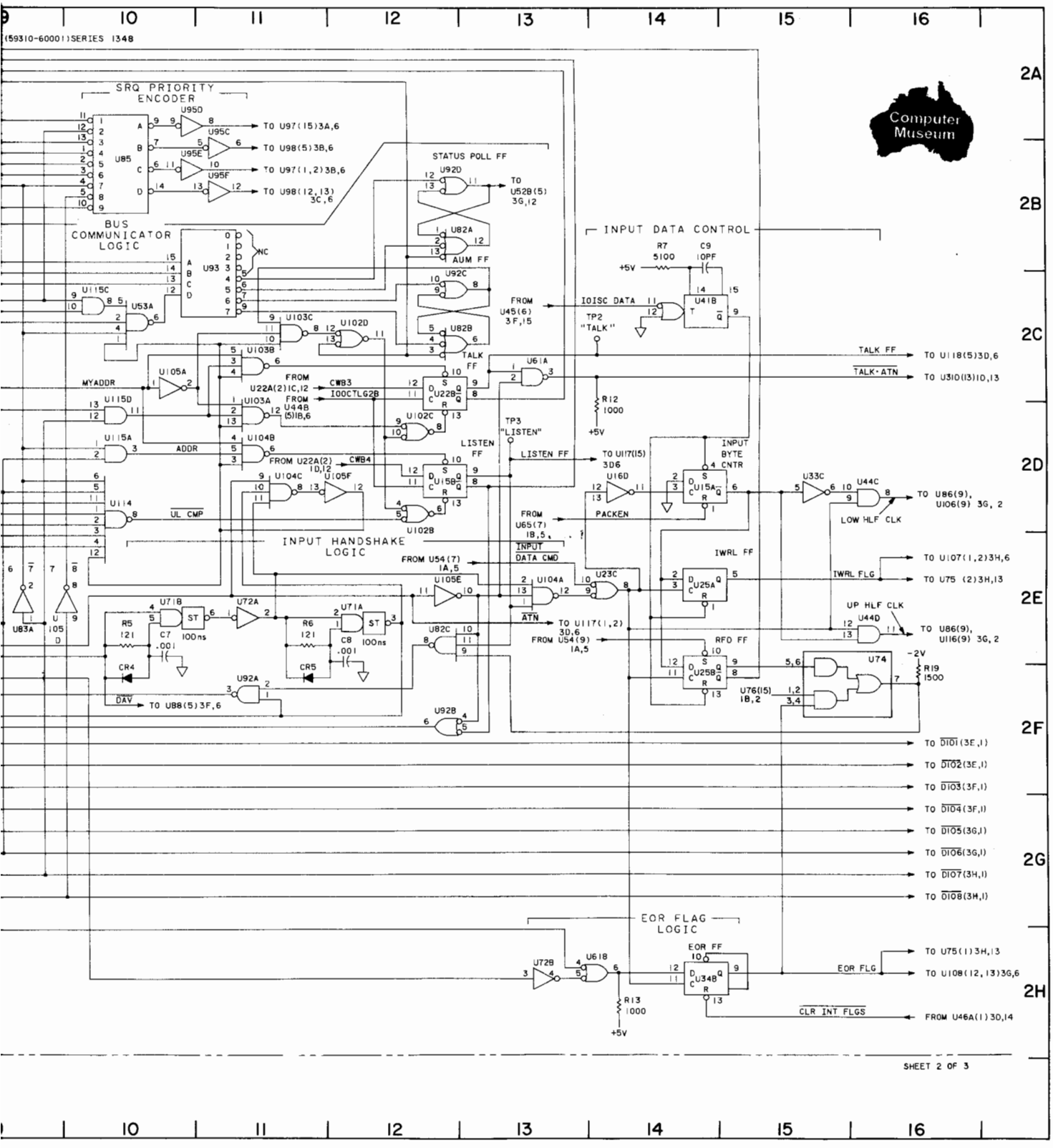
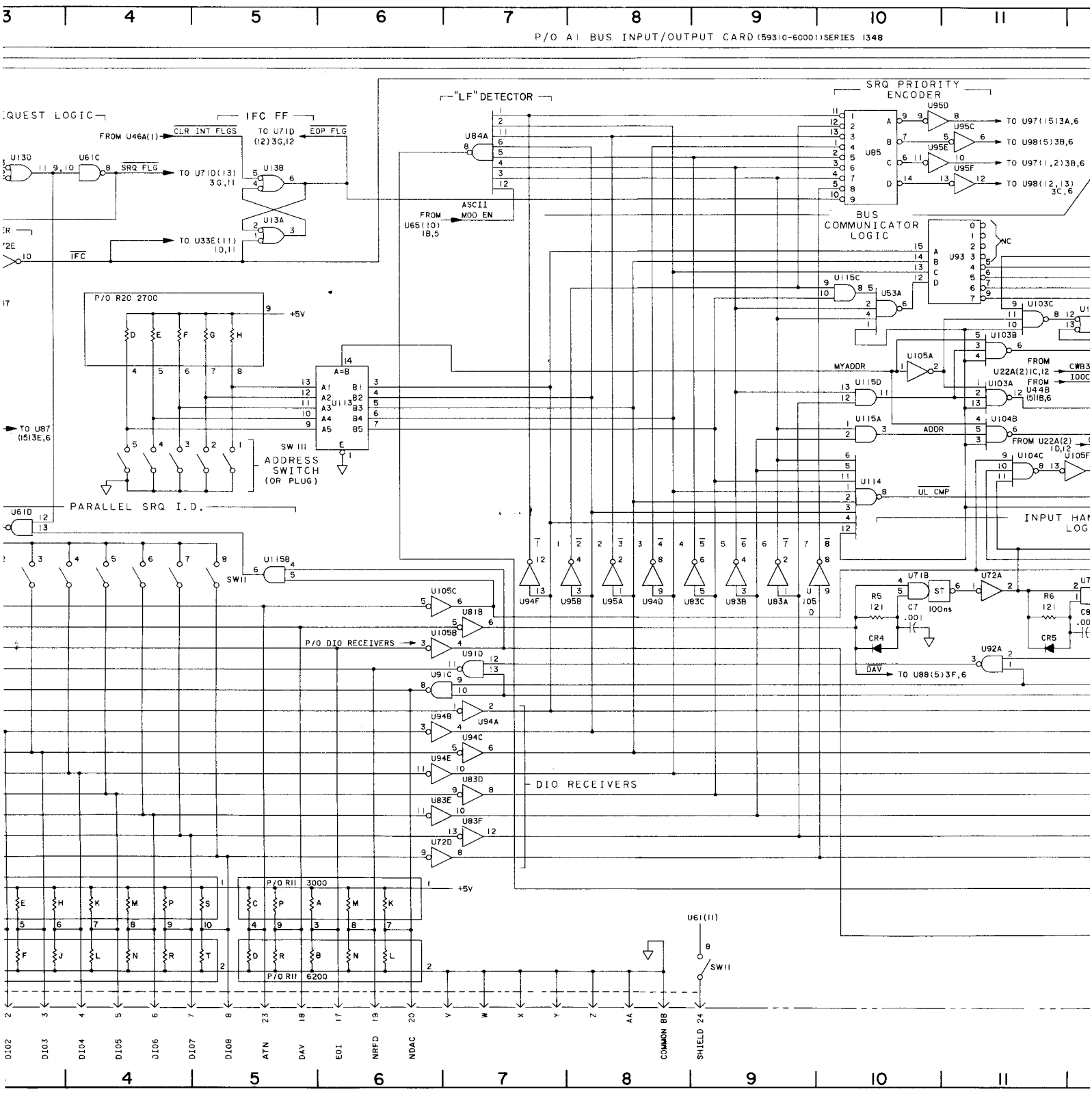
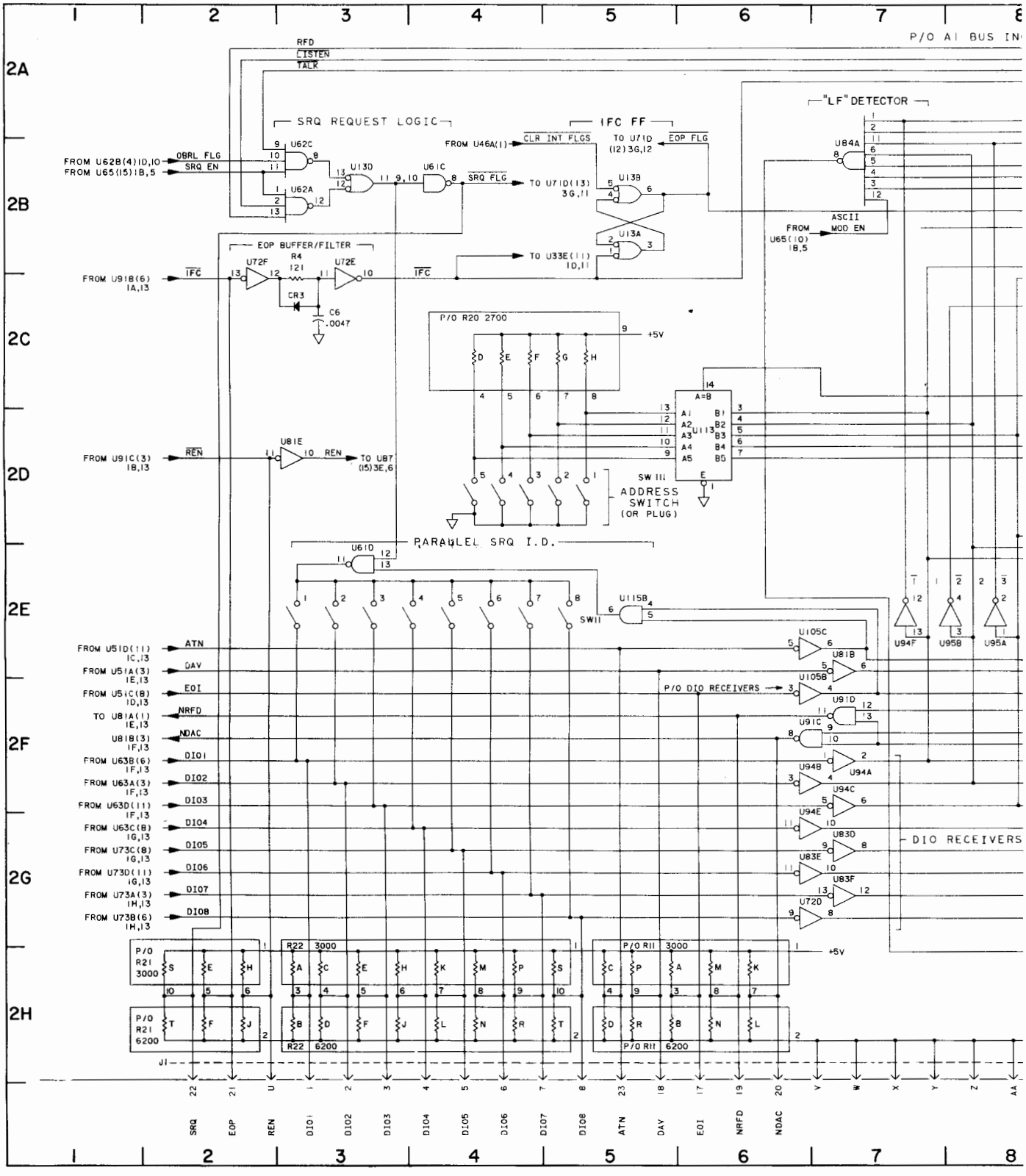


Figure 8–5. 59310A Schematic Diagram (Sheet 2 of 3)



ons corresponding to numbered grids
s: sheet 3, row H, column 16.



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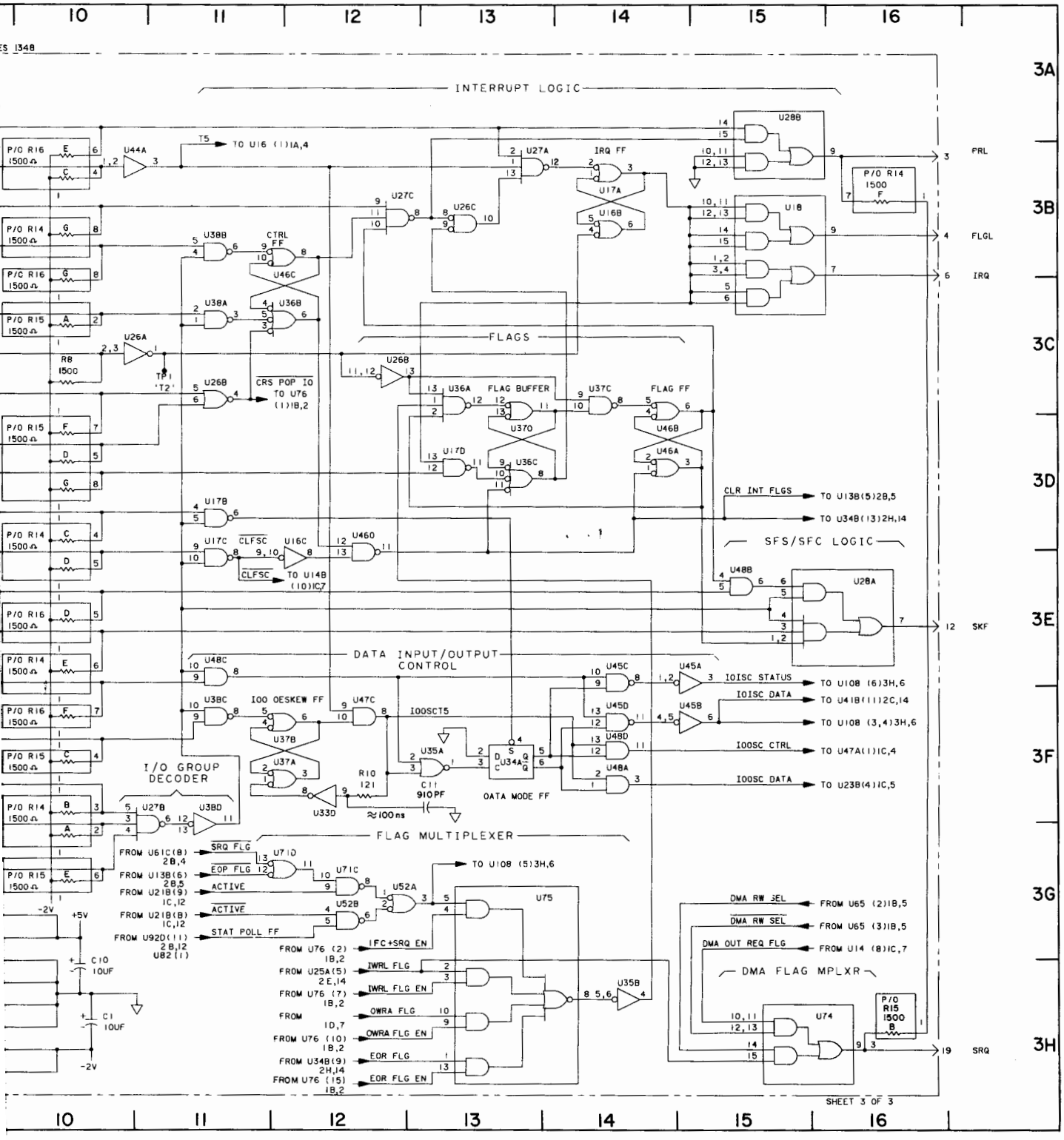
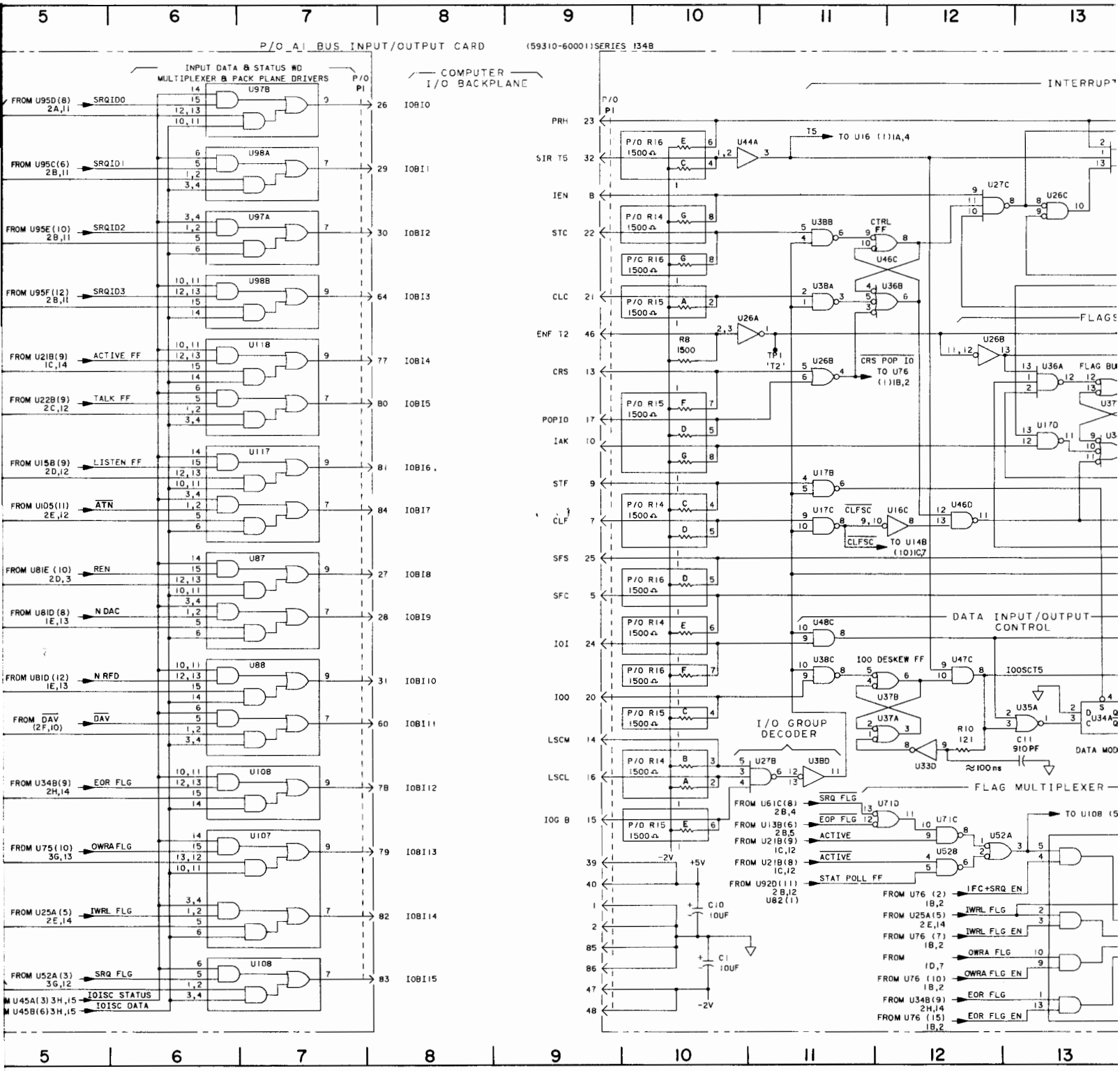
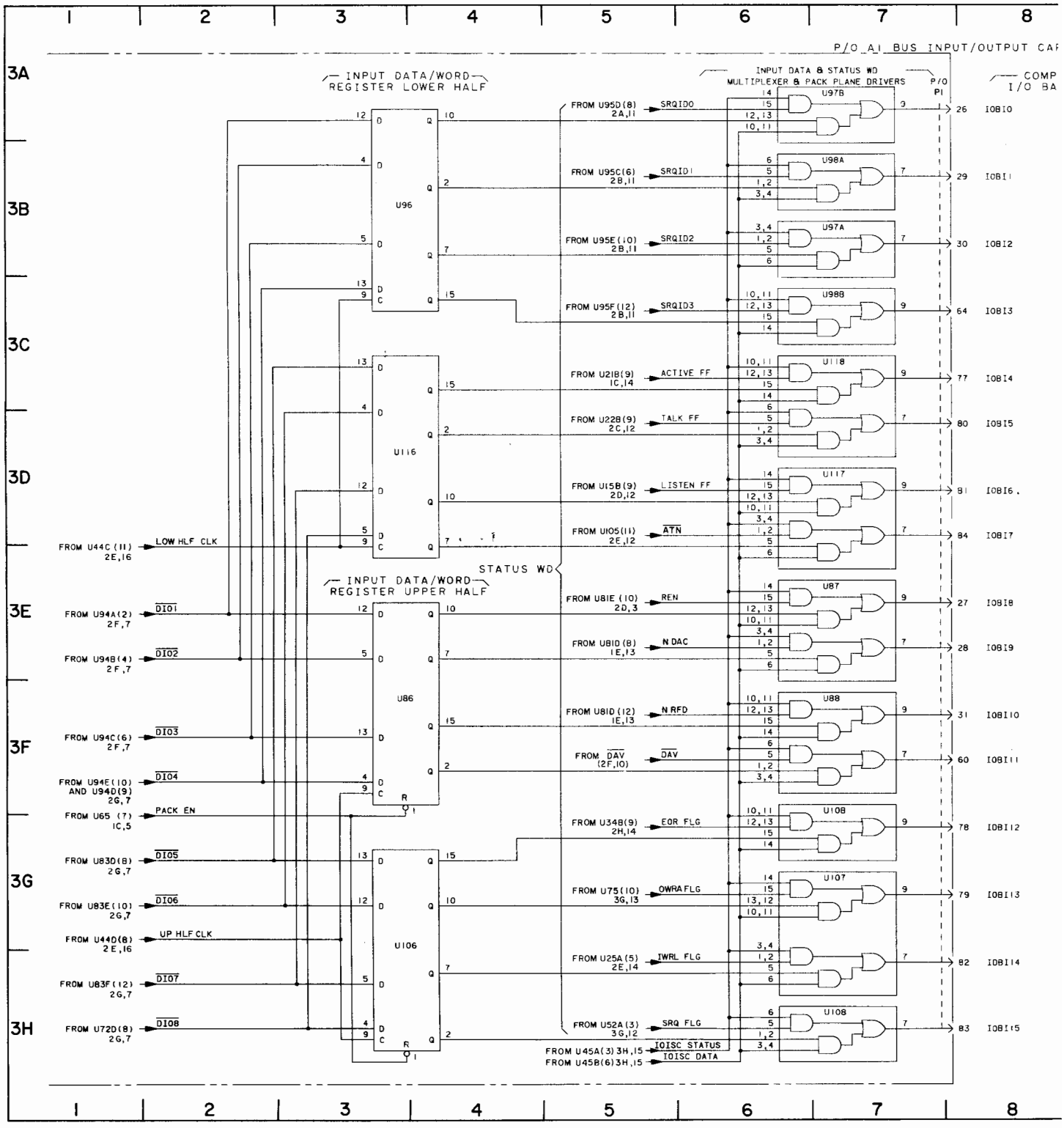


Figure 8-5. 59310A Schematic Diagram (Sheet 3 of 3)



ered grids
16.



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