SIGNAL	LOCATION	USE	GENERAL DESCRIPTION
ADDRESS BUS A0–A15	(pins [P1] 1–16)	System expansion, activity monitor (Logic Analyzer), and DMA (direct memory access) of on-board memory and I/O.	All address lines are demultiplexed and buffered. HLDA signal causes bus to float.
DATA BUS D0–D7	(pins [P2] 1–8)	System expansion, activity monitor (Logic Analyzer), and DMA of on-board memory and I/O.	Direct connection to the system data bus. Requires external buffering near the edge connector if more than 1 LS TTL load is connected, or if appreciable cable or board capacitance is added (>100 pf). HLDA signal causes bus to float (with 10K pull-up resistors).
DATA INPUT BUS D0–D7	(pins [P2] K-T)	Allows 8 external input signals to be connected to the μLab input port (address 2000) for system expansion.	Inputs go directly to input port IC13 and to input switch S3. Because this switch ties these lines directly to ground when placed in the down switch position, individual input data switches must be in the up (logic 1) position for any externally controlled lines. All switches can be placed in the up position if desired. 10K pull-up resistors are on each line. The IN 20 instruction will also access this port.
DATA OUTPUT BUS D0–D7	(pins [P2] 9–16)	Provides 8 latched output signals for system expansion using the μLab's output port (address 3000).	The output pins of output port IC15 go directly to output LEDs DS12 to DS19 and the edge connector. The OUT 30 instruction will also access this port.
INTERRUPTS RST5.5 INTR	(P1-L) (P1-K)	System expansion.	RST5.5 and INTR provide additional interrupt capability for the μLab. To use these interrupts, jumpers J3 and J2, respectively, must first be opened on the μLab PC board.*
$\overline{\text{INTA}}$ (Interrupt Acknowledge)	(P1-J)	Handling of an INTR interrupt.	This output from the microprocessor responds to the device that caused the INTR interrupt by asking for an instruction.
CLOCK OUT	(P1-D)	System expansion and synchronization with external circuits.	A 2 MHz TTL level square wave signal controlled by the crystal oscillator on the μLab.
VA (Valid Address)	(P1-V)	System expansion, address decoding and activity monitor (Logic Analyzer).	When this signal is high, a valid address is present on the address bus and either a read or a write is being performed on memory or I/O.

Table G-1. Edge Connector Signals

SIGNAL	LOCATION	USE	GENERAL DESCRIPTION
ALE (Address Latch Enable) $\overline{ALE}$	(P1-A) (P1-U)	System expansion using multiplexed address/data bus chips, and activity monitor (Logic Analyzer).	Microprocessor generated signals that indicate valid address data is present on the data bus. Both true and complement signals are provided for user convenience.
$\overline{WR}$ (Write)	(P1-T)	System expansion, activity monitor (Logic Analyzer), and DMA of on-board RAM and output ports.	Buffered output. HLDA signal causes it to float with DS7A pulling it up. An external circuit must be able to provide 4 ma in the logic 0 state.
$\overline{RD}$ (Read)	(P1-R)	System expansion, activity monitor (Logic Analyzer), and DMA of on-board memory and input ports.	Buffered output. HLDA signal causes it to float with DS7B pulling it up. An external circuit must be able to provide 4 ma in the logic 0 state.
IO/$\overline{M}$ (Input-output/ memory)	(P1-S)	System expansion of memory or I/O.	Microprocessor signal indicating either I/O or memory operation.
SID (Serial Input Data)	(P1-N)	System expansion.	A single bit input port to the microprocessor controlled by the RIM instruction. To use this input, jumper J4 must first be opened on the μLab PC board.*
SOD (Serial Output Data)	(P1-W)	System expansion.	One bit of serial output data identical to the data sent to the speaker, but separately buffered. Controlled by the SIM instruction. HLDA signal causes this line to float.
READY	(P1-B)	System expansion with slow bus devices.	Normally used by the μLab to perform the single-step functions. A low logic level on this line forces the microprocessor to wait for slow bus devices. To use this input, jumper J5 must first be opened on the μLab PC board.* If the single-step feature is also desired, the step signal must be externally gated back into the READY line (see the STEP line description that follows).
STEP	(P1-X)	Retains the μLab's single-step functions for internal and external memory and I/O when an external READY input is used.	When jumper J5 is opened to allow external control of the READY input, the μLab single-step circuits are no longer gated into the microprocessor. To re-insert the single-step features, the circuit shown in Figure G-1 can be used.

Table G-1. Edge Connector Signals (Continued)

SIGNAL	LOCATION	USE	GENERAL DESCRIPTION
$\overline{\text{RESET IN}}$	(P1-C)	External power-on reset control of μLab.	A low logic level on this line causes the μLab to execute the same power-on reset cycle that it does when first turned on.
RESET OUT	(P1-M)	Initializing external circuits.	This line goes to a logic 1 whenever the microprocessor is reset (during power-up or when the $\overline{\text{RESET IN}}$ line is pulled low).
HOLD	(P1-E)	DMA of μLab memory and I/O.	A high logic level on this input causes the microprocessor to enter the hold state. In this state the HLDA line goes high, forcing the address, data, and control lines into their high impedance state (see HLDA output). To use this input, jumper J1 must first be opened on the μLab PC board.*
HLDA (Hold Acknowledge)	(P1-P)	Disables all system memory and I/O control lines so that an external controller can perform DMA.	When this line is high, the μLab's microprocessor is in the hold state and the address, data, and control bus lines ($\overline{\text{RD}}$, $\overline{\text{WR}}$, IO/$\overline{\text{M}}$) are in their high impedance state. In this mode an external controller can transfer data directly to or from the system bus devices. HLDA results from a HOLD input signal to the microprocessor.
S0 (State 0) S1 (State 1)	(P1-H) (P1-F)	System expansion.	Output signals directly from the microprocessor that provide advanced state and system information.

Table G-1. Edge Connector Signals (Continued)

*NOTE: Circuit jumpers (J1 to J5) are provided on the μLab for system expansion. All five are shorted at the factory using traces on the PC board. To open a jumper, a sharp knife can be used to break the narrow trace that connects the pair of plated-through holes at the jumper position. To restore the short, a solder bridge or piece of wire connecting the holes can be used.

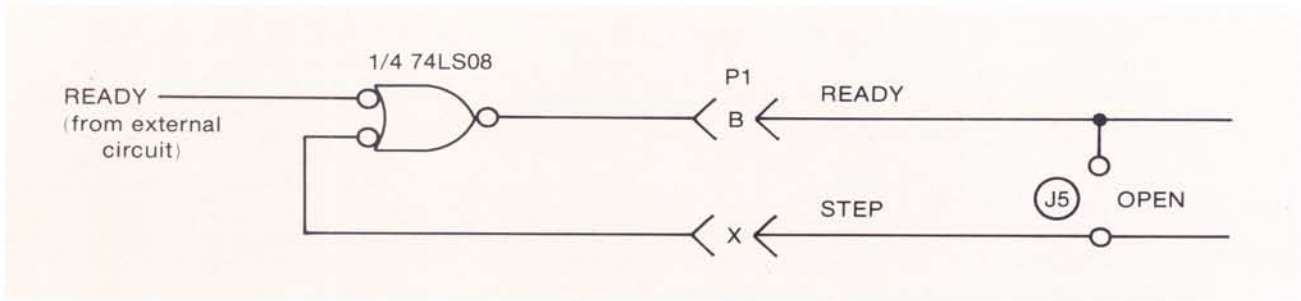

Figure G-1. A Circuit for Retaining the Single-Step Feature When Using an External READY Input