HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

37203A

HP-IB EXTENDER
(Including Option 001)

SERIAL NUMBERS

This manual applies directly to instruments with serial number prefixed 2009U. For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

Manual Part Number 37203-90000
Microfiche Part Number 37203-90025

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MANUAL CHANGES

MANUAL IDENTIFICATION

Model Number: 37203A
Date Printed: Aug. 1980
Part Number: 37203-90000

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement.

Make all ERRATA corrections.

Make all appropriate serial number related changes indicated in the tables below.

Serial Prefix or Number	Make Manual Changes
2030U	1
2040U	2
2040U00186	3
2040U00211	4
2040U00356	5
2040U00550	6
2040U00771	7
2040U02995	8
2040U04081	9

Serial Prefix or Number	Make Manual Changes
2040U05981	10
2325U	11*

*NEW ITEM

ERRATA

Change Schematic Diagram, Figure, A1-9 as shown in Figure 1.

Page 6-6, Table 6-2, Replaceable Parts:
Change A1U53 to 1820-0685

Page 6-7, Table 6-2, Replaceable Parts:
Add E1 Part Number 0960-0444, Line Module, unfiltered.

NOTE

Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of the supplement. Free copies are available from all HP offices. When requesting copies quote the manual identification information from your supplement or the model number and print date from the title page of the manual.

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ERRATA (CONT'D):

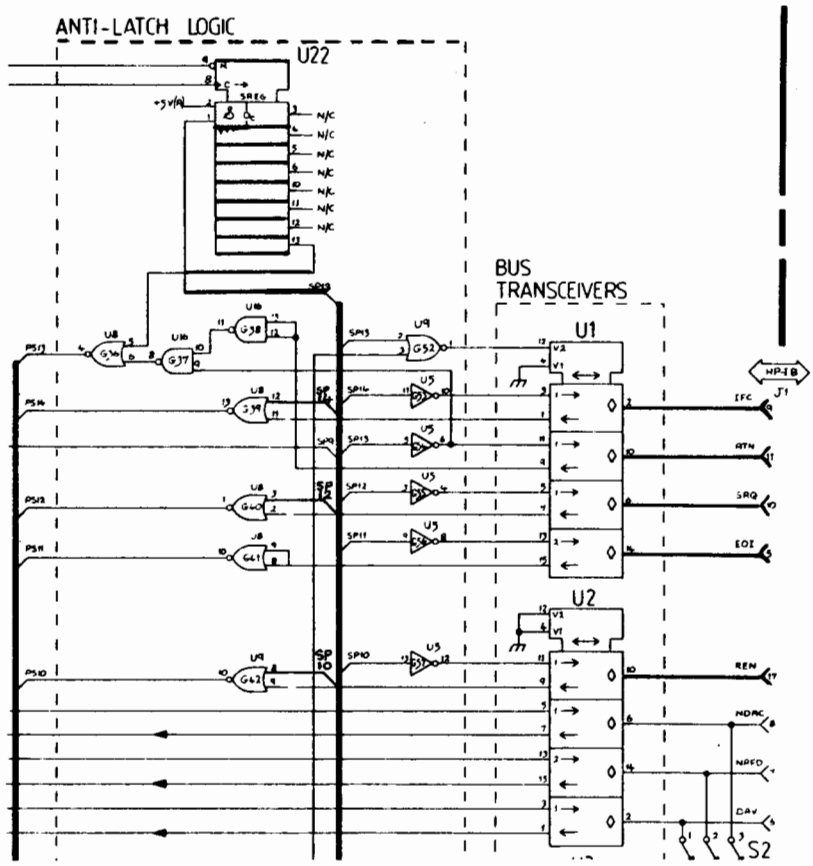


Figure 1 HP-IB Section Schematic Diagram.

Page 8-30:
Delete Paragraphs A1-15 and A1-16.

*Page 6-6, Table 6-2, Replaceable Parts:
Change A1U55 from 1820-1197 to 1820-0681.

ERRATA (CONT'D):

Section 8, all oscilloscope photographs:
Note that the photopgraphs were taken using the 10:1 probe so the amplitude scale is given as oscilloscope setting.

Page 8-24, Table A1-2 Switch Settings:
Change A1S3 Setting to 1/16.

Page 8-25, Table A1-3 Signature List:
Change Parallel Register signatures from HA3U to 5AAH
and 7U8P to UU1F

Page 8-32, Figures A1-10,A1-11, A1-12 and A1-13:
Change timebase scale to 0.02μs/div, 10μs/div, 0.05μs/div and 0.5μs/div respectively.

Page 8-32, Check 4- Algorithmic State Machine 'A':
Change oscilloscope triggering point from Test Point MCLK to X(U30(7)

Page 8-32, Table A1-10 ASM'B' SA Test Signatures
Change $U56(_{11})$ signature to 6A7P
Change Monitor Point U57(16) to U57(6)

Page 8-32, Table A1-9 Switch Settings:
Change A1S3 setting to 1/16.

CHANGE 1

Effective on and after Serial Prefix 2030U two 5 way connectors are fitted allowing the 37203A option 001, Fibre Optic Transmitter and Receiver to be plug-in instead of solder-in.

Page 6-6, Table 6-2, Replaceable Parts:
Add A1J3, 1200-0926, 5 way connector.
Add A1J4, 1200-0926, 5 way connector.

Figure A1-9, Schematic Diagram:
Change the value of C1 from 430pF to 470pF.

Page 6-4, Table 6-2, Replaceable Parts:
Amend A1C1 to 0160-3533, Capacitor Fixed 470pF.

CHANGE 2

Effective on and after Serial Prefix 2040U
Changes to the circuits as shown in Figure 2 and Figure 3.
Change the Schematic Diagrams Figure A1-9 and A1-16 as appropriate.

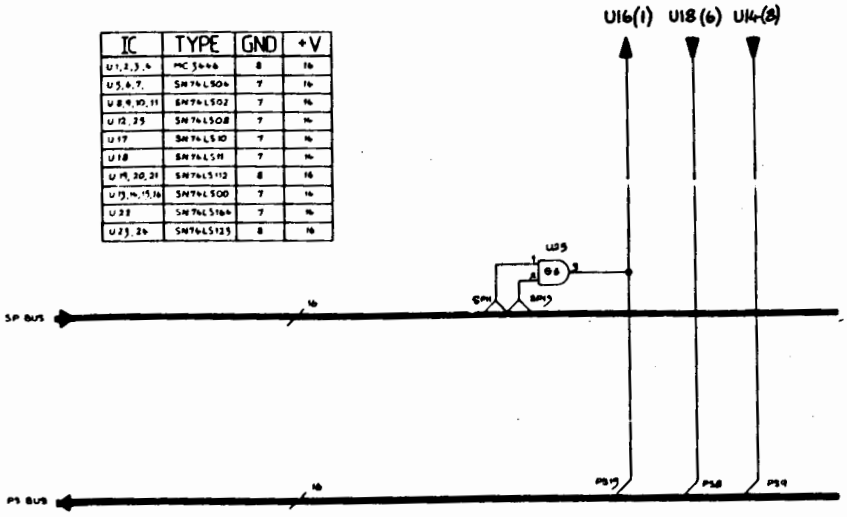


Figure 2 HP-1B Section Schematic Diagram (Figure A1-9).

CHANGE 2 (CONT'D):

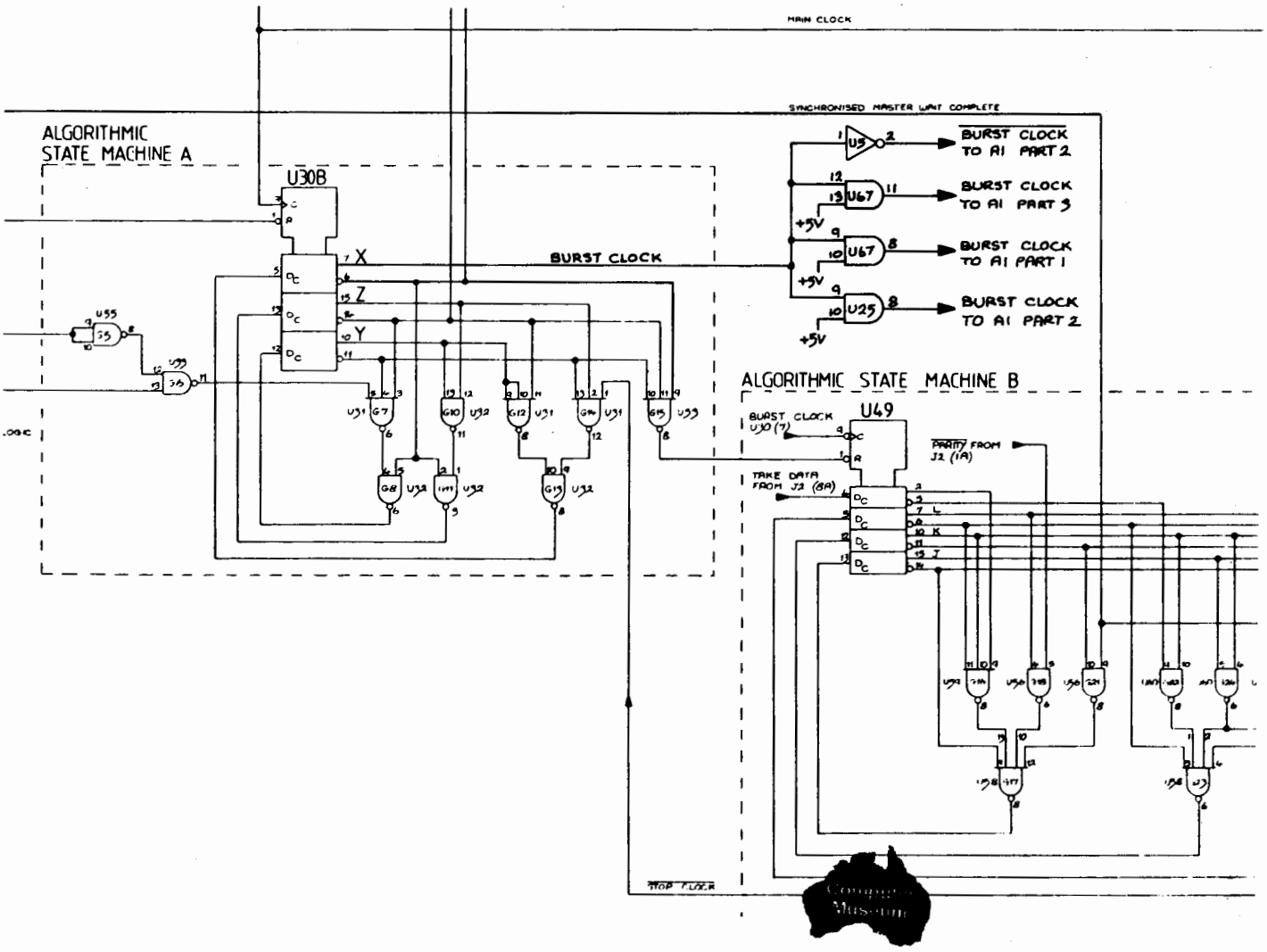


Figure 3 Control Logic Schematic Diagram (Figure A1-16).

CHANGE 2 (CONT'd):

Change Burst Clock U30(7) to Burst Clock U67(11) at U47(2), U48(2) U49(9), U50A(9), U50B(9), U50C(9), U50D(9), and U67(1) on Figure A1-16.

Change Burst Clock U30(7) to Burst Clock U67(8) at the Signature Analysis Clock Test point on Figure A1-16.

Page 6-4, Table 6-2, Replaceable Parts:
Change Part Number A1 from 37203-60001 to 37203-60020.
Change Part Number A1 option 001 from 37203-60101 to 37203-60050

Page 6-6, Table 6-2, Replaceable Parts:
Change Part Number A1U67 from 1820-1201 to 1820-1367

On Figures A1-3, A1-4, A1-8, A1-15 and A1-18 change Part Number 37203-60001 to 37203-60020.

CHANGE 3

Effective on and after Serial Number 2040U00186 a change to the TX Coax Driver Circuit as shown in Figure 4. Change the Schematic Diagram Figure A1-3 as appropriate.

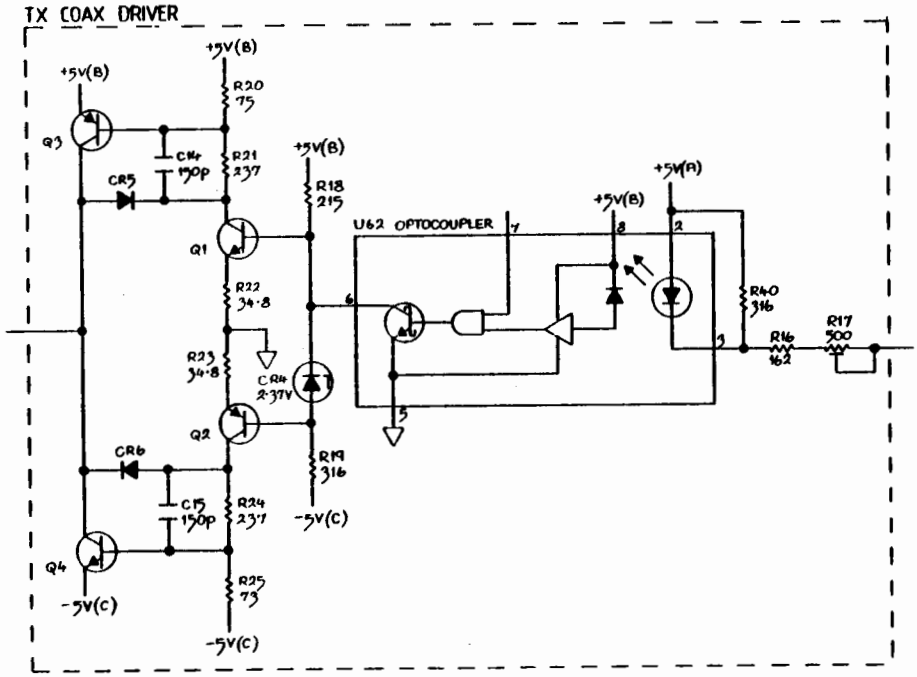


Figure 4 TX Coax Driver Circuit (Figure A1-3).

CHANGE 3 (CONT'd):

Page 6-4, Table 6-2, Replaceable Parts:
Change A1R16 to 0757-0405, Resistor 162Ω.
Add A1R40, 0698-3444, Resistor 316Ω.

CHANGE 4

Effective on and after Serial Number 2040U00211 a new power module is fitted.
Change Schematic Diagram, Figure A1-18 as shown in Figure 5.

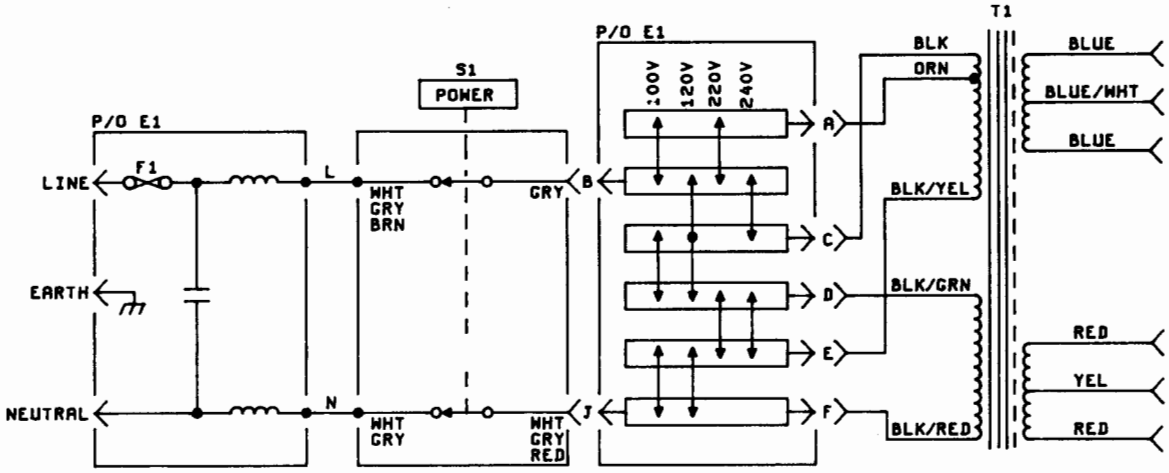


Figure 5 Power Supply Circuit (Figure A1-18)

Page 6-4, Table 6-2, Replaceable Parts:
Delete A1C1

Page 6-7, Table 6-2, Replaceable Parts: (Main List)
Change E1 from 0960-0444 to 0960-0448, Line Module filtered.

CHANGE 5

Effective on and after Serial Number 2040U00356 there is a change to the circuit as shown in Figure 6.
Change the Schematic Diagram Figure A1-3 as appropriate.

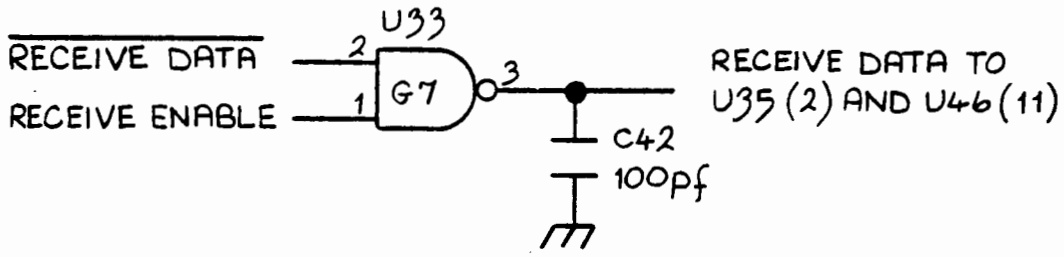


Figure 6 Serial Section Schematic Diagram.

Page 6-4, Table 6-2, Replaceable Parts:
Add Part Number A1C42, 0160-4389 Capacitor-Fxd 100pF.

CHANGE 6

Effective on and after Serial Number 2040U00550 there is a change to the Main Clock Generator circuit on Control Logic, A1Part 3.
Change Value A1C23 from 240pF to 100pF.

Page 6-4, Replaceable Parts:
Change A1C23 from 240pF to 0160-2204, Capacitor-Fxd 100pF.

Page 8-33, Figure A1-16 Schematic Diagram A1Part 3.
Change C23 from 240pF to 100pF.

CHANGE 7

Effective on and after Serial Number 2040U00771 there is a change to the Algorithmic State Machine "A" circuit, as shown in Figure 7.

Change the Schematic Diagram Figure A1-16 as appropriate.

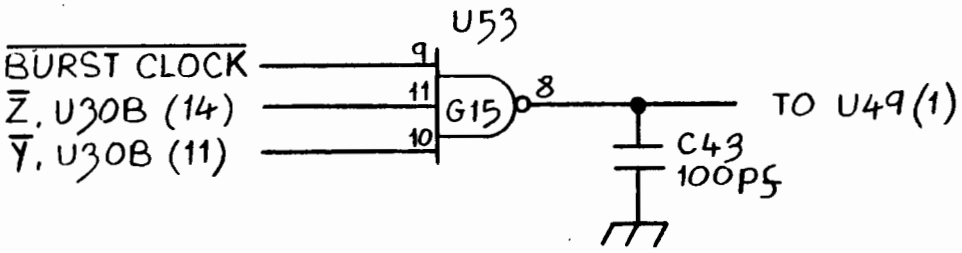


Figure 7 Control Logic Schematic Diagram.

Page 6-4, Table 6-2, Replaceable Parts:
Add Part Number A1C43, 0160-4389, Capacitor-Fxd 100pF.

CHANGE 8

Effective on and after Serial Number 2040U02995 the Main Clock Generator circuit changes from discrete components to a packaged oscillator, as shown in Figure 8.
Change Schematic Diagram Figure A1-16 as appropriate.

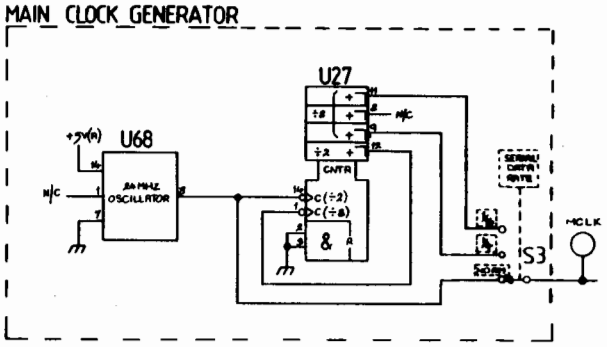


Figure 8 Control Logic Schematic (Main Clock Generator).

Page 6-4, Table 6-2, Replaceable Parts:
Delete: A1C21, A1C22, A1C23, A1C24, A1C25, A1L1, A1Q7, A1Q8, A1R32, A1R33, A1R34, A1R35, A1R36, A1R37 and A1Y1.
Add: A1U68, 1813-0227 Oscillator IC 24MHz ±0.1%

CHANGE 9

Effective on and after Serial Number 2040U04081 there is a change to the Power Supply circuit, A1 Part 4.

Change value A1C9 from 330μF to 47μF.

Page 6-4, Replaceable Parts
Change A1C9 from 330μF to 0180-3009, Capacitor Fxd 47μF, 50V.

Page 8-35, Figure A1-18 Schematic Diagram A1 Part 4
Change C9 from 330μF to 47μF.

CHANGE 10

Effective on and after Serial Number 2040U-05981 there is a change to Algorithmic State Machine "A" circuit. Change value of C43 from 100pF to 470pF.

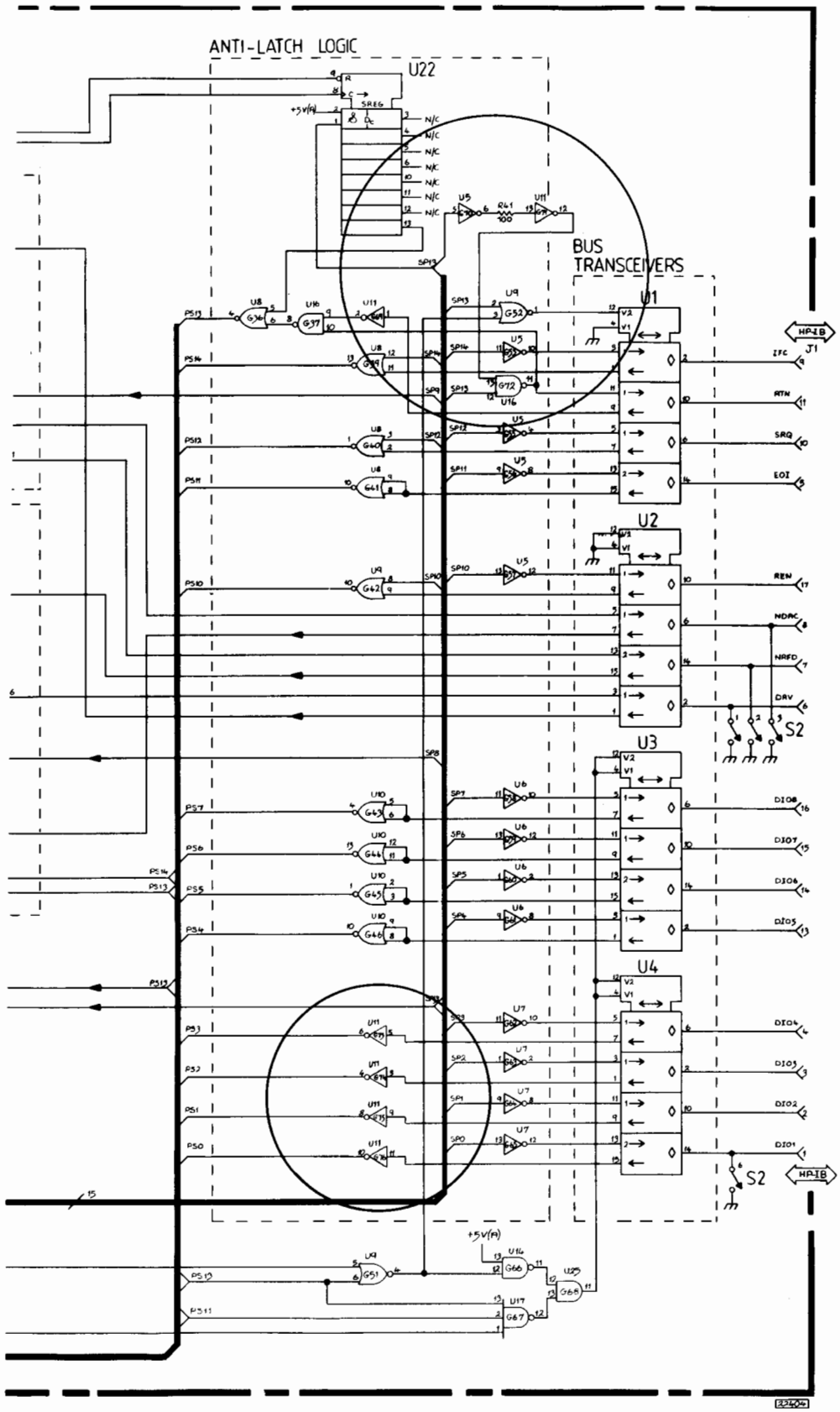
Page 6-4, Table 6-2, Replaceable Parts:
A1C43, 0160-4365, Capacitor Fxd 470pF.

*CHANGE 11

Effective on and after Serial Prefix 2325U there is a change to the HP-IB circuit as shown in Figure 9.

Change Schematic Diagram Figure A1-9, Page 8-31, as appropriate.

Page 6-4, Table 6-2 Replaceable Parts;
Change Part Number A1U11 from 1820-1144 to 1820-1199.
Add Part Number A1R41 0757-0401, Resistor 100 ohms.


ANTI-LATCH LOGIC
U22
SREG
N/C
BUS
TRANSCEIVERS
U1
U2
U3
U4
HP-IB
J1
IFC
ATN
SRQ
EOI
REN
NDAC
NRFD
DAV
DIO8
DIO7
DIO6
DIO5
DIO4
DIO3
DIO2
DIO1
S2
+5V(A)
R41
100
PS14
PS13
PS12
PS11
PS10
PS7
PS6
PS5
PS4
PS3
PS2
PS1
PS0
SP14
SP13
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22404

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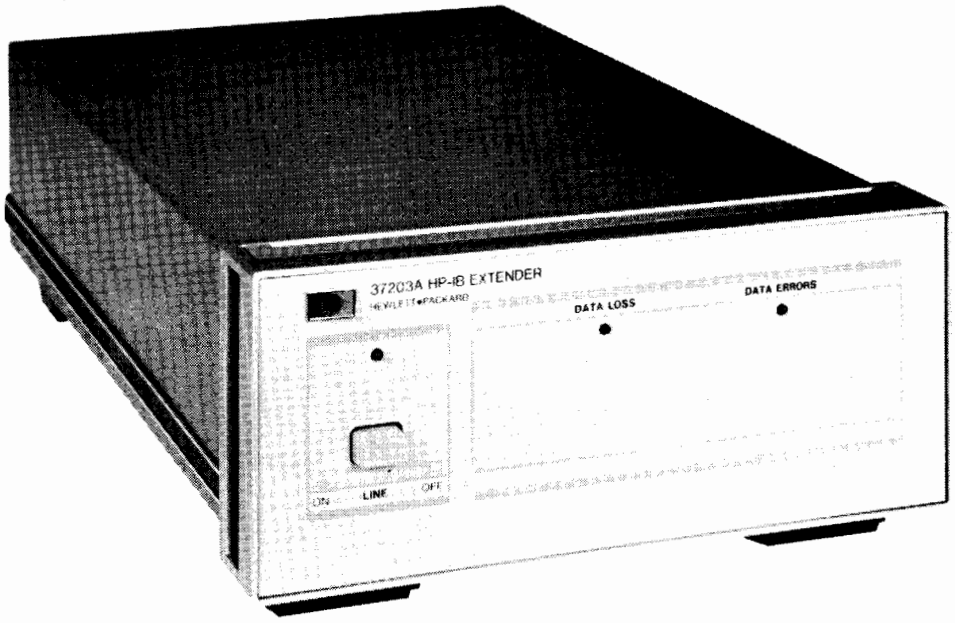


Figure 1-1 Model 37203A HP-IB Extender

SECTION I

GENERAL INFORMATION

1-1 INTRODUCTION

1-2 This Operating and Service Manual contains information required to install, operate, test, adjust and service the Hewlett-Packard Model 37203A HP-IB Extender. Figure 1-1 shows the 37203A.

1-3 This section of the manual describes the instrument and includes information on the identification, accessories, characteristics, safety and other basic information.

1-4 Listed on the title page of this manual is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement.

1-5 OPERATING CHARACTERISTICS

1-6 These Operating Characteristics summarise the features and nominal performance of the 37203A. They do not constitute warrantable specifications.

1-7 HP-IB Data-Byte Rate

1-8 The HP-IB data-byte rate differs from system to system, depending on the following factors:

Serial transmission rate
Serial link propagation delay
Handshake rate of devices connected to the HP-IB Extenders.

1-9 The recommended coaxial cable or fibre optic cable was used in achieving the maximum transfer rates given in Table 1-1 and the speed of the 37203A was not reduced by the effect of other devices connected to the bus.

1-10 HP-IB Interface

1-11 The 37203A may be connected directly to a maximum of 14 other HP-IB devices subject to the normal cabling restrictions imposed by the interface standard. It will provide extension for the full range of HP-IB functions.

1-12 HP-IB is Hewlett-Packard's implementation of IEEE Standard 488-1978. The 37203A is in general compliance with each of the following standards and supports their major capabilities:

IEEE Standard 488-1978
ANSI Standard MC1.1
IEC Standard 625-1

1-13 Total compatability among independently designed products interconnected via the 37203A is beyond the control and scope of this product, see Section 6 of the above referenced standards.

Table 1-1 Maximum Transfer Rates (Nominal)

	Coaxial Cable (see Note 2)				Fibre Optic Cable (Opt 001)		
	Short (at normal) speed) See Note 1	250m (max range at normal speed)	500m (max range at 1/4 speed)	1000m (max range at 1/16 speed)	Short See Note 1	250m	1000m
Max HP-IB byte transfer rate (k byte/s)	50	40	14.5	2.75	50	39	25
Max SRQ propagation delay (μs)	14	18	55	200	14	20	30
Max Parallel Poll response time (μs)	20	25	75	270	20	25	40

Note 1 For distances <250m, interpolate between Short and 250m columns.

Note 2 These results were achieved using the recommended coaxial cable (Belden cable type 9248)

1-14 General

Power Requirements: 100/120/220/240 ac +5 −10%; 48 to 66Hz, 25VA max.
Operating Temperature: 0 to +55°C.
Dimensions: 89mm high, 213mm wide, 356mm deep.
Weight: 3.5kg (7.7lb), net. 5kg (11lb), shipping.

1-15 SAFETY CONSIDERATIONS

1-16 This Safety Class 1 instrument (provided with a protective earth terminal) has been designed and tested according to international safety standards. Information with regard to safety is presented at appropriate places throughout the manual.

1-17 INSTRUMENTS COVERED BY MANUAL

1-18 Attached to the instrument is a serial number plate. The serial number is in the form: 0000U00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix listed under SERIAL NUMBERS on the title page.

1-19 An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains 'change information' that explains how to adapt the manual to the newer instrument.

1-20 In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complementary copies of the supplement are available from Hewlett-Packard.

1-21 For information concerning a serial number prefix that is not listed on the title page or in the Manual Change supplement, contact your nearest Hewlett-Packard office.

1-22 DESCRIPTION

1-23 The 37203A HP-IB Extender enables the distance between groups of devices interfaced by the Hewlett-Packard Interface Bus (HP-IB) to be extended beyond the limits imposed by direct HP-IB cabling. Functional HP-IB operation of a programmed HP-IB system will usually be identical, with and without the 37203A's, except that due to the transmission delay in an extended system the parallel poll response time will increase slightly. There is no restriction in passing control between devices.

Note: HP-IB is Hewlett-Packard's implementation of IEEE Std. 488-1978 "Standard Digital Interface for Programmable Instrumentation".

1-24 The 37203A has a maximum HP-IB data-byte transfer rate of 50kbyte/s whether data is transmitted over coaxial cable or dual fibre optic cable. The actual HP-IB data-byte transfer rate will be governed principally by the speed of the slowest local or remote HP-IB device.

1-25 By using the 37203A HP-IB Extenders and a coaxial cable or dual fibre optic cable, transmission distances of up to 1000 metres are attainable (see Figure 1-2).

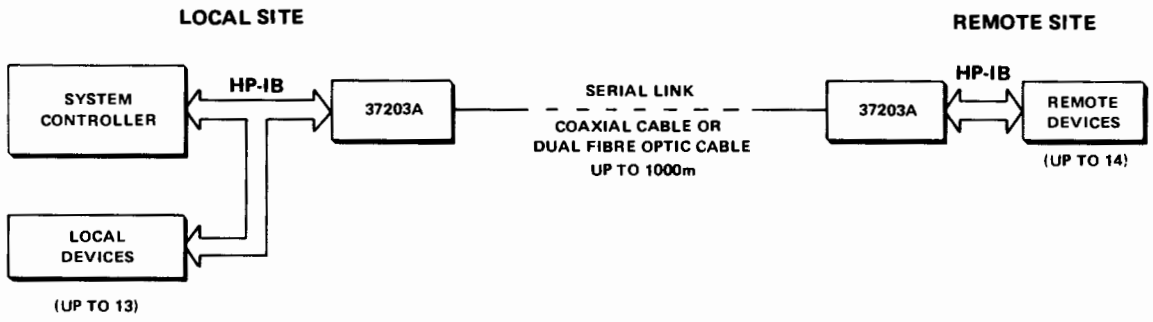


Figure 1-2 System Configuration - Point -to- Point

1-26 One 37203A converts the bit parallel HP-IB protocol into a bit serial stream that is transmitted over coaxial cable or dual fibre optic cable for distances up to 1000 metres. The 37203A at the other end of the serial link performs the reverse function. The entire range of HP-IB functions may be extended to the remote sites but the timing of the parallel poll response will be slightly altered due to the transmission delay in an extended system.

1-27 A pair of HP-IB Extenders communicate with each other using 22 bit data frames. These data frames shuttle continuously back and forth between ends, continually updating each end with the current state of the devices and HP-IB Extender at the other.

1-28 Each transmitted data frame includes a cyclic redundancy check code which is rechecked when the frame is received. Any errors which are detected will cause the erroneous frame to be rejected and one 37203A will restart the data frame shuttle.

1-29 Two HP-IB Extenders can extend the full range of HP-IB functions. The HP-IB Extenders provide a transparent interface i.e. it is usually possible to insert two HP-IB Extenders at any point in the HP-IB without altering the controller-programming. Due to transmission delay in an extended system the parallel poll response time from remote devices will increase slightly. The parallel poll response time from local devices will not be affected.

1-30 The maximum number of HP-IB devices that can be connected to a single 37203A is 14. A complete system using one pair of Extenders therefore, could consist of up to 14 devices, plus a 37203A at the local end, and another 14 HP-IB device, plus a 37203A at the remote end.

1-31 OPTIONS

1-32 Option 001

1-33 The 37203A Option 001 adds a fibre optic transmitter and fibre optic receiver to the standard 37203A. This provides the capability of extending the HP-IB over either dual fibre optic cable or coaxial cable. The 37203A Option 001 transmits the bit serial stream over dual fibre optic cable for distances up to 1000 metres. The 37203A Option 001 enables a higher HP-IB data-byte transfer rate to be attained for transmission distances greater than 250 metres than is possible with the standard 37203A (see Table 1-1). The fibre optic cable removes the metallic connection between the Bus Extenders and therefore eliminates any electromagnetic pick-up on the serial link. Option 001 is recommended for use in severe electrical environments or where the use of electrical signalling is not acceptable.

1-34 Option 301

1-35 The 37203A Option 301 provides a kit for mounting a single 37203A into a full module width rack, see Figure 1-3.

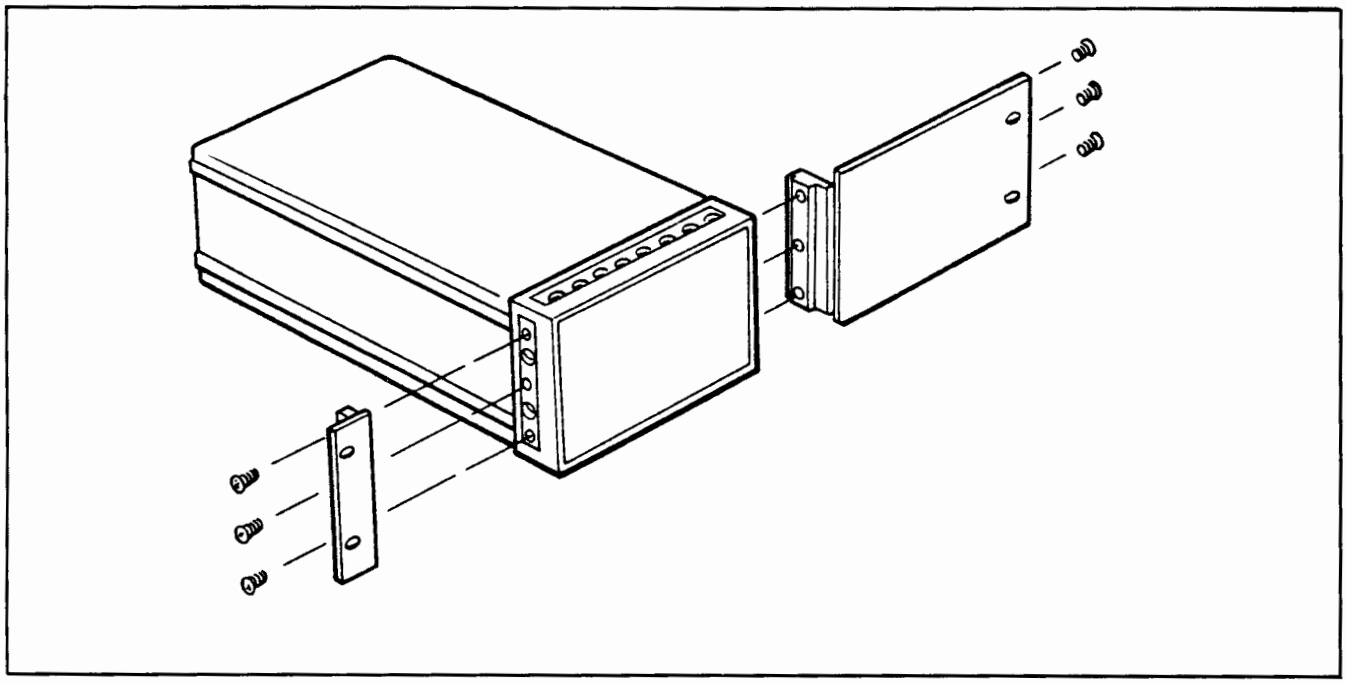


Figure 1-3 Option 301

1-36 Option 302

1-37 The 37203A Option 302 provides a kit for mounting a 37203A plus another unit of the same width and height or another 37203A into a full module width rack, see Figure 1-4.

1-38 ACCESSORIES SUPPLIED

1-39 Supplied with the 37203A is a power cord appropriate to the country of destination (see Section 2).

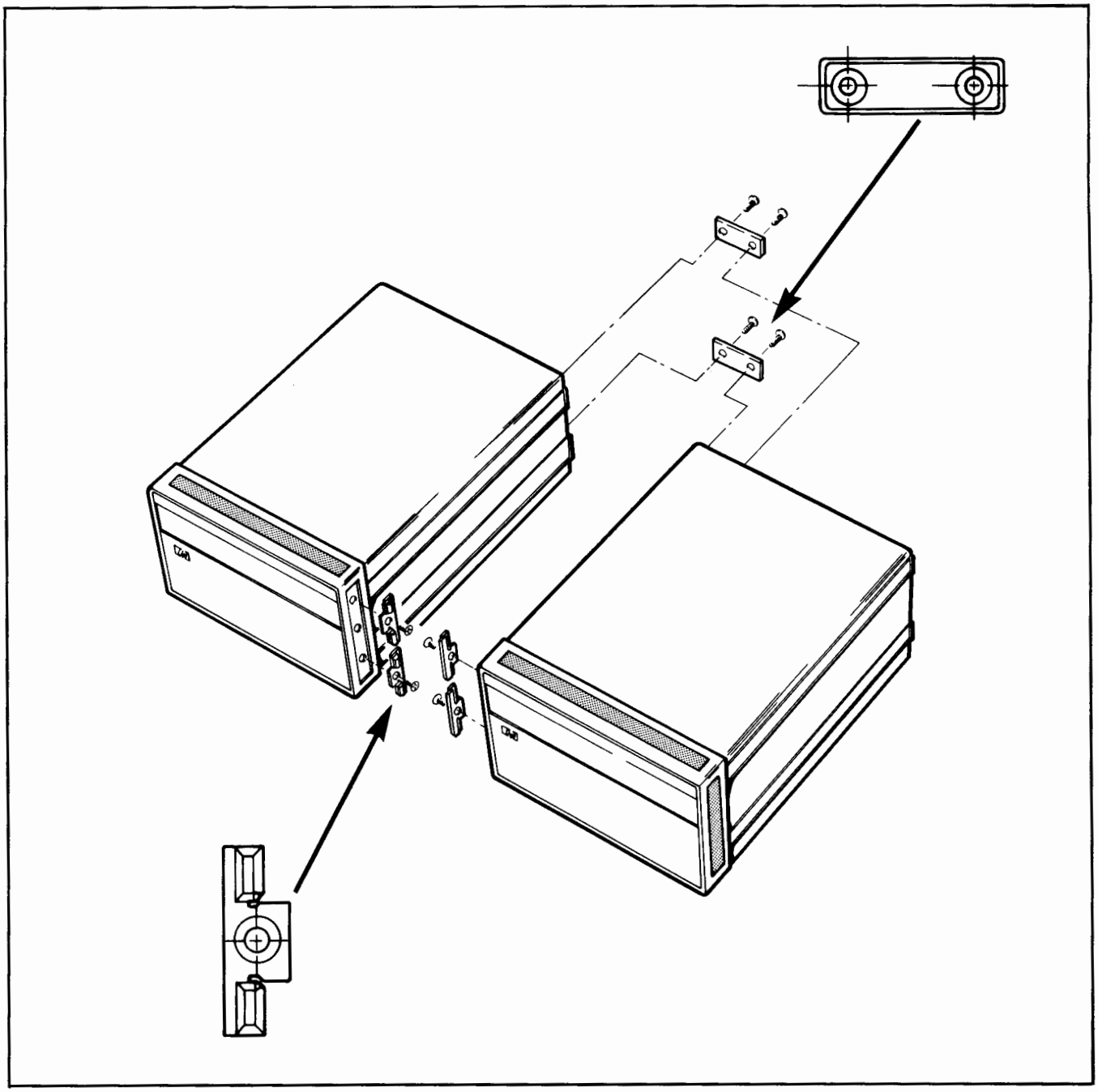


Figure 1-4 Option 302

1-40 ACCESSORIES AVAILABLE

1-41 Table 1-2 lists the accessories available from Hewlett-Packard which can be used in assembling an Extended HP-IB System.

Table 1-2 Accessories Available

Description		HP Part Number	
HP-IB Cables	1 metre	10833A	
	2 metres	10833B	
	4 metres	10833C	
	0.5 metre	10833D	
		Simplex Cable	Duplex Cable
Fibre Optic Cable (with connectors) See Note 1	⩽1000 metres	39200A	39200B

Note 1: 39200A/B defines an optical cable for user specified length supplied with factory installed and tested connectors. Length must be specified in metres and can be any 1 metre increment from 1 to 1000 metres. Length information is shown as option 001 to the base product with quantity equal to the number of cable assemblies ordered. The length should include some excess to allow for limited repair.

Examples: For two lengths of simplex cable 245 metres long specify
39200A Optic Cable Assy Quantity 2
Option 001 245 metres long Quantity 2

For seven lengths of duplex cable 1000 metres specify
39200B Optic Cable Assy Quantity 7
Option 001 1000 metres long Quantity 7

39200A cable is simplex cable, therefore 2 lengths will be required per serial link.

1-42 RECOMMENDED TEST EQUIPMENT

1-43 Equipment required to maintain the 37203A is listed in Table 1-3. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-3 Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model	Use*
Oscilloscope and plug-ins	100MHz bw, 0.5μs/div, 4 Channels	HP 180C/1809A/1825A	A, T
Frequency Counter	Frequency range 10Hz to 25MHz	HP 5302A	A, T
Signature Analyser	Unique	HP 5004A	T
Digital Multimeter	±0.1 at ±5V	HP 3476A/B	T
Desktop Computer	Unique	HP 9825A	P, T
Interface Card (2 off)	Unique	HP 98034A	P, T
Performance Verification Tape	Unique	HP 37203- 12101	P, T
String & Advanced Programming ROM	Unique	HP 98210A	P, T
General I/O & Extended I/O ROM	Unique	HP 98213A	P, T
Logic Probe	TTL Compatible	HP 545A	T
Logic Pulser	TTL Compatible	HP 546A	T

* A = Adjustments, P = Performance Tests, T = Troubleshooting

SECTION II

INSTALLATION

2-1 INTRODUCTION

2-2 This section contains information and instructions required to install the 37203A HP-IB Extender. This section also includes information about initial inspection, operating environment and storage and shipment.

2-3 INITIAL INSPECTION

2-4 Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked both mechanically and electrically. The contents of the shipment should be as shown in Figure 1-1. Procedures for performance verification are given in Section IV. If the contents of the shipment are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Verification, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping material for carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5 PREPARATION FOR USE

2-6 Power Requirements

2-7 The 37203A HP-IB Extender requires a power source of 100, 120, 220, or 240V ac +5% -- 10% at 48 to 66Hz single phase. Power consumption is less than 25VA.

2-8 A timed fuse of 250mA, 250V normal blow (2110-0201) is required for 100/120V operation, and 125mA, 250V normal blow (2110-0318) is required for 220/240V.

2-9 Line Voltage Selection

2-10 Figure 2-1 provides instructions for line voltage and fuse selection.

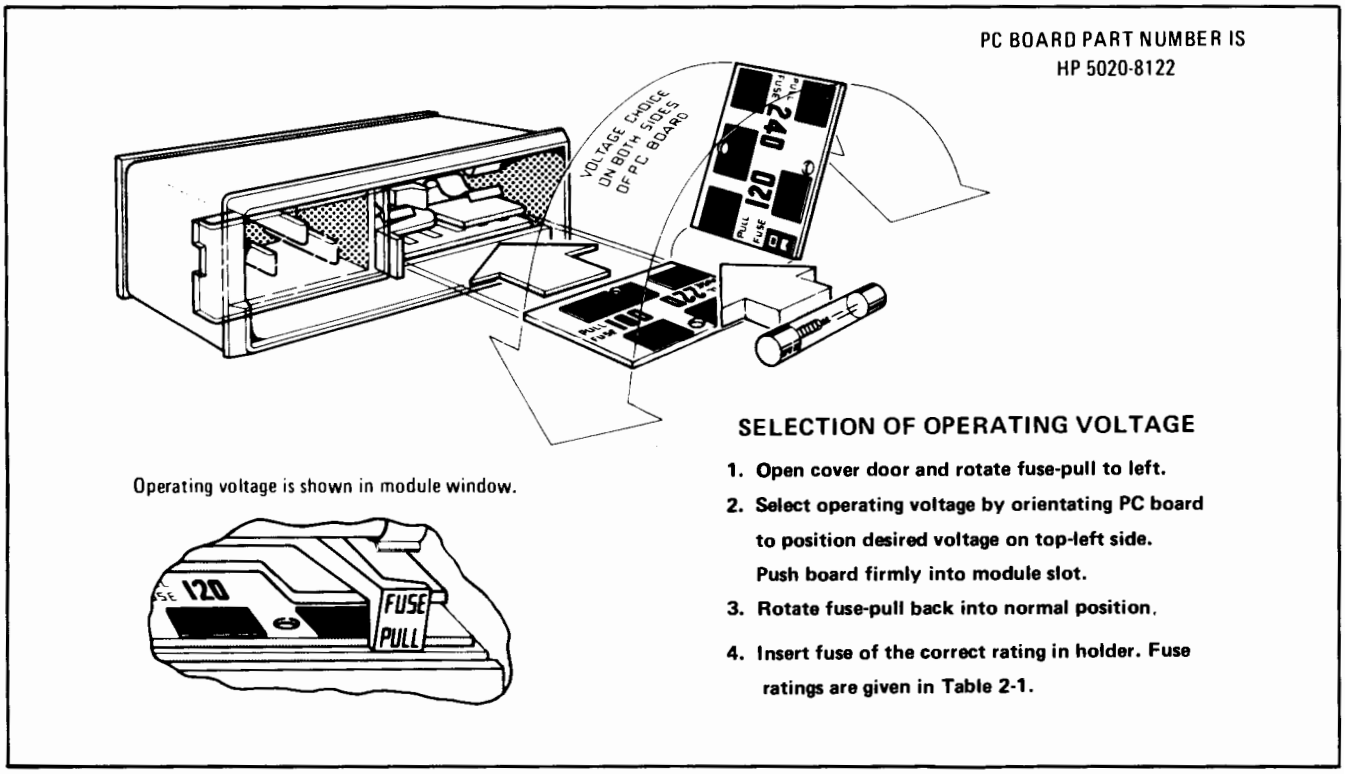


Figure 2-1 Line Selector

CAUTION

Before connecting this instrument to a power outlet, ensure the voltage selector is correctly set for the voltage of the power source and a fuse of the correct rating is fitted.

2-11 Power Cable

2-12 In accordance with the international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument cabinet. The type of power cable supplied with the instrument depends on the country of destination. Figure 2-2 illustrates the standard power plugs commonly used. The number shown below each plug is the HP Part Number of the power cord equipped with that plug. If the appropriate power cord is not included with the instrument, notify the nearest Hewlett-Packard office and a replacement will be provided.

2-13 The colour codes used in each power cable are:

Line – Brown
Neutral – Blue
Ground – Green/Yellow

2-14 Operating Environment

2-15 **Temperature.** The instrument may be operated in temperatures from $0^{o}C$ to $+55^{o}C$.

2-16 **Humidity.** The instrument should be protected from extreme temperature changes which may cause condensation within the instrument.

2-17 **Altitude.** The instrument may be operated at altitudes up to 4600 metres (15,000 feet).

2-18 Rack Mounting

2-19 Rack mounting kits are available and can be purchased through your nearest Hewlett-Packard office.

Rack Mount Kit (for single unit) 5061-0072
Rack Mount Kit (for two units) . . . . . 5061-0094 and 5061-0074

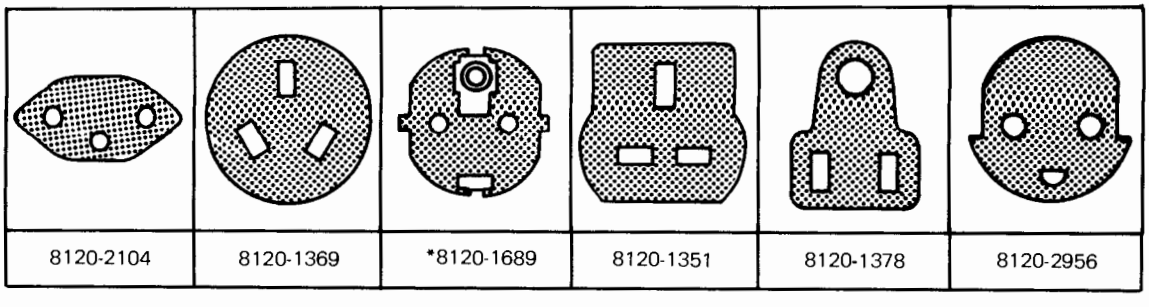
WARNING

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on:

(a) Note that the protection provided by grounding the instrument cabinet may be lost if any power cable other than the three-pronged type supplied is used to couple the ac line voltage to the instrument.

(b) If this instrument is to be energized via an auto-transformer to reduce or increase the line voltage, make sure that the common terminal is connected to the neutral pole of the power source.

(c) The power cable plug shall only be inserted into a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord without a protective conductor (grounding).



Note: In order to pass German Std FTZ527 Power cord 8120-2857 must be fitted to the instrument.*

Figure 2-2 Power Receptacle

2-20 HP-IB

2-21 The instrument is connected to the HP-IB by means of an HP-IB interface cable from the connector on the rear panel of the instrument. Each end of the cable has both a male and female "piggyback" connector which simplifies interconnection of instruments and cables by allowing connectors to be stacked. Up to 15 HP-IB devices, including a 37203A, may be interconnected by HP-IB interface cables.

2-22 In order to maintain proper line voltages and timing relationships, restrictions are placed on the length of HP-IB cable used in direct HP-IB coupling. When connecting devices directly on to the HP-IB, at the local and remote ends, the following rules should be observed to ensure correct operation:

The total HP-IB cable length for the devices connected to a 37203A must be.

(1) Less than or equal to 20 metres (65.6 feet).

(2) Less than or equal to 2 metres (6.56 feet) times the total number of devices connected to the bus but the total length must not exceed 20 metres.

2-23 A list of HP-IB interconnecting cables available is given in Table 2-1.

Table 2-1 HP-IB Interconnecting Cables

Length	Accessory Number
1 metre	10833A
2 metres	10833B
4 metres	10833C
0.5 metre	10833D

2-24 HP-IB Connector

2-25 Figure 2-3 shows the HP-IB connector pin allocation and signal names. A description of the signals on this connector follows.

HP-IB Pins 1-4 (DIO1-DIO4)
and
HP-IB Pins 13-16 (DIO5-DIO8) are the Data Input/ Output Lines of the HP-IB.

HP-IB Pin 5 (EOI). This line, End or Identity, is used to indicate the end of a multiple byte message, and is also used for parallel polling.

HP-IB Pin 6 (DAV)
HP-IB Pin 7 (NRFD)
HP-IB Pin 8 (NDAC). Data Valid, Not Ready for Data and No Data Accepted lines are the Handshake lines which control the transfer of data bytes between addressed devices.

HP-IB Pin 9 (IFC). This is the "Interface Clear" line. When the system controller sets IFC low true all HP-IB instruments are unaddressed.

HP-IB Pin 10 (SRQ). This is the "Service Request" line and is set low true by any instrument requiring service.

HP-IB Pin 11 (ATN). This is the "Attention" line which is pulled low true to set the HP-IB in the Command mode, and is also used for parallel polling.

HP-IB Pin 12 (SHIELD) is the ground to chassis pin at the HP-IB connector.

2-26 For further information on the HP-IB, refer to the "Condensed Description of the Hewlett-Packard Interface Bus" HP Part Number 59401-90030.

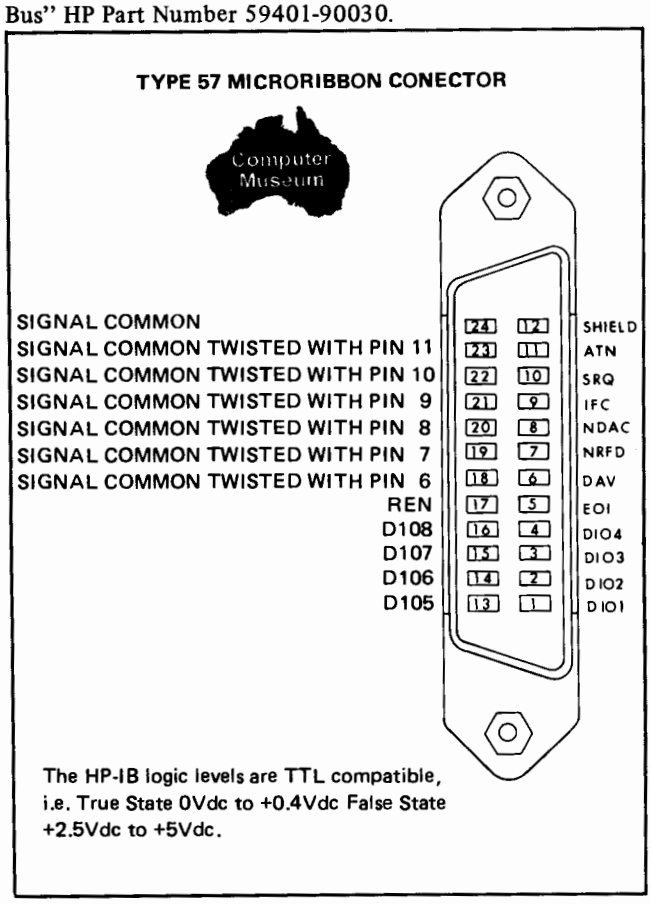


Figure 2-3 HP-IB Connector

2-27 COAXIAL CABLE

2-28 The use of Belden type 9248 cable is recommended. However any other cable which meets the specifications as listed in paragraph 3-20 may be used. A 75Ω BNC connector should be attached to each end of the cable. Trompeter type UPL 20-41 is suitable for use with the recommended Belden type 9248 cable.

2-29 TEST SWITCHES AND BOARD

2-30 The RUN/TEST switch A1S1 should be set to R (RUN) on both 37203A's (see Figure 2-4).

2-31 The test board A1TL1 should be in the factory preset RUN position (see Figure 2-4).

2-32 Switches 1 to 6 of switch A1S2 should be in the factory preset OFF position (see Figure 2-5).

2-33 37203A CONFIGURATIONS

2-34 The following paragraphs outline the steps required to configure the 37203A. The configuration of the 37203A will depend whether the serial link is coaxial cable or dual fibre optic cable. The configurations described are Point-to-Point using coaxial cable and dual fibre optic cable. For system configurations (Star and Tandem) see Paragraph 3-22.

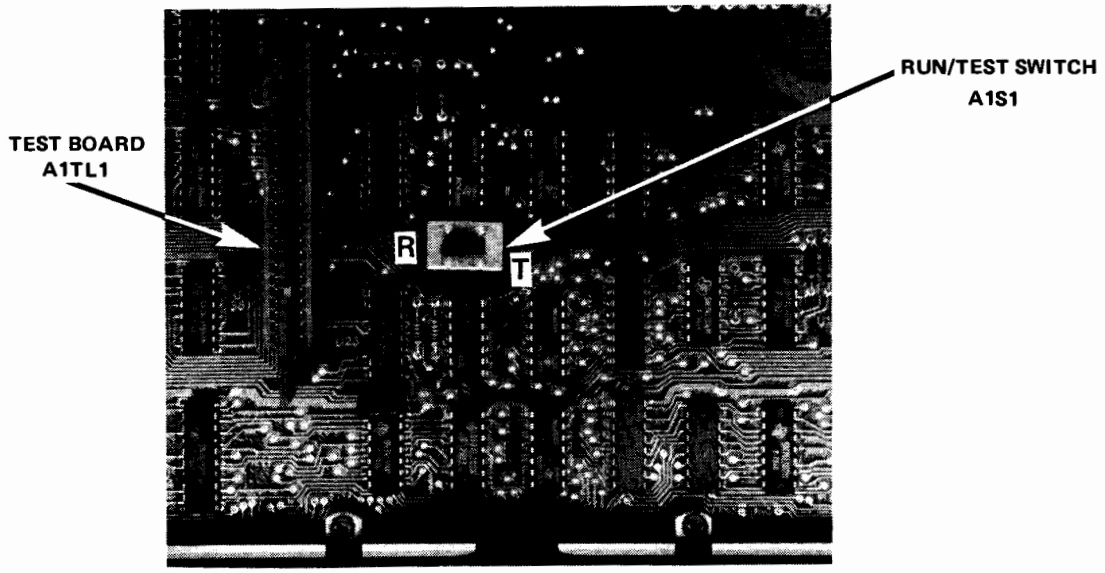


Figure 2-4 Run/Test Switch and Test Board

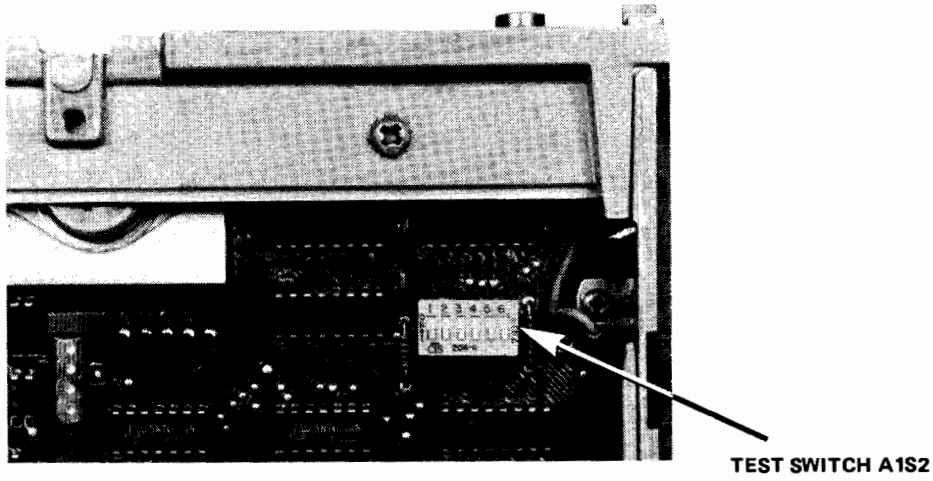


Figure 2-5 Test Switch

2-35 Point-to-Point Coaxial Configuration

2-36 Figure 2-6 shows how two 37203A's can be connected to extend the operating distance between instruments on the HP-IB by using up to 1000 metres of coaxial cable. Up to 14 HP-IB devices can be connected to the 37203A at the local and remote sites.

2-37 The COAX/OPT switch A1S5 should be set to the COAX position on both 37203A's, see Figure 2-8.

2-38 The SERIAL DATA RATE switch on the rear panel of both 37203A's see Figure 3-4, should be set to the rate according to the distance between 37203A's, see Table 3-1.

2-39 The MASTER/SLAVE switch on the rear panel should be set to MASTER on the unit at one end of the serial link and SLAVE on the unit at the other end, see Figure 3-4. As the switch is purely concerned with communication start up, in the event of a serial data error occurring, it is unimportant which way round the MASTER and SLAVE are assigned.

WARNING

When the coaxial cable is used in an out of doors environment, do not remove or connect the coaxial cable from or to the HP-IB Extenders during an electrical storm. To do so could result in a lethal electric shock!

2-40 Point-to-Point Fibre Optic Configuration (Option 001)

2-41 Figure 2-7 shows how two 37203A's can be connected to extend the operating distance between instruments on the HP-IB by using up to 1000 metres of dual fibre optic cable. Up to 14 HP-IB devices can be connected to a 37203A at the local and remote sites.

2-42 The COAX/OPT switch A1S5 should be set to the OPT position on both 37203A's, see Figure 2-8.

2-43 The SERIAL DATA RATE switch on the rear panel of both 37203A's may be set to any rate, see Figure 3-4.

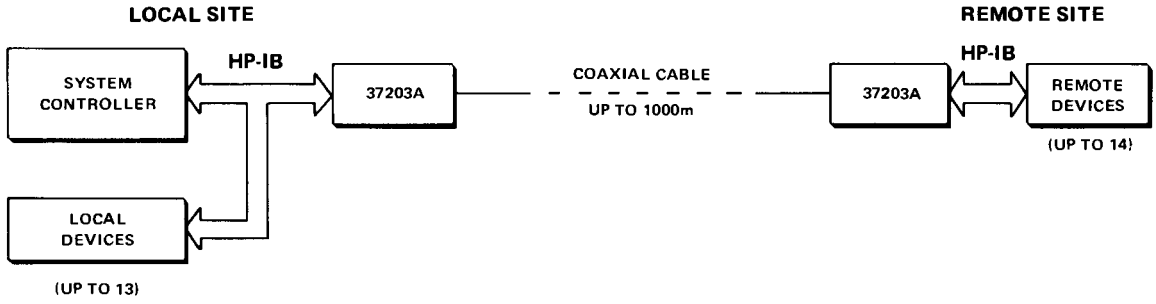


Figure 2-6 Point-to-Point Coaxial Configuration

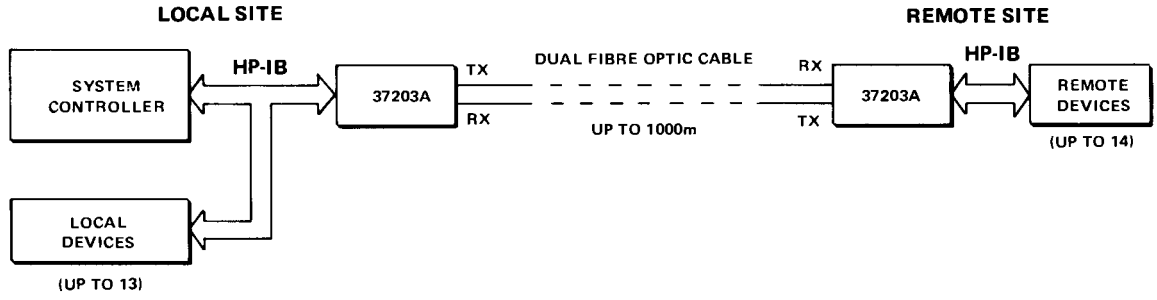


Figure 2-7 Point-to-Point Fibre Optic Configuration

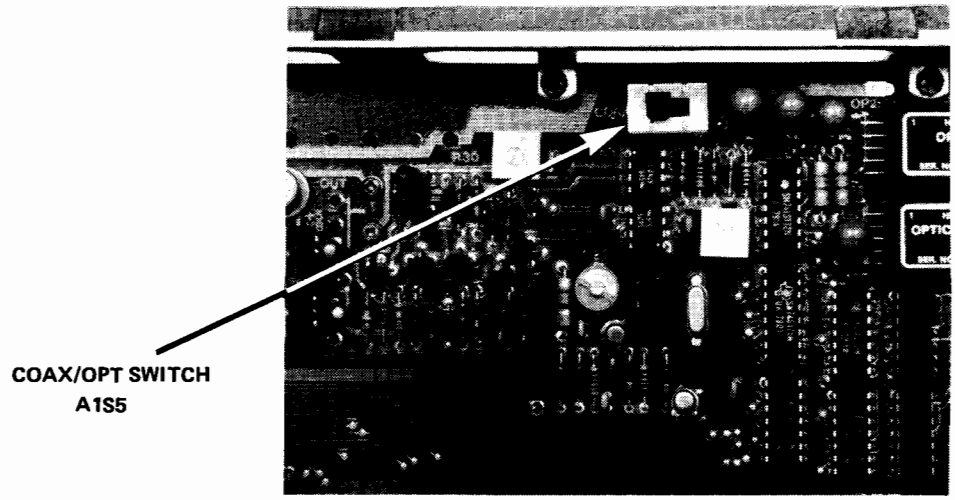


Figure 2-8 COAX/OPT Switch

2-44 The MASTER/SLAVE switch on the rear panel should be set to MASTER on the unit at one end of the serial link and SLAVE on the unit at the other end, see Figure 3-4. As the switch is purely concerned with communication start up, in the event of a serial data error occurring, it is unimportant which way round the MASTER and SLAVE are assigned.

2-45 FIBRE OPTIC CABLE INSTALLATION

2-46 For best results cable installers should observe the following cautions.

2-47 **Storage Temperature.** Cable should be stored at temperatures between $-40^{o}C$ and $+85^{o}C$. Storage at lower temperatures could cause temporary degradation of the optical (loss) properties of the cable. Storage above $85^{o}C$ may cause softening of polyurethane outer cable jacket.

2-48 **Operating Temperature.** HP optical cable assemblies are guaranteed to meet all specified mechanical and performance parameters over the range of $0^{o}C$ to $70^{o}C$ operating. Cables operating outside this range but within the storage temperature range $-40^{o}C$ to $+85^{o}C$ will not be damaged. They will, however, increase in optical attenuation (loss) at the lower temperatures. This increase in optical loss will reduce the operating margin of the optical transmission system and may result in an increase in bit errors below $0^{o}C$.

2-49 **Pull Force on Cable.** Maximum pull force on cable should not exceed 30kg (66 lbs) per channel or 60kg (132 lbs) for duplex. Greater forces may cause stretching and breaking of the optical fibre inside the cable. The light weight of HP optical cable should allow easy installation in most applications without exceeding this limit.

2-50 **Pull Force on Connector.** Maximum pull force applied to the optical connector should not exceed 5kg (11 lbs). This pull strength is designed for reliable and repeated connections and disconnections of the connectors. The connector is not designed to support the pull force of drawing the cable through trays or conduits. Pulling and installation tools should be attached to the cable jacket several inches away from the optical connectors.

2-51 **Bending Radius of Cable.** The minimum safe bend diameter of the HP optical cable is 1.4cm (0.6"). Any tighter bending places a severe stress on the internal glass fibre and can result in breakage of the optical path.

2-52 Care should be taken that at no time during installation or use the cable is kinked, knotted, or bent into a loop smaller than 0.6". All installation pulleys, bends in conduits and corners to be turned should be checked for or built up to this diameter. HP optical cable has been designed and tested to withstand at least 50,000 repeated bends to the 1.4cm specified diameter, so observing these procedures should assure that no cable is damaged during installation.

2-53 **Crushing Force and Impact Resistance.** HP optical cable has been designed and tested to withstand crush loads and impacts equal to or greater than wire cables can tolerate. The cables can be stepped or even driven over without damage if laid on a flat surface. (This is not recommended as standard practice.) They can be installed along floorboards or under carpets if required. Standard precautions must be observed to avoid cutting the cable with a sharp object, snagging it with passing equipment, slamming it in a door or tripping over it. These problems could break the cable completely, or could exceed the minimum bending diameter and break the inner glass fibre.

2-54 **Scuffing and Abrasion.** The cable jacket is polyurethane, a tough, smooth plastic material with excellent abrasion resistance. Surface scuffs and abrasion to this jacket, should they occur, will not affect cable performance, since the optical fibre path lies in the centre of the cable, protected by buffering jackets and tough, aramid fibre strength members.

2-55 **Suspending the Cable.** Due to the light weight and high tensile strength of the HP optical cable, it can support almost 4000 metres (13,000 ft) of its own weight. It can thus be suspended along walls or over dropped ceilings if necessary.

2-56 **Cable to Cable Interconnection.** Only one length of cable can be used between 37203A units, i.e. no cable to cable interconnections are permitted.

2-57 **Resistance to Solvents and Moisture.** HP optical cables are specified for operation in environments with relative humidity up to 95%. Cable jacketing is polyurethane. The cable should perform as well as or better than standard copper cable similarly jacketed.

2-58 **Outdoor Use.** Although the cable jacket contains additives to retard damage by ultra-violet rays (sunlight) it is not specified or tested for outdoor use. If the cable must be used outdoors, make every effort to control the cable environment to stated specifications; otherwise, performance and useable life of the cable may be degraded.

2-59 Connecting Fibre Optic Cable

2-60 The HP optical connectors contain precision ferrules which maintain close tolerance optical fibre alignment to the optical ports of the 37203A. These connectors should be screwed in snugly by holding the connector in one hand and tightening the coupling nut "finger tight" with the other.

Note: Coupling nut "finger tight" torque is defined as 0.05 to 0.10 Newton-metres.

CAUTION

No wrenches, gloves, rags or tools should be used for added leverage on the connector nut. Excessive tightening of the knurled nut will result in misalignment and possible permanent damage to the connector or the optical ports.

2-61 STORAGE AND SHIPMENT

2-62 Environment

2-63 The instrument may be stored or shipped in environments within the following limits:

Temperature	-40^{o}C to $+75^{o}$C
Altitude	up to 15,300 metres (50,000 feet)

The instrument should also be protected from temperature extremes which could cause condensation within the instrument.

2-64 Packaging

2-65 **Tagging for Service.** If the instrument is being returned to Hewlett-Packard for service, please complete one of the blue repair tags at the end of this section and attach it to the instrument.

2-66 **Original Packaging.** Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container 'FRAGILE' to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-67 **Other Packaging.** The following general instructions should be used for re-packing with commercially available materials:

(a) Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service centre, attach tag indicating type of service required, return address, model number, and full serial number.)

(b) Use strong shipping container. A double-wall carton made of 200-pound test material is adequate.

(c) Use a layer of shock absorbing material 50 to 75mm (2 to 3 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect the control panel with cardboard.

(d) Seal shipping container securely.

(e) Mark shipping container FRAGILE to ensure careful handling.

(f) In any correspondence, refer to instrument by model number and full serial number.

SECTION III

OPERATION

3-1 INTRODUCTION

3-2 This section of the manual explains the operating characteristics and the function of the controls and indicators of the Model 37203A HP-IB Extender.

3-3 OPERATING CHARACTERISTICS

3-4 A basic description of the 37203A is given in Section I Paragraph 1-22 to 1-30. The following paragraphs describe some aspects of the 37203A Operating Characteristics in more detail.

3-5 Rejection of Electrical Interference

3-6 The coaxial cable driver/receiver circuit is isolated by optical couplers which enables the circuit to float free from ground, limited to approximately ± 24V by a varistor. This provides protection from differing ground potentials at the two ends and from the effects of induced interference in the cable, by preventing earth currents. Data is transferred to and from the floating circuit through the optical couplers. Rejection of all but extremely severe electrical interference is assured when using coaxial cable with 100% screening.

3-7 Transmitted data frames are also checked by a 4-bit Cyclic Redundancy Check Code. This provides some additional protection from HP-IB errors.

3-8 Transparent HP-IB Extension

3-9 'Transparent', in the context used here, means that HP-IB functional operation is maintained when the 37203A's are introduced. Occasionally, however, program alterations may be necessary to accommodate slightly changed timing relationships.

3-10 The function of 'transparent' extension provided by each of the 37203A's is to accept data from, or source data onto, each bus on behalf of instruments at the opposite end. Bytes are passed between distant buses effectively without transit buffer storage, which means that at no time does unwanted data need to be flushed from the buffers, e.g. upon change of data direction, as in other extenders.

3-11 No special programming is required when using the 37203A's which are fully transparent. The timing relationships of operational events may, however, be slightly altered in the case of fast devices when the 37203A's are introduced.

3-12 Performance with the Parallel Poll Function

3-13 The 37203A supports the Parallel Poll Function but results in a small departure from the IEEE 488 Standard. Due to absolute transmission delay, no Extender, including the 37203A, can guarantee a correct and up-to-date Parallel Poll response from devices distant from the controller within the 2μs which the Standard requires. Instead a pair of 37203A's return the response from distant devices, as rapidly as possible, to the polling controller, and within a time shown in Table 3-1.

3-14 Between the poll being conducted by the controller and the response becoming available from the remote end, the DIO lines at the local Extender are held in the passive (false) condition to prevent the lines being interpreted erroneously.

3-15 Performance with Service Request Function

3-16 The pair of 37203A's communicate the Service Request message (SRQ) to the controller within the times shown in Table 3-1.

Table 3-1 Distance and Speed of Operation at the different Serial Data Rates

	Coaxial Cable (see Note 2)				Fibre Optic Cable (Opt 001)		
	Short (at normal speed) *see Note 1*	250m (max range at normal speed)	500m (max range at 1/4 speed)	1000m (max range at 1/16 speed)	Short *See Note 1*	⩽250m	⩽1000m
Max HP-IB byte transfer rate (k byte/s)	50	40	14.5	2.75	50	39	25
Max SRQ propagation delay (μs)	14	18	55	200	14	20	30
Max Parallel Poll response time (μs)	20	25	75	270	20	25	40

Note 1: For distances <250m, interpolate between Short and 250 columns.

Note 2 These results were achieved using the recommended coaxial cable (Belden cable type 9248)

3-17 Serial Data Rate Settings

3-18 When the serial link is dual fibre optic cable the serial data rate may be set to NORMAL regardless of the length of dual fibre optic cable.

3-19 When the serial link is coaxial cable the serial data rate must be reduced as the length of the coxial cable increases, see Table 3-1. This is due to the following characteristics of coaxial cable:

> As the length of the coaxial cable increases the attenuation increases and the bandwidth decreases. These characteristics result in the high frequency components of the Transmit waveform of the data frame being distorted. This degradation of the waveform ultimately results in serial data errors. Reducing the serial data rate minimises the degradation and so maintains the integrity of the serial link.

3-20 The recommended coaxial cable has:

a) 75Ω impedance.

b) loss not exceeding 6.9dB per 100 metres at 100MHz.

c) dc resistance (inner plus outer conductors) not exceeding 4.1Ω per 100 metres.

d) 100% shield coverage, see Paragraph 3-6.

3-21 Inferior cable may be used providing that the total loss and resistance does not exceed that of the recommended cable at its maximum distance. Coaxial cable with reduced shield coverage may be used if the environment is not electrically noisy.

3-22 System Configurations

3-23 The 37203A can only be used in pairs, so multiple drops from the cable are not possible. However, further pairs of 37203A's can be used to support additional clusters of remote devices in arrangements which avoid loops. In these system configurations the serial link may be either coaxial cable or dual fibre optic cable.

3-24 The 37203A pairs may be arranged in a star configuration where the pairs are connected in parallel, see Figure 3-1. In this configuration a total of 14 HP-IB devices can be connected to any remote bus. The total number of devices in a system is limited by the addressing capability of the HP-IB.

3-25 The 37203A pairs may be arranged in a tandem configuration where the pairs are connected in series, see Figure 3-2. In this configuration a total of 13 HP-IB devices can be connected to any remote bus. The total number of devices in a system is limited by the addressing capability of the HP-IB.

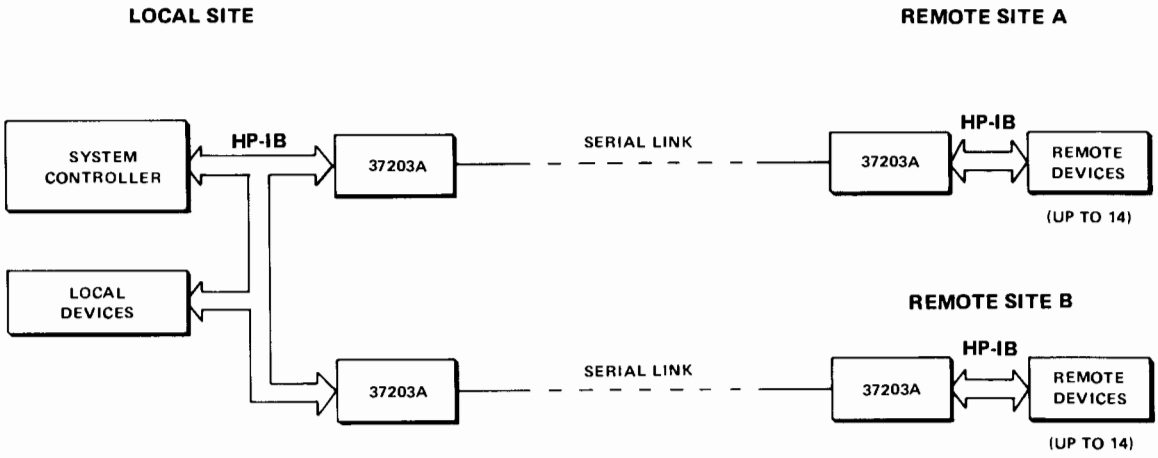


Figure 3-1 Star Configuration

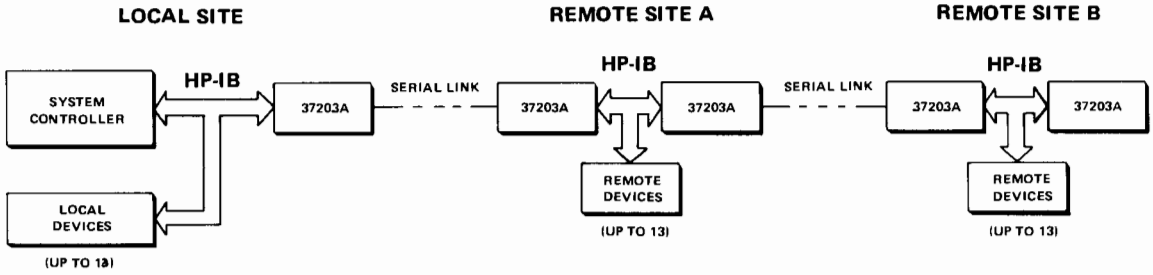
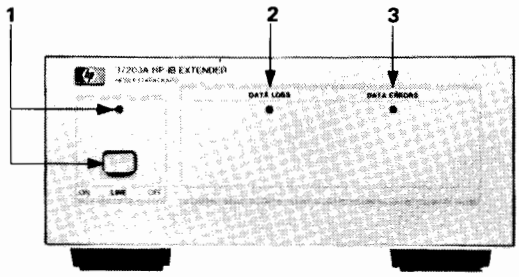


Figure 3-2 Tandem Configuration

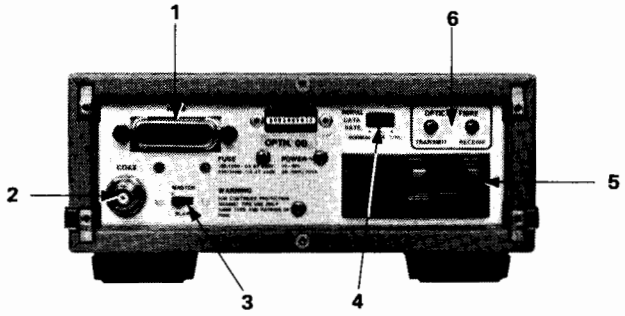
3-26 FRONT AND REAR PANEL FEATURES

3-27 The front and rear panel features on the 37203A are described in Figures 3-3 and 3-4.



1. LINE. The LINE switch, switches the ac supply ON or OFF. A line-on indicator is illuminated to give a visual indication of when the instrument is in the 'line-on' condition.
2. DATA LOSS. The DATA LOSS indicator gives a visual indication of a loss of data frames.
3. DATA ERRORS. The DATA ERRORS indicator gives a visual indication that an error has been detected by the Cyclic Redundancy Check Code. The indicator flashes when an error has been detected but will stay on continuously if many errors occur.

Figure 3-3 37203A HP-IB Extender Front Panel Features



1. Connector for the HP-IB; used to connect the 37203A to the HP-IB.
2. Connector for the coaxial cable; used for interconnecting 37203A's for distances up to 1000 metres.
3. MASTER/SLAVE. The MASTER/SLAVE switch should be set to Master on the unit at one end of the serial link and Slave on the unit at the other end. It is unimportant which way round the Master and Slave are assigned.
4. SERIAL DATA RATE. The SERIAL DATA RATE switch sets the speed of operation of the 37203A. Reducing the serial data rate allows the maximum transmission distance by coaxial cable to increase up to a maximum of 1000 metres.
5. Power Module connection receptacle with fuse and line voltage selector. Figure 2-1 indicates the method of selecting the line voltage.
6. Connectors for the fibre optic cables (Option 001); used for interconnecting 37203A's for distances up to 1000 metres.

Figure 3-4 37203A HP-IB Extender Rear Panel Features

3-28 OPERATOR's MAINTENANCE

3-29 Fibre Optics

3-30 No grease, dirt or other foreign material should be allowed to collect on the alignment ferrule of the optical connector. Dirt at this point can reduce the optical signal and may scratch the fibre end during connector insertion. If a dirty ferrule is observed or suspected, the ferrule tip can be cleaned with a swab moistened in alcohol.

3-31 Service and Repair

3-32 HP optical cables are not customer or field repairable. They contain optical waveguide and precision optical interfaces which must be repaired or replaced at the factory.

3-33 A damaged connector or a cable broken at the connector would normally be repaired by cutting off the damaged section and installing new connectors.

3-34 Consult with the local Hewlett-Packard Sales and Service Office, listed at the rear of this manual, for directions on what action to take.

SECTION IV

PERFORMANCE VERIFICATION

4-1 INTRODUCTION

4-2 The 37203A's are used in pairs and are designed to work with virtually all bus-compatible equipment, provided such equipment conforms to IEEE Standard 488-1978. The 37203A is transparent to all HP-IB functions. The performance verification routines check that the 37203A supports these HP-IB functions.

4-3 PERFORMANCE VERIFICATION ROUTINES

4-4 The Performance Verification routines are supplied on data cartridge HP 37203-12101. A list of routines is given in Table 4-1.

4-5 EQUIPMENT REQUIRED

4-6 Equipment required to run the Performance Verification is as given in table 4-2.

Table 4-1 Performance Verification Routines

Routine
REMOTE ENABLE
SERVICE REQUEST TEST
PARALLEL POLL TEST
CONTROLLER SENDS LISTEN ADDRESS
CONTROLLER SENDS UNLISTEN
CONTROLLER SENDS TALK ADDRESS
CONTROLLER SENDS UNTALK
CONTROLLER SOURCES 0-255
CONTROLLER ACCEPTS 0-255
CONTROL PASSES TO INTERFACE 8

Table 4-2 Equipment Required

Quantity	Item	Type
1	Desktop Computer	HP 9825A
1	String & Advanced Programming ROM	HP 98210A
1	General I/O & Extended I/O ROM	HP 98213A
2	HP-IB Interface Card	HP 98034A
2	HP-IB Bus Extender	HP 37203A
1	Coax Cable	–
1	Performance Verification Tape	HP 37203-12101

4-7 SELECT CODE AND INTERFACE ADDRESS

4-8 Before the Performance Verification can be run one of the HP 98034A HP-IB Interface Cards select code and interface address needs to be changed.

4-9 The select code switch is accessible through a small hole on top of the interface case. The switch is preset to select code 7 at the factory. The select code should be set to 8 by rotating the switch using a small screwdriver.

4-10 The interface address switch is situated internally and the interface covers should be removed, see Figure 4-1.

4-11 Follow these steps to change the interface address switches.

1. Remove the 8 screws as shown in Figure 4-1.
2. Remove edge connector.
3. Carefully separate the two printed circuit boards.
4. Set the switches as illustrated in Figure 4-1. Switches 1 to 5 select the address (octal 26, bit 5 is the most significant bit and setting each switch to the "ON" position corresponds to a "0"). Switch 6 the System Controller enable switch should be set to OFF because only one system controller is allowed in a system.
5. To reassemble ensure that the five pin connectors on one board are aligned with their sockets on the other board.
6. Reconnect the edge connector.
7. Position the cable wires so that they are not crimped as the interface case is pressed together.
8. Replace all the screws.

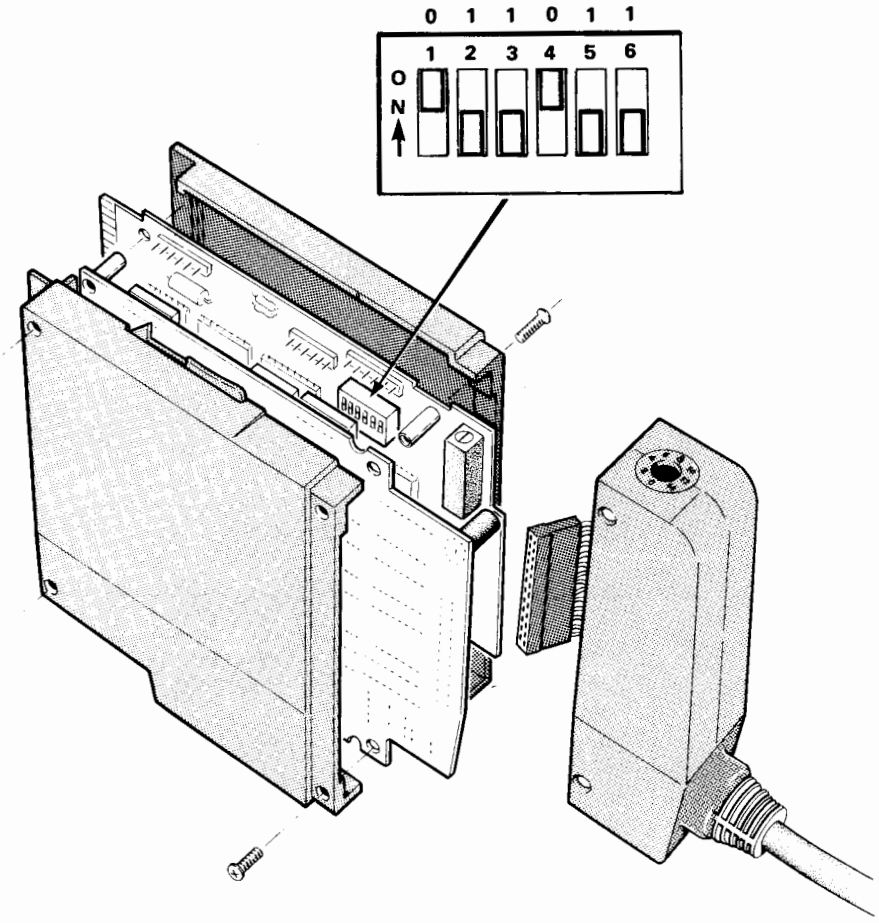


Figure 4-1 HP 98034A Interface Card

4-12 The other HP 98034A HP-IB Interface Card should be left set to the factory preset values; select code 7, interface address octal 25, system control enable on.

Note: Both interface cards Parallel Poll Sense and Parallel Poll Bit should be left set to their factory preset values, position 1 and Bit 1 respectively.

4-13 Table 4-3 summarises the HP 98034A HP-IB Interface Cards switch settings.

4-14 PERFORMANCE VERIFICATION SYSTEM CONFIGURATION

4-15 Connect the Desktop Computer, HP-IB Interface Cards and HP-IB Extenders as shown in Figure 4-2 and explained in paragraph 4-16.

4-16 These steps should be followed carefully to ensure correct configuration.

1. Connect the two 37203A's using a coax cable.
2. Ensure that both 37203A's have switch A1S5 set to COAX; A1S1 set to RUN; A1S2 switches all set to OFF and A1TL1 in RUN mode.
3. Set the Serial Data Rate switch to Normal on both 37203A's.
4. Set the 'Local' 37203A to MASTER.
5. Set the 'Remote' 37203A to SLAVE.
6. Connect the HP-IB Interface Card with select code 7 to the Master 37203A HP-IB connector.
7. Connect the HP-IB Interface Card with select code 8 to the Slave 37203A HP-IB connector.
8. Insert both cards into separate I/O slots on the rear panel of the HP 9825A.

4-17 DESKTOP COMPUTER & HP-IB INTERFACE CARD VERIFICATION

4-18 Before the Performance Verification is run the desktop computer and HP-IB interface cards should be checked to ensure they have been configured correctly.

Table 4-3 HP 98034A Switch Settings

Function	Setting	
Select Code	7	8
Desktop Computer Address	Talk = U Listen = 5	Talk = V Listen = 6
System Controller	ON	OFF
Parallel Poll Sense	Negative – True Logic (Position 1)	Negative – True Logic (Position 1)
Parallel Poll Bit	Bit 1 (least significant bit)	Bit 1 (least significant bit)

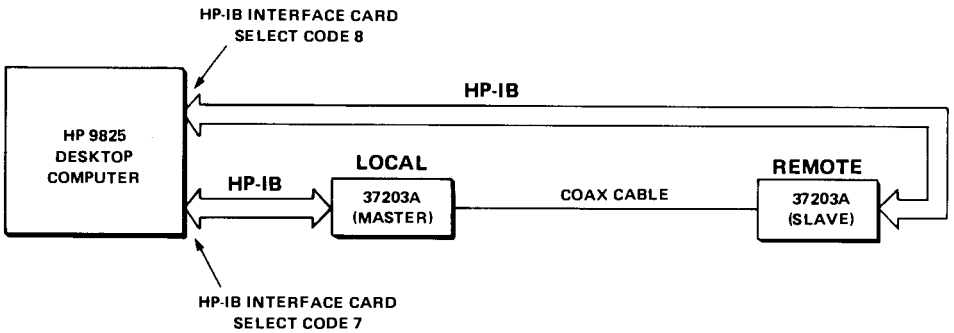


Figure 4-2 Performance Verification System Configuration

4-19 Insert the Performance Verification Cartridge 37203-12101 into the HP 9825A tape transport.

4-20 Switch on all the equipment .

4-21 Ensure that both DATA LOSS and DATA ERROR leds are off. If either of the lamps are on, check that the Serial Data Rate is set to NORMAL on both 37203A's and that one 37203A is set to Master and the other Slave. If either lamp is still on refer to the General Service Sheet G1 in Section VIII.

4-22 Press Special Function Key [f_0] .

4-23 Verify the display:

0.00 213.00 68.00 76.00

4-24 This verifies the HP-IB Interface Card with select code 7.

4-25 If the display is verified proceed to Paragraph 4-26. If the display is not verified switch the 37203A's OFF then ON and repeat Paragraph 4-22. If the display is still not verified check the HP-IB Interface Card switch settings (see Table 4-3); if this is correct the HP-IB Interface Card is defective.

4-26 Press Special Function Key [f_1] .

4-27 Verify the display:

0.00 214.00 68.00 4.00

4-28 This verifies the HP-IB Interface Card with select code 8.

4-29 If the display is not verified switch the 37203A's OFF then ON and repeat Paragraph 4-26. If the display is still not verified check the HP-IB Interface Card switch settings (see Table 4-3); if this is correct the HP-IB Interface Card is defective.

4-30 This completes the Desktop Computer and HP-IB Interface Card verification. The system is ready to verify that the two 37203A's function correctly.

4-31 Before running the Performance Verification routines ensure that the DATA LOSS and DATA ERRORS leds are off. If either of the lamps are on check the Serial Data Rate switch is set to Normal on both 37203A's and that one 37203A is set to Master and the other Slave. If either lamp is still on refer to General Service Sheet G1 in Section VIII.

4-32 To run the Performance Test routines press [f_2] .

4-33 A successful verification is indicated by:

PROGRAM SUCCESSFULLY COMPLETED

being displayed on the 9825.

4-34 If a Performance Verification routine fails an error message will be displayed. Power both 37203A's OFF then ON and repeat paragraph 4-32. If the routine fails again refer to General Service Sheet G1 in Section VIII.

SECTION V

ADJUSTMENTS

5-1 INTRODUCTION

5-2 This section describes the adjustments required to return the instrument to peak operating capabilities when repairs have been made. Included in this section are adjustment procedures, adjustment location diagrams and a table of adjustable components.

5-3 Adjustments should only be made after ascertaining that the instrument is out of calibration. To avoid any interaction between adjustments, the procedures in this section should be performed in the order given.

5-4 Table 5-1 is a list of the adjustable components with related information. The location of each of the adjustable components is shown in Figure 5-1.

5-5 EQUIPMENT REQUIRED

5-6 Equipment required for the adjustments is listed in the table of Recommended Test Equipment in Section I. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended models.

5-7 SAFETY CONSIDERATIONS

5-8 This section contains warnings and cautions that must be followed for your protection and to avoid damage to the equipment.

WARNING

Maintenance described herein is performed with protective covers removed and power applied to the instrument. Maintenance should be performed only by service trained personnel who are aware of the hazards involved.

Table 5-1 Adjustable Components

Adjustment Name	Reference Designator	Adjustment Paragraph	Service Sheet	Description
24MHz OSCILLATOR	A1C25	5-11	A1	Adjusts 24MHz crystal oscillator
TRANSMIT DATA-SKEW	A1R17	5-12	A1	Adjusts input to optocoupler U62
RECEIVE DATA-SKEW	A1R30	5-13	A1	Adjusts input to optocoupler U63

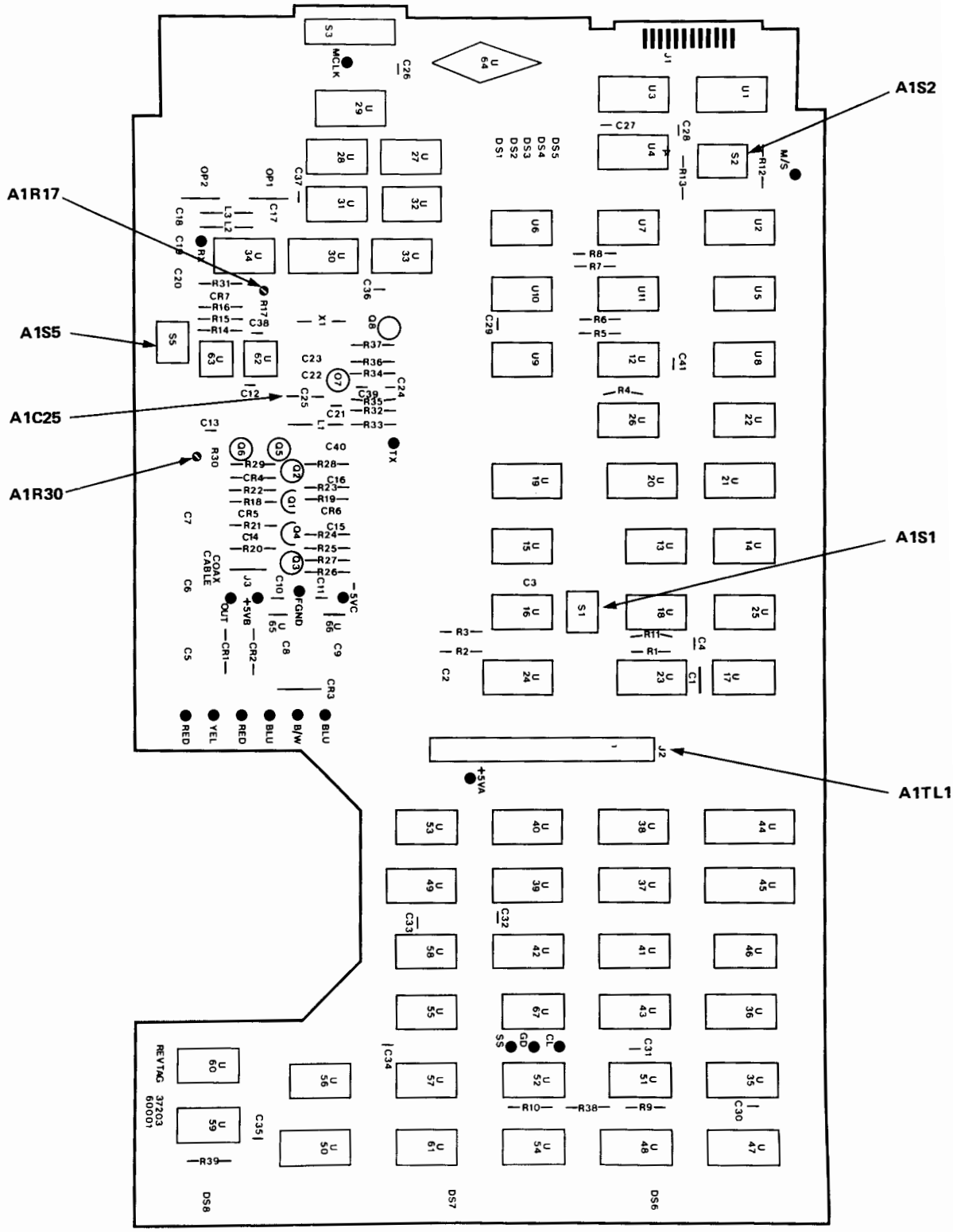


Figure 5-1 Location of Adjustable Components

5-9 ADJUSTMENT PROCEDURE

5-10 Preliminary Procedure

1. Remove top cover.

5-11 24MHz OSCILLATOR ADJUSTMENT

DESCRIPTION

This adjustment tunes the oscillator to 24MHz.

EQUIPMENT

Frequency counter . . . . . hp 5302A

PROCEDURE

1. Connect the counter to Test Point MCLCK on A1.
2. Adjust A1C25 to obtain a frequency of 24 ± 0.25MHz.

5-12 TRANSMIT DATA – SKEW ADJUSTMENT

DESCRIPTION

This adjustment provides the correct mark-space ratio of the output signal to the coaxial cable, to compensate for the opto-coupler.

EQUIPMENT

Oscilloscope . . . . . hp 180C, 1809A, 1825A
10:1 Probe . . . . . hp 10004D

PROCEDURE

1. Set the SERIAL DATA RATE switch on the rear panel to NORMAL.
2. Set the MASTER/SLAVE switch on the rear panel to MASTER.
3. Set the COAX/OPT switch A1S5 to COAX.
4. Set the R/T switch A1S1 to R.
5. Set switch 6 of A1S2 to ON and switches 1-5 switch OFF.
6. Set the plug-in card A1TL1 located in J2 to the RUN position.
7. Connect the oscilloscope to Test Point OUT on A1 using Test Point FGND on A1 to ground the oscilloscope probe.
8. Switch the 37203A OFF for 5 seconds then ON.
9. Set the oscilloscope to 0.05μs/cm, negative trigger and when using the 10:1 probe to 0.2V/cm.
10. Adjust X-POSITION to centre transition between bits 1 and 2 on the vertical middle line of the graticule, see Figure 5-2.

11. Adjust Y-POSITION to put ground level in the middle of the trace.

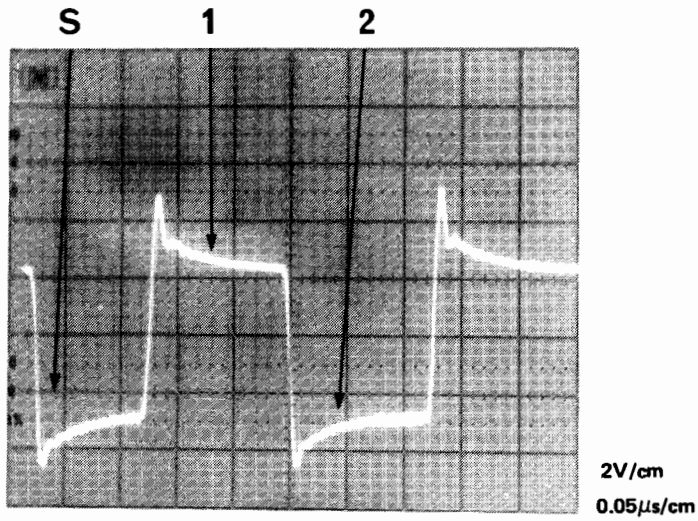


Figure 5-2 Transmit Skew

12. Adjust A1R17 to make the duration of bits 1 and 2 equal at the mid-amplitude of the waveform. Use the X-POSITION to exactly centre the transition on the vertical middle line of the oscilloscope as the adjustment is being made.

13. Disconnect Oscilloscope.

5-13 RECEIVE DATA – SKEW ADJUSTMENT

DESCRIPTION

This adjustment provides the correct mark-space ratio of the incoming data signal to compensate for the optocoupler.

EQUIPMENT

Oscilloscope	hp 180C, 1809A, 1825A
10:1 Probe	hp 10004D

PROCEDURE

1. Set the SERIAL DATA RATE switch on the rear panel to NORMAL.

2. Set the MASTER/SLAVE switch on the rear panel to MASTER.

3. Set the COAX/OPT switch on A1S5 to coax.

4. Set the R/T switch A1S1 to R.

5. Set switch 6 of the A1S2 to ON and switches 1-5 switch OFF.

6. Set the plug-in card A1TLĺ located in J2 to the RUN position.

7. Connect the oscilloscope to Test Point RX on A1.

8. Switch the 37203A OFF for 5 seconds then ON.

9. Set the oscilloscope to 0.05μs/cm, positive trigger and when using the 10:1 probe 0.2V/cm.

10. Adjust the X-POSITION to centre the transition between bits 1 and 2 on the vertical middle line of the graticule, see Figure 5-3.

11. Adjust the Y-POSITION to put ground on the 0V line.

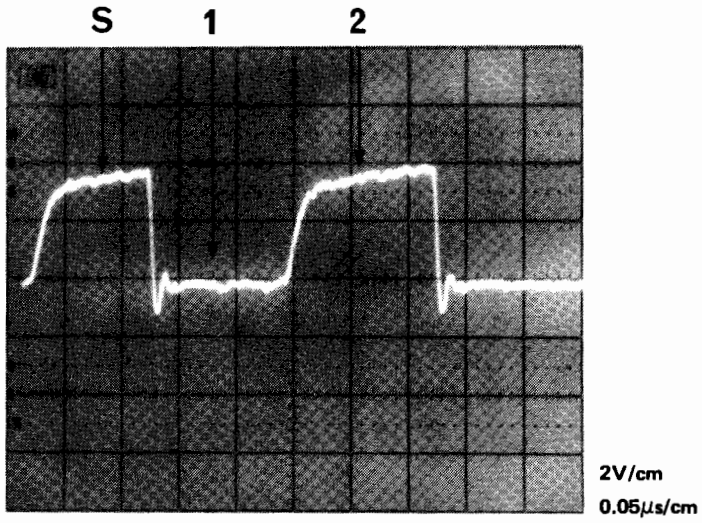


Figure 5-3 Receive Skew

12. Adjust A1R30 to make the durations of bits 1 and 2 equal at the +1.4V level. Use the X-POSITION to exactly centre the transition on the +1.4V level as the adjustment is being made.

13. Disconnect oscilloscope.

SECTION VI

REPLACEABLE PARTS

6-1 INTRODUCTION

6-2 This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers code numbers.

6-3 ABBREVIATIONS

6-4 Table 6-1 lists all abbreviations used in the parts list, the schematics and throughout the manual. In some cases two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower and upper case letters.

6-5 REPLACEABLE PARTS LIST

6-6 Table 6-2 is the list of replaceable parts and is organised as follows:

(a) Electrical assemblies and their components in alpha-numeric order by reference designation.

(b) Chassis-mounted parts in alpha-numeric order by reference designation.

(c) Miscellaneous parts.

The information given for each part consists of the following:

(a) The Hewlett-Packard part number.

(b) Part number check digit (CD).

(c) The total quantity (Qty) in the instrument.

(d) The description of the part.

(e) A typical manufacturer of the part in a five-digit code.

(f) The manufacturers number for that part.

The total quantity for each part is given only once – at the first appearance of the part in the list.

6-7 ORDERING INFORMATION

6-8 To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-9 To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

6-10 DIRECT MAIL ORDER SYSTEM

6-11 Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

(a) Direct ordering and shipment from the HP Parts Centre in Mountain View, California.

(b) No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

(c) Prepaid transportation (there is a small handling charge for each order).

(d) No invoices – to provide these advantages, a cheque or money order must accompnay each order.

6-12 Mail Order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1 Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A . . . . . assembly
AT . . attenuator; isolator; termination
B . . . . . fan; motor
BT . . . . . battery
C . . . . . capacitor
CP . . . . . coupler
CR . . . . . diode; diode thyristor; varactor
DC . . . directional coupler
DL . . . . . delay line
DS . . . . . annunciator; signaling device (audible or visual); lamp; LED
E . . . . . miscellaneous electrical part
F . . . . . fuse
FL . . . . . filter
H . . . . . hardware
HY . . . . . circulator
J . . . electrical connector (stationary portion); jack
K . . . . . relay
L . . . . . coil; inductor
M . . . . . meter
MP . . . . . miscellaneous mechanical part
P . . . electrical connector (movable portion); plug
Q . . . . . transistor: SCR; triode thyristor
R . . . . . resistor
RT . . . . . thermistor
S . . . . . switch
T . . . . . transformer
TB . . . . . terminal board
TC . . . . . thermocouple
TP . . . . . test point
U . . . . . integrated circuit; microcircuit
V . . . . . electron tube
VR . . . voltage regulator; breakdown diode
W . . . . cable; transmission path; wire
X . . . . . socket
Y . . . . crystal unit (piezo-electric or quartz)
Z . . . . tuned cavity; tuned circuit

ABBREVIATIONS

A . . . . . ampere
ac . . . . alternating current
ACCESS . . . . . accessory
ADJ . . . . . adjustment
A/D . . . . analog-to-digital
AF . . . . . audio frequency
AFC . . . . . automatic frequency control
AGC . . . . . automatic gain control
AL . . . . . aluminum
ALC . . . . . automatic level control
AM . . . amplitude modulation
AMPL . . . . . amplifier
APC . . . . automatic phase control
ASSY . . . . . assembly
AUX . . . . . auxiliary
avg . . . . . average
AWG . . . . American wire gauge
BAL . . . . . balance
BCD . . . . . binary coded decimal
BD . . . . . board
BE CU . . . . . beryllium copper
BFO . . . . . beat frequency oscillator
BH . . . . . binder head
BKDN . . . . . breakdown
BP . . . . . bandpass
BPF . . . . . bandpass filter
BRS . . . . . brass
BWO . . . . . backward-wave oscillator
CAL . . . . . calibrate
ccw . . counter-clockwise
CER . . . . . ceramic
CHAN . . . . . channel
cm . . . . . centimeter
CMO . . cabinet mount only
COAX . . . . . coaxial
COEF . . . . . coefficient
COM . . . . . common
COMP . . . . . composition
COMPL . . . . . complete
CONN . . . . . connector
CP . . . . . cadmium plate
CRT . . . cathode-ray tube
CTL . . . . complementary transistor logic
CW . . . . . continuous wave
cw . . . . . clockwise
cm . . . . . centimeter
D/A . . . . digital-to-analog
dB . . . . . decibel
dBm . . . . decibel referred to 1 mW
dc . . . . . direct current
deg . . degree (temperature interval or difference)
$^{\circ}$ . . . . . degree (plane angle)
$^{\circ}$C . . . . . degree Celsius (centigrade)
$^{\circ}$F . . . . degree Fahrenheit
$^{\circ}$K . . . . . degree Kelvin
DEPC . . deposited carbon
DET . . . . . detector
diam . . . . . diameter
DIA . . . diameter (used in parts list)
DIFF AMPL . . differential amplifier
div . . . . . division
DPDT . . . . . double-pole, double-throw
DR . . . . . drive
DSB . . . . double sideband
DTL . . . . diode transistor logic
DVM . . . digital voltmeter
ECL . . . . emitter coupled logic
EMF . . electromotive force
EDP . . . . . electronic data processing
ELECT . . . . . electrolytic
ENCAP . . . . encapsulated
EXT . . . . . external
F . . . . . farad
FET . . . . . field-effect transistor
F/F . . . . . flip-flop
FH . . . . . flat head
FIL H . . . . . fillister head
FM . . frequency modulation
FP . . . . . front panel
FREQ . . . . . frequency
FXD . . . . . fixed
g . . . . . gram
GE . . . . . germanium
GHz . . . . . gigahertz
GL . . . . . glass
GRD . . . . . ground(ed)
H . . . . . henry
h . . . . . hour
HET . . . . . heterodyne
HEX . . . . . hexagonal
HD . . . . . head
HDW . . . . . hardware
HF . . . . . high frequency
HG . . . . . mercury
HI . . . . . high
HP . . . . . Hewlett-Packard
HPF . . . . . high pass filter
HR . . . . . hour (used in parts list)
HV . . . . . high voltage
Hz . . . . . Hertz
IC . . . . integrated circuit
ID . . . . . inside diameter
IF . . . . . intermediate frequency
IMPG . . . . . impregnated
in . . . . . inch
INCD . . . . . incandescent
INCL . . . . . include(s)
INP . . . . . input
INS . . . . . insulation
INT . . . . . internal
kg . . . . . kilogram
kHz . . . . . kilohertz
kΩ . . . . . kilohm
kV . . . . . kilovolt
lb . . . . . pound
LC . . . . . inductance-capacitance
LED . . light-emitting diode
LF . . . . . low frequency
LG . . . . . long
LH . . . . . left hand
LIM . . . . . limit
LIN . . . linear taper (used in parts list)
lin . . . . . linear
LK WASH . . . lock washer
LO . . . low; local oscillator
LOG . . . . logarithmic taper (used in parts list)
log . . . . . logrithm(ic)
LPF . . . . . low pass filter
LV . . . . . low voltage
m . . . . . meter (distance)
mA . . . . . milliampere
MAX . . . . . maximum
MΩ . . . . . megohm
MEG . . . . meg (10^6) (used in parts list)
MET FLM . . . . metal film
MET OX . . metallic oxide
MF . . . medium frequency; microfarad (used in parts list)
MFR . . . . . manufacturer
mg . . . . . milligram
MHz . . . . . megahertz
mH . . . . . millihenry
mho . . . . . mho
MIN . . . . . minimum
min . . . . . minute (time)
. . .' . . . . . minute (plane angle)
MINAT . . . . . miniature
mm . . . . . millimeter
MOD . . . . . modulator
MOM . . . . . momentary
MOS . . . . . metal-oxide semiconductor
ms . . . . . millisecond
MTG . . . . . mounting
MTR . . . meter (indicating device)
mV . . . . . millivolt
mVac . . . . . millivolt, ac
mVdc . . . . . millivolt, dc
mVpk . . . . millivolt, peak

NOTE

All abbreviations in the parts list will be in upper-case.

Table 6-1 Reference Designations and Abbreviations (continued)

mVp-p . . . millivolt, peak-to-peak
mVrms . . . . millivolt, rms
mW . . . . . milliwatt
MUX . . . . . multiplex
MY . . . . . mylar
μA . . . . . microampere
μF . . . . . microfarad
μH . . . . . microhenry
μmho . . . . . micromho
μs . . . . . microsecond
μV . . . . . microvolt
μVac . . . . . microvolt, ac
μVdc . . . . . microvolt, dc
μVpk . . . microvolt, peak
μVp-p . . . microvolt, peak-to-peak
μVrms . . . . microvolt, rms
μW . . . . . microwatt
nA . . . . . nanoampere
NC . . . . . no connection
N/C . . . . normally closed
NE . . . . . neon
NEG . . . . . negative
nF . . . . . nanofarad
NI PL . . . . . nickel plate
N/O . . . . . normally open
NOM . . . . . nominal
NORM . . . . . normal
NPN . . . negative-positive-negative
NPO . . . . negative-positive zero (zero temperature coefficient)
NRFR . . not recommended for field replacement
NSR . . . . . not separately replaceable
ns . . . . . nanosecond
nW . . . . . nanowatt
OBD . . . order by description
OD . . . . . outside diameter
OH . . . . . oval head
OP AMPL . . . operational amplifier
OPT . . . . . option
OSC . . . . . oscillator
OX . . . . . oxide
oz . . . . . ounce
Ω . . . . . ohm
P . . . . peak (used in parts list)
PAM . . . . pulse-amplitude modulation
PC . . . . . printed circuit
PCM . . pulse-code modulation; pulse-count modulation
PDM . . . . . pulse-duration modulation
pF . . . . . picofarad
PH BRZ phosphor bronze
PHL . . . . . Phillips
PIN . . . positive-intrinsic-negative
PIV . . . . . peak inverse voltage
pk . . . . . peak
PL . . . . . phase lock
PLO . . . . . phase lock oscillator
PM . . . . phase modulation
PNP . . . positive-negative-positive
P/O . . . . . part of
POLY . . . . . polystyrene
PORC . . . . . porcelain
POS . . positive; position(s) (used in parts list)
POSN . . . . . position
POT . . . . . potentiometer
p-p . . . . . peak-to-peak
PP . . . peak-to-peak (used in parts list)
PPM . . . . . pulse-position modulation
PREAMPL . . . preamplifier
PRF . . . . pulse-repetition frequency
PRR . . . . pulse repetition rate
ps . . . . . picosecond
PT . . . . . point
PTM . . . . . pulse-time modulation
PWM . . . . . pulse-width modulation
PWV . . . . . peak working voltage
RC . . . . . resistance-capacitance
RECT . . . . . rectifier
REF . . . . . reference
REG . . . . . regulated
REPL . . . . . replaceable
RF . . . . . radio frequency
RFI . . . . radio frequency interference
RH . . . . round head; right hand
RLC . . . . . resistance-inductance-capacitance
RMO . . . rack mount only
rms . . . . root-mean-square
RND . . . . . round
ROM . . read-only memory
R&P . . . . . rack and panel
RWV . . . reverse working voltage
S . . . scattering parameter
s . . . . . second (time)
. . . " . second (plane angle)
S-B . . . . . slow-blow (fuse) (used in parts list)
SCR . . . silicon controlled rectifier; screw
SE . . . . . selenium
SECT . . . . . sections
SEMICON . . . . . semiconductor
SHF . . . . . superhigh frequency
SI . . . . . silicon
SIL . . . . . silver
SL . . . . . slide
SNR . . signal-to-noise ratio
SPDT . . . . . single-pole, double-throw
SPG . . . . . spring
SR . . . . . split ring
SPST . . . . . single-pole, single-throw
SSB . . . . . single sideband
SST . . . . . stainless steel
STL . . . . . steel
SQ . . . . . square
SWR . . standing-wave ratio
SYNC . . . . . synchronize
T . . timed (slow-blow fuse)
TA . . . . . tantalum
TC . . . . . temperature compensating
TD . . . . . time delay
TERM . . . . . terminal
TFT . . thin-film transistor
TGL . . . . . toggle
THD . . . . . thread
THRU . . . . . through
TI . . . . . titanium
TOL . . . . . tolerance
TRIM . . . . . trimmer
TSTR . . . . . transistor
TTL . . transistor-transistor logic
TV . . . . . television
TVI television interference
TWT . . traveling wave tube
U . . . . . micro (10^{-6}) (used in parts list)
UF . . . microfarad (used in parts list)
UHF . . ultrahigh frequency
UNREG . . . . unregulated
V . . . . . volt
VA . . . . . voltampere
Vac . . . . . volts, ac
VAR . . . . . variable
VCO . . . voltage-controlled oscillator
Vdc . . . . . volts, dc
VDCW . . volts, dc, working (used in parts list)
V(F) . . . . . volts, filtered
VFO . . variable-frequency oscillator
VHF . . . . . very-high frequency
Vpk . . . . . volts, peak
Vp-p . . volts, peak-to-peak
Vrms . . . . . volts, rms
VSWR . . . voltage standing wave ratio
VTO . . . . . voltage-tuned oscillator
VTVM . . . . vacuum-tube voltmeter
V(X) . . . . . volts, switched
W . . . . . watt
W/ . . . . . with
WIV . . . . working inverse voltage
WW . . . . . wirewound
W/O . . . . . without
YIG . . yttrium-iron-garnet
Z_o . . . . . characteristic impedance

NOTE

All abbreviations in the parts list will be in upper-case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

Table 6-2 Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	37203-60001	5	1	BOARD ASSEMBLY	28480	37203-60001
A1C1	0160-0939	4	1	CAPACITOR-FXD 430PF +-5% 300VDC MICA	28480	0160-0939
A1C2	0160-2204	0	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A1C3	0160-2207	3	1	CAPACITOR-FXD 300PF +-5% 300VDC MICA	28480	0160-2207
A1C4	0180-2814	0	1	CAPACITOR-FXD 22UF+-20% 10VDC TA	28480	0180-2814
A1C5	0180-3029	1	3	CAPACITOR-FXD 2200UF 25V AL	28480	0180-3029
A1C6	0180-3029	1		CAPACITOR-FXD 2200UF 25V AL	28480	0180-3029
A1C7	0180-3029	1		CAPACITOR-FXD 2200UF 25V AL	28480	0180-3029
A1C8	0180-0550	7	2	CAPACITOR-FXD 330UF+100-10% 25VDC AL	28480	0180-0550
A1C9	0180-0550	7		CAPACITOR-FXD 330UF+100-10% 25VDC AL	28480	0180-0550
A1C10	0180-2662	6	2	CAPACITOR-FXD 10UF+-10% 10VDC TA	25088	D4R7081A10K
A1C11	0180-2662	6		CAPACITOR-FXD 10UF+-10% 10VDC TA	25088	D4R7081A10K
A1C12	0160-0576	5	15	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C13	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C14	0140-0196	3	3	CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300MV1CR
A1C15	0140-0196	3		CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300MV1CR
A1C16	0140-0196	3		CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300MV1CR
A1C17	0180-2816	2	4	CAPACITOR-FXD 68uF±20% 10VDC TA	28480	0180-2816
A1C18	0180-2816	2		CAPACITOR-FXD 68uF±20%10VDC TA	28480	0180-2816
A1C19	0180-2816	2		CAPACITOR-FXD 68UF+-20% 10VDC TA	28480	0180-2816
A1C20	0180-2816	2		CAPACITOR-FXD 68UF+-20% 10VDC TA	28480	0180-2816
A1C21	0160-3879	7	2	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C22	0160-2199	2	2	CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2199
A1C23	0140-0199	6	1	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300MV1CR
A1C24	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C25	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A1C26	0180-0418	6	2	CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A1C27	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C28	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C29	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C30	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C31	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C32	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C33	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C34	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C35	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C36	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C37	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C38	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C39	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C40	0160-2199	2		CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2199
A1C41	0180 -0418	6		CAPACITOR-FXD 1UF +-20% 35VDC TA	28480	0180 -0418
A1CR1	1901-0673	5	2	DIODE-PWR RECT 100V 1.5A	28480	1901- 0673
A1CR2	1901-0673	5		DIODE-PWR RECT 100V 1.5A	28480	1901- 0673
A1CR3	1906-0096	7	1	DIODE-FW BRDG 200V 2A	04713	MDA202
A1CR4	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
A1CR5	1901-0539	3	2	DIODE-SCHOTTKY	28480	1901-0539
A1CR6	1901-0539	3		DIODE-SCHOTTKY	28480	1901-0539
A1CR7	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1DS1	1990-0486	6	7	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A1DS2	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A1DS3	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A1DS4	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A1DS5	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A1DS6	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A1DS7	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A1DS8	1990-0485	5	1	LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A1J1	1251-3283	1	1	CONNECTOR 24-PIN F MICRORIBBON	28480	1251-3283
A1J2	1251-3507	2	1	CONNECTOR-PC EDGE 24-CONT/ROW 2-ROWS	28480	1251-3507
A1L1	9140-0096	1	1	COIL-MLD 1UH 10% Q=50 .155DX.375LG-NOM	28480	9140-0096
A1L2	9140-0098	3	2	COIL-MLD 2.2UH 10% Q=33 .155DX.375LG-NOM	28480	9140-0098
A1L3	9140-0098	3		COIL-MLD 2.2UH 10% Q=33 .155DX.375LG-NOM	28480	9140-0098
A1Q1	1854-0215	1	4	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q2	1853-0015	7	2	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
A1Q3	1853-0015	7		TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
A1Q4	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q5	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q6	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q7	1854-0019	3	2	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
A1Q8	1854-0019	3		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
A1R1	0757-0442	9	8	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R2	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A1R3	0698-3449	6	1	RESISTOR 28.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2872-F
A1R4	0698-3447	4	8	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R5	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2 Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R6	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R7	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R8	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R9	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R10	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R11	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R12	0757-0438	3	2	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R13	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R14	0698-3444	1	3	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A1R15	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R16	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A1R17	2100-0554	5	1	RESISTOR-TRMR 500 10% C TOP-ADJ 1-TRN	28480	2100-0554
A1R18	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A1R19	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A1R20	0757-0398	4	2	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A1R21	0698-3442	9	2	RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A1R22	0698-3434	9	2	RESISTOR 34.8 1% .125W F TC=0+-100	24546	C4-1/8-T0-34R8-F
A1R23	0698-3434	9		RESISTOR 34.8 1% .125W F TC=0+-100	24546	C4-1/8-T0-34R8-F
A1R24	0698-3442	9		RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A1R25	0757-0398	4		RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A1R26	0757-0276	7	1	RESISTOR 61.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-61R9-F
A1R27	0757-0427	0	1	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A1R28	0698-0084	9	3	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1R29	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R30	2100-3211	7	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A1R31	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R32	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1R33	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1R34	0698-3439	4	3	RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A1R35	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A1R36	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R37	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A1R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R39	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A1S1	3101-1596	0	3	SWITCH-SL DPDT MINTR 1A 125VAC PC	28480	3101-1596
A1S2	3101-2158	2	1	SWITCH-SL 6-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2158
A1S3	3101-0493	4	1	SWITCH-SLIDE 8P3T 8	28480	3101-0493
A1S4	3101 - 1596	0		SWITCH-SL DPDT MINTR 1A 125VAC PC	28480	3101-1596
A1S5	3101-1596	0		SWITCH-SL DPDT MINTR 1A 125VAC PC	28480	3101-1596
A1TL1	37203-20002	2	1	TEST BOARD	28480	37203-20002
A1U1	1820-1689	4	4	IC UART TTL QUAD	04713	MC3446P
A1U2	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A1U3	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A1U4	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A1U5	1820-1199	1	4	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U6	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U7	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U8	1820-1144	6	5	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U9	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U10	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U11	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U12	1820-1201	6	4	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U13	1820-1197	9	8	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U14	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U15	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U16	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U17	1820-1202	7	4	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U18	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A1U19	1820-1212	9	3	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A1U20	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A1U21	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A1U22	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A1U23	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U24	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U25	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U26	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U27	1820-1478	9	2	IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS93N
A1U28	1820-1478	9		IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS93N
A1U29	1820-1991	1	1	IC CNTR TTL LS DECD DUAL 4-BIT	01295	SN74LS390N
A1U30	1820-1191	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A1U31	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A1U32	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U33	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U34	1820-1197	6		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U35	1820-1276	5	9	IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS194AN

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2 Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U36	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U37	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U38	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U39	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U40	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U41	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U42	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U43	1820-1276	5		IC SHF-RGTR TTL LS R=8 PRL-IN PRL-OUT	01295	SN74LS194AN
A1U44	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U45	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U46	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A1U47	1820-1430	3	2	IC CNTR TTL LS 8IN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U48	1820-1430	3		IC CNTR TTL LS 8IN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U49	1820-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A1U50	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A1U51	1820-1211	8	2	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A1U52	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A1U53	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U54	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U55	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U56	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U57	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U58	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A1U59	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U60	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U61	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U62	1990-0429	7	2	OPTO-ISOLATOR LED-IC GATE IF=10MA-MAX	28480	1990-0429
A1U63	1990-0429	7		OPTO-ISOLATOR LED-IC GATE IF=10MA-MAX	28480	1990-0429
A1U64	1826-0181	1	1	IC V RGLTR TO-3	27014	LM323K
	37203-00004	2	1	HEAT SINK	28480	37203-00004
A1U65	1826-0122	0	1	IC 7805 V RGLTR TO-220	07263	7805UC
A1U66	1826-0445	0	1	IC 7905 V RGLTR TO-220	07263	UA7905UC
A1U67	1820 - 1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1Y1	0410-1217	4	1	CRYSTAL-24MHZ	28480	0410-1217

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2 Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				37203A MAIN LIST		
A1	37203-60001	5		BOARD ASSEMBLY	28480	37203-60001
C1	0160-3561	4	1	CAPACITOR-FXD 1000PF/1000PF +100-0%	28480	0160-3561
C2	0150-0096	3	1	CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0150-0096
F1	2110-0201	0	1	FUSE .25A 250V 1.25X.25 UL (115V OPERATION)	75915	313.250
F1	2110-0318	0	1	FUSE .125A 250V 1.25X.25 UL (250V OPERATION)	75915	313.125
MP1	37203-00001	9	1	FRONT PANEL	28480	37203-00001
MP2	37203-00003	1	1	FRONT PANEL-SUB	28480	37203-00003
MP3	5020-8813	8	1	FRAME-FRONT	28480	5020-8813
MP4	5040-7203	0	1	TRIM STRIP-TOP	28480	5040-7203
MP5	5020-8830	9	2	SIDE STRUT	28480	5020-8830
MP6	5060-9818	9	1	COVER-TOP	28480	5060-9818
MP7	5060-9963	5	1	COVER-BOTTOM	28480	5060-9963
MP8	5040-7201	8	4	FOOT(STANDARD)	28480	5040-7201
MP9	5001-0438	7	2	TRIM STRIP-SIDE	28480	5001-0438
MP10	37203-00002	0	1	REAR PANEL	28480	37203-00002
MP11	5020-8814	9	1	FRAME-REAR	28480	5020-8814
MP12	37203-00006	4	1	BRACKET-TRANSFORMER	28480	37203-00006
MP13	37203-00005	3	1	BRACKET-SWITCH	28480	37203-00005
RV1	0837-0204	6	1	VARISTOR-24V	28480	0837-0204
S1	3101-2216	3	1	SW-PB DPDT	28480	3101-2216
	5041-0268	5	1	KEY CAP	28480	5041-0268
T1	37203-80001	7	1	TRANSFORMER	28480	37203-80001
W1	37203-60011	7	1	CABLE ASSEMBLY-POWER	28480	37203-60011
W2	37203-60010	6	1	CABLE ASSEMBLY-COAX	28480	37203-60010
	00310-48801	0	2	INSULATOR-BNC	28480	00310-48801
				MISCELLANEOUS PARTS		
	6960-0006	8	2	PLUG-HOLE DOME-HD FOR .25-D-HOLE STL	28480	6960-0006
	0380-0644	4	2	STANDOFF-HEX .327-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
				OPTION 001 HAS THE SAME PARTS AS THE STANDARD - LESS THE FOLLOWING		
	6960-0006	8		PLUG-HOLE DOME-HD FOR .25-D-HOLE STL	28480	6960-0006
	37203-60001	5		BOARD ASSEMBLY	28480	37203-60001
				PLUS THE FOLLOWING:		
	37203-60101	6	1	BOARD ASSEMBLY	28480	37203-60101
				OPTION 001 BUS EXTENDER		
				USE STANDARD REPLACEABLE PARTS LIST WITH THE FOLLOWING EXCEPTIONS		
A1	37203-60101	6	1	BOARD ASSEMBLY-OPTION 001	28480	37203-60101
A1OP1	1005-0021	9	1	FIBRE OPTIC TRANSMITTER	28480	1005-0021
A1OP2	1005-0005	8	1	FIBRE OPTIC RECEIVER	28480	1005-0005

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3 Code List of Manufacturers

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01295	TEXAS INSTR INC SEMICOND COMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25088	SIEMENS CORP	ISELIN	NJ	08830
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
52763	STETTNER-TRUSH INC	CAZENOVIA	NY	13035
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
75915	LITTELFUSE INC	DES PLAINES	IL	60016

SECTION VII

MANUAL CHANGES

7-1 INTRODUCTION

7-2 This section normally contains information for adapting this manual to instruments for which the manual content does not apply directly. Since this manual does apply directly to instruments having Serial Numbers listed on the title page, no change information is given here. Refer to INSTRUMENT AND MANUAL IDENTIFICATION in Section I for additional important information about Serial Numbers coverage.

SECTION VIII

SERVICE

8-1 INTRODUCTION

8-2 This section of the manual contains the information required to repair the 37203A HP-IB Extender. All the circuitry is contained on one printed circuit board, but for ease of documentation the instrument is divided into four sections. The sections are: Serial Section A1 Part 1, HP-IB Section A1 Part 2, Control Logic A1 Part 3, Power Supply A1 Part 4. Detailed information, i.e. circuit descriptions, schematic diagrams, component locations and troubleshooting information pertaining to each section is contained respectively in Service Sheets A1 Part 1,2,3,4.

8-3 By way of an introduction to the hardware, an overall general theory of operation is presented in Paragraph A1-1.

8-4 TROUBLESHOOTING

8-5 The troubleshooting of the 37203A assumes that the system controller and HP-IB cabling to the local 37203A are operating. Also, that no errors are introduced by the HP-IB devices or cabling connected to the remote 37203A. The System Troubleshooting in General Service Sheet G1, isolates the fault to a 37203A in the system. The Instrument Troubleshooting in General Service Sheet G2 isolates the fault to an area within the 37203A and will lead to the relevant Service Sheet containing troubleshooting, component location and schematic diagram. Fibre Optic Troubleshooting in General Service Sheet G3 isolates a faulty Fibre Optic Transmitter, Fibre Optic Receiver or Fibre Optic Cable in an Option 001 37203A.

8-6 SAFETY REQUIREMENTS

8-7 This section contains information and warnings which must be followed for your protection and to avoid damage to the equipment.

WARNING

Procedures described in this section are performed with protective covers removed and power supplied to the instrument. Servicing should only be performed by trained personnel who are aware of the hazards involved.

8-8 RECOMMENDED TEST EQUIPMENT

8-9 Test equipment required to maintain the 37203A is listed in Table 1-3. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended models.

8-10 LOGIC SYMBOLS

8-11 The logic symbols used in this manual are based on the American National Standard ANSI Y32.14-1973, 'Graphic Symbols for Logic Diagrams (Two-State Devices)'.

8-12 Qualifiers

8-13 Qualifiers are that portion of a logic symbol that denotes its logic function. The following qualifiers are used in this manual:

T	–	Toggle input
&	–	AND
mCNTR	–	COUNTER with modulus m
+m	–	COUNT UP INPUT (m is replaced with a number indicating number of shifts or counts)
◄►	–	Bilateral Switch: A binary controlled circuit which acts as an on/off switch to analog or binary signals flowing in both directions.
⎍ t =	–	Monostable Element: Single shot multivibrator output becomes active when input becomes active. Output remains active for the period of time (t) that is characteristic of the device or external components.

8-14 Indicator Symbols

8-15 Indicator symbols identify the active state or level of a symbol's input or output, see Figure 8-1.

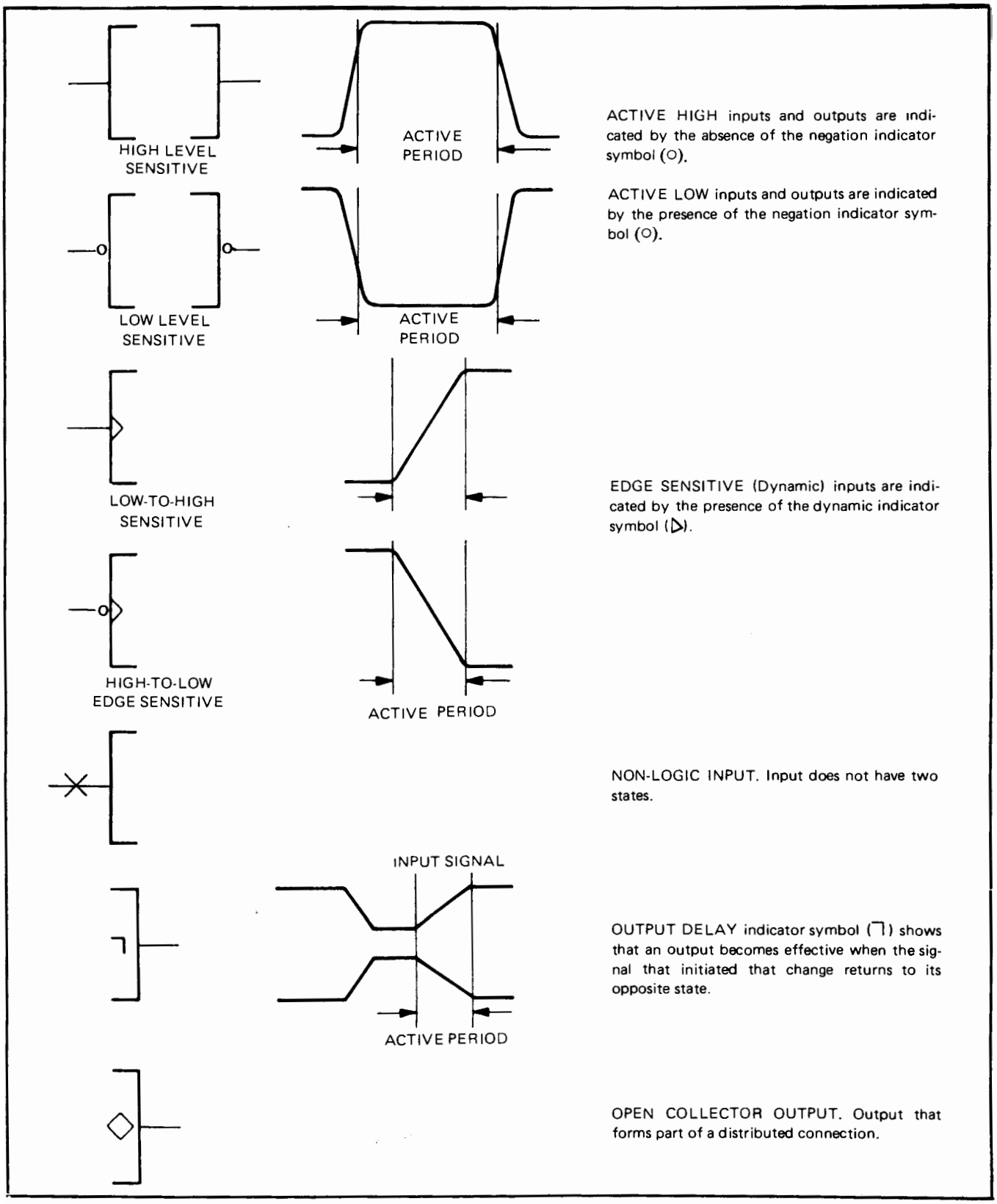


Figure 8-1 Indicator Symbols

8-16 Dependancy Notation

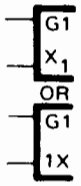
8-17 Dependancy notation is the technique for defining input/output and input/input relationships without showing all the elements and interconnections involved. Logic relationships between inputs and outputs are shown in this manual by using the following notation:

Gm – Gate (AND) Dependancy: The G input gates those inputs or outputs labelled with the same identifier m. The m is replaced with a number.

Cm – Control Dependancy: This is used only with D-type Flip-Flops and indicates that the basic function of the Flip-Flop is controlled by inputs with the same identifier. The m is replaced with a number.

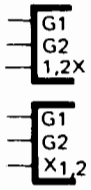
Vm – OR Dependancy: The V input has an OR relationship with those inputs or outputs labelled with the same identifier. When the V input is active, it makes the affected output active regardless of other inputs or functions being active. The m is replaced with a number.

– The input that controls or gates other inputs is labelled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labelled with the same number. In this example, "1" is controlled by "G1".



– When the controlled or gated input or output already has a functional label (X is used here), that level will be prefixed or subscripted by the identifying number.

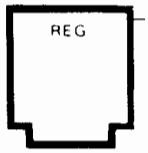
– If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.



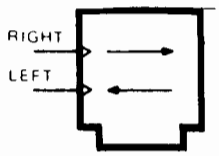
– If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript separated by commas. In this example "X" is controlled by "G1" and "G2".

8-18 Control Blocks

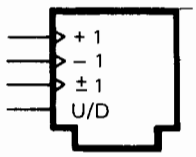
8-19 Control Blocks are used with complex logic to show when common control signals are applied to a group of functionally seperate units. Typical examples of control blocks follow.



Register control block: This symbol used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



Shift Register control block: These symbols are used with an array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.



Counter control block: The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or –1 inputs causes the counter to increment one count upward or downward, respectively. An active transition at the ±1 input causes the counter to increment one count upward or downward depending on the input at an up/down control.

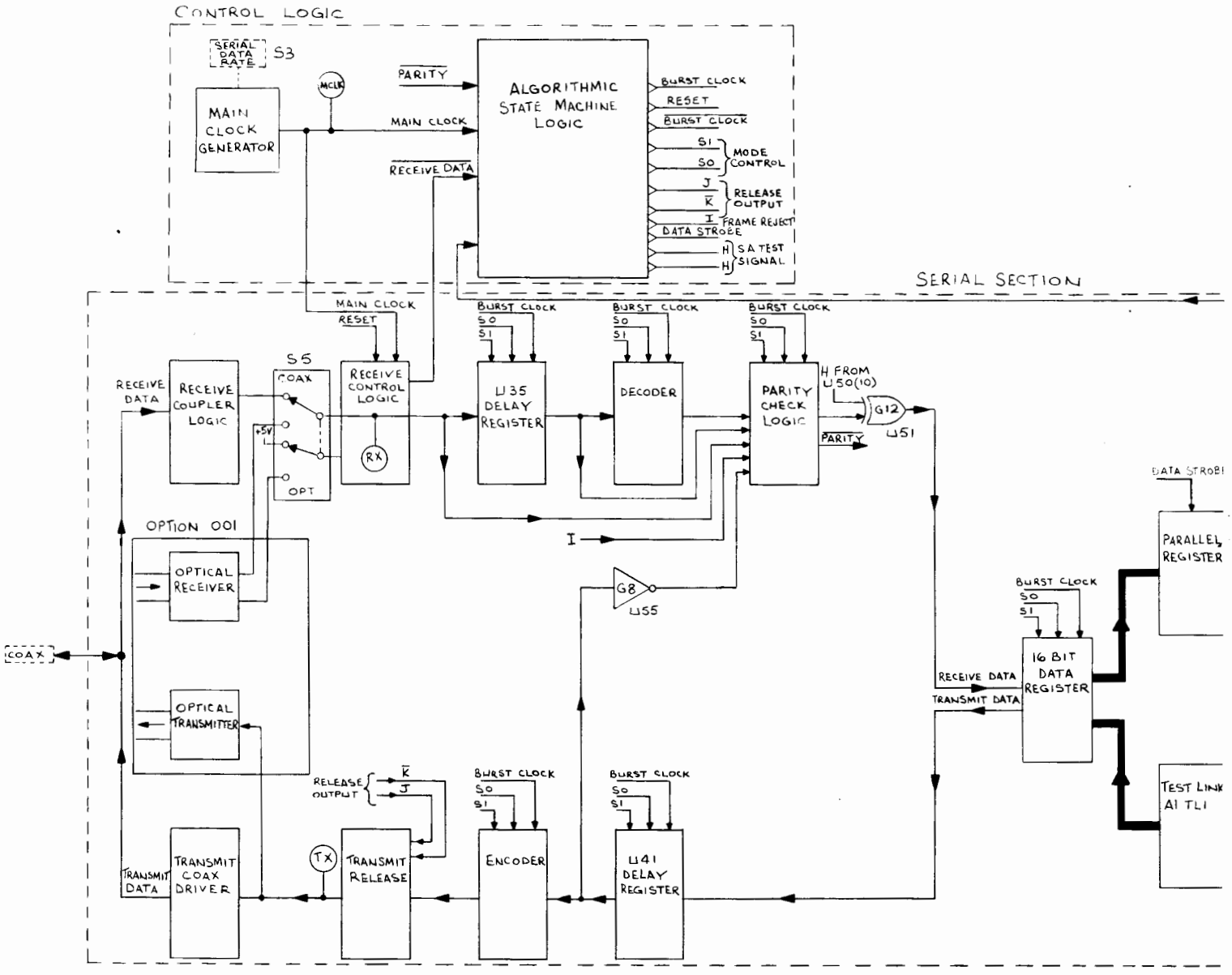
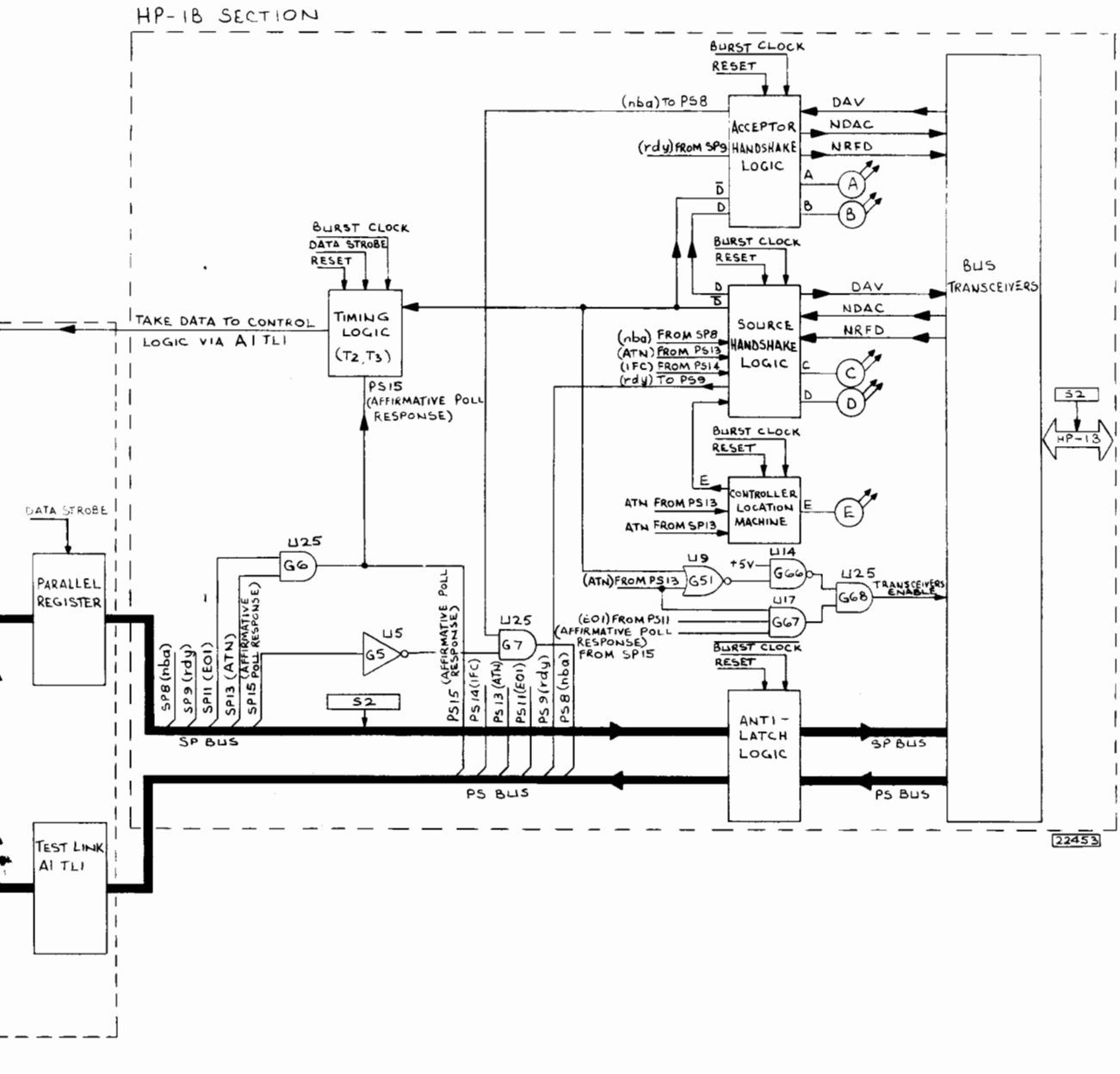


Figure 8-2 Overall Block Diagram


HP-IB SECTION
BURST CLOCK
RESET
(nba) TO PS8
ACCEPTOR HANDSHAKE LOGIC
DAV
NDAC
NRFD
(rdy) FROM SP9
A
B
D
BURST CLOCK
DATA STROBE
RESET
BURST CLOCK
RESET
BUS TRANSCEIVERS
TAKE DATA TO CONTROL LOGIC VIA A1 TLI
TIMING LOGIC (T2, T3)
SOURCE HANDSHAKE LOGIC
(nba) FROM SP8
(ATN) FROM PS13
(IFC) FROM PS14
(rdy) TO PS9
C
D
PS15 (AFFIRMATIVE POLL RESPONSE)
S2
HP-IB
BURST CLOCK
RESET
E
CONTROLLER LOCATION MACHINE
ATN FROM PS13
ATN FROM SP13
DATA STROBE
U25
G6
U9
G51
+5V
U14
G66
U25
G68
TRANSCEIVERS ENABLE
(ATN) FROM PS13
U17
G67
(EOI) FROM PS11
(AFFIRMATIVE POLL RESPONSE) FROM SP15
U5
G5
U25
G7
BURST CLOCK
RESET
PARALLEL REGISTER
SP8 (nba)
SP9 (rdy)
SP11 (EOI)
SP13 (ATN)
SP15 (AFFIRMATIVE POLL RESPONSE)
S2
PS15 (AFFIRMATIVE POLL RESPONSE)
PS14 (IFC)
PS13 (ATN)
PS11 (EOI)
PS9 (rdy)
PS8 (nba)
ANTI-LATCH LOGIC
SP BUS
SP BUS
PS BUS
PS BUS
TEST LINK A1 TLI
22453

8-20 OVERALL THEORY OF OPERATION

8-21 INTRODUCTION

8-22 The maximum distance apart that devices operating via HP-IB can be is normally 20 metres and usually less. The 37203A enables this distance to be extended, up to 1000 metres via coaxial cable. Two 37203A's are required, one at each end of the cable. Option 001 provides the added capability of using fibre optic cable as an alternative to coaxial cable. Figure 8-3 is a simplified block diagram showing the basic functions of the two 37203A's connected to the serial link.

Note. The 37203A contains both a transmitter and receiver for the 22 bit data frame (see Figure 8-4) which continuously shuttles back and forth between the 37203A's. This data frame contains the HP-IB information reporting the current state of the devices and the HP-IB Extender at each end.

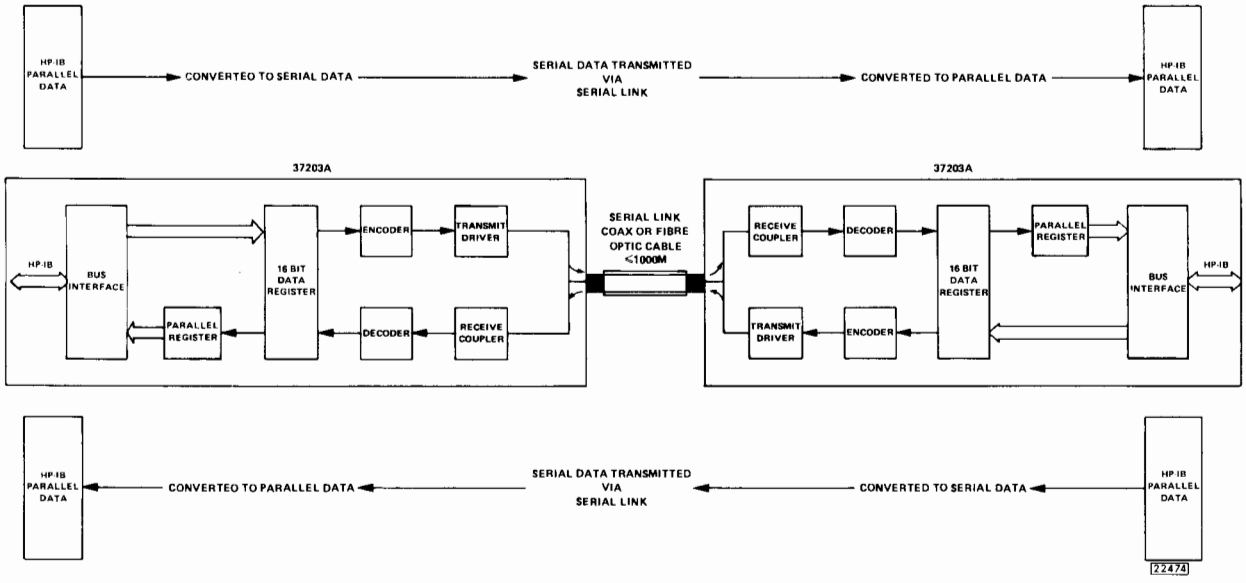
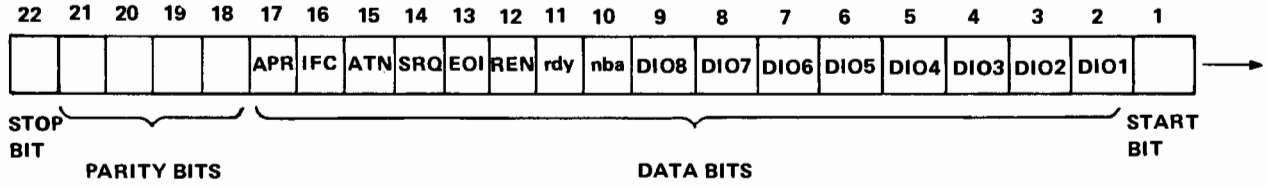


Figure 8-3 Simplified Block Diagram



APR	–	Affirmative Poll Response
IFC	–	Interface Clear
ATN	–	Attention
SRQ	–	Service Request
EOI	–	End or Identify
REN	–	Remote Enable
rdy	–	ready
nba	–	new byte available

Figure 8-4 Data Frame (before encoding)

8-23 DESCRIPTION (Figure 8-2)

8-24 The receive data frame arrives at the Receive Coupler Logic which passes the data frame via A1S5 to the Receive Control Logic. The Receive Control Logic continually looks for a start bit to synchronise the Algorithmic State Machine (ASM) Logic with the incoming data frame. The Receive Control Logic samples the incoming data frame at the Main Clock frequency which can be 24MHz, 6MHz or 1.5MHz depending on the setting of the Serial Data Rate switch. This synchronisation of the incoming data frame with the ASM Logic ensures that the data frame is sampled at the correct times. The following is a brief description of the control lines from the Control Logic:

Burst Clock

The ***Burst Clock*** provides the timing. All timing is referenced to the leading edge of the clock input. The frequency of the ***Burst Clock*** can be 8MHz, 2MHz or 0.5MHz depending on the setting of the Serial Data Rate switch.

Reset

This line is low active and is used as a power-on reset in the 37203A.

Mode Control (S_0, S_1)

These lines are used to control the mode of operation of the shift registers (U35 to U43). In the 37203A the mode can be parallel load, shift right or do nothing.

Release Output (J, $\overline{K}$)

These lines are high active and allow a data frame to be transmitted at the correct time, otherwise holding Transmit Data in the true state.

Frame Reject (I)

This line is used to reject the first receive frame after power-on.

Data Strobe

This line clocks the data from the Parallel Registers into the HP-IB section via the Serial to Parallel Data Bus (SP Bus).

Signature Analysis Test Signal (H, $\overline{H}$)

These lines are used as inputs to the 16 bit Data Register when the Signature Analysis Test is being performed.

8-25 After the start bit from the receive frame has been detected the data is clocked through the Delay Register to the Decoder. The receive data frame is then decoded and clocked through the Parity Check Logic into the 16-bit Data Register. After decoding, the four parity bits, the stop bits, the start bit and the frame reject signal are checked, and if they are all correct, the 16 data bits are loaded into the Parallel Register. The transfer of the 16 data bits from the 16-bit Data Register to the Parallel Register is the serial to parallel conversion. Should the Parity Check fail the 16 data bits will not be transferred and the Master 37203A will re-transmit the status of its HP-IB, see Paragraph 8-70. This parallel data is passed, via the Serial to Parallel Data Bus (SP Bus – see Figure 8-5), to the Anti-Latch Logic. The Anti-Latch Logic prevents the HP-IB lines from locking up and staying permanently in one state, due to a closed logic loop which would otherwise be set up.

8-26 The status of the Management Lines and the Data Input/Output Lines is transferred to the Bus Transceivers via the Anti-Latch Logic. The status of the Local Messages, *ready* (SP9, *rdy*) and *new byte available* (SP8, *nba*), is sent between 37203A's to control the Source and Acceptor Handshake Logic. The interlocked handshake sequence (explained in Paragraph 8-42) between the Source Handshake Logic in one 37203A and the Acceptor Handshake Logic in the other 37203A guarantees asynchronous transfer of the HP-IB data. Once the receive data frame has been accepted and after the handshake sequence has completed, or a 5μs timeout from the Timing Logic has elapsed, the 37203A assembles a return frame. The status of the 16 HP-IB lines is then passed to the 16-bit Data Register via the Parallel to Serial Data Bus (PS Bus – see Figure 8-5). The Test Link (A1TL1), when connected in the RUN Mode, provides a straight through connection. This Test Link when connected in the TEST Mode is used for Signature Analysis troubleshooting.

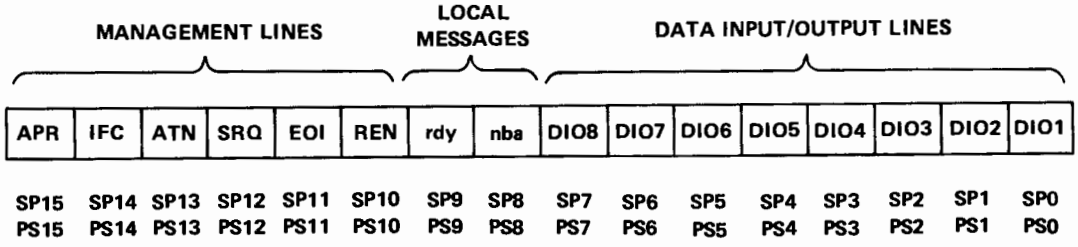


Figure 8-5 SP and PS Bus Structure

8-27 The return frame is clocked from the 16-bit Data Register through the Delay Register to the Encoder. The Encoder (a 4 bit cyclic redundancy check encoder) encodes the return frame from the HP-IB section and the 4 parity check bits into a transmit data frame as it is being transmitted. Transmission of the data frame is enabled when the *Release Output lines (J, $\overline{K}$)* are high. The transmit data frame is then transmitted over coaxial cable by the Transmit Coax Driver.

8-28 Option 001

8-29 Option 001 of the 37203A provides the capability of operation over dual fibre optic cable as a user selectable alternative to coaxial cable.

8-30 The operation of the 37203A, when configured for fibre optic operation, replaces the Receive Coupler Logic with an Optical Receiver and the Transmit Coax Driver with an Optical Transmitter.

8-31 The Optical Receiver receives the coded light signal and converts it to the corresponding TTL levels which are passed, via Switch A1S5, to the Receive Control Logic. The operation of the instrument is identical to the coaxial configured instrument up to the output of the Transmit Release Logic. The output of the Transmit Release Logic is connected to the Optical Transmitter which converts the transmit data frame into a coded light signal suitable for transmission over fibre optic cable.

8-32 Receive Coupler Logic and Transmit Coax Driver

8-33 The Receive Coupler Logic and the Transmit Coax Driver have a floating ground to provide protection from differing ground potentials at the two ends of the coaxial cable. The float range is limited by a varistor RV1 to approximately ±24V. The data frames are transferred to and from the floating circuit by two opto-couplers.

8-34 The Transmit Driver uses a transistor switching circuit, run from a floating ±5V supply, to drive the coaxial cable. This circuit has a built-in overshoot to provide some compensation for the losses in coaxial cable at the highest (NORMAL) Serial Data Rate.

8-35 During receive periods, the collectors of Q3 and Q4 (in the Transmit Driver) are held in a mark condition, since transmission is not then taking place. This provides a fixed threshold on the base of Q6, enabling the long-tailed switching pair Q5 and Q6 to detect the received signal and drive the optocoupler, U63.

8-36 Receive Control Logic

8-37 The Rx test point is actually $\overline{\textit{Receive Data}}$ (inverted by G4). Monitoring $\overline{\textit{Receive Data}}$ is necessary when adjusting the Receive Data Skew, see Section 5.

8-38 Delay Register U35, U41

8-39 The Delay Registers provide a 1 bit delay to compensate for the propogation delay of the exclusive OR gates in the Decoder and Encoder.

8-40 Timing Logic

8-41 The Timing Logic provides the necessary timeouts to ensure the transfer of valid data:

T_2 (0.7μs) allows the Anti-Latch Logic to settle before the Source Handshake sets DAV low.

T_3 (5μs) *Take Data* will go true and the transmit frame will be loaded into the 16-bit Data Register as soon as the handshake sequence is complete or after a wait of 5μs (timed from the transfer of new data to the SP Bus) whichever occurs first.

8-42 Source and Acceptor Handshake Logic

8-43 Both the source and acceptor handshake logic in a pair of 37203A's at power-on are in a known quiescent state. After power-on the source handshake sets DAV (Data Valid) high indicating that data on the bus is not valid and the acceptor handshake sets NRFD (Not Ready for Data) low and NDAC (No Data Accepted) low indicating that data has neither been accepted nor is the 37203A ready to accept data. Upon receipt of *rdy* from the source handshake NRFD will be set high to indicate the 37203A is ready to accept data from the bus. A source instrument may then source the data byte onto the DIO lines and set DAV low. When this occurs the acceptor handshake sends *nba* to the source handshake and sets NRFD and NDAC low. The source handshake places the data byte on the bus and when the receiving bus is ready to accept it, sets DAV low to indicate that the data is valid. When the bus has accepted the data byte the source handshake sets DAV high indicating that data on the DIO lines is no longer valid and sends *rdy* false. This allows the acceptor handshake to set NDAC high to inform the source instrument that the data has been accepted and the acceptor handshake sends *nba* false which returns the source handshake to its quiescent state. The source instrument then sets DAV high to indicate that data is no longer valid and this permits the acceptor handshake to return to its power-on state holding both NRFD and NDAC low. The cycle repeats as the HP-IB data transfer continues.

8-44 No step in this sequence can be initiated until the previous step is complete. Thus the HP-IB data transfer can proceed as fast as the HP-IB devices can respond, but not faster than the slowest device.

8-45 The timing monostable in the Source Handshake Logic produces a 2μs timeout (T_1). This allows the DIO lines to settle before the Source Handshake Logic sets DAV low.

8-46 Controller Location Machine

8-47 The Controller Location Machine determines which 37203A (in a pair) sent ATN last. This is used when passing control from one controller to another. PS13 is ATN sent from the 37203A to the controller. SP13 is ATN received from the controller.

8-48 Anti-Latch Logic

8-49 The Anti-Latch Logic (U5-U11, U16 and U22) interfaces between the SP Bus and the PS Bus. It allows the logical state of the HP-IB to be passed to the Serial Section and vice versa by breaking communications between the buses. The Anti-Latch Logic also prevents the SP Bus and the PS Bus from locking up and staying permanently in one state, due to a closed logic loop which would otherwise be set up.

8-50 Bus Transceivers

8-51 The Bus Transceivers (U1-U4) control the bidirectional flow of HP-IB information. The Management and Handshake lines are routed via U1 and U2. The DIO lines are routed via U3 and U4. The Bus Transceivers are 'low' enable to allow the data to flow out onto the HP-IB. The lines DAV, NRFD, NDAC, REN, SRQ, ATN and IFC are permanently enabled. G52 enables EOI when data is being sourced onto the HP-IB or in order to perform a Parallel Poll. The DIO lines are enabled when data is being sourced onto the HP-IB and when the local controller performs a Parallel Poll.

8-52 Bus Transceivers U3 and U4 are enabled during sourcing by $\overline{D}$ and PS13 (ATN) both being 'low' at the input to G51. U3 and U4 are enabled during a Parallel Poll by PS13 (ATN), PS11 (EOI) and SP15 (APR) all being 'high' at the input of G67.

8-53 Parallel Poll Sequence (Figure 8-6)

8-54 During a Parallel Poll the controller activates ATN and EOI which sets bits PS13 and PS11 true in the local 37203A. At the remote 37203A this sets bits SP13 and SP11 true. SP13 and SP11 are the inputs to G6 and the output is PS15 (Affirmative Poll Response, APR). PS15 is now ready to be sent to the local 37203A. The Parallel Poll is performed and the Parallel Poll Response (DIO1 to DIO8 are used to convey the device status bits) is ready to be sent to the local 37203A. PS15 sent to the Timing Monostables ensures that the data will not be clocked into the 16-bit Data Register by *Take Data* until a 5μs timeout has elapsed. This allows the Affirmative Poll Response and the Parallel Poll Response (PS15 and PS0-7) to be sent back to the local 37203A in the same data frame. The Affirmative Poll Response and the Parallel Poll Response, now SP15 and SP0-7 in the local 37203A, causes the Bus Transceivers to be enabled and the Parallel Poll Response to be passed to the controller respectively.

8-55 G5 and G7 ensures that the controller cannot source a byte until the Affirmative Poll Response is faulse.

8-56 The LED's (DS1 to DS5) are used during troubleshooting when, in conjunction with S2, the Source and Acceptor Handshake Logic can be forced to cycle. The LED's give a visual indication of each step of the handshake sequence, see Paragraph A1-10.

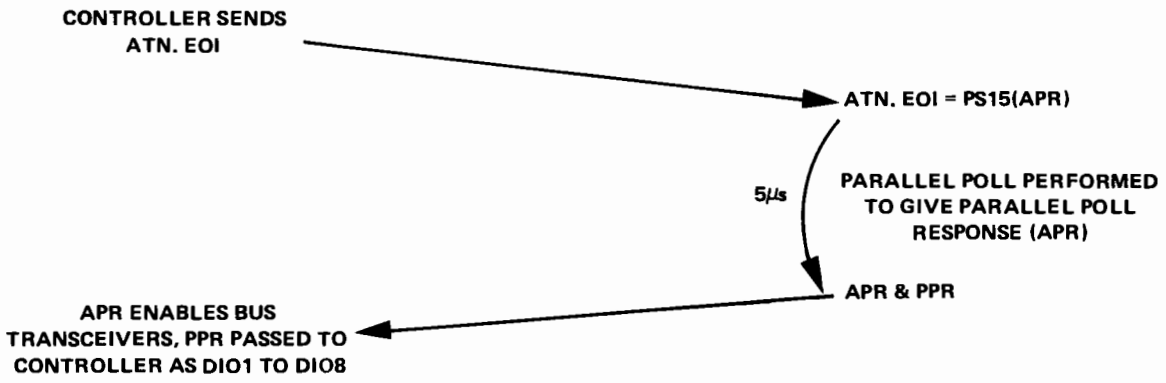


Figure 8-6 Parallel Poll Sequence

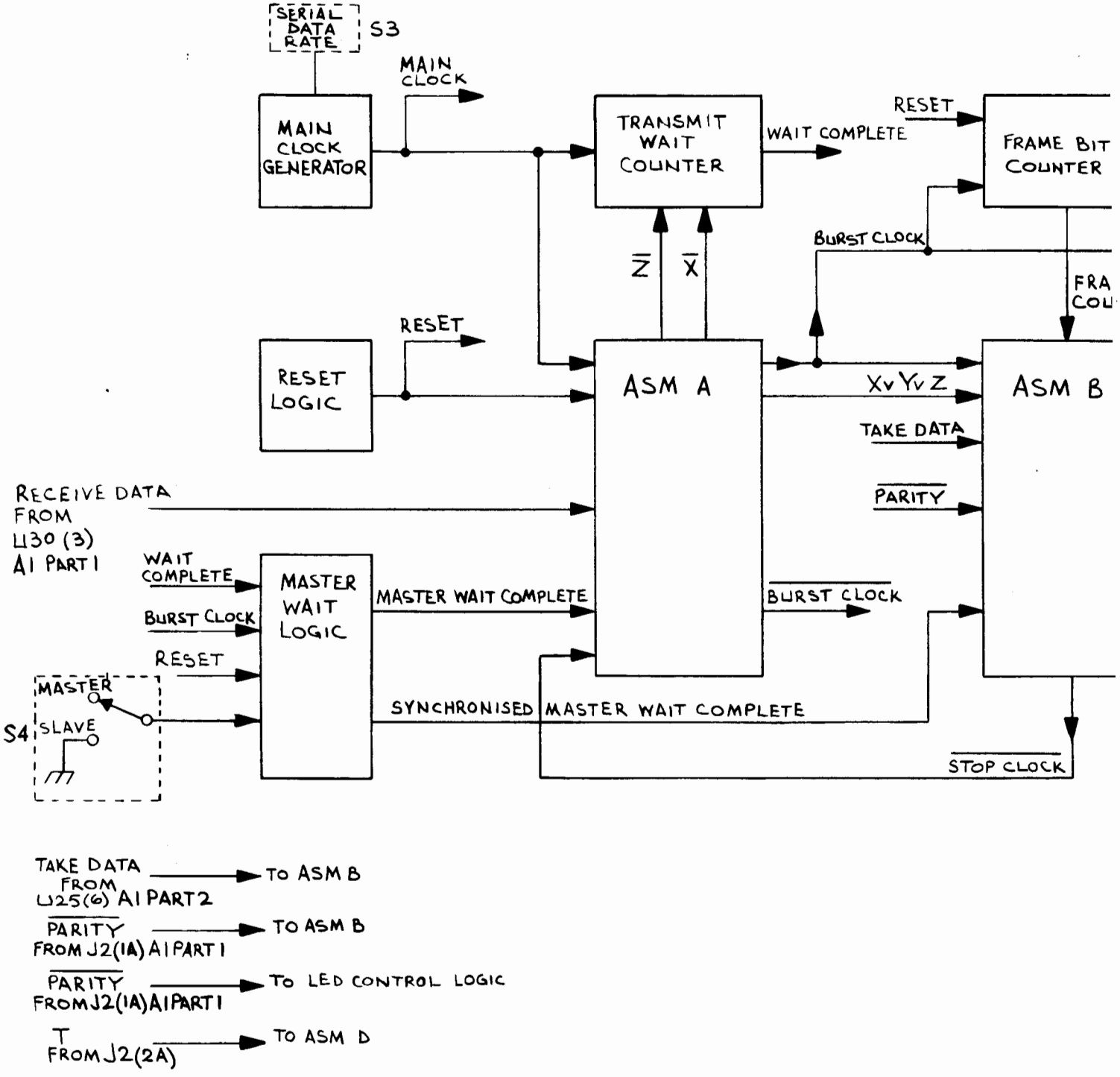
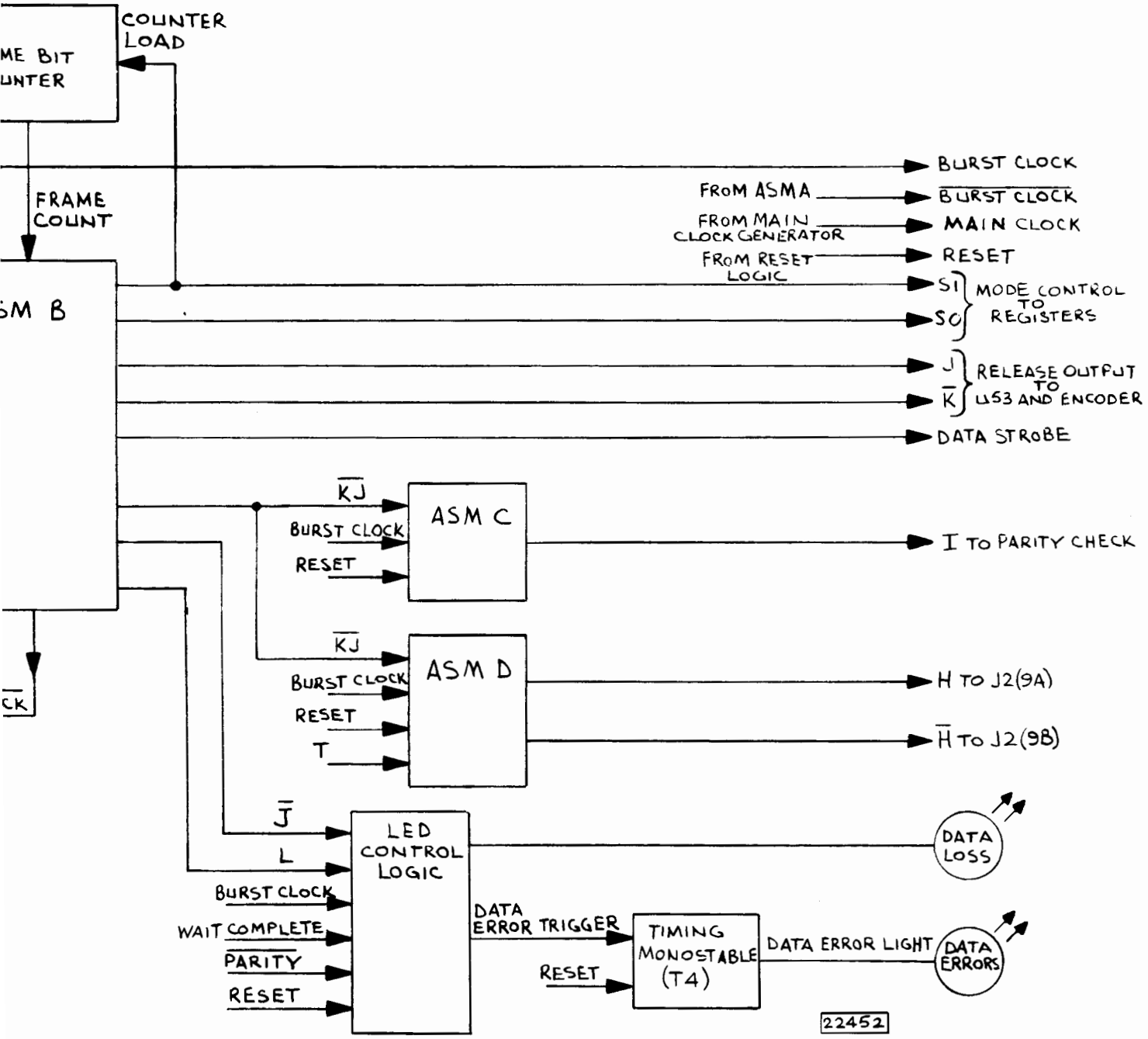


Figure 8-7 Control Logic Block Diagram


ME BIT
UNTER
COUNTER
LOAD
FRAME
COUNT
SM B
CK
BURST CLOCK
FROM ASMA
BURST CLOCK
FROM MAIN
CLOCK GENERATOR
MAIN CLOCK
FROM RESET
LOGIC
RESET
S1
S0
MODE CONTROL
TO
REGISTERS
J
K
RELEASE OUTPUT
TO
LI53 AND ENCODER
DATA STROBE
KJ
BURST CLOCK
RESET
ASM C
I TO PARITY CHECK
KJ
BURST CLOCK
RESET
T
ASM D
H TO J2(9A)
H TO J2(9B)
J
L
BURST CLOCK
WAIT COMPLETE
PARITY
RESET
LED
CONTROL
LOGIC
DATA
LOSS
DATA
ERROR TRIGGER
RESET
TIMING
MONOSTABLE
(T4)
DATA ERROR LIGHT
DATA
ERRORS
22452

8-57 CONTROL LOGIC THEORY OF OPERATION

8-58 DESCRIPTION (Figure 8-7)

8-59 The Main Clock Generator circuit produces a 24MHz clock which can be divided by 4 or 16 depending on the setting of the Serial Data Rate switch. Reducing the main clock frequency permits the 37203A to communicate over greater distances. Thus the main clock can be 24MHz, 6MHz or 1.5MHz.

8-60 The Reset Logic produces the *Reset* line. This line is low active and is used as a power-on reset in the 37203A.

8-61 A start bit from $\overline{Receive\ Data}$ is the 'trigger' for ASM 'A'. Once triggered ASM 'A' divides the main clock by 3 to produce the *Burst Clock* of 8MHz, 2MHz or 0.5MHz.

8-62 The *Burst Clock* from ASM 'A' is the clock for ASM 'B' (and other shift registers). By changing the mode of the registers, ASM 'B' controls the movement of the data through the registers in the Serial Section and to and from the HP-IB section. ASM 'B' produces the mode control lines S_0 and S_1, which change the mode of the registers to shift right, load or do nothing. After the receive frame is clocked into the 16-bit Data Register and the parity check code passes, *Data Strobe* is set high. The data is then transferred from the 16-bit Data Register to the Parallel Register. Once the receive data has been accepted by the HP-IB section, and after completion of the handshake sequence or the 5μs timeout (T_3) *Take Data* is set high. This changes ASM 'B' from the receive phase to the transmit phase i.e. ready to transmit a return frame to the opposite end.

8-63 The Frame Bit Counter counts the data bits going into the registers in the Serial Section during the transmit and receive phases. After the transmit data frame has been transmitted ASM 'B' sets $\overline{Stop\ Clock}$ low to reset ASM 'A' which stops the *Burst Clock* and resets ASM 'B'. While ASM 'A' is in its idle state the Transmit Wait Counter is released and counts the *Main Clock* until the start bit from the next receive data frame starts ASM 'A' which resets the Transmit Wait Counter. If there is no receive data frame the Transmit Wait Counter continues to count the *Main Clock*, setting *Wait Complete* high approximately every 30μs. On the master 37203A when *Wait Complete* goes high the Master Wait Logic sets the *Master Wait Complete* high to start ASM 'A' producing the *Burst Clock*. The Master Wait Logic also sets *Synchronised Master Wait Complete* high to put ASM 'B' into the transmit phase to restart communication.

8-64 At power-on, to prevent any erroneous data being transferred to the HP-IB, ASM 'C' causes the first receive data frame to be rejected and also ensures the correct initial conditions for ASM 'B'.

8-65 If the parity check code is incorrect $\overline{Parity}$ is held high and the LED Control Logic sets *Data Error Trigger* high to trigger the Timing Monostable (T_4). This illuminates the Data Errors LED for 100ms. The Data Loss LED is illuminated, if there is a break in the serial link between 37203A's, by the Transmit Wait Counter setting *Wait Complete* high approximately every 30μs.

8-66 Algorithmic State Machine 'A'

8-67 The Algorithmic State Machine A is a 5 state ASM (see Figure 8-8 for the state diagram). At power-on the machine will be in state 1 waiting for the start bit on $\overline{Receive\ Data}$ to set U31(5) high. The machine then passes through state 2 (a transitional state for timing purposes only) to states 3, 4 and 5. (The machine continually loops states 3, 4 and 5 to divide the *Main Clock* by 3 to produce the *Burst Clock* in phase with the receive frame). State 3 gives the true state of the *Burst Clock* at U30(7). The *Burst Clock* will run until ASM 'B' reaches state 11 putting $\overline{Stop\ Clock}$ low. ASM 'A' will then idle in state 1 waiting for the start bit from the next receive frame.

8-68 Algorithmic State Machine B (ASM 'B')

8-69 The Algorithmic State Machine B is a 7 state ASM (see Figure 8-8 for the state diagram). At power-on the machine will be in state 6 waiting for the *Burst Clock* from ASM 'A' to start the machine. During state 6 the receive data frame is shifted serially into the registers until the *Frame Count* signal indicates that the last bit is ready to be loaded. The machine then goes into state 7. If the parity check code is correct $\overline{Parity}$ will be false so, the machine moves into state 8 when the data is transferred from the 16-bit Data Register to the Parallel Register. *Data Strobe* is now set high and the registers are put in the load mode with the data being passed to the HP-IB section. After the receive frame has been sourced onto the HP-IB the return frame has to be sent. The HP-IB section sets *Take Data* high to move the machine into state 9. During this state the return data frame is shifted serially into the registers until the *Frame Count* signal indicates that the last bit has been transferred to the Serial Section. The machine will now move into state 9a. During states 9 and 9a *Release Output* is set high to allow the return frame to be transmitted over the serial link. State 9a allows the last bit of the return frame to be encoded and transmitted over the serial link. The machine then moves into state 10 where the registers are loaded with the correct initial conditions for the next receive data frame. Once the registers are loaded the machine moves into state 11 where the $\overline{Stop\ Clock}$ is set low to stop the *Burst Clock* from ASM 'A'. ASM 'B' then idles in state 6 waiting for the *Burst Clock* from ASM 'A'.

8-70 If the parity check code is incorrect $\overline{Parity}$ will be high so the machine will not go into state 8 but instead will go into state 10 then state 11, and in this case no return frame will be transmitted. The unit that is configured as the master will, after approximately 30μs, produce a start signal, *Master Wait Complete*, to trigger ASM 'A'. This in turn clocks ASM 'B' and as the *Synchronised Master Wait Complete* signal is high the machine will move from state 6 to state 9 which will then transmit a frame representing the present state of the HP-IB.

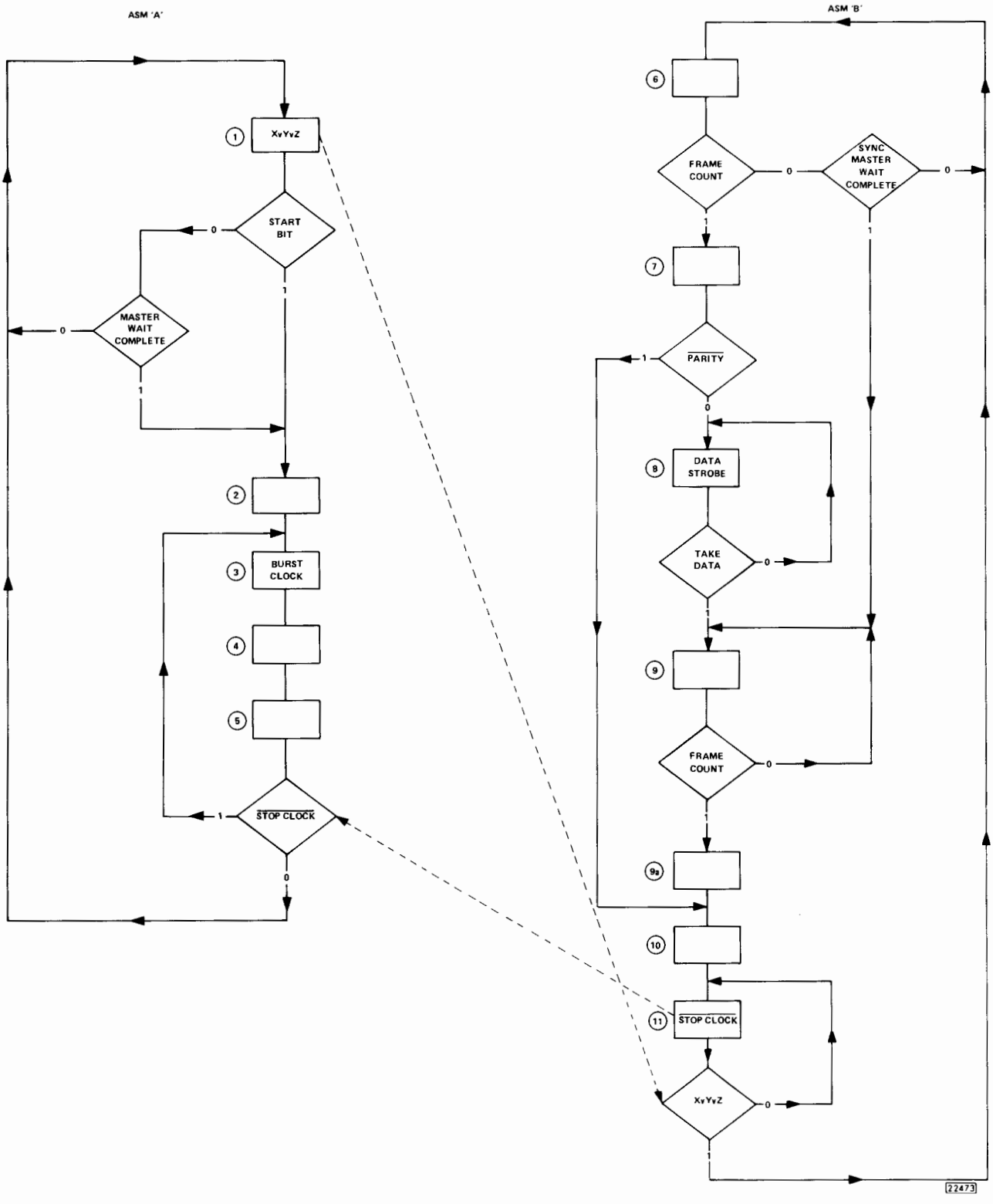


Figure 8-8 State Diagram of ASM 'A' and ASM 'B'

8-71 Algorithmic State Machine C (ASM 'C')

8-72 The Algorithmic State Machine C causes the first receive data frame to be rejected by holding *I* low which prevents $\overline{Parity}$ going true. If there were no ASM 'C' and a slave 37203A was switched on in the middle of a receive frame and the parity check code was correct, the erroneous data frame would be passed to the HP-IB section. ASM 'C' prevents this occurring, and also ensures the correct initial conditions for ASM 'B'.

8-73 Algorithmic State Machine D (ASM 'D')

8-74 ASM 'D' is used only during signature analysis testing. When *T* is forced true it produces a variable *(H)* which inverts every time ASM 'B' is activated. During signature analysis testing ASM 'A' and ASM 'B' can be forced to cycle by:

(a) forcing *Master Wait Complete* high to trigger ASM 'A'.

(b) forcing *Take Data* high so that the duration of state 8 in ASM 'B' is no longer determined by the Timing Logic (T_3).

(c) forcing the parallel input lines of the 16 bit Data Register into two complementary states used alternately with each cycle of ASM 'B', ie *H* and $\overline{H}$.

(d) forcing $\overline{Parity}$ low so that ASM 'B' goes through a complete cycle.

8-75 Frame Bit Counter

8-76 The frame bit counter is loaded with 43_{10} while *Counter Load* is high. Once the *Burst Clock* from ASM 'A' has started ASM 'B' *Counter Load* is set low so starting the counter. The counter counts 21 bits of the receive frame then sets the *Frame Count* signal high. At this time the 16 data bits will be loaded into the 16-bit Data Register ready for passing to the Parallel Register should the parity check code pass. It also counts off the 21 data bits of the transmit frame during transmission.

GENERAL SERVICE SHEET G1

SYSTEM TROUBLESHOOTING

G1-1 INTRODUCTION

G1-2 The following procedures cover fault diagnosis of the different types of system configuration and are intended only as a guide to help in indicating a faulty area (local 37203A, remote 37203A or serial link). The procedures assume that the System Controller and HP-IB cabling to the local 37203A are operating.

G1-3 The serial link can either be coaxial cable or fibre optic cable. Hence, for each system configuration there are two troubleshooting procedures, see Table G1-1. Before proceeding to the paragraph indicated in Table G1-1 the initial checks should be completed.

Table G1-1 Troubleshooting Procedure Index

System	Coaxial Cable	Fibre Optic Cable
Point-to-Point	Paragraph G1-8	Paragraph G1-11
Star	Paragraph G1-9	Paragraph G1-12
Tandem	Paragraph G1-10	Paragraph G1-13

G1-4 INITIAL CHECKS

G1-5 Before proceeding with the troubleshooting check the following points:

(a) That all 37203A's have line 'ON'.

(b) That all 37203A's are configured correctly, see Section 2 Paragraphs 2-29 to 2-44.

(c) That the 37203A specification is not being exceeded in distance or Serial Data Rate, taking into account the loss of the coaxial cable being used.

G1-6 EQUIPMENT REQUIRED

G1-7 Equipment required to perform the troubleshooting is given in Table G1-2.

Table G1-2 Equipment Required

Quantity	Item	Type
1	Oscilloscope	HP180C, 1809A, 1825A
1	10:1 Probe	HP10004D

G1-8 POINT-TO-POINT CONFIGURED SYSTEM (COAXIAL CABLE)

1. Is the DATA LOSS indicator ON?

If the DATA LOSS indicator is OFF proceed to step 2.
If the DATA LOSS indicator is ON check the serial link:
If the SERIAL DATA RATE switch, on the rear panel is set to NORMAL reduce it to 1/16 on both 37203A's, otherwise check the continuity of the cable.

(a) Indicator goes OFF check the skew adjustments in both 37203A's, see Section 5.

(b) Indicator stays ON check the continuity of the cable.

If the continuity check passes proceed to step 3.
If the continuity check fails replace the coaxial cable.

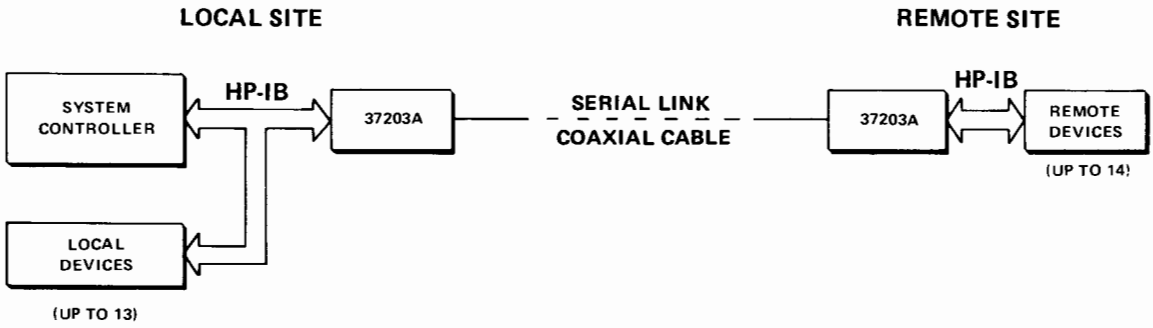


Figure G1-1 Point-to-Point Configured System

2. Is the DATA ERRORS indicator ON?

   If the DATA ERRORS indicator is ON proceed to step 3.
   If the DATA ERRORS indicator is OFF jump to step 16.

3. Disconnect the coaxial cable and HP-IB from the local 37203A and set the MASTER/SLAVE switch, on the rear panel, to MASTER.

4. Remove the top cover from the local 37203A.

5. Connect the oscilloscope to Test Point OUT using Test Point FGND to ground the oscilloscope probe.

6. Set the oscilloscope to 0.05μs 1 div, 0.2V/div and negative trigger.

7. Switch the local 37203A OFF for 5 seconds then ON.

8. Compare the waveform on the oscilloscope to Figure G1-2.

   If the waveform is identical proceed to step 9.
   If the waveform is different check the Serial Section and Control Logic, see Service Sheet A1 Parts 1 and 3.

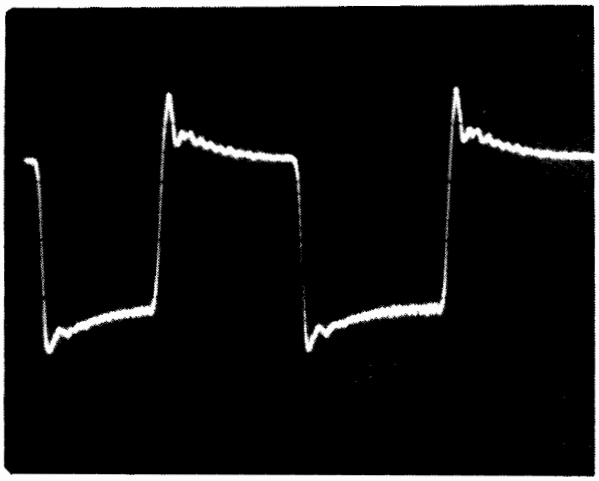


Figure G1-2 Start of Waveform of Transmit Frame

9. Connect the oscilloscope to Test Point RX.

10. Set the oscilloscope to 0.05μs/div, 0.2V/div and positive trigger.

11. Switch the local 37203A OFF for 5 seconds then ON.

12. Compare the waveform on the oscilloscope to Figure G1-3.

    If the waveform is identical proceed to step 13.
    If the waveform is different check the Serial Section and Control Logic, see Service Sheet A1 Parts 1 and 3.

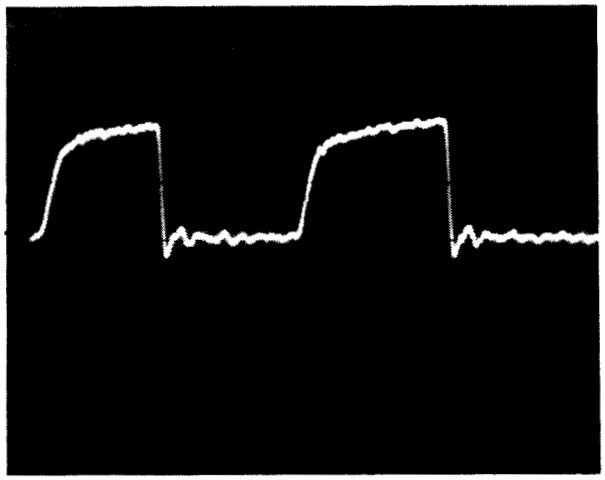


Figure G1-3 Start of Waveform of Receive Frame

13. Disconnect the coaxial cable and the HP-IB from the remote 37203A and set the MASTER/SLAVE switch on the rear panel to MASTER.

14. Repeat steps 4 to 11 on the remote 37203A.

15. Compare the waveform on the oscilloscope to Figure G1-3.

    If the waveform is identical proceed to step 16.
    If the waveform is different check the Serial Section and Control Logic, see Service Sheet A1 Parts 1 and 3.

16. Check the HP-IB Section in the remote 37203A, see Service Sheet A1 Part 2.

    If the remote HP-IB Section is correct proceed to step 17.

17. Check the HP-IB Section in the local 37203A, see Service Sheet A1 Part 2.

18. After the fault has been eliminated run the Performance Verification routines, see Section 4.

G1-9 STAR CONFIGURED SYSTEM (COAXIAL CABLE)

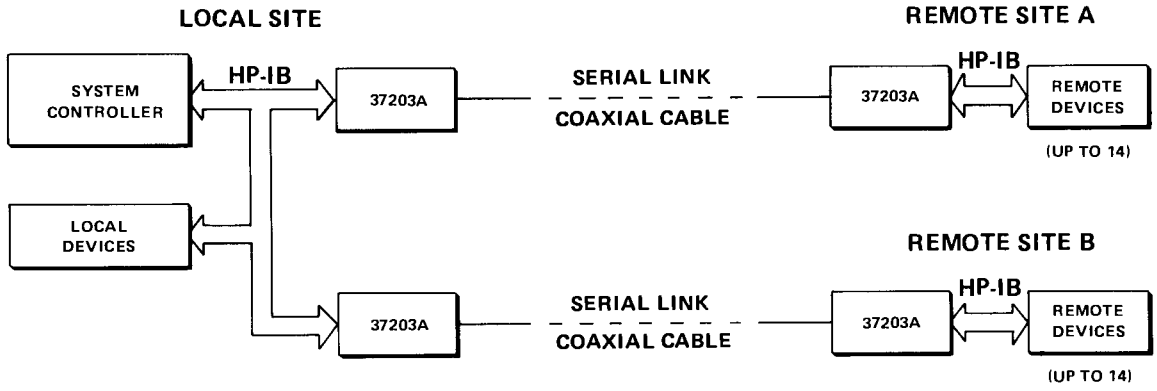


Figure G1-4 Star Configured System

1. Check each link individually to isolate the faulty link.

   (a) Disconnect all the local 37203A's from the HP-IB.

   (b) Connect one local 37203A to the HP-IB.

   (c) Check that the system is operational using the System Controller.

   (d) Repeat (b) and (c) for each local 37203A until the faulty link has been detected then proceed to step 2.

2. Is the DATA LOSS indicator ON?

   If the DATA LOSS indicator is OFF proceed to step 4.
   If the DATA LOSS indicator is ON check the serial link.
   If the SERIAL DATA RATE switch on the rear panel is set to NORMAL reduce it to 1/16 on both 37203A's, otherwise check the continuity of the cable.

   (a) Indicator goes OFF check the skew adjustments on both 37203A's, see Section 5.

   (b) Indicator stays ON check the continuity of the cable.

   If the continuity check passes proceed to step 3.
   If the continuity check fails replace the coaxial cable.

3. Check the local 37203A:

   (a) Set the MASTER/SLAVE switch on the rear panel to MASTER on the local 37203A.

   (b) Disconnect the coaxial cable and HP-IB from the local 37203A.

   (c) Remove the top cover from the local 37203A.

   (d) Compare the waveform at Test Points OUT and RX on the oscilloscope, using Test Point FGND to ground the oscilloscope probe on Test Point OUT. The waveform at RX should be the logical inverse of the waveform at OUT.

   If the RX waveform is the logical inverse of the OUT waveform the fault is in the 'remote' 37203A, see General Service Sheet G2.
   If the RX waveform is not the logical inverse of the OUT waveform the fault is in the 'local' 37203A, see General Service Sheet G2.

4. Is the DATA ERRORS indicator ON?

   If the DATA ERRORS indicator is OFF proceed to step 5.
   If the DATA ERRORS indicator is ON replace the local 37203A with one of the other local 37203A's.
   If the indicator goes OFF the fault is in the local 37203A.
   If the indicator stays ON the fault is in the remote 37203A.
   Identify the faulty area of the defective 37203A using the Instrument Troubleshooting in General Service Sheet G2.

5. If there are no indicators ON replace the local 37203A with one of the other local 37203A's. Check the operation of the remote site with the system controller.

   If the fault disappears the local 37203A is defective.
   If the fault remains the remote 37203A is defective.
   Identify the faulty area on the defective 37203A using the Instrument Troubleshooting in General Service Sheet G2.

6. After the fault has been eliminated run the Performance Verification routines, see Section 4.

G1-10 TANDEM CONFIGURED SYSTEM (COAXIAL CABLE)

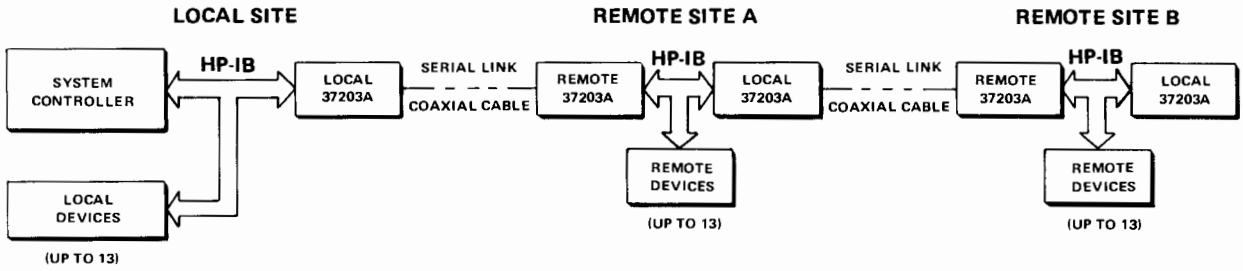


Figure G1-5 Tandem Configured System

1. Check each link individually to isolate the faulty link.

   (a) Disconnect the 'local' 37203A at remote site A from the HP-IB.

   (b) Check that the system is operational using the System Controller.

   (c) Repeat (a) and (b) at each remote site until the faulty link has been detected then proceed to step 2.

2. Is the DATA LOSS indicator 'ON'?

   If the DATA LOSS indicator is OFF proceed to step 4.
   If the DATA LOSS indicator is ON check the serial link:
   If the SERIAL DATA RATE switch on the rear panel is set to NORMAL reduce it to 1/16 on both 37203A's, otherwise check the continuity of the cable:

   (a) Indicator goes OFF check the skew adjustments of both 37203A's, see Section 5.

   (b) Indicator stays ON check the continuity of the cable.

   If the continuity check passes proceed to step 3.
   If the continuity check fails replace the coaxial cable.

3. Check the 'local' 37203A:

   (a) Set the MASTER/SLAVE switch on the rear panel to MASTER on the 'local' 37203A.

   (b) Disconnect the coaxial cable and HP-IB from the 'local' 37203A.

   (c) Remove the top cover from the 'local' 37203A.

   (d) Compare the waveform at Test Points OUT and RX on the oscilloscope, using Test Point FGND to ground the oscilloscope probe on Test Point OUT. The waveform at RX should be the logical inverse of the waveform at OUT.

   If the RX waveform is the logical inverse of the OUT waveform the fault is in the 'remote' 37203A, see General Service Sheet G2.
   If the RX waveform is not the logical inverse of the OUT waveform the fault is in the 'local' 37203A, see General Service Sheet G2.

4. Is the DATA ERRORS indicator ON?

   If the DATA ERRORS indicator is OFF proceed to step 5.
   If the DATA ERRORS indicator is ON (for the final link proceed to (b) otherwise (a)).

   (a) Swap 37203A at the 'remote' site.
   If the indicator goes OFF the fault is in the 'remote' 37203A.
   If the indicator stays ON the fault is in the 'local' 37203A.
   Identify the faulty area of the defective 37203A using the Instrument Troubleshooting in General Service Sheet G2.

   (b) Swap 37203A's at the 'local' site and observe the indicators on the previous link.
   If the indicator comes ON the fault is in the 'local' 37203A.
   If the indicator remains OFF the fault is in the 'remote' 37203A.
   Identify the faulty area of the defective 37203A using the Instrument Troubleshooting in General Service Sheet G2.

5. If there are no indicators ON and the fault is in the final link proceed to (b) otherwise (a).

   (a) Swap 37203A's at the 'remote' site. Check the operation of the link with the system controller.
   If the fault disappears the 'remote' 37203A is defective.
   If the fault remains the 'local' 37203A is defective.
   Identify the faulty area of the defective 37203A using the Instrument Troubleshooting in General Service Sheet G2.

   (b) Swap 37203A's at the 'local' site. Check the operation of the previous link with the system controller.
   If there is no fault the 'remote' 37203A is defective.
   If there is a fault the 'local' 37203A is defective.
   Identify the faulty area of the defective 37203A using the Instrument Troubleshooting in General Service Sheet G2.

6. After the fault has been eliminated run the Performance Verification routines, see Section 4.

G1-11 POINT-TO-POINT CONFIGURED SYSTEM (FIBRE OPTIC CABLE)

1. Is the DATA LOSS indicator ON?

   If the DATA LOSS indicator is 'OFF' proceed to step 2.
   If the DATA LOSS indicator is 'ON' check the serial link.

   (a) Connect the 37203A's together with a piece of coaxial cable.

   (b) Remove the top cover from both 37203A's.

   (c) Switch the COAX/OPT switch, A1S5, to COAX on both 37203A's.

   If the indicator goes OFF the fault is in the fibre optic transmitter, fibre optic receiver or fibre optic cable, see General Service Sheet G3.
   If the indicator stays ON the fault is in the Serial Section of either 37203A proceed to step 3 and disconnect the coaxial cable from both 37203A's.

2. Is the DATA ERRORS indicator ON?

   If the DATA ERRORS indicator is ON proceed to step 3.
   If the DATA ERRORS indicator is OFF jump to step 16.

3. Disconnect the fibre optic cable and HP-IB from the local 37203A and set the MASTER/SLAVE switch, on the rear panel, to MASTER.

4. Remove the top cover from the local 37203A.

5. Connect the oscilloscope to Test Point OUT using Test Point FGND to ground the oscilloscope probe.

6. Set the oscilloscope to 0.05μs/div, 0.2V/div and negative trigger.

7. Switch the local 37203A OFF for 5 seconds then ON.

8. Compare the waveform on the oscilloscope to Figure G1-7.

   If the waveform is identical proceed to step 9.
   If the waveform is different check the Serial Section and Control Logic, see Service Sheet A1 Parts 1 and 3.

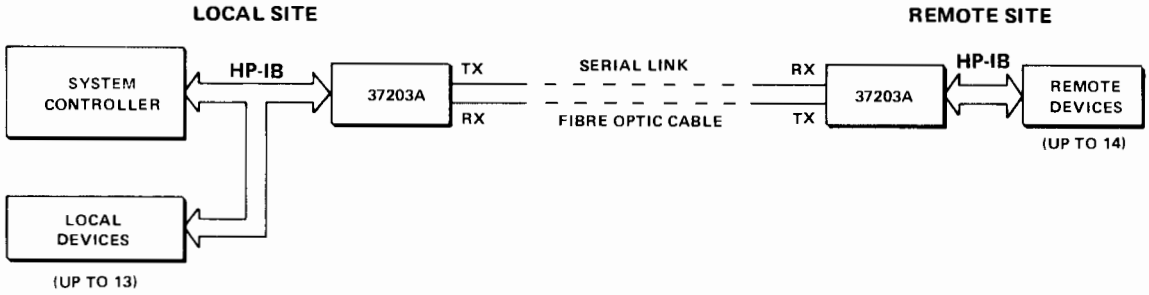


Figure G1-6 Point-to-Point Configured System (Fibre Optic)

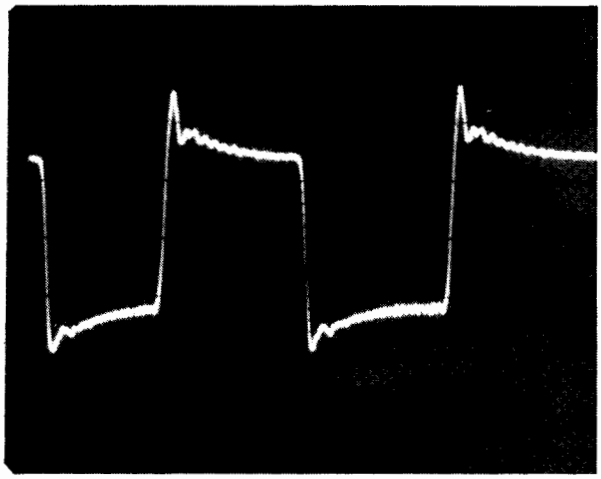


Figure G1-7 Start of Waveform of Transmit Frame

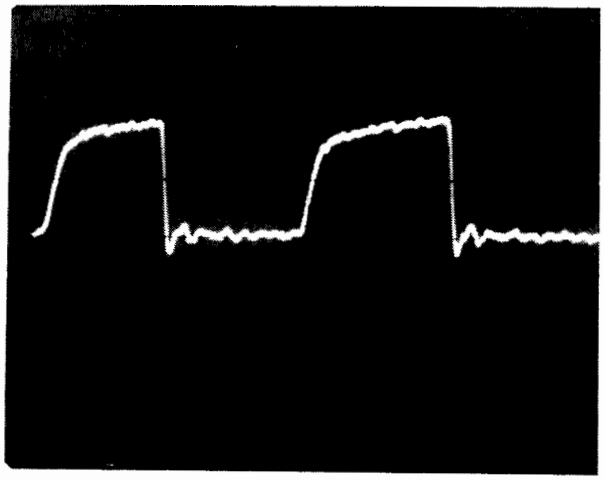


Figure G1-8 Start of Waveform of Receive Frame

9. Connect the oscilloscope to Test Point RX.

10. Set the oscilloscope to 0.05μs/div, 0.2V/div and positive trigger.

11. Switch the local 37203A OFF for 5 seconds then ON.

12. Compare the waveform on the oscilloscope to Figure G1-8.

    If the waveform is identical proceed to step 13.
    If the waveform is different check the Serial Section and Control Logic, see Service Sheet A1 Parts 1 and 3.

13. Disconnect the fibre optic cable and the HP-IB from the remote 37203A and set the MASTER/SLAVE switch on the rear panel to MASTER.

14. Repeat steps 4 to 11 on the remote 37203A.

15. Compare the waveform on the oscilloscope to Figure G1-8.

    If the waveform is identical proceed to step 16.
    If the waveform is different check the Serial Section and Control Logic, see Service Sheet A1 Parts 1 and 3.

16. Check the HP-IB Section in the remote 37203A, see Service Sheet A1 Part 2.

    If the remote HP-IB Section is correct proceed to step 17.

17. Check the HP-IB Section in the local 37203A, see Service Sheet A1 Part 2.

18. After the fault has been eliminated run the Performance Verification routines, see Section 4.

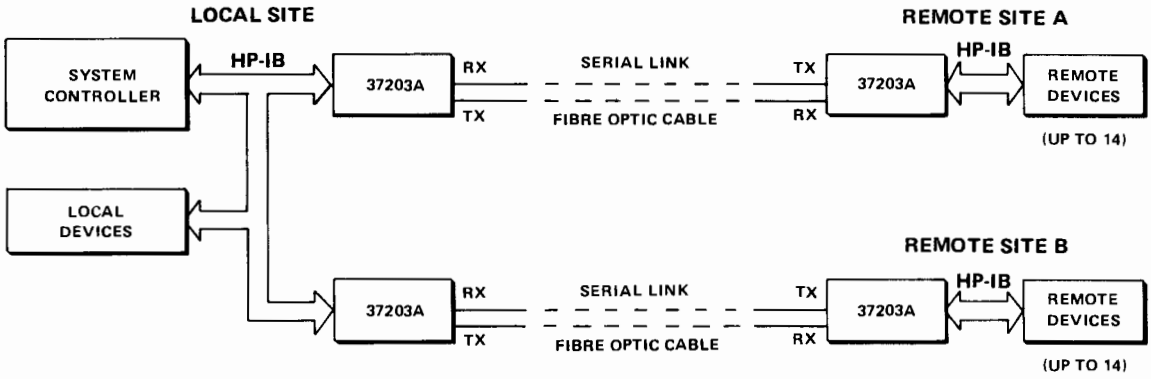


Figure G1-9 Star Configured System (Fibre Optic)

G1-12 STAR CONFIGURED SYSTEM (FIBRE OPTIC CABLE)

1. Check each link individually to isolate the faulty link.

   (a) Disconnect all the local 37203A's from the HP-IB.

   (b) Connect one local 37203A to the HP-IB.

   (c) Check that the system is operational using the System Controller.

   (d) Repeat (b) and (c) for each 37203A until the faulty link has been isolated. When the faulty link has been detected proceed to step 2.

2. Perform the troubleshooting on the faulty link as for the Point-to-Point configured system, see Paragraph G1-11.

G1-13 TANDEM CONFIGURED SYSTEM (FIBRE OPTIC CABLE)

1. Check each link individually to isolate the faulty link.

   (a) Disconnect the 'local' 37203A at remote site A from the HP-IB.

   (b) Check that the system is operational using the System Controller.

   (c) Repeat (a) and (b) at each remote site until the faulty link has been isolated. When the faulty link is detected proceed to step 2.

2. Perform the Point-to-Point configured system trouble-shooting on the faulty link, see Paragraph G1-11.

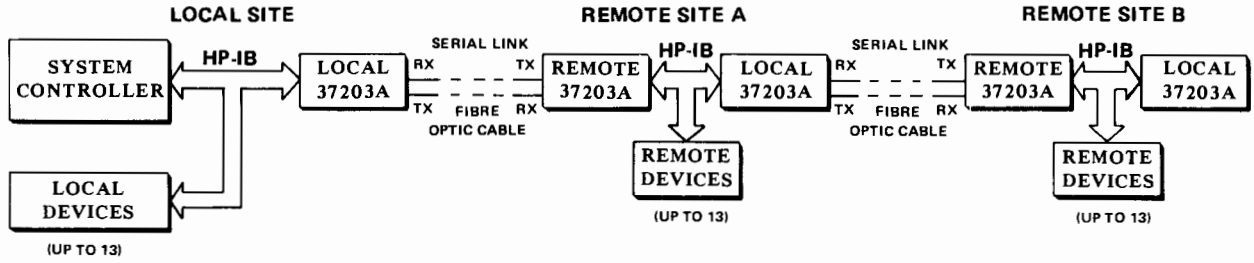


Figure G1-10 Tandem Configured System (Fibre Optic)

GENERAL SERVICE SHEET G2
INSTRUMENT TROUBLESHOOTING

G2-1 INTRODUCTION

G2-2 The following procedures verify the existence of a fault in a 37203A and isolate it to a section (Serial, HP-IB or Control Logic).

G2-3 EQUIPMENT REQUIRED

G2-4 Equipment required to carry out the Instrument Troubleshooting is given in Table G2-1.

G2-5 TROUBLESHOOTING PROCEDURE

G2-6 Using the faulty 37203A as the local 37203A and the spare 37203A as the remote 37203A, configure the system and run the Performance Verification as described in Section 4.

G2-7 The front panel indicators give an indication of the probable location of the fault.

G2-8 If the DATA LOSS indicator or DATA ERRORS indicator is ON the fault is most likely to be in the Serial Section or Control Logic, see Service Sheet A1 Parts 1 and 3.

G2-9 If the DATA LOSS and DATA ERRORS indicators are OFF and the Performance Verification fails to complete, the fault is in the HP-IB Section, see Service Sheet A1 Part 2.

G2-10 After the fault has been eliminated run the Performance Verification routines, see Section 4.

Table G2-1 Equipment Required

Quantity	Item	Type
1	HP-IB Extender	HP37203A
1	Desktop Computer	HP9825A
1	String & Advanced Programming ROM	HP98210A
1	General I/O & Extended I/O ROM	HP98213A
2	HP-IB Interface Card	HP98034A
1	Coax Cable	–
1	Performance Verification Tape	HP37203-12101
1	Oscilloscope	HP180C, 1809A, 1825A
1	10:1 Probe	HP10004D
1	Signature Analyser	HP50004A
1	Logic Probe	HP545A
1	Logic Pulser	HP546A

GENERAL SERVICE SHEET G3

FIBRE OPTIC TROUBLESHOOTING

G3-1 INTRODUCTION

G3-2 The troubleshooting contained in this service sheets is for Option 001. The procedures detect a fault in the fibre optic transmitter, fibre optic receiver or fibre optic cable.

G3-3 TROUBLESHOOTING PROCEDURE

1. Disconnect the fibre optic cable from the optical fibre receive port on both 37203A's and look for a glow at the end of each cable.

   If there is no glow at the end of either cable proceed to step 2.
   If there is a glow at the ends of both cables proceed to step 4.

2. Disconnect the fibre optic cable from the optical fibre transmit port.

3. Connect a short length of fibre optic cable to the optical fibre transmit port.

   If there is a glow at the end of the cable replace the fibre optic cable.
   If there is no glow at the end of the cable replace the fibre optic transmitter.

4. Clean the ends of the cable, see Section 3 Paragraph 3-29.

5. On the local 37203A connect the optical fibre transmit port to the optical fibre receive port with a short length of fibre optic cable.

6. Set the MASTER/SLAVE switch, on the rear panel, to MASTER on the local 37203A.

7. Remove the top cover of the local 37203A.

8. Compare the waveforms at Test Points TX and RX on the oscilloscope. The RX waveform should be the logical inverse of the TX waveform.

   If the waveform at Test Point RX is not the logical inverse of the waveform at Test Point TX jump to step 10.
   If the waveform at Test Point RX is the logical inverse of the waveform at Test Point TX proceed to step 9.

9. Repeat steps 5 to 8 on the remote 37203A.

   If the waveform at Test Point RX is not the logical inverse of the waveform at Test Point TX jump to step 12.
   If the waveform at Test Point RX is the logical inverse of the waveform at Test Point TX replace the fibre optic cable.

10. Connect the local optical fibre transmit port to the remote optical fibre receive port with a short length of fibre optic cable.

11. Compare the waveforms at the local Test Point TX and the remote Test Point RX on the oscilloscope. The RX waveform should be the logical inverse of the TX waveform.

    If the RX waveform is the logical inverse of the TX waveform replace the fibre optic receiver in the local 37203A.
    If the RX waveform is not the logical inverse of the TX waveform replace the fibre optic transmitter in the local 37203A.

12. Connect the remote optical fibre transmit port to the local optical fibre receive port with a short length of fibre optic cable.

13. Compare the waveforms at the remote Test Point TX and the local Test Point RX on the oscilloscope. The RX waveform should be the logical inverse of the TX waveform.

    If the RX waveform is the logical inverse of the TX waveform replace the fibre optic receiver in the remote 37203A.
    If the RX waveform is not the logical inverse of the TX waveform replace the fibre optic transmitter in the remote 37203A.

SERVICE SHEET A1

PART 1 – SERIAL SECTION

A1-1 TROUBLESHOOTING

A1-2 There are two schematic diagrams given in this Service Sheet due to the test board A1TL1 having two modes, RUN shown in Figure A1-3 and TEST shown in Figure A1-4. Set A1TL1 to the RUN position.

A1-3 Receive Coupler Logic and Transmit Coax Driver

Check 1

The typical voltages at various points of the circuit are given in Table A1-1.

Check 2

The built-in overshoot on the transmit waveform can be observed by connecting the oscilloscope to Test Point OUT and grounding the probe at Test Point FGND, see Figure A1-1.

A1-4 Signature Analysis of the Registers

A1-5 The Delay Registers, Decoder, Encoder, Parity Check, 16-Bit Data Register and Parallel Register can be tested using Signature Analysis.

A1-6 Ensure that the 37203A is not connected to any other device and the switches are set as shown in Table A1-2.

Table A1-1 Typical Voltages

Monitor Point	Voltage
Q1 EMITTER	+1.05V
Q2 BASE	–0.40V
Q3, Q4 COLLECTOR	+2.15V
Q5 EMITTER	+1.6V
Q6 BASE	+1.3V

Important Note: These voltages were obtained with the 37203A configured as a MASTER and using Test Point FGND as the ground connection.

Table A1-2 Switch Settings

Switch	Setting
A1S1	RUN
A1S2	OFF (ALL 6)
A1S3	NORMAL
A1S4	MASTER
A1S5	COAX
A1TL1	TEST

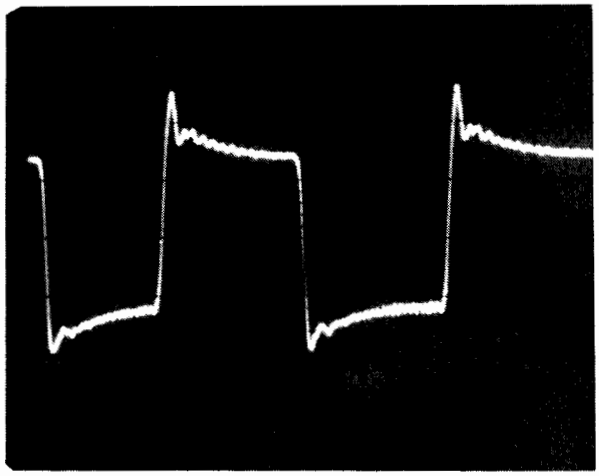


Figure A1-1 Start of Transmit Waveform

A1-7 With the 37203A configured as a Master a data frame is transmitted approximately every 30μs. A1TL1 set to Test forces ASM 'A' and ASM 'B' to cycle while ASM 'D', which produces two complimentary states, forces the inputs to the 16-Bit Data Register into a known state. The schematic diagram showing A1TL1 in the Test Position is shown in Figure A1-4.

A1-8 An HP5004A Signature Analyzer (SA) is required for the following checks. Connect the SA as follows:

CLOCK probe. . . . . .Test Point CL
START probe . . . . . .Test Point SS
STOP probe . . . . . .Test Point SS
GROUND probe . . . . . .Test Point GD
Logic probe ground . . . . . .Test Point GD

Set the S.A. controls as follows:

LINE switch. . . . . .IN
START switch . . . . . .IN
STOP switch. . . . . .IN
CLOCK switch . . . . . .IN
HOLD switch . . . . . .OUT
SELF TEST switch . . . . . .OUT

Check 1

Check that the S.A. Gate lamp is flashing, if not proceed to the Control Logic Troubleshooting (Service Sheet A1 Part 3).

Note: Before taking signatures, switch the 37203A power OFF for approximately 5 seconds then ON to provide a reset.

Check 2

Check +5V signature is A5C1 and 0V signature is 0000.

Check 3

Check the signatures in the Serial Section with the ones given below in Table A1-3. Correct signatures indicate that the Serial Section appears to be operational. If one signature is faulty the device can be assumed to be faulty. If all the signatures are incorrect check the Control Logic Troubleshooting, see Service Sheet A1 Part 3. If all the signatures are correct check the HP-IB Section, see Service Sheet A1 Part 2.

Table A1-3 Signature List

	Monitor Point	Signature
Delay Register	U35 (15)	4256
Decoder	U43 (12)	AU87
	U43 (13)	HCA2
	U51 (8)	3673
Parity Check	U36 (12)	09PP
	U36 (13)	9770
	U36 (14)	2PP1
	U36 (15)	H96U
16 Bit Data Register	U37 (12)	C38U
	U37 (13)	89FH
	U37 (14)	79P4
	U37 (15)	1H1A
	U38 (12)	6HC3
	U38 (13)	35C5
	U38 (14)	0115
	U38 (15)	PFU8
	U39 (12)	4050
	U39 (13)	6P72
	U39 (14)	C69A
	U39 (15)	83P6
	U40 (12)	37C1
	U40 (13)	81C0
	U40 (14)	H79F
	U40 (15)	9517
Delay Register	U41 (15)	H17H
Encoder	U42 (12)	768P
	U42 (13)	A8PH
	U42 (14)	8045
Parallel Register	U44 (2)	HA3U
	U44 (5)	HA3U
	U44 (6)	HA3U
	U44 (9)	HA3U
	U44 (12)	HA3U
	U44 (15)	HA3U
	U44 (16)	HA3U
	U44 (19)	HA3U
	U45 (2)	HA3U
	U45 (5)	HA3U
	U45 (6)	HA3U
	U45 (9)	HA3U
	U45 (12)	HA3U
	U45 (15)	7U8P
	U45 (16)	HA3U
	U45 (19)	HA3U

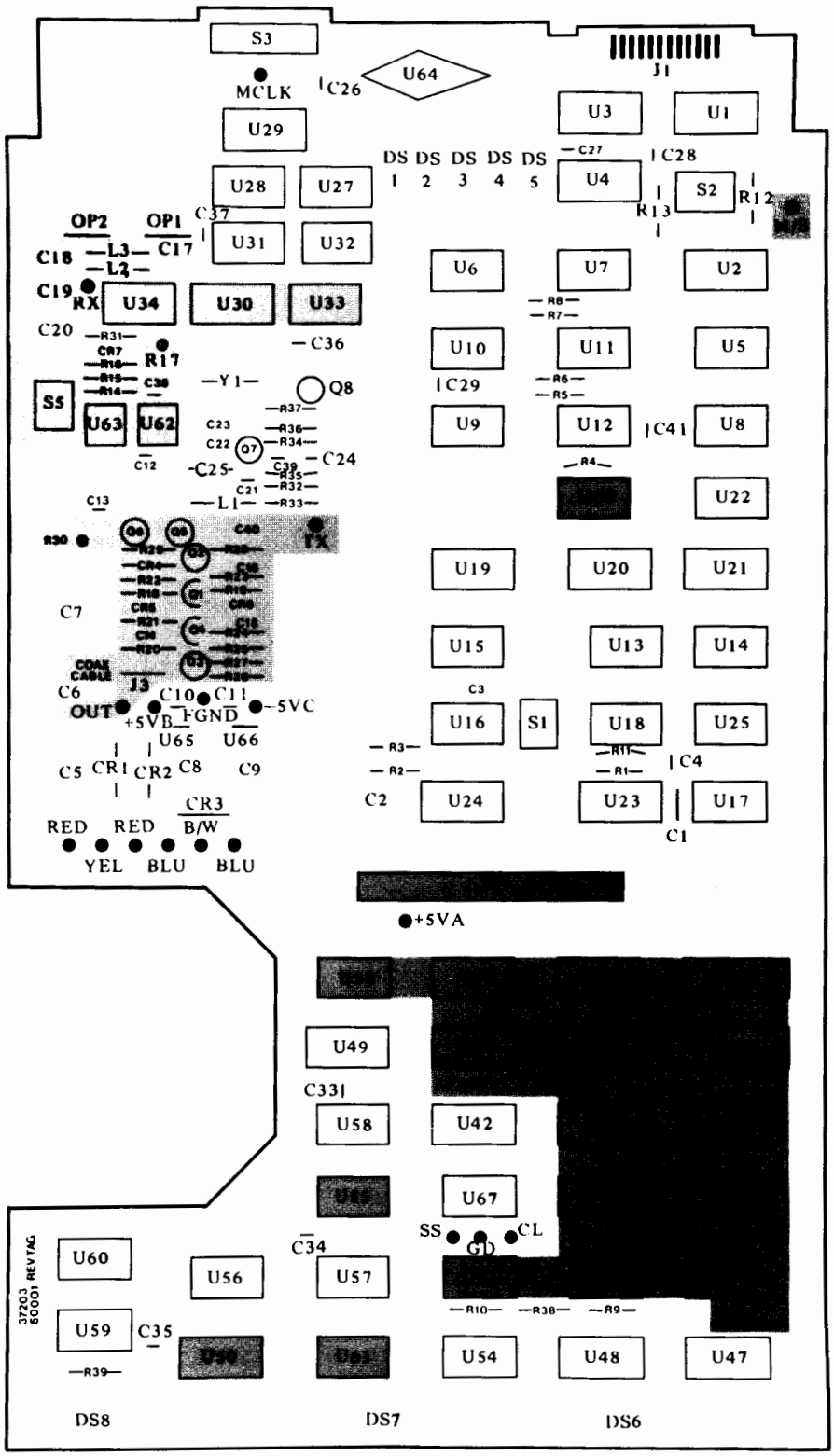


Figure A1-2 Component Location A1 Part 1

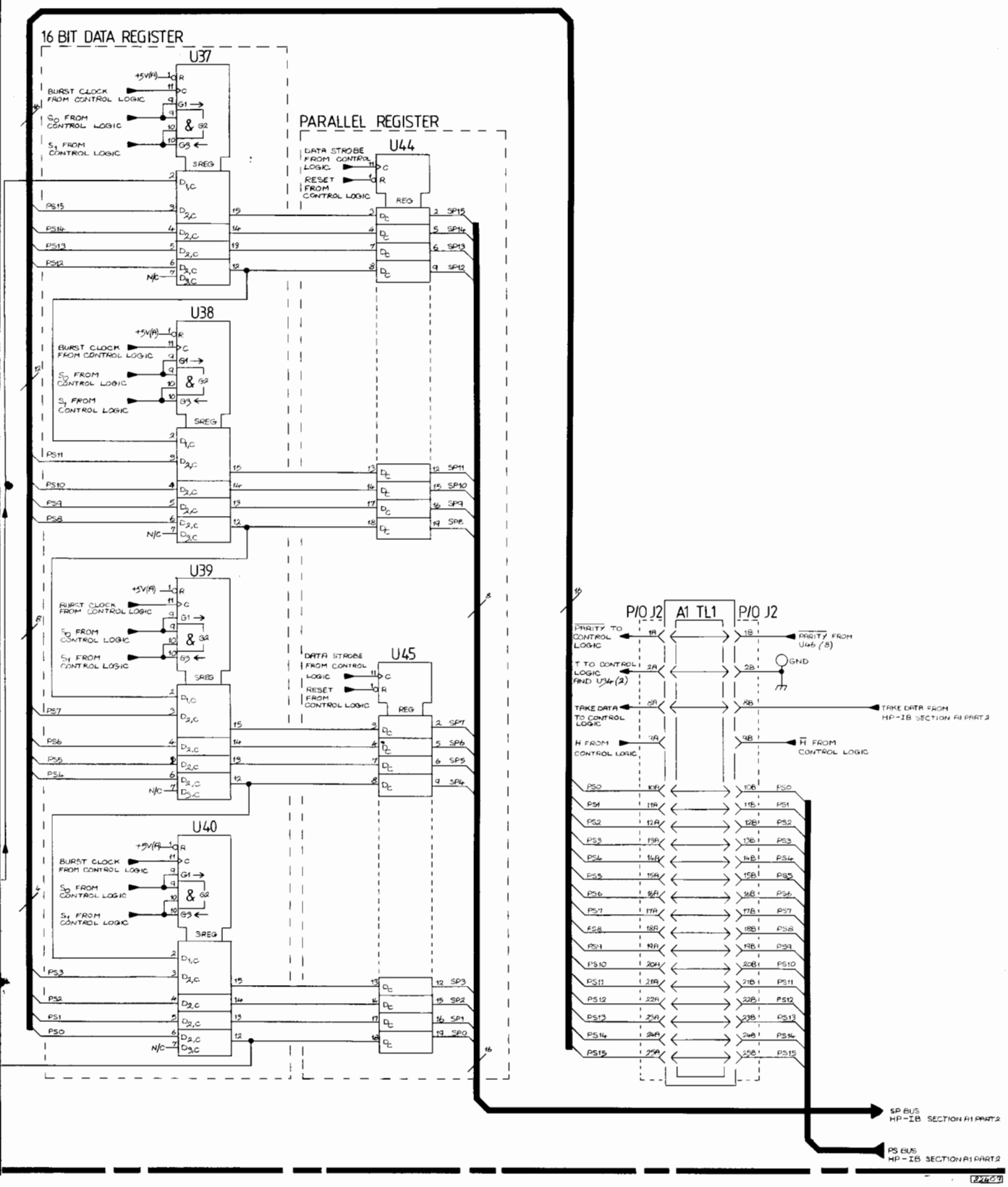
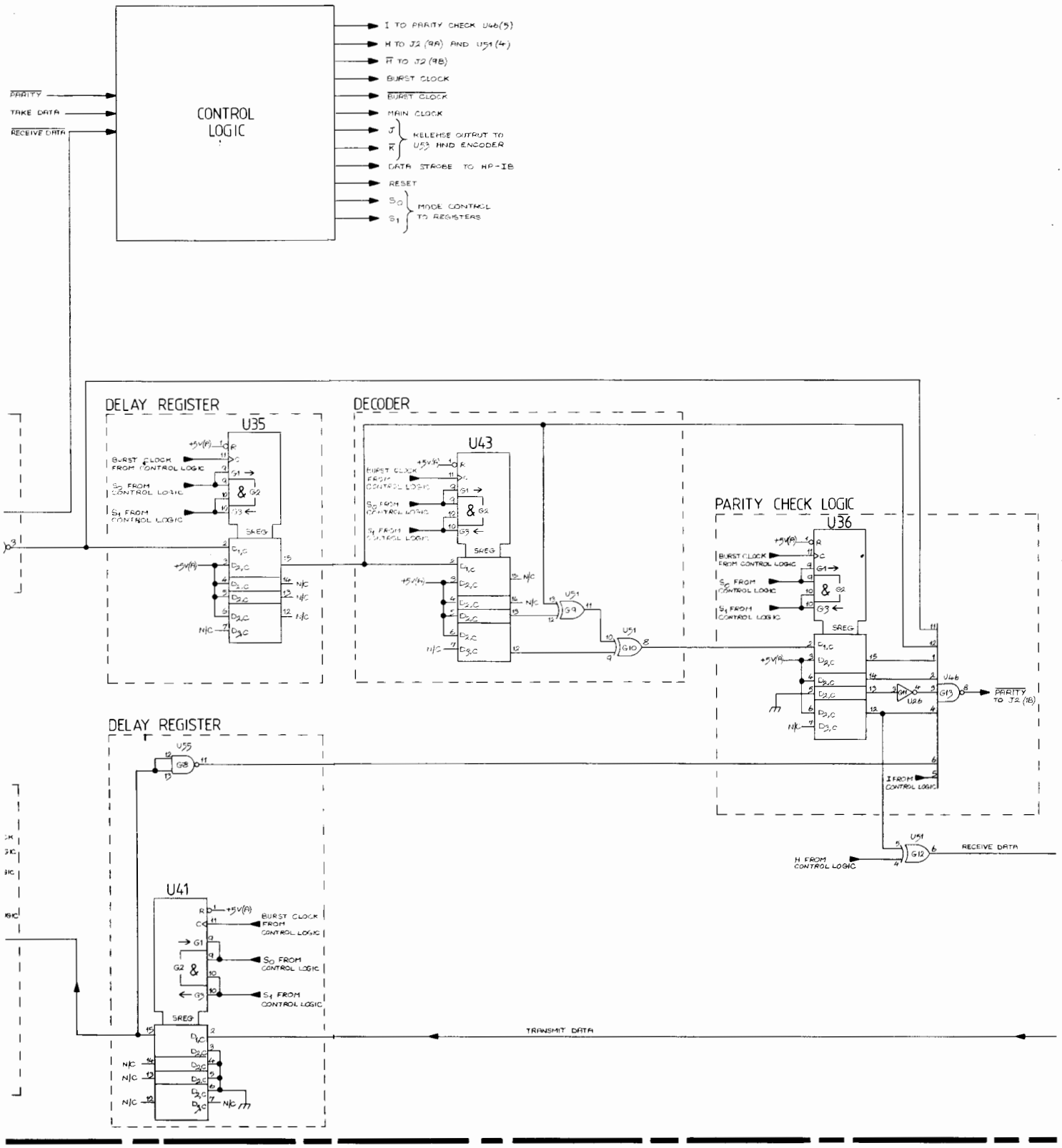
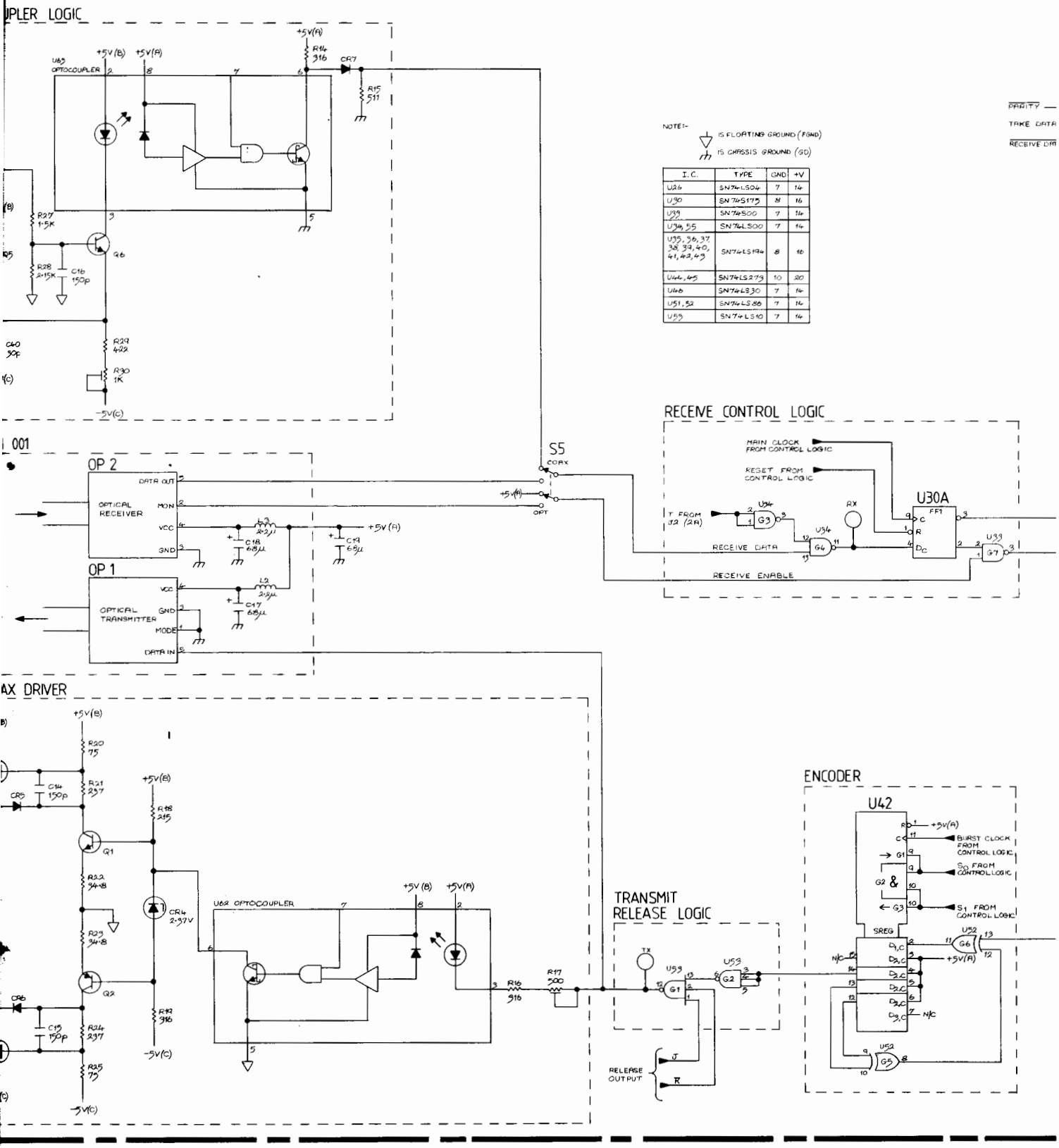


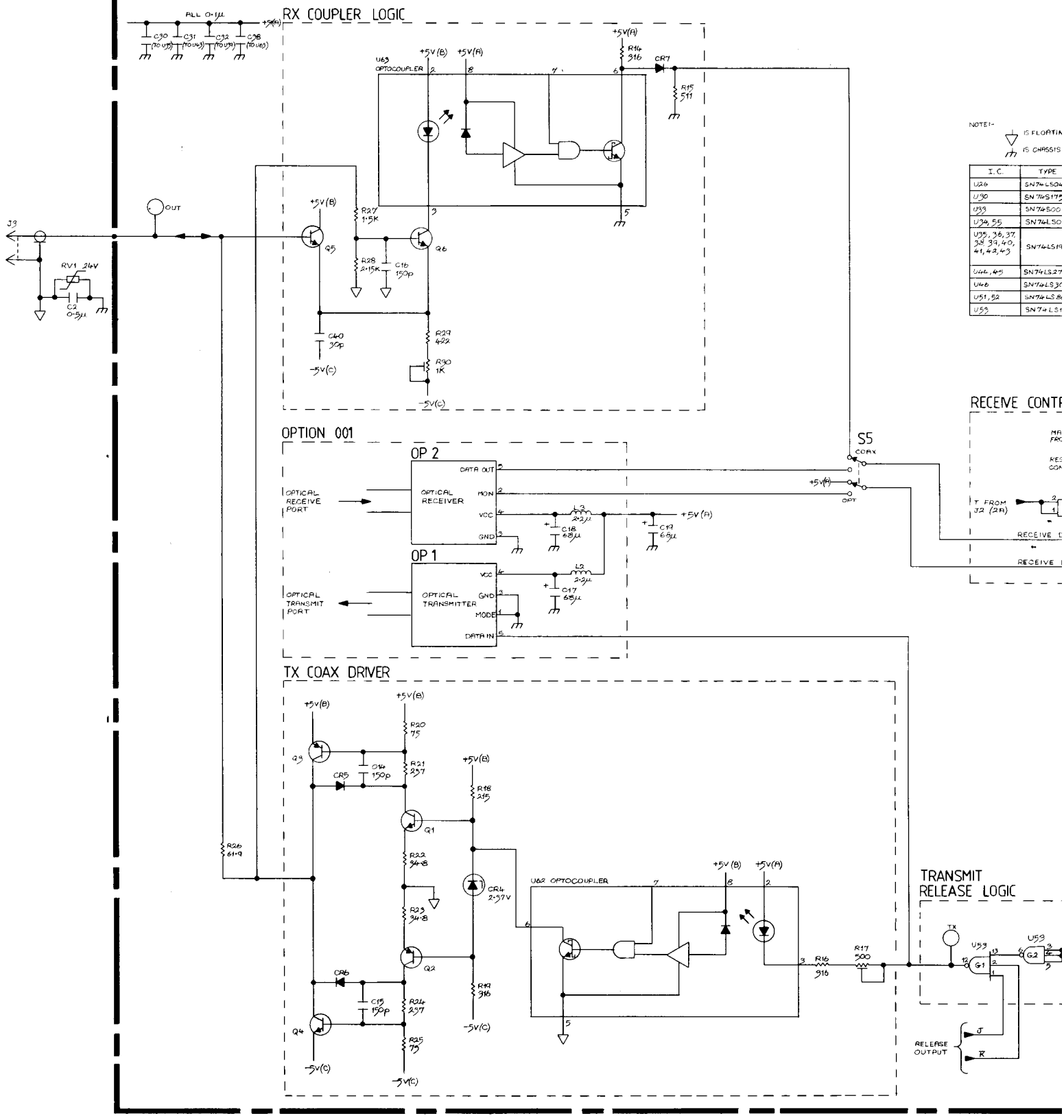
Figure A1-3 Schematic Diagram A1 Part 1A


CONTROL LOGIC
PARITY
TAKE DATA
RECEIVE DATA
I TO PARITY CHECK U46(5)
H TO J2 (9A) AND U51(4)
H TO J2 (9B)
BURST CLOCK
BURST CLOCK
MAIN CLOCK
J
K
RELEASE OUTPUT TO U53 HND ENCODER
DATA STROBE TO HP-IB
RESET
S0
S1
MODE CONTROL TO REGISTERS
DELAY REGISTER
U35
DECODER
U43
PARITY CHECK LOGIC
U36
BURST CLOCK FROM CONTROL LOGIC
S0 FROM CONTROL LOGIC
S1 FROM CONTROL LOGIC
SREG
U51
G9
G10
U46
G13
PARITY TO J2 (1B)
I FROM CONTROL LOGIC
G12
RECEIVE DATA
H FROM CONTROL LOGIC
DELAY REGISTER
U55
G8
U41
TRANSMIT DATA

(37203-60001)


UPLER LOGIC
+5V(A)
+5V(B)
U63 OPTOCOUPLER
R14 316
CR7
R15 511
R27 1·5K
Q6
R28 2·15K
C16 150p
R29 422
R30 1K
-5V(C)
NOTE:-
IS FLOATING GROUND (FGND)
IS CHASSIS GROUND (GD)
I.C. | TYPE | GND | +V
U26 | SN74LS04 | 7 | 14
U30 | SN74S175 | 8 | 16
U39 | SN74S00 | 7 | 14
U34,55 | SN74LS00 | 7 | 14
U35,36,37,38,39,40,41,42,43 | SN74LS194 | 8 | 16
U44,45 | SN74LS273 | 10 | 20
U46 | SN74LS30 | 7 | 14
U51,52 | SN74LS86 | 7 | 14
U53 | SN74LS10 | 7 | 14
PARITY
TAKE DATA
RECEIVE DATA
RECEIVE CONTROL LOGIC
MAIN CLOCK FROM CONTROL LOGIC
RESET FROM CONTROL LOGIC
T FROM J2 (2A)
U34
G3
RX
U30A
FF1
RECEIVE DATA
G4
U33
G7
RECEIVE ENABLE
S5
COAX
OPT
+5V(A)
OP 2
OPTICAL RECEIVER
DATA OUT
MON
VCC
GND
L3 2·2µ
C18 65µ
C19 65µ
OP 1
OPTICAL TRANSMITTER
L2 2·2µ
C17 65µ
MODE
DATA IN
AX DRIVER
+5V(B)
R20 75
C14 150p
CR5
R21 237
Q1
R22 348
R23 348
CR4 2·37V
Q2
CR6
C13 150p
R24 237
R25 75
-5V(C)
R18 215
R19 316
U6R OPTOCOUPLER
R16 316
R17 500
TRANSMIT RELEASE LOGIC
TX
U59
U53
G1
G2
RELEASE OUTPUT
J
R
ENCODER
U42
+5V(A)
BURST CLOCK FROM CONTROL LOGIC
G1
S_0 FROM CONTROL LOGIC
G2 &
G3
S_1 FROM CONTROL LOGIC
SREG
U52
G6
G5
N/C

A1 PART 1A SERIAL SECTION (37203-60001)



NOTE:-
IS FLOATIN
IS CHASSIS

I.C.	TYPE
U26	SN74LS04
U30	SN74S175
U33	SN74S00
U34, 55	SN74LS00
U35, 36, 37, 38, 39, 40, 41, 42, 43	SN74LS19
U44, 45	SN74LS27
U46	SN74LS30
U51, 52	SN74LS86
U53	SN74LS1

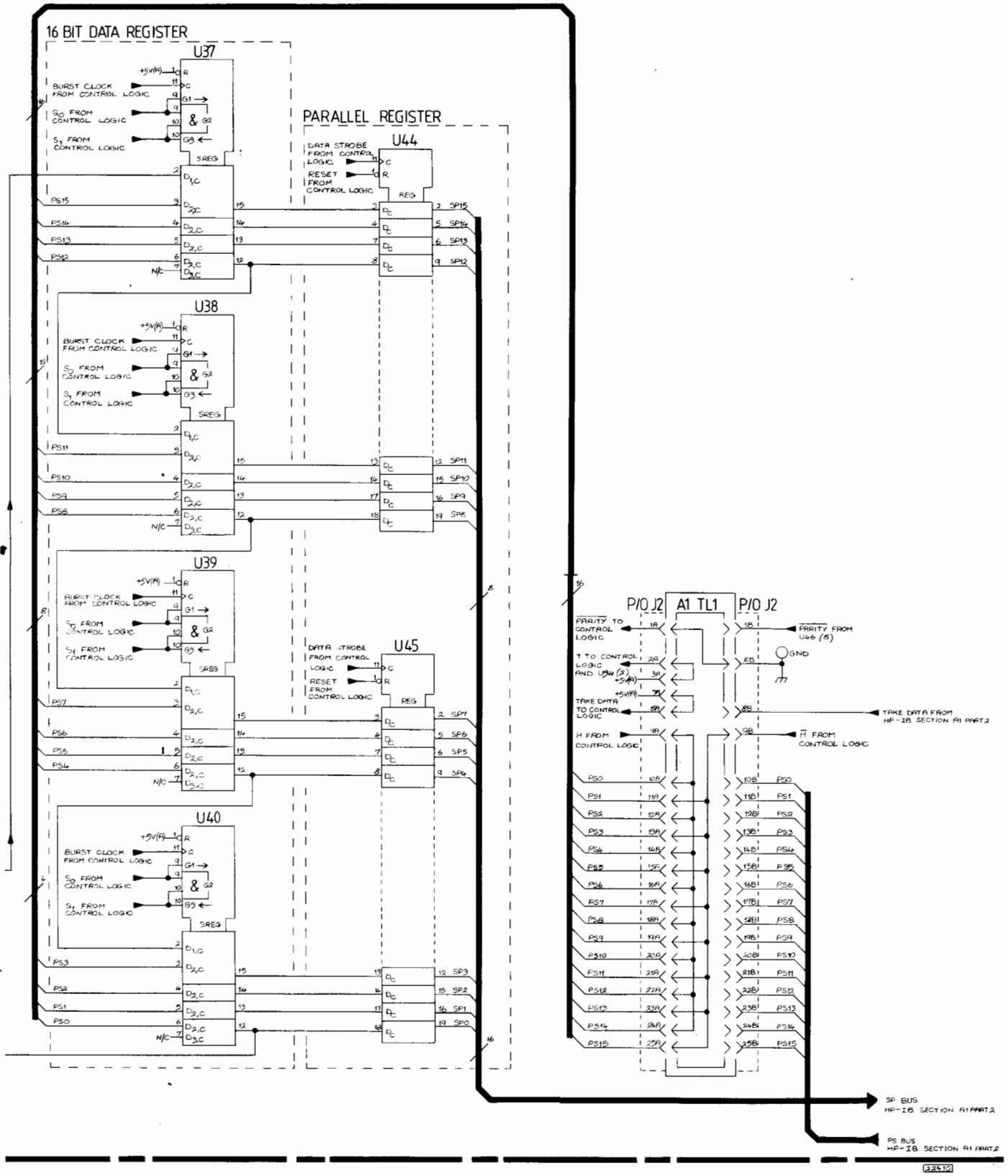
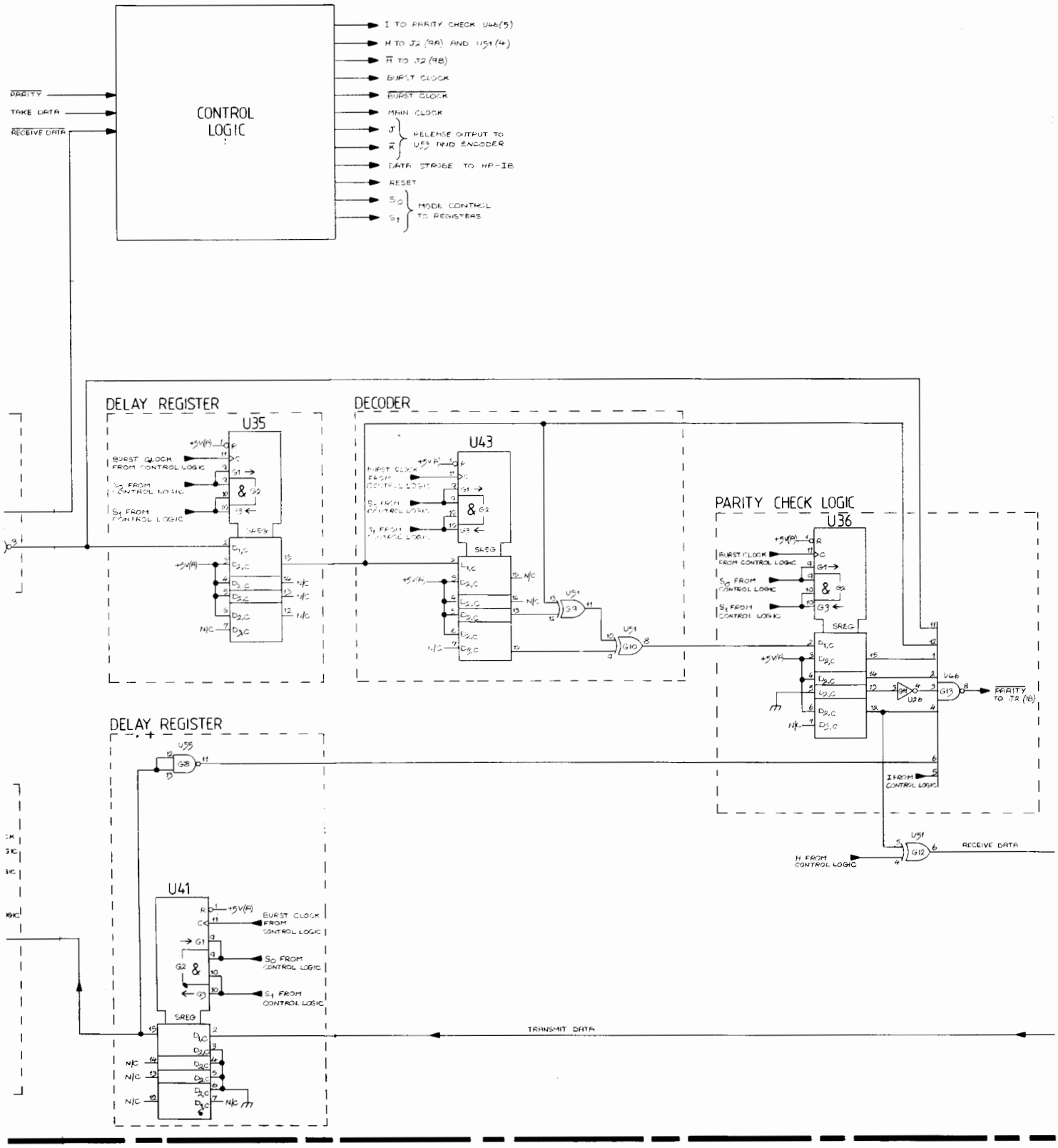
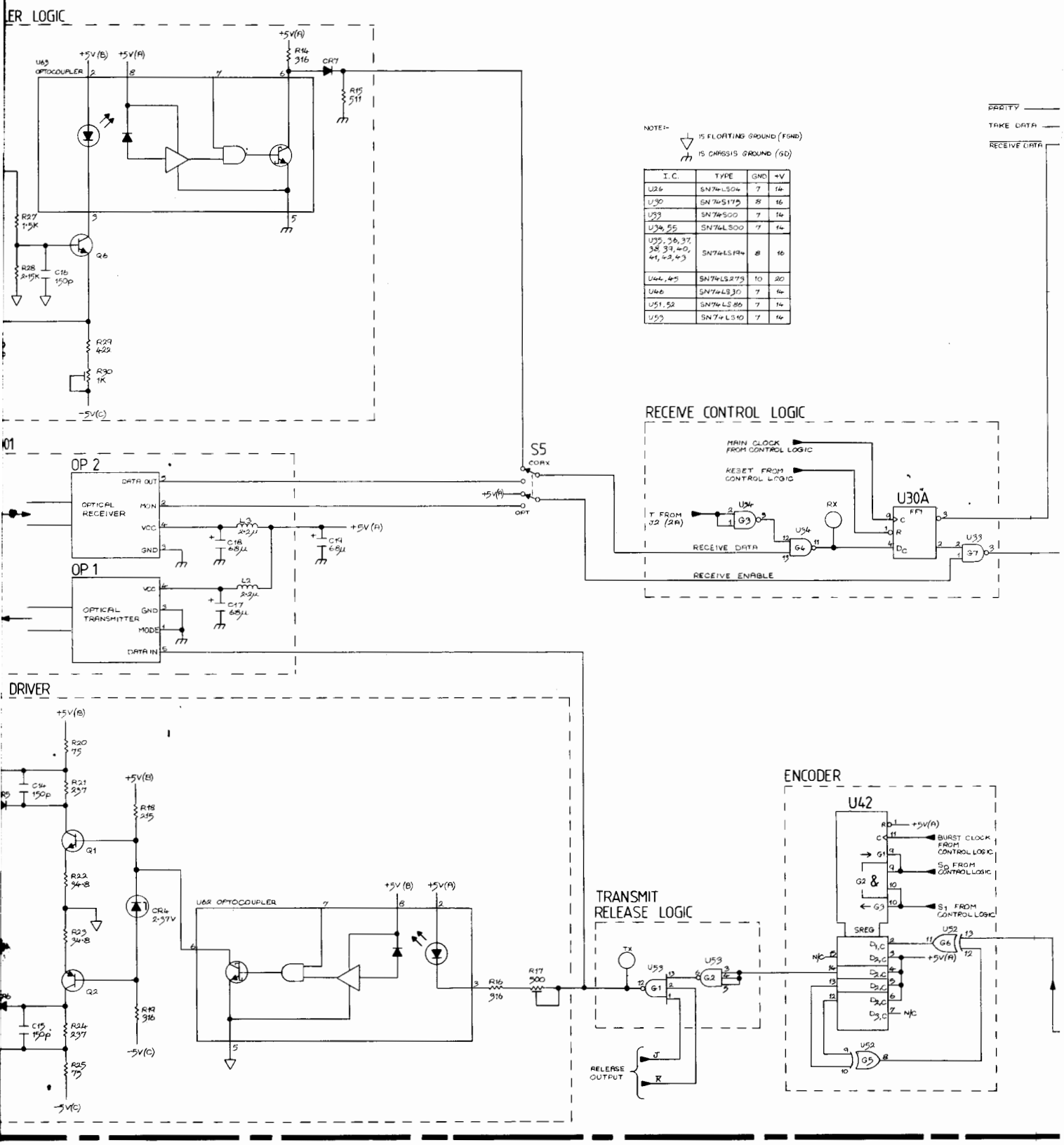
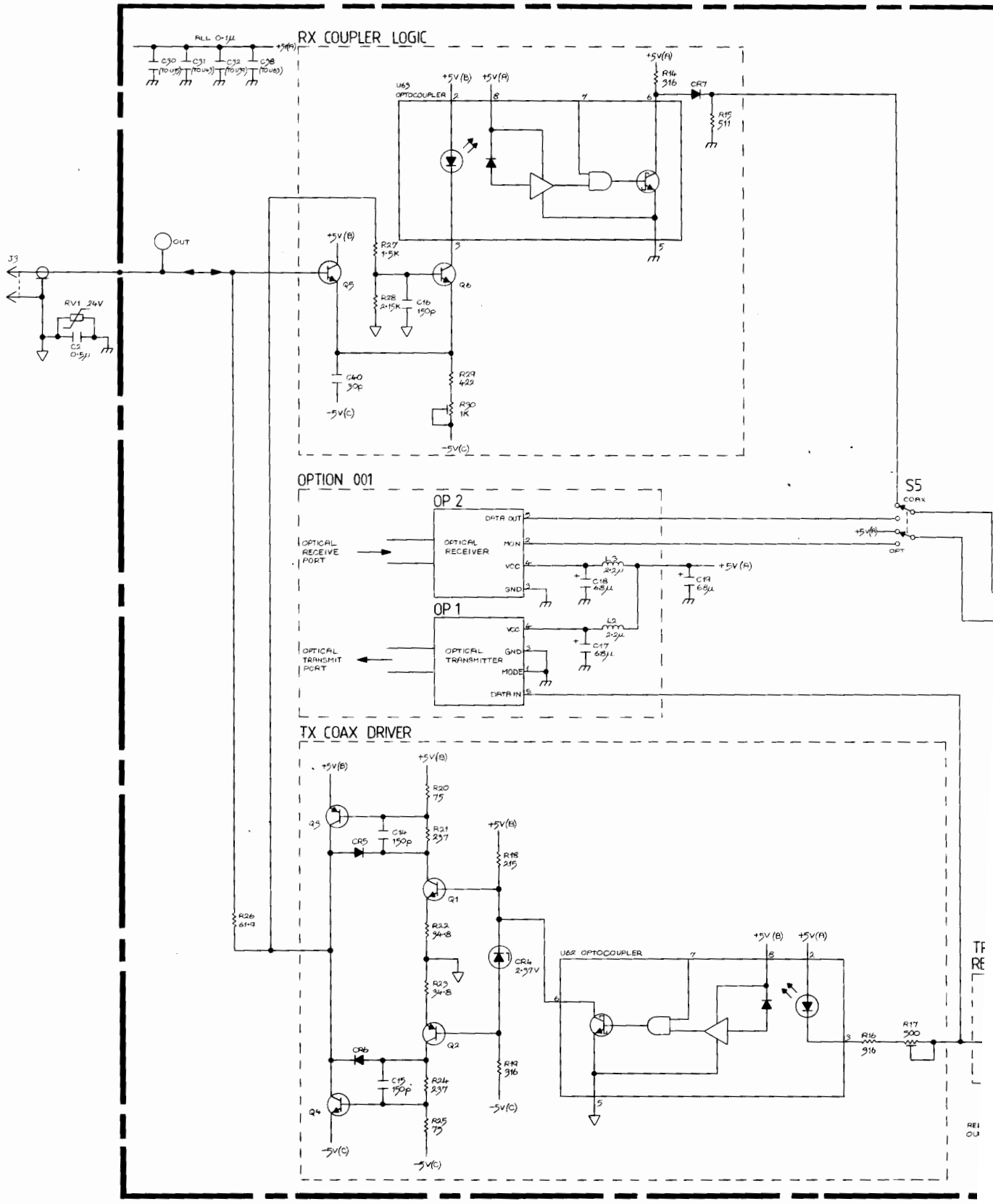


Figure A1-4 Schematic Diagram A1 Part 1B (Troubleshooting)


CONTROL LOGIC
PARITY
TAKE DATA
RECEIVE DATA
I TO PARITY CHECK U46(5)
H TO J2 (9A) AND U51(4)
H TO J2 (9B)
BURST CLOCK
BURST CLOCK
MAIN CLOCK
J
K
RELEASE OUTPUT TO U53 FIND ENCODER
DATA STROBE TO HP-IB
RESET
S0
S1
MODE CONTROL TO REGISTERS
DELAY REGISTER
U35
DECODER
U43
PARITY CHECK LOGIC
U36
DELAY REGISTER
U55
U41
BURST CLOCK FROM CONTROL LOGIC
S0 FROM CONTROL LOGIC
S1 FROM CONTROL LOGIC
SREG
+5V(A)
N/C
U51
U46
PARITY TO J2 (18)
I FROM CONTROL LOGIC
H FROM CONTROL LOGIC
RECEIVE DATA
TRANSMIT DATA


ER LOGIC
U43 OPTOCOUPLER
+5V(B)
+5V(A)
R14 316
CR7
R15 511
R27 1·5K
Q6
R28 2·15K
C16 150p
R29 422
R30 1K
-5V(C)
NOTE:-
IS FLOATING GROUND (FGND)
IS CHASSIS GROUND (GD)
I.C. | TYPE | GND | +V
U26 | SN74LS04 | 7 | 14
U30 | SN74S175 | 8 | 16
U33 | SN74S00 | 7 | 14
U34,55 | SN74LS00 | 7 | 14
U35,36,37,38,39,40,41,42,43 | SN74LS194 | 8 | 16
U44,45 | SN74LS273 | 10 | 20
U46 | SN74LS30 | 7 | 14
U51,52 | SN74LS86 | 7 | 14
U53 | SN74LS10 | 7 | 14
PARITY
TAKE DATA
RECEIVE DATA
RECEIVE CONTROL LOGIC
MAIN CLOCK FROM CONTROL LOGIC
RESET FROM CONTROL LOGIC
T FROM J2 (2A)
U34
G3
RX
U30A
FF1
RECEIVE DATA
G4
U33
RECEIVE ENABLE
01
OP 2
DATA OUT
OPTICAL RECEIVER
MON
VCC
GND
L2 2·2µ
C18 68µ
+5V(A)
C14 68µ
S5
COAX
OPT
OP 1
OPTICAL TRANSMITTER
MODE
DATA IN
L3 2·2µ
C17 68µ
DRIVER
R20 75
C14 150p
R21 237
R18 215
Q1
R22 34·8
CR4 2·37V
U62 OPTOCOUPLER
R23 34·8
Q2
C15 150p
R24 237
R19 316
R25 75
R16 316
R17 500
TRANSMIT RELEASE LOGIC
TX
U53
G1
G2
RELEASE OUTPUT
J
K
ENCODER
U42
BURST CLOCK FROM CONTROL LOGIC
S0 FROM CONTROL LOGIC
S1 FROM CONTROL LOGIC
SREG
U52
G6
G5
N/C

A1 PART 1B SERIAL SECTION (TROUBLESHOOTING) (37203-60001)



SERVICE SHEET A1
PART 2 – HP-IB SECTION

A1-9 TROUBLESHOOTING

A1-10 Acceptor Handshake and Source Handshake Logic

A1-11 The Acceptor and Source Handshake Logic can be thoroughly checked using DIP switch A1S2 to force the Handshake Logic round its four states. The indicators (DS1 – DS5) give a visual indication of each state.

A1-12 Set switch A1S1 to TEST. Switch A1S2 configuration is shown in Figure A1-5.

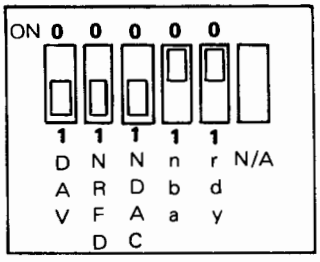


Figure A1-5 Switch A1S2 Configuration

Check 1 – Acceptor Handshake Logic

The Acceptor Handshake Logic is checked by toggling rdy and DAV and observing indicators A(DS1) and B(DS2). The remaining DIP switches should be left alone. Indicators C(DS3), D(DS4) and E(DS5) should be ignored. The switch positions should be changed in the sequence given in Table A1-4.

Table A1-4 Acceptor Handshake Switch Settings

Switch Setting					Indicator	
DAV	NRFD	NDAC	nba	rdy	A	B
1	1	1	0	0	0	0
1	1	1	0	1	0	1
0	1	1	0	1	1	1
0	1	1	0	0	1	0
1	1	1	0	0	0	0

Indicator 0 is OFF
1 is ON

If the Acceptor Handshake Logic fails to complete the 4 stakes refer to Schematic diagram Figure A1-9.

Check 2 – Source Handshake Logic

The Source Handshake Logic is checked by toggling NRFD, NDAC and nba and observing indicators C(DS3) and D(DS4). The remaining DIP switches should be left alone. Indicators A(DS1), B(DS2) and E(DS5) should be ignored. The switch positions should be changed in the sequence given in Table A1-5.

Table A1-5 Source Handshake Switch Settings

Switch Setting					Indicator	
DAV	NRFD	NDAC	nba	rdy	C	D
1	0	0	0	0	0	0
1	0	0	1	0	0	1
1	1	0	1	0	1	1
1	0	0	1	0	1	1
1	0	1	1	0	1	0
1	0	0	1	0	1	0
1	0	0	0	0	0	0

Indicator 0 is OFF
1 is ON

If the Source Handshake Logic fails to complete the four states refer to Schematic Diagram Figure A1-9.

A1-13 Controller Location Machine

A1-14 The Controller Location Machine can be checked using a logic pulser and observing indicator E(DS5).

Check 1

Set switch A1S1 to TEST. Set switch A1S2 as shown in Figure A1-6

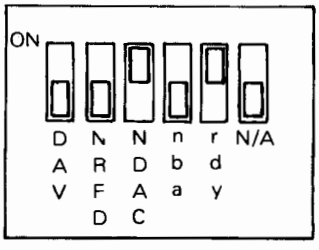


Figure A1-6 A1S2 Switch Setting

Switch the 37203A power OFF for 5 seconds then ON to provide a reset. Indicator E(DS5) should be OFF.

Using the logic pulser pulse U1 pin 10 and indicator E should come on. Pulse SP13 at U5 pin 5 and indicator E should go off.

A1-15 Bus Tranceivers and Serial to Parallel Bus (SP BUS)

A1-16 The Bus Tranceivers and SP Bus can be checked using Signature Analysis. Ensure that the 37203A is not connected to any other device and the switches are set as shown in Table A1-6.

Table A1-6 Switch Settings

Switch	Setting
A1S1	RUN
A1S2	OFF (ALL 6)
A1S3	1/16
A1S4	MASTER
A1S5	COAX
A1TL1	TEST

Check 1

An HP 5004A Signature Analyzer is required for the following check. Connect the SA as follows:

CLOCK probe . . . . . .Test Point CL
START probe . . . . . .Test Point SS
STOP probe. . . . . .Test Point SS
GND probe . . . . . .Test Point GD
Logic probe ground. . . . . .Test Point GD

Set the SA controls as follows:

LINE switch. . . . . .IN
START switch . . . . . .IN
STOP switch. . . . . .IN
CLOCK switch . . . . . .IN
HOLD switch . . . . . .OUT
SELF TEST switch . . . . . .OUT

Check that the SA Gate lamp is flashing if not proceed to the Control Logic Troubleshooting (Service Sheet A1 Part 3).

Check that the signatures on the SP Bus (SP0 to SP14) are 5AAH. If the signatures are incorrect proceed to the Anti-latch Logic and Bus Transceivers (see Paragraph A1-17). Check the signatures at the Bus Transceivers with the signatures listed in Table A1-7.

Table A1-7 Bus Transceivers Signatures

Pin	U1	U2	U3	U4
1	UU1F	FAP6	2511	A5C1
3	UU1F	FAP6	UU1F	5AAH
5	UU1F	1PUU	UU1F	UU1F
7	UU1F	1PUU	2511	2511
9	UU1F	UU1F	2511	2511
11	UU1F	UU1F	UU1F	UU1F
13	UU1F	P8CP	UU1F	UU1F
15	UU1F	P8CP	2511	2511

If all the signatures are incorrect check the Control Logic Troubleshooting (Service Sheet A1 Part 3). If one signature is incorrect the Anti-latch Logic should be checked – proceed to Paragraph A1-17.

A1-17 Anti-latch Logic and Bus Transceiver

A1-18 The Anti-latch Logic and Bus Transceivers can be checked using a logic pulser and a logic probe simultaneously.

Check 1

Set switch A1S1 to TEST. Set switch A1S2 as shown in Figure A1-7.

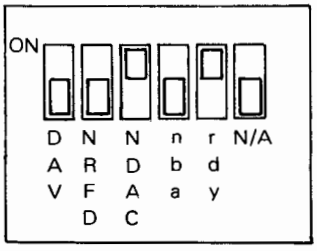


Figure A1-7 A1S2 Switch Setting

Switch the 37203A power OFF for 5 seconds then on to provide a reset.

Connect the logic pulser to SP0, U7(13), and pulse the input (high).

Connect the logic probe to outputs U7(12), U4(14), U4(15) and check the outputs pulse low each time U7(13) is pulsed. This check should be repeated for inputs SP1 to SP14 (excluding SP8 & SP9). The adjacent outputs of the Bus Transceivers can be checked to eliminate internal shorts.

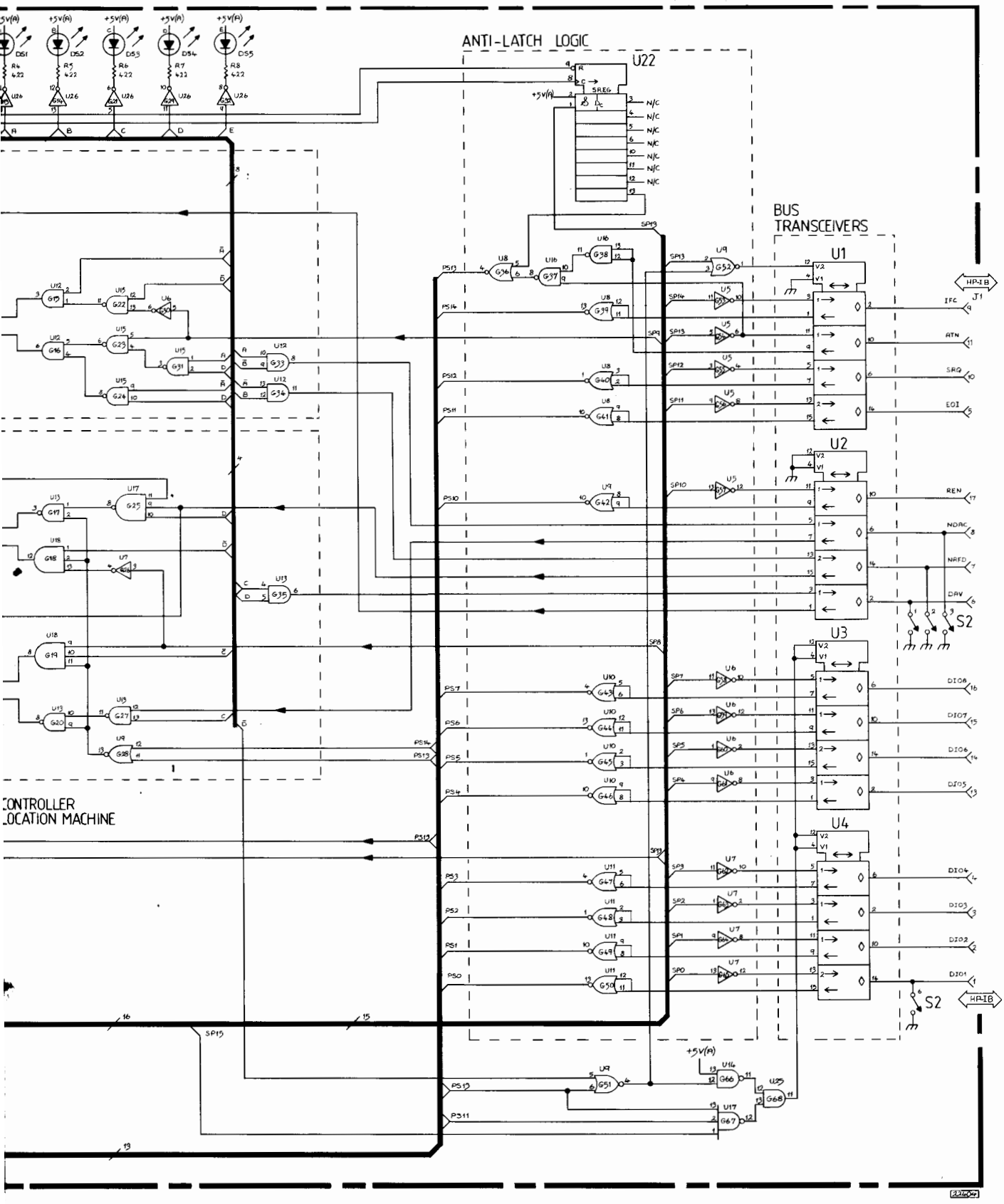
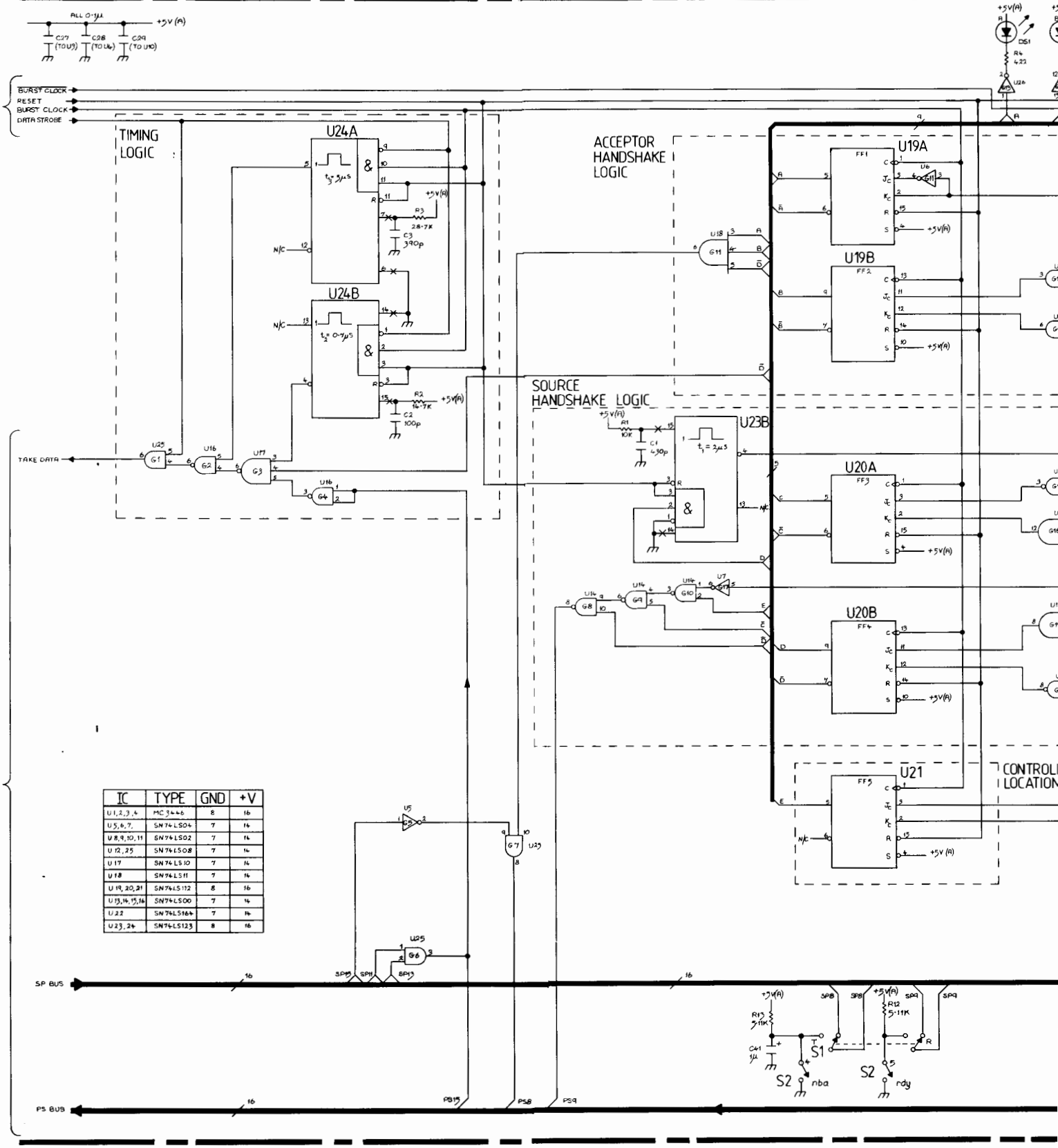


Figure A1-9 Schematic Diagram A1 Part 2

A1 PART 2 - HP-IB SECTION (37203-60001)



IC	TYPE	GND	+V
U1,2,3,4	MC3446	8	16
U5,6,7,	SN74LS04	7	14
U8,9,10,11	SN74LS02	7	14
U12,25	SN74LS08	7	14
U17	SN74LS10	7	14
U18	SN74LS11	7	14
U19,20,21	SN74LS112	8	16
U13,14,15,16	SN74LS00	7	14
U22	SN74LS164	7	14
U23,24	SN74LS123	8	16

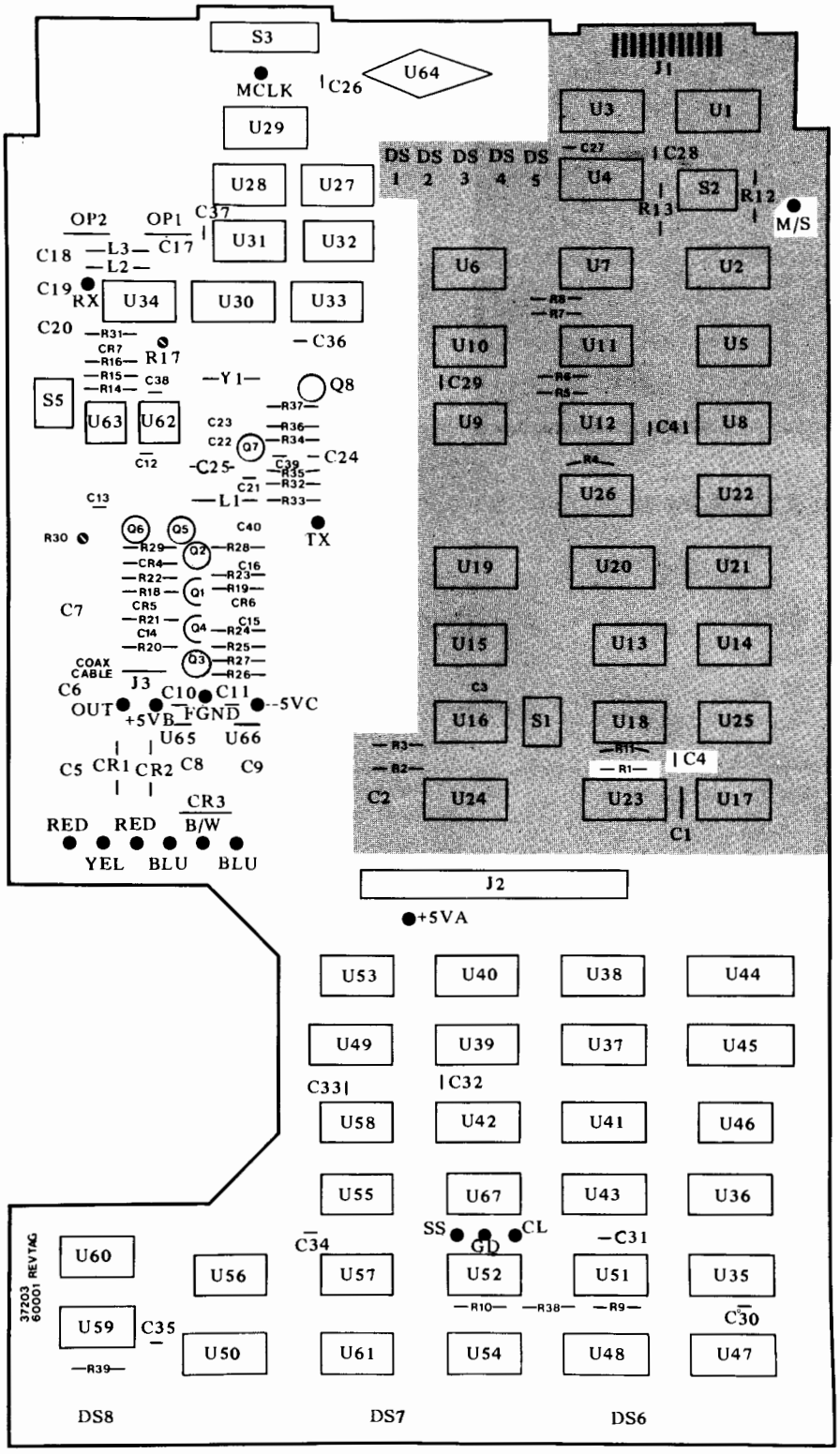


Figure A1-8 Component Location A1 Part 2

SERVICE SHEET A1
PART 3 – CONTROL LOGIC

A1-19 TROUBLESHOOTING

A1-20 INTRODUCTION

A1-21 When troubleshooting the Control Logic the 37203A should be configured as a MASTER, the Serial Data Rate switch set to NORMAL and A1TL1 set to the RUN position.

Check 1 – 24MHz Oscillator

Use the oscilloscope to compare the waveform at Test Point MCLK with Figure A1-10. The Serial Data Rate switch, on the rear panel, should be set to NORMAL. The voltage at Q7 emitter is +1.26V and at Q8 emitter is +2.75V.

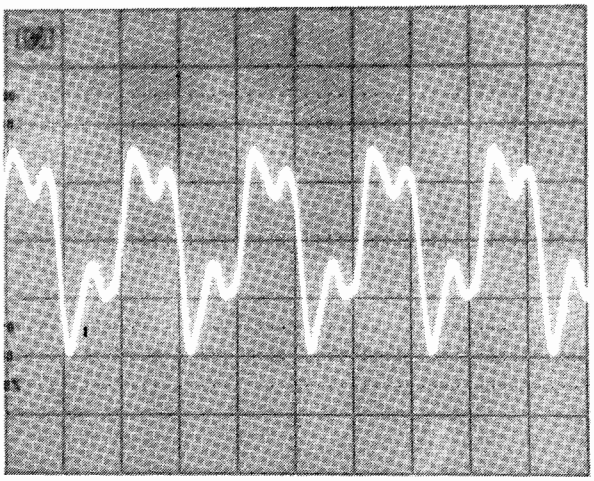


Figure A1-10 24MHz Oscillator Waveform

Check 2 – Frequency Divider

Connect the frequency counter to Test Point MCLK and verify that the frequency is 6MHz with the Serial Data Rate switch, on rear panel, set to ¼ and 1.5MHz with the Serial Data Rate switch set to 1/16. Reset the Serial Data Rate switch to NORMAL.

Check 3 – ASM 'A' Burst Clock

Use the oscilloscope to compare the waveform at Test Point CLOCK with Figure A1-11.

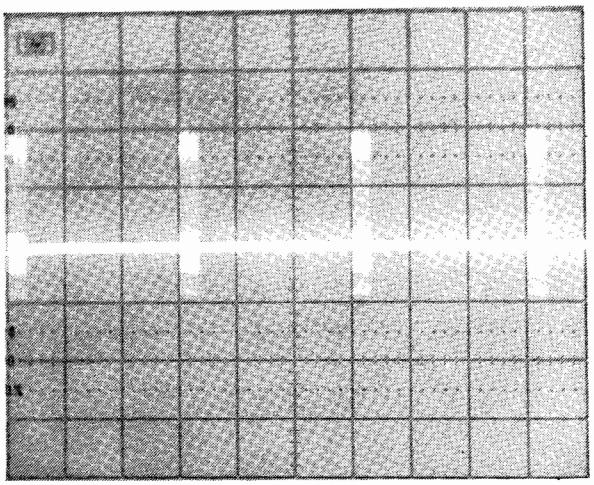


Figure A1-11 ASM 'A' Burst Clock Waveform

Check 4 – Algorithmic State Machine 'A'

Connect the three outputs X, Y, Z to the four channel oscilloscope with triggering from Test Point MCLK. ASM 'A' should be observed looping round state 3, state 4 and state 5, see Figure A1-12 and Table A1-8.

Table A1-8 ASM 'A' States

State	X U30(7)	Y U30(10)	Z U30(15)
1	0	0	0
2	0	1	0
3	1	0	0
4	0	1	1
5	0	0	1

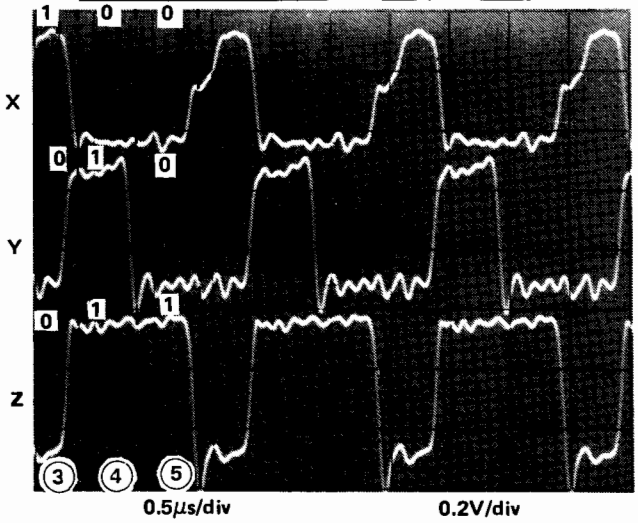


Figure A1-12 ASM 'A'

Check 5 – ASM 'B' Signature Analysis

Ensure that the 37203A is not connected to any other device and the switches are set as shown in Table A1-9.

Table A1-9 Switch Settings

Switch	Setting
A1S1	RUN
A1S2	OFF (ALL 6)
A1S3	NORMAL
A1S4	MASTER
A1S5	COAX
A1TL1	TEST

An HP5004A Signature Analysis is required and should be connected as follows:

CLOCK probe. . . . . .Test Point CL
START probe. . . . . .Test Point SS
STOP probe . . . . . .Test Point SS
GROUND probe . . . . . .Test Point GD
Logic probe ground . . . . . .Test Point GD

Set the S.A. controls as follows:

LINE switch. . . . . .IN
START switch . . . . . .IN
STOP switch. . . . . .IN
CLOCK switch . . . . . .IN
HOLD switch . . . . . OUT
SELF TEST switch . . . . . .OUT

Note: Before taking signatures, switch the 37203A power OFF for approximately 5 seconds then ON to provide a reset.

Check +5V signature is A5C1 and 0V signature is 0000.

Check the signatures on ASM 'B' with the signatures in Table A1-10. Correct signatures indicate the ASM 'A', ASM 'B', ASM 'D' appear to be operational. If a signature is faulty, proceed to check 6.

Table A1-10 ASM 'B' SA Test Signatures

Monitor Point	Signature
U49(6)	U352
U49(7)	56P3
U49(15)	A435
U49(14)	0184
U49(11)	4FU5
U55(3)	8092
U56(11)	P861
U57(16)	27AP
U60(6)	FH42

Check 6 – Algorithmic State Machine 'B'

Connect the three outputs J, K, L to the four channel oscilloscope with triggering from Test Point CLOCK. ASM 'B' should be observed going through states 6, 9, 9a, 10, 11, see Figure A1-14 and Table A1-11. The test board A1TL1 should be in the RUN mode. Switch the power OFF for approximately 5 seconds then ON prior to carrying out this check.

Table A1-11 ASM 'B' States

State	J U49(15)	K U49(10)	L U49(7)	Register Mode	S_1 U56(11)	S_0 U49(6)
6	0	0	0	Right Shift	0	1
7	0	1	1	Do Nothing	0	0
8	0	1	0	Load	1	1
9	1	0	0	Right Shift	0	1
9a	1	0	1	Do Nothing	0	0
10	1	1	0	Load	1	1
11	1	1	1	Do Nothing	0	0

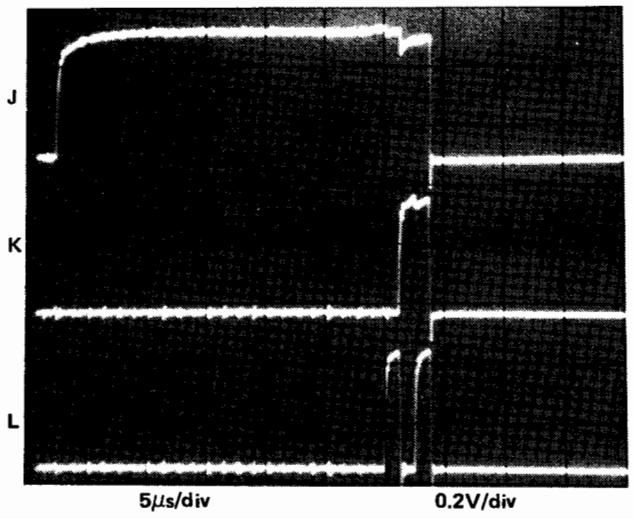


Figure A1-13 ASM 'B'

Check 7 – Transmit Wait Counter

Use the oscilloscope to verify that the *Wait Complete* signal, U29(9), is a +5V pulse with a period of approximately 30μs.

Check 8 – Frame Bit Counter

Use the oscilloscope to verify that the *Frame Count* signal, U48(12) is a high pulse with a period of 30μs. With the MASTER/SLAVE switch, on the rear panel, set to SLAVE the observed waveform should be continuously low. Reset the MASTER/SLAVE switch to MASTER.

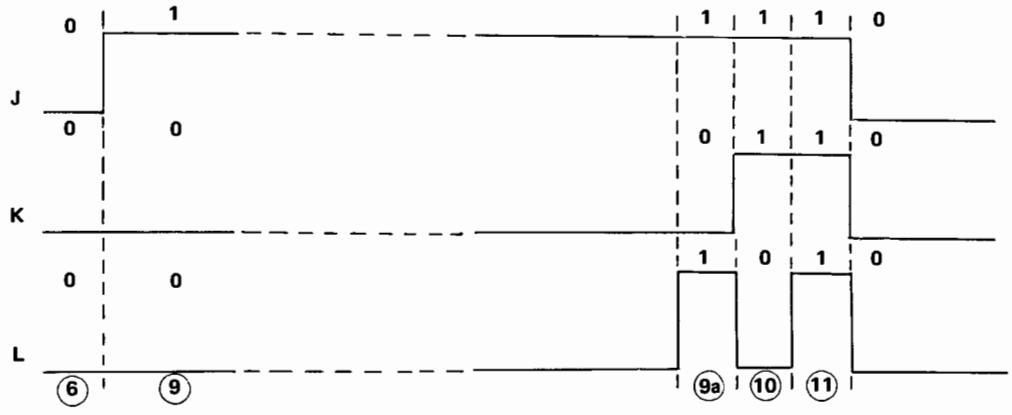


Figure A1-14 Expanded ASM 'B' Waveform

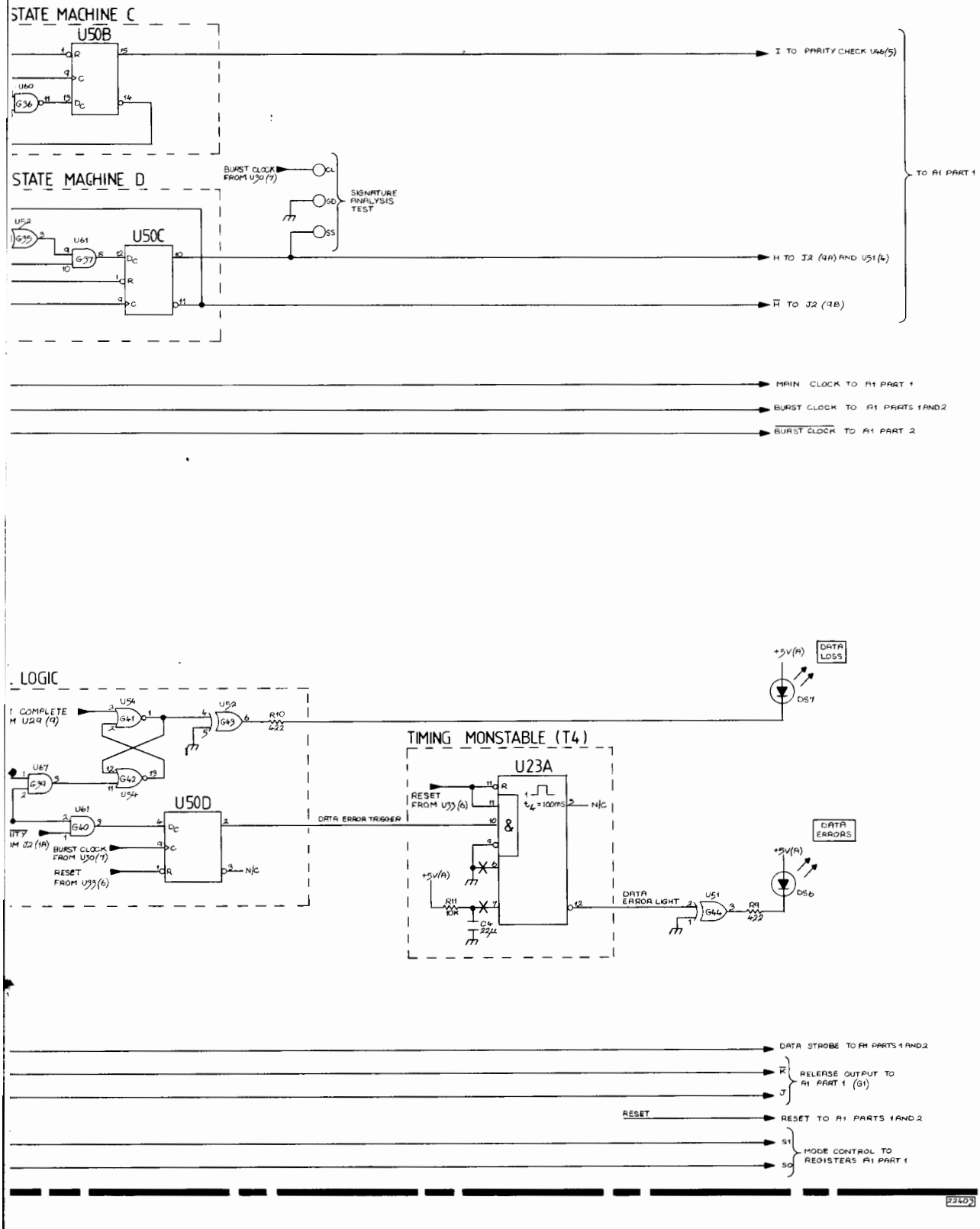
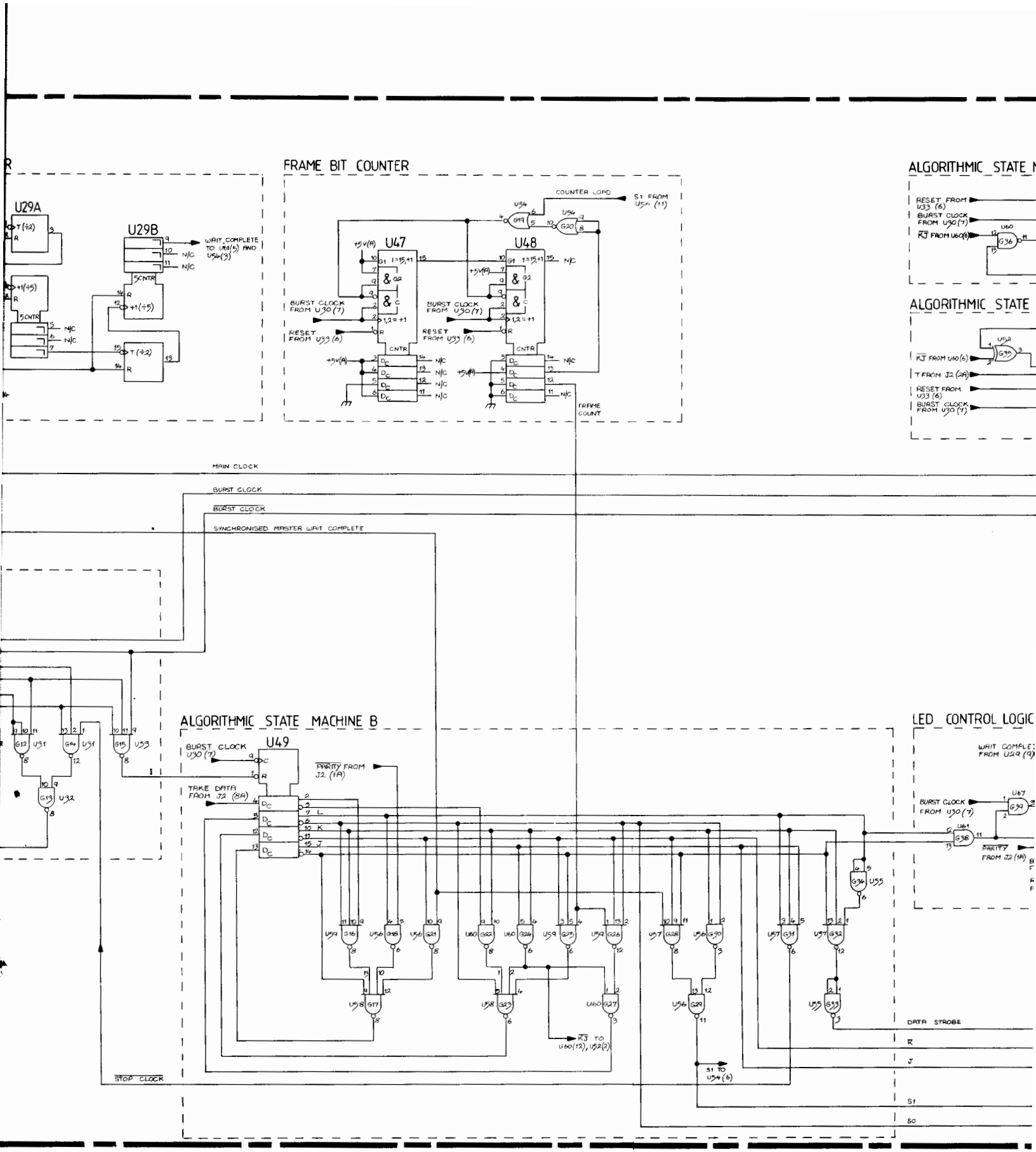
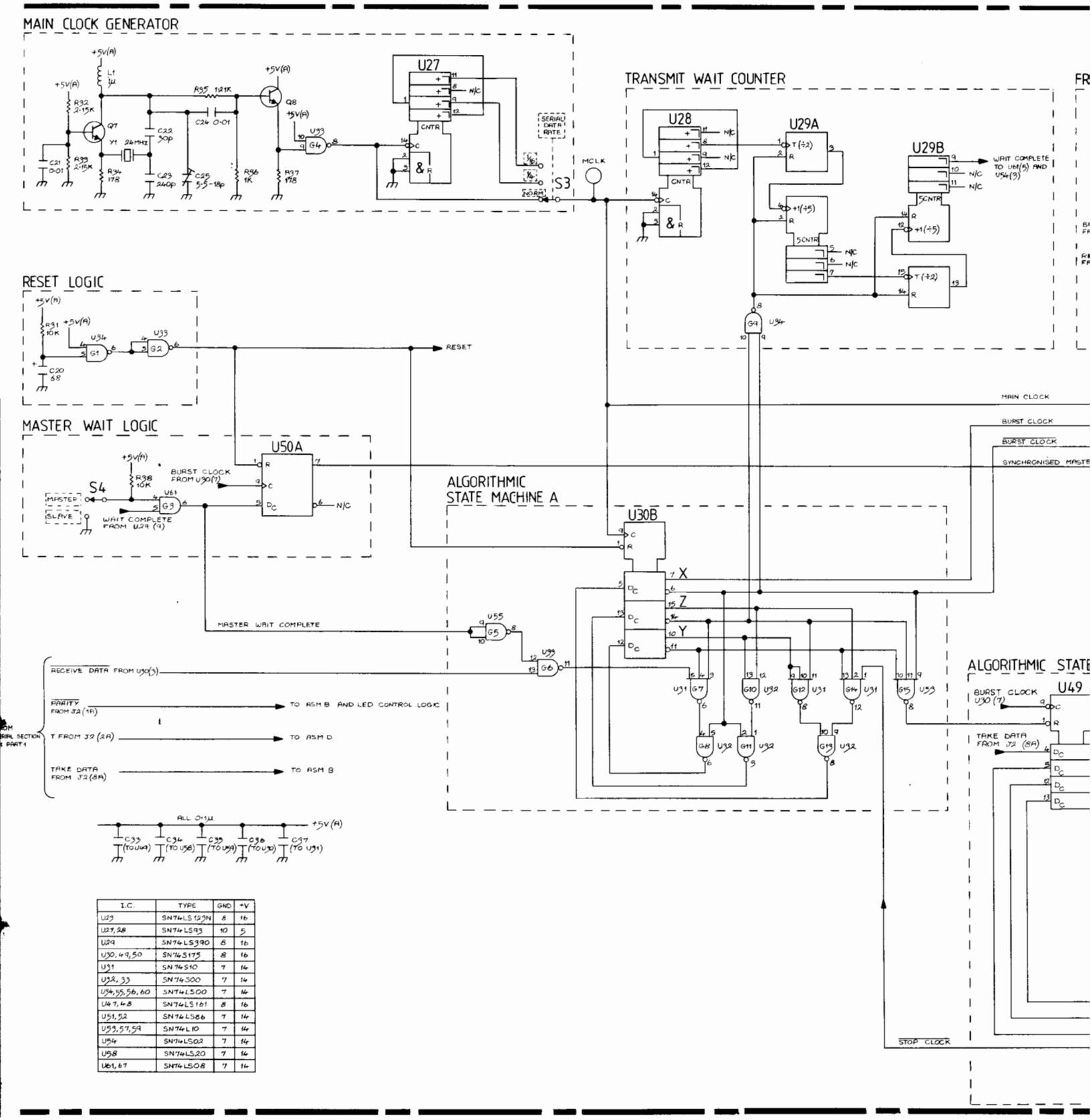


Figure A1-16 Schematic Diagram A1 Part 3


FRAME BIT COUNTER
ALGORITHMIC STATE
U29A
U29B
WAIT COMPLETE TO U41(5) AND U54(3)
5 CNTR
U47
U48
COUNTER LOAD
S1 FROM U54 (11)
BURST CLOCK FROM U30 (7)
RESET FROM U33 (6)
CNTR
FRAME COUNT
RESET FROM U33 (6)
BURST CLOCK FROM U30 (7)
KJ FROM U60(6)
T FROM J2 (2A)
MAIN CLOCK
BURST CLOCK
BURST CLOCK
SYNCHRONISED MASTER WAIT COMPLETE
ALGORITHMIC STATE MACHINE B
LED CONTROL LOGIC
U49
TAKE DATA FROM J2 (8A)
PARITY FROM J2 (1A)
STOP CLOCK
KJ TO U60(12), U52(2)
S1 TO U54(6)
DATA STROBE
R
J
S1
SO



I.C.	TYPE	GND	+V
U29	SN74LS129N	8	16
U27, 28	SN74LS93	10	5
U29	SN74LS390	8	16
U30, 49, 50	SN74S175	8	16
U31	SN74S10	7	14
U32, 33	SN74S00	7	14
U34, 55, 56, 60	SN74LS00	7	14
U47, 48	SN74LS161	8	16
U51, 52	SN74LS86	7	14
U53, 57, 59	SN74L10	7	14
U54	SN74LS02	7	14
U58	SN74LS20	7	14
U61, 67	SN74LS08	7	14

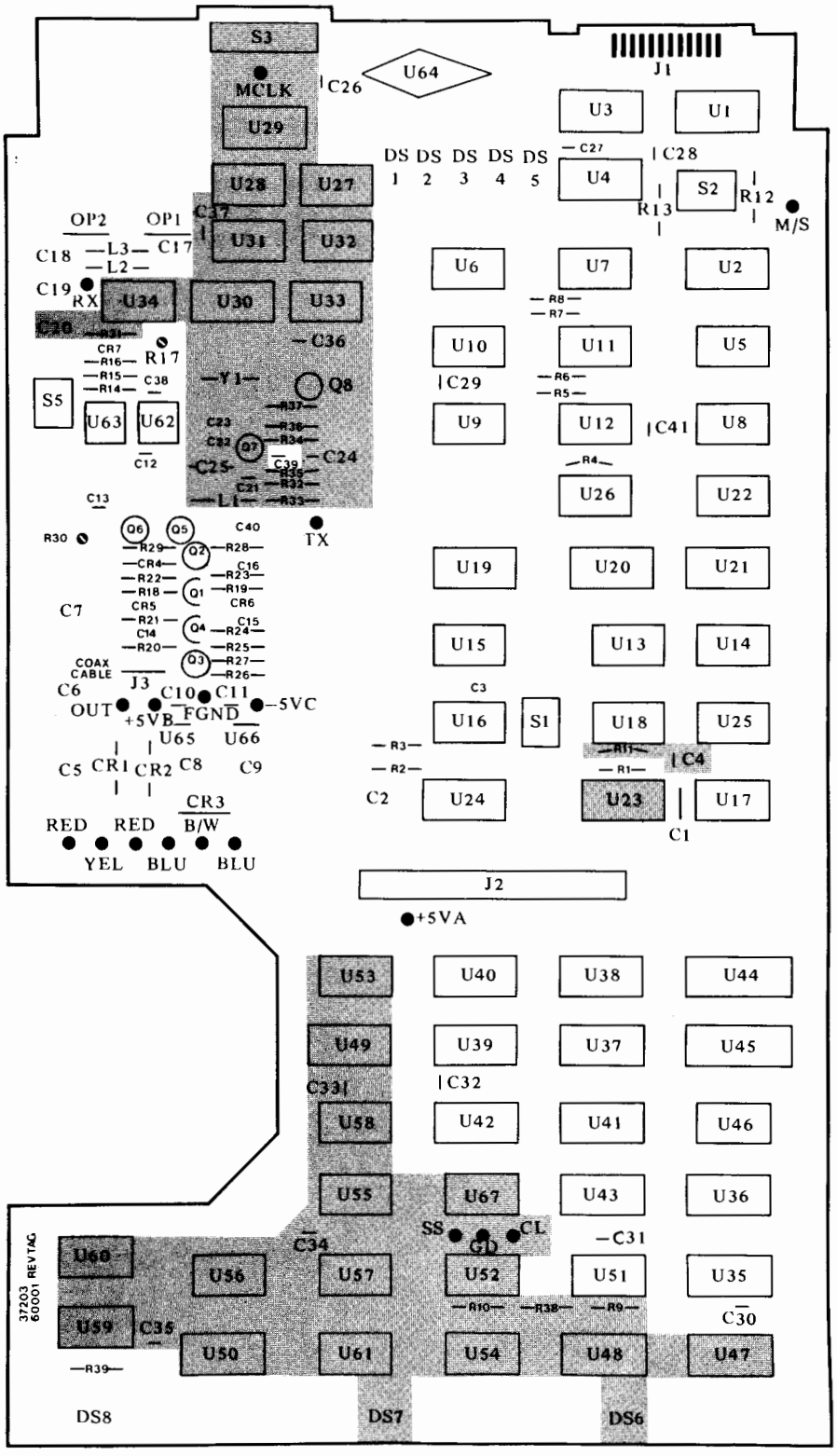


Figure A1-15 Component Location A1 Part 3

SERVICE SHEET A1
PART 4 – POWER SUPPLY

A1-22 INTRODUCTION

A1-23 The +5V(A), +5V(B) and −5V(C) are provided by conventional series regulator integrated circuits.

A1-24 DESCRIPTION

A1-25 The +5V(B) and −5V(C) supplies use a floating ground as a reference. The floating ground is limited by varistor RV1 to approximately ±24V.

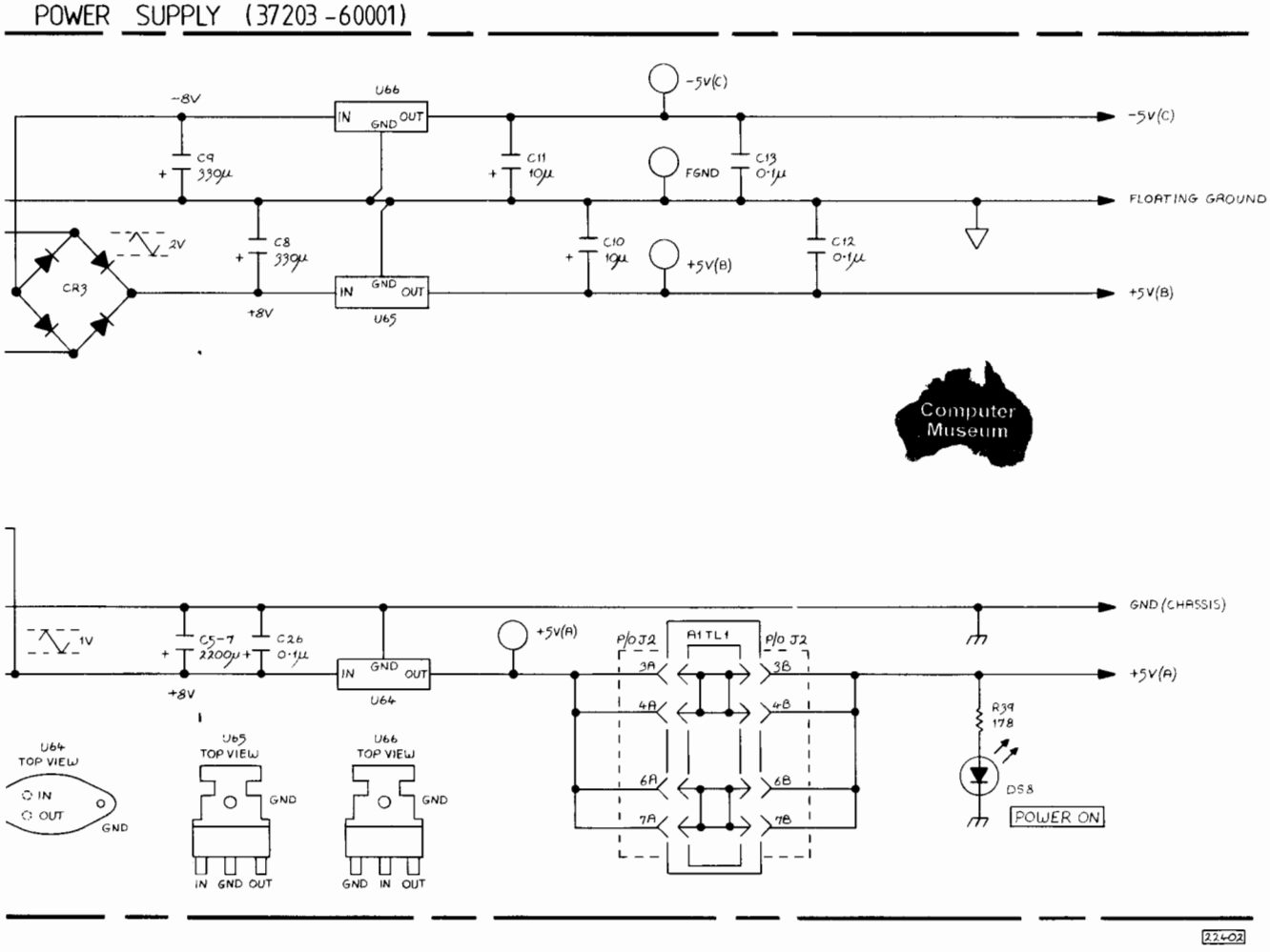
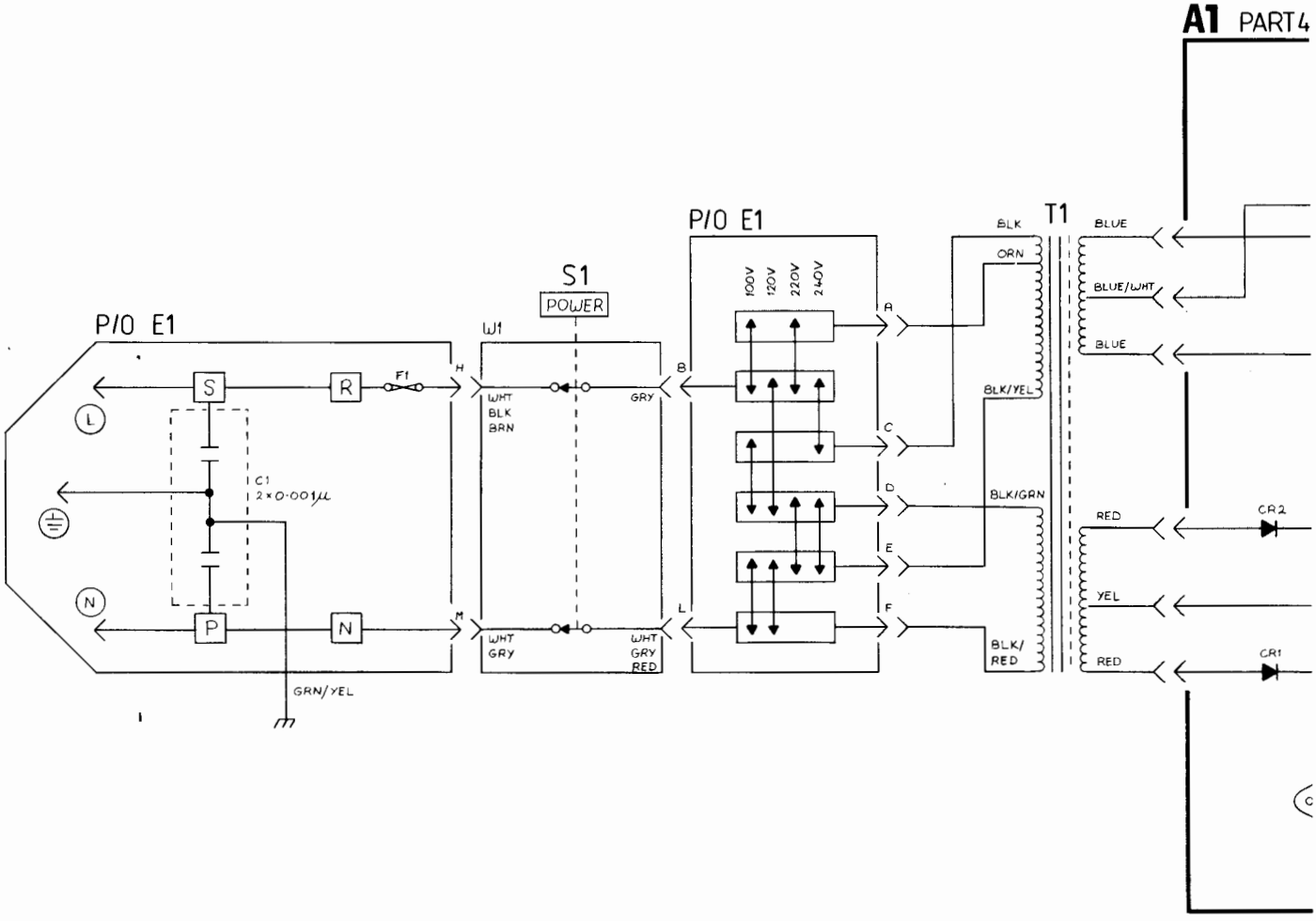


Figure A1-18 Schematic Diagram A1 Part 4


A1 PART 4
P/O E1
S1
POWER
W1
P/O E1
T1
S
R
F1
H
WHT
BLK
BRN
GRY
B
L
C1
2×0·001μ
N
P
N
M
WHT
GRY
WHT
GRY
RED
GRN/YEL
100V
120V
220V
240V
A
C
D
E
F
BLK
ORN
BLK/YEL
BLK/GRN
BLK/
RED
BLUE
BLUE/WHT
BLUE
RED
CR2
YEL
RED
CR1

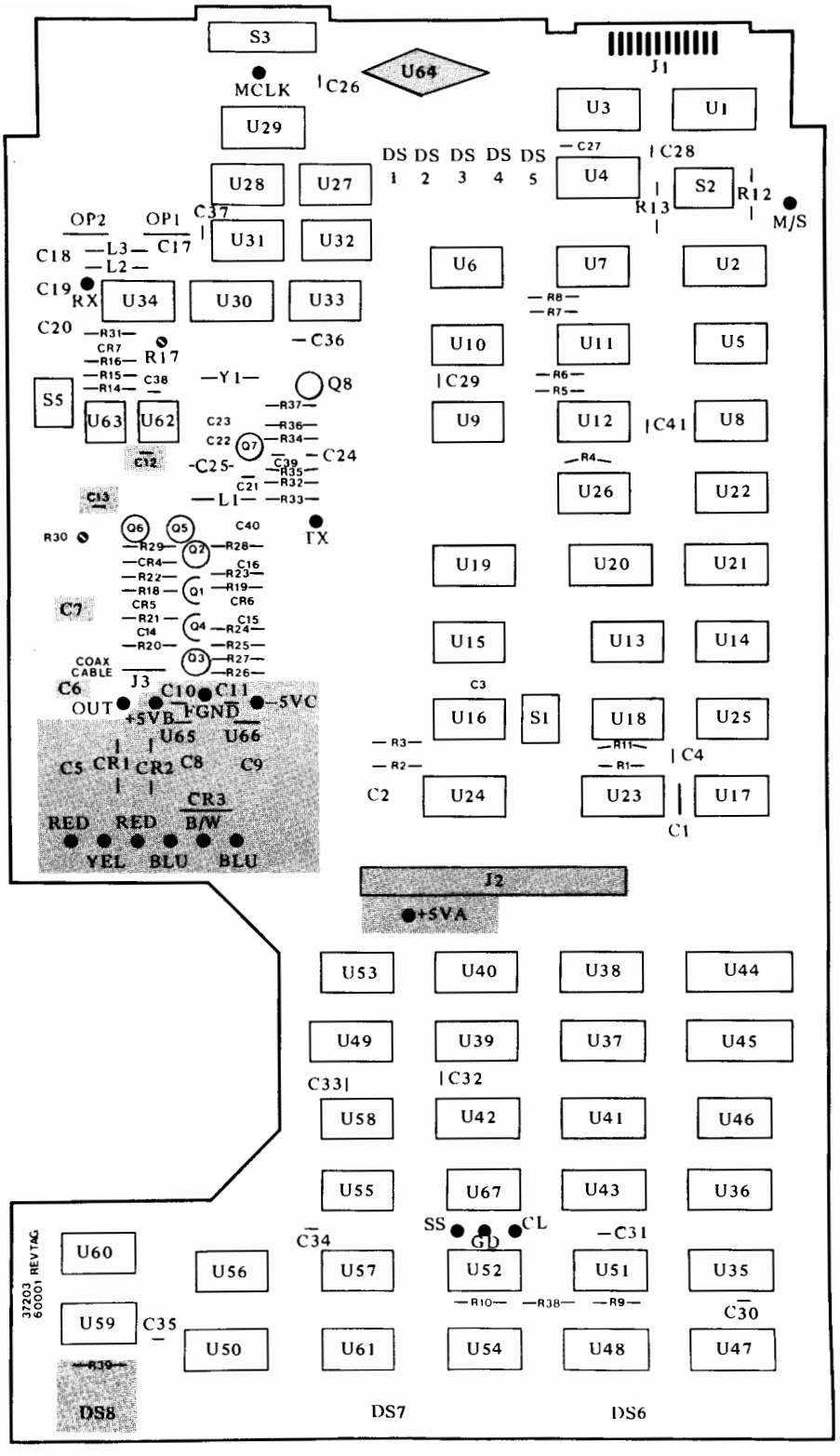


Figure A1-17 Component Location A1 Part 4