

CODE SEGMENT TABLE

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A		M		R		T		LENGTH							
RESERVED												PB BANK			
ADDRESS															

- A Absence bit (= 1 if segment is absent)
- M Mode bit (= 1 if privileged mode)
- R Reference bit (for statistical use by operating system, set to 1 when accessed)
- T Trace bit (= 1 to call Trace routine)
- LENGTH This value times 4 (max = 16,380)
- ADDRESS Absolute memory address (for PB) or low order 16 bits of absolute disc address if absent.

PB BANK Bank Number if present of High Order Disc Address if absent.

SEGMENT TRANSFER TABLE Words

STT Length															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	U	0	0	0	0	0	0	0	0	0	0	0	0	0	0
												LENGTH			

U Uncallable bit
 LENGTH Maximum = 255 (Calls from external segments may reference only the first 128 entries, PL thru PL-127.)

Local Program Label

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	U	ADDRESS													

U Uncallable bit
 ADDRESS PB relative, + only

External Program Label

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	STT #											SEG #			

STT # = STT = entry number in target segment, maximum = 127
 SEG # = Target segment

INTERRUPTS/TRAPS

STT Entry Number	Interrupt	Parameter
1	EXTERNAL INTERRUPT	DEV #
2	BOUNDS VIOLATION	100401
3	ILLEGAL MEMORY ADDRESS	101001
4	NON-RESPONDING MODULE	101401
5	SYSTEM PARITY ERROR	102001
6	ADDRESS PARITY ERROR	102401
7	DATA PARITY ERROR	103001
	MODULE INTERRUPT	MODULE #
11	POWER FAIL	104401
20	UNIMPLEMENTED INSTRUCTION	110001
21	STT VIOLATION	110401
22	CST VIOLATION	111001
23	DST VIOLATION	111401
24	STACK UNDERFLOW	112001
25	PRIVILEGED MODE VIOLATION	112401
30	STACK OVERFLOW	114001
31	USER TRAPS	114401
	INTEGER OVERFLOW	1
	FLOATING-POINT OVERFLOW	2
	FLOATING-POINT UNDERFLOW	3
	INTEGER DIVIDE BY 0	4
	FLOATING-POINT DIVIDE BY 0	5
	EXT. PRECISION OVERFLOW	10
	EXT. PRECISION UNDERFLOW	11
	EXT. PRECISION DIVIDE BY 0	12
	DECIMAL OVERFLOW	13
	INVALID ASCII DIGIT	14
	INVALID DECIMAL DIGIT	15
	INVALID SOURCE WORD COUNT	16
	RESULT WORD COUNT OVERFLOW	17
	DECIMAL DIVIDE BY 0	20
37	ABSENT CODE SEGMENT	P-LABEL
	PCAL	N
	EXIT	0
	IXIT	0
40	TRACE	P-LABEL
	PCAL	N
	EXIT	0
	IXIT	0
41	STT ENTRY UNCALLABLE	P-LABEL
42	ABSENT DATA SEGMENT	DST #
43	POWER ON	121401
44	COLD LOAD	
	START I/O (SIO)	0
	DIRECT I/O (DIO)	122001

NOTE: If parameter not shown, parameter is external program label.

Instructions

00 STACK OPS

0	1	3	4	6	7	9	10	12	13	15
0	0									

1st POSITION		2nd POSITION	
C	O	C	C

C	O	C	C	00	NOP				40	DEL
A	X	X		01	DELB				41	ZROB
A	X	X	A	02	DDEL	A			42	LDXB
A	X	X	A	03	ZROX	A			43	STAX
A	X	X	A	04	INCX	A			44	LDXA
A	X	X	A	05	DECX	A			45	DUP
A	X	X	A	06	ZERO	A			46	DDUP
A	X	X	A	07	DZRO	A			47	FLOT
C			C	10	DCMP	C			50	FCMP
A	X	X	A	11	DADD	A	X		51	FADD
A	X	X	A	12	DSUB	A	X		52	FSUB
A	CI	X	A	13	MPYL	A	X		53	FMPY
A	X	X	A	14	DIVL	A	X		54	FDIV
A	X	X	A	15	DNEG	A			55	FNEG
A	X	X	A	16	DXCH	A			56	CAB
C			C	17	CMP	C			57	LCMP
A	X	X	A	20	ADD	A	X		60	LADD
A	X	X	A	21	SUB	A	X		61	LSUB
A	X	X	A	22	MPY	A	X		62	LMPY
A	X	X	A	23	DIV	A	X		63	LDIV
A	X	X	A	24	NEG	A			64	NOT
A			A	25	TEST	A			65	OR
A			A	26	STBX	A			66	XOR
A	X	X	A	27	DTST	A			67	AND
A			A	30	DFLT	A	X		70	FIXR
B			A	31	BTST	A	X		71	FIXT
A			A	32	XCH				72	SPARE
A	X	X	A	33	INCA	A	X		73	INCB
A	X	X	A	34	DECA	A	X		74	DECB
A	X	X	A	35	XAX				75	XBX
A	X	X	A	36	ADAX	A	X		76	ADBX
A	X	X	A	37	ADXA	A	X		77	ADXB

CC = condition, O = overflow, C = carry, CI = clears bit

01 SHIFTS/BRANCHES

0	1	3	4	6	7	9	10	12	13	15
0	1									

A			X	0	0				SC	ASL
A			X	0	1				SC	ASR
A			X	0	2				SC	LSL
A			X	0	3				SC	LSR
A			X	0	4				SC	CSL
A			X	0	5				SC	CSR
A			X	0	6	0			SCAN	
A	X	X	1	0	7	+/-			P branch	IABZ
A			X	0	1	0			SC	TASL
A			X	0	1	1			SC	TASR
A	X	X	1	0	2	+/-			P branch	IXBZ
A	X	X	1	0	3	+/-			P branch	DXBZ
CI			1	0	4	+/-			P branch	BCY
CI			1	0	5	+/-			P branch	BNCY
A			X	0	1	6	0		TNSL	
A			1	7					SC	OASL(X)
A			X	1	0	0			SC	OASR(X)
A			X	1	0	0			SC	DASL
A			X	1	0	1			SC	DASR
A			X	1	0	2			SC	DLSL
A			X	1	0	3			SC	DLSR
A			X	1	0	4			SC	DCSL
A			X	1	0	5			SC	DCSR
A			1	1	0	6	+/-		P branch	CPRB\$
A	X	X	1	1	0	7	+/-		P branch	DABZ
CI			1	1	1	0	+/-		P branch	BOV
CI			1	1	1	1	+/-		P branch	BNOV
..			X	1	1	2			bit position	TBC
..			X	1	1	3			bit position	TRBC
..			X	1	1	4			bit position	TSBC
..			X	1	1	5			bit position	TCBC
..			1	1	1	6	+/-		P branch	BRO
..			1	1	1	7	+/-		P branch	BRE

CI = clears bit
 \$ = uses Index Reg.
 .. bit = 0 CCE, bit = 1 CCG or CCL
 SC = shift count (0 - 63)
 P branch signed magnitude (0 - 31)
 bit position (0 - 63) [MOD 16]
 CPRB X < (S-1) CCL X > (S) CCG (S-1) < X ≤ (S) CCE

02 MOVES/IMMEDIATES

0	1	3	4	6	7	9	10	12	13	15
0	2									

			0	0	0	0	0	0	PB	DB 0	SDEC	MOVE	
			0	0	0	0	0	0	1	PB	DB 0	SDEC	MVB
			0	0	1	0						SDEC	MVBL
			0	0	1	1						SDEC	MABS
B			0	0	1	2						SDEC	SCW
			0	0	1	3						SDEC	MTDS
			0	0	1	4						SDEC	MVLB
			0	0	1	5						SDEC	MDS
			0	0	1	6						SDEC	SCU
			0	0	1	7						SDEC	MFDS
B			0	0	2	0	N	A			U	SDEC	MVBW
C			0	0	2	1	PB	DB 0				SDEC	CMPB
A			0	0	3	0	0				0	RSW	
A			0	0	3	0	0				1	LLSH\$	
A			0	0	3	2	2				0	PLDA\$	
A			0	0	3	2	1				1	PSTA\$	
A			0	0	3	4	0				0	LSEA	
A			0	0	3	4	1				1	SSEA	
			0	0	3	4	2				2	LDEA	
			0	0	3	4	3				3	SDEA	
			0	0	3	6	0				0	IXIT	
			0	0	3	6	1				1	Reserved	
			0	0	3	6	2				2	PCN	
			0	0	3	6	3				3	Reserved	
A	X		0	0	4	1	0				0	EADD	
A	X		0	0	4	1	1				1	ESUB	
A	X		0	0	4	1	2				2	EMPY	
A	X		0	0	4	1	3				3	EDIV	
A			0	0	4	1	4				4	ENEG	
C			0	0	4	1	5				5	ECMP	
			0	0	5	7	0				0	DMUL	
			0	0	5	7	1				1	DDIV	
A	X		0	0	6	0	0				0	DMPY	

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02 MOVES/IMMEDIATES (cont.)

0	1	3	4	6	7	9	10	12	13	15	
...	

A X		0	6	0	0	2	CVAD					
A X		0	6	0	0	3	CVDA					
A X		0	6	0	4	CVBD						
A X		0	6	0	5	CVDB						
A X	X	0	6	0	6	SLD						
A X	X	0	6	0	7	NSLD						
A X	X	0	6	1	0	SRD						
A X	X	0	6	1	1	ADDD						
C X	X	0	6	1	2	CMPD.						
A X	X	0	6	1	3	SUBD						
A X	X	0	6	1	4	MPYD						
A		1	0	←	Imm Opr	→	LDI					
A		1	1	←	Imm Opr	→	LDXI					
C		2	0	←	Imm Opr	→	CMPI					
A X	X	2	1	←	Imm Opr	→	ADDI					
A X	X	3	0	←	Imm Opr	→	SUBI					
A X	X	3	1	←	Imm Opr	→	MPYI					
A		4	0	←	Imm Opr	→	DIVI					
A		4	1	SBK	DB DL Z STA X QS	PSHR	↑					
A		5	0	←	Imm Opr	→	LDNI					
A		5	1	←	Imm Opr	→	LDXN					
C		6	0	←	Imm Opr	→	CMPN					
A		6	1 J J	J J K	K K K	EXF						
A		7	0 J J	J J K	K K K	DPF						
C		7	1 SBK	DB DL Z STA X QS	SETR							

§ = uses Index Register
 SDEC pop stack (0 - 3)
 Imm Opr Immediate operand (0 - 255)
 JJJ Beginning bit position (0 - 15)
 KKKK field length (0 - 15)
 * SCW CARRY → Terminating character
 * SCU CARRY → Terminating character

03 I/O LINKAGE CONTROL

0	1	3	4	6	7	9	10	12	13	15	
...	

		0	0	0	0	0	K K K	K K K	LST			
		0	0	0	1	0	n n n	n n n	PAUS			
		0	0	1	0	0	0	0	D/ESD			
3		0	0	0	6	0	XCHD					
		0	0	6	6	1	PSDB					
		0	0	6	6	2	DISP					
		0	0	6	6	3	PSEB					
3		0	1	0	0	0	SMSK					
		0	1	0	0	1	SCLK					
		0	1	2	0	0	RMSK					
		0	1	2	1	1	RCLK					
*		0	1	1	0	K K K	XEQ					
D		0	1	1	1	K K K	SIO					
D		0	2	0	0	K K K	RIO					
D		0	2	0	1	K K K	WIO					
1		0	2	1	0	K K K	TIO					
1		0	2	1	1	K K K	CIO					
		0	3	0	0	K K K	CMD					
		0	3	0	1	K K K	SST					
1		0	3	1	0	K K K	SIN					
		0	3	1	1	n n n	HALT					
		0	1	←	SST	→	SCAL					
		1	0	←	SST	→	PCAL					
		1	1	←	SDEC + (4)	→	EXIT					
		2	0	←	SDEC + (1)	→	SXIT					
A		2	1	←	Imm Opr	→	ADXI					
A		3	0	←	Imm Opr	→	SBXI					
		3	1	←	PL - Disp	→	LLBL					
		4	0	←	P - Disp	→	LDPP					
		4	1	←	P - Disp	→	LDPN					
		5	0	←	Imm Opr	→	ADDS					
		5	1	←	Imm Opr	→	SUBS					
		6	0	0	0	0	SPARE					
A		6	1	←	Imm Opr	→	ORI					
A		7	0	←	Imm Opr	→	XORI					
A		7	1	←	Imm Opr	→	ANDI					
C	O	C										

KKKK Stack displacement (0 - 15)
 Imm Opr Immediate operand (0 - 255)
 STT entry position (0 - 255)
 n Not used.
 1. normally CCE, non-responding CCL
 D norm CCE, non-respond CCL, not ready CCG
 3. norm CCE, IF error CCL

MEMORY REFERENCE

0	1	3	4	6	7	9	10	12	13	15	
...	

A		X	1	0	←	P	→					
A		X	1	1	←	DOS	→					
		0	5	0	+/-	P rel branch	→	TBA				
		2	+/-	P rel branch	→	MTBA						
		4	+/-	P rel branch	→	TBX						
		6	+/-	P rel branch	→	MTBX						
		X	1	1	←	DOS	→	STOR				
C		0	6	X	1	0	←	P	→	CMPM		
C		X	1	1	←	DOS	→					
A	X	X	0	7	X	1	0	←	P	→	ADDM	
A	X	X	1	0	←	DOS	→					
A	X	X	1	0	←	P	→	SUBM				
A	X	X	1	1	←	DOS	→					
A	X	X	1	1	←	DOS	→					
A	X	X	1	1	←	P	→	MPYM				
A	X	X	1	1	←	DOS	→					
A	X	X	1	2	X	1	0	←	DOS	→	INCM	
A	X	X	1	1	←	DOS	→					
A	X	X	1	1	←	DOS	→					
A	X	X	1	3	X	1	0	←	P	→	LDX	
A		X	1	1	←	DOS	→					
A		X	1	0	+/-	P rel branch	→	BR				
X	1	1	←	DOS indirect	→	BR						
I	0	1	GEL	+/-	P branch	BCC						
B		1	5	X	1	0	←	DOS	→	LDB		
A		X	1	1	←	DOS	→	LDD				
		1	6	X	1	0	←	DOS	→	STB		
		X	1	1	←	DOS	→	STD				
		X	1	0	←	DOS	→	LRA				
		X	1	1	←	DOS	→					

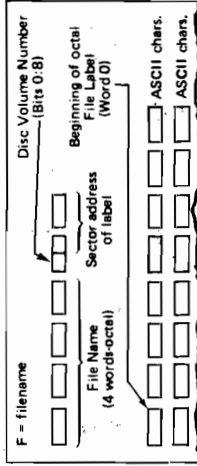
7 8 9 10 - 1213 - 15
 P P+ 0 0:377
 P- 1 0:377
 DB+ 0 0:377
 Q+ 1 0 0:177
 DOS 0- 1 1 0 0:77
 S- 1 1 1 0:77

GEL { 1. Less than (BL)
 2. Equal (BE)
 3. Less than or equal (BLE)
 4. Greater than (BG)
 5. Not equal (BNE)
 6. Greater or equal (BGE)



FILE LABELS

Format of LISTF-1 Listing

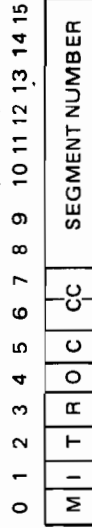


Words Dec.	Contents
0-3	Local file name.
4-7	Group name.
8-11	Account name.
12-15	Identity of file creator.
16-19	File lockword.
20-21	File security matrix.
24-25	(Bits 0:15) Not used.
26	(Bit 15:1) File secure bit: If 1, file secured. If 0, file released.
27	File creation date
28	Last access date.
29	Last modification date.
30	File code.
31	File control block vector.
32	File control block vector.
33	Store Bit. (If on, :STORE or :RESTORE, in progress.)
34	Restore Bit. (If on, :RESTORE in progress.)
35	Load Bit. (If on, program file is loaded.)
36	Exclusive Bit. (If on, file is opened with exclusive access.)
37	Device sub-type.
38	Device type.
39	File is open for write.
40	File is open for read.
41	Number of user labels written.
42	Number of user labels.
43	Maximum number of logical records.
44	Private Volume Information.
45	Checksum.
46	Cold-load identity.
47	Options specifications.
48	Logical record size (in negative bytes).
49	Block size (in words).
50	Sector offset to data.
51	Not used.
52	Number of extents minus 1.
53	Logical size of last block.
54	Extent size.
55	Number of logical records in file.
56	Two-word addresses of up to 32 disc extents, beginning with address of first extent (words 44-45).
57	Device Class.

ASCII

CHAR	BYTE POSITION		Dec.
	Left	Right	
A	040400	000101	65
B	041000	000102	66
C	041400	000103	67
D	042000	000104	68
E	042400	000105	69
F	043000	000106	70
G	043400	000107	71
H	044000	000110	72
I	044400	000111	73
J	045000	000112	74
K	045400	000113	75
L	046000	000114	76
M	046400	000115	77
N	047000	000116	78
O	047400	000117	79
P	050000	000120	80
Q	050400	000121	81
R	051000	000122	82
S	051400	000123	83
T	052000	000124	84
U	052400	000125	85
V	053000	000126	86
W	053400	000127	87
X	054000	000130	88
Y	054400	000131	89
Z	055000	000132	90
[055400	000133	91
\	056000	000134	92
^	056400	000135	93
_	057000	000136	94
`	057400	000137	95
{	060000	000140	96
a	060400	000141	97
b	061000	000142	98
c	061400	000143	99
d	062000	000144	100
e	062400	000145	101
f	063000	000146	102
g	063400	000147	103
h	064000	000150	104
i	064400	000151	105
j	065000	000152	106
k	065400	000153	107
l	066000	000154	108
m	066400	000155	109
n	067000	000157	110
o	067400	000158	111
p	070400	000160	112
q	070400	000161	113
r	071000	000162	114
s	071400	000163	115
t	072000	000164	116
u	072400	000165	117
v	073000	000166	118
w	073400	000167	119
x	074000	000170	120
y	074400	000171	121
z	075000	000172	122
{	075400	000173	123
	076000	000174	124
}	076400	000175	125
DEL	077000	000176	126
	077400	000177	127

STATUS REGISTER



M Mode User Privileged
 I Ext Interrupts Enabled
 T User Traps Enabled
 R Right Stack Op Pending
 O Overflow
 C Carry
 CC Condition Code
 CCL = 1
 CCE = 2
 DDG = 0

CONDITION CODES

CCA CCL Operand < 0
 CCE Operand = 0
 CCG Operand > 0

CCB CCL Special ASCII Char
 CCE Alphabetic
 CCG Numeric

CCC CCL Operand 1 < OPR 2
 CCE Operand 1 = OPR 2
 CCG Operand 1 > OPR 2

CCD CCL Non-responding device controller
 CCE Responding device controller, or device ready
 CCG Device not ready (busy)

STACK MARKER SPECIAL STACK MARKER
 (normal) (resulting from ICS interrupt)

X	INDEX
	Relative P
	P + 1 - PB
	STATUS
Q, S	ΔQ
	DB BANK
	S DB

X	INDEX
	Relative P
	P + 1 - PB
	STATUS
Q	ΔQ
	DB BANK
S	DB