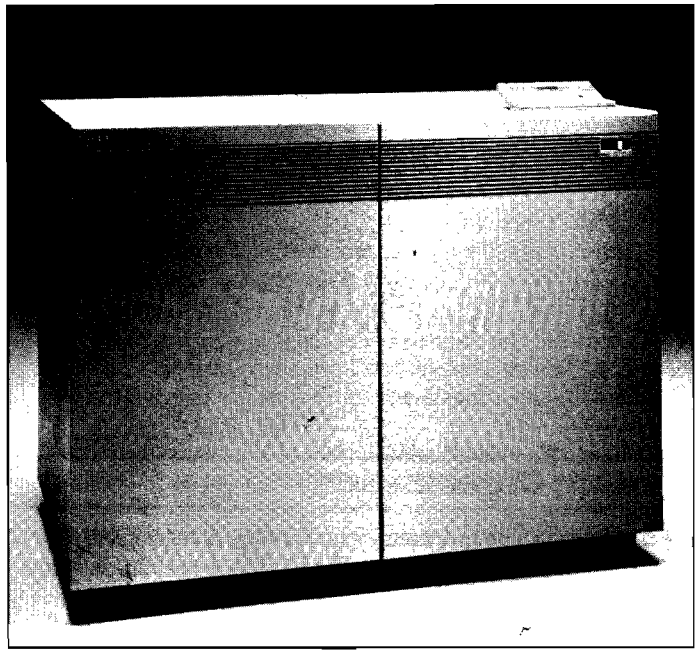
HEWLETT-PACKARD

HP 3000 Computer Systems

Series 950

Product Description

The Series 950 is the highest performance member of the broad family of HP 3000 business computers. By incorporating the latest in VLSI technology with HP Precision Architecture, the Series 950 delivers a highly reliable, cost effective solution to high-end data processing needs. As a member of the HP 3000 product line, the Series 950 builds on the strong reputation established by the HP 3000 over the past decade in the commercial data processing marketplace. To excel in large commercial applications, the Series 950 combines a high-speed CPU with an operating system specifically designed for commercial data processing — MPE XL. Add to this a tightly integrated network and relational database and the result is a system that provides high performance and functionality in multi-user, multi-tasking interactive and batch environments. Due to its powerful processor, the Series 950 also is very effective in computationally-intensive applications. Completing the Series 950 offering is a wide variety of financial, manufacturing, service industry and information management software to put the processing power of the Series 950 to work solving your data management challenges.



System Features

- 7 MIPS CPU performance
- Single chip VLSI CPU, single board processor
- HP Precision Architecture
- 73 nanosecond system clock cycle
- 48-bit virtual addressing
- 32 Mb main memory standard, expandable to 128 Mb
- 128 Kb high-speed CPU cache for data and instructions
- Floating Point Coprocessor standard
- Advanced instruction pipelining
- Battery backup, auto-restart standard
- Three-level I/O hierarchy providing high I/O bandwidth
- High-speed, 100 Mb/second, system memory bus
- IEEE 802.3 standard Local Area Network terminal connection
- MPE XL operating system
- Network and relational database management systems standard
- AdvanceNet networking solutions

Advanced Technologies

HP Precision Architecture

The Series 950 uses HP Precision Architecture (HPPA) to achieve high performance and reliability at a low cost. HPPA is based on the concept of Reduced Instruction Set Computing (RISC), a design approach which leads to greatly simplified computers that are optimized to provide the highest performance for a given integrated circuit (IC) technology. In addition to offering higher performance, the inherent simplicity of HPPA means lower cost and higher reliability because machines can be implemented with fewer components.

At the core of HPPA is an instruction set containing 140 carefully selected, fixed-format instructions. Because the instruction set is simple, instructions can be hardwired directly in the Central Processing Unit (CPU). This eliminates the need for microcode and the necessity to decode complex instructions. HPPA utilizes a Load/Store

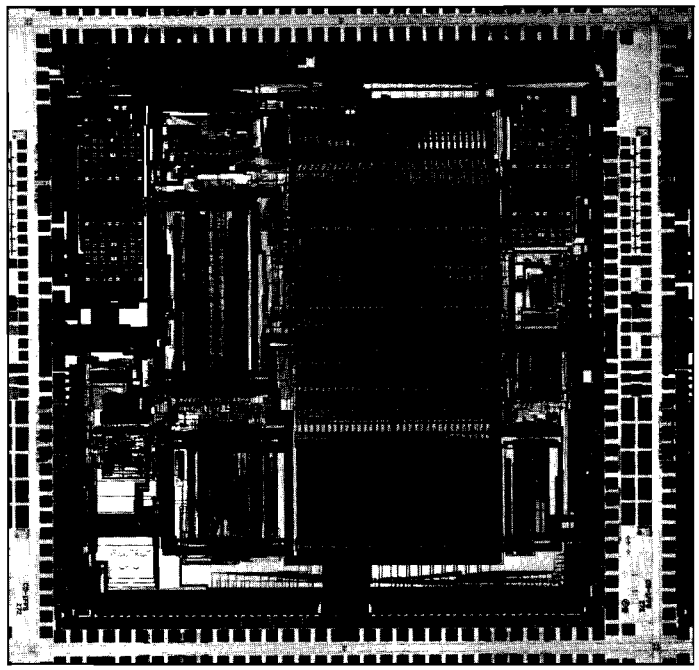
design to reduce the number of relatively slow memory accesses, as most operations are performed register-to-register. To further enhance performance, Optimizing Compilers are used to schedule instructions and manage the instruction pipeline. With hardwired control, a Load/Store design, and Optimizing Compilers, one instruction is executed with virtually every clock cycle. Single cycle execution provides much of the performance benefit of HPPA over traditional architectures.

HPPA also incorporates many other features unrelated to RISC which greatly enhance its functionality. For example:

- Support for coprocessors (i.e. Floating Point)
- Extended addressing
- Memory-mapped I/O subsystem

VLSI Technology

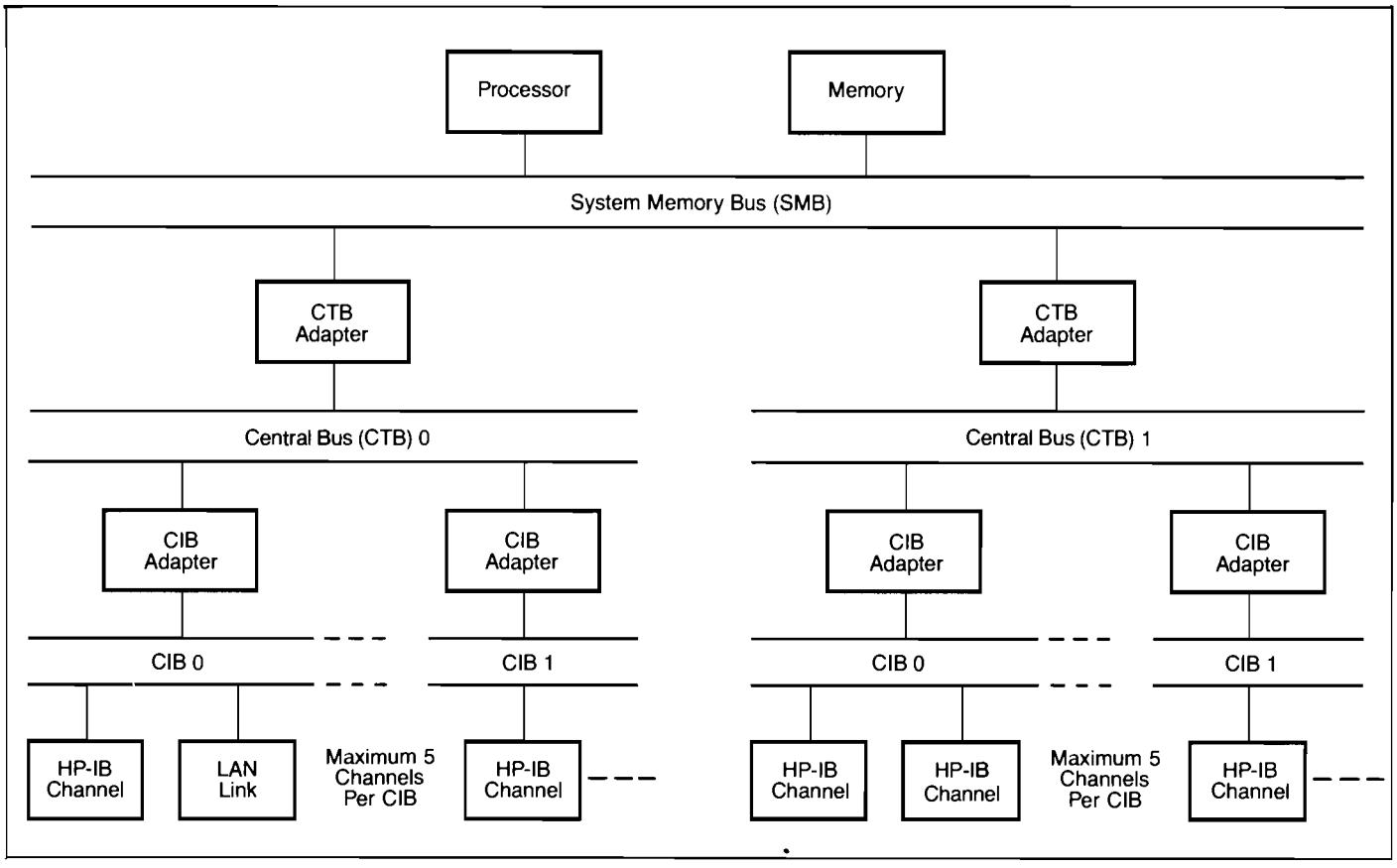
The Series 950 is implemented using HP's proprietary NMOS III, VLSI technology, allowing the entire Series 950 CPU to be put on a single 144 thousand-transistor chip. Furthermore, the entire processor, including a 128 Kb cache, 4 K-Entry Translation Lookaside Buffer (TLB) and the Floating Point Coprocessor, is on a single printed circuit board.



Series 950 CPU Chip

System Organization

The processor communicates with main memory via the System Memory Bus (SMB). The SMB is a very high-speed bus that provides a 64-bit data path and can support sustained data transfer rates of up to 100 Mb/second. The SMB connects to two Central Busses (CTBs) through separate CTB Adapters. Each CTB supports two Channel I/O Busses (CIBs) via separate CIB Adapters. The CIBs support I/O interfaces to peripheral devices and local area network (LAN) links.



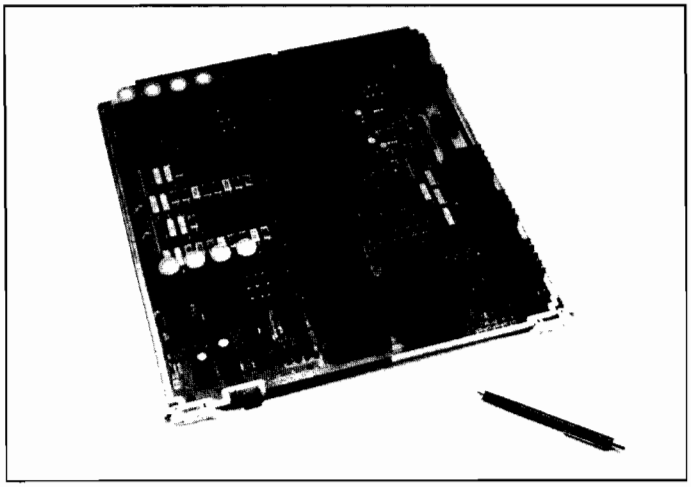
System Structure

HP Computer Museum
www.hpmuseum.net

For research and education purposes only.

The Series 950 Processor

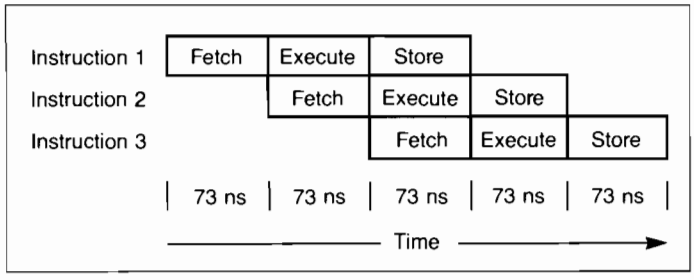
The entire Series 950 processor is contained on a single board implemented using HP's proprietary NMOS III, VLSI technology. The processor module consists of nine VLSI chips, including a Central Processor Unit (CPU), a Translation Lookaside Buffer Control Unit (TCU), two Cache Control Units (CCUs), a System Interface Unit (SIU), a Math Interface Unit (MIU), and three math chips (ADD/SUB, MUL, and DIV). The Floating Point Coprocessor is comprised of the MIU chip along with the three math chips.



Series 950 Processor Board

Instruction Pipelining

The Series 950 is pipelined at the instruction level allowing for operation on three instructions simultaneously. The instruction pipeline consists of three 73 nanosecond stages. During the first stage the instruction is fetched from the cache and decoded. The specified function or calculation is performed during the second stage, and in the third stage the result of the calculation is saved to a CPU general purpose register or cache. Excepting penalties for cache misses, etc., the net effect is that one instruction completes with every 73 ns CPU cycle.



Instruction Pipelining

Caches

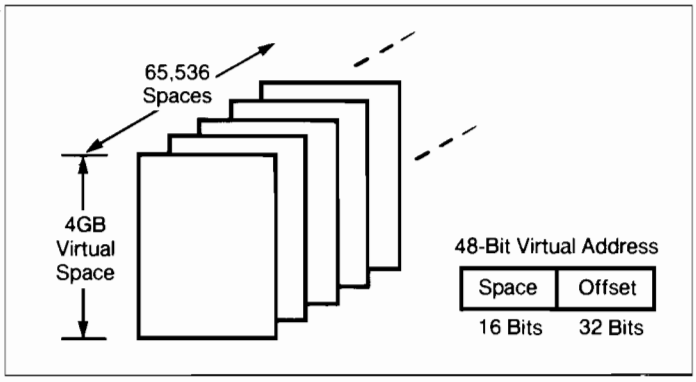
The cache is a high-speed buffer for the CPU which minimizes the number of relatively slow transactions with main memory. The Series 950 uses a 128 Kb high-speed, integrated CPU cache for data and instructions. The cache uses a *write-to* management scheme, is two-way associative (direct mapped) and is organized in sets of 4096 cache lines, with 32 bytes per cache line. Data modified in the cache is written to main memory only when the processor requires other data to be in that cache location, or when a Direct Memory Access (DMA) operation is performed within that data area, or upon a power fail.

Floating Point Coprocessor

Single-precision and double-precision floating point calculations are performed by the Floating Point Coprocessor. The coprocessor significantly decreases the time required to perform floating point calculations. The Floating Point Coprocessor and the CPU can operate in parallel, allowing for increased performance in applications which use floating point.

Virtual Memory Management

Virtual Addresses on the Series 950 are 48 bits in length. This greatly extended address space ensures sufficient expandability to meet evolving software needs. Virtual Memory is divided into a set of 65,536 spaces, with each space 4 Gb in length. Spaces are further divided into fixed length 2 Kb pages, with a given page holding either data, code, or both. A single data structure can be up to either 1 Gb or 4 Gb in length (compiler-dependent) and code can span multiple spaces.



Virtual Memory Organization

Virtual Address Translation

Virtual-to-Physical address translation is done by Translation Lookaside Buffers (TLBs) which cache recently accessed virtual page translations and convert the 48-bit virtual address into a 30-bit physical address. The Series 950 TLB holds translations for 4096 virtual pages, and is split into a 2048-entry instruction TLB and a 2048-entry data TLB. Page-level access protection is provided on the Series 950, and the TLB hardware supports protection mechanisms to ensure that the currently executing process has sufficient authorization to perform the requested data, code, or I/O access.

Memory Subsystem

The Series 950 supports 32 Mb of main memory standard and is expandable to 128 Mb in 16 Mb increments. The memory subsystem uses 1 M-bit, Nibble-mode Dynamic RAMs. Main memory has battery back up to ensure that information is maintained for a minimum of 15 minutes in the event of an interruption in AC power. This allows the operating system to be automatically restarted and processing to continue without data loss, upon resumption of power.

The internal memory word size is 72 bits, with 64 data bits of two 32-bit words, plus eight bits for error detection and correction. Single-bit memory errors are automatically corrected, with automatic detection of all double-bit errors.

I/O Subsystem

I/O Busses

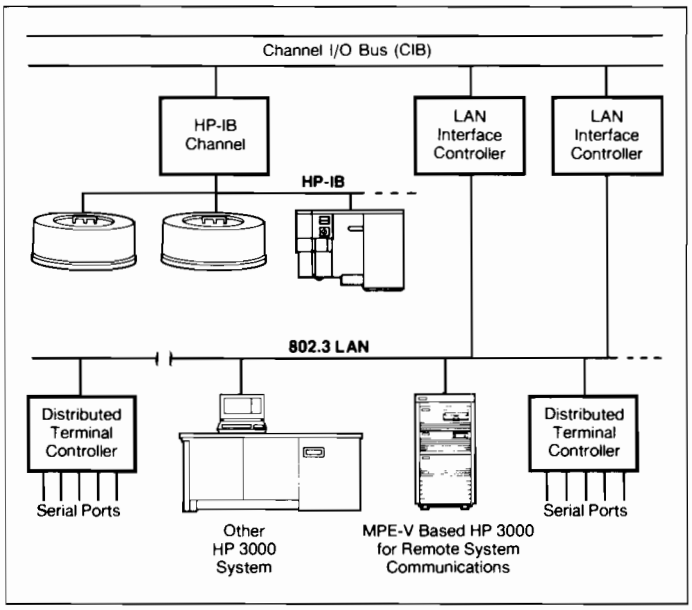
Channel I/O Busses (CIBs) support up to 5 cards each for interfacing peripheral devices and providing for local area networking. Each CIB Adapter provides DMA functions and has a data throughput capacity of up to 5 Mb/second. Two CIB adapters directly connect to each Central Bus (CTB). Each of the two CTBs run synchronously with a 9 MHz clock and can support data transfer rates of up to 20 Mb/second.

Memory Mapped I/O

Input/Output operations are initiated and controlled via a memory-mapped I/O scheme, such that the processor only needs to access reserved virtual or physical memory locations to control I/O operations. Memory Mapped I/O allows for streamlined I/O operations and thus increases system performance in I/O intensive applications.

Peripheral Connection

Discs, tapes and printers are connected via an HP-IB Channel which supports the 8 bit wide, IEEE-488 standard Hewlett-Packard Interface Bus (HP-IB). Each HP-IB channel supports up to six peripheral devices.



I/O Attachments

Workstation and Serial Printer Connection

Connections for workstations, serial printers and other serial devices are provided via Distributed Terminal Controllers (DTCs) which are distributed over an IEEE 802.3 standard Local Area Network (LAN). This flexible connection scheme allows DTCs to be situated in the department that they service, saving the cost and effort of running cables from each workstation back to the processor. Each DTC can support up to 48 direct connect ports, or 36 modem ports, or a combination of the two. Both RS-232 and RS-422 interfaces are supported.

System-to-System Datacommunications

AdvanceNet compatible local HP 3000 to HP 3000 communications are supported via the LAN, with available services including Network File Transfer, Remote File Access, Virtual Terminal, and Remote Data Base Access to TurboIMAGE databases.

Supported via an HP 3000 MPE V-based system acting as a datacomm server on the LAN are IBM communications, including SNA NRJE/IMF and Bisync RJE, MRJE and IMF, as well as remote HP 3000 to HP 3000 communications.

Environmental Specifications

AC Input Voltage
208 VAC, three phase @ 60 Hz
380 VAC, three phase @ 50 Hz
415 VAC, three phase @ 50 Hz

Input Voltage Tolerance
±10%

Input Voltage Frequency
50 Hz or 60 Hz (±2%)

Input Current
16.0 amps @ 208 VAC 60 Hz
8.0 amps @ 380 VAC 50 Hz
7.5 amps @ 415 VAC 50 Hz

Input Power Consumption, Max.
3000 watts

Heat Dissipation, Max.
15,000 BTU/hour

Physical Dimensions
Height: 1.00 meter (39 inches)
Width: 1.30 meter (51 inches)
Depth: 0.71 meter (28 inches)

Weight
400 Kg (880 lbs)

Operating Temperature, System
20-25.5 degrees C (68–78 degrees F)

Relative Humidity, System (Operating)
40–60% (non-condensing)

Altitude (Operating)
Up to 15,000 feet

Battery Backup Time, Minimum
15 minutes

Acoustics
73 dB (A) Sound Power

Regulatory Compliance

Safety
UL Listed, CSA Certified
Compliant to IEC 380/435

Electromagnetic Interference
Complies with FCC Rules and Regulations, Part 15, Subpart J, as a Class A computing device. FTZ Individual Permit (Level A Serial License).

System Software

Listed below are software products currently available for the HP 3000 Series 950. This list will be expanded in the near future as development and testing of additional software products continues.

Operating System
MPE XL

Datacommunications
Network Services (NFT, RFA, VT, RDBA)
HP SNA Server Access/XL
HP AdvanceLink

Utilities

EDIT/V	TDP/V
FCOPY/XL	HP Spell/V
SORT-MERGE/XL	

Languages

COBOL II/XL	HP Business BASIC/V
HP Pascal/XL	SPL/V
HP FORTRAN 77/XL	RPG/V

Information Management

ALLBASE/XL	Query/V
TurboIMAGE/XL	Transact/V
TurboIMAGE DBchange/V	VPLUS/V
TurboIMAGE Profiler/V	HP System Dictionary/XL
Inform/V	Dictionary/V
Report/V	KSAM/V
HP Toolset/XL	

Application Software

A wide range of manufacturing, financial and information management applications are available for HP 3000 systems. Your HP Sales Representative can provide further information regarding specific applications on the Series 950.

Supported Peripherals

Listed below are peripheral devices currently available for the HP 3000 Series 950. This list will be expanded in the near future as development and testing of additional peripherals continues.

Terminals

2392A Block-mode terminal, 2397A and 2627A Color Graphics Terminals, 2393A Black and White Graphics Terminal, 2624B Forms Terminal, 2622 Data Entry Terminal. Portable PLUS, VECTRA, and HP 150 Touchscreen Personal Computers supported as workstations. Maximum 400 workstations per system.

Disc Drives

7933H, 7937H Fixed Media and 7935H Removable Media Disc Drives. Maximum 24 discs per system.

Tape Drives

7974A and 7978A/B half-inch tape drives. Maximum eight per system.

System Printers

2565A 600 LPM and 2566A/B 900 LPM line printers: maximum eight per system. 2680A and 2688A Page Printers: maximum four per system.

Serial Printers

2686A Page Printer and 2934A 200 CPS dot matrix printer. Maximum 32 remote printers per system.

Support Services

A wide range of hardware and software services are available worldwide for all HP 3000 Products. Contact your HP Sales Representative for details on available support services.

Ordering Information

The HP 3000 Series 950 SPU includes 32 Mb main memory, two CIBs, two HP-IB channels and one LAN interface. The SPU hardware is available either without systems software or as part of a preconfigured system. As shown below, the preconfigured system product includes SPU hardware, operating system, data management software, and migration utilities. Return credits are available when upgrading most HP 3000 systems to the Series 950.

Product Number	Description
32491A	HP 3000 Series 950 SPU hardware. Includes processor with 32 Mb Memory, two CIB, two HP-IB Channels, one LAN interface.
32490A	HP 3000 Series 950 Preconfigured System. Includes Series 950 SPU, MPE XL Operating System, System Dictionary/XL, ALLBASE/XL Data Management System, TurboIMAGE/XL, QUERY/V, KSAM/V, VPLUS/V, SORT-MERGE/XL, EDIT/V, FCOPY/XL, DEBUG/V, Migration Utilities.

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