# HEWLETT-PACKARD

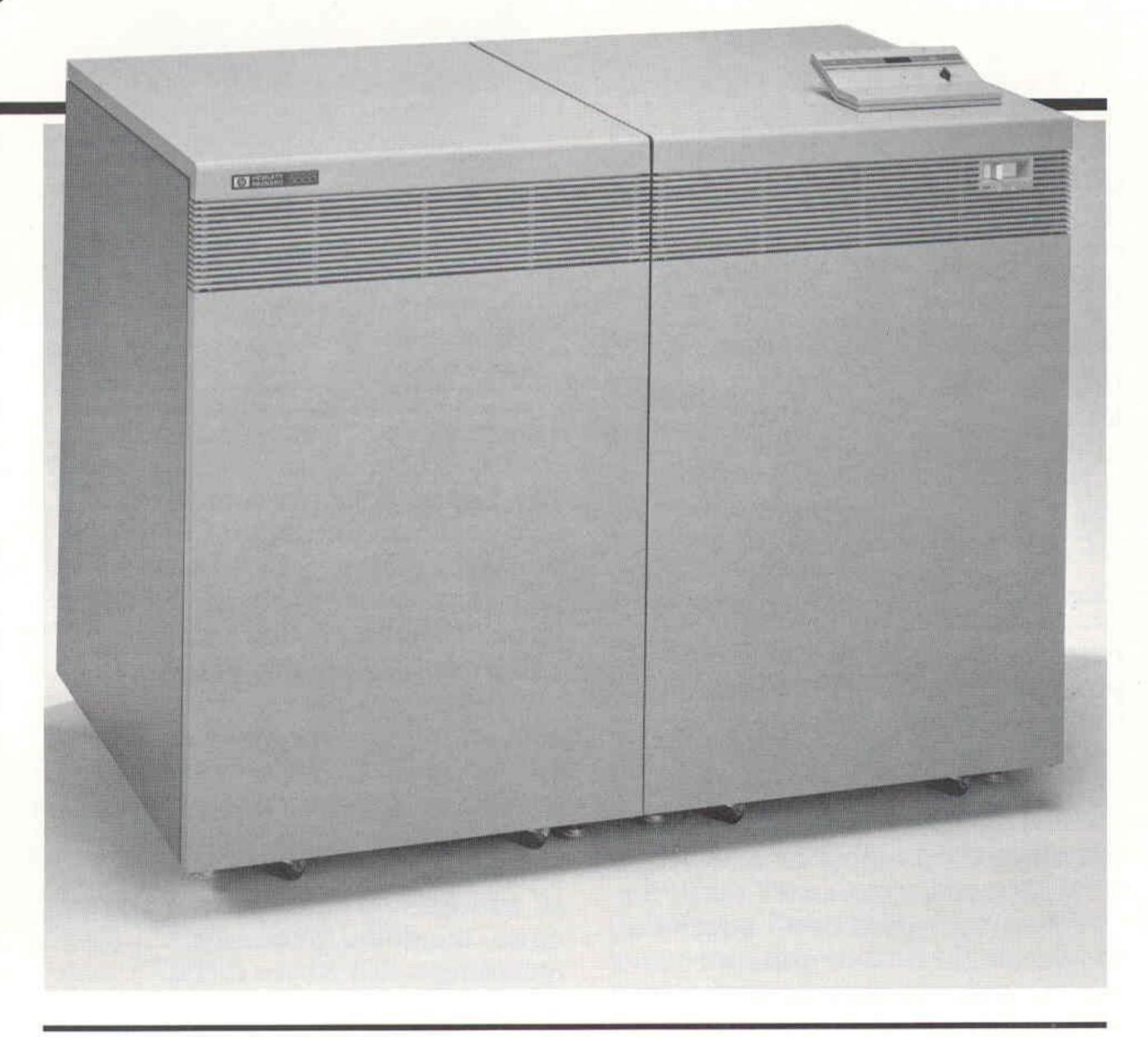
## Series 955

## **HP 3000 Computer Systems**

## Data Sheet

### **Product description**

The Series 955 is the highest performance member of the broad family of compatible HP 3000 business computers. The Series 955 takes advantage of HP Precision Architecture (HPPA) and an advanced implementation of Hewlett-Packard's proprietary NMOS III VLSI technology to provide powerful uniprocessor performance. The Series 955 also uses an impressively few number of parts, including a single-chip CPU on a single-board processor, thereby providing an exceptionally reliable and cost-effective solution for data processing applications challenges at the high end. A convenient field upgrade to the high performance Series 950, the Series 955 delivers significant, incremental growth with a modular approach to extending the HP 3000 system family. As an HP 3000, the Series 955 takes advantage of an operating system designed specifically for commercial data processing. The Series 955 also utilizes its powerfully designed processor and a high performance floating point coprocessor to excel in computationally intensive applications. In total, the Series 955 provides exceptional performance and functionality in multi-user, multi-tasking interactive and batch environments and runs a wide variety of financial, manufacturing, service industry, and information management software to meet your data management needs.



#### **Features**

- 11 MIPS CPU Performance
- Single-chip VLSI CPU, singleboard processor
- 40 nanosecond system clock cycle
- 48 bit virtual addressing
- 48 Mbyte main memory standard, expandable to 128 Mbytes
- 128 Kbyte high-speed CPU instruction cache
- 128 Kbyte high-speed CPU data cache
- Ultra high-performance floating point coprocessor standard
- Advanced five-stage instruction pipelining

- 16K-entry Translation Lookaside Buffer
- Battery backup, auto restart standard
- Three-level I/O hierarchy providing high I/O bandwidth
- High-speed, 100 Mbytes/second System Memory Bus
- IEEE 802.3 standard local area network terminal connection
- MPE XL operating system
- Network and relational database management systems standard

### Advanced technologies

#### **HP Precision Architecture**

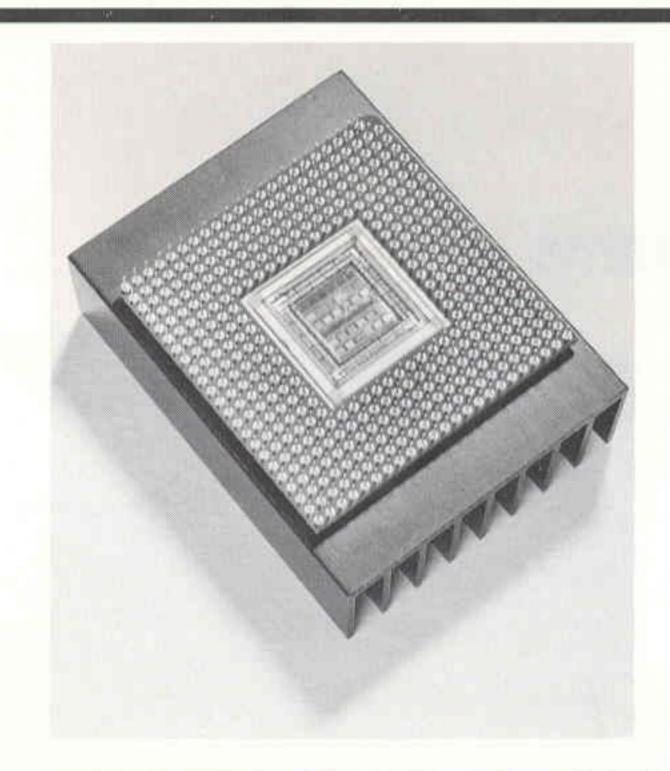
The Series 955 uses HP Precision Architecture (HPPA) and a very powerful implementation of HP's proprietary NMOS III VLSI technology to produce a high performance, highly reliable system at a low cost. HPPA builds on reduced instruction set computing (RISC), a design approach that delivers greatly simplified computers that are optimized to provide the highest performance for a given integrated circuit (IC) technology. In addition, the inherent simplicity of HPPA means lower cost and higher reliability due to the need for fewer components.

The core of HPPA is an instruction set containing 140 carefully selected, fixed-format instructions. Because the instruction set is simple, instructions can be hardwired directly in the central processing unit (CPU), eliminating the need for microcode and the necessity to decode complex instructions.

HPPA utilizes a Load/Store design to reduce the number of relatively slow memory accesses, as most operations are performed registerto-register. To further enhance performance, optimizing compilers are used to schedule instructions and manage the instruction pipeline. With hardwired control, a Load/Store design, and optimizing compilers, one instruction is executed with virtually every clock cycle. Single-cycle execution provides much of the performance benefit of HPPA over traditional architectures.

HPPA goes beyond RISC to incorporate other features that greatly enhance its performance and functionality. For example:

- Support for coprocessors (i.e., floating point)
- Extended addressing
- Memory-mapped I/O subsystem



## **VLSI** technology

The Series 955 is implemented using a powerful design in HP's proprietary NMOS III VLSI technology, allowing the entire Series 955 CPU to be put on a single 1.4cm die, comprising 180,000 transistors and packaged in a 408-pin pin-grid-array (PGA). This 408-pin PGA allows separate paths for data and instructions from the cache to memory and enables single-cycle execution for every 40 nanosecond clock cycle. Furthermore, the entire processor, including a 256 Kbyte cache, 16K-entry translation Lookaside Buffer (TLB), and the high performance floating point coprocessor, exist on a single printed circuit board.

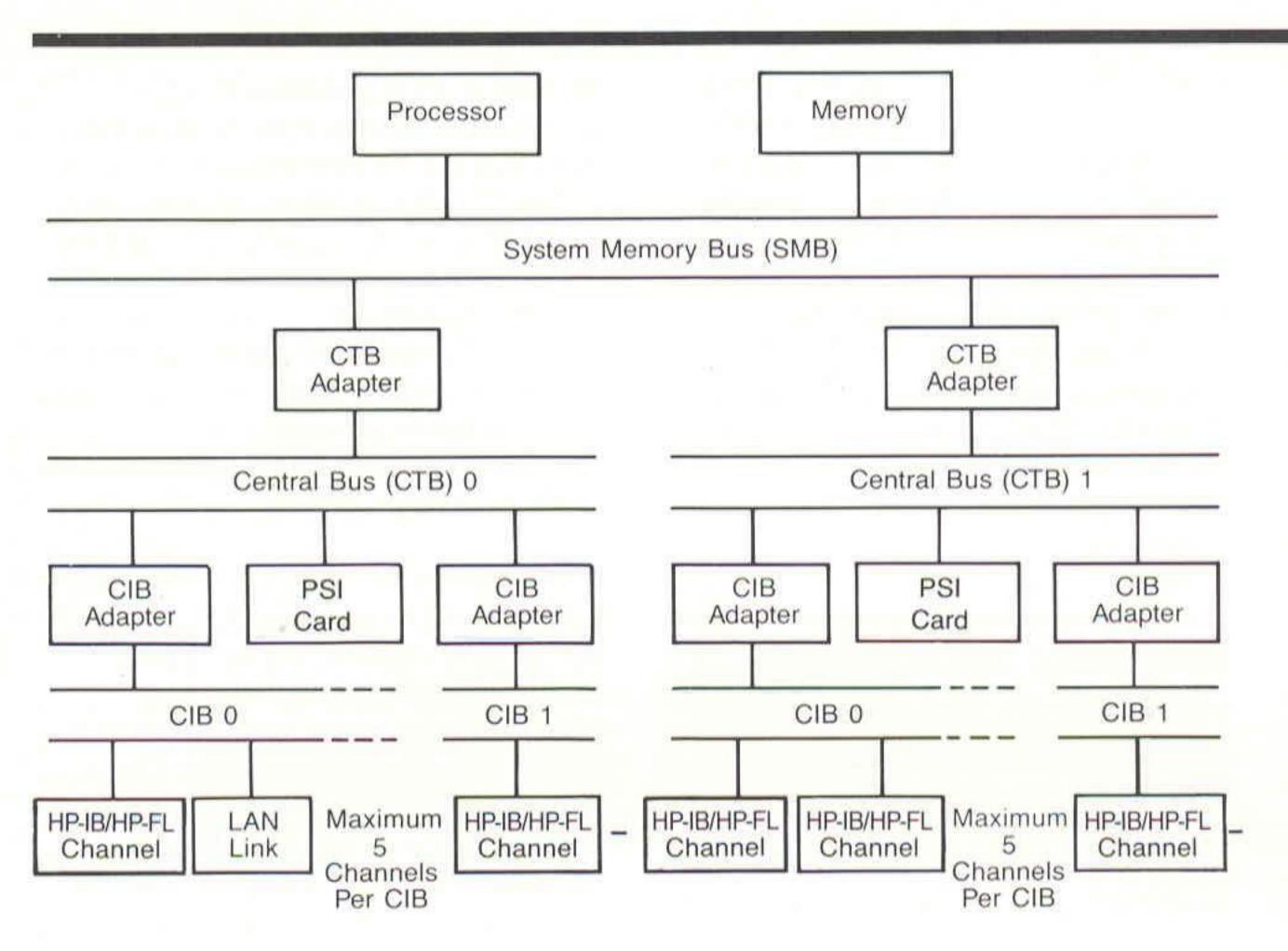
## System organization

The processor communicates with main memory via the System Memory Bus (SMB). The SMB is a very high-speed bus that provides a 64-bit data path and can support sustained data transfer rates of up to 100 Mbytes/second. The SMB connects to two central buses (CTBs) through separate CTB adapters. Each CTB supports two channel I/O buses (CIBs) via separate CIB adapters. The CIBs support I/O interfaces to peripheral devices and Local Area Network (LAN) links.

The CTBs also support
Programmable Serial Interfaces
(PSI cards), allowing the HP 3000
900 Series systems to be linked to
other computers in a distributed
processing environment. The
Series 955 supports 8 PSI cards.

## The Series 955 processor

The entire Series 955 processor, implemented using HP's proprietary NMOS III VLSI technology, the 256 Kbyte cache for data and instruction, and the 16K-entry Translation Lookaside Buffer resides on a single printed circuit board. The design includes a Central Processing Unit (CPU), a Translation Lookaside Buffer Control Unit (TCU), an Instruction Cache Control Unit (ICCU), a Data Cache Control Unit (DCCU), a System Interface Unit (SIU), and the floating point coprocessor consisting of a Floating Point Controller (FPC) and two math chips.



System Structure

Instruction 1	Fetch	Instruction Decode	Execute	Condition	Store				
Instruction 2		Fetch	Instruction Decode	Execute	Condition	Store		3	
Instruction 3		1	Fetch	Instruction Decode	Execute	Condition	Store		
Instruction 4		,,		Fetch	Instruction Decode	Execute	Condition	Store	
Instruction 5					Fetch	Instruction Decode	Execute	Condition	Store
	40 ns	40 ns	40 ns	40 ns	40 ns	40 ns	40 ns	40 ns	40 ns

### Instruction pipelining

The Series 955 is pipelined at the instruction level, allowing operation on five instructions simultaneously. The instruction pipeline consists of five 40 nanosecond stages. During the first stage, the instruction is fetched from cache. The specified instruction is decoded during the second stage, and the resulting CPU internal calculation or function is performed during the third stage. The fourth stage is used to generate the condition code for the corresponding result. Finally in the fifth stage, a general purpose register is set with the corresponding cache or internal result. Excepting penalties for cache misses, etc., the net effect is that one instruction completes with every 40 nanosecond CPU cycle.

#### **Caches**

The cache is a high-speed buffer for the CPU that minimizes the number of relatively slow transactions with main memory. The Series 955 uses a 128 Kbyte high-speed CPU instruction cache and a 128 Kbyte high-speed CPU data cache. Each cache uses a write-to management scheme, is two-way associative (direct mapped), and is organized in sets of 4,096 cache lines, having 32 bytes per line. Data modified in the cache is written to main memory only when the processor requires other data to be in that cache location, or when a direct memory access (DMA) operation is performed within that data area, or upon a power fail.

## Floating point coprocessor

Single-precision and doubleprecision floating calculations are performed by the floating point coprocessor. The coprocessor is designed using ultra high performance chips and significantly decreases the time required to perform floating point calculations. The floating point coprocessor and the CPU can operate in parallel, allowing for increased performance in applications that use floating point.

## Virtual memory management

Virtual addresses on the Series 955 are 48 bits in length. This greatly extended address space ensures sufficient expandability to meet evolving software needs. Virtual memory is divided into a set of 65,536 spaces, with each space 4 Gbytes in length. Spaces are further divided into fixed-length, 2 Kbyte pages, with a given page holding either data, code, or both. A single data structure can be up to either 1 Gbyte or 4 Gbytes in length (compiler dependent), and code can span multiple spaces.

## Virtual address translation

Virtual-to-physical address translation is done by Translation Lookaside Buffers (TLBs) that cache recently accessed virtual page translations and convert the 48-bit virtual address into a 30-bit physical address. The Series 955 TLB holds translations for 16,384 virtual pages, and is split into an 8,192-entry instruction TLB and an 8,192-entry data TLB. Page-level access protection is provided on the Series 955, and the TLB hardware supports protection mechanisms to ensure that the currently executing process has sufficient authorization to perform the requested data, code, or I/O access.

### **Memory Subsystem**

The Series 955 supports 48 Mbyte of main memory standard and is expandable to 128 Mbytes in 16 Mbyte increments. The memory subsystem uses 1 Mbit, nibblemode dynamic RAMs. Main memory has battery backup to ensure that information is maintained for a minimum of 15 minutes in the event of an interruption in AC power. This allows the operating system to be automatically

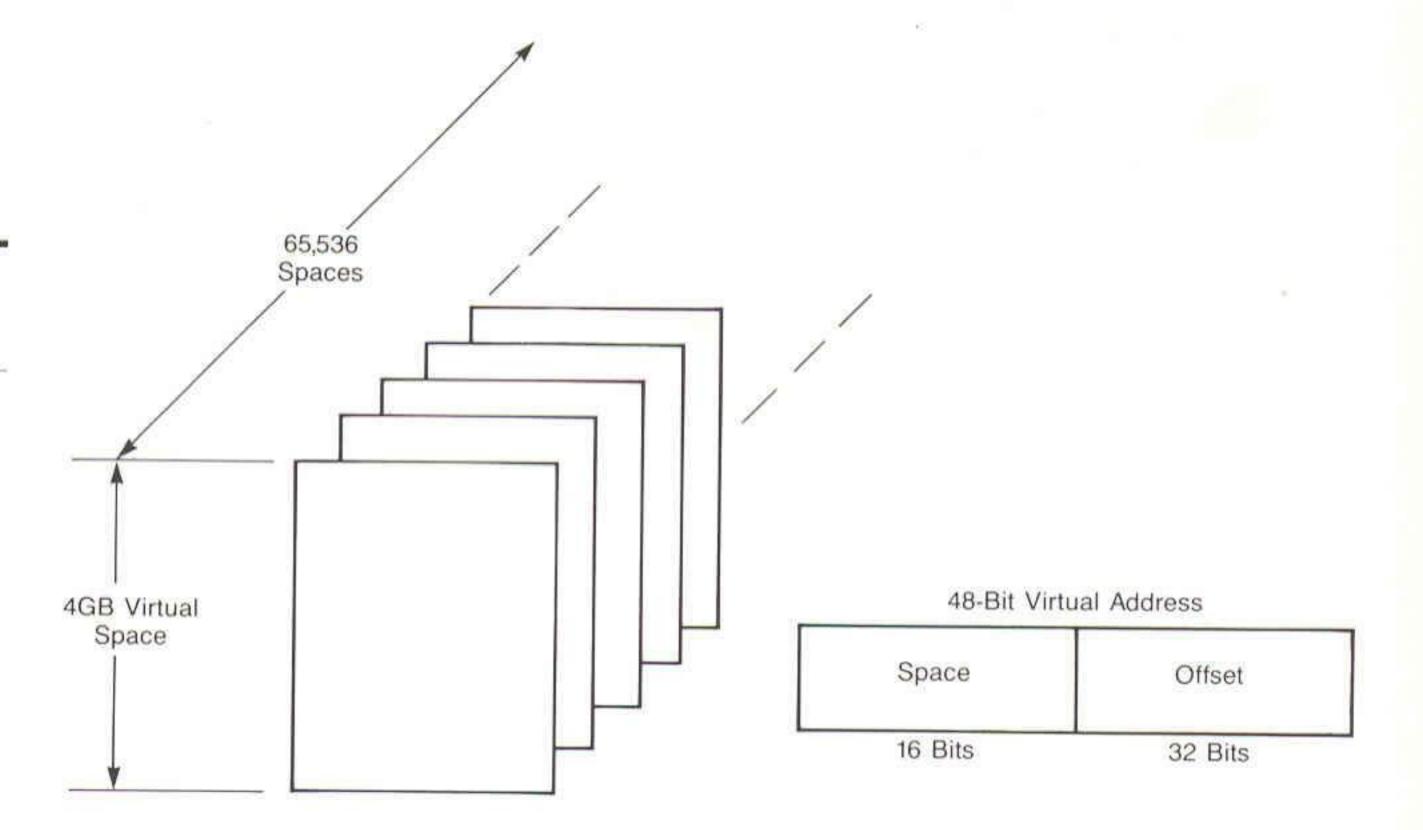
restarted and processing to continue without data loss upon resumption of power.

The internal memory word size is 72 bits, with 64 data bits of two 32-bit words, plus 8 bits for error detection and correction. Single-bit memory errors are automatically corrected, with automatic detection of all double-bit errors.

### I/O subsystem

#### I/O Buses

Channel I/O Buses (CIBs) support up to five cards each for interfacing peripheral devices and providing for local area networking. Each CIB adapter provides DMA functions and has a data throughput capacity of up to 5 Mbytes/second. Two CIB adapters directly connect to each Central Bus (CTB). Each of the two CTBs run synchronously with a 9-MHz clock and can support data transfer rates of up to 20 Mbytes/second.



#### Memory-Mapped I/O

Input/output operations are initiated and controlled via a memory-mapped I/O scheme, such that the processor only needs to access reserved virtual or physical memory locations to control I/O operations. Memory-mapped I/O allows for streamlined I/O operations and thus increases system performance in I/O-intensive applications.

#### **Peripheral Connection**

Discs, tapes and printers are connected via an HP-IB channel that supports the 8-bit wide, IEEE-488 standard Hewlett-Packard Interface Bus (HP-IB). Each HP-IB channel supports up to six peripheral devices.

Discs are also connected via HP Fiber-optic Link Channels (HP-FL), each supporting up to 8 discs.

#### Workstation and Serial Printer Connection

Connections for workstations, serial printers, and other serial devices are provided via Distributed Terminal Controllers (DTCs) that are distributed over an IEEE 802.3 standard local area network (LAN). This flexible connection scheme allows DTCs to be situated in the department that they service, saving the cost and effort of running cables from each workstation back to the processor. Each DTC can support up to 48 direct connect ports, or 36 modem ports, or a combination of the two. Both RS-232C and RS-422C interfaces are supported.

PCs can also be connected to the 802.3 LAN via HP StarLAN which is a local area networking scheme using unshielded twisted pair (or phonewire).

#### Channel I/O Bus (CIB) LAN LAN HP-IB HP-FL Interface Interface Channel Channel Controller Controller ( TVV) CLAS ( TVT) 802.3 LAN Distributed Distributed **HPStarLAN** Terminal Terminal Controller Controller (c=i)Serial Ports Other HP 3000 System

## Environmental specifications

**AC Input Voltage** 

208 VAC, three phase @ 60 Hz 380 VAC, three phase @ 50 Hz 415 VAC, three phase @ 50 Hz

Input Voltage Tolerance

± 10%

Input Voltage Frequency 50 Hz or 60 Hz (±2%)

Input Current

8.0 amps @ 208 VAC 60 Hz 4.4 amps @ 380 VAC 50 Hz 4.0 amps @ 415 VAC 50 Hz

Input Power Consumption, Maximum

2,300 watts

Heat Dissipation, Maximum 7,900 BTU/hour

Physical Dimensions

Height: 1.00 meter (39 inches)
Width: 1.30 meters (51 inches)
Depth: 0.71 meters (28 inches)

Weight

400 Kg (880 lbs)

Operating Temperature, System 20-25.5 degrees C (68-78 degrees F)

Relative Humidity, System

(Operating)

40-60% (noncondensing)

Altitude (Operating)

Up to 15,000 feet

Battery Backup Time, Minimum

15 minutes

Acoustics

73 dB (A) Sound Power

## System-to-system datacommunications

NS3000/XL and LAN Link/XL provide virtual terminal, network file transfer, remote file and database access, network interprocess communication, and remote process management between HP 3000s on an IEEE 802.3 LAN. These same capabilities for remote communications are currently provided via an MPE V HP 3000 system. SNA IMF, SNA NRJE, and SNA Link provide HP 3000 to IBM system communications.

## System software

Listed below are software products currently available for the HP 3000 Series 955 as of MPE XL Release 1.1. This list will be expanded over time as development and testing of additional software products continue. Check with your local sales representative for more information.

### **Application software**

A wide range of solutions is available for the HP 3000 systems in application areas that include manufacturing, financial management, and information management. Your sales representative can provide more information that is specific to your needs.

#### Operating System

MPE XL

#### **Datacommunications**

NS3000/XL LAN Link/XL SNA IMF SNA NRJE

SNA Link

Office Automation
TDP/V
HP/Spell/V
HP Deskmanager
HP Curator

#### Languages

COBOL II/V
COBOL II/XL
Pascal/V
HP Pascal/XL
FORTRAN 66/V
HP FORTRAN 77/V
HP FORTRAN 77/XL
HP FORTRAN 77/XL
HP FORTRAN 77/XL

HP AdvancePrint

#### Information Management

Query/V ALLBASE Transact/V TurboIMAGE/XL Transact/XL Visor/XL VPLUS/V TurboIMAGE DBchange/V HP System Dictionary/XL KSAM/V Inform/V Dictionary/V Report/V BRW/V HP Toolset/XL BRW/XL Information Access/XL

Terminals						
2392		HP Vectra PC				
2393			Portable Plus			
2397			HP Vectra CS			
2394			HP Vectra ES, ES12			
700/92			Touchscreen II PC			
700/94						
Disc Drives						
7937H/XP			7935H/XP			
7933H/XP			7936H/XP			
			7937FL			
Tape Drives						
7978A/B	×.		7979A			
7974A			7980A			
Printers						
2680	2566A/B	2686	2563A/B	2567B		
2688	2565A	2934	2564B	LaserJet 2000		

## Supported peripherals

Listed here are peripheral devices currently available for the HP 3000 Series 955 as of MPE XL Release 1.1. This list will be expanded over time as development and testing of additional peripherals continue. Check with your sales representative for more information.

### Support services

A wide range of hardware and software support services are available worldwide for all HP 3000 products. Contact your HP sales representative for details on available support services.

## **Ordering Information**

The HP 3000 Series 955 SPU includes 48 Mbyte main memory, two CIBs, one LAN interface, a console connection, and two HP-IB channels. Return credits are available when upgrading HP 3000 systems other than the Series 950 to the Series 955. The Series 955 is also available as a field upgrade from the Series 950. For more information, contact your local HP sales office.

