



PAPER TAPE NO. 12924-16001

HP 2892A/12924A  
CARD READER SUBSYSTEM  
DIAGNOSTIC

for

hp 2100 SERIES COMPUTERS

**reference manual**



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## Section I

### INTRODUCTION

#### 1-1. GENERAL

The purpose of this program is to check and exercise the HP 2892A Card Reader with its interface. Any hardware malfunction will be detected. The program is designed in such a manner that it will also aid the operator in detecting specific components that failed.

#### 1-2. REQUIRED HARDWARE

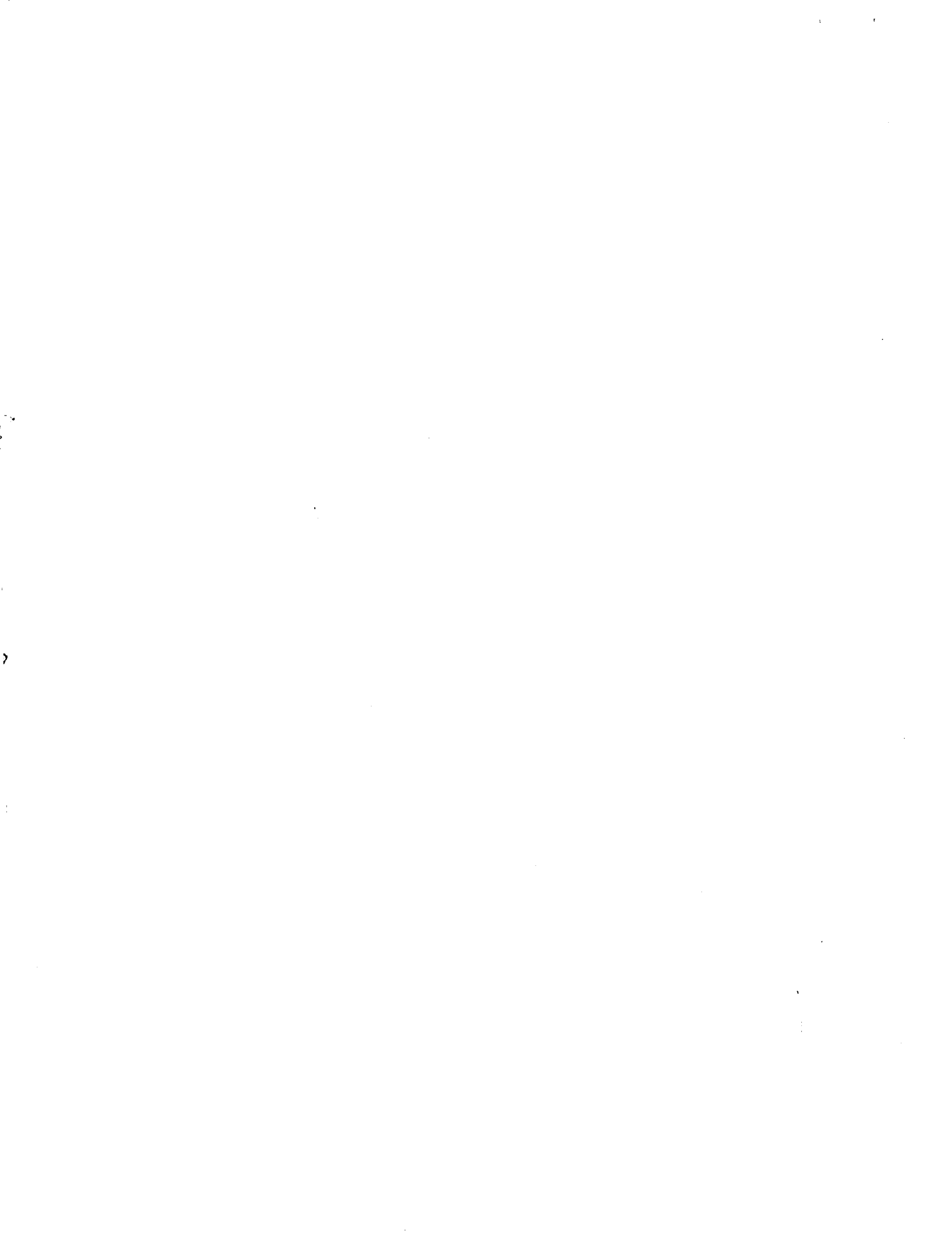
The following hardware is required:

- a. HP 2100 series computer with a minimum 4K memory.
- b. An HP 12924A interface with a 2892A Card Reader.
- c. A paper tape reading device (used only for loading).
- d. A console teleprinter device for message reporting (recommended but not required).
- e. Optional: Time Base Generator, HP 12539 (for READ RATE TEST).

#### 1-3. REQUIRED SOFTWARE

The following software is required:

- a. Diagnostic Configurator Product No. 24296 used for equipment configuration and as a console device driver. The product includes the following part no.:  
Binary object tape      Part No. 24296-60001  
Manual                      Part No. 02100-90157
- b. HP 2892A Card Reader Diagnostic binary object tape, Part Number 12924-16001.
- c. One card deck consisting of 50 identical cards prepunched with the worst case pattern. See Figure 4-3. This card deck Part Number 12924-90004 was shipped with the interface kit.



Section II  
PROGRAM ORGANIZATION



2-1. ORGANIZATION

The diagnostic is grouped in four functional blocks. Each block will be explained in detail later in the text. The four blocks are Control, Message Reporting, Functional Tests and pseudo Operator Design.

The functional tests (each test is covered under Diagnostic Performance in section IV) are set up to check basic functions first, then move to more complex functions. The functions will cover:

- a. Basic I/O control (flag and interrupt for HP 2100 series interface).
- b. Status Reporting (card reader ready, off line, picker trouble, etc.).
- c. Timing (from pick command to first column, between columns, and column 80 to End-of-Operation).
- d. Data Pattern (worst case)
- e. Read Rate (cards per minute).
- f. Direct Memory Access Transfer (also using a worst case pattern).

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device for operator information then executes the tests according to the options selected by the operator on the switch register. The control section primarily checks switch register bits 12, 13 and 15. If set, bit 12 is used to loop on the diagnostic, bit 13 is used to loop on a given test that is running at the time. Bit 15, if set, will halt the computer at the completion of a test.

The control block also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if switch register bit 10 is clear). The count will be reset only if the program is re-started.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed.

2-3. TEST SELECTION

The control portion of the program enables the operator to select his own test, or sequence of tests. Set switch register bit 9 to indicate operator test selection desired then pressed RUN. The computer will halt (102075) to indicated it is ready for the selection. If the program is running a test, that test will be completed. The program will then halt. The operator then loads the A-register with test selections. A-register bit 0 represents Test 00, bit 1 represents Test 01, and so on. Bit 6 represents Test 06, the highest possible selection. The operator must clear switch register bit 9 and press RUN to continue. The selection will then be run. If the operator clears all bits on the A-register, the standard sequence will be run.

Table 2-1 Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	Test 00 BASIC I/O
1	Test 01 STATUS
2	Test 02 TIMING
3	Test 03 DATA PATTERN
4	Test 04 READ RATE
5	Test 05 DMA TRANSFER
6	Test 06 PSEUDO OPERATOR DESIGN
7 - 15	Reserved

NOTE: The B-Register is reserved

The standard set of tests consists of tests 00 through 05. If operator selection is not requested, or if operator selection is requested and the A-register is cleared, the default case tests 00 through 05 will be executed. If operator selection is requested and A-register bits 7 through 15 or any B-register bits are set, they will be ignored. Only the valid A-register bits 0 through 6 have any meaning.

#### 2-4. MESSAGE REPORTING

There are two types of messages, error and information. Error messages are used to inform the operator of the failure of the Card Reader to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or instruct the operator to perform some operation related to Card Reader functions. In the last case mentioned an associated halt will occur to allow the operator time to perform the function. To continue the operator must press RUN.

If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available.

Example - Error with halt

Message: E013 SECOND INT OCCURRED (CONSOLE DEVICE)  
Halt Code: 102013<sub>8</sub> (T-or Memory Data Register)

Example - Information with halt

Message: H024 PRESS PRESET, THEN RUN  
Halt Code: 102024<sub>8</sub>

Refer to table 4-1 for specific meanings.

Example - Information only

Message: H025 BI-0 COMP  
Halt Code: None

Error messages can be suppressed by selection of the switch register bit 11 and error halts can be suppressed by switch register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by switch register bit 10.

#### 2-5. PROGRAM LIMITATIONS

Checking the interface for capability of receiving, passing and denying priority is not completely checked by this diagnostic. If the interface does not receive priority (PRH from next lower select code) an error E014 NO INT will occur. To check this, remove an interface having a lower select code and run the Basic I/O test and the above mentioned error should occur. Checking the interface ability to pass or deny priority is beyond the scope of this diagnostic.





## Section III

### OPERATING PROCEDURE

#### 3-1. LOADING BINARY TAPES AND CONFIGURING

- a. Load Diagnostic configurator binary object tape. If it is a configured version skip to step b. Configure program according to the Diagnostic Configurator M.O.D.\*
- b. The operator may dump a configured Diagnostic Configurator binary object tape at this point.
- c. Load main diagnostic binary object tape. At this point a binary tape of the combined configurator and diagnostic may be dumped using the configurator dump routine.
- d. If a preconfigured binary tape was loaded, go to paragraph 3-2.
- e. Load P-register with the starting address  $1000_8$ .
- f. Load the switch register with the select codes of the Card Reader under test (bits 0-5 for CR I/O select code) and the Time Base Generator (HP 12539) if available (bits 9-14 for TBG I/O select code).
- g. Press PRESET (INT/EXT) and press RUN. The computer will run then halt with  $102074_8$  in the MEMORY DATA register. If halt  $102073_8$  occurs, one of the select codes input was less than or equal to  $7_8$ ; correct the select code and press RUN.

At this point the operator may dump to paper tape a copy of the configured program. Refer to the M.O.D.\* for the configurator dump routine operation instructions. If this is done, the operator must set the P-register equal to  $2000_8$  before continuing to the next section.

#### 3-2. SWITCH REGISTER SELECTION AND RUNNING

- a. If a preconfigured tape was loaded set the P-register equal to  $2000_8$ , if not skip this step.
- b. Make selection of switch register options according to table 3-1.

\*M.O.D. - Manual of Diagnostics

Table 3-1. Switch Register Settings

BIT	MEANING IF SET
0	Loop on Pseudo Operator Design
1	Check for ready
2	Read a card and put data in read buffer
3	Compare read buffer with standard data pattern
4	List read buffer
5	Delay 1 second between picks
6	Print Status
7	Reserved
8	Reserved
9	Abort current diagnostic execution and halt (102075); user may specify a new group of tests in the A-register, clear bit 9 and then press RUN.
10	Suppress non-error messages.
11	Suppress error messages
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or teletype is not present. Also those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number in octal.

pseudo  
operator  
design  
only

If switch register is cleared, the program will execute all tests (except pseudo Operator Design) and halt with 102077<sub>8</sub> in the data register. It is suggested that this be done on the first pass of the diagnostic.

- c. Press PRESET (INT/EXT) and press RUN. The program will now execute the diagnostic according to the switch register options. At the completion of each pass of the diagnostic the pass count is output to the console for operator information. If switch register bit 12 was not selected the computer will halt with 102077<sub>8</sub> in the memory data register. At this point the A-register contains the pass count. To run another pass the operator need only press RUN.
- d. The program may be restarted by setting the P-register to 2000<sub>8</sub> and proceeding from step b above.

- e. To restart and reconfigure, proceed from paragraph 3-1, step e.
- f. If a trap cell halt occurs (106077), the user must determine the cause of the interrupt of transfer of control to the location in the M-register. The program may need to be reloaded to continue.

### 3-3. PSEUDO OPERATOR DESIGN

This section is mainly designed to aid the operator in trouble shooting and repairing the card reader or interface. The operator must select test 6 to enter Pseudo Operator Design. When entered, the program will output to the console (if available and switch register bit 10 is cleared) "H117 PSEUDO OPDESIGN" indicating the program has been entered then halt with 106017<sub>8</sub> displayed. At this point the operator selects what he wants the program to do by setting the appropriate switch then presses RUN. The program will sequentially scan the switch register for selected functions and will perform each then halt with 106017<sub>8</sub> again. If the operator wishes to loop on the selected functions, he may do so by selecting switch zero.

<u>SWITCH</u>	<u>MEANING IF SET</u>
0	Loop on Pseudo Opdesign
1	Check for card reader ready (BIT 0)
2	Read a card and put data in read buffer
3	Compare read buffer with Standard Pattern
4	List Read Buffer
5	Delay 1 second before next READ
6	Print current CR Status (does not halt)



After the first pass, the A-register will contain the current status of the card reader at halt 106017<sub>8</sub>. To exit Pseudo Operator Design, clear switches 0-6 and press RUN.

The routines used for switches 1, 2 and 3 are common to other tests.

Switch 1 - Check for ready

If the Card Reader is found ready the program will continue. If the Card Reader is found not ready (Bit 0=1), the program will output the message "H055 CR NOT READY" and then halt (102055<sub>8</sub>). To continue, make the Card Reader ready and press RUN. If the Card Reader is still not ready, the message will be output

again. This will continue until the Card Reader is ready or switch 1 is cleared.

#### Switch 2 - Read a card

This routine reads a card and puts the data in a buffer for later reference. The program allows 1 second response time before an error is reported and checks that 80 columns have been read. The messages are "E130 CR TIMED OUT" and "E131 EOP BEFORE 80 COLUMNS."

#### Switch 3 - Compare Buffer

This checks the data read with the standard worse case pattern. If any data is found in error, the message "H132 DATA ERROR ACT XXXX EXP YYYY" will be output for each error. When the computer is halted, the A-register = XXXX and the B-register = YYYY.

#### Switch 4 - List read buffer

The message "H120 BUFFER LIST" and the buffer contents (4 columns) will be output. Column 1 represents columns 1-20 on the card, column 2 is 21-40, column 3 is 41-60 and column 4 is 61-80. The data is in 4 octal numbers reading left (rows 12-11-0) to right (rows 7-8-9). If a console device is not available the computer will halt (106020<sub>g</sub>) with the A register equal to each column.

RUN must be pressed for each column, unless switch 4 is cleared.

#### Switch 5 - Delay one second

Delay one-second before next scan of switch register.

#### Switch 6 - Print Status

This routine reads the status from the Card Reader and outputs the message "H120 STATUS IS XXXXXX." The computer does not halt for this message. The last status is displayed when halted with 106017<sub>g</sub>.

Section IV  
DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

4-2. BASIC I/O CHECKS

TEST Ø

Subtest 1 - Checks the ability to clear set and test the interrupt system.  
The following instruction combinations are tested:

CLF Ø - SFC Ø  
CLF Ø - SFS Ø  
STF Ø - SFC Ø  
STF Ø - SFS Ø

Errors in the above sequences produce error messages EØØØ-EØØ3.

Subtest 2 - Checks the ability to clear, set and test the interface select code.  
The following instruction combinations are tested:

CLF CH - SFC CH  
CLF CH - SFS CH  
STF CH - SFC CH  
STF CH - SFS CH

Errors in the above sequences produce error messages EØØ5-EØ1Ø.

Subtest 3 - Checks that the test select code does not cause an interrupt with the flag and control set on the interface and the interrupt system is off. The sequence of instructions is shown below:

STF Ø  
STF CH  
STC CH  
CLF Ø

The CLF Ø instruction should inhibit an interrupt from occurring. Error message EØØ4 occurs if CLF Ø fails.

Subtest 4 - Checks that the flag of the interface under test is not set when all other select code flags are set. Error message EØ11 occurs if the flag is set incorrectly.

Subtest 5 - Checks the ability of the interface to interrupt. With the flag and control set and the interrupt system on, there should be an interrupt on the I/O channel. If not, error message EØ14 occurs. Checks that the interrupt occurred where expected. The interrupt should not occur before a string of priority affecting instructions are executed. The following instructions are used to check the hold-off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP **+1,I
DEF **+1
JSB **+1,I
DEF **+1
NOP
```

Error messages E012 and E015 will occur if this is not true. Checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if this is not true. Checks that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the constol FF and flag FF set, there is no interrupt following a CLC CH instruction. The following sequence of instructions are used.

```
STC CH
STF CH
STF 0
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message E016 will occur.

Checks that the CLC 0 instruction inhibits interrupts when the control FF and flag FF are set. The following sequence of instructions is used.

```
CLF CH
STC CH
STF CH
STF 0
CLC 0
```

If the CLC 0 fails to inhibit an interrupt, error message E017 will occur.

Subtest 7 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) switches on the computer front panel performs the following actions:

1. Sets all flags (EXTERNAL).
2. Clears all control (EXTERNAL).
3. Turns off the interrupt system (INTERNAL).
4. Clears the I/O data lines (EXTERNAL).

#### 4-3. STATUS TEST

The Status Tests check that the correct status is reported from the interface and card reader. Some checks require manual operation by the operator. The program first checks status when the reader is off and on. Then continues to check the interface status and operation. The program then moves to check the status reported from the reader by forcing errors with specially prepared cards. The following is a description of the necessary cards:

- a. Two half cards and two standard cards. These are used to generate a card motion error by placing the half cards in the stacker and the two standard cards in the hopper. When the program reads the first card the front edge will hit the two half cards and block the stacker photo cell. When the second card is read, the card motions error should occur.
- b. A card with a 1/4 inch square notch torn from the leading edge. This card is used to check the Dark Check error detection circuitry.
- c. Two cards hooked together from approximately column 80 to the back edge of the card. These are used to check the pick failure detection circuitry.

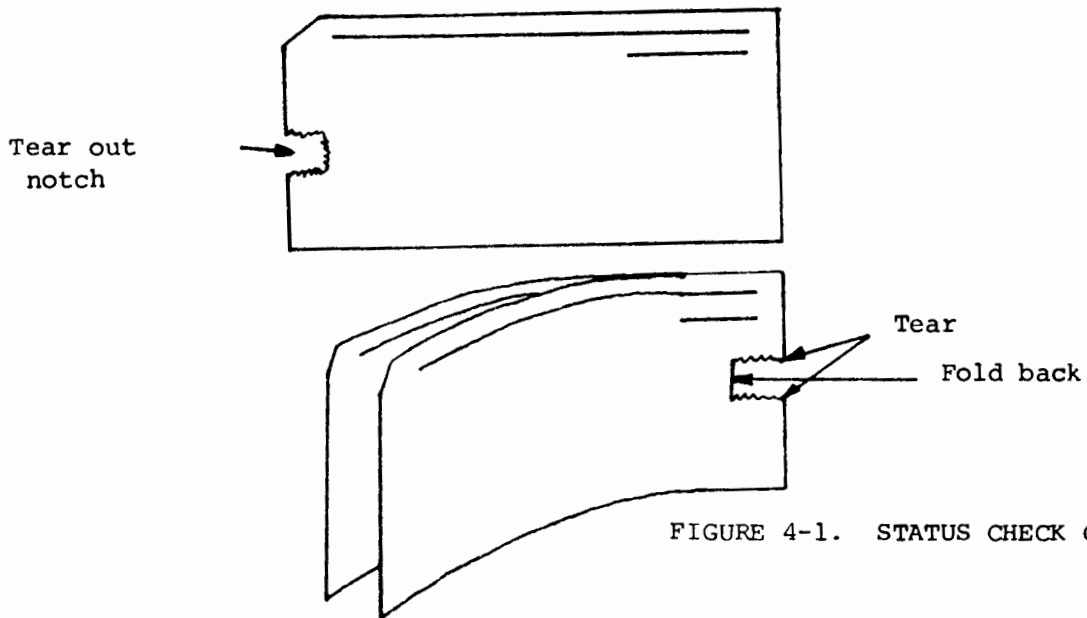


FIGURE 4-1. STATUS CHECK CARDS

The following sequence is used to check status.

(CR = card reader). Step numbers are in octal and correspond to Status Error halts if octal 30 is added. For status test, operator instructions must be followed exactly.

1. Turn CR power off .

- A. OFF-LINE = 0 (BIT 2)
- B. "NOT" READY = 1 (BIT 0)



2. Turn CR power on
  - A. OFF-LINE =  $\emptyset$  (BIT 2)
  - B. "NOT" READY = 1 (BIT  $\emptyset$ )
3. Give PICK command (STC CR,C).
  - A. PICK = 1 (BIT 8)
  - B. RIP = 1 (BIT 12)
  - C. EOP =  $\emptyset$  (BIT 15)
4. Put CR in OFF-LINE mode
  - A. OFF-LINE = 1 (BIT 2)
  - B. PICK =  $\emptyset$  (reset by OFF-LINE) (BIT 8)
  - C. EOP = 1 (BIT 15)
  - D. "NOT" READY =  $\emptyset$  (BIT  $\emptyset$ )
  - E. RIP = 1 (BIT 12)
  - F. FLAG SET BY OFF-LINE and PICK
5. Give PICK command (STC CR,C when in OFF-LINE).
  - A. PICK =  $\emptyset$  (prevented by OFF-LINE) (BIT 8)
  - B. RIP = 1 (BIT 12)
  - C. EOP = 1 (BIT 15)
6. Put CR in ON-LINE mode. Load three cards. Start CR.
  - A. OFF-LINE TO ON-LINE           
SETS FLAT WHEN CONTROL SET AND RIP = 1
  - B. All bits indicate ready
7. Extend Stacker Arm and hold (should cause STOP).
  - A. "NOT" Ready = 1 (BIT  $\emptyset$ )
  - B. STACKER FULL = 1 (BITS 5 & 6)
10. Give PICK command (STC CR,C).
 

(now CLC CR,C clears PICK)

  - A. PICK =  $\emptyset$
11. Release Stacker Arm and Start CR.
  - A. ALL BITS INDICATE READY
12. Pick two cards (STC CR,C).
  - A. CHECK LOST DATA (BIT 3)  
(NO LIA during read)
  - B. CHECK LOST DATA (BIT 3)  
(OTA but no LIA)

13. Press END-OF-FILE
  - A. END-OF-FILE = 1 (BIT 7)
  - B. HOPPER EMPTY = 1 (BIT 5)
  
14. Load two half cards in the STACKER and two standard cards in the HOPPER. Press START on CR.
  - A. ALL BITS INDICATE READY
  
15. Pick card (First interrupt GENERATE CRS) .
  - A.  $\overline{\text{RIP}} = 1$  (Bit 12)
  - B. EOP = 1 (BIT 15)
  - C. PICK =  $\emptyset$  (BIT 8)
  
16. Pick card
  - A. TROUBLE = 1 (BIT 1)
  - B. MOTION/PICK = 1 (BIT 11)
  
17. Load NOTCHED card. Press START on CR. Press RUN.
  - A. ALL BITS INDICATE READY
  
20. Pick the card
  - A. TROUBLE = 1 (BIT 1)
  - B. ERROR L/D = 1 (BIT 9)
  
21. Load two cards taped together. Press START on CR. Press RUN.
  - A. ALL BITS INDICATE READY
  
22. Pick the card
  - A. TROUBLE = 1 (BIT 1)
  - B. MOTION/PICK = 1 (BIT 11)

4-4. TIMING TESTS

This test requires 10 cards be placed in the CR. The program will pick each card and verify the timing on each (all data is ignored). The timing checks are as follows:

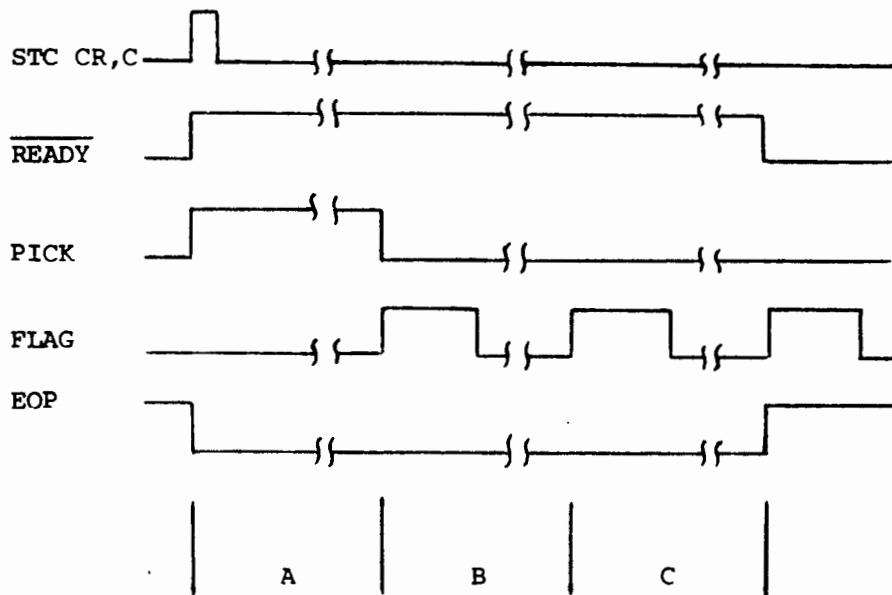


FIGURE 4-2 Card Reader Timing Chart

- A. Normal 24 to 27 milliseconds (time from pick to first int.) If greater than 27 but less than 40 then possible picker trouble. If over 40 but less than 300 then more than one pick attempt. If over 300, status should indicate pick failure. Maximum allowance is 1 second then no EOP is assumed.
- B. Normal 870  $\mu$ sec (time between data). If greater than 1 millisecond, the CR is in error and a message is output to the operator.
- C. Normal 3480  $\mu$ sec (time from last data to EOP). If greater than 4 milliseconds the CR is in error and a message is output to the operator.

During the above checks the number of flags received is also checked to insure 80 Data Columns have been read for each card. Any data is ignored.

#### 4-5. DATA PATTERN TEST

This checks a worst case data pattern. The cards are supplied with the Card Reader and have the worst case pattern prepunched. There will be 50 cards read and the data verified.

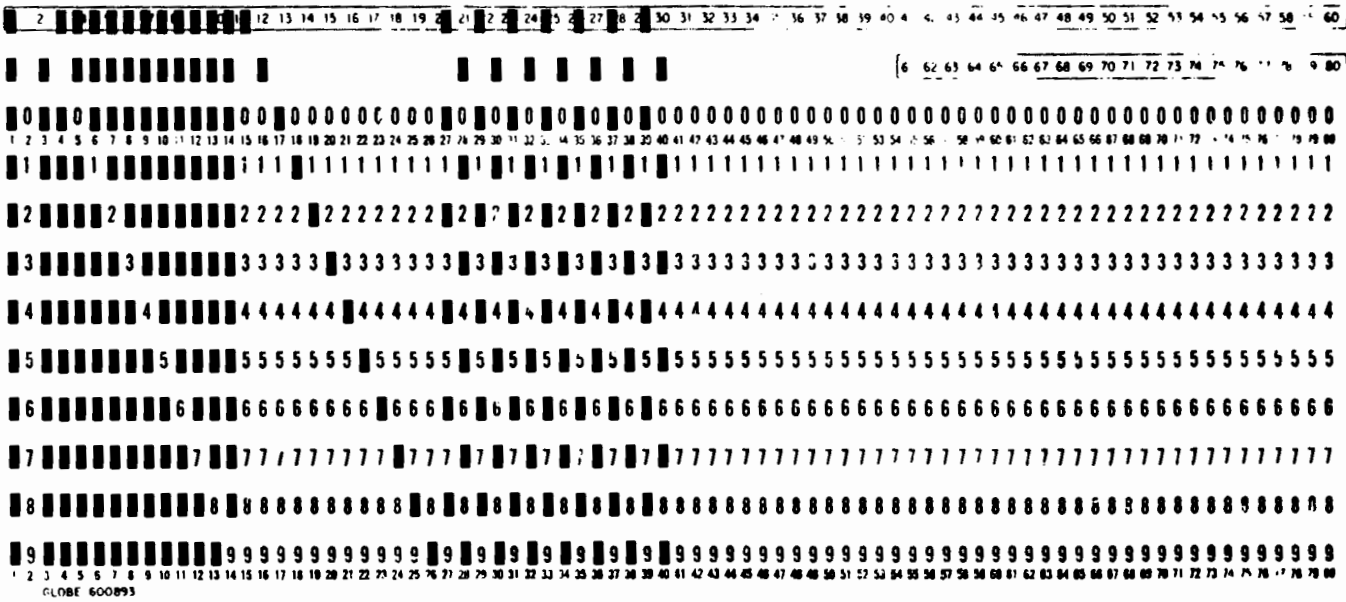


FIGURE 4-3. Worst Case Data Pattern Card

4-6. READ RATE TEST

This will read 50 cards and from that determine the cards-per-minute read rate. This reading is only accurate to +5 cards per minute if a TBG is not specified during configuration. A variation of a few cards per minute can be expected between old and new cards, how full the hopper is, if the cards are bent, etc. The CPR reading will be output to the console device if available or a halt with the A-register equal to the octal representation of the number.

4-7. DMA TRANSFER TEST

In this test, the program reads the same 50 cards as the Data Pattern test except using the DMA portion of the computer and interface card. The test will only be executed if DMA is available.

4-8. ERROR INFORMATION MESSAGES AND HALT CODES

Table 4-1 summarizes the diagnostic halt codes and table 4-2 defines the card reader status bits.

Table 4-1. Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
102073	Configuration	None	I/O select code entered at configuration invalid. Must be greater than 7 <sub>8</sub> . Re-enter a valid select code and press RUN.
102074	Configuration	None	Select code entered during configuration valid. Enter program option bits in switch register and press RUN.
102075	Test Control	None	Test selection request resulting from switch register bit 9 being set. Enter in A/B-registers the desired group of tests to be executed and press RUN.
102076 A REG = TEST NUMBER	Test Control	None	End of test halt resulting from switch register bit 15 being set (A-register has the test number). To continue press RUN.
102077 A REG = PASS COUNT	Test Control	PASS XXXXXX	Diagnostic run complete. Register options may be changed. To continue press RUN
106077	Test Control	None	Halt stored in location 2-77 <sub>8</sub> to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot which interrupted. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.
102000	Test 0	E000 CLF 0-SFC 0 ERROR	CLF/SFC 0 combination failed. CLF did not clear flag or SFC caused no skip with flag clear.



Table 4-1. Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
102001	Test 0	E001 CLF 0-SFS 0 ERROR	CLF/SFS 0 combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102002	Test 0	E002 STF 0-SFC 0 ERROR	STF/SFC 0 combination failed. STF did not set flag or SFC caused skip with flag set.
102003	Test 0	E003 STF 0-SFS 0 ERROR	STF/SFS 0 combination failed. STF did not set flag or SFS caused no skip with flag set.
102004	Test 0	E004 CLF 0 DID NOT INHIBIT INT	With card flag and control set, CLF 0 did not turn off interrupt system.
102005	Test 0	E005 CLF CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102006	Test 0	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102007	Test 0	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set flag or SFC caused skip with flag set.
102010	Test 0	E010 STF CH-SFS CH ERROR	STF/SFS CH combination failed. STF did not see flag or SFS caused no skip with flag set.
102011 AREG = XX <sub>8</sub>	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. XX = select code that caused that card flag to set.
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.

Table 4-1. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102013	Test 0	E013 SECOND INT OCCURRED	Interface interrupted a second time after initial interrupt was processed
102014	Test 0	E014 NO INT	No interrupt occurred with interface flag and control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0	E016 CLC CH ERROR	CLC CH did not clear interface control with the interrupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear control with the interrupt system on.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the interface flag.
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I/O LINES	PRESET (EXT) did not clear I/O data lines.
102024	Test 0	H024 PRESS PRESET (EXT & INT), RUN	Press PRESET (External, Internal), RUN.
NONE	Test 0	H025 BI-O COMP	Basic I/O Tests completed
102026	Test 0	E026 INT EXECUTION ERROR	Interrupt was not processed correctly.
NONE	Test Control	2892A CARD READER DIAGNOSTIC	Introductory message.

Table 4-1 Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
NONE	Test Control	TEST XX	Information message before error message (XX = test number). Message occurs only once within a test but is suppressed for any subsequent messages within the same test.
102030	Test 1	E030 CR TIMED OUT	The card reader failed to respond to a pick command. Refer to Status test steps 12, 13, 16 and 20.
102031	Test 1	E031 STATUS IS XXXXXX AND EXPECTED 110001	Refer to Status test Step 1. A = Current Status B = Expected Status
102032	Test 1	E032 STATUS IS XXXXXX AND EXPECTED 110041	Refer to Status test Step 2 A = Current Status B = Expected Status
102033	Test 1	E033 STATUS IS XXXXXX AND EXPECTED 010441	Refer to Status test Step 3. A = Current Status B = Expected Status
102034	Test 1	E034 STATUS IS XXXXXX AND EXPECTED 110045	Refer to Status test Step 4. A = Current Status B = Expected Status
102035	Test 1	E035 STATUS IS XXXXXX AND EXPECTED 11045	Refer to Status test Step 5 A = Current Status B = Expected Status
102036	Test 1	E036 STATUS IS XXXXXX AND EXPECTED 110000	Refer to Status Report Step 6 A = Current Status B = Expected Status
102037	Test 1	E037 STATUS IS XXXXXX AND EXPECTED 110141	Refer to Status test Step 7 A = Current Status B = Expected Status
102040	Test 1	E040 STATUS IS XXXXXX AND EXPECTED 010141	Refer to Status test Step 10 A = Current Status B = Expected Status
102041	Test 1	E041 STATUS IS XXXXXX AND EXPECTED 010000	Refer to Status test Step 11 A = Current Status B = Expected Status



Table 4-1 Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102042	Test 1	E042 STATUS IS XXXXXX AND EXPECTED 110012	Refer to Status test Step 12 A = Current Status B = Expected Status
102043	Test 1	E043 STATUS IS XXXXXX AND EXPECTED 110241	Refer to Status test Step 13. A = Current Status B = Expected Status
102044	Test 1	E044 STATUS IS XXXXXX AND EXPECTED 110000	Refer to Status test Step 14. A = Current Status B = Expected Status
102045	Test 1	E045 STATUS IS XXXXXX AND EXPECTED 110001	Refer to Status test Step 15. A = Current Status B = Expected Status
102046	Test 1	E046 STATUS IS XXXXXX AND EXPECTED 114043	Refer to Status test Step 16. A = Current Status B = Expected Status
102047	Test 1	E047 STATUS IS XXXXXX AND EXPECTED 110000	Refer to Status test Step 17. A = Current Status B = Expected Status
102050	Test 1	E050 STATUS IS XXXXXX AND EXPECTED 111043	Refer to Status test Step 20. A = Current Status B = Expected Status
102051	Test 1	E051 STATUS IS XXXXXX AND EXPECTED 110000	Refer to Status test Step 21. A = Current Status B = Expected Status
102052	Test 1	E052 STATUS IS XXXXXX AND EXPECTED 114003	Refer to Status test Step 22. A = Current Status B = Expected Status
102053	Test 1	E053 FLAG NOT SET OFF-LINE + PICK	Refer to Status test Step 4.
102054	Test 1	E054 FLAG NOT SET OFF-TO-ON LINE	Refer to Status test Step 6.
102055	Test 2-6	E055 CR NOT READY	The Card Reader was found not ready by checking bit 0=0. The Card Reader can be made ready and RUN.

Table 4-1 Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102056	Test 2	E056 EOP BUT NO INTERRUPT	pressed. If the program still finds the Card Reader not ready the test is aborted.  A pick command was given to the CR but no interrupt occurred after 1 second. When checking status EOP was found high which indicates an interrupt should have occurred.
102057	Test 2	E057 NO EOP AFTER PICK	After giving a pick command no interrupt occurred and checking status indicated EOP=0.
102060	Test 2	E060 PICK FAILURE	Card Reader failed to pick card.
102061	Test 2	E061 PICK TO INT OVER 300 MS	Refer to Timing test Part A.
102062	Test 2	E062 POSSIBLE PICKER TROUBLE	Refer to Timing test Part A.
102063	Test 2	E063 EOP BEFORE 80 COLUMNS	During Timing test EOP occurred before all 80 columns had been checked.
102064	Test 2	E064 TIME BETWEEN DATA OVER 1MS	Refer to Timing test Part B.
102065	Test 2	E065 80 COLUMNS BUT NO EOP	The full 80 columns were read but no EOP occurred within 1 second after the last data column.
102066	Test 2	E066 DATA TO EOP OVER 4 MS	Refer to Timing test Part C.
102067	Test 2	E067 INT TIME OUT DURING READ	More than 1 second elapsed between data columns.
106000	Test 1	H100 TURN CR POWER OFF AND REMOVE ANY CARDS	
106001	Test 1	H101 TURN CR POWER ON	

Table 4-1 Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
106002	Test 1	H103 PUT CR ON-LINE LOAD THREE CARDS START CR	
106004	Test 1	H104 EXTEND STOCKER ARM AND HOLD	
106005	Test 1	H105 RELEASE STACKER ARM START CR	
106006	Test 1	H106 PRESS CR END-OF-FILE	
106007	Test 1	H107 LOAD SHORT CARDS AND TWO LONG CARDS START CR	Two short cards in stacker and long cards in hopper.
106010	Test 1	H110 LOAD NOTCHED CARD START CR	
106011	Test 1	H111 LOAD 2 CARDS HOOKED TOGETHER	
106012	Test 2	H112 LOAD TEN CARDS FOR TIMING TEST AND START CR	
106013	Test 3	H113 LOAD 50 CARDS FOR DATA PATTERN CHECK START CR	
106014	Test 4	H114 LOAD 50 CARDS FOR READ RATE AND START CR	
106015	Test 4	H115 XXX CARDS PER MINUTE	xxx = The calculated number of cards read per minute.
106016	Test 5	H116 LOAD 50 CARDS FOR DMA TEST START CR	
106017	Test 6	H117 PSEUDO OPDESIGN	Operator may make switch register function selection then press RUN.
NONE	Test 6	H120 STATUS IS XXXXXX	Operator selected switch register bit 6 during Pseudo Opdesign.
106021	Test 6	H121 BUFFER LIST	Operator selected switch register bit 4 during Pseudo Opdesign. A read buffer list will follow, the columns.

Table 4-1 Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
106030	Test 3,6	E130 CR TIMED OUT	are represented 1-20, 21-40, 41-60 and 61-80. During a read operation the card reader failed to respond within 1 sec.
106031	Test 3,6	E131 EOP BEFORE 80 COLUMNS	During a read operation EOP (bit 15) went high before all 80 columns were read.
106032	Test 3,6	E132 DATA ERROR ACT XXXX EXP YYYY	Data read from card reader did not compare with standard data table. When halted A-reg = XXXX and B reg = YYYY
106033	Test 4	E133 CR TIMED OUT	During the read rate that the card reader did not respond.
106034	Test 5	E134 CR NOT READY	During the read rate test the card reader went not ready.
106035	Test 5	E135 DMA TIMED OUT	After starting DMA and giving a pick command there was no response from either DMA or the Card Reader interface.
106036	Test 5	E136 DMA TRANSFER	After a DMA transfer, the count left in DMA register was not 5. DMA is asked to transfer 85 data words and therefore should not complete and have a count of 5 left when good transfer takes place. (A=DMA COUNT-LIA 2)
106037	Test 5	E137 NO EOP AFTER DMA TRANSFER	After a DMA bit 15 (EOP) of the interface was low and should be high.
106040	Test 5	E140 DMA COMPLETED BEFORE CR	More than 85 data words were transferred to DMA without EOP occurring.

Table 4-2. Card Reader Status Bits

BIT	MEANING IF SET
0	Card Reader not ready or off-line.
1	Trouble during read    a. Card motion b. Light/Dark error c. Data loss
2	Card Reader is Off-Line
3	Data lost                    a. Missed an LIA or LIB b. OTA or OTB but no LIA or LIB during read
4	Not used
5	Hopper Empty or Stacker Full
6	Stacker Full
7	End-of-File and Hopper Empty
8	Pick. STC was issued but first column has not been read
9	Light/Dark check error
10	Not used
11	Motion/Pick Check
12	"NOT" Read in Progress ( $\overline{\text{RIP}}$ ). Card Reader is not reading a card
13	
14	
15	End-of-Operation            a. Power on or preset b. Went Off-Line when Pick = 1 c. Data read complete d. Reader failed to read within 875 $\pm 150$ mit/sec.