HP 13255

PROCESSOR (8008-1) MODULE

Manual Part No. 13255-91008

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AUG-01-76

NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

This module uses the Intel 8008-1 microprocessor as the central controlling element in the terminal. The processor fetches and executes instructions which are stored in the terminal's memory modules.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Processor (8008-1) Module is contained in tables 1.0 through 5.1.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60008	Processor (8008-1) PCA	12.5 x 4.0 x 0.5	6.31

Number of Backplane Slots Required: 1

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Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.005 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 400 mA	@ 005 mA	@ 075 mA	@ mA
			NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz +/- 0.1%

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19		} Not
-20		} Used
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 4.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		} Not
-C		} Used
-D	PWR ON	System Power On
-E	BUS0	Negative True, Data Bus Bit 0
-F	BUS1	Negative True, Data Bus Bit 1
-H	BUS2	Negative True, Data Bus Bit 2
-J	BUS3	Negative True, Data Bus Bit 3
-K	BUS4	Negative True, Data Bus Bit 4
-L	BUS5	Negative True, Data Bus Bit 5
-M	BUS6	Negative True, Data Bus Bit 6
-N	BUS7	Negative True, Data Bus Bit 7
-P	WRITE	Negative True, Write/Read Type Cycle
-R		} Not
-S		} Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	PROC ACTVE	Negative True, Processor Active (Controlling Bus)
-W	BUSY	Negative True, Bus Currently Busy (Not Available)
-X	RUN	Allow Processor to Access Bus
-Y	REQ	Negative True, Request (Bus Data Currently Valid)
-Z	ATN	Negative True, Data Comm Interrupt Request

Table 5.0 Module Bus Pin Functions for Input Instructions

Module Address: (ADDR 11,10,9,4) = (M2,M1,M0,A4)

During an input instruction the upper byte of the address register is loaded with the input instruction and the lower byte, with the contents of the accumulator just prior to the execution of the input instruction. ADDR4 is controlled by bit 4 of the accumulator. The other seven bits may be used by the IO module for strobes.

M2 M1 M0 = Module address from input instruction (INP)

A4 = Controlled by program; set by contents of bit 4 in accumulator before input instruction is executed

A4 = 1 Modules 1,3,5,7,11,13,15,17 (octal)

A4 = 0 Modules 0,2,4,6,10,12,14,16 (octal)

Value	Bus Signal
0	ADDR 15
0	ADDR 14
0	ADDR 13
0	ADDR 12
M2	ADDR 11
M1	ADDR 10
M0	ADDR 9
1	ADDR 8
A7	ADDR 7
A6	ADDR 6
A5	ADDR 5
A4	ADDR 4
A3	ADDR 3
A2	ADDR 2
A1	ADDR 1
A0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Data Bus Bit Interpretation:

B7 - B0 Data from terminal bus is loaded into accumulator (A-register) of microprocessor.

Table 5.1 Module Bus Pin Functions for Output Instructions

Module Address: (ADDR 11,10,9,4) = (M2,M1,M0,R1)

During an output instruction, the instruction itself is loaded into the upper and lower bytes of the address register. The format of the output instruction determines which module is addressed.

M2 M1 M0 = Module address from output instruction (OUT)

R2 R1 - 01} ADDR4 = 1 Modules 1,3,5,7,11,13,
11} 15,17 (octal)

R2 R1 - 10} ADDR4 = 0 Modules 0,2,4,6,10,12,
14,16 (octal)

R2 R1 - 00} Cannot be generated from processor

Data Bus Bit Interpretation:

B7 - B0 Contents of accumulator (A-register) are gated to the terminal bus.

Value	Bus Signal
0	ADDR 15
0	ADDR 14
R2	ADDR 13
R1	ADDR 12
M2	ADDR 11
M1	ADDR 10
M0	ADDR 9
1	ADDR 8
0	ADDR 7
1	ADDR 6
R2	ADDR 5
R1	ADDR 4
M2	ADDR 3
M1	ADDR 2
M0	ADDR 1
1	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagrams (figures 3 and 4), component location diagram (figure 5), and parts list (02640-60008) located in the appendix.

The Processor (8008-1) Module consists of the following functional groups: microprocessor, clock generator, processor state decoder logic, bus cycle logic, data register, upper and lower byte address registers, interrupt logic, and restart logic.

3.1 MICROPROCESSOR.

3.1.1 The 8008-1 microprocessor is an 8-bit central processing unit which is implemented on a single LSI integrated circuit. The microprocessor chip has a basic 8-bit architecture internally with an accumulator, six registers, a program counter, and a subroutine return address stack (allowing seven levels of subroutines).

3.1.2 The microprocessor (U31) has 48 different instruction types of one, two, or three bytes per instruction. It has only one 8-bit input/output bus which is multiplexed between data and address information by the state outputs. The chip requires two phase clocks and has a basic cycle time of 2.8 microseconds (two periods of the phase clocks). The microprocessor has an addressing range of 16,384 bytes (14 bits).

3.1.2.1 Processor signals. The microprocessor has eighteen pins including two for power, +5 volts (Pin 10) and -9 volts (Pin 1). Eight pins comprise the bidirectional bus (Pins 2 through 9) which is used for data and address output and data input. Three output signals S2 (Pin 11), S1 (Pin 12), and S0 (Pin 13) encode processor state information which is used to control the other logic elements of the Processor (8008-1) Module. Two inputs (Pins 15 and 16) are used for the two phase clocks. The microprocessor provides an output called SYNC (Pin 18) which is used with the clocks to define a basic microprocessor cycle (T-cycle). The remaining signals are inputs READY (Pin 17) and INTERRUPT (Pin 18). READY is used to synchronize the microprocessor with the terminal bus and INTERRUPT is used to start the microprocessor during a power on or reset sequence.

3.1.2.2 Processor bus. The microprocessor bus is multiplexed, under control of the state outputs, for lower and upper address byte out, instruction fetch, and data in or out of the processor. The direction of data flow is determined by control information available when the upper address byte is output during microprocessor state T2.

Open-collector inverting buffers (U33 and U43) gate information from the terminal bus when DATA IN STROBE (U13, Pin 6) is high. Inverters (U32 and U42) buffer the data output from the microprocessor, since the output drive is limited. The pull-up resistor network (R2) and transistor (Q1) provide input drive current for the buffers (U33 and U43) and are disabled during output operations (decreasing the input current).

3.1.2.3 Processor states. The state outputs S2, S1, and S0 encode eight microprocessor states as illustrated below. These states are one T-cycle (or 2.8 microseconds) and indicate to the module processor state decoder logic what the processor is doing. States T1 and T2 are used to output lower and upper address bytes. State T3 is instruction fetch or data in or out and states T4 and T5 are used to execute instructions. Wait is a special state entered when the READY line is not high in time for the microprocessor to enter the T3 state. This allows the Processor Module to synchronize with the terminal bus and perform single step operations during program development. State T1I is a special Interrupt state which is entered only when a halt instruction is executed. Stopped is the processor state entered after a halt instruction and is used to force the module into a power on sequence to prevent the microprocessor from dying unexpectedly. (Refer to figure 3 for processor state timing information.)

8008-1 PROCESSOR STATES

S2	S1	S0	NAME	COMMENTS
0	1	0	T1	Lower eight bits of address out of processor
0	0	1	T2	Upper six bits of address and two control bits
0	0	0	Wait	If bus not ready processor will stay in this state
1	0	0	T3	Instruction or data in or out of the processor
1	1	1	T4	Instruction execution
1	0	1	T5	Instruction execution
0	1	0	T1I	Interrupt state, used to start processor
1	1	0	Stopped	Entered after halt instruction causes power on sequence

3.1.2.4 Instruction set. The microprocessor has 48 different instruction codes which can be one, two, or three bytes long. Each instruction begins with a memory read to fetch the first byte. If the instruction decoded is one byte only, it is executed in states T4 and T5. If more bytes are needed to complete the instruction, they are read during succeeding memory cycles. Instructions can be from 3 to 11 microprocessor states (each 2.8 microseconds) plus any additional wait states. Several instruction codes (restart, input/output, and halt) require special handling. The halt instruction should not be used because it will cause a power on sequence to occur, thus causing the microprocessor to begin executing instructions at memory location zero.

3.1.2.5 Input/output instructions. (See tables 5.0 and 5.1) The input and output instructions are special cases in that the upper and lower byte address registers hold different information than when a memory read or write is performed. When an output instruction is executed, the upper byte address register (U36 and U46) and lower byte address register (U35 and U45) both contain the output instruction when the address information is gated to the bus. During an input instruction, the upper address byte contains the input instruction and the lower byte contains the contents of the accumulator just prior to the input instruction fetch. Address information for input/output is then decoded by the modules on the bus and output data from the processor's accumulator register is received by the addressed module or data from an addressed module is loaded into the processor's accumulator register.

3.1.2.6 Restart instruction. The special use of the restart instruction is described in section 3.9. The microprocessor executes a subroutine call when it receives a restart instruction and the bus signal $\overline{\text{ATN}}$ is low causing a subroutine call to one of eight predefined locations as encoded in the Restart instruction.

3.2 CLOCK GENERATOR.

3.2.1 The clock generator provides the required two phase clocks to the 8008-1 microprocessor. The two phase clocks are derived from the terminal bus system clock by dividing the system clock down with a counter. Additional timing information is generated using the SYNC output (U31, Pin 18).

3.2.2 The basic microprocessor timing cycle is two periods of the phase clocks (each 1.4 microseconds) for a machine state of 2.8 microseconds. Each phase of the clocks will occur during a T-cycle. Each instruction is made up of three or more machine states, which determines the time that a particular instruction will take. The microprocessor clock and processor state decoder outputs determine the control and timing necessary for the various module functions.

3.2.2.1 Counter. The basic clock timing period is produced by a 4-bit counter (U41) which counts seven periods and then is preset at Pin 1 to redo the sequence (1, 2, 3, 4, 5, 6, 7, with state 8 causing a preset). Two AND gates (U51, Pins 11 and 8) decode the counter states and produce microprocessor clock PHASE 1 and PHASE 2.

3.2.2.2 SYNC flip-flop. The microprocessor SYNC output signal (Pin 14) goes high at the beginning of a processor T-cycle and goes low at the midpoint of the cycle, as shown in the clock generator timing diagram in figure 4. Flip-flop U210 at Pin 8 latches SYNC on the PHASE 2 fall edge. The SYNC flip-flop outputs generate two additional signals, PHASE 11 (U15, Pin 11) and PHASE 12 (U16, Pin 11). These signals provide timing information to the rest of the Processor (8008-1) Module.

3.2.2.3 READY. The READY line at Pin 17 is used to synchronize the microprocessor with the terminal bus. Flip-flop U110 at Pin 9 holds this information. If READY is not high by PHASE 12 of state T2, then the microprocessor will enter the Wait state until READY does go high again, thus allowing the microprocessor to enter state T3.

3.3 PROCESSOR STATE DECODER.

3.3.1 The processor state decoder controls the Processor (8008-1) Module by decoding microprocessor states. The state decoder controls address and data, in and out of the microprocessor.

3.3.2 The processor state decoder receives three outputs from the microprocessor which have state information encoded. This state information tells what the 8-bit bus is being used for (data in or out, or address upper or lower out) or if the microprocessor is in a special state such as Wait or Stopped. The outputs of the processor state decoder logic control other module functions.

3.3.2.1 State decoder. The microprocessor has three encoded state outputs (U31, Pins 13, 12, and 11) which are decoded by a one-of-eight decoder (U22). The three inputs encode the eight microprocessor states, which decode as eight outputs (U22, Pins 7, and 9 through 15). The outputs of the decoder indicate when the microprocessor is in a particular state (low output). The only states not used in controlling Processor (8008) Module functions are states T4 and T5 which are instruction execution cycles.

3.3.2.2 Address register clocks. The processor state decoder logic uses the outputs of the decoder and the PHASE 12 clock to strobe data into the upper (U46 and U36) and lower (U45 and U35) byte address registers. The registers have clock and data enable inputs (Pins 7 and 9) which control the address inputs. The upper byte address registers have $\overline{\text{WRITE}}$ (Pin 14), $\overline{\text{I/O}}$ (Pin 13), and address inputs clocked in during state T2 and on the rising edge of PHASE 12. The lower byte address register has address inputs clocked in ($\overline{\text{LOWER CLOCK}}$) at U13, Pin 11 during state T1 of all except output instructions and during state T2 of output instructions. The four registers all have PHASE 12 at Pin 7 as the input clock which is buffered by a gate at U13, Pin 8. The upper byte address register receives two control bits which represent $\overline{\text{WRITE}}$ and $\overline{\text{I/O}}$ on the bus. $\overline{\text{I/O}}$ is derived by decoding BIT7 and BIT6 of the upper address byte out of the processor during state T2. $\overline{\text{WRITE}}$ is derived by decoding an input instruction or a write command from the two control bits of processor state T2.

3.3.2.3 Data register clocking. The processor state decoder logic also controls the data register (U34 and U44). Data from the microprocessor is clocked into the data register on the rising edge of PHASE 12 Clock (U34 and U44, Pin 7) during state T3 of all (except I/O instructions) and during state T1 of an output instruction. Data is gated onto the bus during write cycles when $\overline{\text{DATA OUT}}$ (U15, Pin 6) is low. Another signal, DATA IN STROBE (U13, Pin 6) is provided by the processor state decoder logic to enable data from the terminal bus during read or input instructions. DATA IN STROBE controls the direction of data on the 8-bit processor bus and enables the current switch (Q1) so that resistor R2 can act as a pull-up to buffers U43 and U44.

3.4 BUS CYCLE LOGIC.

3.4.1 The bus cycle logic controls the microprocessor's access to the terminal bus, controls gating of data and address onto the bus, and controls $\overline{REQ}$ and $\overline{PROC\ ACTIVE}$ signals for the module. The RUN signal from the bus determines if the bus cycle will be allowed to begin, which enables halting the processor temporarily or single stepping during development of programs.

3.4.2 A bus access is begun during processor state T2 and ended during state T3 for (reads or inputs) and (during write or output). If the terminal bus is not obtained and ready before state T3, the processor will enter a Wait state by following its READY input (U31, Pin 17).

3.4.2.1 Bus cycle states. The three J-K flip-flops labled "C" (U410, Pin 6), "D" (U410, Pin 8), and "E" (U310, Pin 6) implement a 6-state counter which times the terminal bus access. The six bus cycle states are summarized below. The Idle state is in effect when no bus cycle is needed. Bus Bid is the state which begins a bus cycle. Bus Obtained is the state where the Processor (8008-1) Module gains control of the bus, makes $\overline{BUSY}$ low, and gates data and address to the terminal bus. The Request state actually performs the data transfer on the bus and Access Complete is the state which begins the last three states. The Release State is followed by Idle and the Processor (8008-1) Module has then completed the terminal bus cycle.

BUS CYCLE LOGIC

FF C	FF D	FF E	NAME	COMMENTS
0	0	0	Idle	Processor does not require terminal bus
1	0	0	Bus Bid	Begin terminal bus access (during T2 and RUN is high)
1	1	0	Bus Obtained	Processor (8008-1) Module has control of terminal bus
1	1	1	Request	$\overline{REQ}$ made true (data & address gate out during Bus Obtained)
0	1	1	Access Complete	Begin process of releasing bus, $\overline{REQ}$ off
0	0	1	Release	Processor (8008-1) Module gives up bus and goes to Idle

3.4.2.2 Bus cycle start. A bus cycle is begun when the T2 state is entered (or wait if bus is not ready) and the RUN line is high. This sets flip-flop "C" which makes the state counter go from Idle to Bus Bid. The PRIOR OUT signal is disabled at U47, Pin 6 and then waits until the PRIOR IN signal is high and the bus is not available. Flip-flop "D" is set at U48, Pin 12 putting the module in the Bus Obtained state, and making the bus busy by making $\overline{BUSY}$ at U38, Pin 3 low.

3.4.2.3 When the module is in the Bus Obtained state it gates address and data to the bus and makes $\overline{PROC\ ACTIVE}$ true. The bus cycle logic stays in the Bus Obtained state until REQUEST START at U18, Pin 6 goes high. This will set flip-flop "E" and put the state counter in the Request state. The module then makes $\overline{REQ}$ (U38, Pin 6) low which will begin the bus operation. The state counter will stay in the Request state until flip-flop "C" is reset by the REQUEST STOP signal at U18, Pin 3.

3.4.2.4 Bus cycle end. The bus cycle state counter enters the Access Complete state when flip-flop "C" is reset by REQUEST STOP and flip-flop "E" being set (Request state). REQUEST STOP is high when a write is in progress at PHASE 11 and when a read is in progress at PHASE 12 of processor state T3 (Refer again to figure 3 for processor state timing information). After flip-flop "C" is reset, the bus cycle logic goes to the Release state ($\overline{REQ}$ is brought high) and then to the Idle state with flip-flops "D" and "E" being reset on the next two clocks. The state counter is in the Idle state and the bus has been released.

3.5 DATA REGISTER.

3.5.1 The data register holds data from the microprocessor during writes to memory or during output instructions. The data comes out of the microprocessor on the 8-bit microprocessor bus and is clocked into the data register. The data register is a 3-state latch and is gated onto the terminal data bus by the processor state decoder logic during a write or output.

3.5.2 The data registers (U34 and U44) hold the 8-bit output from the microprocessor bus which is buffered by inverters (U32 and U42). Data is clocked into the registers on the rising edge of PHASE 12 during processor state T3 of all writes (except I/O) and during state T1 for

output instructions. The data registers are normally in the off condition and the data registers are not enabled. During data write or output, however, the data registers are enabled and drive the bus. The $\overline{\text{DATA OUT}}$, signal at U15, Pin 6 enables data out when U15, Pin 3 and U18, Pin 8 are true.

3.6 UPPER BYTE ADDRESS REGISTER.

3.6.1 Two 3-state latches (U46 and U36) make up the upper byte address register and receive address inputs from the microprocessor bus during processor state T2.

3.6.2 For a memory read or write, the register will hold the most significant six bits ($\overline{\text{ADDR13}}$ thru $\overline{\text{ADDR8}}$) and two bits of control ($\overline{\text{WRITE}}$ and $\overline{\text{I/O}}$). The two control bits are encoded from the processor bus BIT7 and BIT6 and are loaded into the upper byte address register (U46) at Pins 13 and 14. During an I/O instruction, the instruction itself, is loaded into the upper byte address register and is used to address I/O modules. The clock and enable signals for the registers are provided by the processor state decoder logic. Address information from the registers is gated to the terminal bus when $\overline{\text{PROC ACTIVE}}$ is high.

3.7 LOWER BYTE ADDRESS REGISTER.

3.7.1 Two 3-state latches (U45 and U35) make up the lower byte address register and receive address inputs from the microprocessor bus during processor state T1 (for memory access or an input instruction) and during state T2 (for an output instruction).

3.7.2 The lower byte address register will contain the least significant eight bits of a memory address for a read or write. During an input instruction, the registers will hold the contents of the microprocessor accumulator (A-register) prior to fetching the input instruction. During an output instruction, the register will hold the output instruction itself, which is sent out from the microprocessor during state T2 of the instruction execution. The registers receive clock and enable signals (U45 and U35, Pins 7 and 9) from the processor state decoder logic. Address information in the registers is gated to the terminal bus when $\overline{\text{PROC ACTIVE}}$ is true.

3.8 INTERRUPT LOGIC.

3.8.1 The interrupt logic ensures that the microprocessor initializes correctly during power on or reset. This logic also detects the microprocessor Stopped state and performs a reset function to ensure that the microprocessor does not remain halted. The start-up function is performed by forcing a special 1-byte instruction into the microprocessor which causes the processor to begin executing instructions at location zero. This special instruction is called a restart.

3.8.2 The interrupt logic consists of two J-K flip-flops, flip-flop "A" (U210, Pin 6) and flip-flop "B" (U310, Pin 8) which implement a counter. The following is a summary of the states and their meanings.

FF A	FF B	State Name	Comments
0	0	Begin Interrupt	Either power on, reset or halt
1	0	Interrupt	Cause processor to enter T1I
1	1	Restart Fetch	Gate Restart to microprocessor
0	1	Interrupts Off	Sequence complete - go to Begin Interrupt if halted or reset

3.8.2.1 The interrupt logic state counter starts when PWR ON at U210, Pin 4 and U310, Pin 10 resets the two flip-flops which puts the state counter in the Begin Interrupt state. The state counter will go to the Interrupt state on the next PHASE 12 clock and make the microprocessor INTERRUPT signal (U39, Pin 8) true. When the microprocessor enters the T1I state, the interrupt logic goes to the Restart Fetch state at U39, Pin 11 and causes the input buffers (U33 and U34) to force a restart instruction into the microprocessor. Two bus drivers (U38, Pins 8 and 11) are enabled by RESTART and PROC ACTIVE and cause $\overline{\text{BUS2}}$ and $\overline{\text{BUS0}}$ to be changed to "1's" during the fetch. During the fetch of the restart instruction $\overline{\text{REQ}}$ is not enabled, so the RESTART 0 pattern is present on the terminal bus. On the next processor T1 state, the counter will advance to the Interrupts Off state.

3.8.2.2 Both power on and reset cause the interrupt logic to start an interrupt sequence. This is done by making PWR ON low. The state counter will advance through the states described in section 3.8.2 until the microprocessor has executed a restart instruction and has begun execution of terminal programs at location zero of the memory range.

3.8.2.3 When the microprocessor executes a halt instruction, it will enter the Stopped state. This is decoded by the processor state decoder logic at U22, Pin 9. The interrupt logic state counter will be in the Interrupts Off state and will go to the Begin Interrupt state when flip-flop "B" is reset at U310, Pin 11. The state counter advances through the sequence described in section 3.8.2.1 and the microprocessor goes out of the Stopped state and begins executing instructions at location zero.

3.9 RESTART LOGIC.

3.9.1 The restart logic block implements a special hardware/software interrupt feature for the microprocessor. During program execution restart instructions will be placed in the program when a data comm interrupt is allowed. The Restart will be changed to an alternate 8008-1 instruction code if no data comm interrupt exists, otherwise a normal restart instruction will be performed.

3.9.2 The restart instruction is a 1-byte subroutine call and is conditionally executed based on the terminal bus $\overline{ATN}$ signal. If the $\overline{ATN}$ line is high, all restart instructions encountered will be modified to an alternate 8008-1 instruction code (see summary below). If $\overline{ATN}$ is low, the restart instruction will not be modified and a subroutine will be executed to service the interrupt condition. This allows the program

to control when it can be interrupted so that the modified instruction codes do not make unexpected changes to the microprocessor registers.

RESTART INSTRUCTIONS

INSTRUCTION ADDRESS	ATN = HIGH	ATN = LOW	SUBROUTINE START
RST 0	LAH	RST 0	0
RST 1	LBH	RST 1	8 (10 OCTAL)
RST 2	LCH	RST 2	16 (20 OCTAL)
RST 3	LDH	RST 3	24 (30 OCTAL)
RST 4	LEH	RST 4	32 (40 OCTAL)
RST 5	LHH	RST 5	40 (50 OCTAL)
RST 6	LLH	RST 6	48 (60 OCTAL)
RST 7	LMH	RST 7	56 (70 OCTAL)

The restart logic makes a check during processor state T2 of an instruction fetch at U17, Pin 6 and 12 to see if $\overline{ATN}$ is low. If $\overline{ATN}$ is low or if it is not an instruction fetch, the Restart Disable flip-flop is reset at U59, Pin 5, which disables the restart instruction decoding and allows data to pass unmodified. If $\overline{ATN}$ is high (no interrupt), the restart instruction decoding at U11, Pin 8 will modify all restart instructions according to the restart instruction summary above. This modifying is done by disabling the buffers (U43, Pin 6 and 3) which change BIT7 and BIT6 of the instruction from "0" to "1".

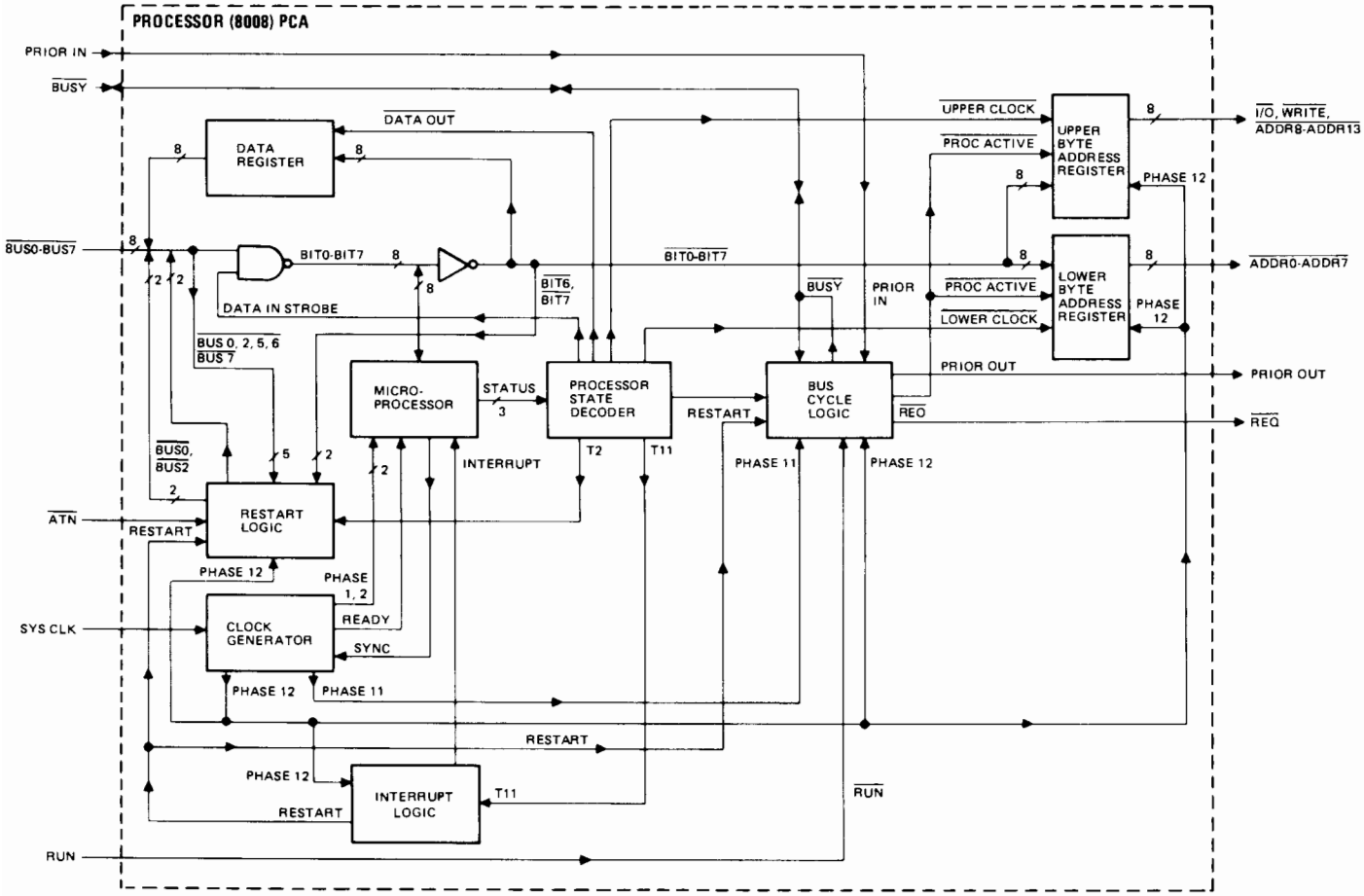


Figure 1
Processor (8008-1) PCA Block Diagram
AUG-01-76 13255-91008

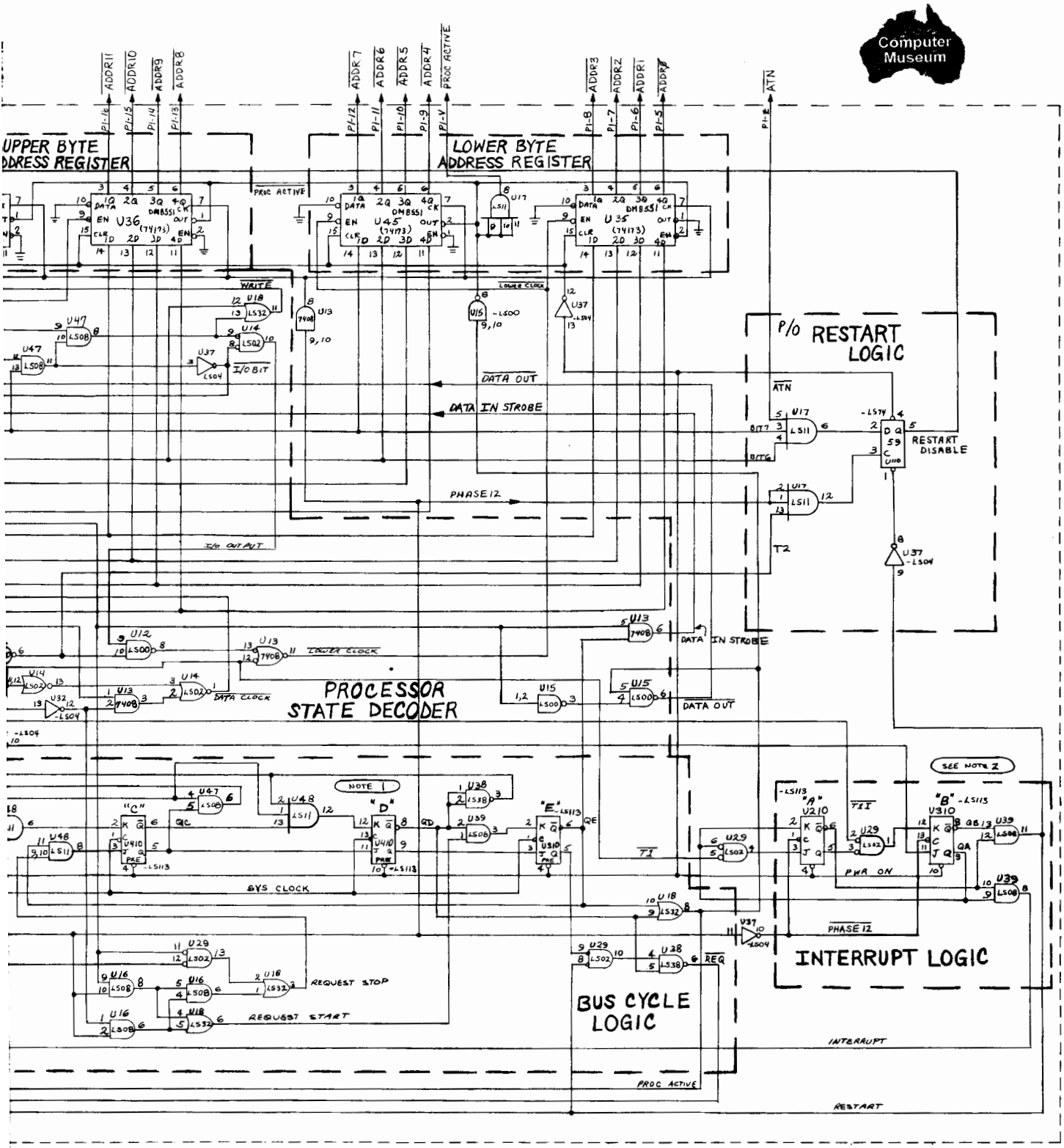
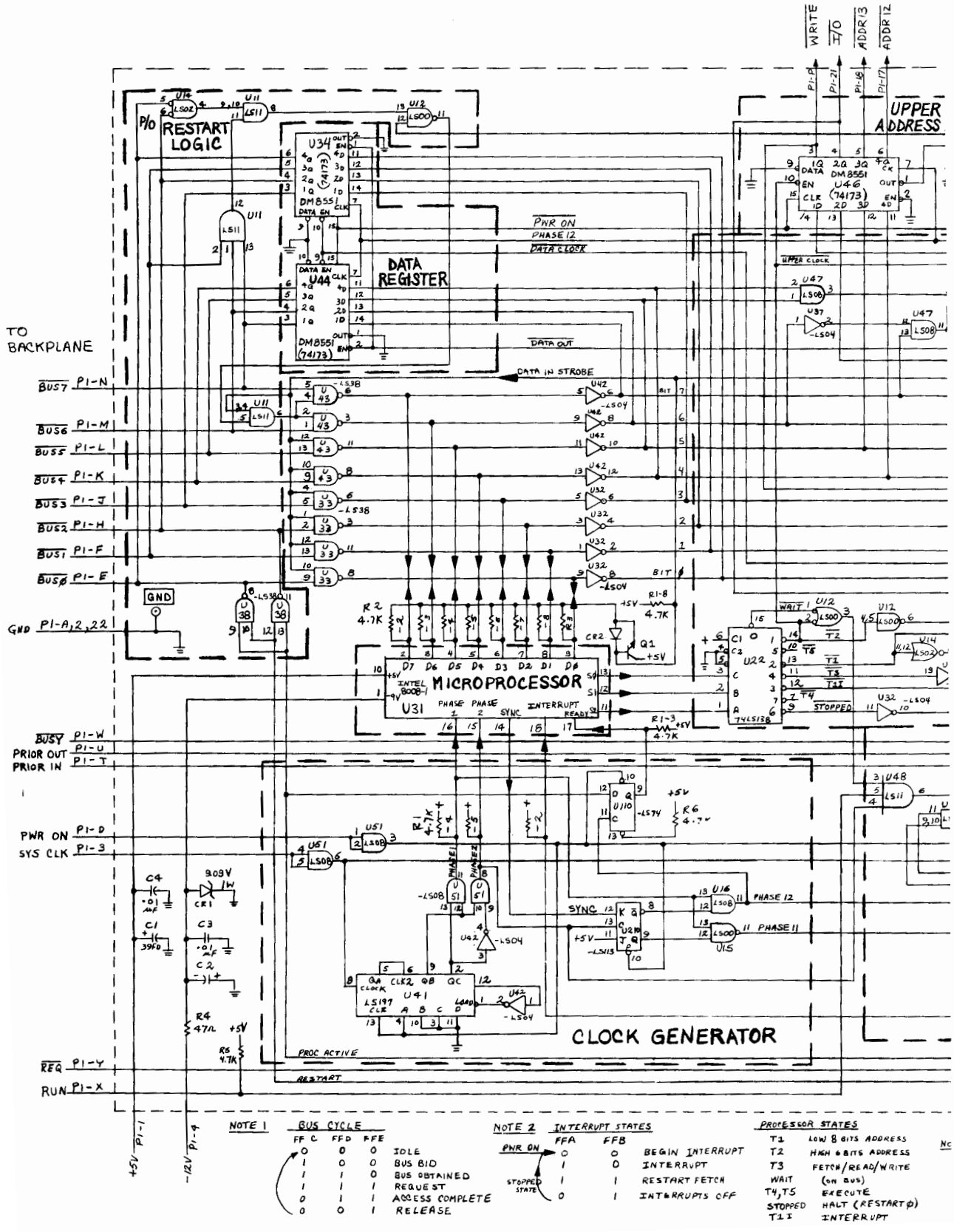


Figure 2
Processor (8008-1) PCA Schematic Diagram
AUG-01-76 13255-91008


P/O RESTART LOGIC
DATA REGISTER
UPPER ADDRESS
MICROPROCESSOR
U31
CLOCK GENERATOR
TO BACKPLANE
WRITE
I/O
ADDR13
ADDR12
PWR ON
PHASE 12
DATA CLOCK
DATA OUT
DATA IN STROBE
UPPER CLOCK
BUS7 P1-N
BUS6 P1-M
BUS5 P1-L
BUS4 P1-K
BUS3 P1-J
BUS2 P1-H
BUS1 P1-F
BUS0 P1-E
GND P1-A,2,22
BUSY P1-W
PRIOR OUT P1-U
PRIOR IN P1-T
PWR ON P1-D
SYS CLK P1-3
REQ P1-Y
RUN P1-X
+5V P1-1
-12V P1-4
PROC ACTIVE
RESTART
PHASE 12
PHASE 11
SYNC
WAIT
STOPPED
NOTE 1
BUS CYCLE
FF C FFD FFE
0 0 0 IDLE
1 0 0 BUS BID
1 1 0 BUS OBTAINED
1 1 1 REQUEST
0 1 1 ACCESS COMPLETE
0 0 1 RELEASE
NOTE 2
INTERRUPT STATES
FFA FFB
PWR ON 0 0 BEGIN INTERRUPT
1 0 INTERRUPT
STOPPED STATE 1 1 RESTART FETCH
0 1 INTERRUPTS OFF
PROCESSOR STATES
T1 LOW 8 BITS ADDRESS
T2 HIGH 6 BITS ADDRESS
T3 FETCH/READ/WRITE
WAIT (ON BUS)
T4,T5 EXECUTE
STOPPED HALT (RESTART Ø)
T1I INTERRUPT

SIGNAL NAME	CONNECTOR & PIN NUMBER
PHASE 1	U51, PIN 11
PHASE 2	U51, PIN 8
SYNC	U31, PIN 14
S_0	U31, PIN 13
S_1	U31, PIN 12
S_2	U31, PIN 11
PROCESSOR STATE	–

MODULE FUNCTIONS DURING NORMAL CYCLES

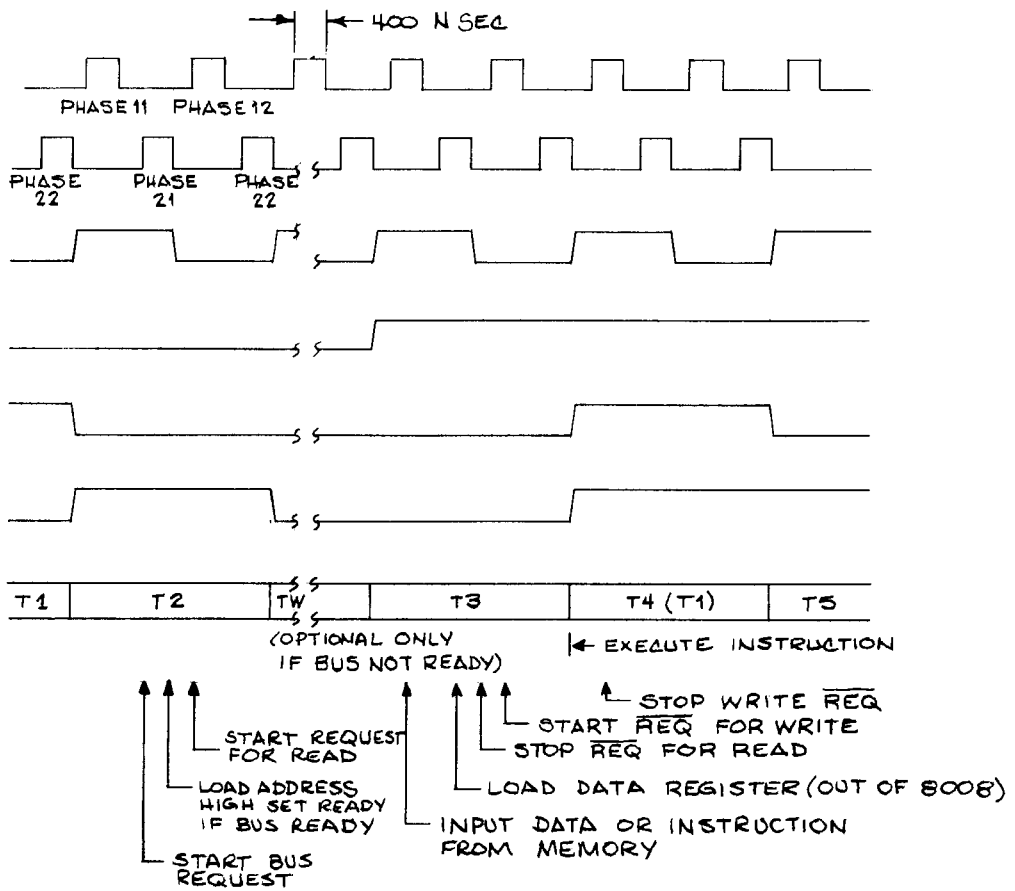


Figure 3
Processor State Timing Diagram
AUG-01-76 13255-91008

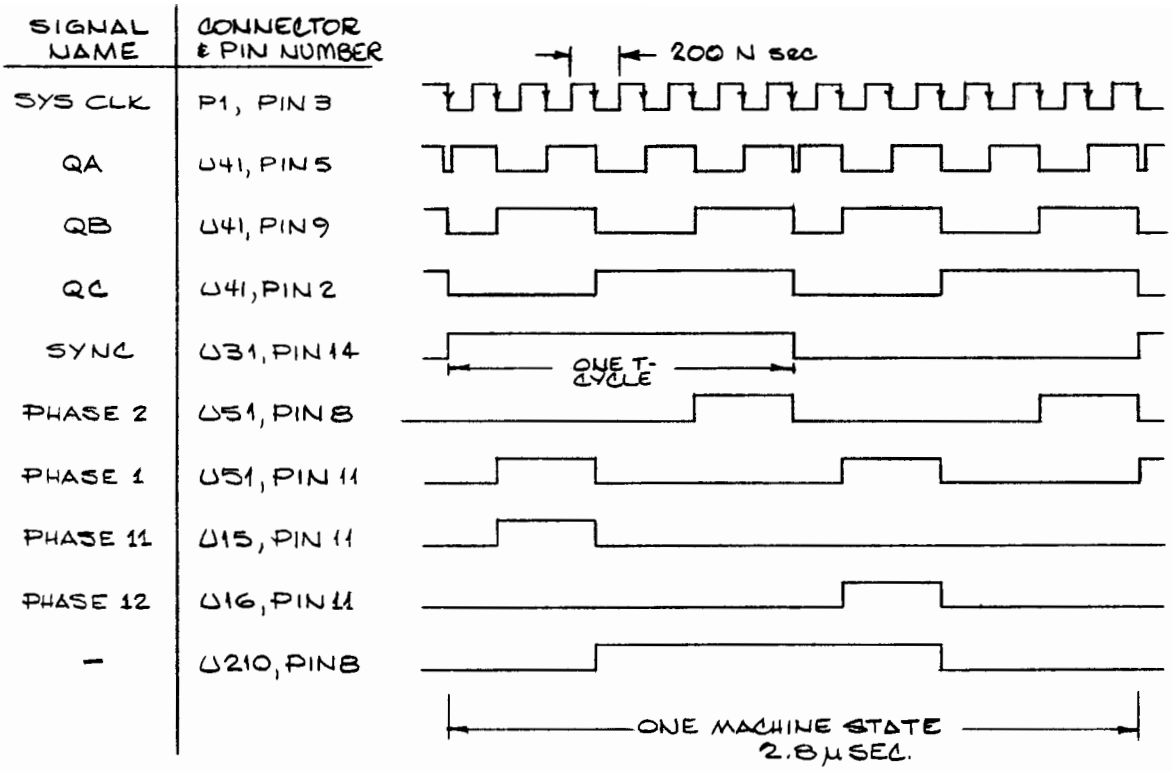


Figure 4
Clock Generator Timing Diagram
AUG-01-76 13255-91008

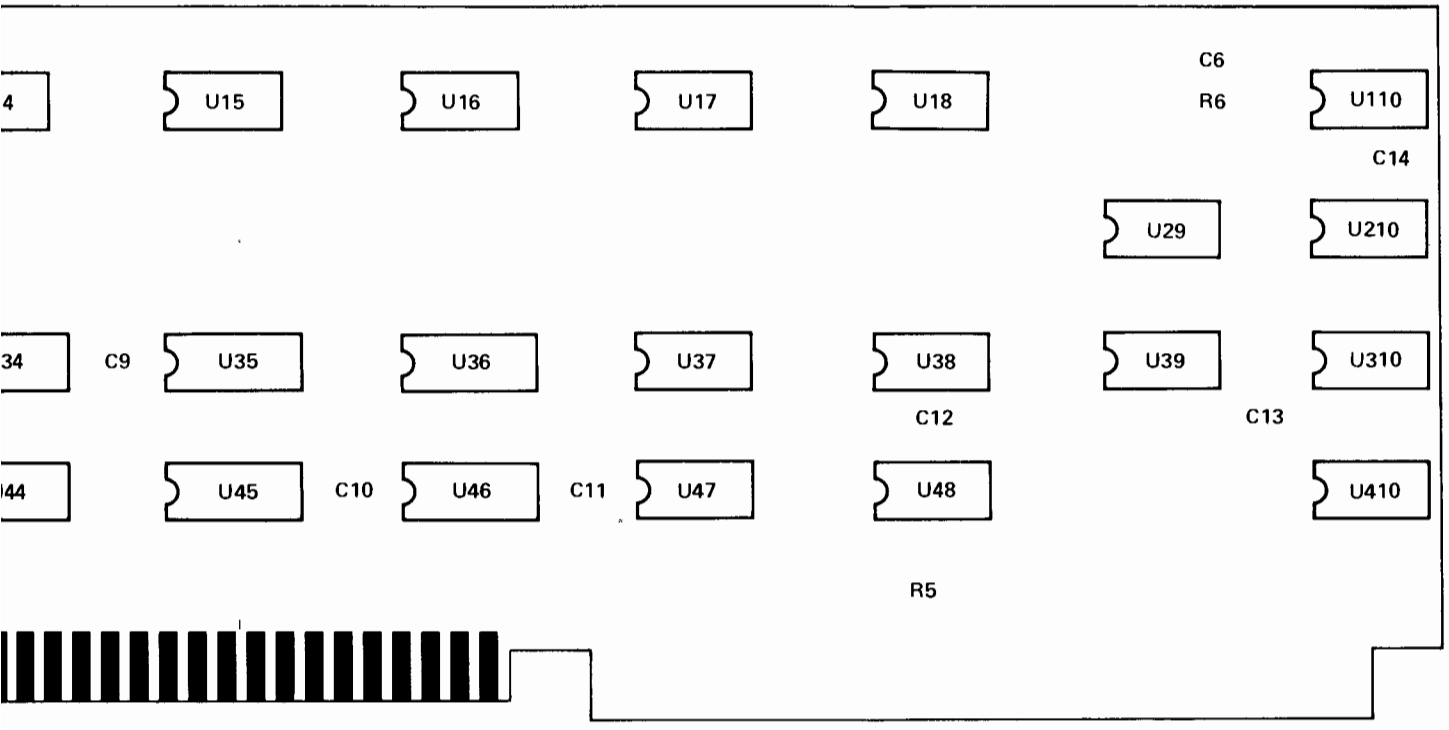
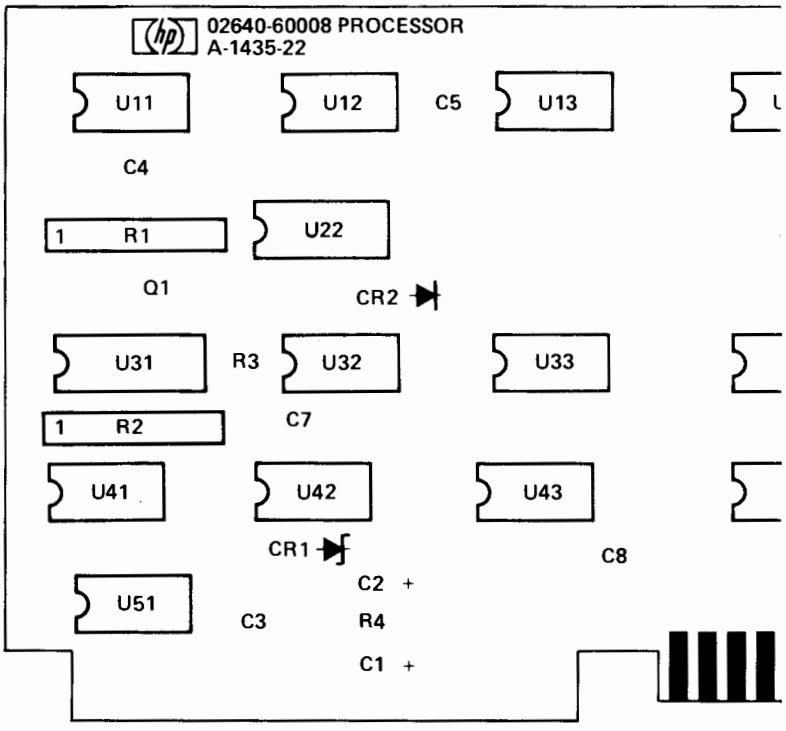


Figure 5
Processor (8008-1) PCA Component Location Diagram
AUG-01-76 13255-91008


02640-60008 PROCESSOR
A-1435-22
U11
U12
C5
U13
C4
1 R1
U22
Q1
CR2
U31
R3
U32
U33
1 R2
C7
U41
U42
U43
CR1
C8
C2 +
U51
C3
R4
C1 +

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60008	1	PROCESSOR (8008-1) ASSEMBLY DATE CODE: A-1435-22 REVISION CODE: 04-15-76	28480	02640-60008
C1	0160-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0160-1746	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C3	0160-2055	12	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1902-0651	1	DIODE-ZNR 9.09V 5% DO-15 PD=1W TC=+.057%	28480	1902-0651
CR2	1901-0040	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
E1	0360-0124	1	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
Q1	1854-0467	1	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
R1	1810-0125	2	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R3	0683-4725	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R4	0683-4705	1	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R5	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R6	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
U11	1820-1203	3	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U12	1820-1197	2	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U13	1820-0511	1	IC-DIGITAL SN7408N TTL QUAD 2 AND	01295	SN7408N
U14	1820-1144	2	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U15	1820-1197	5	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U16	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U17	1820-1203		IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U18	1820-1208	1	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U22	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U29	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U31	1820-1221	1	IC-DIGITAL C8008-1 MOS	34649	C8008-1
U32	1820-1199	3	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U33	1820-1209	3	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U34	1820-0574	6	IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
U35	1820-0574		IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
U36	1820-0574		IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
U37	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U38	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U39	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U41	1820-1193	1	IC-DIGITAL SN74LS197N TTL LS BIN	01295	SN74LS197N
U42	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U43	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U44	1820-0574		IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
U45	1820-0574		IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
U46	1820-0574		IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
U47	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U48	1820-1203		IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U51	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U110	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U210	1820-1213	3	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U310	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U410	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
XU31	1200-0539	1	SOCKET-IC 18-CONT DIP-SLDR	28480	1200-0539