HP 13272 FLEXIBLE DISC SYSTEM
MANUAL PART NO. 13255-91223

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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1.0 INTRODUCTION

The 13272 FLEXIBLE DISC SYSTEM consists of one MINIFLOPPY CONTROLLER PCA (02640-60223) in the HP 264X terminal, and up to two external Flexible Disc Drives (13270-60013). In a one drive system, the DISC DRIVE is connected to the CONTROLLER PCA through the CONTROLLER CABLE. In a two drive configuration, the second drive is daisy chained to the first one using the T-BLOCK and the NEXT DRIVE CABLE. The file system needed to support the FLEXIBLE DISC SYSTEM is presently only in the terminal firmware of the 2642A. The disc system hardware is compatible with all other members of the 264X family except the 2640B.

The MINIFLOPPY CONTROLLER PCA provides the control logic and processing capabilities needed to interface the HP 264X terminal with the DISC DRIVES. The MINIFLOPPY CONTROLLER PCA contains a Processor (Z80-A) and ROM (8K X 8bits), which enable it to directly execute DISC COMMANDS received from the Terminal PROCESSOR (02640-60209).

The DRIVE itself is composed of the DRIVE ELECTRONICS PCA, the SERVO CONTROL PCA, and the DRIVE MECHANISM. It uses 5.25 inch (13.4 cm) FLEXIBLE DISCS.

The function of the DRIVE ELECTRONICS PCA is to write and read magnetic transitions to and from the disc. It receives digital data from the controller and converts them to analog form for magnetic storage on the disc. It also takes these magnetic transitions from the media and, after amplification, filtering, and differentiation, converts them back to digital form for decoding in the controller.

2.0 OPERATING PARAMETERS

A summary of operating parameters for the MINIFLOPPY DISC MODULE is contained in Tables 1.0 to 5.8.

Table 1.0 Physical parameters

Part Number	Nomenclature	Size (L X W X D) +/- 0.2 cm	Weight (kg)
02640-60223	MINIFLOPPY CONTROLLER	32.6 X 10.2 X 1.4	
13270-60002	DRIVE ELECTRONICS PCA	16.3 X 14.4 X 1.0	
13270-60013	DRIVE (in package)	28.8 X 12.8 X 18	4.4
13270-60003	CONTROLLER CABLE	1.2 m (length)	
13270-60004	NEXT DRIVE CABLE	0.7 m (length)	
13270-60005	T - BLOCK	10.5 X 3.6 X 1.8	

Number of backplane slots required: 1

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B
Restrictions:	Type tested at product level. This environmental classification does not apply to the disc itself. The temperature and humidity specifications for the flexible disc are as follows:
	Ambient temperature 10 C – 40 C
	Relative humidity 20 % – 80 %
	Maximum wet bulb 25 C

Failure rate:	MINIFLOPPY CONTROLLER PCA	: 3.1 % per 1000 hours
	DRIVE ELECTRONICS PCA	: 1.5 % per 1000 hours
	SERVO CONTROL PCA	: .5 % per 1000 hours
	DRIVE MECHANISM	: 2.5 % per 1000 hours (at 5% motor duty cycle)

Table 3.0 Power Supply and Clock Requirements
MINIFLOPPY CONTROLLER PCA
(At +/- 5% unless otherwise specified)

+ 5 Volts DC	+12 Volts DC	-12 Volts DC	-42 Volts DC
@ 875 mA typ 1400 mA max	@ 35 mA typ 45 mA max	@ 16 mA typ 30 mA max	@ mA NOT APPLICABLE

115 Volts AC	220 Volts AC
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock frequency: 16.0 +/- .05 MHZ, generated on board.

Table 3.1 Power Supply Requirements
DRIVE ELECTRONICS PCA
DRIVE MECHANISM

+5 Volts DC	+12 Volts DC	-12 Volts DC	-42 Volts DC
@ 280 mA (drive electronics PCA)	460 mA (drive electronics PCA + Stepper Motor. 320 ma for Stepper Motor alone) 600 ma (Servo PCA) +12 VA @ 84 mA (see note 1)	@ mA NOT APPLICABLE	@ mA NOT APPLICABLE

115 Volts ac	220 Volts ac
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency : NOT APPLICABLE

NOTE 1: The DRIVE ELECTRONICS PCA receives power from the CONTROLLER PCA through the CONTROLLER CABLE. A total of six lines is dedicated to +12 volts. Two of them are named +12 VA on the DRIVE ELECTRONICS PCA. +12 VA has a separate LC filtering network on the DRIVE ELECTRONICS PCA to keep the large transients associated with the spindle motor from disturbing the read/write circuits.

Table 4.0 MINIFLOPPY CONTROLLER PCA
Backplane interface connector

Connector and Pin No	Signal Name	Signal Description
P1 pin 1	+5 V	+5 Volts dc power supply
- 2	GND	Ground common return (power and signal)
- 3	not used	
- 4	-12 V	-12 Volts dc power supply
- 5	$\overline{ADDR0}$	Negative true, address bit 0
- 6	$\overline{ADDR1}$	Negative true, address bit 1
- 7		Not used
- 8		Not used
- 9	$\overline{ADDR4}$	Negative true, address bit 4
-10		Not used
-11		Not used
-12		Not used
-13		Not used
-14	$\overline{ADDR9}$	Negative true, address bit 9
-15	$\overline{ADDR10}$	Negative true, address bit 10
-16	$\overline{ADDR11}$	Negative true, address bit 11
-17		Not used
-18		Not used
-19		Not used
-20		Not used
-21	$\overline{I/O}$	Negative true, Input Output / Memory
-22	GND	Ground common return (power and signals)

Table 4.0 Backplane interface connector (cont'd.)

Connector and pin No	Signal name	Signal Description
P1 pin A	GND	Ground common return (power and signals)
-B	$\overline{\text{POLL}}$	Negative true, Polled interrupt Identification Request
-C	+12 V	+12 Volts DC Power supply
-D		Not used
-E	$\overline{\text{BUS0}}$	Negative true, Data bus bit 0
-F	$\overline{\text{BUS1}}$	Negative true, Data bus bit 1
-H	$\overline{\text{BUS2}}$	Negative true, Data bus bit 2
-J	$\overline{\text{BUS3}}$	Negative true, Data bus bit 3
-K	$\overline{\text{BUS4}}$	Negative true, Data bus bit 4
-L	$\overline{\text{BUS5}}$	Negative true, Data bus bit 5
-M	$\overline{\text{BUS6}}$	Negative true, Data bus bit 6
-N	$\overline{\text{BUS7}}$	Negative true, Data bus bit 7
-P	$\overline{\text{WRITE}}$	Negative true, Write/Read type cycle
-R	$\overline{\text{ATN2}}$	Negative true, CTU and Polled interrupt Request
-S		Not used
-T	PRIOR IN	Bus controller priority input
-U	PRIOR OUT	Bus controller priority output
-V		Not used
-W		Not used
-X		Not used
-Y	$\overline{\text{REQ}}$	Negative true, Request (Bus data currently valid)
-Z		Not used

Table 4.1 MINIFLOPPY CONTROLLER PCA AND DRIVE ELECTRONICS PCA
Drive interface connector (SEE NOTE 2)

Connector and pin No	Signal name	Signal description
P2/J1 pin 1	OUTDA0	Output address to next drive (LSB) (SEE NOTE 2)
- 2	DA0/INDA0	Output, Drive address Bit 0 (SEE NOTE 2)
- 3	OUTDA1	Output address to next drive (MSB) (SEE NOTE 2)
- 4	DA1/INDA1	Output, Drive address Bit 1 (SEE NOTE 2)
- 5	GND	Ground common return (power and signals)
- 6	$\overline{\text{INDEX}}$	Input, Index pulse, Indicates that the first physical sector of the track follows. (low assertion)
- 7	GND	Ground common return (power and signals)
- 8	$\overline{\text{HEAD LOAD}}$	Output, This signal commands the drive to lower the head onto the disc. HEAD LOAD is latched by the addressed drive when the STROBE signal is asserted. The latched signal is also used to change the definition of P2-13 and 11. This signal has no mechanical effect on the TANDON DRIVE, since there is no head load solenoid. (low assertion)
- 9	DISCID1	Input, Disc identification bit 1, The middle bit of the identification code that allows the controller to find out what type of drive is connected.
-10	$\overline{\text{STROBE}}$	Output, Strobe signal, Latches the following signals on the DRIVE ELECTRONICS PCA: $\overline{\text{MOTOR ON}}$, $\overline{\text{DRIVE SELECT}}$, $\overline{\text{HEAD LOAD}}$, and $\overline{\text{SIDE SELECT}}$. (low assertion)
-11	DISCID2	Input, Disc identification bit 2 (MSB), This signal is the disc ID when the latched HEAD LOAD signal is false. When the latched HEAD LOAD is true, this signal is used during self test to indicate that read data or write data pulses are occuring more frequently than every 9 uSec.

Table 4.1 Drive interface connector (cont'd.)

Connector and pin No	Signal name	Signal description
P2/J1 pin12	DRIVE SELECT	Output, Indicates that the drive is being selected for reading, writing, seeking, or returning status to the controller. DRIVE SELECT is latched by the addressed drive when the STROBE signal is asserted. In addition, circuitry is provided on each drive board to deselect the drive if another drive is selected. This prevents buffer contention, since the latched DRIVE SELECT signal is used to enable the outputs from each drive that are wired in parallel on the interface. (low assertion)
-13	DISCID0	Input, Disc identification bit 0 (LSB). This signal is the disc ID when the latched HEAD LOAD signal is false. When the latched HEAD LOAD signal is true, this signal is used to indicate that a disc is installed and is spinning (i.e. that index pulses are occuring more frequently than every 300 msec)
-14	$\overline{\text{STEP}}$	Output, Commands the selected drive to move the head one track in the direction indicated by the DIRC signal. (low assertion)
-15	$\overline{\text{DISC CHANGE}}$	Input, Indicates that a disc has been removed from or inserted into the drive. Transitions of the write protect switch cause the disc change flip-flop to be set. This flip-flop may be cleared by addresssing and strobing the drive with DRIVE SELECT, HEAD LOAD, and MOTOR ON deasserted. (low assertion)
-16	$\overline{\text{DIRC}}$	Output, Specifies which direction the head is to be moved by the STEP pulses. The head moves inward (i.e. toward higher numbered tracks) when this signal is asserted. (low assertion)
-17	$\overline{\text{READ DATA}}$	Input, Serial data read from the drive. This signal pulses each time a flux transition is detected by the read circuitry. (low assertion)

Table 4.1 Drive interface connector (cont'd.)

Connector and pin No	Signal name	Signal description
P2/J1 pin18	MOTOR ON	Output, Commands the drive to turn on the spindle motor. MOTOR ON is latched by the addressed drive when the STROBE signal is asserted. (low assertion)
-19	SIDE SELECT	Output, Indicates which side of the diskette is being read from or written to. SIDE SELECT is latched by the addressed drive when the STROBE signal is asserted. ASSERTED = Head 1 selected NOT ASSERTED = Head 0 selected
-20	WG	Output, Write Gate. Enables writing on the selected drive. It is asserted by the FDC chip to turn on the write and erase currents. (low assertion)
-21	POR	Output, Power on reset, Sets the drive board in a known state following application of power or reception of a soft power-on from the terminal. The reset state is DRIVE SELECT, MOTOR ON, HEAD LOAD, and SIDE SELECT deasserted In addition, writing is disabled during the assertion of POR. (low assertion)
-22	WD	Output, Write Data. This signal is pulsed by the write circuitry for each transition to be written on the disc. It is used in conjunction with the WG signal to write data on the disc. (low assertion)
-23	WPRT	Input, Indicates that the state of the write protect switch will not allow writing on the disc. (low assertion)
-24	TR00	Input, Track 0 Indicator, Signals that the head assembly is positioned on track 0 (the outermost track). (low assertion)
-25	EN2	Not used on Controller Module
-26	EN1	Input, Enables Controller output driver, This prevents buffer contention if the controller to drive cable is connected to the wrong side of the T-block when connecting a two drive system.

Table 4.1 Drive interface connector (cont'd.)

Connector and pin No	Signal name	Signal description
P2/J1 pin27	GND	Ground common return (power and signals)
-28	GND	Ground common return (power and signals)
-29	+5 V	+ 5 Volts D C Power supply
-30	GND	Ground common return (power and signals)
-31	+5 V	+ 5 Volts D C Power supply
-32	+5 V	+ 5 Volts D C Power supply
-33	GND	Ground common return (power and signals)
-34	GND	Ground common return (power and signals)
-35	+12 VA	+ 12 Volts D C Power supply (Analog)
-36	+12 VA	+ 12 Volts D C Power supply (Analog)
-37	+12 V	+ 12 Volts D C Power supply (Motors)
-38	+12 V	+ 12 Volts D C Power supply (Motors)
-39	+12 V	+ 12 Volts D C Power supply (Motors)
-40	+12 V	+ 12 Volts D C Power supply (Motors)

NOTE 2 : The drive interface connector is named P2 on the CONTROLLER PCA, and J1 on the DRIVE ELECTRONICS PCA. The pin assignment is the same, except for pins 1 through 4. These four pins are used to daisy-chain the address to the second drive. The address is sent from the CONTROLLER PCA to the first drive on pins 2 and 4. The first drive then outputs the modified address to the second drive on pins 1 and 3. The T-BLOCK shifts these signals to pins 2 and 4 of the next drive connector so that the second drive also receives the (modified) address on pins 2 and 4. This allows the CONTROLLER and NEXT DRIVE CABLES to be wired point to point (ie. pin1 --> pin1, pin2 --> pin2, etc.).
All the signals are shown in this table as inputs or outputs for the CONTROLLER PCA (P2). These directions are reversed for the DRIVE ELECTRONICS PCA (J1).

Table 5.0 DRIVE ELECTRONICS PCA
Test point connector

Connector	Signal Name	Signal Description
J2- 1	GND	
- 2	TP1	Test point 1) Filtered Preamp output (differential)
- 3	TP2	Test point 2)
- 4	TP3	Test point 3) differentiator output (differential)
- 5	TP4	Test point 4)

Table 5.1 DRIVE ELECTRONICS PCA / DRIVE INTERFACE
Head 1 connector (Top Head)

Connector	Signal Name	Signal Description
J5- 1	GND	GND wrapped around head leads
- 2	ERASE	Erase coil in head assembly
- 3	R/W 1	Read/write coil; first half
- 4	C.T.	Center tap of head assembly
- 5	R/W 2	Read/write coil; Second half

Table 5.2 DRIVE ELECTRONICS PCA / DRIVE INTERFACE
Head 0 connector (Bottom Head)

Connector	Signal Name	Signal Description
J6- 1	ERASE	Erase coil in head assembly
- 2	R/W 1	Read/write coil; first half
- 3	C.T.	Center tap of head assembly
- 4	R/W 2	Read/write coil; second half
- 5	GND	GND wrapped around head leads

Table 5.3 DRIVE ELECTRONICS PCA / DRIVE INTERFACE
Write Protect Switch Connector

Connector	Signal Name	Signal Description
J8- 1	WPRT	Open when a write protected disc is inserted. Grounded otherwise
- 2	GND	Ground to write protect switch
- 3	N.C.	No connection
- 4	N.C.	No connection

Table 5.4 DRIVE ELECTRONICS PCA / DRIVE INTERFACE
Drive Select LED Connector

Connector	Signal Name	Signal Description
J9- 1	DRIVE SELECT	Cathode of the DRIVE SELECT LED
-2	ACTIVITY LED	Anode of the DRIVE SELECT LED
- 3	N.C.	No connection
- 4	N.C.	No connection

Table 5.5 DRIVE ELECTRONICS PCA / DRIVE INTERFACE
Index Hole detector Connector

Connector	Signal Name	Signal Description
J10- 1	EMITTER	Anode of index INFRARED emitter
- 2	PHOTO	Emitter of Photo transistor sensor
- 3	+5 V	Collector of Photo transistor sensor
- 4	GND	Ground to INFRARED emitter

Table 5.6 DRIVE ELECTRONICS PCA / DRIVE INTERFACE
Track 0 Switch Connector

Connector	Signal Name	Signal Description
J11- 1	TR00	Normally open, Grounded when head is on track zero
- 2	TR00	Normally connected, Open when head is on track zero
- 3	N.C.	No connection
- 4	GND	Ground to Track 0 switch

Table 5.7 DRIVE ELECTRONICS PCA / DRIVE INTERFACE
Stepper Motor Connector

Connector	Signal Name	Signal Description
J12- 1	PHASE 4	Phase 4 of stepper motor
- 2	PHASE 2	Phase 2 of stepper motor
- 3	PHASE 1	Phase 1 of stepper motor
- 4	PHASE 3	Phase 3 of stepper motor
- 5	+12 V	Common to all phases of stepper motor

Table 5.8 DRIVE ELECTRONICS PCA / SERVO BOARD INTERFACE
Servo Board PCA Connector

Connector	Signal Name	Signal Description
J13- 1	MOTOR ON	Turns spindle motor on (low true)
- 2	N.C.	No connection
- 3	GND	Servo PCA Ground
- 4	+12 V	+12 V to Servo PCA supply

3.0 MINIFLOPPY CONTROLLER PCA THEORY OF OPERATION

Refer to the Block Diagram (Figure 1), schematic diagram (Figure 18), component location diagram (Figure 19), parts list (02640-60223), and other figures, located in SECTION 7.0.

Throughout this section, components will be referenced according to their designators in the schematic diagram (Fig 18). Functional blocks in the Block Diagram (Fig 1), are referenced with numbers in parentheses; example: Z80-A CPU (3), RAM BUFFER (5).

3.1 GENERAL OVERVIEW

3.1.1 FUNCTION

The function of the MINIFLOPPY CONTROLLER MODULE is to interface the 13272 MINIFLOPPY DISC DRIVE to the 264X Terminal. The DISC DRIVE contains all the circuits to perform the transformation from digital to analog pulses during write operations, and from analog to digital during read operations.

The minifloppy controller is a single 264X size board. The controller employs a Z-80A processor with 1 Kbytes of RAM, 8 Kbytes of ROM, and a Floppy Disc Controller (FDC) chip (Western Digital 1791-02 compatible). A single 40 conductor cable connects the controller board to the external drive unit(s). This cable provides power to the unit(s) and all of the interface control and data lines. In addition, the shield is used to send earth ground to the external drive package.

The controller is comprised of three sections: the processor, the drive interface, and the terminal interface. The Z-80A processor provides the intelligent link between the drive and terminal interfaces. It accepts high level commands (e.g. seek, read, write, etc.) from the terminal operating system and executes command routines with the help of the FDC chip. The Z-80A also performs a self-test of the minifloppy system.

The drive interface section is made up of the 1791 FDC chip and the data encoder/decoder. The FDC chip is a specialized LSI chip that replaces much of the discrete logic necessary in a floppy disc interface. The FDC accepts command and data bytes from the Z-80A and generates the control signals needed by the minifloppy drive. The FDC controls CRC generation and checking, calculates write precompensation, and performs seeking, reading, writing, formatting, and various other functions. Together, the Z-80A and 1791 FDC form a high throughput (31 Kbytes/sec) data channel. This data transfer rate cannot be fully utilized in the 13272 system because of the 1 Kbyte/sec. limitation of the terminal operating system.

3.1.2 READ AND WRITE OPERATIONS

Read and write operations are performed on SECTORS on the disc. Each SECTOR is 256 bytes long.

During a write operation, the 8 bit bytes to be written on the disc are transfered by the Terminal PROCESSOR from the Terminal DISC BUFFER to the MINIFLOPPY CONTROLLER MODULE Backplane Interface. The Z80-A CPU(3) transfers each byte from the Backplane Interface(1) to the RAM BUFFER(5). Then the Z80-A CPU(3) transfers the data from the RAM BUFFER(5) to the FLOPPY DISC CONTROLLER CHIP(7), which performs a parallel to serial transformation on the data. The FLOPPY DISC CONTROLLER (7) converts the data into a series of pulses, according to the Modified Frequency Modulation (MFM) code.

The WRITE PRECOMPENSATION circuit(9) then modifies the timing of the data pulses to reduce the effect of bit shift which occurs during the write/read process. Each WRITE DATA PULSE causes the DISC DRIVE to create a magnetic flux transition on the disc.

During a read operation, the DISC DRIVE sends a serial pulse stream to the MINIFLOPPY CONTROLLER MODULE. Each READ DATA PULSE corresponds to a magnetic flux transition on the disc.

The CONTROLLER decodes this serial pulse stream into 8 bit bytes. The FLOPPY DISC CONTROLLER CHIP(7) performs this function, using the READ CLOCK (RCLK) signal. The PHASE LOCKED LOOP (8) generates the READ CLOCK by locking to the READ DATA PULSE stream. Each byte reconstructed by the FDC(7) is read by the Z80-A CPU(3), and written in the RAM BUFFER(5). The CPU(3) then transfers these data bytes to the BACKPLANE INTERFACE(1), where they are read by the Terminal PROCESSOR.

3.1.3 PARTITIONING OF THE MINIFLOPPY CONTROLLER MODULE

The MINIFLOPPY CONTROLLER PCA can be described as ten functional blocks. The following sections describe each of them in detail (see Figure 1 - MINIFLOPPY CONTROLLER PCA BLOCK DIAGRAM) :

```
1- Backplane Interface                    )==> TERMINAL INTERFACE

2- Clock Generator                        )
3- CPU                                    )
4- ROM                                    )==> PROCESSOR
5- RAM                                    )
6- Memory and I/O address decoders        )

7- Floppy Disc Controller                 )
8- Phase Locked Loop                      )==> DRIVE INTERFACE
9- Write Pre-Compensation                 )
10- Drive Interface Drivers / Receivers   )
```

3.2 TERMINAL INTERFACE

The interface between the Terminal Processor and the MINIFLOPPY CONTROLLER MODULE is a set of four registers. The two input registers are DATA IN (U23) and COMMAND (U33). The two registers which output information to the terminal processor are DATA OUT (U43) and STATUS (U53).

3.2.1 MODULE SELECTION

The CONTROLLER PCA address is I/O MODULE 15. When the module is addressed, the state of ADDR0, ADDR1, and WRITE determines which register or function is selected (U34). The following table summarizes the terminal interface registers.

Table 6.0 Terminal interface register addressing

SIGNAL/REG. SELECTED	READ/WRITE	ADDRESS
DATA IN	WRITE	8F00
COMMAND	WRITE	8F01
SPON	WRITE	8F02
CLR ATN	WRITE	8F03
DATA OUT	READ	8F00
STATUS	READ	8F01

3.2.2 POLL and ATN2

When the MINIFLOPPY CONTROLLER needs service from the terminal processor , the Z80-A writes I/O register E0 (see appendix D). This sets the interrupt flip-flop (U41), and asserts ATN2 on the backplane. When the flip-flop is set, the CONTROLLER asserts bit 5 during a "polled interrupt identification" operation. The interrupt flip-flop is cleared by the terminal processor writing to memory address 8F03 (see table above).

3.2.3 INPUT REGISTERS

The DATA IN register (memory address 8F00) is used by the terminal processor to transfer data bytes to the CONTROLLER. When the register is written, a handshake flip-flop (U42) is cleared, indicating to the Z80-A (I/O address 80, bit 0) that a data byte may be read. When the Z80-A reads the byte (I/O address 60), the handshake flip-flop is automaticaly set.

The COMMAND register (memory address 8F01) is similar to the DATA IN register. The handshake flip-flop (U41) is cleared when the register is written, and can be read by the Z80-A as I/O address 80, bit 2. When the Z80-A reads the command byte (I/O address 40), the handshake flip-flop is set.

3.2.4 OUTPUT REGISTERS

The DATA OUT register (memory location 8F00) is used by the CONTROLLER to transfer data bytes to the terminal PROCESSOR. When the register is written by the Z80-A (I/O address 80), the handshake flip-flop is set, indicating to the terminal (memory address 8F01, bit 7) that a data byte may be read. When the terminal PROCESSOR reads the register (memory address 8F00) the handshake flip-flop is automaticaly reset.

The STATUS register (memory address 8F01) is used by the CONTROLLER to transfer status information to the terminal PROCESSOR. The Z80-A writes into this register as I/O address A0. When the terminal PROCESSOR reads the STATUS register (memory address 8F01), the outputs of buffer U52 are enabled on the terminal backplane data bus. This allows the terminal PROCESSOR to read the handshake flip-flops in the same operation.

The three handshake bits (U42 and U52) are initialized by the Z80-A writing I/O address C0. The table below summarizes the result of this operation.

Table 7.0 Handshake bit description

Handshake	Z80-A I/O reg. 80 bit #	Terminal mem. add. 8F01, bit#	Meaning of RESET state	Indication
DATA IN	0	6	FULL	TERMINAL HAS WRITTEN IN THE DATA IN REGISTER.
DATA OUT	1	7	EMPTY	Z80-A HAS NOT WRITTEN IN THE DATA OUT REGISTER.
COMMAND	2	5	FULL	TERMINAL HAS WRITTEN IN THE COMMAND REGISTER.

3.3 PROCESSOR

3.3.1 Z80-A CPU(3)

The MINIFLOPPY CONTROLLER MODULE uses a Z80-A CPU chip (U12) as the central processing element.

The use of moderate access time devices, like the ROM(U14) and the FDC(U18), is made possible by adding one WAIT STATE to every OP CODE fetch cycle (M1), and every I/O REQUEST (IORQ) cycle. The maximum access time allowed is 600 ns. This function is performed by the "WAIT STATE MACHINE" (U21, U11, U22).

The Power-on reset circuit (U212, U28, C39, R21, and CR10) asserts the INPOR line for aproximately 50 ms after power-on. The SPON (SOFTWARE POWER-ON) line allows the Terminal software to force the controller into the POWER-ON RESET state. (see Section 3.2.1)

The Z80-A may be interrupted by the floppy disc controller (INTRQ) or by the missing pulse signal from the selected drive. It determines which source is interrupting by reading the Potpourri register (I/O address 20). See section 3.4.1 for more details on these interrupts.

3.3.2 ROM (4)

The MINIFLOPPY CONTROLLER MODULE program is contained in an 8K X 8 bit ROM (U14).

3.3.3 RAM (5)

The 1 KBYTE RAM memory on the CONTROLLER MODULE is composed of two 1K X 4 bit static RAM chips (U16 and U26). This memory is used by the Z80-A CPU for variable storage and data buffering.

3.3.4 CLOCK GENERATOR (2)

The basic 16 MHZ clock is provided by a crystal oscillator (U61). The 16 MHZ clock signal is gated by two NAND gates (U36). This provides the capability of disabling the internal clock (test point E2), and supplying an external clock signal on test point E1.

The 74LS163(U24) counter divides the 16 MHZ clock to create 8MHZ, 4MHZ, and 1MHZ clocks. The 4MHZ clock is used by the Z80-A CPU. The Write Precompensation circuit uses the 8 and 1MHZ clocks, and the FDC(U18) u s 1MHZ only.

The Z80-A CPU clock input requires a VOH (min) of 4.2V, with rise and fall times of less than 15 ns when operating at 4MHZ. The transistor circuit (Q19,R3,R4,R5, and C1), in parallel with the NAND driver (U22), reduces the rise time of the NAND gate, while resistor R2 ensures the minimum high clock level.

3.3.5 MEMORY AND I/O ADDRESS DECODERS (6)

The memory address decoder circuit (U21, U22, U31, and U32) generates the CS (CHIP SELECT) signals for the ROM and the RAMS.
The following table summarizes the locations of memory:

ROM 0000H to 1FFFH
RAM 4000H to 43FFH

Two 74LS138 DEMULTIPLEXERS (U27, U17) are used to decode the I/O select lines. U27 selects which output device is being written to, and U17 selects which input device is being read from.

The ERROR DISPLAY REGISTER (U37) and the LED ARRAY (CR1), are used to display the current CONTROLLER STATUS. In addition, the track number is displayed during formatting, and the test number is shown during SELF-TEST. Refer to APPENDIX C for the self test LED codes.

Bit 5 of the ERROR DISPLAY REGISTER is used as MASTER RESET for the FDC(U18) and DRIVE BOARD INTERFACE. This allows the Z80-A CPU to separately reset all DRIVE related functions under software control. It also allows extending of the POR pulse for the FDC.

The following table summarizes the addresses of the Z80-A I/O registers.

Table 8.0 Z80-A I/O register addresses

I/O address	Read	Write
0 0	FDC STATUS	FDC COMMAND
0 1	FDC TRACK	FDC TRACK
0 2	FDC SECTOR	FDC SECTOR
0 3	FDC DATA	FDC DATA
2 0	POTPOURRI	STOP DSA (NOT USED)
4 0	COMMAND	ERROR DISPLAY
6 0	DATA IN	DRIVE 3 FUNCTION
6 1	---	DRIVE 2 FUNCTION
6 2	---	DRIVE 1 FUNCTION
6 3	---	DRIVE 0 FUNCTION
8 0	HANDSHAKE	DATA OUT
A 0	---	STATUS
C 0	START DSA (NOT USED)	INITIALIZE HANDSHAKE
E 0	---	SET SYST INT, (ATN2)

3.4 DRIVE INTERFACE

See also Table 4.1 in Section 2.0, for signal description.

3.4.1 DRIVE INTERFACE DRIVERS AND RECEIVERS (10)

There are 12 output lines on the Disc Interface. Eight of them are the outputs of a 74LS240 (U210) 3-state octal buffer: DA0, DA1, DRIVE SELECT, MOTOR ON, HEAD LOAD, SIDE SELECT, STROBE, and STEP. STROBE is asserted when the Z80-A writes to I/O addresses 60-63. STEP is an FDC Output. DRIVE SELECT, MOTOR ON, HEAD LOAD, and SIDE SELECT are DATA BUS bits 2 to 5; DA0 and DA1 are ADDRESS BUS bits 0 & 1.

The outputs of the buffer (U210) are enabled whenever EN1=RG=WG=0. EN1 (P2-26) is connected to ground on the DRIVE ELECTRONICS PCA. They are disabled (U211) when either READ GATE or WRITE GATE is asserted, indicating that a read or write operation is being performed on the DRIVE. This suppresses the noise transmited to the DRIVE by the buffered DATA BUS and ADDRESS BUS lines. A resistor network (R20) provides the necessary pull up to prevent the lines from toggling when U210 is disabled.

The WRITE GATE (WG) signal is buffered by a 3-state buffer (U29). It is disabled when the READ GATE (RG) is asserted. The DIRECTION CONTROL (DIRC), WRITE DATA (WD), and POWER ON (POR) signals are buffered (U29) and always enabled.

Each of the 8 Input lines from the DISC DRIVE to the CONTROLLER MODULE is connected to a 74LS14 SCHMITT trigger inverter, with a 10K resistor pull up. This increases the noise margin on the logic levels transmited through the CONTROLLER TO DRIVE CABLE.

The POTPOURRI REGISTER (U110) is a buffer which allows the Z80-A to sample the state of eight signals. Table 9.0 summarizes this register.

Table 9.0 POTPOURRI register description

Bit #	Assertion state	Description
0	HIGH	WRITE PROTECT, Write protect tab is installed on disc in selected drive.
1	LOW	FDC DATA REQUEST, A data byte is available during a read operation; a data byte is required during a write operation.
2	LOW	FDC INTERRUPT REQUEST, Asserted by the FDC when it completes a command.
3	HIGH	DISCID0 (head unloaded on selected drive), LSB of the disc drive identification code.
	LOW	MISSING PULSE (head loaded on selected drive) , Disc in selected drive is not spinning.
4	HIGH	DISCID1 (head unloaded on selected drive) , Middle bit of the disc drive identification code.
5	HIGH	DISCID2 (head unloaded on selected drive) , MSB of the disc drive identification code.
	HIGH	9 uSec (head loaded on selected drive) , Data pulses are occuring at least every 9 uSec. Used during write/read self test.
6	HIGH	SELF TEST jumper installed
7	HIGH	LOOP DSA test point grounded (not used)

3.4.2 FLOPPY DISC CONTROLLER (7)

The FLOPPY DISC CONTROLLER (U18) performs the functions of Floppy Disc Formatter and Controller. It is composed of two primary sections: the parallel Processor Interface, and the Floppy Disc Interface.

The Processor Interface uses the 8 bidirectional DATA lines. Two address lines A0 & A1, with the READ ENABLE (RE) and WRITE ENABLE (WE) signals, provide access to 5 internal registers. These registers contain DATA, COMMAND, SECTOR NUMBER, TRACK NUMBER, and STATUS information. The DATA REQUEST (DRQ) signal tells the Processor that a full 8 bit word has been received (sent) during a READ (WRITE) operation. INTERRUPT REQUEST (INTRQ) is used to signal the processor on completion of each command.

The Disc Interface section contains the logic to control the DISC DRIVE.

Table 10.0 Disc Interface signals on the FDC

Outputs	Description
WG	Write Gate
$\overline{WD}$	Write Data
$\overline{STEP}$	Step pulses to the Drive's stepper motor moving the head assembly
$\overline{DIRC}$	DIRection Control, controls the direction of the head assembly motion.
RG	Read Gate
EARLY	Control for the write pre-compensation circuit
LATE	Control for the write pre-compensation circuit

Inputs	Description
$\overline{RAW\ READ}$	Serial pulse stream from the disc drive
RCLK	Read Clock, generated by the Phase Locked Loop
$\overline{IP}$	Index Pulse indicator
$\overline{WPRT}$	Write Protect switch indicator
READY	Drive Ready indicator (DISC CHANGE signal)
$\overline{TR00}$	Track 0 Indicator, indicates that the disc drive's head assembly is positioned on track number 0.

3.4.3 WRITE PRECOMPENSATION (9)

Write precompensation is a technique that is used to reduce the effects of bit shift (see Fig 2). Data pulses are time shifted prior to being written, in the direction opposite the anticipated bit shift. The FDC provides the EARLY and LATE signals, which are used to perform the write precompensation. The internal algorithm for the precompensation is described in the following table.

Table 11.0 Internal Write Precompensation algorithm

Already sent		Sending	To be sent	Precompensation (MFM) required
X	1	1	0	EARLY
X	0	1	1	LATE
0	0	0	1	EARLY
1	0	0	0	LATE

X = don't care
All other combinations = NO Precomp (nominal)

In order to eliminate the effect of jitter in the FDC WRITE DATA generation circuitry, each WRITE DATA (WD) pulse is resynchronized (U45) with the 1 MHZ clock prior to precompensation. This delay necessitates latching the EARLY and LATE signals from the FDC for later use. The rising edge of WD clocks the values of LATE and EARLY into flip-flops (U39). At the same time, WD presets the first U45 flip-flop. The next high to low transition of 1MHZ clocks a "1" into the second U45 flip-flop. A high level is then present at the serial input of the LS164 shift register (U48), which is clocked with the 8MHZ clock. This creates a 250 ns pulse which propagates through the shift register with a 125 ns time difference between each output. The latched EARLY and LATE signals are used to select the appropriate shift register output for the serial pulse stream (QA=EARLY, QB=NOMINAL, QC=LATE).

3.4.4 PHASE LOCKED LOOP (8)

3.4.4.1 Introduction

The Phase Locked Loop (PLL) is the most critical part of the DATA DECODER. It is responsible for creating a clock signal in phase with the incoming READ DATA pulses. The FDC (U18) uses this phase information to decode the MFM encoded data. For a given READ DATA signal quality (noise, jitter, etc...), the PLL accuracy determines the quality of the data recovery operation. It must be able to LOCK on the input pulses, and TRACK slow variations in the input pulse period (disc rotation speed variations).

The PLL contains three (3) major functional blocks: the Voltage Controlled Oscillator (VCO), the Phase Detector, and the Synchro Detection & Locking Logic.

The VCO generates a free running frequency of about 470 KHZ. The Synchro detection & Locking logic detects the SYNCRONIZATION FIELDS in the pulse stream, and issues the FAST LOCK, RESET, and CLAMP signals to the Phase detector and VCO. The Phase detector generates the control voltage for the VCO. It compares the relative phases of the VCO and the data pulses, and changes the control voltage so that the VCO is locked to the phase of the READ DATA pulse stream. The output of the VCO is divided by two to create the READ CLOCK (RCLK) signal which the data separator inside the FDC uses to recover the encoded data.

See Figures 3 to 7 for block diagrams, operation, and timing diagrams of the PLL.

3.4.4.2 Voltage Controlled Oscillator

The VCO contains three sections: a Ramp Generator, a Comparator with hysteresis, and a Voltage/current converter. The operation of the circuit can best be described by analyzing the two states of the oscillator output.

First, assume that the oscillator output is low (Figure 7A). Q14 is OFF, and Q15 is ON. Since Q14 is OFF, Q12 and Q13 are also OFF. Current I1 through Q15 and Q16 discharges capacitor C34. When the voltage on C34 reaches the low-going threshold of the comparator hysteresis (2.4 V, set by R13, R14), the comparator output switches to a high level.

When this happens (Figure 7B), the base of Q14 is one diode higher than the base of Q15 , Q14 is ON, and Q15 is OFF. Now current I1 flows through Q12, Q14, and Q16. Q12 and Q13 are connected in a current mirror arrangement; if I1 flows through Q12, the same current flows through Q13. This current charges capacitor C34. When the voltage on C34 reaches the high-going threshold of the comparator hysteresis (5V) the comparator output changes state, returning to the low level.

The frequency of the oscillator is set by the values of the hysteresis levels, current I1, and the value of capacitor C34:

$$f = \frac{I1}{2\,(Vhmax - Vhmin)\,C34}$$

The control current I1 is generated by the V/I converter Q17, Q16, and R38. The input to this V/I converter is the output of the Phase Detector filter.

The circuit formed by Q10, Q11, and Q18, sets the control voltage on C37 when the loop is reset. When RESET is asserted, Q11 is OFF, keeping the JFET Q10 ON. The voltage on the collector of Q18 (-5.2 V) is then applied to C37 through the small Ron of the JFET. This voltage is converted to an I1 value which sets the FREE RUNNING FREQUENCY of the oscillator (about 470 KHZ). This frequency is chosen to be close to twice the expected data frequency.

When RESET is not asserted, Q11 is ON and Q10 is pinched OFF. In this state the filter voltage is allowed to move in response to correction currents from the Phase Detector.

The CLAMP input to the VCO allows the Synchro detection & Locking logic to stop the VCO , and then restart it in phase with the incoming data pulses (see Section 3.4.4.4).

3.4.4.3 Phase Detector

The Phase Detector generates the control voltage used by the VCO. To perform this function, it receives three inputs: the window pulses, the ramp signal from the VCO, and the output of the VCO. The ramp voltage is buffered by a darlington-connected emitter follower (Q2 and Q3). The triangle voltage at the emitter of Q3 is converted into a triangle current through Q4 and Q5.

The Phase Detector functions only during the 250 ns window created by the delay line as a result of a READ DATA pulse.

The operation of the Phase Detector will be described in the same way as the VCO, assuming that the window signal is asserted (high). When the oscillator output is low, Q6 is ON, and Q7, Q8 and Q9 are OFF. Current I2, set by current source Q4, flows through Q6 and charges capacitor C37 (IF = I2). When the oscillator output is high, Q6 is OFF, and Q7, Q8, and Q9 are ON. Current I2 flows through Q4, Q7, and Q9. The current mirror Q8-Q9 forces the same amount of current (-IF) to flow through Q8, discharging capacitor C37.

When the PLL is locked to the data stream, the 250 ns window resulting from the READ DATA pulse is centered around the lowest point of the ramp signal in the VCO (Figure 5A). The current into capacitor C37, is shown in Figure 5B. When the voltage ramp slope is negative, IF is a charging current; when the voltage ramp slope is positive IF is a discharging current. The amount of charge transfered to or from C37 is proportional to the area of the shaded triangles on Figure 5B.

If the input data pulse is not centered around the ramp minimum point (i.e. it is not in phase with RCLK), the frequency of the oscillator is modified so that the next data pulse will have less phase difference with RCLK. Figures 5C and 5D illustrate this frequency modification. If the data pulse is late (Figure 5C), the discharge time is greater than the charge time, so that the net charge into C37 is negative. The control voltage to the VCO decreases, I1 decreases, and the slope of the ramp signal decreases. This reduces the frequency of the VCO. Figure 5D shows the net positive current into the filter resulting from an early data pulse.

Because of the integration of the filter, the action of the Phase Detector is not instantaneous. It averages over a large number of data pulses to modify the VCO control voltage. Because of this, it tracks the slow disc speed variations without tracking the data pulse jitter, which could lead to read errors.

During data reading the Phase Detector gain is set by the current flowing through current source Q4 (TRACKING gain value). During LOCKING it is desirable to increase the Phase Detector gain to reduce the lockup time. This is done by the FAST LOCK signal, which allows current source Q5 to sum in parallel with Q4. When FAST LOCK is asserted, the Phase Detector gain increases to the LOCKING value, which is five times the TRACKING value.

3.4.4.4 Synchro Detection and Locking logic

The purpose of this circuit is to detect the SYNCHRONIZATION FIELDS (SYNC fields) in the serial data pulse stream, and to provide the VCO with the signals necessary to LOCK to the data pulses in the SYNC field (See Figures 6 and 7). In the format used in this system, a SYNC field is composed of 12 bytes of "00" HEX, which is encoded as equally spaced transitions in MFM coding (4uSec period). See MFM patterns, Figure 12.

The phase locked loop continually attempts to lock on the data pulse stream. The Synchro Detection and Locking Logic resets the loop if any of the following conditions becomes true:

1) The separation between data pulses is >= 5 uSec and READ GATE is not asserted (the current data is not a SYNC FIELD),
2) The FDC does not assert READ GATE within 10 bytes of the beginning of the SYNC FIELD (the FDC does not intend to read),

or 3) The FDC deasserts READ GATE sometime after the 10th byte (the FDC has completed reading or did not find the address mark).

The operation of the synchro detection & locking logic can be described by looking at the sequence of events starting with the occurence of one READ DATA pulse. Assume the following starting conditions:

a) READ DATA is not asserted (the pulse has not arrived yet),
b) S/R flip-flop U35 is reset (output low),
c) Shift register U63 is cleared,
d) FAST LOCK is asserted,
e) RESET is asserted,

and f) CLAMP is not asserted.

Refer to the schematic (Figure 19), the Synchro Detection and Locking Logic Block diagram (Figure 6), and the Clamp and Locking Timing diagram (Figure 7.0).

Each delayed (250 nSec) READ DATA pulse clears shift register U62. If U62 is clocked by the 1 MHZ clock 5 times without being cleared, the period between data pulses is greater than 4 uSec. Therefore, the field currently being read is NOT a SYNC FIELD. Output QE of U62 going high clears counter U46 and sets the S/R flip-flop U35. This clears shift register U63. The synchro detection circuit is then completely reset.

If the QE output of U62 is never asserted (i.e. the data pulses are < 5uSec apart), each data pulse clocks the 4 bit counter U46. Each 16 data pulses (2 bytes), shift register U63 is clocked. After two bytes, RESET is deasserted. At this time, the CLAMP signal (U59) is asserted, reseting the phase of the VCO. The next data pulse clocks a "1" into flip-flop U49, deasserting CLAMP. The VCO ramp is released with a well defined phase relation with the incoming READ DATA pulses. This completes the fist part of the locking process.

At this point, the VCO still oscillates at the FREE RUNNING FREQUENCY. The Phase Detector extracts the phase information and modifies the control voltage to the VCO for the next 8 bytes. During this period of time FAST LOCK is asserted, and the Phase Detector gain is at the LOCKING value. After 10 bytes, output QE of U63 goes high, deasserting FAST LOCK. This reduces the Phase Detector gain to the TRACKING value. By this time the FDC (U18) will have asserted the Read Gate (RG) signal if it intends to read. This forces the reset of S/R flip-flop U35, so that shift register U63 cannot be cleared again. When the FDC finishes reading the ID field or DATA field, READ GATE is deasserted. This allows the SYNCHRO DETECTION LOGIC to reset itself. If RG has not been asserted by the twelfth byte of the sync field, output QF of U63 goes high and sets the S/R flip-flop U35. This clears shift register U63 , and the synchro detection logic is reset.

4.0 DRIVE ELECTRONICS PCA THEORY OF OPERATION

Refer to Figure 8 for the MINIFLOPPY DRIVE ELECTRONICS PCA block diagram, Figure 20 for the schematic, Figures 9 through 11 for timing diagrams, and Figure 21 for the component location diagram. All are located in SECTION 7.0.

4.1 GENERAL OVERVIEW

The MINIFLOPPY DRIVE ELECTRONICS PCA consists of three major blocks: the CONTROL LOGIC, the WRITE CIRCUIT, and the READ CIRCUIT. The WRITE CIRCUIT creates magnetic transitions on the disc by switching current through the read/write head coil. These transitions are converted back to digital form by the READ CIRCUIT. The CONTROL LOGIC supports these and other essential functions such as index hole detection, head positioning, and track 0 position sensing.

Both the encoding and decoding of the digital data is performed by the MINIFLOPPY CONTROLLER module.

4.2 CONTROL LOGIC

4.2.1 UNIT ADDRESS DECODER

The controller/drive interface allows independent function selection for each drive. When the Z80-A on the MINIFLOPPY CONTROLLER module writes to one of the drive function registers, the addressed drive latches the information on the deassertion of STROBE. The "addressed drive" (U24-1) is the drive which receives an INPUT ADDRESS of 00.

4.2.2 NEXT DRIVE ADDRESS GENERATOR

The NEXT DRIVE ADDRESS GENERATOR modifies the INPUT ADDRESS to create the OUTPUT ADDRESS. The OUTPUT ADDRESS is connected to the INPUT ADDRESS of the next drive by the T-BLOCK (see Section 6.0). This alteration of the drive address as it propagates down the daisy chain assures that only one drive will be the "addressed drive", even though all drives are decoding for an INPUT ADDRESS of 00. The following truth table summarizes the function of the NEXT DRIVE ADDRESS GENERATOR:

Table 12.0 Next Drive Address Generator truth table

INDA1	INDA0	OUTDA1	OUTDA0
0	0	1	1
0	1	0	0
1	0	0	1
1	1	1	0

It should be noted that the progagation delay through the NEXT DRIVE ADDRESS GENERATOR (45 nSec. max.) increases the required DRIVE ADDRESS -> STROBE setup time as additional drives are added to the daisy chain.

4.2.3 FUNCTION SELECT LATCHES

Four FUNCTION SELECT signals are latched on the deassertion edge of the STROBE signal: DRIVE SELECT, SIDE SELECT (U13), MOTOR ON, and HEAD LOAD (U23). The outputs of these latches are used on the board to define the state of the drive. This gives the controller the flexibility to perform some simultaneous operations (e.g. both motors spinning for disc-to-disc copying) and some staggered operations (e.g. motor turn-on) on two drive systems. Since the unlatched function select signals are not used on the board, any reference to these signals is intended to mean the latched signals.

The "selected drive" is the drive on which DRIVE SELECT is asserted. This is the drive which is chosen for reading, writing, seeking, or returning status. Only the "selected drive" enables the output buffers which drive the signals that are wired in parallel on the drive/controller interface. A drive may be deselected in one of two ways: 1) the controller writes an explicit deselect command to the drive, or 2) the controller writes a select command to another drive. Circuitry (U62, 63) was included to deselect the drive when another drive was selected to avoid buffer contention on the interface. DRIVE SELECT is also buffered (U22) to drive the front panel LED.

The state of SIDE SELECT determines which head is biased in the active state (read or write). When SIDE SELECT is asserted, HEAD 1 (the top head) is active.

When MOTOR ON is asserted, the servo board is commanded to start the spindle motor and regulate its speed. The starting of the spindle motors in the two drive system is staggered to reduce the peak current requirements of the system.

HEAD LOAD is normally used to control a solenoid which lowers the top head on to the disc. Since the top head is loaded when the door is closed on the Tandon drive, this signal has no mechanical effect. However, it is used to multiplex between the DISC ID CODE (head unloaded) and two status signals (head loaded). See Section 4.2.4 for more information.

The assertion of the POWER-ON RESET signal initializes the function select latches to the following state:

Table 13.0 State of the Function Select Latches after initialization

Signal	State
DRIVE SELECT	Deselected
HEAD LOAD	Unloaded
MOTOR ON	Deasserted
SIDE SELECT	Side 0

4.2.4 DISC ID

The DISC IDENTIFICATION code (U15-14,3,16) is a three bit number that tells the controller what type of drive is connected to it. This allows the controller to control drives with different capacities, step rates, etc. In addition, an ID code of 7 indicates that there is no drive connected. The ID code is read by the controller from the Potpourri Register when HEAD LOAD on the selected drive is not asserted. The ID code for the Tandon TM100 drive (DRIVE ELECTRONICS PCA 13270-60002) is 0.

When HEAD LOAD is asserted, DISCID0 and DISCID2 have different meanings. DISCID0 (U15-14) becomes the output of the "Missing Pulse" one-shot multivibrator (U14-4). The assertion of this signal means that there has not been an INDEX PULSE in the last 465 mSec. This implies that the disc is not inserted or is not spinning.

With HEAD LOAD asserted, DISCID2 (U15-16) becomes the output of the "9 uSec" one-shot multivibrator (U14-12). This one-shot is used in self test routines to determine if two adjacent data pulses are more than 9 uSec. apart. The ideal maximum separation is 8 uSec. for the 10101 pattern. The input to the one shot (U22-6) is READ DATA during a read operation and WRITE DATA during a write operation.

4.2.5 DISC CHANGE

The DISC CHANGE signal (U15-5) indicates that there has been a change in the state of the WRITE PROTECT switch. Generally, this means that a disc has been removed from or inserted into the drive. This signal is used by the MINIFLOPPY CONTROLLER module to prevent inadvertant writing on a newly installed disc. It also allows the file system to automatically mount new volumes.

The output of the WRITE PROTECT switch is used to generate DISC CHANGE. The switch signal is filtered by R81, R10, and C55 to prevent false triggering from mechanical vibration. After buffering (U43), this signal drives a bidirectional one-shot multivibrator (R71, C44, U53) which creates a pulse on each transition of the switch. These pulses set a flip-flop (U54) which retains the information until the controller clears it. DISC CHANGE is cleared when the controller writes to the function register of the addressed drive with DRIVE SELECT, HEAD LOAD, and MOTOR ON all deasserted.

4.2.6 STEPPER MOTOR LOGIC

A four phase stepper motor is used to position the head mechanism over the target track. It is controlled by a 2 bit shift register (U52) which is clocked by step pulses from the MINIFLOPPY CONTROLLER MODULE. The DIRECTION (DIRC) signal from the controller determines the stepping direction. When DIRC is asserted, step pulses change the phases to cause the stepper motor to move the head toward the inner (higher numbered) tracks. The following table shows the required state of the phases of the stepper motor for each track:

Table 14.0 Phases of the Stepper Motor

Track	Phase 1	Phase 2	Phase 3	Phase 4
00	ON	OFF	OFF	ON
01	ON	ON	OFF	OFF
02	OFF	ON	ON	OFF
03	OFF	OFF	ON	ON
***				
4N	ON	OFF	OFF	ON
4N + 1	ON	ON	OFF	OFF
4N + 2	OFF	ON	ON	OFF
4N + 3	OFF	OFF	ON	ON

The outputs of the shift register are buffered (U32) to handle the current and voltage requirements of the stepper motor.

In addition to the shift register, logic is included to inhibit stepping when the write current is flowing (U63-6), or when track 0 is reached while stepping out (U12-11). The stepper motor phases are initialized to the track 0 state by the assertion of power-on reset (POR).

4.2.7 TRACK 0

The TRACK 0 (TR00) signal indicates to the controller that the head assembly is located at physical track 0 (the outermost track). This signal is derived from the output of a mechanical switch ANDed with the appropriate phases of the stepper motor (1 and 4). The switch output is debounced using an R-S flip-flop (U12). The electrical state of the stepper motor is needed to precisely define track 0 because of the mechanical tolerance of the switch mounting.

4.2.8 INDEX

The INDEX hole in the disc provides the controller with a time reference point during each revolution of the disc. The INDEX signal is also used by the controller during self test to time the rotation period of the disc. In addition, this signal is the input to the "Missing Pulse" one-shot, which determines if the disc is spinning (see Section 4.2.4).

The index hole is detected by an infrared emitter and phototransistor detector mounted on the drive mechanism. The phototransistor current is converted to a voltage by R7, and this voltage is compared (U45) to a reference voltage of 1.66V formed by R13 and R14. The comparator has a hysteresis of +- 0.2V to prevent oscillations at the edge of the hole.

4.3 WRITE CIRCUIT

The write circuit creates magnetic flux transitions on the disc by switching current through the read/write head coil. In addition, the written track is trimmed by the erase field to prevent intertrack crosstalk. In order to write on the disc, five conditions must be met:

1) The drive must be selected,
2) WRITE GATE (WG) must be asserted,
3) WRITE PROTECT (WRPT) must be deasserted (i.e. the disc must not have a write protect tab on it),
4) POWER-ON RESET (POR) must be deasserted,

and 5) the power supplies must be high enough to satisfy the requirements of the glitch protect circuit (see Section 4.3.1).

4.3.1 GLITCH PROTECT CIRCUIT

The GLITCH PROTECT CIRCUIT prevents spurious writing or erasing when the power supplies are not fully up. The circuit consists of two comparators which independently sense the +5V and +12V supplies. The composite output (U66-7) grounds the write and erase current enable signals until the conditions for both comparators are satisfied.

The +5V supply is sensed by U45-11,10,13. A fraction of +5V (R40,R41) is compared with the zener diode reference formed by CR1 and R29. When the +5V supply is less than 4.35 +- 0.34 V and the +12V supply is within specification (+-5%), the output of the comparator will be low. This insures that the conditions required by the +12V comparator to permit writing will not be satisfied.

A fraction of the +12V supply (R24,R27) is also compared with the zener diode reference (U45-5,4,2). If the +12 V supply is less than 10.4 +- 0.83 V or if the +5 V comparator is not satisfied, the output of the +12V comparator (U45-2) is off. This allows R43 and/or R45 to supply base current to U66-6, insuring that output U66-7 is asserted.

The output of the glitch protection circuit (U66-7) is also connected to the clear input of the erase current turn-off delay one-shot (U44-3, see Section 4.3.4). This prevents the one-shot from being triggered as the supplies are coming up and remaining triggered after the glitch protection circuit is satisfied. In addition, the output is also tied to the clear input of the "Missing Pulse" one-shot (Section 4.2.4), so that the controller will get a "drive not ready" indication when the supplies are not high enough to permit writing.

4.3.2 HEAD CENTER TAP BIASING

The function performed by the read/write head is determined by the biasing of the head center tap. The voltage at U46-7 is applied to the appropriate center tap by transistors U46-3,2,1 and U46-12,13,14 based upon the state of the latched SIDE SELECT signal. For reading, transistor U46-5,6,7 is off and the center tap voltage of the active head is set by zener diode CR3 (6.8V), diode CR2 and the saturation voltage of the side selection transistor. For a write operation, transistor U46-5,6,7 is saturated, and the center tap of the active head is biased at approximately 11.6 volts. For both reading and writing, the center tap of the inactive head is biased to ground by R48 or R47. The following table summarizes the center tap biases for each function.

Table 15 Center tap biasing

Function	Head 0 C.T.	Head 1 C.T.
Read head 0	6.0 V	Ground
Write head 0	11.6 V	Ground
Read head 1	Ground	6.0 V
Write head 1	Ground	11.6 V

4.3.3 WRITE CURRENT SOURCE

When the conditions are met for a write operation (see Section 4.3), transistor U46-3,2,1 is switched on. This puts 0.2 V on one side of R52. The voltage on the other side of R52 (3.6 V) is set by R72 and either R67 or R68, depending on the state of flip-flop U51. The "write current" through R52 (3.2 mA +- 10%) is directed alternately through the two halves of the read/write coil by transistors U66-12,13,14 and U66-10,9,8. Refer to Figure 9 for the timing of the waveforms in the write circuit. The direction of the turns in the coil is arranged such that the disc oxide coating is magnetized in opposite directions by the current through the two halves. The leading edges of the WRITE DATA pulses from the CONTROLLER MODULE toggle flip-flop U51. Each change of state of this flip-flop causes a magnetic transition to be written on the disc.

4.3.4 TUNNEL ERASE

During writing, a 0.33 mm. wide data track is recorded. To prevent crosstalk between adjacent tracks, the edges of the track are "tunnel" erased to leave a 0.30 mm. track on the disc. The erase function is performed by passing a DC current of 79 +- 9.0 mA through the erase coil (U32-16, R54).

The tunnel erase gap is located 0.914 +- 0.051 mm. behind the read/write gap (i.e. a given point on the disc will pass the erase gap after the read/write gap). This requires a time delay in turning on and off the erase current with respect to the write current (see Figure 10). The turn-on delay (253 uSec. nominal) is provided by a one-shot multivibrator (U44-12) which is triggered when writing commences. The turn-off delay (1.07 mSec. nominal) is created by another one-shot multivibrator (U44-13). This circuit is triggered at the beginning of writing and is retriggered by every other WRITE DATA pulse. The erase current is turned on after the first one-shot pulse and remains on until the second one-shot times out. In addition, the output of the turn-off delay one-shot is used to switch the head center-tap biasing circuit from the read state to the write state. This keeps the center tap of the head up at the writing voltage from the beginning of writing until the erase current is turned off. The turn-off delay one-shot is cleared by the glitch protect circuit to prevent erase glitches during power supply transitions.

4.4 READ CIRCUIT

The read circuit takes the signal from the head coil and, after amplificaton, filtering and differentiation, creates a READ DATA pulse for each magnetic transition. Please refer to Figure 11 for waveforms in various parts of the read circuit.

4.4.1 PREAMPLIFIER AND FILTER

When the center tap of one of the heads is biased for reading (see Section 4.3.2), the head signal is passed through two pairs of diodes to the input of the preamplifier (U74). This differential amplifier has an AC gain of 250 - 400, which increases the signal amplitude to a minimum of 200 mV peak-to-peak. The output of the preamplifier is filtered by a low-pass three pole Bessel filter to attenuate high frequency noise.

4.4.2 DIFFERENTIATOR AND COMPARATOR

The signal from the output of the Bessel filter is passed through a band pass filter (U72) which effectively differentiates the signal. (see Figure 11c). The signal then goes to a differential comparator (U61), which senses the zero crossings of the differentiated head waveform. These zero points correspond to the peaks of the original head signal (i.e. the center of the magnetic transitions sensed by the head coil). The output of the comparator is a single-ended TTL compatible waveform.

4.4.3 DROOP REJECTION CIRCUIT

Under certain circumstances, the comparator senses zero crossings which do not correspond to flux transitions. These extra zero crossings are caused by "differentiator droop". Differentiator droop results when a high resolution system (head and disc) encounters the 1010101 pattern (8 uSec. spacing) on an outside track (See Figure 11). The relatively flat slope between the two peaks causes the differentiator output to "droop" to zero.

These extra comparator crossings are removed by a time domain filter. The output of the comparator triggers a bidirectional one-shot multivibrator (R35, C21, U31), which generates a pulse for each comparator transition (Figure 11e). These pulses trigger another one-shot multivibrator (2.24 uSec., see Figure 11f). The trailing edge of the pulse from the 2.24 uSec. one-shot clocks the state of the comparator output into a flip-flop (U51). The output of the flip-flop follows the comparator output except for a time delay of 2.24 uSec. In addition, the false transition is removed because the comparator output is back in the correct state by the end of the delay. Q1, R8, C5, C8, and U35 form a pulse stretcher which guarantees a wide enough pulse ()40 nSec.) to trigger the 2.24 uSec. one-shot.

The output of flip-flop U51 triggers a bidirectional one-shot multivibrator (R36, C22, U31), which generates a pulse on each transition. These pulses are stretched by a one-shot multivibrator (U21) to 750 nSec. before being sent to the CONTROLLER MODULE as READ DATA.

5.0 DRIVE MECHANISM

The Disc Drive contains the mechanical parts, sensors, and control circuits necessary to rotate the disc and position the head carriage. It interfaces to the DRIVE ELECTRONICS PCA through 9 connectors described in Tables 5.0 to 5.8, Section 2.0.

The disc is rotated on a spindle assembly driven by a DC motor-tachometer combination through a belt. The speed of the spindle motor is set by the Servo Control PCA, mounted on the back of the drive. The disc rotational speed is 300 rpm +/- 1.5 % (average).

See Section 4.2 for details on the interface between the Drive Mechanism and the DRIVE ELECTRONICS PCA.

6.0 TWO DRIVE SYSTEM CONNECTION

In the two drive system, the second drive is added using the T-BLOCK and the NEXT DRIVE CABLE. The T-BLOCK is mounted on the back of the first drive, providing a connection port for the NEXT DRIVE CABLE. This allows DRIVE 1 to modify the drive address signals before they are sent to DRIVE 2. (see T-BLOCK schematic, Figure 12). All other signals are wired in parallel to both drives.

7.0 FIGURES AND DIAGRAMS

LIST OF FIGURES

APPENDIX A. HP PHYSICAL FORMAT FOR 5.25" FLEXIBLE DISCS.

2 Sides/Disc
35 Tracks/Side
16 Sectors/Track -- MFM Encoding (4 uSec. bit cell)

Number of bytes	Hex Value	Description
85	4E	Post-index gap
16	4E	Sector preamble
12	00	ID sync field
3	A1*	
1	FE	ID address mark
1	XX	Cylinder number
1	XX	Head number
1	XX	Sector number
1	XX	Sector length
2	XX	CRC
22	4E	ID Gap
12	00	Data sync field
3	A1*	
1	FB	Data address mark
256	XX	Data
2	XX	CRC
28	4E	Sector postamble
155	4E	Pre-index gap

Repeated 16 times, once per sector

Notes:

* Missing clock transition between bits 4 and 5.

1. The Tracks on the disc are organized in cylinders. There are 35 cylinders in a disc. Each cylinder consists of 2 tracks, one on each side of the disc. Cylinder numbering begins at 0 (the cylinder with the largest radius). Invisible tracks have cylinder = FF.

2. Head 0 is the lower head. Head 1 is the upper head. Invisible tracks have head number = FF. Defective tracks have bit 5 of head number set to 1. (Bit 0 = LSB)

3. Sector numbering begins at 0. Invisible tracks have sector number = FF.

4. Data length = $2^{7 + \text{sector length}}$; where sector length = 0, 1, 2, 3.

5. Cyclic Redundancy Check (16 bits). The polynomial is:
   $G(X) = X^{16} + X^{12} + X^{5} + X^{1}$. The CRC register is initialized to ones and includes all information starting with the address mark and up to the CRC characters.

6. The minimum Pre-index gap size is 155 bytes based on formatting on a drive which is 3.6% fast. Additional bytes (4E) are written until the index pulse occurs.

APPENDIX B. MODIFIED FREQUENCY MODULATION CODING

B.1 GENERAL.

The information stored on the disc is organized in concentric tracks. Each track consists of a continuous string of sectors, each of which contains a group of 256 bytes. Data is recorded in a sector on a bit-serial basis. Bits of information to be stored are first encoded, then recorded in a specific sector.

The data encoding process specifies a one to one relationship between any given information-bit and the associated sequence or sequences of flux transitions to be recorded on the disc in accordance with the specified rules. A flux transition is defined as the transition of magnetization written by a unit step change of write current, on the disc. An algorithm which produces this sequence of flux transitions for a given information-bit pattern is defined as the recording code. For the code to be useful, this one to one relationship must be unique.

For the purpose of encoding and recording information on the disc, a track is devided into equal elements defined as information-bit cells. Each contains one encoded bit of information. The information bit cell is further partitioned into the boundary-half-bit cell and the center-half-bit cell. The boundary-half-bit cell occupies the half-bit space beginning at the imaginary information-bit boundary. Similarly, the center-half-bit cell occupies the half-bit space beginning at the center of the information-bit cell. (Figure 14)

The data-encoding algorithm is restricted to flux transitions only at half-bit boundaries, which implies that the flux transition intervals will allways be multiples of the half-bit distance. Each boundary-half bit and center-half-bit assumes a value of either one or zero. The magnetization in the erase direction (arbitrarily defined) represents a binary zero, and the magnetization in the direction opposite to the erase represents a binary one. The values of half-bits can change only at the half-bit boundaries, each of which changes represents a transition of magnetization (flux transition).

The data-encoding algorithm produces a sequence of half-bit values to be recorded as magnetization states for a given information-bit pattern. The magnetization states within an information-bit cell can, therefore, be characterized by a pair of half-bit values. The four possible conditions of magnetization within an information-bit cell are designated by half-bit value pairs: ⟨00⟩, ⟨01⟩, ⟨10⟩, ⟨11⟩.

B.2 MODIFIED FREQUENCY MODULATION (MFM) ENCODING

A recording code can be characterized by a sequential machine whose next state is determined by the present value of the input (information bits) and the present state (past history). For a recording code, the magnetization states within an information-bit cell depend not only upon the present value of the input, which in this case happens to be incoming information-bits to be recorded on the disc , but also upon the magnetization states in the previous information-bit cells. Therefore, the data encoding algorithm for a recording code can be represented by the state diagram of a sequential machine. The incoming information-bits cause the machine to sequence through states determined by it's state diagram. The next state transitions in the machine occur at information-bit boundaries. Each machine state is assigned a pair of half-bit values which specifies magnetization states within an information-bit cell.

Definition of the MFM encoding algorithm:

A flux transition is always recorded at the center of the information-bit cell for each incoming information bit with a value of binary one. No flux transition is recorded for the information bit with a value of binary zero, unless it is followed by another information-bit with a value of binary zero, in which case the flux transition is provided at the end of the first information-bit cell.

The sequential machine describing this algorithm has four states, A(00), B(01), C(10), D(11). The state diagram for it is described in fig 13. Fig 14 shows what should be the output of the encoder implementing this algorithm.

The MFM code is self-clocking, that is, it contains at least one transition every two information-bits. This property is useful during decoding of the data read from the recording system, as it allows to reconstruct a clock signal from the information-bit stream itself.

B.3 MODIFIED FREQUENCY MODULATION (MFM) DECODING

During the read operation, the magnetic recording system produces an electrical pulse for each flux transition on the recorded disc. The function of the decoding circuit is to reconstruct the binary information carried by these pulses. In order to perform this task, it needs to create a clock signal in phase with the incoming data pulses, which will clock the decode algorithm state machine. The decode algorithm state machine is the counterpart of the coding algorithm. It has four states, with an associated binary value: A(0), B(1), C(1), D(0). Depending on the present state and the present input (half-bit values), the algorithm determines the next state. Figure 15 shows the decoding algorithm state machine, and Figure 16 is the associated timing diagram.

APPENDIX C. SELF TEST FLOWCHART AND ERROR CODES

C.1 OVERVIEW

1) POWER-ON

Non-Destructive Test (Self Test on Controller PCA)

2) PROGRAMMATIC

A Disc Self Test is performed upon recept of an "Initiate Self Test" disc command by the Controller. The control word received by the controller indicates whether to perform a destructive (write/read operations on disc) or nondestructive Self Test. Destructive Self Test will reformat and write the worse case data patterns on the selected test cylinder. When the CONTROLLER completes the test, the Terminal sends it a "Read Self Test" command to obtain the result of the test.

3) LOCAL

Insert jumper to execute self-test loop (jumper location is indicated in section C.2). The self-test jumper can be inserted at any time, before or after power-on. If a disc is inserted in a drive, a destructive (write/read) test is initiated. The write test reformats and writes the worst case data patterns on test cylinder 34 (worst case cylinder). If an error is found the program loops around the failing test. The LEDs on the Controller PCA indicate the failing test number. If no error is found, the LEDs remain OFF, and the self-test restarts after two seconds.

C.2 SELFTEST RESULTS

Two bytes are returned by the CONTROLLER in response to the "Read Self Test" command. They have the following format.

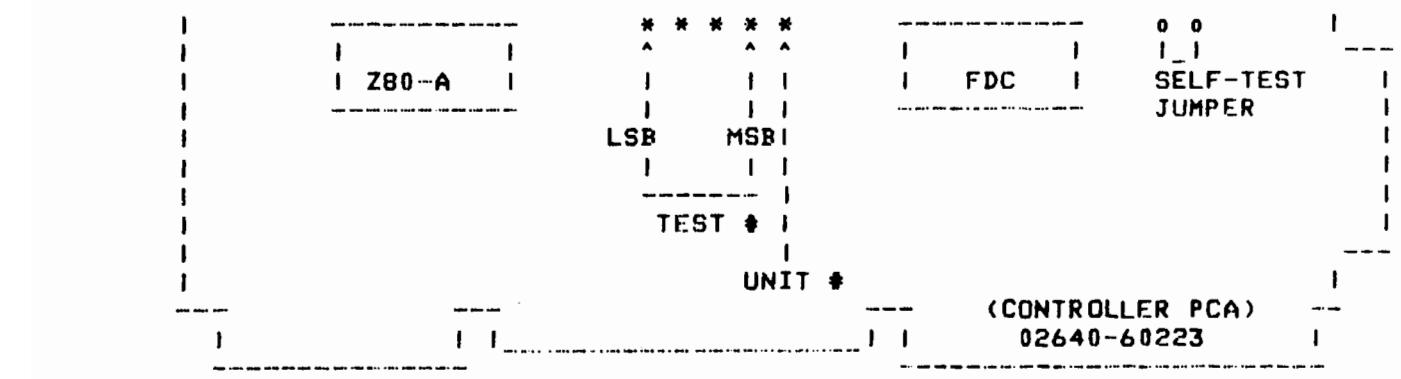
```
+*********+ +*********+
\EHUUXSSS\ \SSSTTTTX\
+*********+ +*********+
    MSB         LSB
```

WHERE

E	Error indicator, Set if error was encountered.
H	Head number, Indicates head on which the read or write test failed.
UU	Unit number, Indicates which unit or drive the CONTROLLER had selected at the time of the failure. The LSB of the unit # is also displayed on the rightmost LED.
SSS SSS	Subtest number, Indicates which subtest of the current test failed.
TTTT	Test number, Indicates which test failed. Also displayed on the LEDs.
X	X's are don't care states.

If no errors are detected, the two bytes returned by the CONTROLLER are ALL zeroes.

LEDs on the controller are read from right (MSB) to left (LSB).



Controller Board Test

		Selftest Error	
		Test(subtest)	LEDs
Hardware Power-on	The LEDs displays this error if the CONTROLLER can not be initialized. 1=LED ON 0=LED OFF	15(X)	1111U ^ ^^ | ||__UNIT # | | | |___MSB |_____LSB
LED Display Test	Change from 1111->0000	15(X)	1111U
ROM Test	CRC Check	4(X)	0010U
RAM 1 Test	Data Pattern (Lower 4 bits)	5(X)	1010U
RAM 2 Test	Data Pattern (Upper 4 bits)	6(X)	0110U
RAM 3 Test	Address lines Error	7(X)	1110U
FDC Test1	FDC Timeout Error	2(0)	0100U
FDC Test2	FDC Interrupt Error	9(4)	1001U
Write Test	Write Encoding circuit (performed only on destructive test)	8(6)	0001U
Z80 I/O Test	I/O and Handshake Registers	10(7)	0101U

Drive Board Test

Seek Test1	After Recalibration, Track 0 indicator was not found.	11(3)	1101U
Seek Test2	Track 0 Indicator was on when not expected.	11(5)	1101U
Seek Test3	Track 0 Indicator was not on when expected.	11(6)	1101U
No Drive	No Drives were found connected to the Controller.	11(7)	1101U
Write/Read	Write/Read Ckt Test	11(8)	1101U
9 uSec Test	Test levels of 9 uSec one shot	11(9)	1101U

Drive Test

No Index Mark	Disc present and spinning, but no Index Mark	12(0)	0011U
Speed Test1	Disc Spinning Faster than Specified Limits	12(1)	0011U
Speed Test2	Disc Spinning Slower than Specified Limits	12(2)	0011U
Missing Pulse	Missing Pulse indicator was not on when expected.	12(6)	0011U

Write Test

No Disc	No Disc inserted in Drive	13(1)	1011U
Write Protected	Selected Drive shows the Disc as being Write Protected.	13(2)	1011U
UnderRun	FDC did not receive byte before 30 uSec.	13(3)	1011U

Read Test

Not Ready	Selected Drive not ready, maybe Disc has been removed.	14(0)	0111U
No ID Field	Target ID Field was not found.	14(2)	0111U
Wrong ID Field	Some ID was found, but not the Target ID Field. Head on wrong Track (Possible Seek Error).	14(3)	0111U
CRC ERROR	Current Data Field contained a CRC Error.	14(5)	0111U
OverRun	OverRun occurred from lost data in the current read attempt.	14(6)	0111U

C.3 TEST FLOW CHART

Test group abbreviations

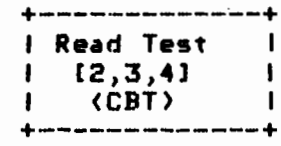
CBT- Controller Board Test
DBT- Drive Board Test
DT - Drive Test
WT - Write Test
RT - Read Test

Each box indicates which particular test is performed, with reference to the test group ( ).

Example:

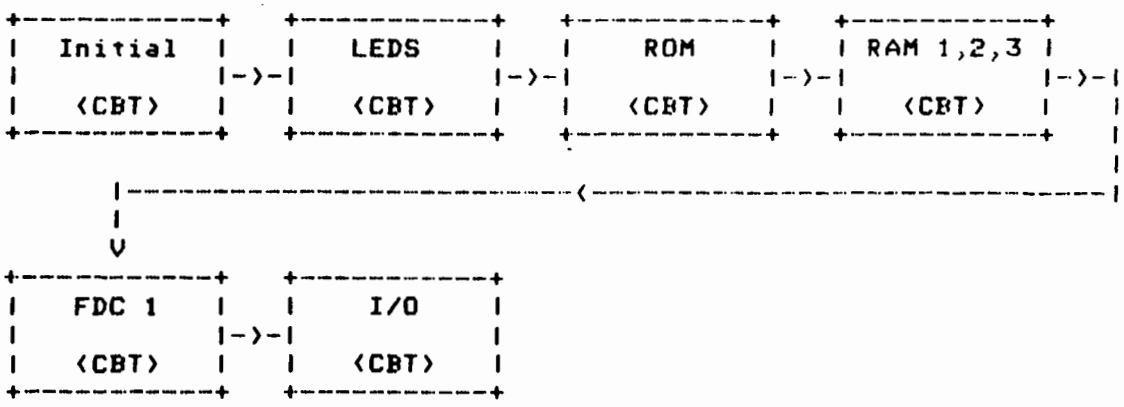
If the test is successful, the test in the next box is performed. Some of the boxes include one or more numbers in brackets [ ]. These are the sub-test branches, located at the end of this flow chart. They are executed in the order indicated within the brackets.

Example:

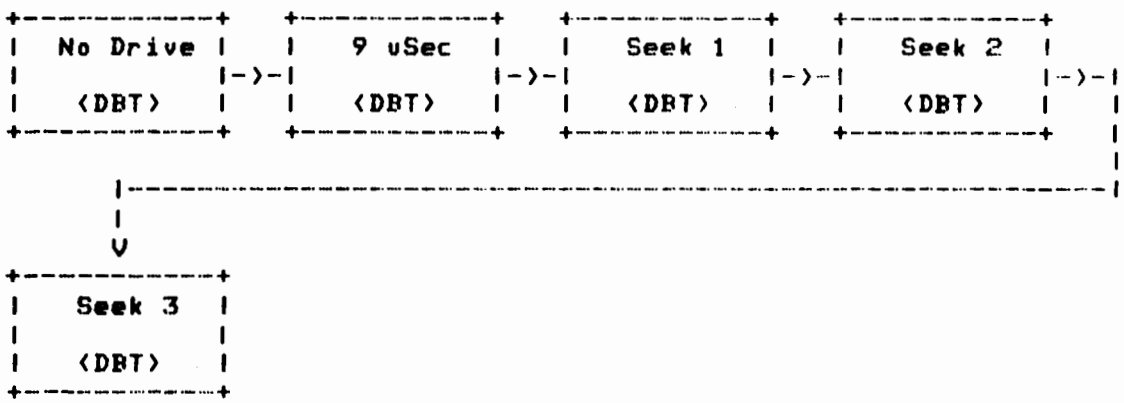


If the Read Test fails but the cause of the error is not a direct read error, the test program branches to the sub-test routines 2,3, and 4 in this order. The cause of the error will then be one of the following OverRun (sub-test 2), Missing Pulse circuit (sub-test 3), or FDC time out (sub-test 4).

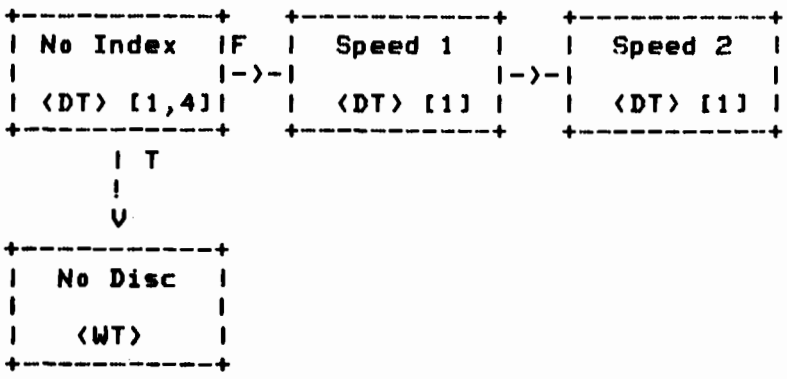
LEVEL 1 (Non Destructive Test)



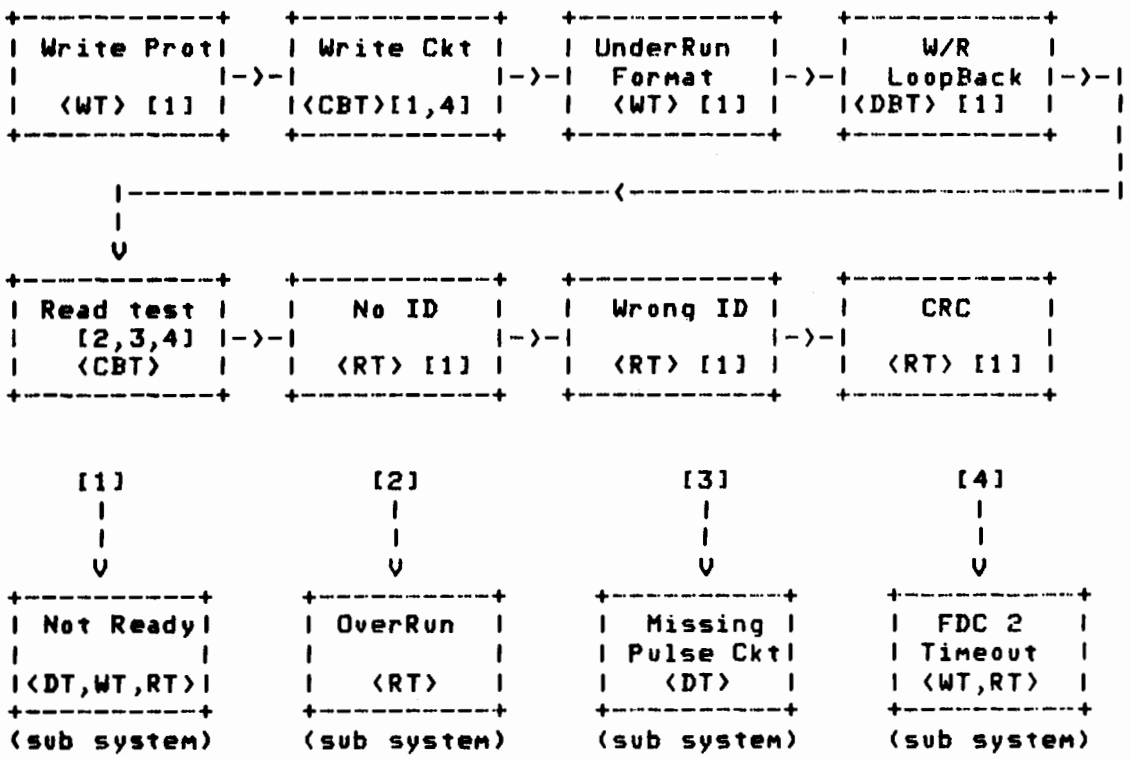
LEVEL 2 (Non Destructive Test)



LEVEL 3 (Non Destructive Test)



LEVEL 4 (Destructive Test)



C.4 SELFTEST TROUBLESHOOTING GUIDE

Controller Board

Hardware Power-on	(1) Rom (2) LED Latches
FDC Test1	(1) Floppy Disc Controller did not time out after 4 revolutions of the disc. (FDC internal timing problem)
FDC Test2	(1) Z80 processor did not receive a force interrupt from the FDC.
Write test	(1) The 9 uSec circuit detected the data pulse separation being equal to zero or greater then 9 uSec. (2) 9 uSec oneshot is defective. (3) Cable broken or not connected to drive
Z80 I/O Test	(1) Data In, Data Out, or Command Handshake registers did not toggle from one state to another.

Drive Board

Seek Test1	(1) After recalibration, the FDC did not detect track 0 indicator being set. (2) Ckt for track 0 indicator is defective. (3) Stepper motor did not move the actuator toward track 0. (4) Cable broken or not connected to drive
Seek Test2	(1) Ckt for track 0 indicator is defective. (2) Stepper motor did not move the actuator toward track 34.
Seek Test3	(1) Ckt for track 0 indicator is defective. (2) Stepper motor (same as Seek Test1)
No Drive	(1) Ckt for drive ID is defective. (2) Cable broken or not connected to drive. (3) Controller received a drive ID of 7HEX.
Write/Read	(1) The data pulse separation was zero or greater than 9 uSec from the write/read loopback circuit. (2) Write/Read circuit is defective on the drive board. (3) 9 uSec one-shot is defective. (4) Floppy Disc Controller chip is defective. (5) Cable broken or not connected to drive
9 uSec Test	(1) 9 uSec one-shot is defective. (2) Cable broken or not connected to drive

Drive

No Index Mark	(1) Index circuit is defective. (2) Photo detector or LED is defective. (3) Motor not spinning (4) Door not closed (5) Floppy Disc Controller chip is defective.
Speed Test 1,2	(1) Motor not spinning within specified limits
Missing Pulse	(1) Missing pulse one shot circuit is defective. (2) Index circuit is defective.

Write

No Disc	(1) Missing pulse detector is defective. (2) Door not closed (3) Belt not in place on spindle
Write Protect	(1) Disc is write protected. (2) Write Protect circuit is defective.
UnderRun	(1) During format operation the FDC did not receive data before 30 uSec. (2) Wait state machine fault (3) CLK running too slow (4) FDC internal timing problem

Read

Not Ready	(1) Disc change circuit is defective. (2) Disc removed from drive
No ID Field	(1) Disc was not formatted due to the Write circuit. (2) Defective disc (3) Defective Floppy Disc Controller chip (4) Read problem on drive or drive board (5) Phase locked loop unable to lock
Wrong ID Field	(1) Seek failure (wrong track)
CRC Error	(1) Defective Floppy Disc Controller chip (2) Phase Lock Loop of the read circuit possibly defective (3) Defective disc (4) Read problem on drive or drive board
OverRun	(1) Data lost between FDC chip and processor (2) Wait state machine/FDC internal timing problems

APPENDIX D. Z80 I/O REGISTER DEFINITIONS

READ REGISTERS

MNEMONIC (REGISTER NAME) [ADDRESS]	BIT DEFINITIONS 7	6	5	4	3	2	1	0
NOTE: FDC registers are complemented (lowtrue).								
FDCSR (*)	NOTRDY	WRPROT	HEADLD	SKERR	CRCERR	TRACK0	INDEX	BUSY
(STATUS) (**) [00HEX]	NOTRDY	WRPROT	RCTYPE	RNF	CRCERR	LOSTDAT	DRQ	BUSY
FDCTR (TRACK REG) [01HEX]	D	D	D	D	D	D	D	D
FDCSECTR (SECTOR REG) [02HEX]	D	D	D	D	D	D	D	D
FDCDR (DATA REG) [03HEX]	D	D	D	D	D	D	D	D

(*) - FDC TYPE I commands
(**)- FDC TYPE II and III commands

	(HEAD LOADED ON SELECTED DRIVE)							
POTPRI (POTPOURRI REG) [20HEX]	DSA-LP	SFTEST	9USEC	X	MSNGPLS	1791INT	DRQ	WRPROT
	hitrue	hitrue	hitrue		lowtrue	lowtrue	lowtrue	hitrue
	(HEAD UNLOADED ON SELECTED DRIVE)							
	DSA-LP	SFTEST	DISKID2	DISKID1	DISKID0	1791INT	DRQ	WRPROT
	hitrue	hitrue				lowtrue	lowtrue	hitrue

000 = Tandon TM100
111 = No Drive connected

D = data dependent, X = state not guaranteed when read

READ REGISTERS

MNEMONIC (REGISTER NAME) [ADDRESS]	BIT DEFINITIONS 7	6	5	4	3	2	1	0
NOTE: COMMAND and DATA IN registers are complemented.								
RDCSR (COMMAND REG) [40HEX]	D	D	D	D	D	D	D	D
RDDIR (DATA IN REG) [60HEX]	D	D	D	D	D	D	D	D
RDHDSHK (HANDSHAKE REG) [80HEX]	X	X	X	X	X	CMDRF lowtrue	DORF lowtrue	DIRMT hitrue

D = data dependent, X = state not guaranteed when read

WRITE REGISTERS

MNEMONIC (REGISTER NAME) [ADDRESS]	BIT DEFINITIONS 7	6	5	4	3	2	1	0
NOTE: FDC registers are complemented.								
FDCCR (COMMAND REG) [00HEX]	D	D	D	D	D	D	D	D
FDCTR (TRACK REG) [01HEX]	D	D	D	D	D	D	D	D
FDCSECTR (SECTOR REG) [02HEX]	D	D	D	D	D	D	D	D
FDCDR (DATA REG) [03HEX]	D	D	D	D	D	D	D	D

D = data dependent, X = don't care for write operation.

WRITE REGISTERS

MNEMONIC (REGISTER NAME) [ADDRESS]	BIT DEFINITIONS 7	6	5	4	3	2	1	0
WREDC (ERROR DISP REG) [40HEX]	X	X	MRESET lowtrue	LED(MSB) low=ON	LED low=ON	LED low=ON	LED low=ON	LED(LSB) low=ON
DFCN0 (DRIVE 0 FUNCTION) [63HEX]	X	X	SIDESEL hitrue	HEADLD hitrue	MOTORON hitrue	DRVSEL hitrue	X	X
DFCN1 (DRIVE 1 FUNCTION) [62HEX]	X	X	SIDESEL hitrue	HEADLD hitrue	MOTORON hitrue	DRVSEL hitrue	X	X
DFCN2 (DRIVE 2 FUNCTION) [61HEX]	X	X	SIDESEL hitrue	HEADLD hitrue	MOTORON hitrue	DRVSEL hitrue	X	X
DFCN3 (DRIVE 3 FUNCTION) [60HEX]	X	X	SIDESEL hitrue	HEADLD hitrue	MOTORON hitrue	DRVSEL hitrue	X	X
NOTE: STATUS register and DATA OUT register are complemented.								
WRDOR (DATA OUT REG) [80HEX]	D	D	D	D	D	D	D	D
WRSTR (STATUS REG) [A0HEX]	X	X	X	NOT USED	NOT USED	BUSY hitrue	DSJ (0,1,2)	DSJ
WRINIT (CLR HANDSHAKE REG) [C0HEX]	X	X	X	X	X	X	X	X
SYSINT (SET SYSTEM INT, ATN2) [E0HEX]	X	X	X	X	X	X	X	X

D = data dependent, X = don't care for write operation

APPENDIX E. DISC COMMANDS

E.1 DESCRIPTION OF THE DISC COMMANDS

1. Request Status

   The controller returns four bytes of status information. Two of these (Status 1 and Unit #) indicate how the last attempted operation completed, and which unit was involved. The other two bytes (Status 2) indicate the current condition of a specified unit.

2. Request Disc Address

   The controller returns four bytes indicating the current "logical" address. This includes two bytes of target track, one byte of target head, and one byte of the target sector.

3. Request Physical Address

   The controller returns three bytes indicating the physical track address on which the actuator is positioned. This includes two bytes of physical track and one byte of physical head. This is useful for calculating the number of invisible tracks between the outermost track and the current target track. This is done by subtracting the physical track address from the target track address.

4. Clear

   A controller clear places the controller in a known state. Thus it is useful when initializing a system, on power up, or after a crash. This is not a hardware reset of the controller.

5. Send DSJ

   The controller returns a byte indicating if the last operation completed normally, abnormally, or if the power to the controller has just been restored.

6. Seek

   The seek command updates a unit's target address and moves the actuator to the new target track. A seek usually precedes a data transfer operation (or a series of consecutive data transfers).

7. END

   The end command is used to put the controller and drives in a "standby state". If there is a status change in any of the drives, the controller will update the new information on that drive, and continue polling drives for either a new command or status change.

8. Read Buffered

This is the preferred method for transferring data from the disc to the Terminal Processor. Data is transferred through an internal buffer in 256 byte bursts. This prevents the relatively slow mini-floppy from monopolizing the backplane for extended periods. This internal buffering allows data to be transferred at an arbitrarily slow rate.

9. Read Unbuffered

The unbuffered read allows multiples of 256 bytes of data to be transferred from the disc to the terminal using a single command. The unbuffered read is included for compatibility with other discs. Due to details of its implementation it is not the preferred method for reading the minifloppy. Unbuffered read is most useful for cold load operations since a large number of bytes can be read with a single command. In this case optimum bus utilization is not important.

10. Verify

The verify command is a read which does not transfer data to the backplane. Two bytes received by the controller indicates the number (N) of sectors to be verified, which can range from 0 to 1055. This is useful for performing a surface analysis of the disc, or checking the integrity of the data on the disc.

11. Write Buffered

This is the preferred method for transferring data from the terminal to the disc. Data is transferred through an internal buffer in 256 byte bursts. Thus, the relatively slow minifloppy will not monopolize the backplane for extended periods of time. Since 256 bytes of data are buffered within the controller, the terminal backplane need not hang waiting for the disc. This also allows data transfers to occur at an arbitrarily low rate.

12. Write Unbuffered

The unbuffered write allows multiples of 256 bytes of data to be transferred from the terminal to the disc using a single command. The unbuffered write is included for compatibility with other discs. Due to details of its implementation, it is not the preferred method for writing to the minifloppy. Unbuffered write is most useful for a cold dump operation since a large number of bytes can be written with a single command. In this case optimum backplane utilization is not important. The data transfer can occur at an arbitrarily slow rate.

13. Initialize

The initialize command is used to set or reset the D (defective) bits. The entire target track is reformatted with all D bits (located in target sector address head number, see APPENDIX A note 2) set or reset. After reformatting, the command accepts write data in a manner identical to the write buffered command. The initialize command is especially useful when formatting a disc.

14. Format

The format command takes a blank disc or a disc in another format and makes it into an HP formatted disc. Appendix A describes the HP physical track format for minifloppies. During this operation any bad/defective tracks on the disc are made into invisible tracks. It should be noted that formatting a disc will destroy all previous data.

15. Initiate Selftest

This command gives the user the capability to remotely initiate a destructive or non-destructive device self test. The self test results may then be read using the Read Selftest command.

16. Read Selftest

The controller returns the results of the last selftest the controller performed (two bytes). This is useful after the initiate self-test command or after the completion of the power-on Selftest.

17. Write Loopback

The controller stores 256 bytes in its internal buffer. A diagnostic might use this command before a Read Loopback in order to test the operation of the backplane interface.

18. Read Loopback

The controller sends 256 bytes from its internal data buffer. This is useful in diagnostics when the Write Loopback command has been used to load the internal buffer.

19. Down Load

After receiving the Down Load command, 256 bytes are stored in the controller memory starting at location 4100 (HEX). Following the reception of the last byte the controller transfers execution to location 4100 (HEX).

20. Physical Seek

This command moves the head to the Physical Target address. The drive remains selected with the disc spinning, until a new command is issued. This command also checks the period of the disc rotation. The 5 error display LEDs are used as a visual indication of the period measured by the controller firmware. When the disc rotation period is 200 +/- 1 mSec (0.5%), the center LED will be ON. When the period (T) is not within 0.5% the other LEDs indicate the period in mSec as follows:

```
        LSB (LEFT OF PCA)                          MSB (RIGHT OF PCA)
         *        *        *        *                 *
       T<197  197<T<199 199<T<201 201<T<203   203<T
(disc spinning                                (disc spinning
 too fast)                                     too slow)
```

See APPENDIX C Section C.2 for the LED layout.

This capability can be used for adjusting the spindle motor speed using the potentiometer located on the Servo Control PCA (on the back of the DRIVE MECHANISM).

21. Read Data

This command is equivalent to Read Buffered, where the data is transferred through an internal buffer in 256 byte bursts. Unlike the Read Buffered command, data is transferred to the backplane interface independent of CRC and Data lost errors.

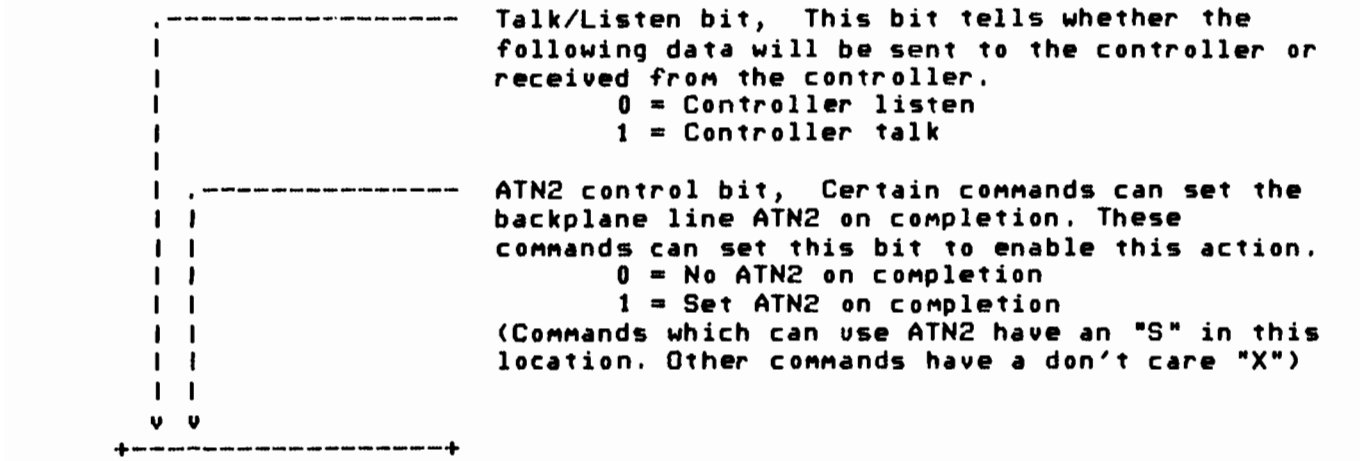
22. Disc Stagger/Interleave

This command determines the disc stagger/interleave. It does this by finding sector zero, and then counting sectors until sector one is found. The disc stagger is stored in the controller data buffer, and can be read using the RLOOP command.

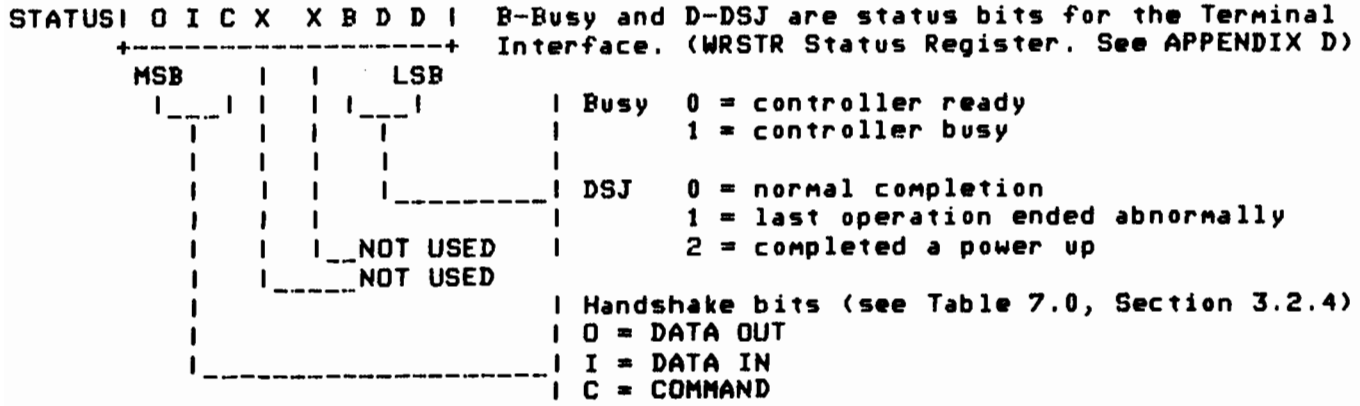
E.2 DETAILS OF THE DISC COMMANDS

See Section 3.2 TERMINAL INTERFACE for a description of the four registers used to communicate between the Controller and the Terminal. These registers are: COMMAND (COM.), STATUS (STATUS), DATA IN (D. IN), and DATA OUT (D. OUT).

Certain command bits are predefined for control purposes.



Certain status bits are predefined. Bits 5,6 and 7 are the handshake bits which tell which registers are full or empty. These bits change automatically when the register is read from or written to. Bits 0-4 are written by the Controller Z80-A when it writes to the STATUS register (WRSTR). Bits 3 and 4 are not used.



1. Request STATUS

Terminal sends four bytes:

COM.	0 X 0 0 1 0 X 0	(08hex or 0Ahex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 0 1 1	(03hex) Request STATUS Opcode
D. IN	Unit # (0-3)	(00hex to 03hex)
STATUS	0 I C X X B D D	Busy bit reset here when ready for command
COM.	1 X 0 0 1 0 0 0	(88hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

Controller sends four bytes:

D. OUT	0 0 D ((- S1 -)) (STATUS 1)	D bit set means last operation had the defective bit set. S1 field is 5 bits of status information about how the last disc operation completed (See Table E 1.0 at the end of this Section for definitions)
D. OUT	Unit # (0-3)	Unit number of last operation
D. OUT	* X X T T T T X	Two bytes (STATUS 2) indicating the current status of the selected unit (See Table E 1.0 at the end of this Section for definitions)
D. OUT	A W X E F C S S	
STATUS	0 I C X X B D D	Busy bit reset here on completion

2. Request Disc Address

Terminal sends four bytes:

COM.	0 X 0 0 1 0 X 0	(08hex or 0Ahex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 1 0 1 0 0	(14hex) Request Disc Addr Op Code
D. IN	X X X X X X X X	Don't Care
STATUS	0 I C X X B D D	Busy bit reset here when ready for command
COM.	1 X 0 0 1 0 0 0	(88hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

Controller sends four bytes:

D. OUT	Cylinder, MSByte 1	Two bytes of logical cylinder 0(=cylinder(=32, for the target track
D. OUT	Cylinder, LSByte 2	
D. OUT	Head (0 or 1)	One byte of head selected
D. OUT	Sector (0-16)	One byte of sector selected
STATUS	0 I C X X B D D	Busy bit reset here on completion

3. Request Physical Address

Terminal sends four bytes:

COM.	0 X 0 0 1 1 0 0	(0Chex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 1 0 1 0 0	(14hex) Request Phys Addr Op Code
D. IN	X X X X X X X X	Don't Care
STATUS	0 I C X X B D D	Busy bit reset here when ready for command
COM.	1 X 0 0 1 0 0 0	(88hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

Controller sends four bytes:

D. OUT	Cylinder, MSByte 1	Two bytes of physical cylinder 0(=cylinder(=34, for physical track
D. OUT	Cylinder, LSByte 2	
D. OUT	Head (0 or 1)	One byte of head selected
D. OUT	0 0 0 0 0 0 0 0	One byte of zero
STATUS	0 I C X X B D D	Busy bit reset here on completion

```
   +--------------------------------+
4. |      Clear                     |
   +--------------------------------+
```

Terminal sends one byte:

```
      +------------------+
COM.  | 0 S 0 1  0 0 0 0 |  (50hex = Set ATN2 on completion)
      +------------------+  (10hex = No ATN2 on completion)
      +------------------+
ATN2  | 0 I C X  X B D D |  ATN2 line set after completion if S = 1
STATUS+------------------+  Busy bit reset here on completion
```

Controller sends no bytes back.

```
   +--------------------------------+
5. |      Send DSJ                  |
   +--------------------------------+
```

Terminal sends one byte:

```
      +------------------+
COM.  | 1 X 0 1  0 0 0 0 |  (90hex)
      +------------------+
      +------------------+
STATUS| 0 I C X  X B D D |  Busy bit set here on receipt of command
      +------------------+
```

Controller sends one byte:

```
      +------------------+
D. OUT| DSJ              |  DSJ byte: 0= last operation OK
      +------------------+  1 = last operation failed
                            2 = power up or self test just
                            occurred
      +------------------+
STATUS| 0 I C X  X B D D |  Busy bit reset here on completion
      +------------------+
```

6. Seek

Terminal sends seven bytes:

COM.	0 S 0 0 1 0 0 0	(48hex = Set ATN2 on completion) (08hex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 0 1 0	(02hex) Seek Opcode
D. IN	Unit # (0-3)	Perform seek on this unit
D. IN	Cylinder, MSByte 1	Two bytes of target cylinder
D. IN	Cylinder, LSByte 2	
D. IN	Head # (0-1)	One byte of target head
D. IN	Sector # (0-16)	One byte of target sector
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

Controller sends no bytes back.

```
      +-----------------------------------+
   7. |      End                          |
      +-----------------------------------+
```

Terminal sends three bytes:

```
      +-------------------+
COM.  | 0 S 0 0  1 0 0 0  |  (48hex = Set ATN2 on completion)
      +-------------------+  (08hex = No ATN2 on completion)
      +-------------------+
STATUS| 0 I C X  X B D D  |  Busy bit set here on receipt of command
      +-------------------+
      +-------------------+
D. IN | 0 0 0 1  0 1 0 1  |  (15hex) End opcode
      +-------------------+
      +-------------------+
D. IN | X X X X  X X X X  |  Don't Care
      +-------------------+
      +-------------------+
ATN2  | 0 I C X  X B D D  |  ATN2 line set after completion if S = 1
STATUS+-------------------+  Busy bit reset here on completion
```

Controller sends no bytes back.

B. Buffered Read

Terminal sends four bytes:

COM.	0 S 0 0 1 0 1 0	(4Ahex = Set ATN2 on completion) (0Ahex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 1 0 1	(05hex) Buffered Read opcode
D. IN	Unit # (0-3)	Selected unit number
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here when ready for command
COM.	1 X 0 0 0 0 0 0	(80hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

Controller sends 256 bytes:

D. OUT	256 bytes data	
STATUS	0 I C X X B D D	Busy bit reset here on completion

9. Unbuffered Read

Terminal sends four bytes:

COM.	0 X 0 0 1 0 0 0	(08hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 1 0 1	(05hex) Unbuffered Read opcode
D. IN	Unit # (0-3)	Selected unit number
STATUS	0 I C X X B D D	Busy bit reset here when ready for command
COM.	1 X 0 0 0 0 0 0	(80hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

Controller sends back:

D. OUT	256xN bytes data	

The controller stops sending data when the terminal enters a new command in the COMMAND register on the Controller.

STATUS	0 I C X X B D D	Busy bit reset here on completion (When a new command is written to the Controller)

10. Verify

Terminal sends five bytes:

COM.	0 S 0 0 1 0 0 0	(48hex = Set ATN2 on completion) (08hex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 1 1 1	(07hex) Verify opcode
D. IN	Unit # (0-3)	
D. IN	Sector count, 1	Two byte sector count MSByte
D. IN	Sector count, 2	LSByte
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

Controller sends no bytes back.

11. Write Buffered

Terminal sends 260 bytes:

COM.	0 S 0 0 1 0 0 1	(49hex = Set ATN2 on completion) (09hex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 1 0 0 0	(08hex) Write Buffered opcode
D. IN	Unit # (0-3)	
STATUS	0 I C X X B D D	Busy bit reset here when ready for command
COM.	0 S 0 0 0 0 0 0	(40hex = Set ATN2 on completion) (00hex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	256 bytes data	
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

Controller sends nothing back.

12. Write Unbuffered

Terminal sends 4 + (256xN) bytes:

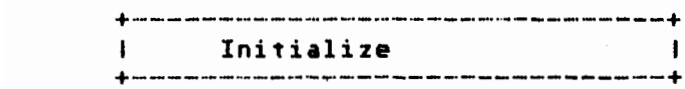
COM.	0 X 0 0 1 0 0 0	(08hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 1 0 0 0	(08hex) Unbuffered Write Op Code
D. IN	Unit # (0-3)	Selected unit number
STATUS	0 I C X X B D D	Busy bit reset here when ready for command
COM.	0 X 0 0 0 0 0 0	(80hex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

D. IN	256xN bytes data

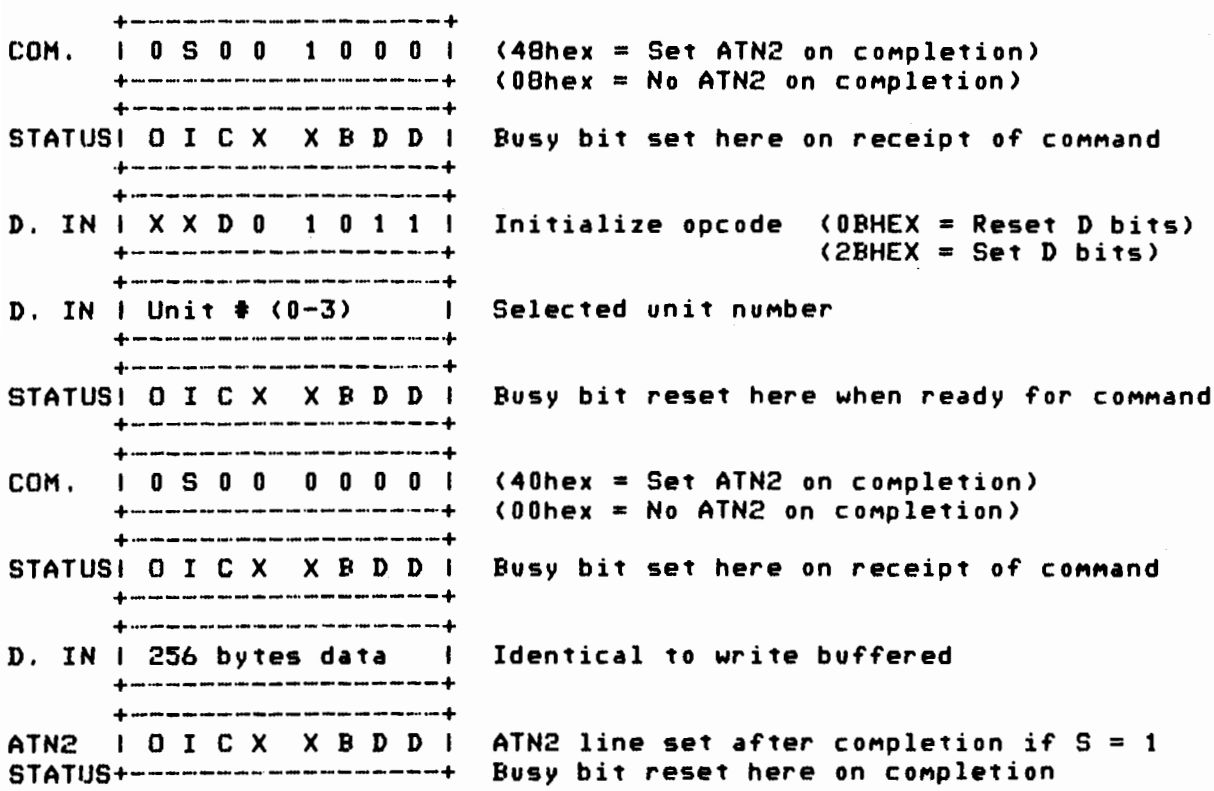
The controller stops receiving data when the terminal enters a new command in the COMMAND register on the Controller.

STATUS	0 I C X X B D D	Busy bit reset here on completion (When a new command is written to the Controller)

Controller sends nothing back.



Terminal sends 260 bytes:



Controller sends nothing back.

14. Format

Terminal sends six bytes:

COM.	0 S 0 0 1 1 0 0	(4Chex = Set ATN2 on completion) (0Chex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 1 1 0 0 0	(18hex) Format opcode
D. IN	Unit # (0-3)	
D. IN	F T T T T T T T	F-set will format the entire disc without invisible tracks T-Type must be 2 for HP format
D. IN	Stagger parameter	Number of physical sectors between consecutive sector numbers on the disc. Stagger parameter can range from 0 to 15.
D. IN	Data Format char.	Binary value to be written in each byte of the sector.
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

Controller sends nothing back.

15. Initiate Self Test

Terminal sends three bytes:

COM.	0 S 0 1 1 1 1 1	(5Fhex = Set ATN2 on completion) (1Fhex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	Cylinder	Cylinder to be written and read
D. IN	X X X X W X X X	W- Tells whether or not a read/write test will be performed
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

Controller sends nothing back.

16. Read Self Test

Terminal sends one byte:

COM.	1 X 0 1 1 1 1 1	(9Fhex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

Controller sends two bytes:

D. OUT	Test results 1	Two bytes of self test results MSByte
D. OUT	Test results 2	LSByte (See Appendix C)
STATUS	0 I C X X B D D	Busy bit reset here on completion

17. Write Loopback Sector

Terminal sends 257 bytes:

COM.	0 X 0 1 1 1 1 0	(1Ehex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	256 bytes data	
STATUS	0 I C X X B D D	Busy bit reset here on completion

Controller sends nothing back.

18. Read Loopback Sector

Terminal sends one byte:

COM.	1 X 0 1 1 1 1 0	(9Ehex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command

Controller sends 256 bytes:

D. OUT	256 bytes data	
STATUS	0 I C X X B D D	Busy bit reset here on completion

19. Down Load

Terminal sends 257 bytes:

COM.	0 X 0 0 1 1 1 1	(0Fhex)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	256 bytes data	
STATUS	0 I C X X B D D	Busy bit reset here on completion

Controller sends nothing back.

20. Physical Seek

Terminal sends six bytes:

COM.	0 S 0 1 1 0 0 0	(58hex = Set ATN2 on completion) (18hex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 0 0 1	(01hex) Physical Seek opcode
D. IN	Unit# (0-3)	Target Unit/Drive for Physical Seek
D. IN	Cylinder MSByte	Two Bytes of target cylinder for Physical Seek
D. IN	Cylinder LSByte	
D. IN	Head	Target head for Physical Seek
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

Controller sends nothing back.

21. Read Data

Terminal sends 3 bytes:

COM.	0 S 0 1 1 0 0 0	(58hex = Set ATN2 on completion) (18hex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 0 1 0	(02hex) Read Data opcode
D. IN	Unit# (0-3)	Target Unit/Drive

Controller sends 256 bytes:

D. OUT	256 bytes data	The Controller sends the bytes regardless of the CRC checking result.
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

22. Data Stagger/Interleave

Terminal sends three bytes:

COM.	0 S 0 1 1 0 0 0	(58hex = Set ATN2 on completion) (18hex = No ATN2 on completion)
STATUS	0 I C X X B D D	Busy bit set here on receipt of command
D. IN	0 0 0 0 0 0 1 1	(03hex) Data Stagger opcode
D. IN	Unit# (0-3)	Target Unit/Drive. After stagger is determined, the value is stored into controller memory (4000hex). It is the first byte received by the controller during a "Read Loopback Sector" command.
ATN2 STATUS	0 I C X X B D D	ATN2 line set after completion if S = 1 Busy bit reset here on completion

Controller sends nothing back.

Table E 1.0 Status Byte Definitions

Status 1 (first byte returned by the CONTROLLER)

(S1)	Definition
00000	Normal Completion, The operation completed without error, or the controller has just been cleared or powered up.
00001	Illegal Opcode, The last command contained an opcode which is not recognized by the Minifloppy Disc System.
00010	The internal timer of the Floppy Disc Controller Chip did not timeout and interrupt the processor within 800 millisec. or four revolutions of the disc.
01000	Data Error, The disc Read or Verify operation was terminated because a data error was detected (CRC error).
01001	Track/Sector Compare Error, The target track or sector cannot be found (READ routine). Up to six passes of the track are made before this status is set.
01010	I/O Program Error, An illegal controller command or sequence has been received by the controller.
10001	Defective Track, During an HP Write, Read, or Verify a set D bit was encountered.
10010	Retryable Hardware Error, An internal hardware timing error occurred during a data transfer or seek.
10011	Status 2 Error, Some condition in status 2 prevented the drive related operation from completing normally. These conditions include: 1. Specified unit is between 0 and 3, but that drive is not connected to the controller. 2. There is no disc in drive. 3. A Hardware problem is detected in the drive. 4. The disc is unformatted or has an unknown format. 5. The disc is write protected (error only during a Disc Write operation). 6. The First Status Bit of the selected drive is set. (See bit "F" in STATUS 2, below)

Table E 1.0 Status Byte Definitions (cont'd)

(S1)	Definition
10111	Unit Unavailable, A command included a request for a unit number greater than 3.
11111	Drive Attention, The indicated drive is requesting attention for one of the following reasons.(see bit "A" in STATUS 2) 1. A Seek completed normally. 2. A Seek command failed due to: a. Drive Fault (See bit "E" in STATUS 2, below) , b. out of bounds target cylinder or sector, or c. the controller cannot find the target address (SEEK routine). 3. Following an End command, a change in the drive status was detected. a. Disc inserted, b. Disc removed, c. Drive connected, d. Drive disconnected

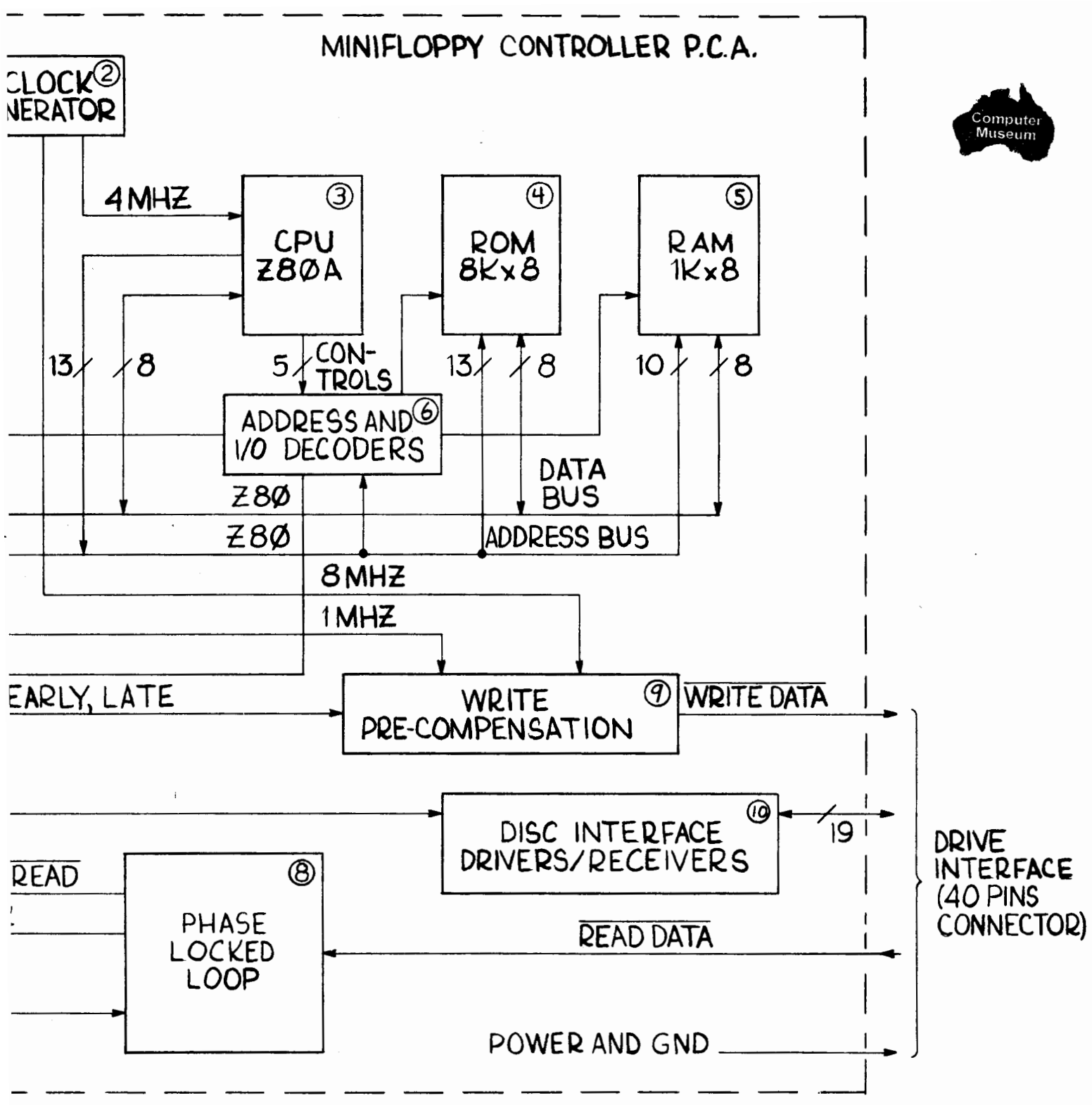
Table E 1.0 Status Byte Definitions (cont'd)

Status 2 (third and fourth bytes returned by the CONTROLLER)

Status 2	Definition
*	Status 2 Error, This bit is set if one or more of the following bits are set in status 2: a. Drive Fault (See bit "E", below) b. Seek Check (See bit "C", below) c. Any Drive Not Ready Error (see bits "SS" below)
TTTT	Disc Type, These bits indicate the type and format of the disc currently present in the selected drive as follows: 0000 - Empty drive 0001 - Blank or unknown format single sided 0010 - HP format single sided 0101 - Blank or unknown format double sided 0110 - HP format double sided
A	Attention, This bit is set when a seek completes (successfully or unsuccessfully). Following an End command, it is set if the door is opened, or the disc changed. It is cleared after the status is read.

Table E 1.0 Status Byte Definitions (cont'd)

Status 2	Definition
W	Write Protected, The disc in the selected drive has the write protect notch covered.
E	Drive Fault, This bit is set after any of the following occurs: a. Drive goes not ready after an End command, b. Drive goes not ready during data transfer, or c. Hardware failure. Drive Fault is cleared after status is read.
F	First Status Bit, This bit is set when a disc is present in the selected drive after: a. Power on, b. The door is closed, c. Self Test completion. The First Status Bit is cleared after status is read.
C	Seek Check, This bit is set when a Seek fails for one or more of the following reasons: a. an out of bounds target sector was specified, b. an attempt was made to access a non-existent physical track, c. The seek algorithm could not find the target logical track. The Seek Check Bit is cleared after status is read.
SS	Drive Ready, These two bits indicate the status of the selected drive as follows: 00 - Drive ready 10 - No drive connected to controller 11 - No disc in drive



MINIFLOPPY CONTROLLER PCA BLOCK DIAGRAM

Figure 1
Minifloppy Controller PCA Block Diagram
DEC-29-80 13255-91223

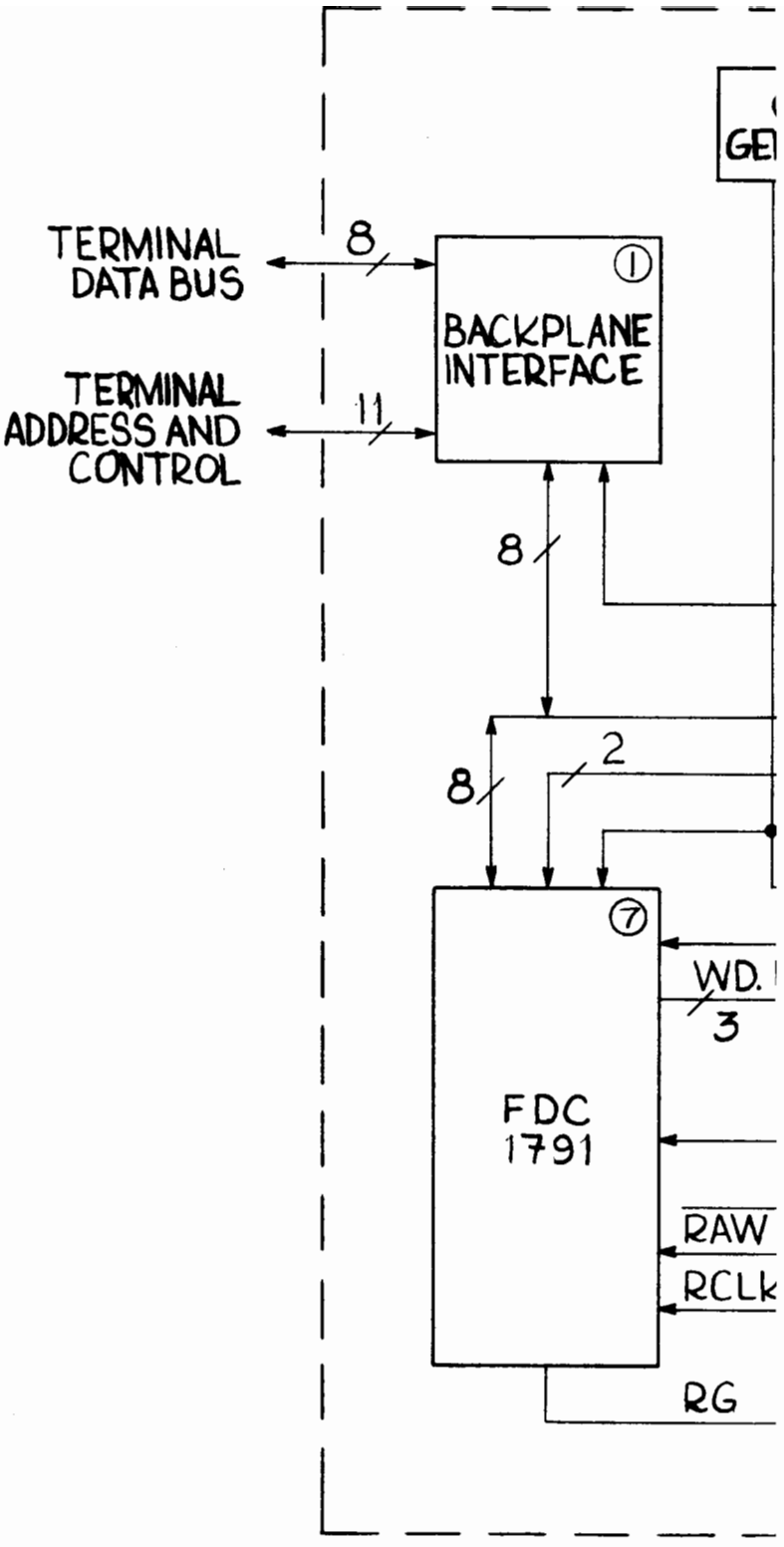

GE
TERMINAL DATA BUS
8
①
BACKPLANE INTERFACE
TERMINAL ADDRESS AND CONTROL
11
8
8
2
⑦
WD.
3
FDC 1791
RAW
RCLk
RG

FIG.1

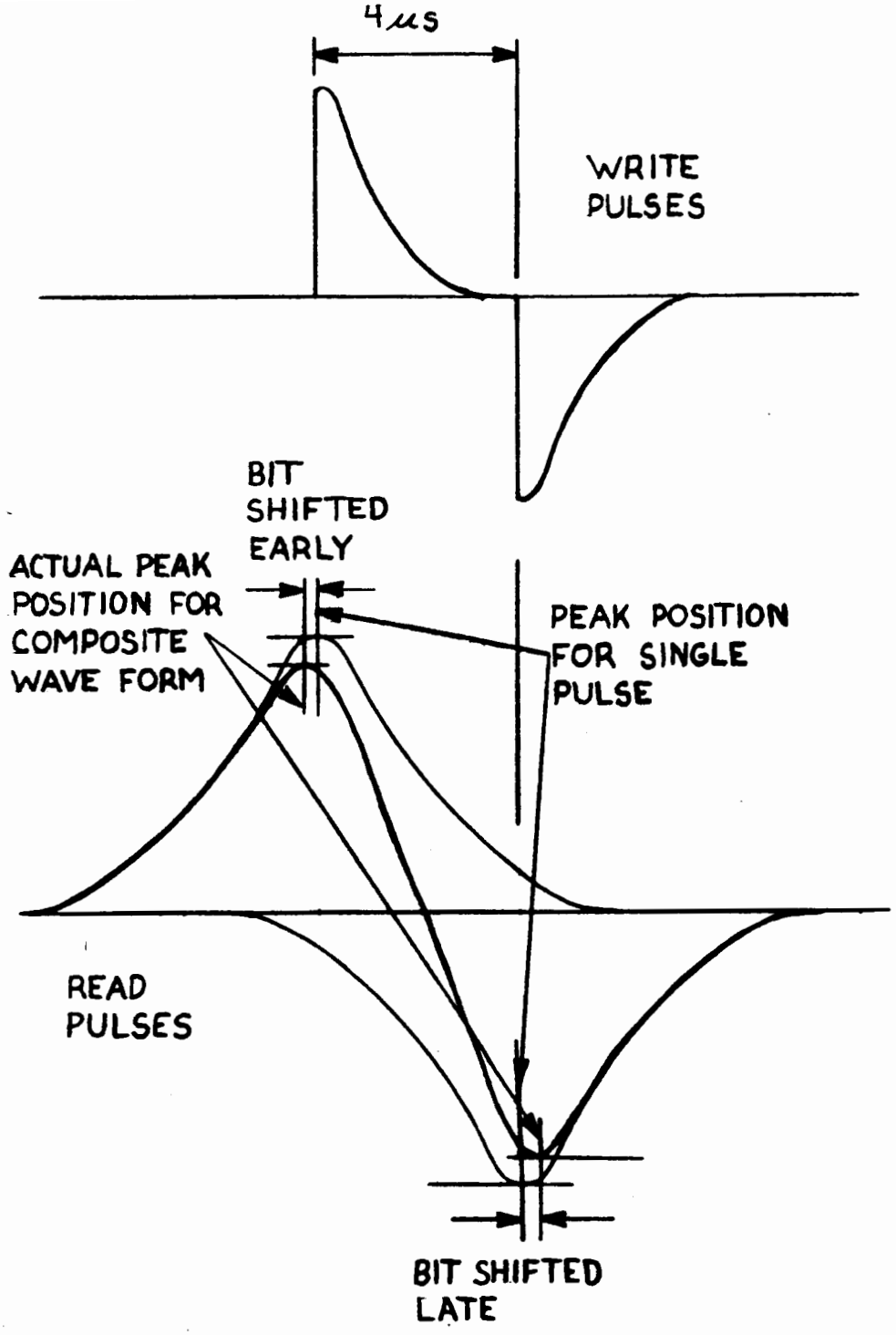


FIG. 2. BIT SHIFT DURING READ OPERATION

Figure 2
Bit shift during read operation
DEC-29-80 13255-91223

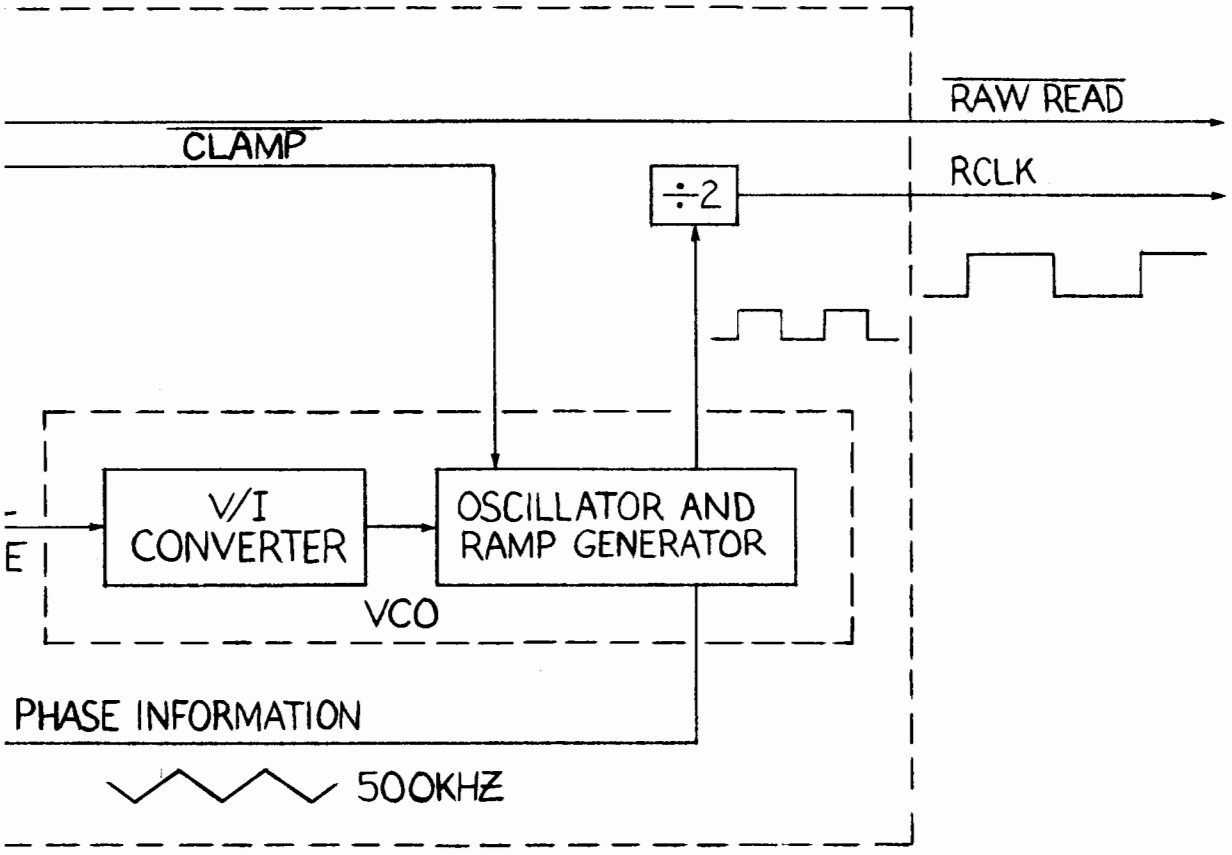


Figure 3
Phase locked loop Block Diagram
DEC-29-80 13255-91223

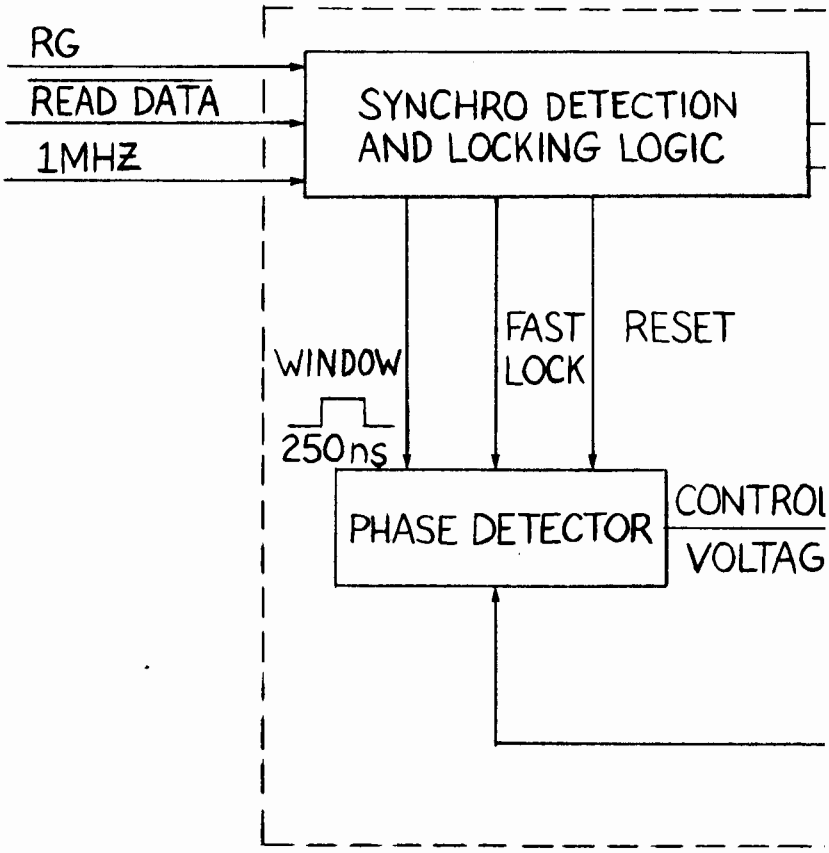


FIG. 3 PHASE LOCKED LOOP BLOCK DIAGRAM

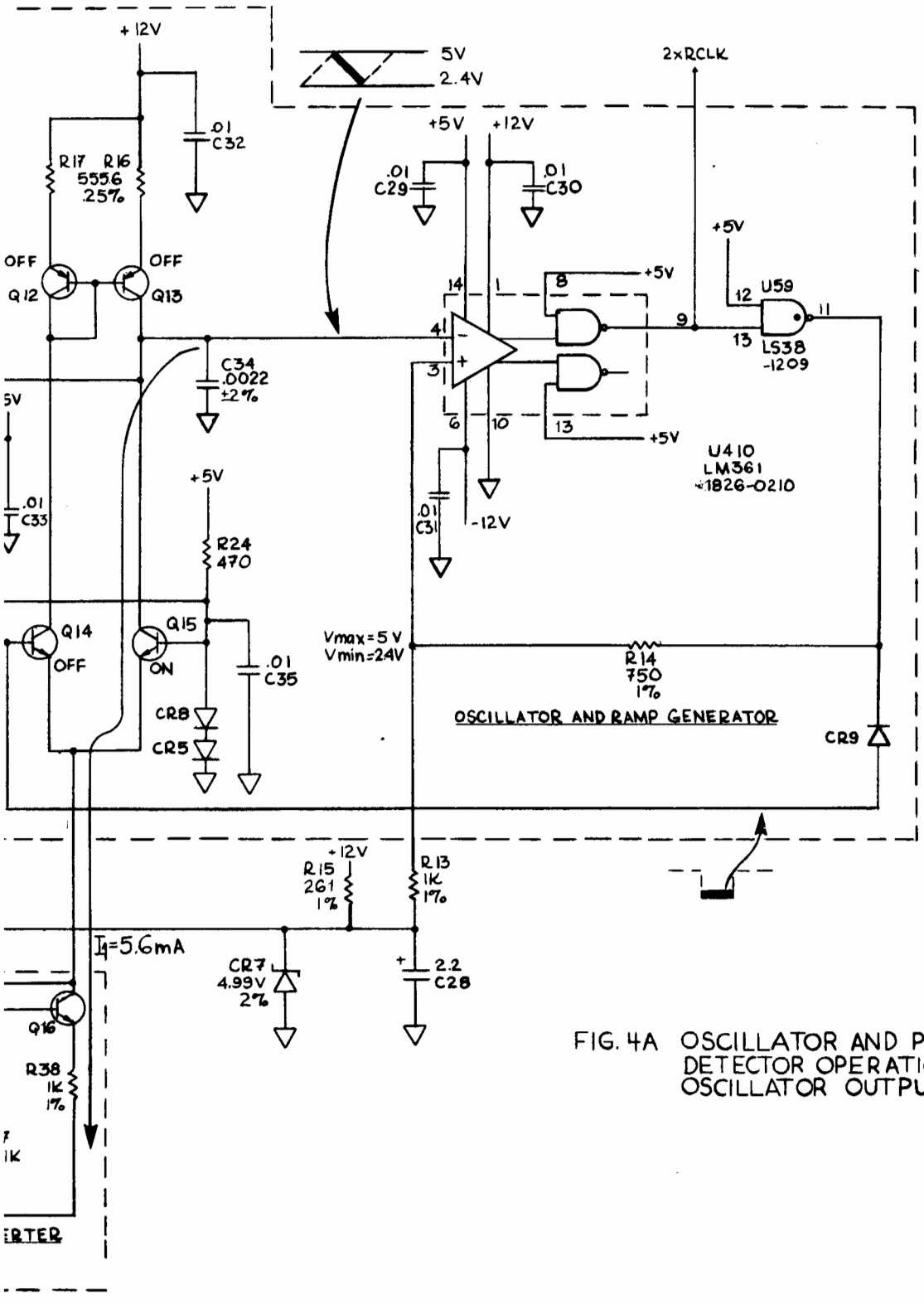
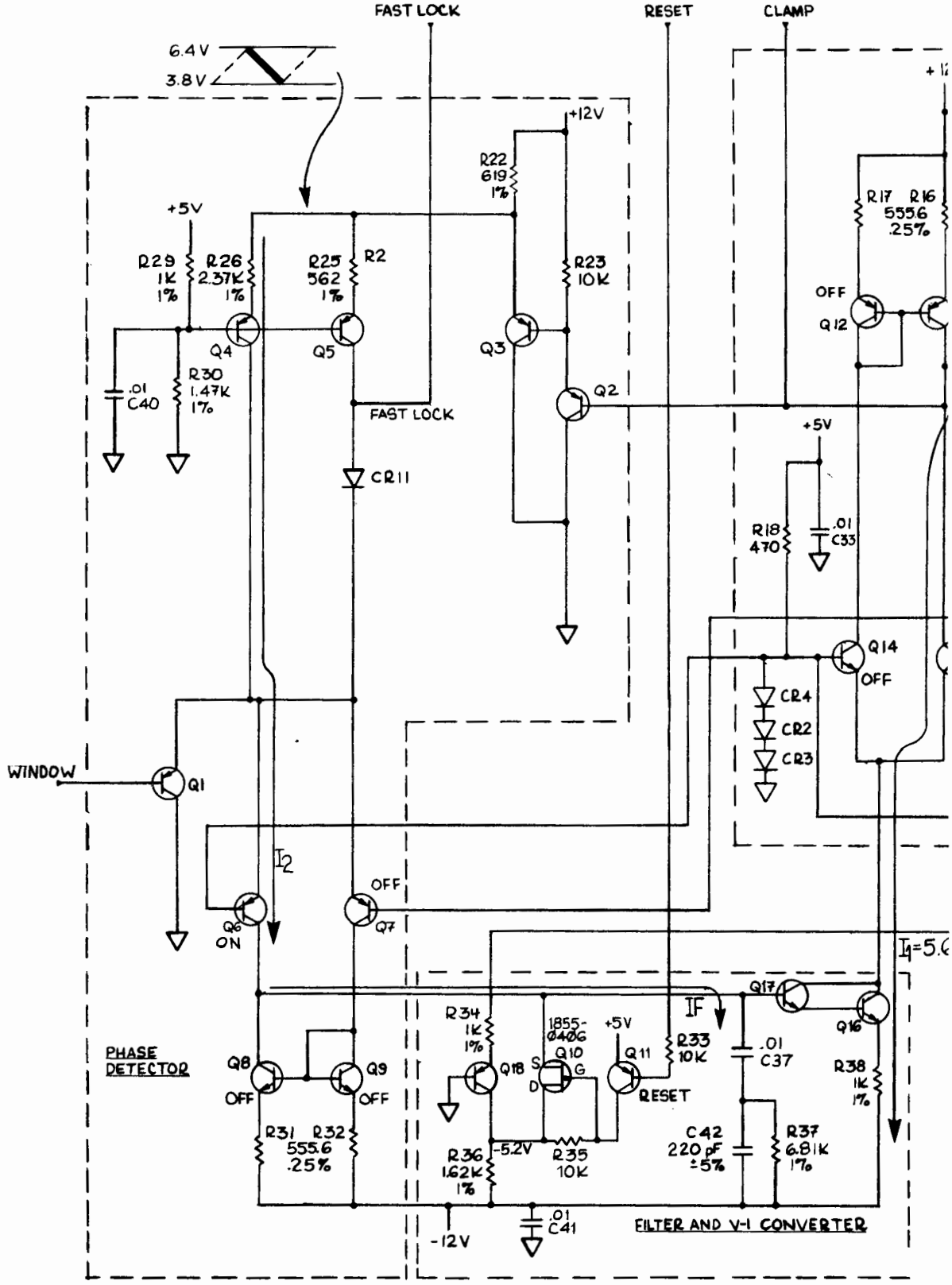


FIG. 4A OSCILLATOR AND PHASE DETECTOR OPERATION OSCILLATOR OUTPUT LOW

Figure 4
Oscillator and Phase Detector operation
DEC-29-80 13255-91223


FAST LOCK
RESET
CLAMP
6.4V
3.8V
+12V
R22
619
1%
+5V
R29
1K
1%
R26
2.37K
1%
R25
562
1%
R2
R23
10K
R17 R16
5556
.25%
OFF
Q12
Q4
Q5
Q3
Q2
.01
C40
R30
1.47K
1%
FAST LOCK
CR11
+5V
R18
470
.01
C33
Q14
OFF
CR4
CR2
CR3
WINDOW
Q1
I2
Q6
ON
OFF
Q7
I4=5.6
Q17
Q16
IF
R34
1K
1%
1855-
Ø40G
Q10
+5V
Q11
R33
10K
.01
C37
R38
1K
1%
PHASE
DETECTOR
Q8
OFF
Q9
OFF
Q18
S
G
D
RESET
R31 R32
555.6
.25%
R36
1.62K
1%
-5.2V
R35
10K
C42
220 pF
±5%
R37
6.81K
1%
-12V
.01
C41
FILTER AND V-I CONVERTER

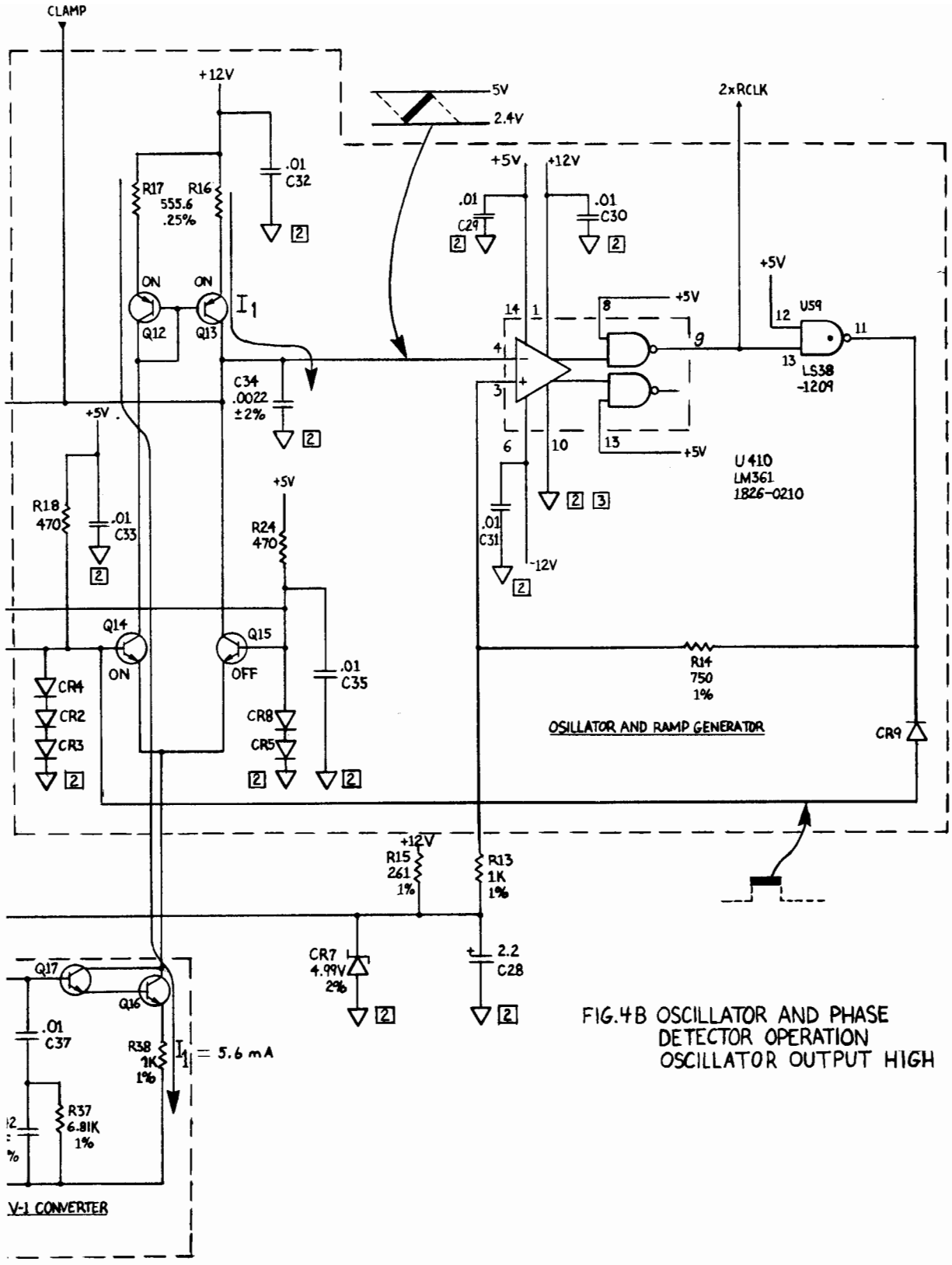


FIG.4B OSCILLATOR AND PHASE DETECTOR OPERATION OSCILLATOR OUTPUT HIGH

Figure 4
Oscillator and Phase Detector operation
DEC-29-80 13255-91223

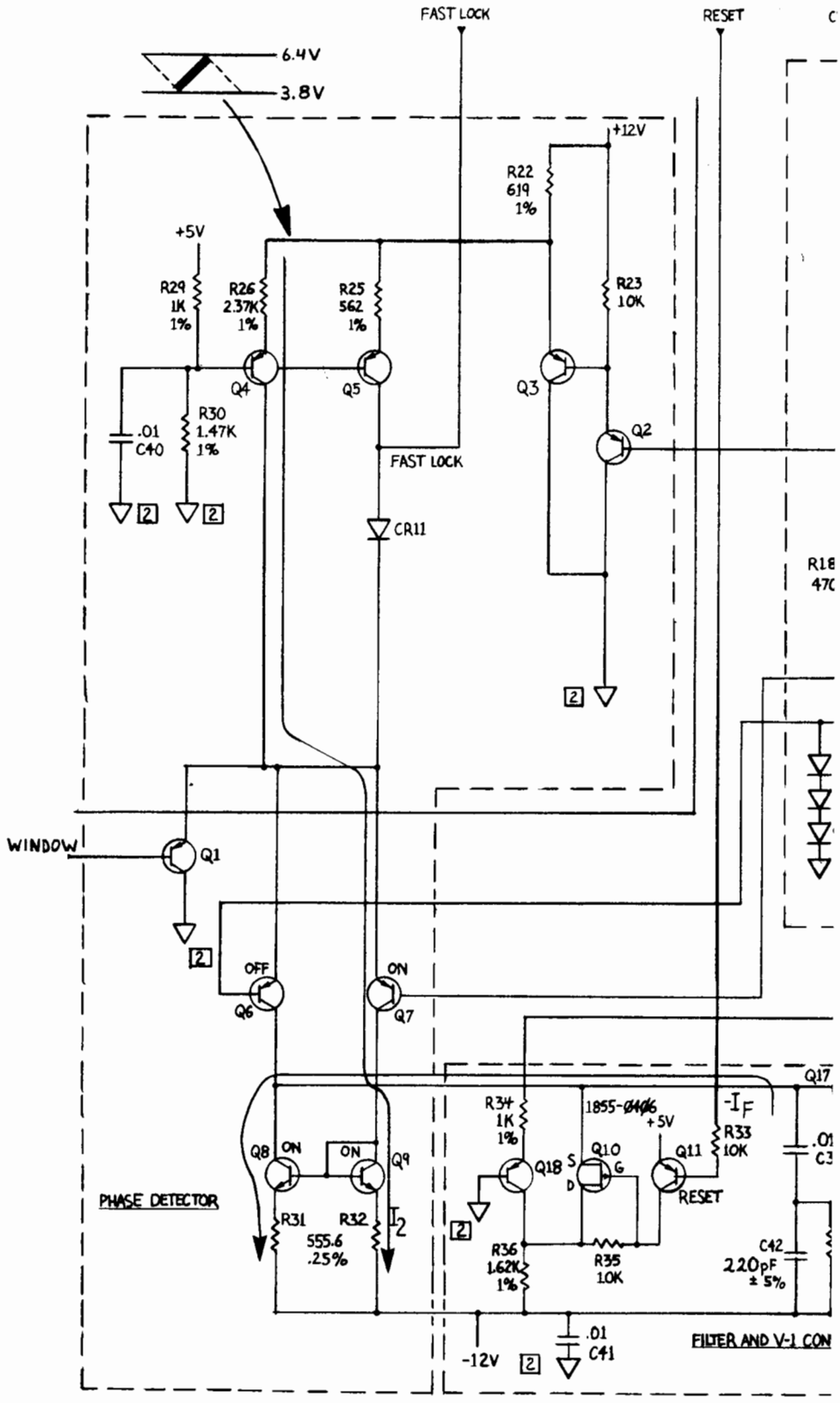

FAST LOCK
RESET
6.4V
3.8V
+12V
R22
619
1%
+5V
R29
1K
1%
R26
2.37K
1%
R25
562
1%
R23
10K
Q4
Q5
Q3
Q2
.01
C40
R30
1.47K
1%
FAST LOCK
CR11
WINDOW
Q1
OFF
Q6
ON
Q7
Q8
ON
ON
Q9
PHASE DETECTOR
R31
R32
555.6
.25%
I_2
R34
1K
1%
1855-0406
+5V
Q10
Q11
Q18
S
D
G
RESET
R33
10K
$-I_F$
R36
1.62K
1%
R35
10K
C42
220pF
±5%
.01
C41
-12V
FILTER AND V-1 CON

FIG. 5 PHASE DETECTOR OPERATION

FIG. 5A

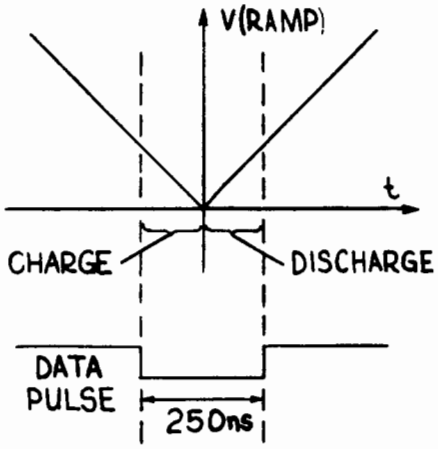
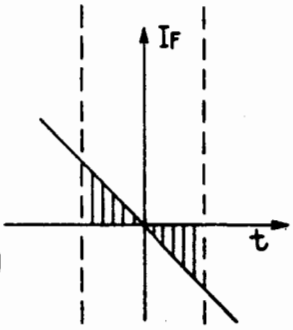


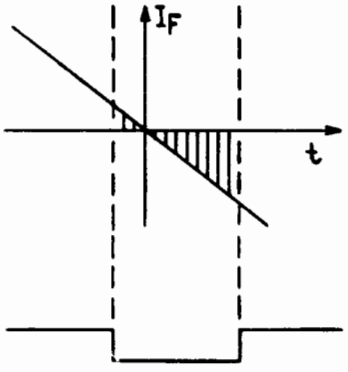
FIG. 5B.

CHARGE:
Increases
control voltage
Increases I_1
Increases
ramp slope
→ Increase
VCO frequency



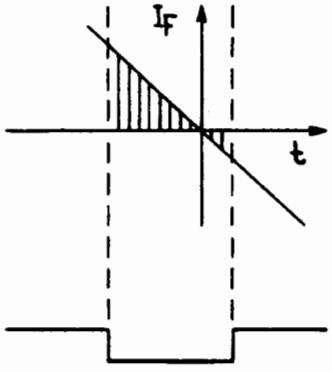
DISCHARGE:
Decreases
control voltage
Decreases I_1
Decreases
ramp slope
→ Decrease
VCO frequency

FIG. 5C



Data pulse is late:
Discharge > Charge
→ Frequency decreases

FIG 5D



Data pulse is early:
Charge > Discharge
→ Frequency increases

Figure 5
Phase detector operation
DEC-29-80 13255-91223

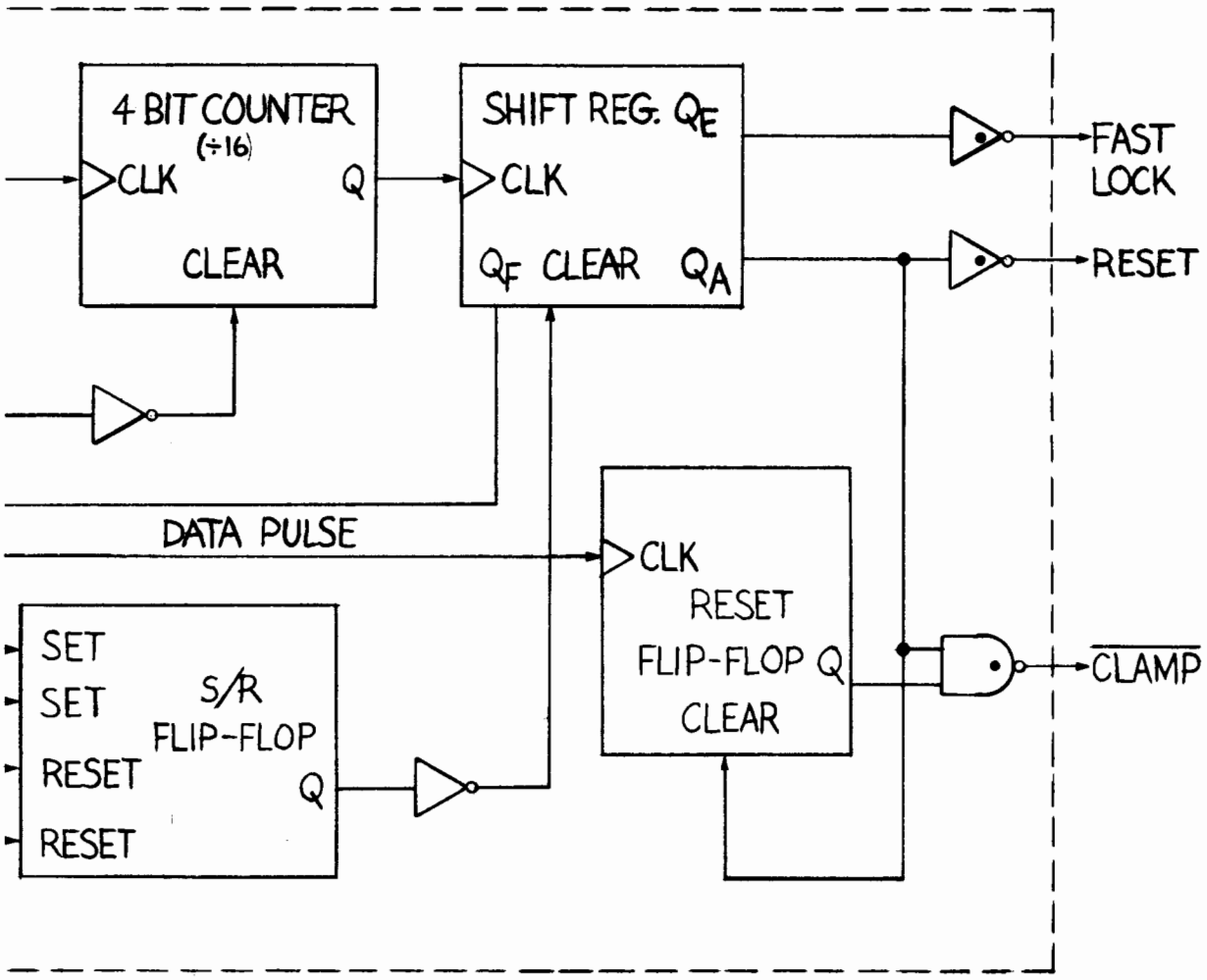


Figure 6
Synchro detection & Locking logic Block Diagram
DEC-29-80 13255-91223

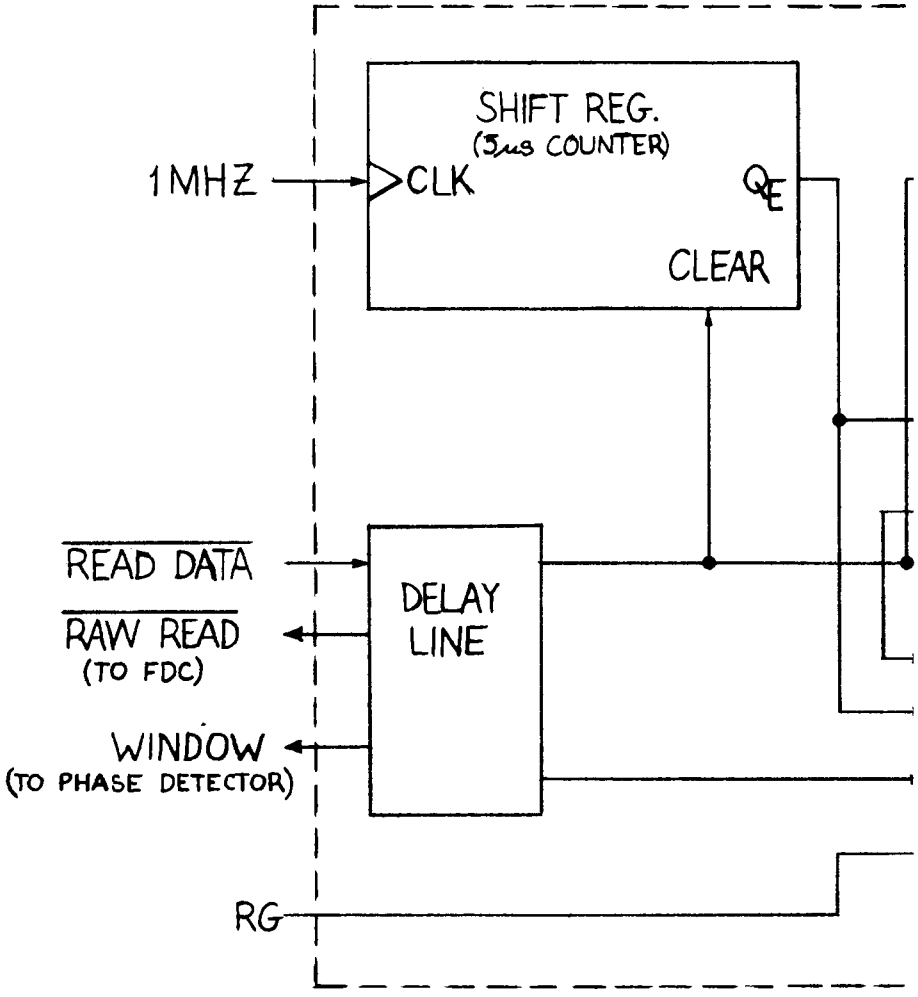
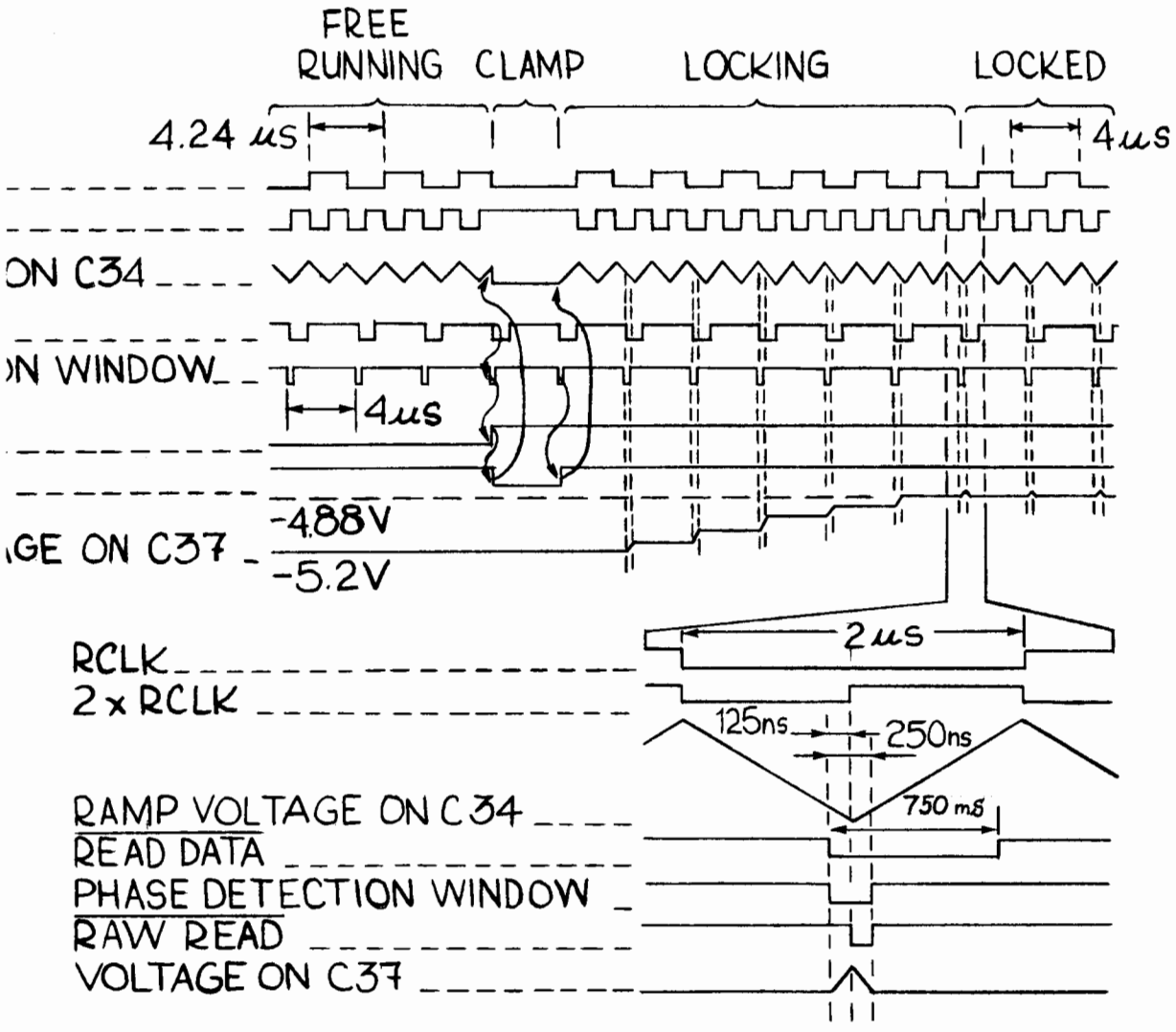


FIG. 6 SYNCHRO DETECTION AND LOCKING
LOGIC BLOCK DIAGRAM



IMING DIAGRAM

Figure 7
Clamp & Locking Timing Diagram
DEC-29-80 13255-91223

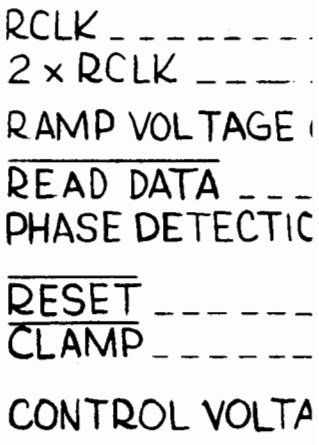


FIG. 7 CLAMP AND LOCKING T

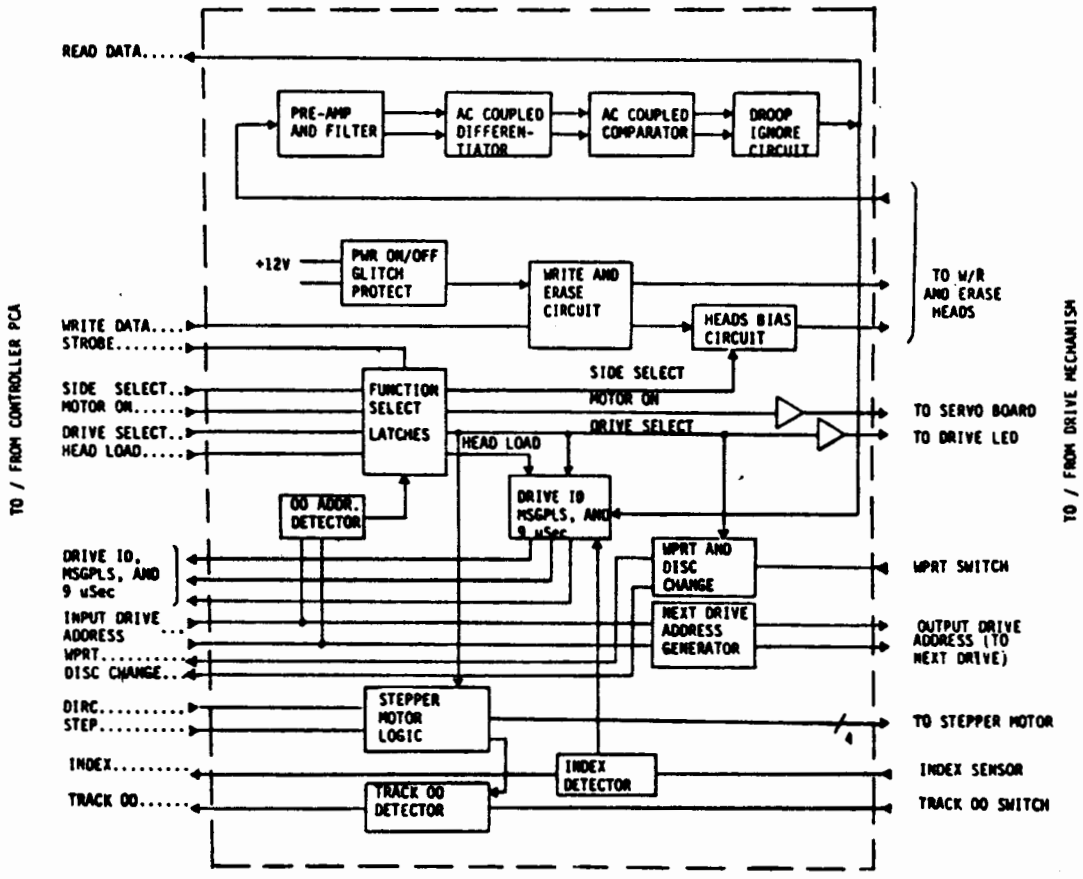


FIG. 8 DRIVE ELECTRONICS PCA BLOCK DIAGRAM

Figure 8
Drive Electronics PCA Block Diagram
DEC-29-80 13255-91223

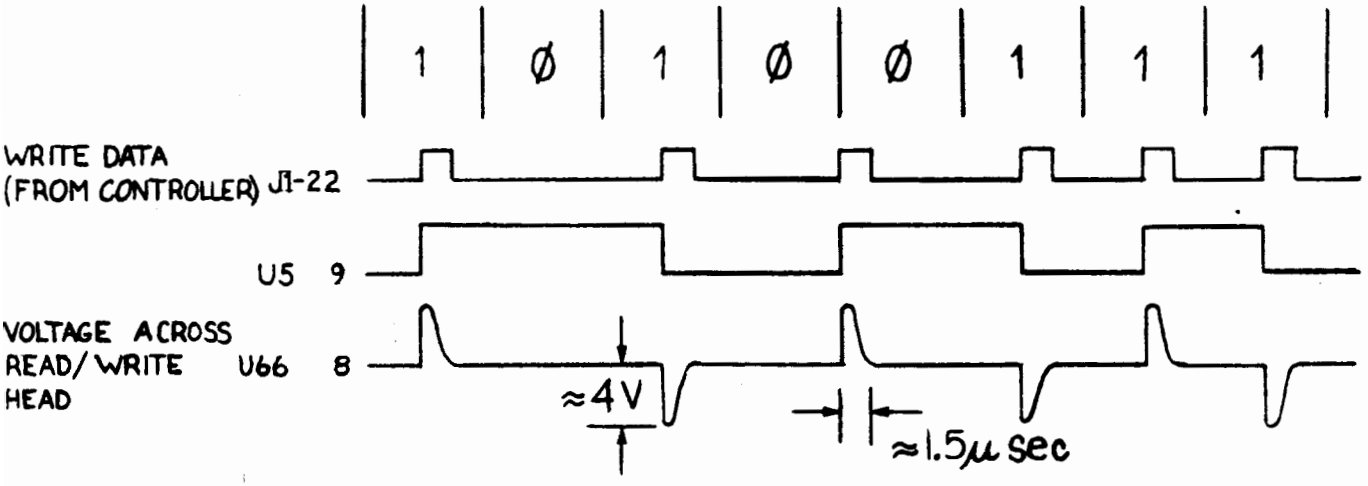


FIG. 9 WRITE CIRCUIT TIMING DIAGRAMS

Figure 9
Write Circuit Timing Diagram
DEC-29-80 13255-91223

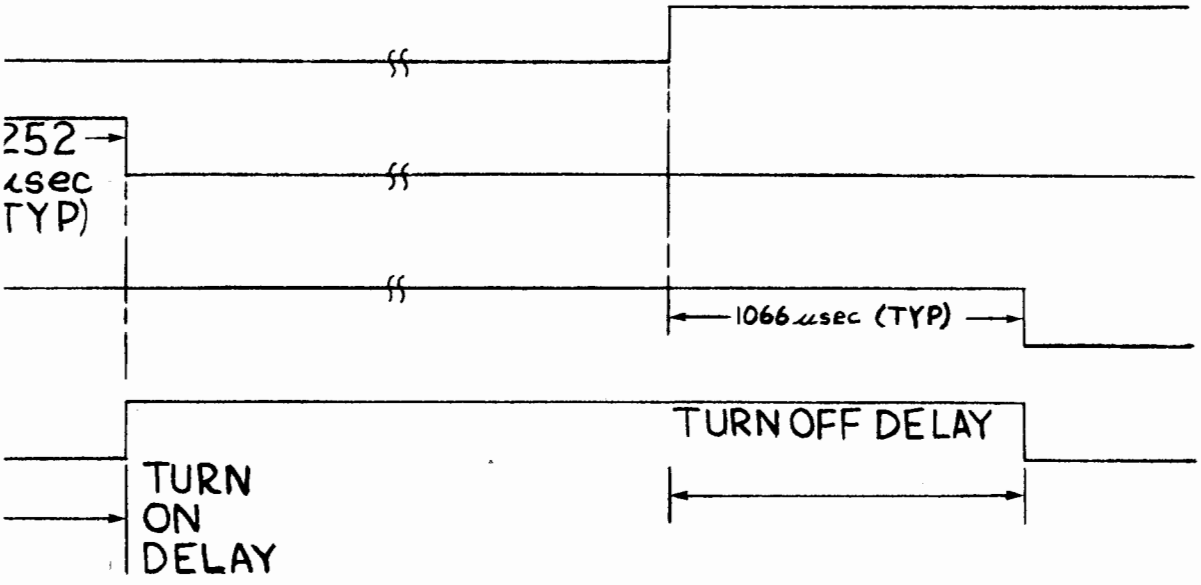


Figure 10
Tunnel Erase Timing
DEC-29-80 13255-91223

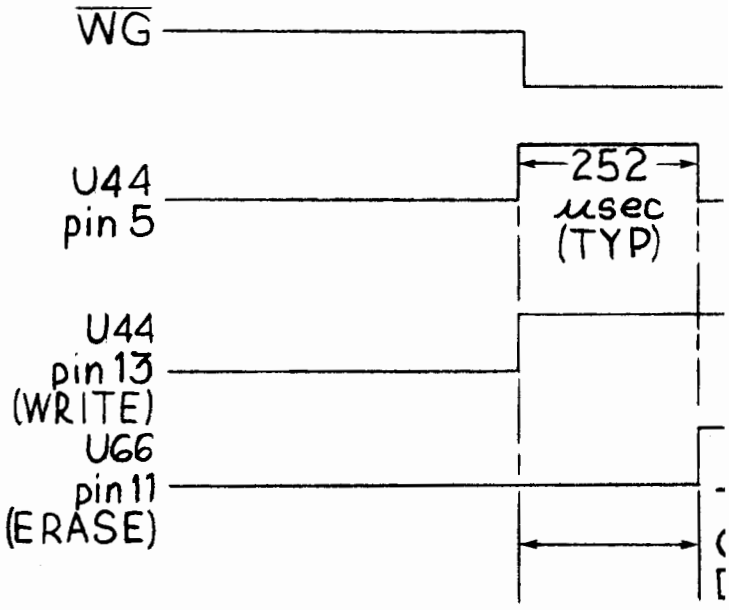


FIG. 10 TUNNEL ERASE TIMING

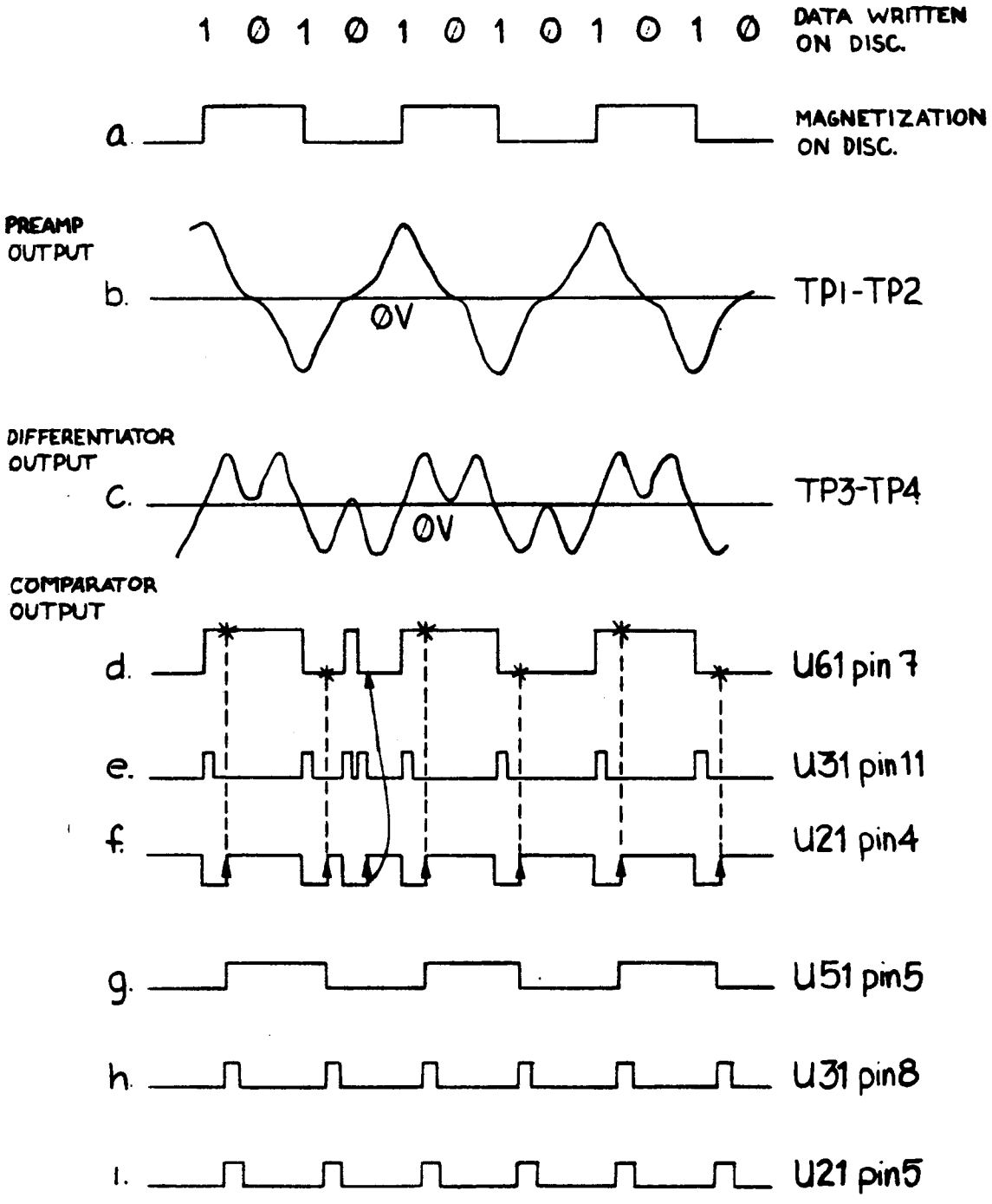


FIG. 11 READ CIRCUIT TIMING DIAGRAM

Figure 11
Read Circuit Timing Diagram
DEC-29-80 13255-91223

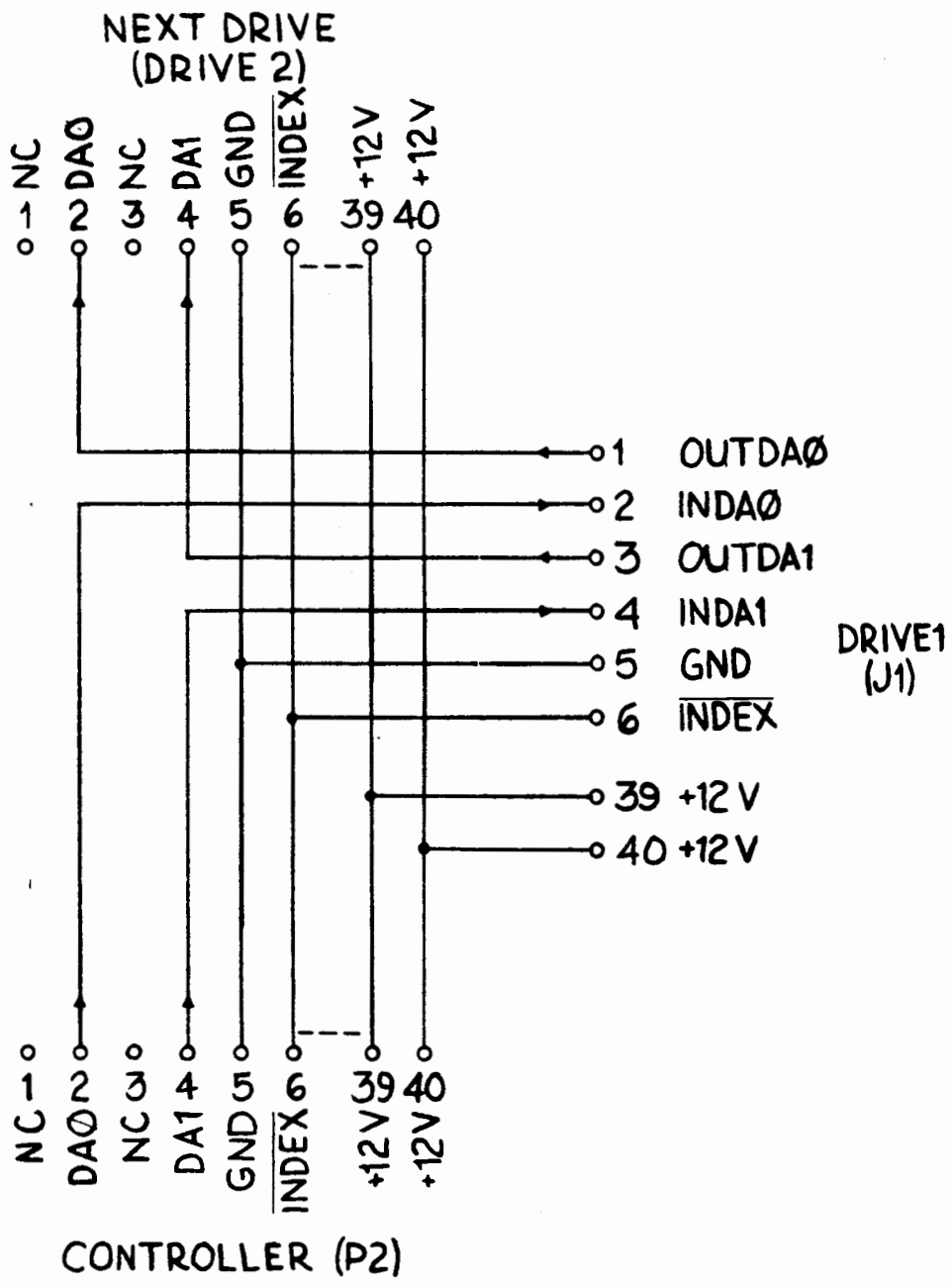


FIG. 12 T-BLOCK SCHEMATIC

Figure 12
T-Block Schematic Diagram
DEC-29-80 13255-91223

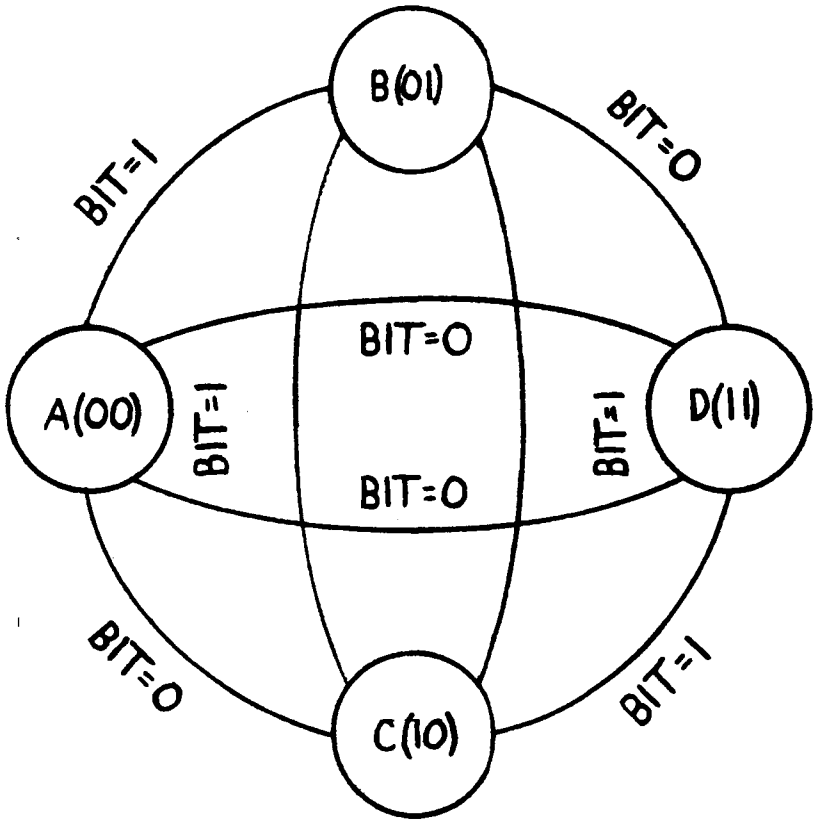


FIG.13 MFM ENCODING ALGORITHM STATE MACHINE

Figure 13
MFM Encoding Algorithm State Machine
DEC-29-80 13255-91223

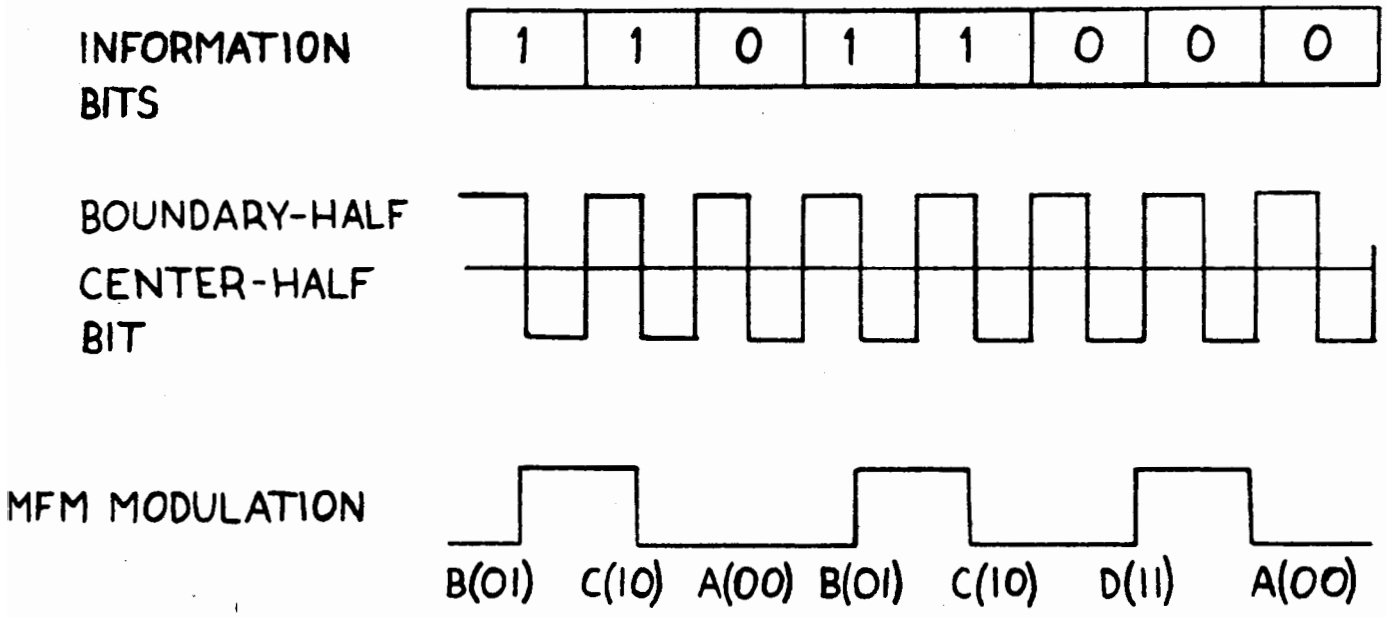


FIG. 14 MFM MODULATION

Figure 14
MFM Modulation
DEC-29-80 13255-91223

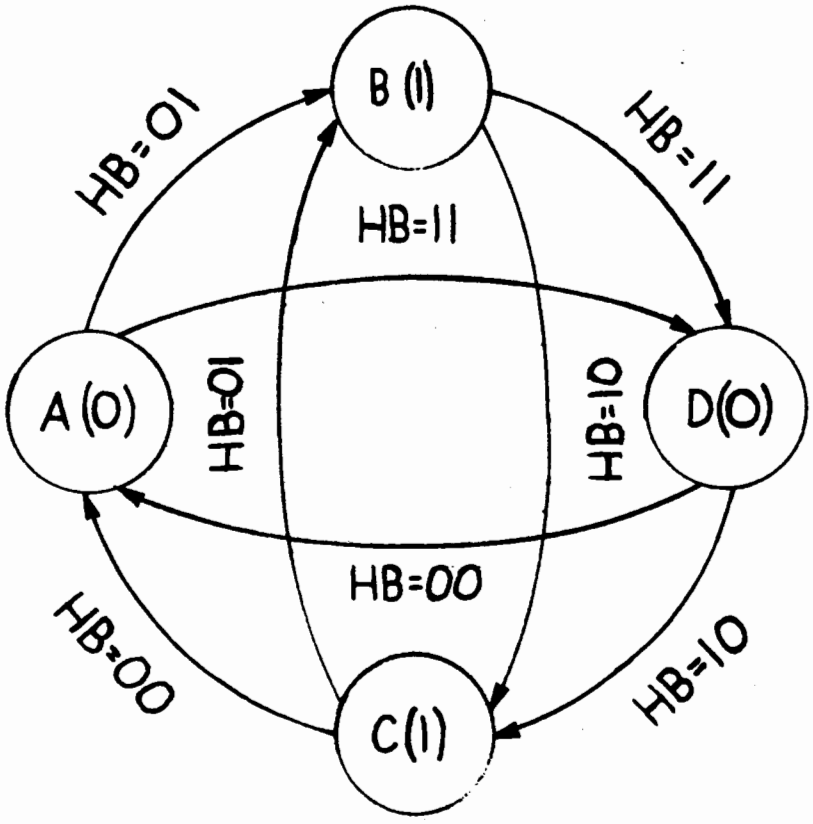


FIG. 15 MFM DECODING ALGORITHM STATE MACHINE

Figure 15
MFM Decoding Algorithm State Machine
DEC-29-80 13255-91223

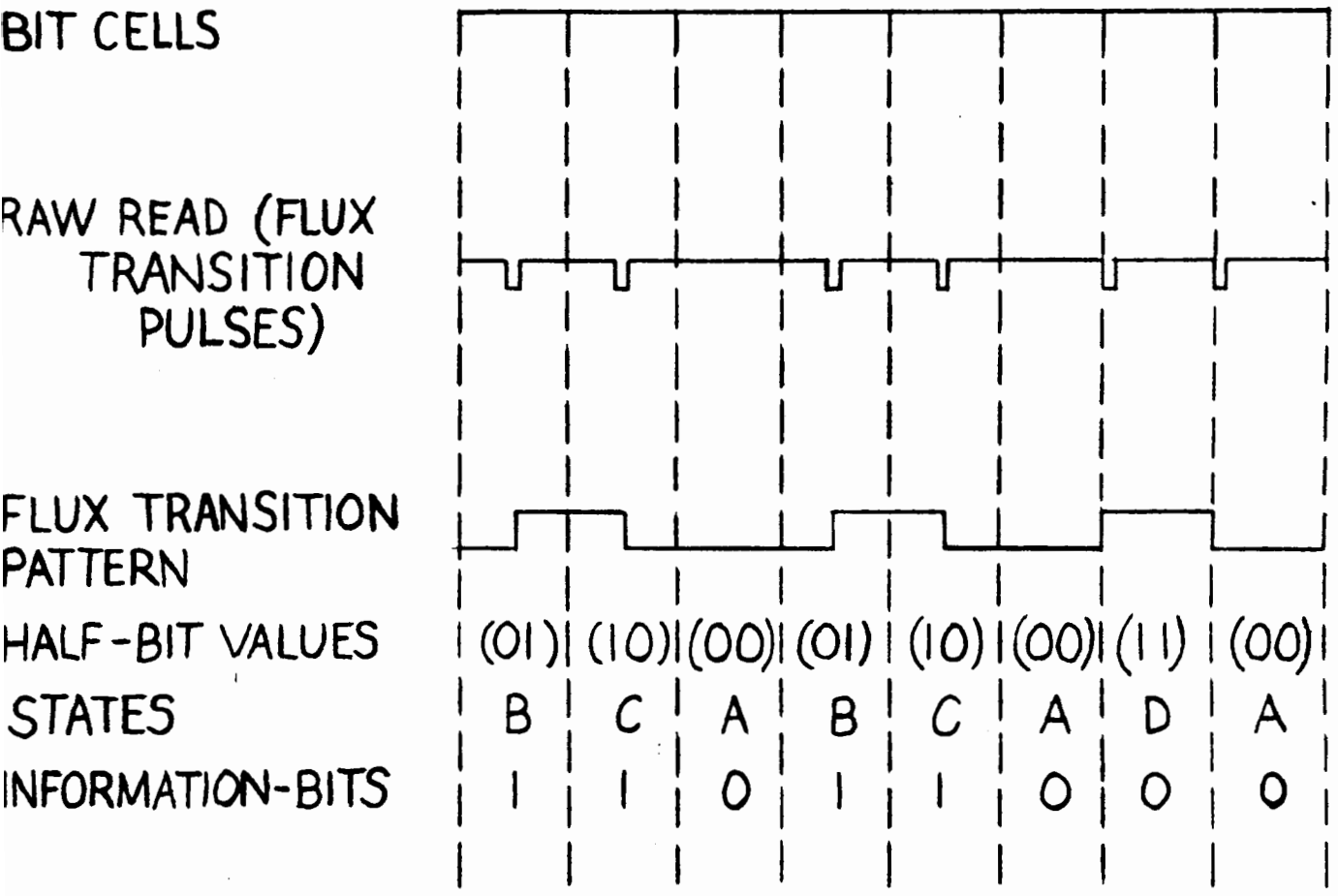
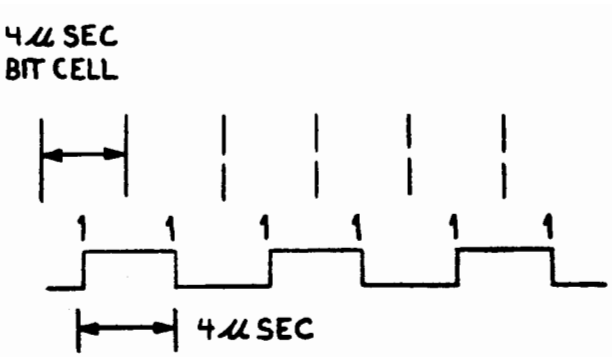
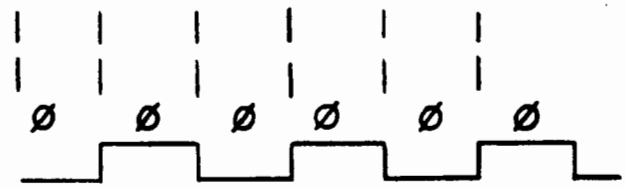


FIG. 16 MFM DECODING TIMING DIAGRAM

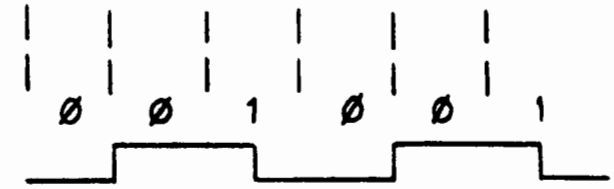
Figure 16
MFM Decoding Timing Diagram
DEC-29-80 13255-91223



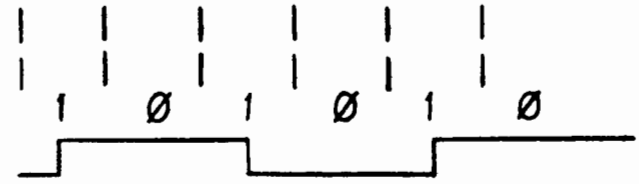
ALLONES DATA - 2f DATA (250 KHZ)



ALL ZEROS DATA - 2f DATA



PATTERN GENERATING 6μSEC PERIOD
PULSE STREAM



PATTERN GENERATING 8μSEC PERIOD
PULSE STREAM - 1f DATA (125 KHZ)
ENCODING RULES :

1. A TRANSITION IS WRITTEN ON THE MIDDLE OF THE BIT CELL FOR EVERY "1."
2. A TRANSITION IS WRITTEN ON THE CELL BOUNDARY WHEN TWO ZEROS OCCUPY ADJACENT BIT CELLS.

FIG. 17 MFM PATTERNS

Figure 17
MFM Patterns
DEC-29-80 13255-91223

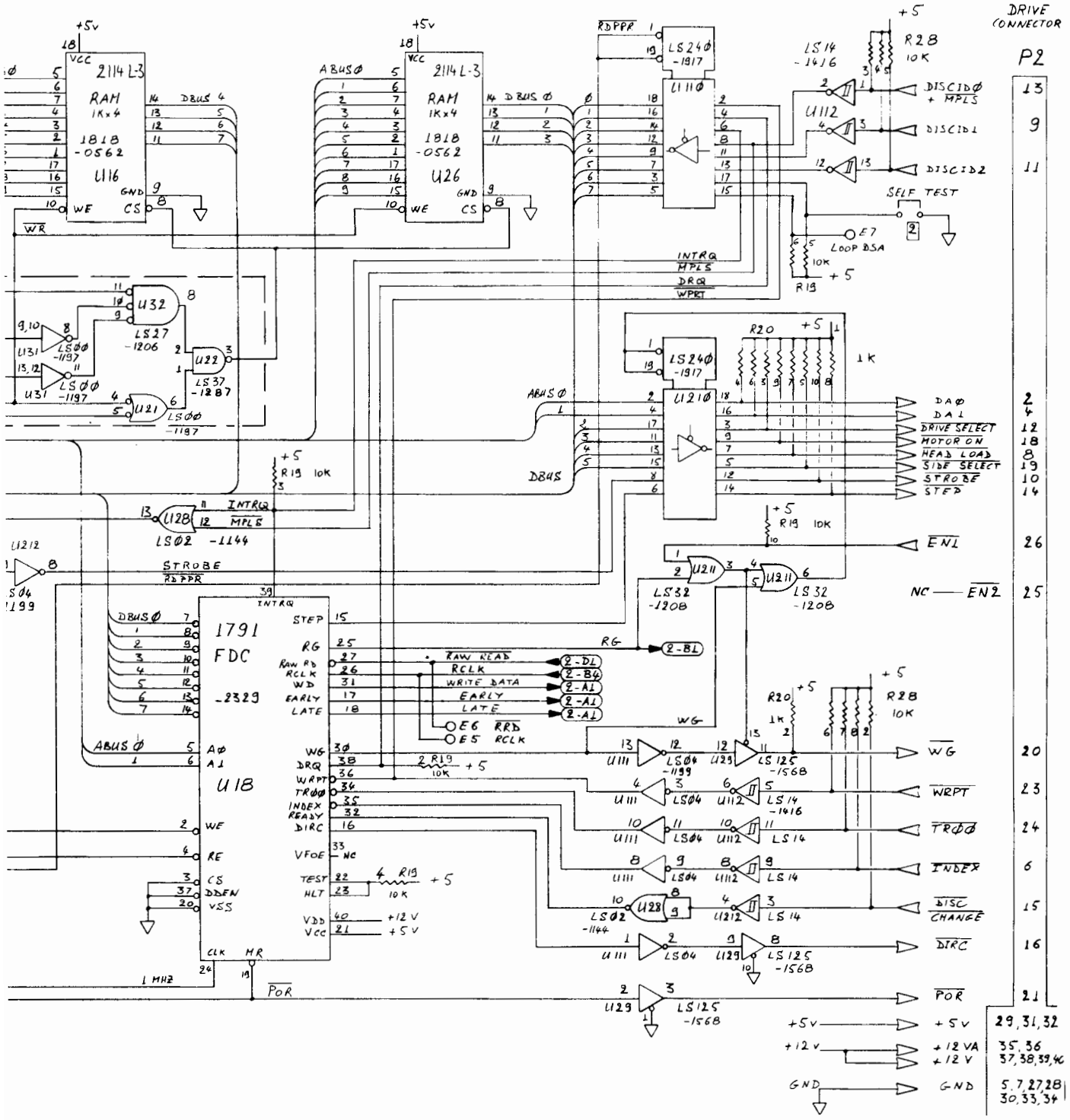
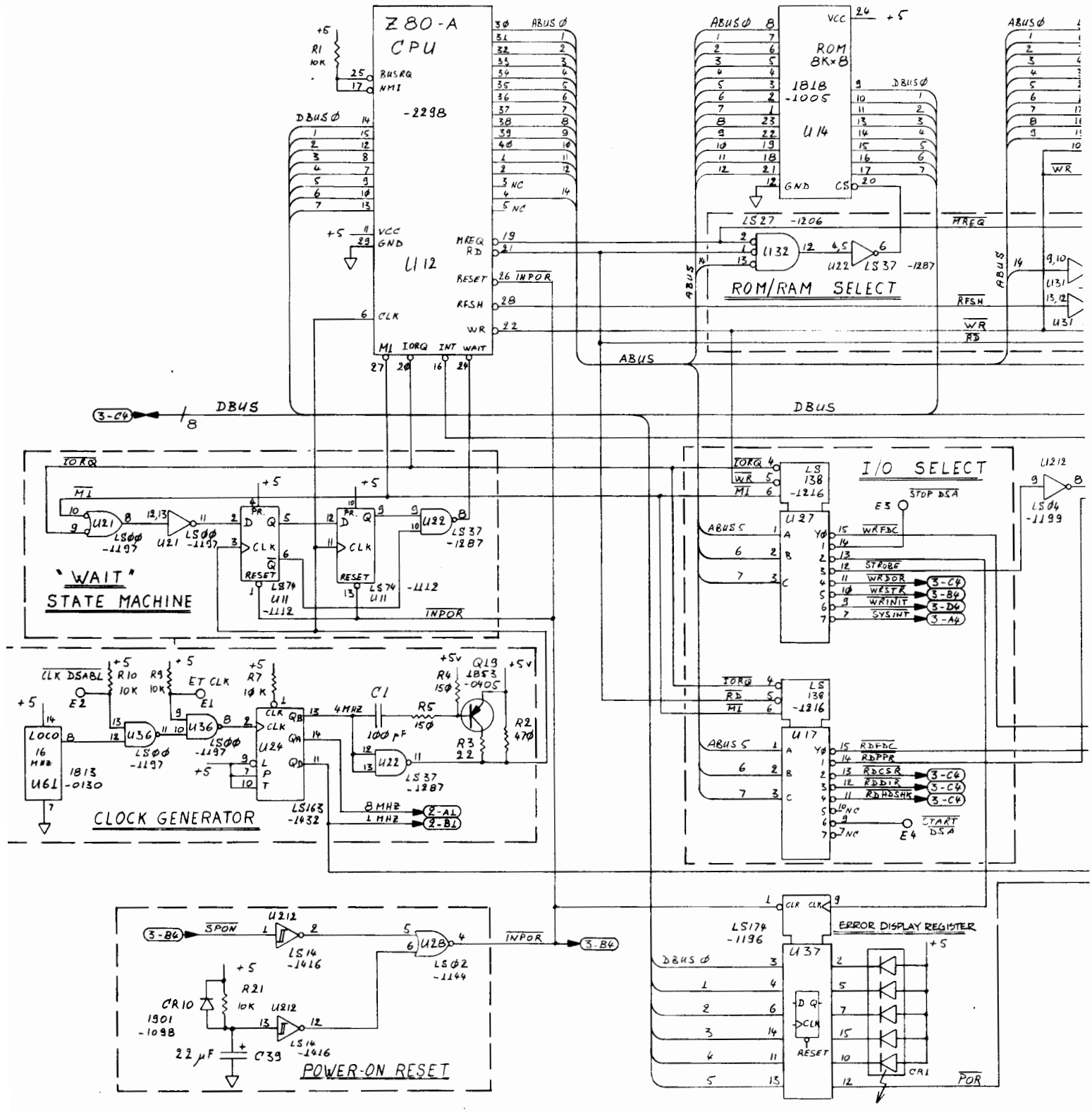


Figure 18
Minifloppy Controller PCA Schematic Diagram
DEC-29-80 13255-91223

NOTES

1 - UNLESS OTHERWISE NOTICED, ALL IC'S 1820 - PREFIX. ALL RESISTORS ARE IN OHMS, ¼ W, 5%.

2 - JUMPER INSTALLED FOR CONTINUOUS SELF TEST ONLY



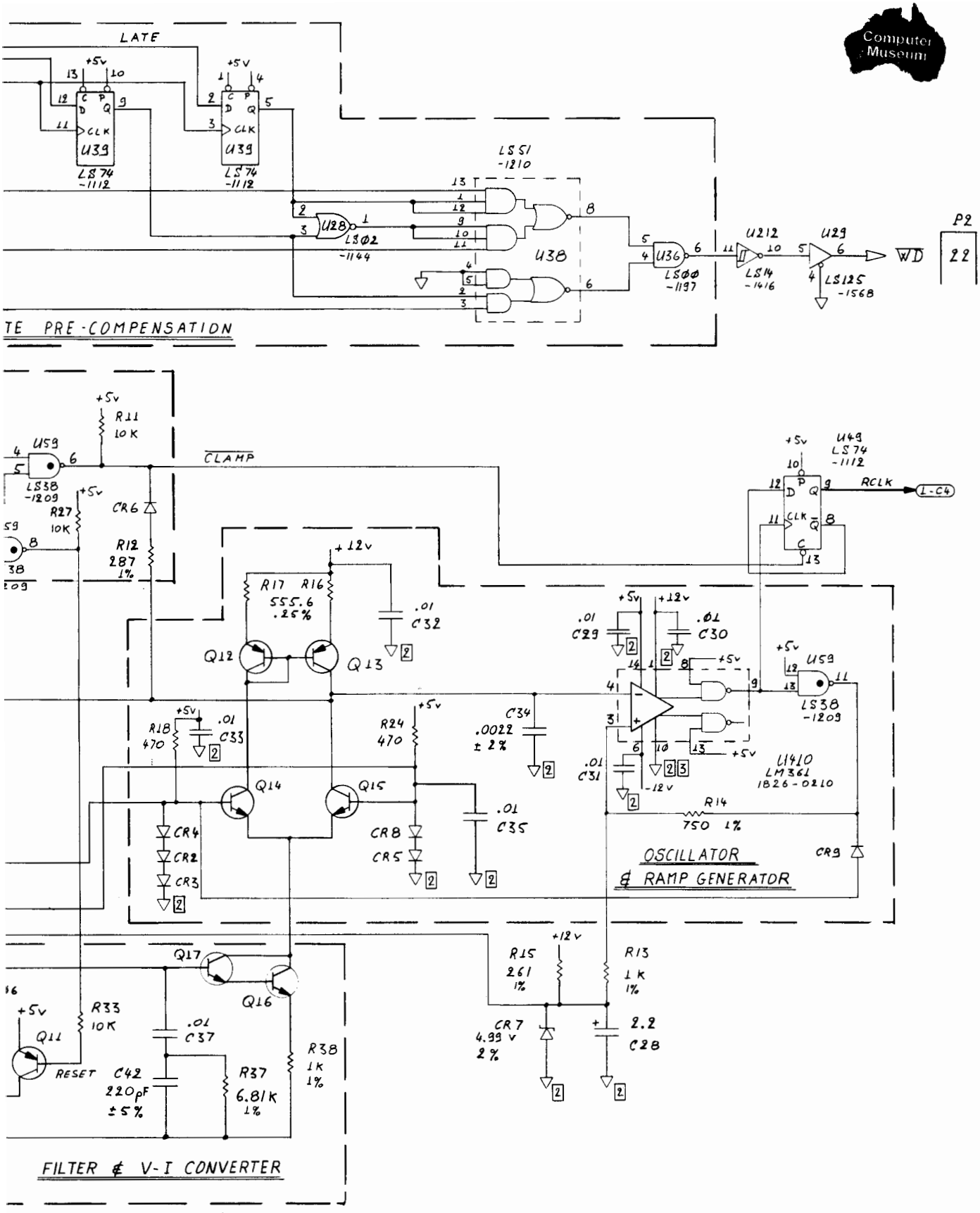
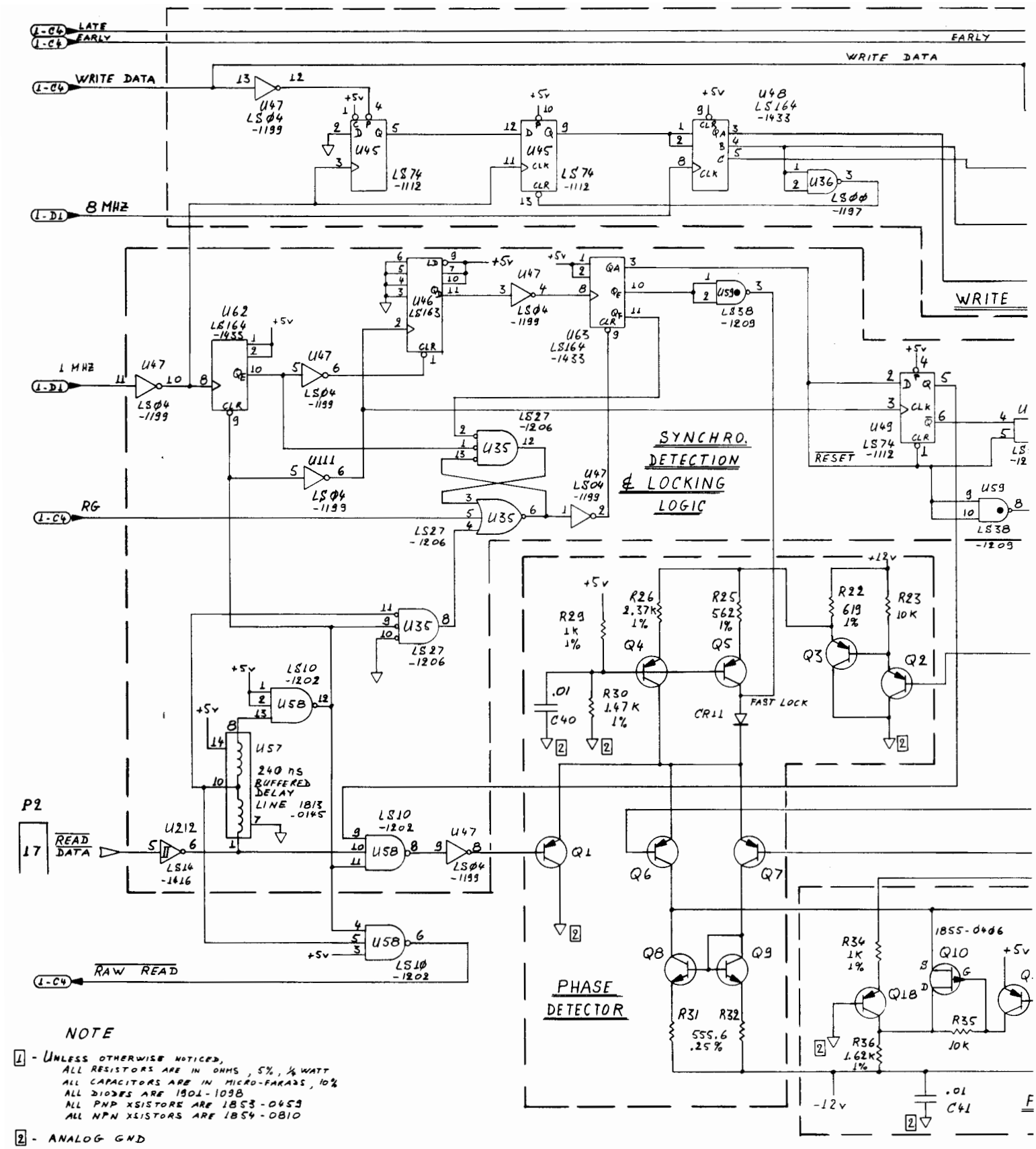


Figure 18
Minifloppy Controller PCA Schematic Diagram
DEC-29-80 13255-91223



NOTE

1 - UNLESS OTHERWISE NOTICED,
ALL RESISTORS ARE IN OHMS, 5%, ¼ WATT
ALL CAPACITORS ARE IN MICRO-FARADS, 10%
ALL DIODES ARE 1901-1098
ALL PNP XSISTORS ARE 1853-0453
ALL NPN XSISTORS ARE 1854-0810

2 - ANALOG GND

3 - ANALOG AND LOGIC GND CONNECTED AT U410 PIN10

NOTES.

1 - UNLESS OTHERWISE NOTICED,
ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
ALL CAPACITORS ARE IN MICROFARADS, 10%.
ALL IC'S 1820 - PREFIX.

2 - .01 BYPASS CAPS ARE C2-8, 10-12, 14-17, 19-27, 36, 38, 40, 41.

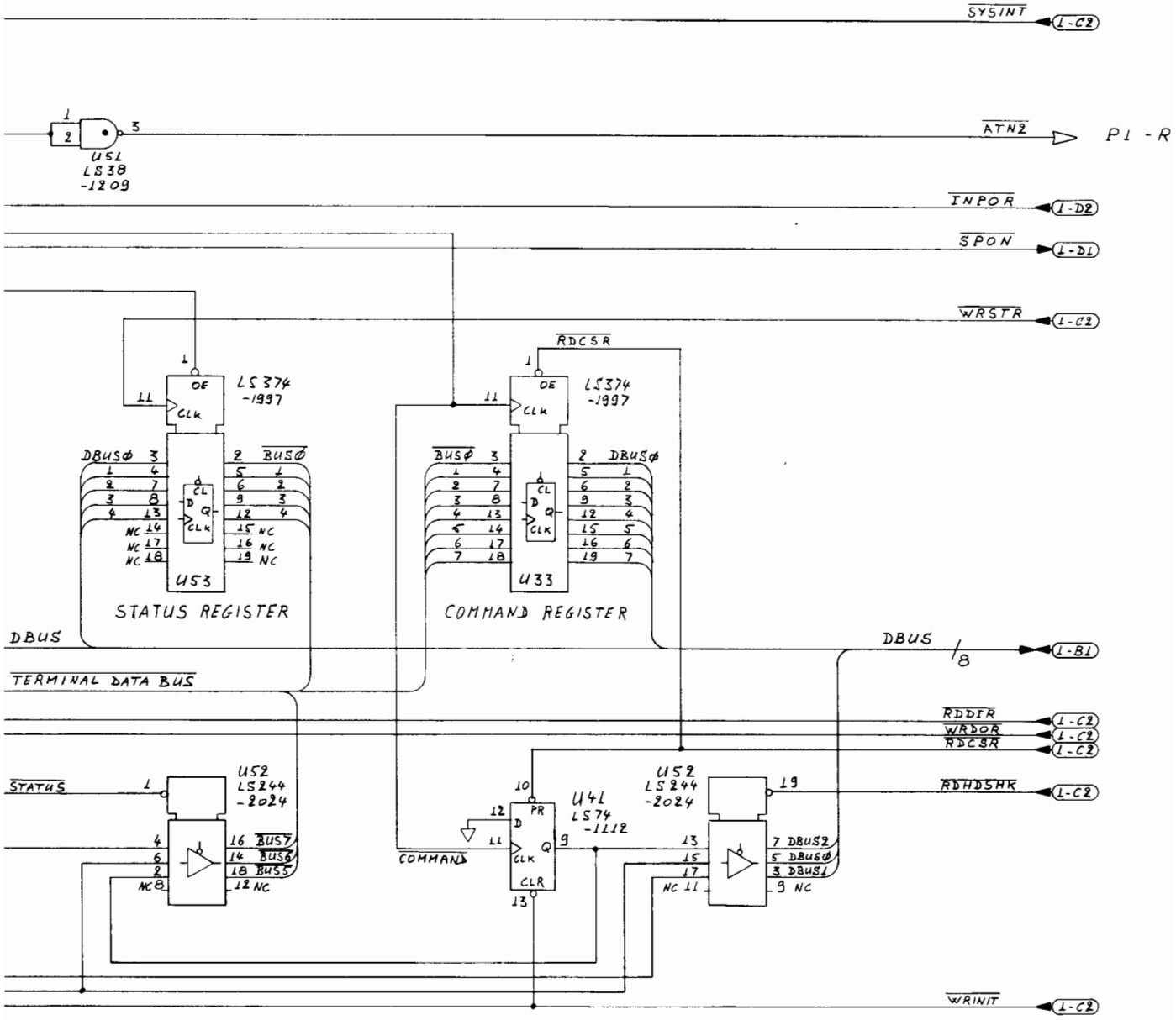
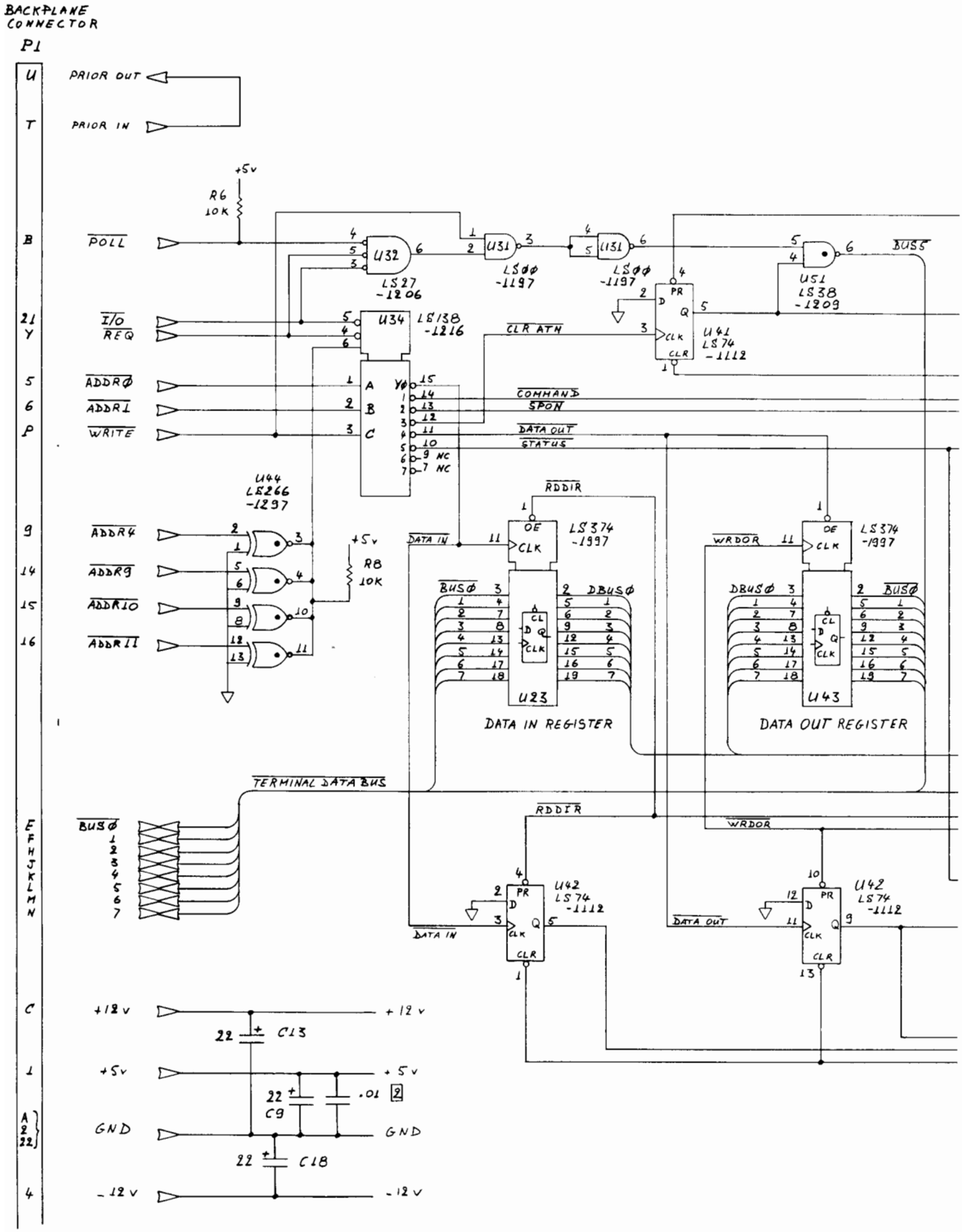


Figure 18
Minifloppy Controller PCA Schematic Diagram
DEC-29-80 13255-91223


BACKPLANE CONNECTOR
P1
U
T
B
21
Y
5
6
P
9
14
15
16
E
F
H
J
K
L
M
N
C
1
A
2
22
4
PRIOR OUT
PRIOR IN
+5v
R6 10K
POLL
I/O REQ
ADDRØ
ADDR1
WRITE
ADDR4
ADDR9
ADDR10
ADDR11
BUSØ
1
2
3
4
5
6
7
U32 LS27 -1206
U31 LSØØ -1197
U131 LSØØ -1197
U34 LS138 -1216
U44 LS266 -1297
R8 10K
CLR ATN
U41 LS74 -1112
U51 LS38 -1209
BUSS
COMMAND SPON
DATA OUT STATUS
RDDIR
DATA IN
LS374 -1997
BUSØ
DBUSØ
U23
DATA IN REGISTER
WRDOR
U43
DATA OUT REGISTER
TERMINAL DATA BUS
U42 LS74 -1112
DATA OUT
+12 v
-12 v
GND
22 C13
22 C9
.01
22 C18

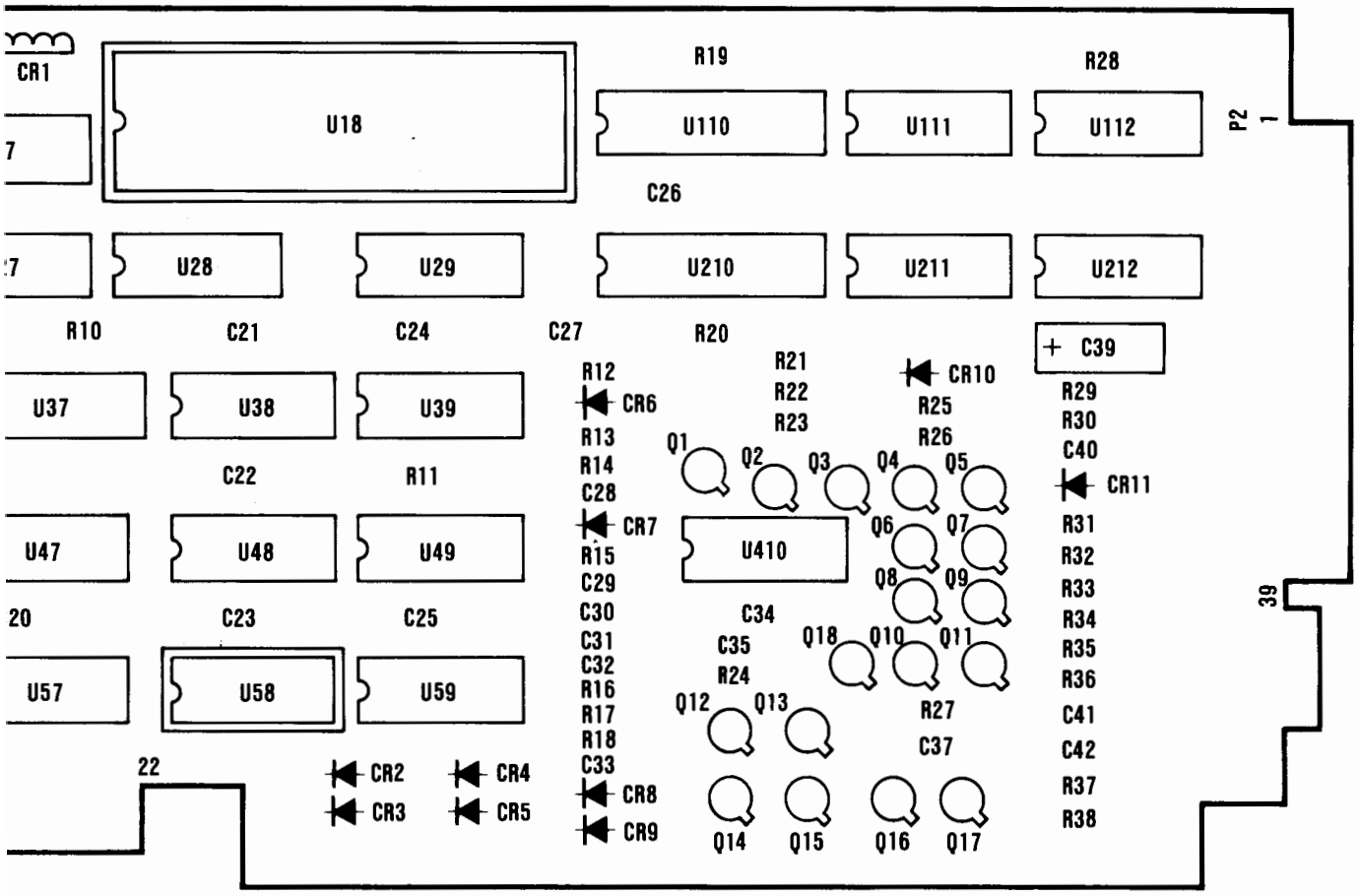
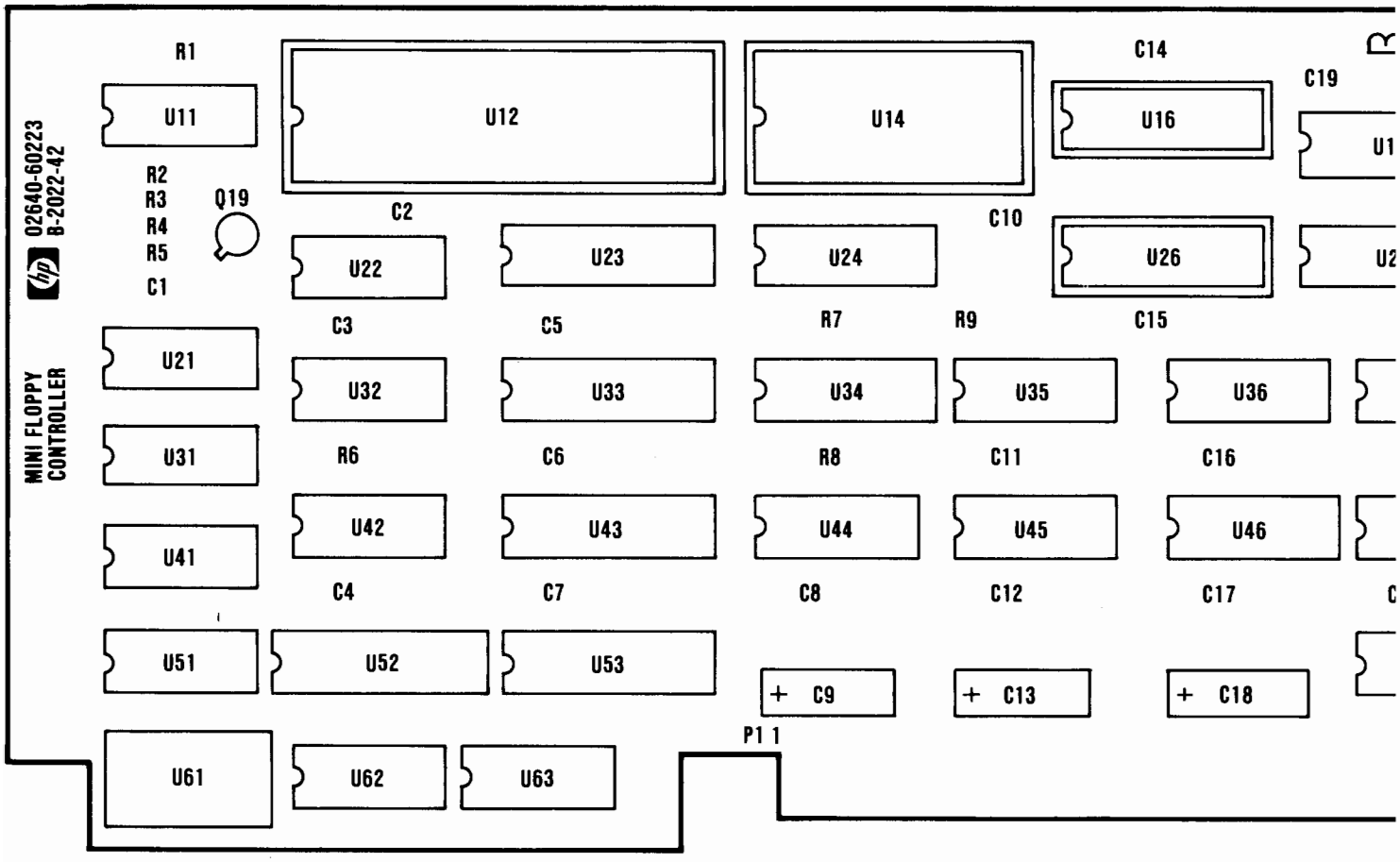


Figure 19
Minifloppy Controller PCA Component Location Diagram
DEC-29-80 13255-91223


02640-60223
B-2022-42
MINI FLOPPY
CONTROLLER
R1
U11
U12
U14
C14
U16
C19
R2
R3
R4
R5
Q19
C1
C2
U22
U23
U24
C10
U26
C3
C5
R7
R9
C15
U21
U32
U33
U34
U35
U36
U31
R6
C6
R8
C11
C16
U42
U43
U44
U45
U46
U41
C4
C7
C8
C12
C17
U51
U52
U53
+ C9
+ C13
+ C18
P1 1
U61
U62
U63

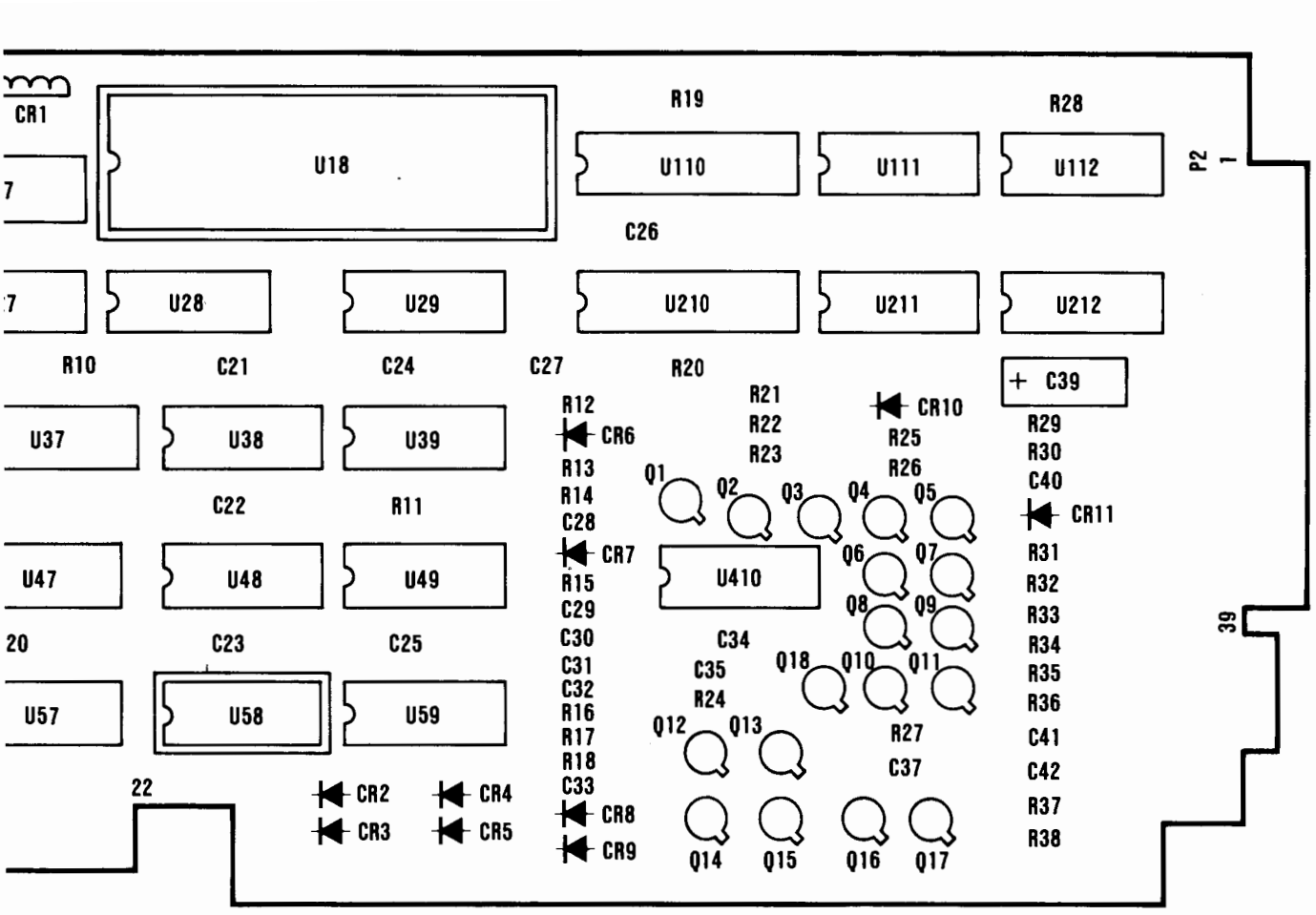
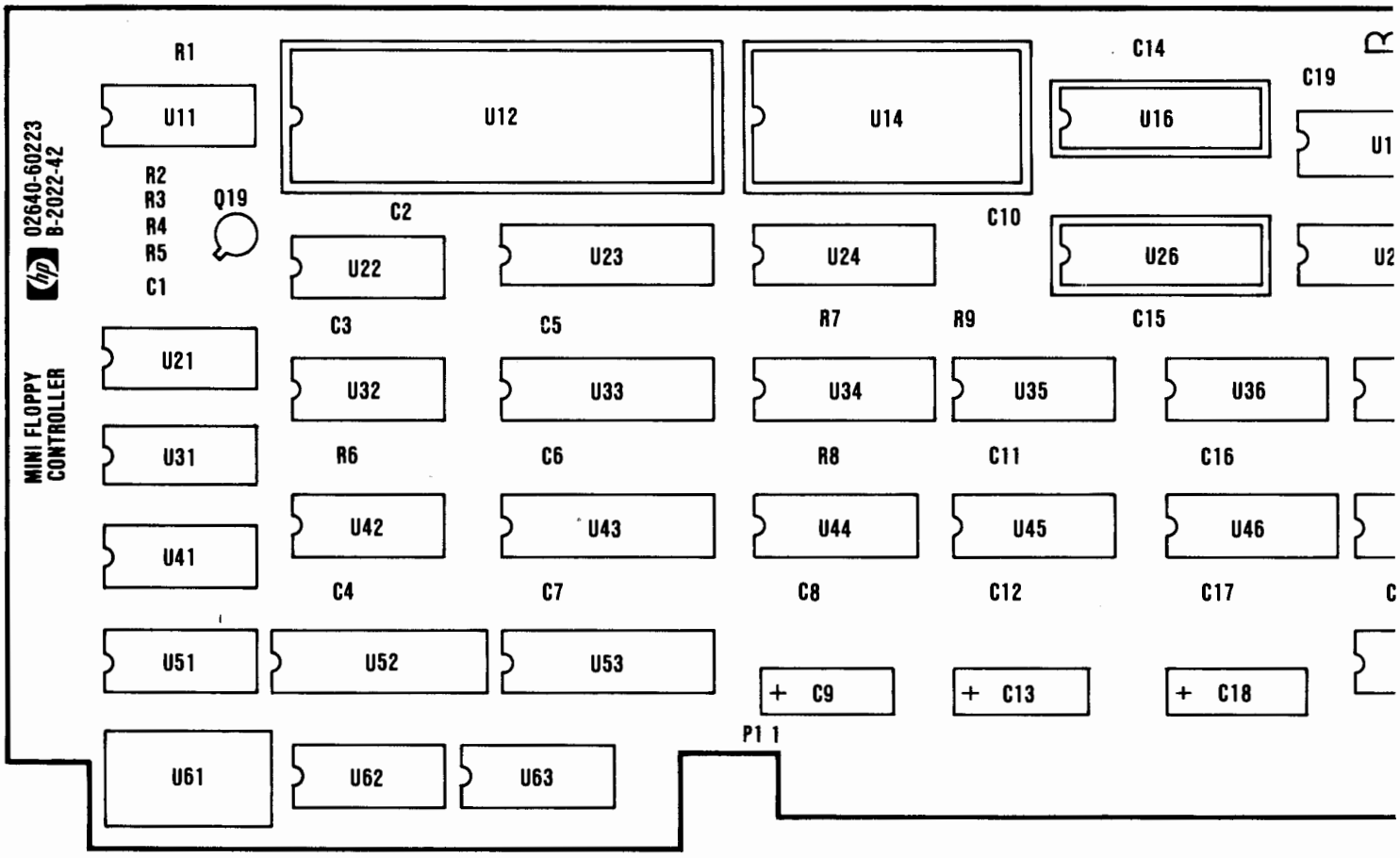
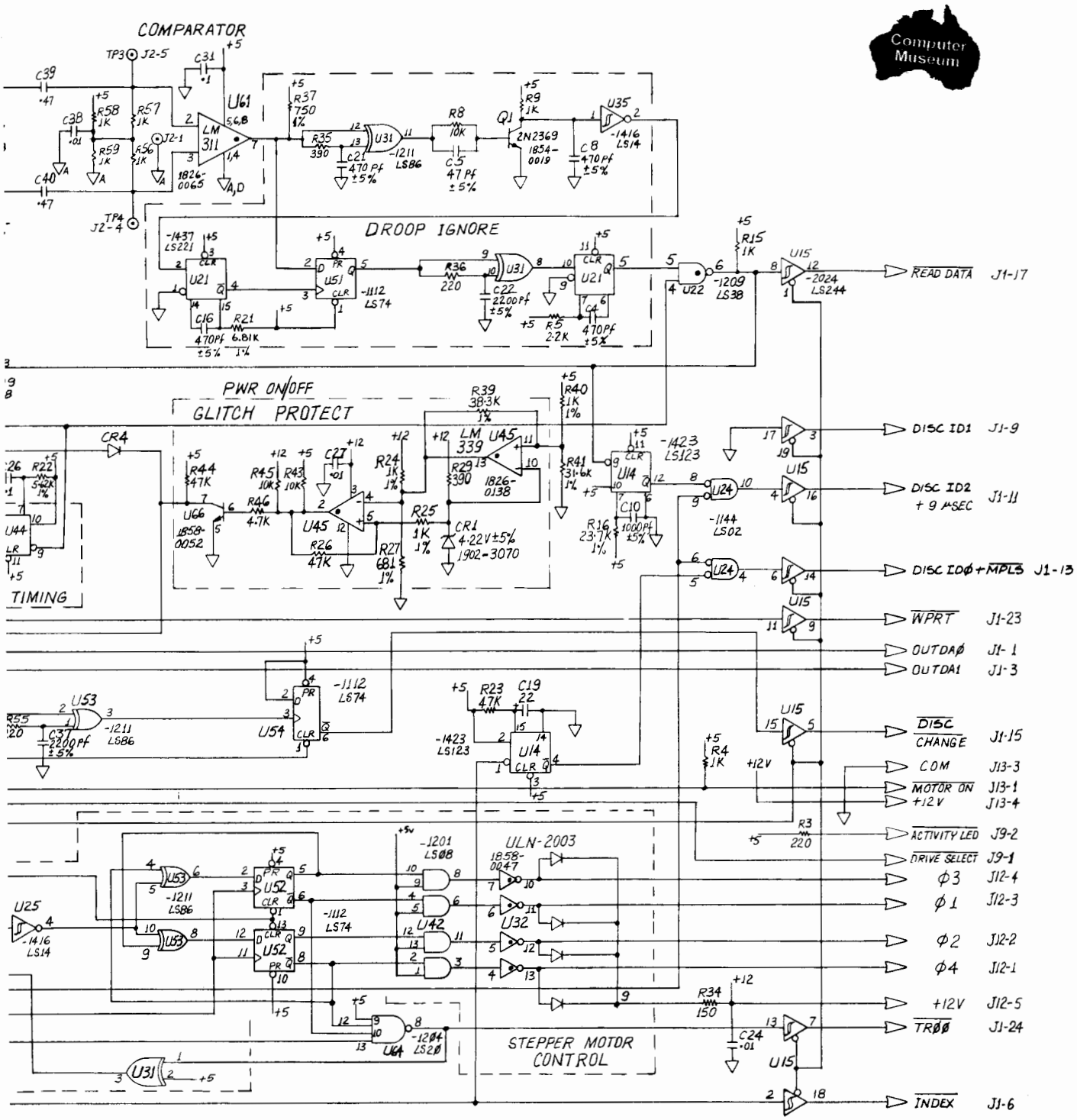


Figure 19
Minifloppy Controller PCA Component Location Diagram
DEC-29-80 13255-91223

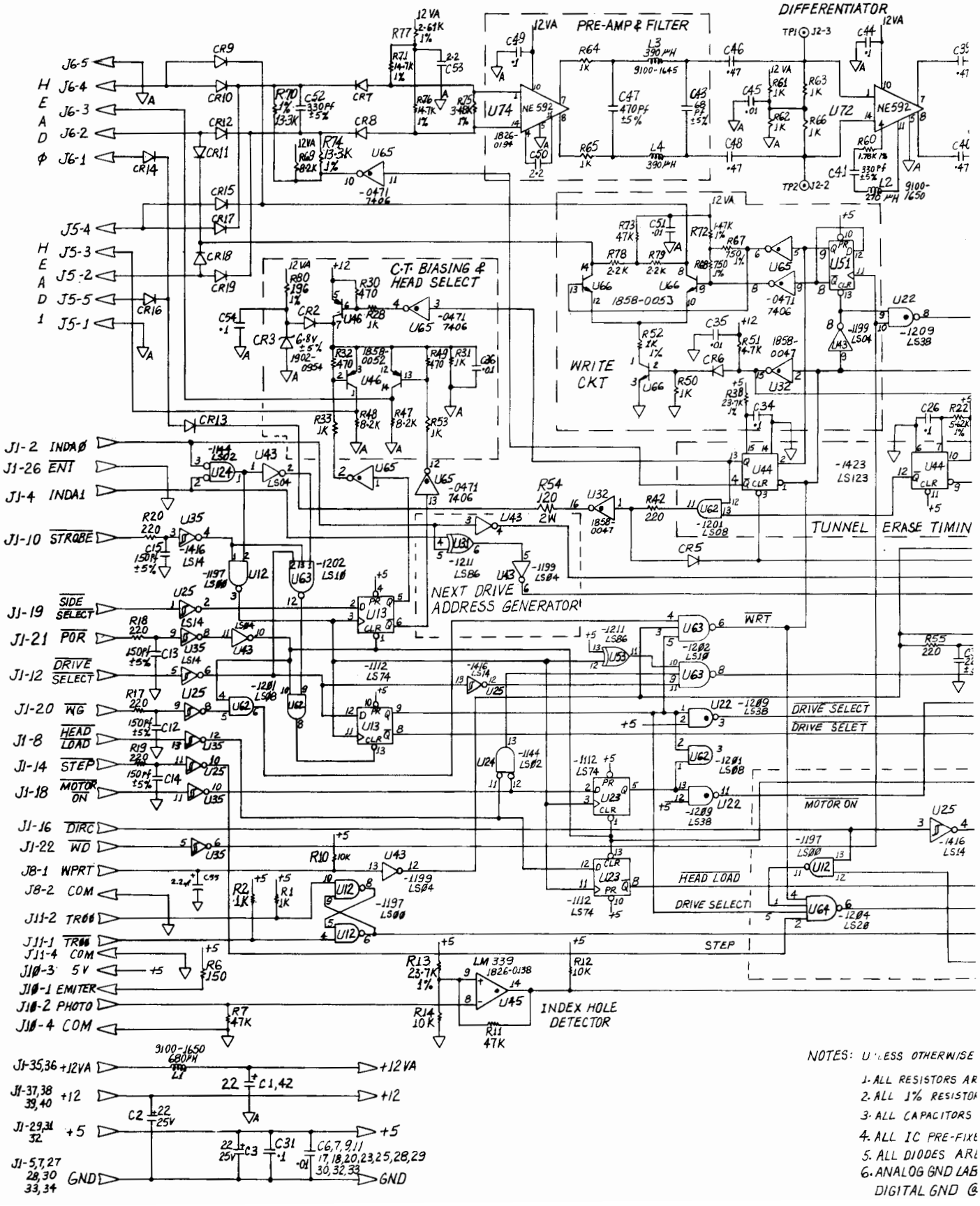

02640-60223
B-2022-42
MINI FLOPPY
CONTROLLER
R1
U11
U12
U14
C14
U16
C19
U1
R2
R3
R4
R5
Q19
C1
C2
U22
U23
U24
C10
U26
U2
C3
C5
R7
R9
C15
U21
U32
U33
U34
U35
U36
U31
R6
C6
R8
C11
C16
U42
U43
U44
U45
U46
U41
C4
C7
C8
C12
C17
U51
U52
U53
+ C9
+ C13
+ C18
P1 1
U61
U62
U63



ERWISE SPECIFIED

STORS ARE IN OHMS, 5%, ¼ W
RESISTORS ARE ⅛ W
ACITORS IN μF, 10%
PRE-FIXES ARE 1820
DES ARE 1901-1098
GND LABELLED ▽A. CONNECTED TO GND @ U61 PINS 1 & 4.

Figure 20
Drive Electronics PCA Schematic Diagram
DEC-29-80 13255-91223



NOTES: U[illegible] LESS OTHERWISE

1. ALL RESISTORS AR
2. ALL 1% RESISTOR
3. ALL CAPACITORS
4. ALL IC PRE-FIXE
5. ALL DIODES ARE
6. ANALOG GND LAB
DIGITAL GND @

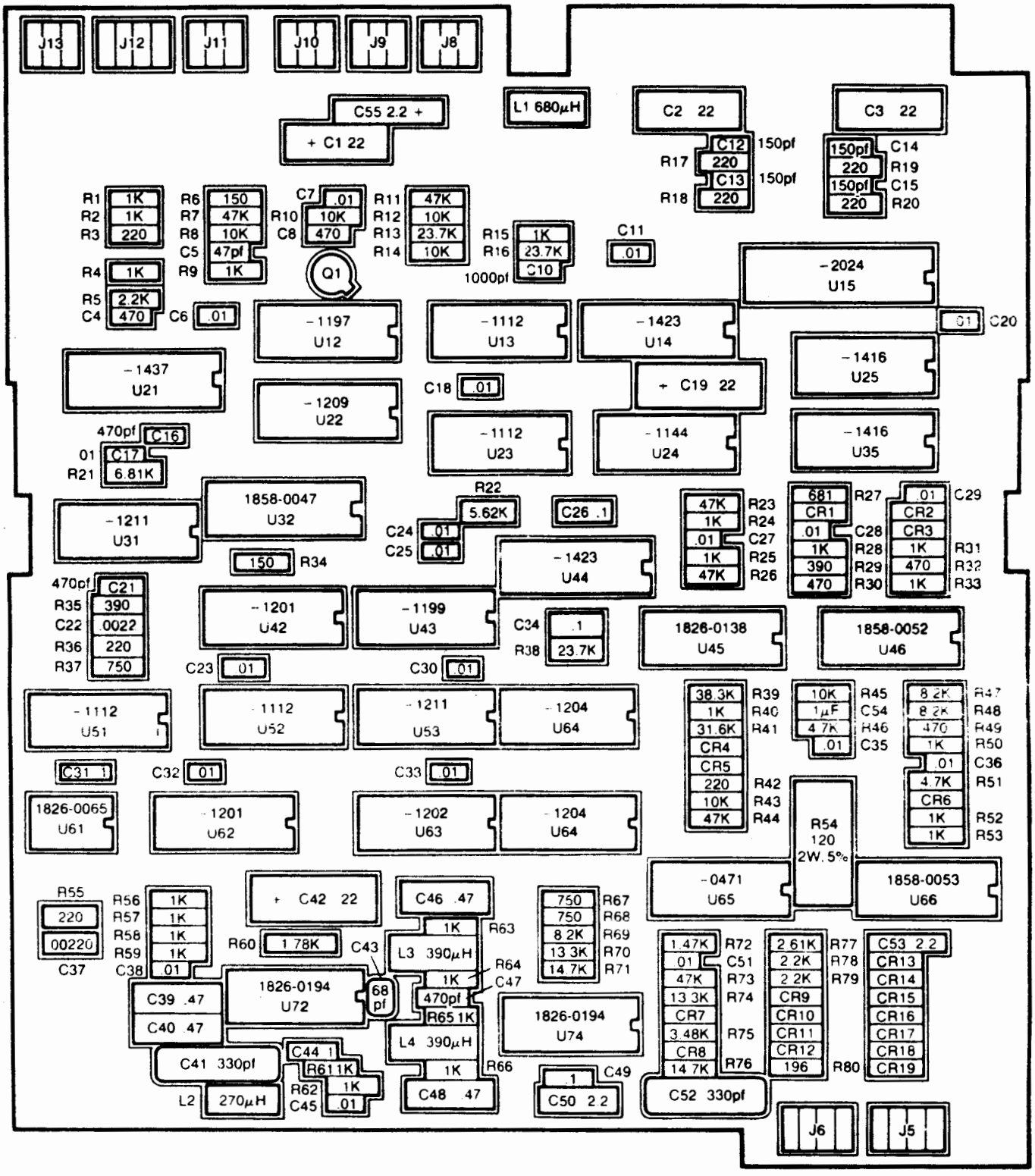


Figure 21
Drive Electronics PCA Component Location Diagram
DEC-29-80 13255-91223

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60223	9	1	MINI-FLOPPY CONTROLLER, PCA	28480	02640-60223
C1	0160-4801	7	1	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C2	0160-4554	7	33	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C4	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C9	0180-2879	7	4	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C13	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C22	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C23	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C24	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C25	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C26	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C27	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C28	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C29	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C30	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C31	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C32	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C33	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C34	0160-5091	9	1	CAPACITOR-FXD 2200PF 2% POLYP	28480	0160-5091
C35	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C36	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C37	0160-0161	4	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C38	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C39	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C40	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C41	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C42	0160-4812	0	1	CAPACITOR-FXD 220PF +-5% 100VDC CER	28480	0160-4812
CR1	1990-0622	2	1	LED-LAMP ARRAY LUM-INT=200UCD	28480	1990-0622
CR2	1901-1098	1	9	DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR3	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR4	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR5	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR6	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR7	1902-3092	1	1	DIODE-ZNR 4.99V 2% DO-35 PD=.4W	28480	1902-3092
CR8	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR9	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR10	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR11	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
Q1	1853-0459	3	12	TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q2	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q3	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q4	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q5	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q6	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q7	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q8	1854-0810	2	6	TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0810
Q9	1854-0810	2		TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0810
Q10	1855-0406	4	1	TRANSISTOR J-FET P-CHAN D-MODE SI	32293	IT110
Q11	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q11	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q12	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q13	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q14	1854-0810	2		TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0810
Q15	1854-0810	2		TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0810
Q16	1854-0810	2		TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0810
Q17	1854-0810	2		TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0810
Q18	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
Q19	1853-0485	9	1	TRANSISTOR PNP SI PD=300MW FT=850MHZ	04713	2N4209

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R1	0683-1035	1	12	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R2	0683-4715	8	3	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R3	0683-2205	9	1	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R4	0683-1515	2	2	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R5	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R6	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R7	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R8	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R9	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R10	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R11	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R12	0698-3443	0	1	RESISTOR 287 1% .125W F TC=0+-100	24546	C4-1/8-T0-287R-F
R13	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R14	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
R15	0698-3132	4	1	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
R16	0699-0038	5	4	RESISTOR 555.6 .25% .125W F TC=0+-50	28480	0699-0038
R17	0699-0038	5		RESISTOR 555.6 .25% .125W F TC=0+-50	28480	0699-0038
R18	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R19	1810-0280	8	2	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R20	1810-0275	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R21	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R22	0757-0418	9	1	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
R23	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R24	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R25	0757-0417	8	1	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
R26	0698-3158	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
R27	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R28	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R29	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R30	0757-1094	9	1	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R31	0699-0038	5		RESISTOR 555.6 .25% .125W F TC=0+-50	28480	0699-0038
R32	0699-0038	5		RESISTOR 555.6 .25% .125W F TC=0+-50	28480	0699-0038
R33	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R35	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R36	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
R37	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
R38	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
S1	1251-1556	7	2	CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
S2	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
U11	1820-1112	8	6	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U12	1820-2298	3	1		28480	1820-2298
U14	1818-1005	3	1	IC NMOS 32768 (32K) ROM 450-NS 3-S	55376	SYP2332 MASKED
U16	1818-0562	5	2	IC NMOS 4096 (4K) RAM STAT 250-NS 3-S	34649	P2114A-5
U17	1820-1216	3	3	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U18	1820-2329	1	1	IC MISC NMOS 8-BIT	52840	FD1791B-01
U21	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U22	1820-1287	8	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS37N
U23	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U24	1820-1432	5	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U26	1818-0562	5		IC NMOS 4096 (4K) RAM STAT 250-NS 3-S	34649	P2114A-5
U27	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U28	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U29	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U31	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U32	1820-1206	1	2	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U33	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U34	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U35	1820-1206	1		IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U36	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U37	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74L8174N
U38	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
U39	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U41	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U42	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U43	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U44	1820-1297	0	1	IC GATE TTL LS EXCL-NOR QUAD 2-INP	01295	SN74LS266N
U45	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U46	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U47	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U48	1820-1433	6	3	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
U49	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U51	1820-1209	4	2	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U52	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U53	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U57	1813-0145	0	1	IC MISC HYBRID	0739H	STTL DM-429
U58	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U59	1820-1209	4		IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U61	1813-0130	3	1	IC OSC HYBRID	34344	K1148A-16.0MH7
U62	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
U63	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
U110	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U111	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U112	1820-1416	5	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U210	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U211	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U212	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U410	1826-0210	7	1	IC COMPARATOR HS 14-DIP-P PKG	27014	LM361N
XU12	1200-0654	7	2	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU14	1200-0541	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU16	1200-0539	7	2	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU18	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU26	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU58	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
Z1	0360-0124	3	8	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124

Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	13270-60002	7	1	MINI-FLOPPY DRIVE, PCA	28480	13270-60002
C1	0180-2879	7	5	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C2	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C3	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C4	0160-4808	4	5	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C5	0160-4805	1	1	CAPACITOR-FXD 47PF +-5% 100VDC CER 0+-30	28480	0160-4805
C6	0160-4554	7	21	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C10	0160-4822	2	1	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4814	2	4	CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4814
C13	0160-4814	2		CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4814
C14	0160-4814	2		CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4814
C15	0160-4814	2		CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4814
C16	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C22	0160-4819	7	2	CAPACITOR-FXD 2200PF +-5% 100VDC CER	28480	0160-4819
C23	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C24	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C25	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C26	0160-4557	0	6	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C27	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C28	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C29	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C30	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C31	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C32	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C33	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C34	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C35	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C36	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C37	0160-4819	7		CAPACITOR-FXD 2200PF +-5% 100VDC CER	28480	0160-4819
C38	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C39	0160-0174	9	4	CAPACITOR-FXD .47UF +80-20% 25VDC CER	28480	0160-0174
C40	0160-0174	9		CAPACITOR-FXD .47UF +80-20% 25VDC CER	28480	0160-0174
C41	0160-4810	8	2	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C42	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C43	0160-4350	1	1	CAPACITOR-FXD 68PF +-5% 200VDC CER 0+-30	28480	0160-4350
C44	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C45	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C46	0160-0174	9		CAPACITOR-FXD .47UF +80-20% 25VDC CER	28480	0160-0174
C47	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C48	0160-0174	9		CAPACITOR-FXD .47UF +80-20% 25VDC CER	28480	0160-0174
C49	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C50	0180-0197	8	3	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C51	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C52	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C53	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C54	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C55	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
CR1	1902-3070	5	1	DIODE-ZNR 4.22V 5% DO-35 PD=.4W	28480	1902-3070
CR2	1901-1098	1	17	DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR3	1902-0954	8	1	DIODE-ZNR 6.8V 5% DO-35 PD=.4W TC=+.057%	28480	1902-0954
CR4	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR5	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR6	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR7	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR8	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR9	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR10	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR11	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR12	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR13	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR14	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR15	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR16	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR17	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR18	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150
CR19	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	0004G	1N4150

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
J2	1251-5103	8	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-5103
J5	1251-4051	3	2	CONNECTOR 10-PIN M POST TYPE	28480	1251-4051
J6	1251-4051	3		CONNECTOR 10-PIN M POST TYPE	28480	1251-4051
J8	1251-5343	8	3	CONNECTOR 12-PIN M POST TYPE	28480	1251-5343
J9	1251-5343	8		CONNECTOR 12-PIN M POST TYPE	28480	1251-5343
J10	1251-5343	8		CONNECTOR 12-PIN M POST TYPE	28480	1251-5343
J11	1251-6053	9	3	CONNECTOR 13-PIN M POST TYPE	28480	1251-6053
J12	1251-6053	9		CONNECTOR 13-PIN M POST TYPE	28480	1251-6053
J13	1251-6053	9		CONNECTOR 13-PIN M POST TYPE	28480	1251-6053
L1	9100-1650	1	1	INDUCTOR RF-CH-MLD 680UH 5% .2DX.45LG	28480	9100-1650
L2	9100-1642	1	1	INDUCTOR RF-CH-MLD 270UH 5% .2DX.45LG	28480	9100-1642
L3	9100-1645	4	2	INDUCTOR RF-CH-MLD 390UH 5% .2DX.45LG	28480	9100-1645
L4	9100-1645	4		INDUCTOR RF-CH-MLD 390UH 5% .2DX.45LG	28480	9100-1645
Q1	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R1	0683-1025	9	20	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R2	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R3	0683-2215	1	8	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R4	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R5	0683-2225	3	3	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R6	0683-1515	2	2	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R7	0683-4735	4	6	RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
R8	0683-1035	1	6	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R9	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R10	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R11	0683-4735	4		RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
R12	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R13	0698-3158	4	3	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
R15	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R16	0698-3158	4		RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
R17	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R18	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R19	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R20	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R21	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
R22	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
R23	0683-4735	4		RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
R24	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R25	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R26	0683-4735	4		RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
R27	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
R28	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R29	0683-3915	0	2	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
R30	0683-4715	0	4	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R31	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R32	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R33	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R34	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R35	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
R36	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R37	0757-0420	3	3	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
R38	0698-3158	4		RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
R39	0698-3161	9	1	RESISTOR 38.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3832-F
R40	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R41	0698-3160	8	1	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
R42	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R43	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R43	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R44	0683-4735	4		RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
R45	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R46	0683-4725	2	2	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R47	0683-8225	5	3	RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
R48	0683-8225	5		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
R49	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R50	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R51	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R52	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R53	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R54	0698-3622	7	1	RESISTOR 120 5% 2W MO TC=0+-200	28480	0698-3622
R55	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R56	0683-1025	9		RESISTOR 1K 5% .25W FC TC= 400/+600	01121	CB1025
R57	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R58	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R59	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R60	0757-0278	9	1	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R61	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R62	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R63	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R64	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R65	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R66	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R67	0757-0420	3		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
R68	0757-0420	3		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
R69	0683-8225	5		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
R70	0757-0289	2	2	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
R71	0698-3156	2	2	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
R72	0757-1094	9	1	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R73	0683-4735	4		RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
R74	0757-0289	2		RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
R75	0698-3152	8	1	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
R76	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
R77	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
R78	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R79	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R80	0698-3440	7	1	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
R81	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
U12	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U13	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U14	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
U15	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U21	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U22	1820-1209	4	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U23	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U24	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U25	1820-1416	5	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U31	1820-1211	8	2	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U32	1858-0047	5	1	TRANSISTOR ARRAY 16-PIN PLSTC DIP	13606	ULN-2003A
U35	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U43	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U44	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
U45	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
U46	1858-0052	2	1	TRANSISTOR ARRAY 14-PIN PLSTC TO-116	04713	SPQ1678
U51	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U52	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U53	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U54	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U61	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P PKG	01295	SN72311P
U62	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U63	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U64	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U65	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
U66	1858-0053	3	1	TRANSISTOR ARRAY 14-PIN PLSTC DIP	28480	1858-0053
U72	1826-0194	6	2	IC WIDEBAND AMPL VID 14-DIP-P PKG	18324	NE592A
U74	1826-0194	6		IC WIDEBAND AMPL VID 14-DIP-P PKG	18324	NE592A

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	13270-60003	8	2	CABLE-1.2 METER	28480	13270-60003
A2	13270-60003	8		CABLE-1.2 METER	28480	13270-60003
	0624-0098	0	4	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0098
	0890-0790	2	1	TUBING-HS .046 DIA	28480	0890-0790
	1251-6177	8	2	CONNECTOR-2 X 20 .100 PC	28480	1251-6177
	1400-0770	2		CABLE CLAMP	18992	MARK 5018
	1600-1016	5	2	CLIP-HOOD, GROUND	28480	1600-1016
	2200-0091	7	2	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2260-0002	6	2	NUT-HEX-DBL-CHAM 4-40-THD .062-IN-THK	00000	ORDER BY DESCRIPTION
	3030-0143	0	2	SCREW-SET 6-32 .5-IN-LG SMALL CUP-PT ALY	00000	ORDER BY DESCRIPTION
	8120-3040	8		CABLE-SHIELDED 40-CONDUCTOR	28480	8120-3040
	5040-6004	7	2	CLAMP-CABLE-SMALL	28480	5040-6004
	5040-6086	5	2	HOOD-CONNECTOR	28480	5040-6086
	5041-1004	9	2	MOUNTING BLOCK-EXT	28480	5041-1004

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	13270-60004	9	1	CABLE-0.7 METER	28480	13270-60004
	0624-0098	0	4	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0098
	0890-0790	2		TUBING-HS .046 DIA	28480	0890-0790
	1251-6177	8	2	CONNECTOR-2 X 20 .100 PC	28480	1251-6177
	1400-0770	2		CLAMP-CABLE	18992	MARK 5018
	1600-1016	5	2	CLIP-HOOD,GROUND	28480	1600-1016
	2200-0091	7	2	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2260-0002	6	2	NUT-HEX-DBL-CHAM 4-40-THD .062-IN-THK	00000	ORDER BY DESCRIPTION
	3030-0143	0	2	SCREW-SET 6-32 .5-IN-LG SMALL CUP-PT ALY	00000	ORDER BY DESCRIPTION
	8120-3040	8		CABLE-SHIELDED 40-CONDUCTOR	28480	8120-3040
	5040-6004	7	2	CLAMP-CABLE-SMALL	28480	5040-6004
	5040-6086	5	2	HOOD-CONNECTOR	28480	5040-6086
	5041-1004	9	2	MOUNTING BLOCK-EXT.	28480	5041-1004

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	13270-60005	0	1	T-BLOCK	28480	13270-60005
	0470-0231	6		COMPOUND-NUT LOCK	05972	242
	1251-6177	8	1	CONNECTOR-2 X 20 .100 PC	28480	1251-6177
	2200-0147	4	2	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	13270-00001	8	1	COVER-T.BLOCK	28480	13270-00001
	13270-80005	2	1	BOARD-ETCHED	28480	13270-80005

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
0004G	UNITRODE COMPUTER PRODUCTS CORP	METHUEN	MA	
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
05972	LOCTITE CORP	NEWINGTON	CT	06111
0739H	NO M/F DESCRIPTION FOR THIS MFG NUMBER			
13606	SPRAGUE ELECT CO SEMICONDUCTOR DIV	CONCORD	NH	03301
16299	CORNING GL WK ELEC CMPNT DIV	RALEIGH	NC	27604
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
18992	HANSCOM H F CO INC	PROVIDENCE	RI	02905
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
32293	INTERSIL INC	CUPERTINO	CA	95014
34344	MOTOROLA INC	FRANKLIN PARK	IL	60131
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
52840	WESTERN DIGITAL CORP	NEWPORT BEACH	CA	92626
55576	SYNERTEK	SANTA CLARA	CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247