HP 13255

EXTENDED DISPLAY MEMORY ACCESS MODULE

Manual Part No. 13255-91124

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1.0 INTRODUCTION.

The Extended Display Memory Access (DMA) fetches characters and imbedded control codes to be displayed on the screen. The Extended DMA fills a line buffer with 80 displayable characters, then trades the buffer to the Display Control and Display Timing PCA's for actual dot generation. The Extended DMA has a bus controller which enables it to get characters from memory without processor intervention.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Extended DMA Module is contained in tables 1.0 through 6.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60124	Extended DMA PCA	12.5 x 4.0 x 0.5	0.35
Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.099 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 640 mA	@ mA	@ 30 mA	@ mA
	NOT APPLICABLE		NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
MSBI	ADDR14, ADDR15 = 1,1	ADDR14, ADDR15 = 0,0

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21		Not Used
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P		Not Used
-R		
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Not Available)
-X		Not Used
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not Used

5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1 through Pin -4		Not Used
-5	$\overline{D1}$	Negative True, Character Dot Position 1
-6		Not Used
-7		
-8	EVEN	Even Row
-9	LBLOAD	Bus Buffer Load
-10	GVS	Vertical Sync
-11		Not Used
-12		
-13	$\overline{IV}$	Negative True, Inverse Video
Pin -14 through Pin -18		Not Used
-19	$\overline{BLNK}$	Negative True, Blanking
-20		Not Used
-21	LOAD	Line Buffer Load
-22		Not Used

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A through Pin -J		Not Used
-K	OCIRC	Line Buffer Circulation
-L	OCIRCEN	Line Buffer Circulation Enable
-M		Not Used
-N		
-P	BIT0	Negative True, ASCII Bit 0
-R	BIT1	Negative True, ASCII Bit 1
-S	BIT2	Negative True, ASCII Bit 2
-T	BIT3	Negative True, ASCII Bit 3
-U	BIT4	Negative True, ASCII Bit 4
-V	BIT5	Negative True, ASCII Bit 5
-W	BIT6	Negative True, ASCII Bit 6
-X	CYS	Negative True, Cursor Y Position Strobe
-Y		Not Used
-Z		

Table 6.0 Module Bus Pin Assignments

Function Performed: Extended DMA On/Off, Maybe EOP, Maybe SKIPEOL

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0111)
Note: Module Address is actually decoded by Display Control PCA.

Extended DMA responds to $\overline{CYS}$ on P3, Pin X.

Function Specifier:
(B6 B5) Extended DMA Control (See table below)
(B4 B3 B2 B1 B0) Cursor Y Position Set

Data Bus Bit Interpretation:

B7 Not Applicable

B6 B5 DMA CONTROL FUNCTION

0	0	DMA On
0	1	DMA On, Maybe EOP
1	0	DMA Off, Maybe SKIPEOL
1	1	DMA Off

B4 Cursor Y Position Bit 4

B3 Cursor Y Position Bit 3

B2 Cursor Y Position Bit 2

B1 Cursor Y Position Bit 1

B0 Cursor Y Position Bit 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
1	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts list 02640-60124 located in the appendix.

The Extended DMA PCA fetches characters from the memory to refresh the display. Each line of characters is found in memory by following through the linked list which begins at the top address of logical memory. Imbedded in the list are control codes to select alternate character sets, alter selection of video enhancement, indicate an end of the current line or page, and link to another part of memory. When an end of line code (EOL) is found, the Extended DMA pads the current line with blanks out to column 80. When an end of page (EOP) code is found, the Extended DMA pads the remainder of the current line with blanks and fills all subsequent lines of the current frame scan with blanks also.
also.

The start of a new frame is indicated by receiving a GVS (Vertical Sync) signal from the display timing circuit. This pulse sets the Extended DMA PCA address register to point at the top of memory.

The start of a new line is indicated by INTSET. This pulse resets the column counter to 0. This allows the Extended DMA PCA to begin fetching characters from memory (or padding with blanks) until 80 characters or blanks have been loaded into the line buffer. When the line buffer has been filled with 80 characters, the Extended DMA freezes until the next INTSET, at which time it starts up to fetch another 80 characters.

The Extended DMA has an address register which it uses to drive the bus when fetching characters from memory. This register is implemented with a presettable counter, which is normally decremented after each byte is fetched, whether control bytes or displayable characters have been fetched. When an EOL has been fetched, decrementing is disabled for the rest of the current line, and when an EOP is fetched, decrementing is disabled for the remainder of the page. When a link is fetched, this is detected when the MSB of the link has been fetched, the address counter is decremented and the LSB is fetched from the address immediately below that from which the MSB was fetched, and after the LSB fetch, both LSB and MSB are parallel loaded into the address counter, thus pointing it toward a new part of memory as indicated by the link.
link.

3.1 ADDRESS DRIVERS. The address drivers consist of three 8097 3-state drivers, of which 16 drivers are used to drive bus address lines, and the remaining two drivers are for the $\overline{REQ}$ and $\overline{BUSY}$ lines. The address

signals are presented to the drivers by the address counter for $\overline{\text{ADDR0}}$ through $\overline{\text{ADDR13}}$. The MSBI Jumper provides for setting $\overline{\text{ADDR14}}$ and $\overline{\text{ADDR15}}$ to either "1" or "0", to provide backward compatiblity with the 02640-60009 DMA PCA design which drove only 14 address lines, where the new board drives all 16.

3.2 ADDRESS COUNTER/REGISTER.

3.2.1 The address counter/register holds the address of the current byte to be read from memory by the DMA.

3.2.2 The address counter/register consists of four 74LS161's cascaded into a 14-bit counter. The normal mode of operation is to increment the counter after each byte is read. Note that incrementing the counter actually decrements the logical address.

3.2.3 The Vertical Sync signal (GVS) clears the counter to "0". This effectively sets the counter to all "1" 's since the address bus runs on negative logic while the counter is positive logic, and there is no inversion between the counter and the bus through the drivers.

3.2.4 The parallel load inputs are driven from the MSB (Most Significant Byte) latch and the LSB latch. Only 6 bits are taken from the MSB latch, since only 14 bits of address are settable, with the two most significant bits controlled by the MSBI Jumper. Clocking of the counter takes place at the end of the bus cycle, at the end of the Release state of the bus controller, and 200 nanoseconds after the end of the $\overline{\text{REQ}}$ on the bus. Thus the addresses are changed at the same time as the drivers are turned off.

3.3 MSB LATCH.

3.3.1 The MSB latch holds data read from the bus while it is decoded and either loaded into the line buffers, or interpreted. It also holds the MSB of a link code.

3.3.2 The MSB latch is loaded at the end of $\overline{\text{REQ}}$ on the bus for all byte read operations except the second byte (LSB) of a link address, which is not loaded into the MSB latch. The latch is implemented with 74LS175's to

provide complementary outputs. The inputs are driven from the LSB latch, to which space codes are ORed for EOL and EOP padding.

3.4 LSB LATCH.

3.4.1 The LSB latch should be transparent at all times except during the 200 nanosecond period of the second byte of a link read, when the LSB latch holds the data from the end of $\overline{REQ}$ until the address counter is loaded.

3.4.2 It is therefore implemented with 74LS75's which are enabled at all times except for this 200 nanosecond period. This timing is derived from the bus controller states.

3.5 ROW COUNTER.

3.5.1 The row counter contains the row number currently being loaded by the Extended DMA into the line buffers. It is not the line currently being displayed on the screen.

3.5.2 The row counter is reset by GVS and clocked by the row clock generator, which itself is set by INTSET, and reset by finding a link whose four least significant bits are not all "1" 's, thus indicating a link to a next row pointer. The row counter is implemented with one 74LS293 and one-half 74LS113 to achieve a 5-bit binary counter.

3.6 ROW COMPARATOR.

3.6.1 The row comparator compares the row counter contents to the Cursor Y position sent out by the processor to determine whether the Extended DMA and the processor are working on the same row simultaneously.

3.6.2 The row comparator generates a signal called MATCH which is used to gate EOP and SKIPEOL latches. The two higher order bits of the Cursor Y position ($\overline{BUS5}$ and $\overline{BUS6}$) are used to indicate whetner EOP or SKIPEOL is to be affected. SKIPEOL will only be affected if the Extended DMA has previously seen, and stopped on an EOL in the current line. EOP can be set anywhere during the current line. Additionally, if the Extended DMA is turned off for any reason while it is in the middle of reading a link on the Cursor Y then it will also do an EOP.

3.7 POWER ON BLANKING COUNTER.

3.7.1 The power on blanking counter blanks the display and sets EOP during and following a PWR ON signal.

3.7.2 There are two parts to the counter, both of which are reset by PWR ON. The short counter consists of one 74LS74, which is clocked by INTSET. This generates a delay after PWR ON of at least one full line time (666 microseconds). The long counter is set by filter PWR ON only after 500 nanoseconds of active PWR ON. This prevents the long counter from being triggered by static discharges. The long counter is actually a 74LS164 shift register which is clocked by GVS. It provides a blanking signal at least seven vertical frame scans in duration, to allow adequate time for the Extended DMA to get the line buffers filled with blanks before the screen is unblanked. The outputs of the short and long counters are ORed together to drive the blanking signal and to set EOP.

3.8 COLUMN COUNTER.

3.8.1 The column counter contains the number of displayable characters which have been fetched in the current row.

3.8.2 The column counter is implemented with a 74393 and one 74LS00 gate. When the counter reaches 80, the gate decodes this state and disables the bus controller. This can occur only after 80 bytes have been loaded into the line buffers, since the line buffers and the column counter share the same clock. This clock is derived from the bus controller state following the Release state, and is ANDed with the data output of the byte decoder, to prevent counting links and control codes as displayable bytes. The column counter is reset by INTSET, and this removes the =80 signal, allowing the bus controller to begin reading data for a new line.

3.9 BYTE DECODER.

3.9.1 The byte decoder examines the bit pattern of each byte as it is read to determine whether it is a control code, a data byte, a Link MSB, an EOP, or an EOL. It provides signals to the inputs of the byte type latches to allow them to be clock during the state following release of the bus controller.

3.9.2 Extended DMA byte decoding:

BIT	7	6	5	4	3	2	1	0	MEANING
	0	X	X	X	X	X	X	X	Data Byte (Displayable)
	1	0	X	X	X	X	X	X	Display Enhancement Code
	1	1	1	X	X	X	X	X	Link MSB
	1	1	0	1	X	X	X	X	Link MSB
	1	1	0	0	0	X	X	X	Firmware Flags
	1	1	0	0	1	0	X	X	Firmware Flags
	1	1	0	0	1	1	0	0	EOL
	1	1	0	0	1	1	0	1	EOL
	1	1	0	0	1	1	1	0	EOP
	1	1	0	0	1	1	1	1	0 (Displayable)

3.10 BYTE TYPE LATCHES. The byte type latches are clocked for each byte read from memory. They hold such information as whether an EOL has been seen on the current line, whether an EOP has been seen on the current page, whether we are fetching a link, whether we are waiting to skip one EOL, and whether the previous line ended with an EOL. These latches set up assorted gating throughout the Extended DMA circuit.

3.11 ODD/EVEN LINE BUFFERS.

3.11.1 The odd/even line buffers are 80-byte shift registers which hold the characters to be displayed on the screen.

3.11.2 At any one moment, one of the buffers is being loaded by the Extended DMA and the other is being read by the display dot generator. When the display has completed its current line, the buffer exchanges roles with EVEN, and the Extended DMA begins filling the now empty buffer (by INTSET). The cycle alternates the buffers all the way to the end of the display frame, when the whole process begins again with GVS.

3.12 SELECTOR.

3.12.1 The selector U29 is driven by the display control circuits, selecting either the even or the odd line buffer for display, and allowing the unselected buffer to be loaded by the Extended DMA.

3.12.2 This is done by routing the clock pulses generated by the Extended DMA circuitry (from U19, Pin 8) and the Display Timing PCA circuitry (from P3, Pin K and P3, Pin L) to the appropriate (odd/even) line buffer.

3.13 BUS CONTROLLER.

3.13.1 The bus controller generates the bus control and timing signals to read characters from the display memory.

3.13.2 The bus controller is implemented with four 74LS113 flip-flops. The controller is disabled from running by the =80 signal from the column counter. When enabled, it continually runs through its states reading characters from memory. It also has auxilliary gating to generate most of the timing and control signals used by the other functional blocks on the Extended DMA PCA.

STATE NAME	STATE CODE
Idle	0000
Bus Bid	1000
Bus Obtain	1100
wait	1110
Request	0111
Release	0011
Load	0001
Idle	0000

3.13.3 Note that the $\overline{\text{REQ}}$ signal is not driven by the bus controller if either EOL or EOP is active. This results in controller cycles which have no excess Wait states, since no $\overline{\text{REQ}}$ causes the bus line $\overline{\text{WAIT}}$ to be pulled low, although some module may be addressed during this cycle. Note that the EOL or EOP signal is synchronized by U12, Pin 5 to prevent generation of a short $\overline{\text{REQ}}$ signal in the event INTSET arrives during a blank-fill bus cycle. Short $\overline{\text{REQ}}$ cycles can cause read-refresh failures in dynamic memories, which then show up as modified memory contents, even though the DMA is incapable of writing. The GVS disable gate U41, (Pins 11, 12 and 13) serves the same general purpose, namely prevention of modification of the address register during a bus cycle. This problem is difficult to diagnose.

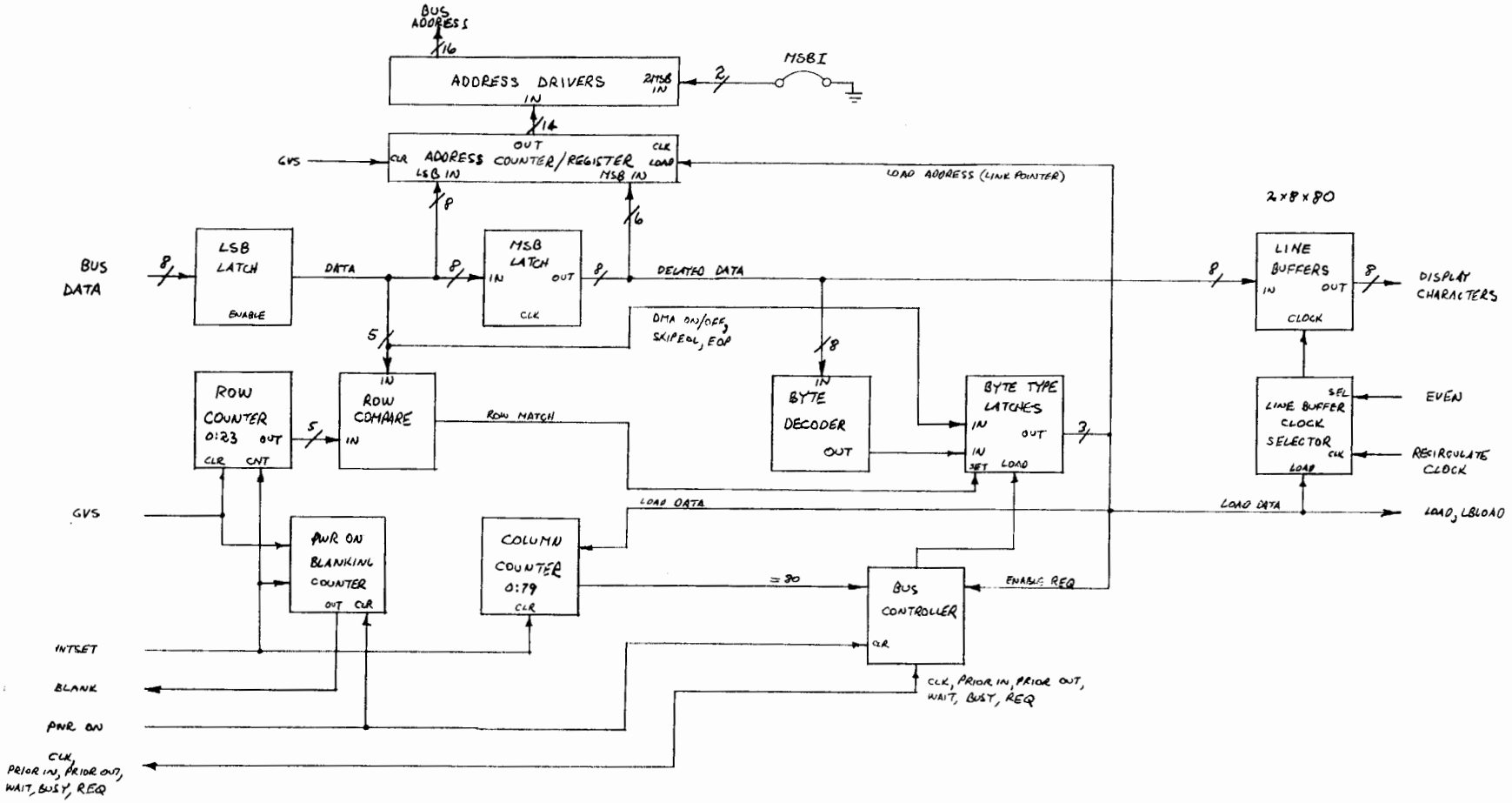


Figure 1
Extended DMA Block Diagram
AUG-01-76 13255-91124

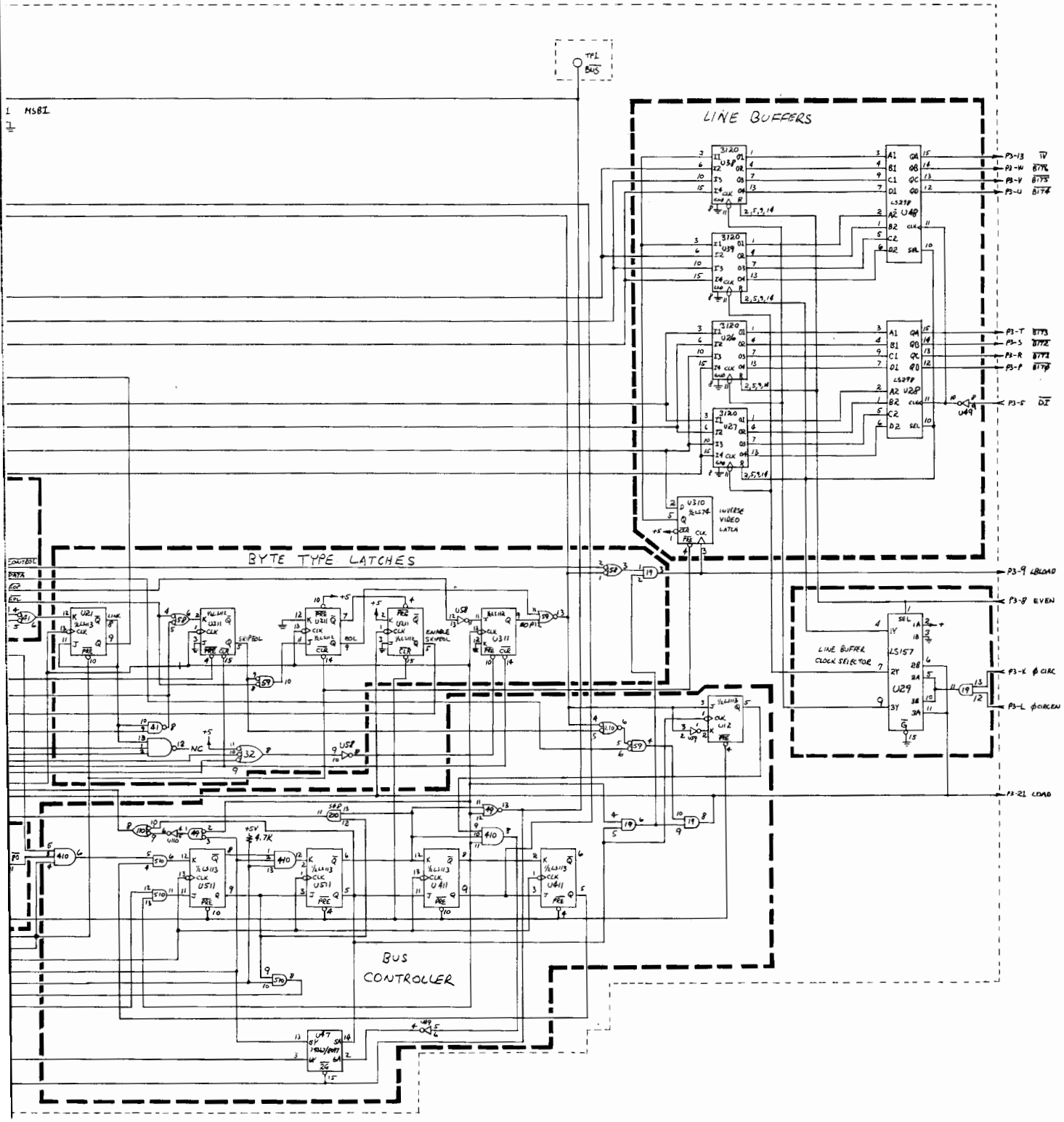
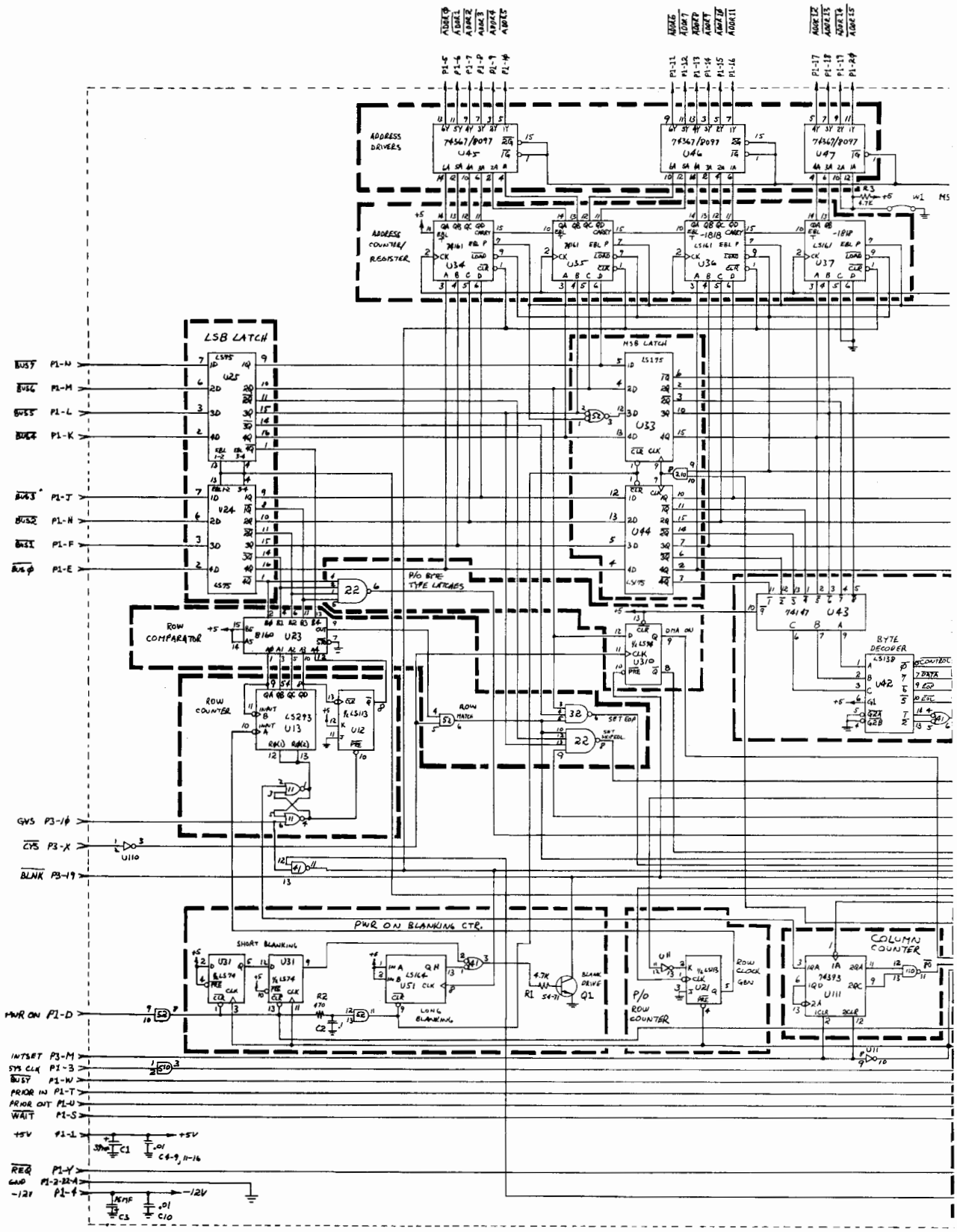
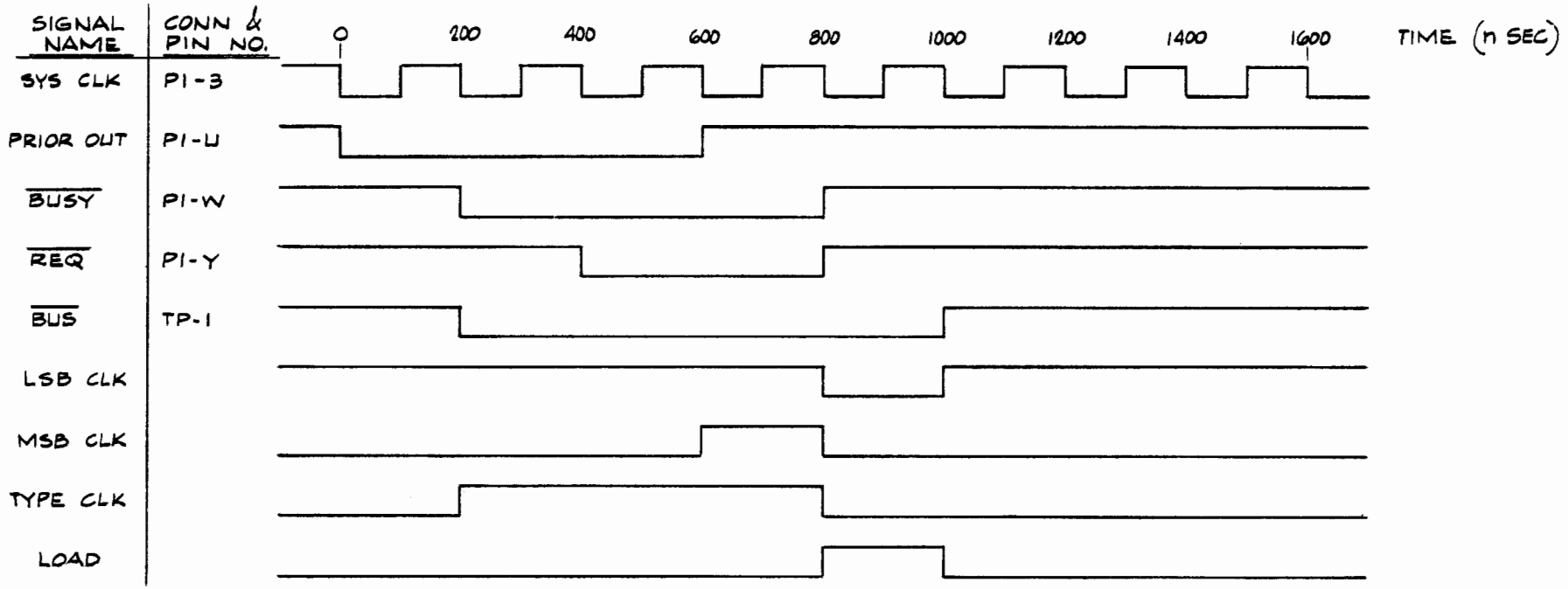


Figure 2
Extended DMA PCA Schematic Diagram
AUG-01-76 **13255-91124**


ADDRESS DRIVERS
ADDRESS COUNTER/ REGISTER
LSB LATCH
MSB LATCH
P/O BYTE TYPE LATCHES
ROW COMPARATOR
ROW COUNTER
BYTE DECODER
PWR ON BLANKING CTR.
SHORT BLANKING
LONG BLANKING
BLANK DRIVE Q1
ROW CLOCK GEN
P/O ROW COUNTER
COLUMN COUNTER
BUS7 P1-N
BUS6 P1-M
BUS5 P1-L
BUS4 P1-K
BUS3 P1-J
BUS2 P1-H
BUS1 P1-F
BUS0 P1-E
GVS P3-16
CVS P3-X
BLNK P3-19
PWR ON P1-D
INTSRT P3-M
SYS CLK P1-3
BUSY P1-W
PRIOR IN P1-T
PRIOR OUT P1-U
WAIT P1-S
+5V P1-L
REQ P1-Y
GND P1-2-22-A
-12V P1-f



NOTES:

1. THIS DIAGRAM DETAILS THE TIMING RELATIONSHIPS BETWEEN THE BUS CONTROLLER SIGNALS "BUSY", "REQ", "PRIOR OUT", AND THE INTERNAL SIGNALS WHICH LOAD THE LSB LATCH, THE MSB LATCH, THE BYTE TYPE LATCH, AND THE LINE BUFFER TO THE BUS CYCLE REQUEST LATCH.

Figure 3
Extended DMA Timing Diagram
AUG-01-76 13255-91124

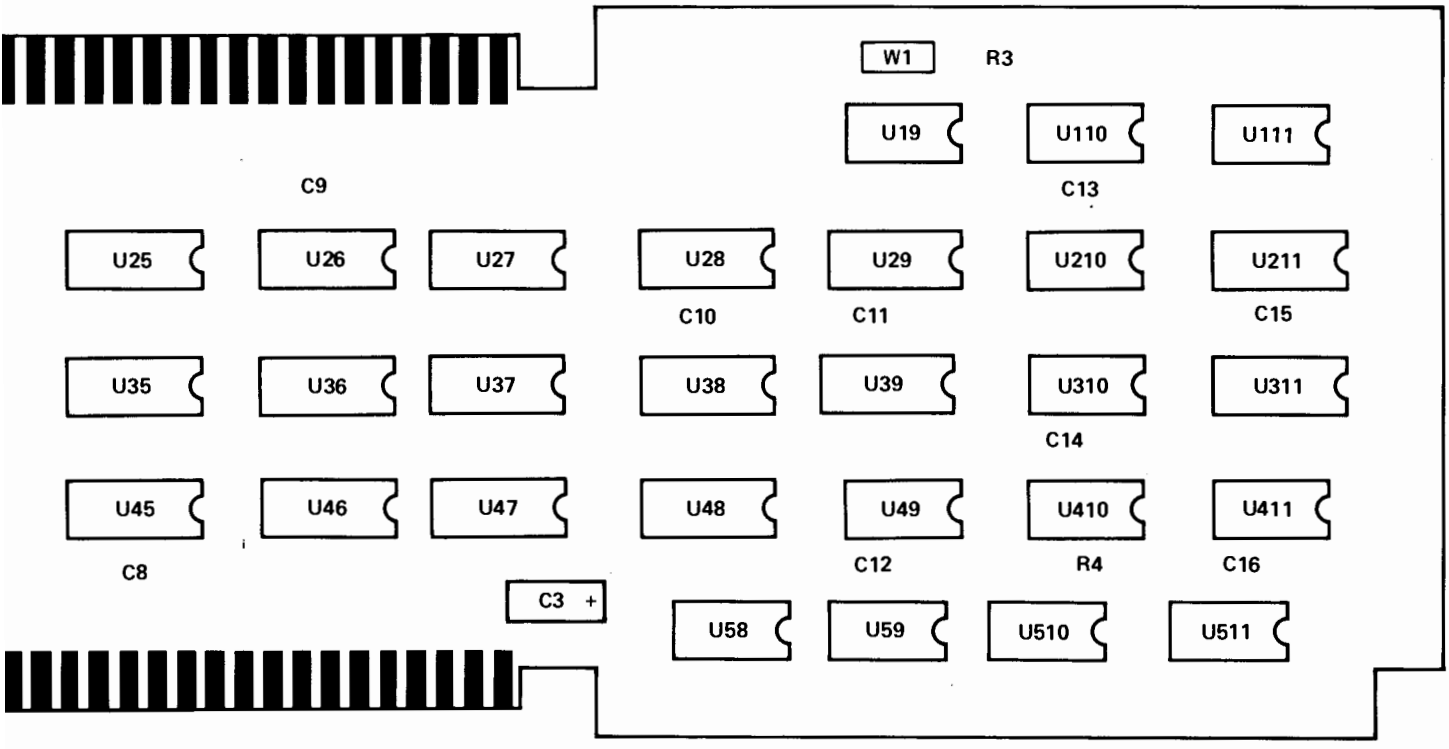
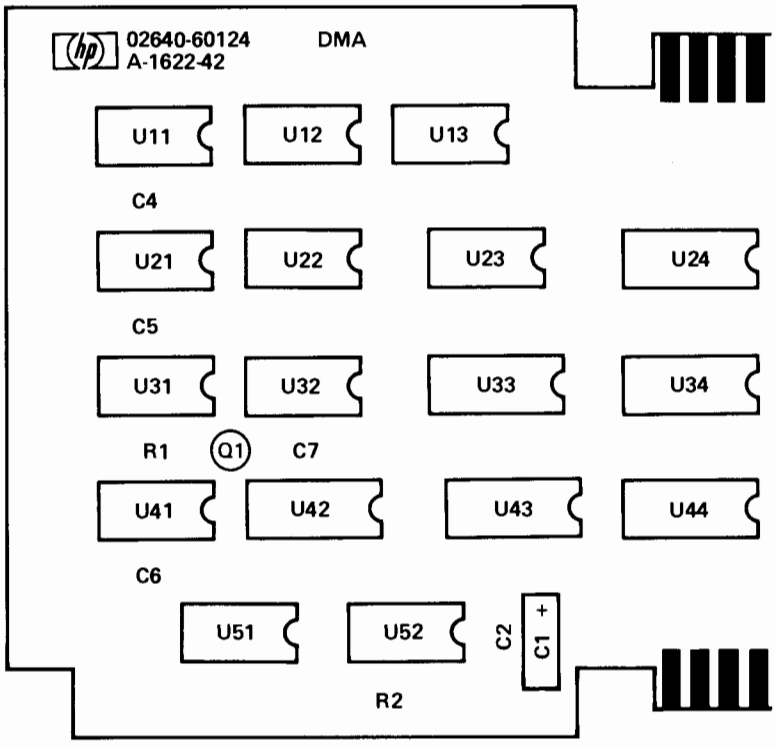


Figure 4
Extended DMA PCA Component Location Diagram
AUG-01-76 13255-91124


02640-60124
A-1622-42
DMA
U11
U12
U13
C4
U21
U22
U23
U24
C5
U31
U32
U33
U34
R1
Q1
C7
U41
U42
U43
U44
C6
U51
U52
C2
C1 +
R2

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60124	1	DMA ASSEMBLY DATE CODE: A-1622-42 REVISION DATE: 09-08-76	28480	02640-60124
C1	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0150-0121	1	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C3	0180-1746	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C4	0160-2055	13	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
E1	0360-0124	2	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
J1	1251-0697	2	CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	22526	75540-001
J2	1251-0697		CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	22526	75540-001
Q1	1854-0071	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
R1	0683-4725	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R2	0683-4715	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R3	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R4	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
U11	1820-1144	3	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U12	1820-1213	4	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U13	1820-1443	1	IC-DIGITAL SN74LS293N TTL LS BIN	01295	SN74LS293N
U19	1820-1201	3	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U21	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U22	1820-1204	1	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U23	1820-1131	1	IC-DIGITAL DM8160N TTL	27014	DM8160N
U24	1820-1411	2	IC-DIGITAL SN74LS75N TTL LS D-TYPE	01295	SN74LS75N
U25	1820-1411		IC-DIGITAL SN74LS75N TTL LS D-TYPE	01295	SN74LS75N
U26	1820-1346	4	IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U27	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U28	1820-1444	2	IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
U29	1820-1470	1	IC-DIGITAL SN74LS157N TTL LS QUAD 2	01295	SN74LS157N
U31	1820-1112	2	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U32	1820-1202	1	IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
U33	1820-1195	2	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U34	1820-0716	2	IC-DIGITAL SN74161N TTL BIN SYNCHRO	01295	SN74161N
U35	1820-0716		IC-DIGITAL SN74161N TTL BIN SYNCHRO	01295	SN74161N
U36	1820-1818	2	IC, DIGITAL 74LS161	28480	1820-1818
U37	1820-1818		IC, DIGITAL 74LS161	28480	1820-1818
U38	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U39	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U41	1820-1197	3	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U42	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U43	1820-1082	1	IC-DIGITAL SN74147N TTL 10	01295	SN74147N
U44	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U45	1820-1049	3	IC-DIGITAL DM8097N TTL HEX 1 NON-INV	27014	DM8097N
U46	1820-1049		IC-DIGITAL DM8097N TTL HEX 1 NON-INV	27014	DM8097N
U47	1820-1049		IC-DIGITAL DM8097N TTL HEX 1 NON-INV	27014	DM8097N
U48	1820-1444		IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
U49	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U51	1820-1433	1	IC-DIGITAL SN74LS164N TTL LS R-S	01295	SN74LS164N
U52	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U56	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U59	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U110	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U111	1820-1464	1	IC-DIGITAL SN74393N TTL DUAL BIN	01295	SN74393N
U210	1820-1367	1	IC-DIGITAL SN74S08N TTL S QUAD 2 AND	01295	SN74S08N
U211	1820-1212	2	IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
U310	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U311	1820-1212		IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
U410	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U411	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U510	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U511	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
W1	1258-0124	1	PIN-PROGRAMMING JUMPER;.30 CONTACT		