HP 13255

DISPLAY EXPANSION MODULE

Manual Part No. 13255-91024

REVISED

FEB-14-80

NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

The Display Expansion Module provides three additional display enhancements to the display subsystem: underline, half-bright, and blinking fields. It also adds the capability for supporting up to three alternate 128-character sets of either the alphanumeric or microvector type. All timing and control signals for the module are received from the Display Controller Module.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Display Expansion Module is contained in tables 1.0 through 6.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60022	Top Plane Connector Ass'y	N/A	N/A
02640-60024	Display Enhancement PCA	12.9 x 4.0 x 0.5	0.44

Number of Backplane Slots Required: 1

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Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.094 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 440 mA	@ mA	@ 22 mA	@ mA
	NOT APPLICABLE		NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 21.06 MHz

Table 4.0 Jumper Definitions

PCA Designation			Function	
			Closed	Open
1A	2A	3A	For ROMs having or type enables (Alphanumeric Sets)	For ROMs having and type enables Microvector Sets,Proms
1B	2B	3B	For Alphanumeric Sets (Enables Half-Shift)	For Microvector Sets (Disables Half-Shift)
1C	2C	3C	For 128 Character Sets (Two ROMs installed)	For 64 Character Sets (One ROM installed)
1D	2D	3D	For Alphanumeric or 9-Bit Microvector Sets	For 8-Bit Microvector Sets
1E*	2E*	3E*	Upper case & lower case treated as 8-Bit Microvector Set	Lower case treated as 8-Bit Microvector Set, Upper case treated as 9-Bit Microvector Set (Allows use of 8-Bit Set in upper case with one Blank column)

Set 1	Set 2	Set 3	Set Affected

*Switch E is only active for 128 Character 8-Bit Microvector Sets, and is a "Don't Care" Otherwise.

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2		Not Used
-3		Not Used
-4	-12V	-12 Volt Power Supply
P1, Pin 5 through Pin 22		Not Used
P1, Pin A	GND	Ground Common Return (Power and Supply)
-B		Not Used
-C		Not Used
-D	PWR ON	System Power On
-E	$\overline{BUS0}$	Negative True, Data Bus Bit 0
-F		Not Used
-H	$\overline{BUS2}$	Negative True, Data Bus Bit 2
-J	$\overline{BUS3}$	Negative True, Data Bus Bit 3
-K	$\overline{BUS4}$	Negative True, Data Bus Bit 4
-L	$\overline{BUS5}$	Negative True, Data Bus Bit 5
P1, Pin M through Pin S		Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
P1, Pin V through Pin Z		Not Used

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	GND	Ground
-2	LC0	Scan Line Counter Bit 0
-3	LC2	Scan Line Counter Bit 2
-4	BIT0	ASCII Bit 0
-5	BIT4	ASCII Bit 4
-6	BIT2	ASCII Bit 2
-7	BIT5	ASCII Bit 5
-8	$\overline{BSS1}$	Negative True, Buffered Set Select Bit 1
-9		Not Used
-10		
-11	$\overline{DBIT1}$	Negative True, Dot 1 Output
-12	$\overline{DBIT3}$	Negative True, Dot 3 Output
-13	$\overline{DBIT5}$	Negative True, Dot 5 Output
-14	$\overline{DBIT7}$	Negative True, Dot 7 Output
-15	GND	Ground

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	GND	Ground
-B	LC1	Scan Line Counter Bit 1
-C	LC3	Scan Line Counter Bit 3
-D	BIT6	ASCII Bit 6
-E	BIT3	ASCII Bit 3
-F	BIT1	ASCII Bit 1
-H	$\overline{\text{BSS0}}$	Negative True, Buffered Set Select Bit 0
-J		Not Used
-K		
-L	$\overline{\text{DBIT0}}$	Negative True, Dot 0 Output
-M	$\overline{\text{DBIT2}}$	Negative True, Dot 2 Output
-N	$\overline{\text{DBIT4}}$	Negative True, Dot 4 Output
-P	$\overline{\text{DBIT6}}$	Negative True, Dot 6 Output
-R	$\overline{\text{DBIT8}}$	Negative True, Dot 8 Output
-S	GND	Ground

5.2 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	$\overline{D0}$	Negative True, Character Dot Position 0
-2		Not Used
-3	$\overline{103}$	Negative True, Column Count 103
-4	BUFCLK	Enhancement Buffer Clock
-5	$\overline{D1}$	Negative True, Character Dot Position 1
-6		Not
-7		Used
-8	EVEN	Even Row
-9	LBLOAD	Bus Buffer Load
-10		Not
-11		Used
-12	$\overline{BBL}$	Negative True, Buffered Blink
-13		Not Used
-14	$\overline{BUL}$	Negative True, Buffered Underline
-15	$\overline{BUF\ HLF\ BRT}$	Negative True, Buffered Half-Bright
-16	$\overline{BSS0}$	Negative True, Buffered Set Select Bit 0
-17	$\overline{BSS1}$	Negative True, Buffered Set Select Bit 1
-18	$\overline{81}$	Negative True, Column Count 81
-19		Not
-20		Used
-21	LOAD	Line Buffer Load
-22	$\overline{XBITS1}$	Negative True, External Bit Stream 1

Table 5.2 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	DSPY CLK	21.060 MHz Display Clock
-B	GND	Ground
-C		Not Used
-D	$\overline{D8}$	Negative True, Character Dot Position 8
-E	$\overline{14}$	Negative True, Scan Line Counter Reset
-F		Not Used
-H	VRTCLK	Scan Line Counter Clock
-J		Not Used
-K	OCIRC	Line Buffer Circulation
-L	OCIRCEN	Line Buffer Circulation Enable
-M	INTSET	Display Controller Interrupt
-N		Not Used
-P	$\overline{BIT0}$	Negative True, ASCII Bit 0
-R	$\overline{BIT1}$	Negative True, ASCII Bit 1
-S	$\overline{BIT2}$	Negative True, ASCII Bit 2
-T	$\overline{BIT3}$	Negative True, ASCII Bit 3
-U	$\overline{BIT4}$	Negative True, ASCII Bit 4
-V	$\overline{BIT5}$	Negative True, ASCII Bit 5
-W	$\overline{BIT6}$	Negative True, ASCII Bit 6
-X		Not Used
-Y	GND	Ground
-Z		Not Used

Table 6.0 Module Bus Pin Assignments

Function Performed: Put Data Bits B0, B2, B3, B4, and B5 Into Holding Register

Poll Bit: Not Applicable

Module Address: Not Applicable

Function Specifier: Not Applicable

Data Bus Bit Interpretation: The data bits (B0, B2, B3, B4, and B5) are loaded under DMA control.

B7: Not Used

B6: Not Used

B5: Holds the Set Select Bit 1

B4: Holds the Set Select Bit 0

B3: Holds the Half-Bright Feature

B2: Holds the Underline Feature

B1: Not Used

B0: Holds the Blink Feature

Value	Bus Signal
N/A	ADDR 15
N/A	ADDR 14
N/A	ADDR 13
N/A	ADDR 12
N/A	ADDR 11
N/A	ADDR 10
N/A	ADDR 9
N/A	ADDR 8
N/A	ADDR 7
N/A	ADDR 6
N/A	ADDR 5
N/A	ADDR 4
N/A	ADDR 3
N/A	ADDR 2
N/A	ADDR 1
N/A	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts lists (02640-60022 and 02640-60024) located in the appendix.

The Display Expansion Module provides the additional display control word width and thus supports the three additional display features and the two set select bits. The module receives all of its timing and control information from the Display Controller Module and is slaved to it. The Display Expansion Module functions as an adjunct to the minimum display subsystem. The module's output consists of an external bit stream ($\overline{XBITS1}$) display enhancement control lines $\overline{BUL}$, $\overline{BUF\ HLF\ BRT}$, and $\overline{BBL}$, and the two set select lines $\overline{BSS0}$ and $\overline{BSS1}$. Electrically, its line buffers operate in parallel with those on the Display Memory Access (DMA) PCA.

3.1 REFRESH AND LOAD LOGIC.

3.1.1 The refresh and load logic drives the clock and control lines of the line buffers. In addition, the logic toggles the line buffers and sends to each one the appropriate clock signals and recirculate commands.

3.1.2 The refresh and load logic controls the line buffers and the dual two-line-to-one-line multiplexer. Its input signals are the circulation clock for the line buffers (the logical AND of 0CIRC and 0CIRCEN) and the LOAD signal from the Display Memory Access PCA. 0CIRC is a continuous circulation signal gated into bursts of 80 pulses by 0CIREN. The EVEN signal controls the multiplexer. When it is high, the DMA controls the clock lines of line buffers U51 and U52. Simultaneously, the display controller circulates the previously loaded information in line buffers U41 and U42 fifteen times, via the 0CIRC signal. At the end of the fifteenth scan line of the row, EVEN changes state, the INTSET signal clears the holding register, and the roles of the pairs of line buffers are reversed.

3.2 HOLDING REGISTER.

3.2.1 The holding register (U43 and U44) is a 5-bit register which stores the display enhancement and set select bits received from the data bus.

3.2.2 Information in the holding register is strobed in by means of LBLOAD under controls of the DMA PCA. The information is buffered and subsequently available for entry into the off-screen line buffer (as determined by the EVEN signal). At the end of a row (end of the fifteenth scan line), INTSET clears out the holding register before a new row is started by the DMA PCA.

3.3 LINE BUFFERS.

3.3.1 The line buffer block consists of two pairs of shift registers (U41, U42, and U51, U52) which hold the underline, half-bright, and blinking enhancement bits along with the two set select bits. They are toggled by the Display Control PCA, each one alternately being loaded by the DMA PCA from the terminal data bus and then cycled 15 times for display on the CRT.

3.3.2 The two line buffers are each 5 bits by 80 bits in length. They operate in parallel with the line buffers on the DMA PCA and, therefore, expand the display control word width by five bits. The line buffers are toggled by the EVEN signal. While one line buffer is being recirculated fifteen times by OCIRC, the other is being loaded by the DMA PCA via LOAD. The outputs of the line buffers are routed to U31 and U32 which act as a five channel two-line-to-one-line multiplexer with latching outputs. The circulated line buffer is selected by EVEN and is loaded into the latch during character dot position 1 ($\overline{D1}$). The output of the latch then consists of the three display enhancement signals, HBEN, ULEN, BLEN and the two buffered set select bits, $\overline{BSS0}$ and $\overline{BSS1}$. The signals appear character synchronously with the corresponding ASCII from the DMA PCA.

3.4 64/128 CHARACTER SET.

3.4.1 Two 1024-word by 8-bit bipolar ROMs comprise one 128-character alphanumeric type character set. The 128-character microvector sets utilize two 1024-word by 9-bit ROMs or two 1024-word by 8-Bit ROMS which emulate the 9-Bit devices by copying one bit. The position of switch D determines the type of ROM used.

3.4.2 Each 64-character alphanumeric character set is encoded into a 1024 word by 8-bit bipolar ROM. A 128-character set requires two ROMs. In the case of microvector type character sets, each 64-character set is encoded in a 1024-word by 9-bit ROM or a 1024-word by 8-Bit ROM emulating a 9-Bit Device by Duplicating the First Bit. (DBit0) Both types of ROMs have identical pinouts. The 8-Bit ROMs have an additional CHIP ENABLE pin which corresponds to an output line on the 9-Bit ROMs.

3.5 CHARACTER SET DECODER.

3.5.1 The character set decoder selects the two buffered set select bits, $\overline{BSS0}$ and $\overline{BSS1}$, to enable the three alternate character sets.

3.5.2 The character set decoder selects $\overline{BSS0}$ as the LSB and $\overline{BSS1}$ as the MSB. The three output lines of U38 are negative true. As a character set is enabled, the corresponding ROM sockets are enabled via the $\overline{E1}$ signal at U110, U310, U510, U19, U39, and U59, Pins 21. If the base set (SET0) is utilized, then $\overline{BSS0}$ and $\overline{BSS1}$ are both high and the character ROMs on the Display Control PCA are enabled.

3.6 CHARACTER SET ENCODER.

3.6.1 The character set encoder's output signals reflect the state of the Set-Type Switches (B,C,D,E) of the alternate character set being currently addressed by buffered set select bits $\overline{BSS0}$ and $\overline{BSS1}$.

3.6.2 The $\overline{HALFSHIFTEN(ABLE)}$(U48,Pin7) Signal controls the shifter logic. When the selected set is of the alphanumeric type, DBIT0 functions as the half-shift control bit. When the selected set is of the microvector type, then $\overline{DBIT0}$ and $\overline{DBIT8}$ are mapped into dot position 0 and 8 respectively.

The $\overline{ZERO\ COPYEN(ABLE)}$(U48,Pin 9) Signal also acts as a control for the Shifter Logic. This line is active if the currently accessed set is of the 8-Bit Microvector type (Switches B and D Open) and fits one of the following categories. A 64 Character Set (Switch C Open); A 128 Character Set (Switch C Closed) with a lower case character being selected; A 128 Character Set with the Copy-All option selected (Switch E Closed) upper or lower case accessed.

If these conditions are met, $\overline{\text{DBIT0}}$ is mapped into dot positions 0 and 1, effectively copying it, while the other seven bits are delayed one dot time and output during dot positions 2 through 8. (The Character ROMs are encoded with this in mind so the Characters do not appear shifted one position.)

3.7 UPPER/LOWER CASE SELECT LOGIC

3.7.1 The character select logic is set up by means of Switch D (each alternate character set to be either 64- or 128-characters in length). It also enables the appropriate upper case or lower case character ROM depending on the ASCII code from the DMA PCA being processed.

3.7.2 This logic selects which ROM of the selected set will be enabled. When BIT5 and BIT6 of the incoming ASCII are both high or both low, then the characters correspond to the control codes (00-37B) or lower case characters (140-177B) respectively. Otherwise, they are upper case characters (40-137B).

When the character select Switch (D) is closed (128 characters), then the corresponding upper case ROM is enabled when $\overline{\text{BIT5}}$ and $\overline{\overline{\text{BIT6}}}$ are the same. When the character select switch is open (64 characters), then the upper case ROM is disabled only when both $\overline{\text{BIT5}}$ and $\overline{\overline{\text{BIT6}}}$ are high. This causes lower case codes to be upshifted to their respective upper case characters and control codes to display nothing.

3.8 SCAN LINE COUNTER.

3.8.1 The scan line counter is a local modulo 15 counter synchronized to the scan line counter on the Display Control PCA. It provides a local source of the four scan line count bits required by the character ROMs.

3.8.2 The scan line counter (U46) is a 4-bit synchronous counter driven by VRTCLK from the Display Control PCA logic. Every 15 lines, it is reset by $\overline{\overline{14}}$. This forces the counter to sequence from a count of 0 to 14. The four output lines of the counter form the four least significant bits of the ROM address, the six most significant bits being the incoming ASCII codes.

3.9 SHIFTER LOGIC.

3.9.1 The shifter Logic block controls the Timing of Data Bit output, it generates the Shift Clock signal applied to the parallel-to-serial converter. The signal is HALFSHIFTED, Dependent on $\overline{DBIT0}$, if the accessed character Set is of the alphanumeric type and the HALFSHIFT enable from the Character Set encoder is active. If the set is of the 9-Bit Microvector type, the shifter Logic accepts $\overline{DBIT8}$ and inserts it into the serial bit stream along with $\overline{DBIT0}$. If an 8-Bit Microvector Set is present, $\overline{DBIT0}$ is output twice, and the remaining seven bits follow.

3.9.2 The shifter logic generates the SHIFT (U23, Pin 8) signal which clocks the parallel-to-serial converter. The logic is controlled by both $\overline{DBIT0}$ and the $\overline{SHIFT\ ENABLE}$ signal. When the selected character set is of the alphanumeric type, $\overline{SHIFT\ ENABLE}$ and SHIFT ENABLE at U26, Pin 8 allow the half-shift control bit ($\overline{DBIT0}$ of Alphanumeric ROMs) to allow $\overline{DBIT0}$ into U22, Pin 2. When the selected character set is of the microvector type, then $\overline{DBIT0}$ is interpreted as a data bit and output, once for a 9-Bit set and twice for an 8-Bit set. If output twice, the other seven bits are delayed to allow this by inhibiting the parallel to serial convertor for one bit time (D0 Time). $\overline{DBIT8}$ is output as a Data Bit also for 9-Bit Microvector Sets and $\overline{DBIT7}$ is routed through its path for 8-Bit Microvector Sets.

Shift pulses can occur on either the leading edge of the display clock (HALF-SHIFTED) or on the trailing edge (not HALF-SHIFTED), depending on the state of $\overline{DBIT0}$. A shift pulse always occurs during dot position 8 time to parallel load the data from the character roms into the parallel-to-serial converter.

3.10 PARALLEL-TO-SERIAL CONVERTER.

3.10.1 The parallel-to-serial converter is loaded with the ROM output word and receives a Shift Clock (SHIFT) signal from U23, Pin 8. The parallel data is serially shifted out; is merged with $\overline{DBIT8}$ and $\overline{DBIT0}$; and becomes the external serial bit stream, $\overline{XBITS1}$.

3.10.2 The parallel-to-serial converter consists of U58 (which handles bits 1 through 7) and U36 (which merges those seven bits with $\overline{DBIT0}$ and $\overline{DBIT8}$). During dot position 8 time, the Load line of U58 at Pin 15 is kept low and the shift clock causes the present ROM Data to be loaded in. The rest of the time, the data is being shifted out serially to U36. If the selected character set is of the 9 Bit Microvector type, $\overline{DBIT0}$ and Buffered $\overline{DBIT8}$ are merged with the output of U58 to form the serial bit stream, $\overline{XBITS1}$. If the set is 8-Bit Microvector, the Serial Data is delayed one Bit position while DBIT6 is output twice. This is done by inhibiting the clock with the $\overline{D0}$ signal. This serial signal, in turn, is sent to the Display Control PCA via the P3 connector where it is merged with th minimum system bit stream.

3.11 ENHANCEMENT GENERATOR.

3.11.1 The enhancement generator is a 3-bit register which receives the display enhancement signals from the line buffers; holds them for one character time; and outputs them to the Display Control PCA. A field position alignment one-shot allows the half-bright display feature to be positioned exactly over the character to which it is applied, thus compensating for accumulated delays in the video generator.

3.11.2 The three latches in the enhancement generator receive the enhancement signals from the line buffers and hold them during the read access cycle of the character ROMs. The underline and blinking latches are directly loaded by BUFCLK while the half-bright latch is clocked by one-shot U13. The FIELD alignment potentiometer is used to compensate the half-bright signal against the accumulated delays incurred by the video signal.

3.12 ROM TYPE

3.12.1 The ROM type select switch (A) allows the use of ROMS or PROMS with two types of enable arrangements, allowing greater flexibility.

3.12.2 Two enable arrangements are currently being used, in the 'And Arrangement', the enables are anded internally: $\overline{E1}$. $\overline{E2}$. E3. E4. in the 'Or Arrangement', the enables are internally arranged as: ($\overline{E1}$. $\overline{E2}$) + (E3.E4). Therefore, E3 must be high for the 'And Arrangement' and low for the 'Or Arrangement' for proper operation.

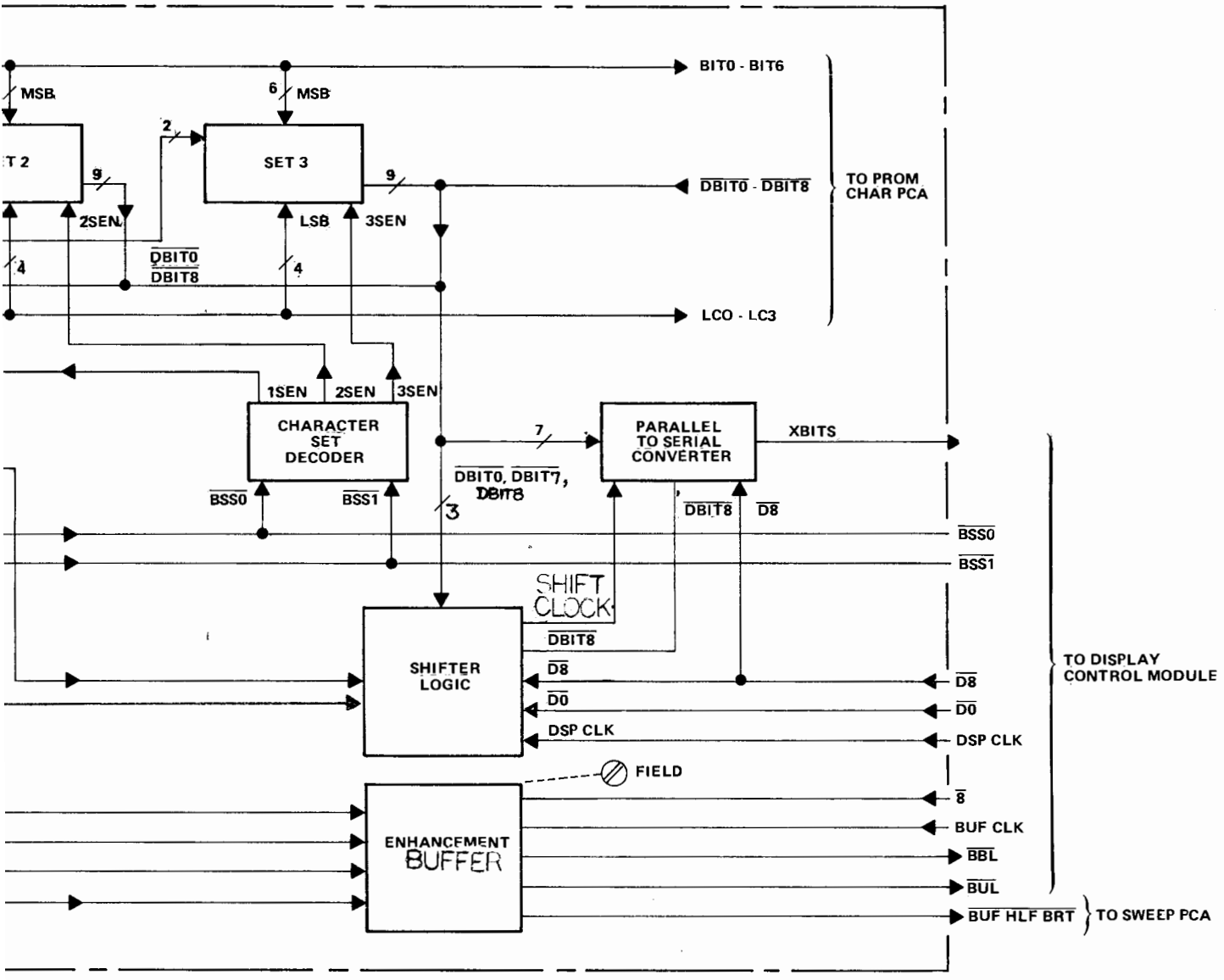
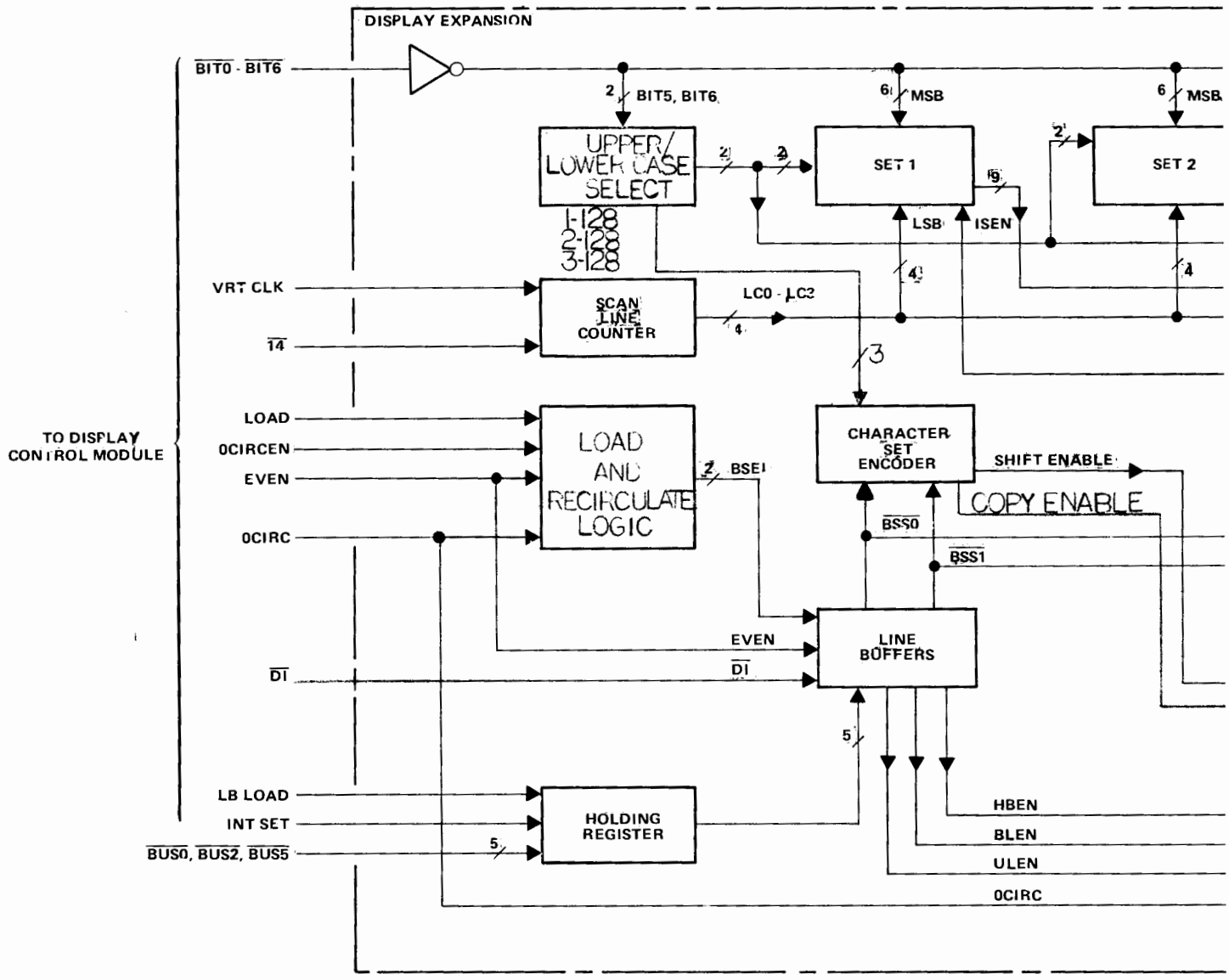


Figure 1
Display Expansion Module Block Diagram
FEB-14-80 13255-91024


DISPLAY EXPANSION
TO DISPLAY CONTROL MODULE
BIT0 - BIT6
2 BIT5, BIT6
6 MSB
6 MSB
UPPER/ LOWER CASE SELECT
1-128
2-128
3-128
SET 1
SET 2
LSB
ISEN
VRT CLK
14
SCAN LINE COUNTER
LC0 - LC3
LOAD
0CIRCEN
EVEN
0CIRC
LOAD AND RECIRCULATE LOGIC
BSEL
CHARACTER SET ENCODER
SHIFT ENABLE
COPY ENABLE
BSS0
BSS1
EVEN
DI
LINE BUFFERS
LB LOAD
INT SET
BUS0, BUS2, BUS5
HOLDING REGISTER
HBEN
BLEN
ULEN
0CIRC

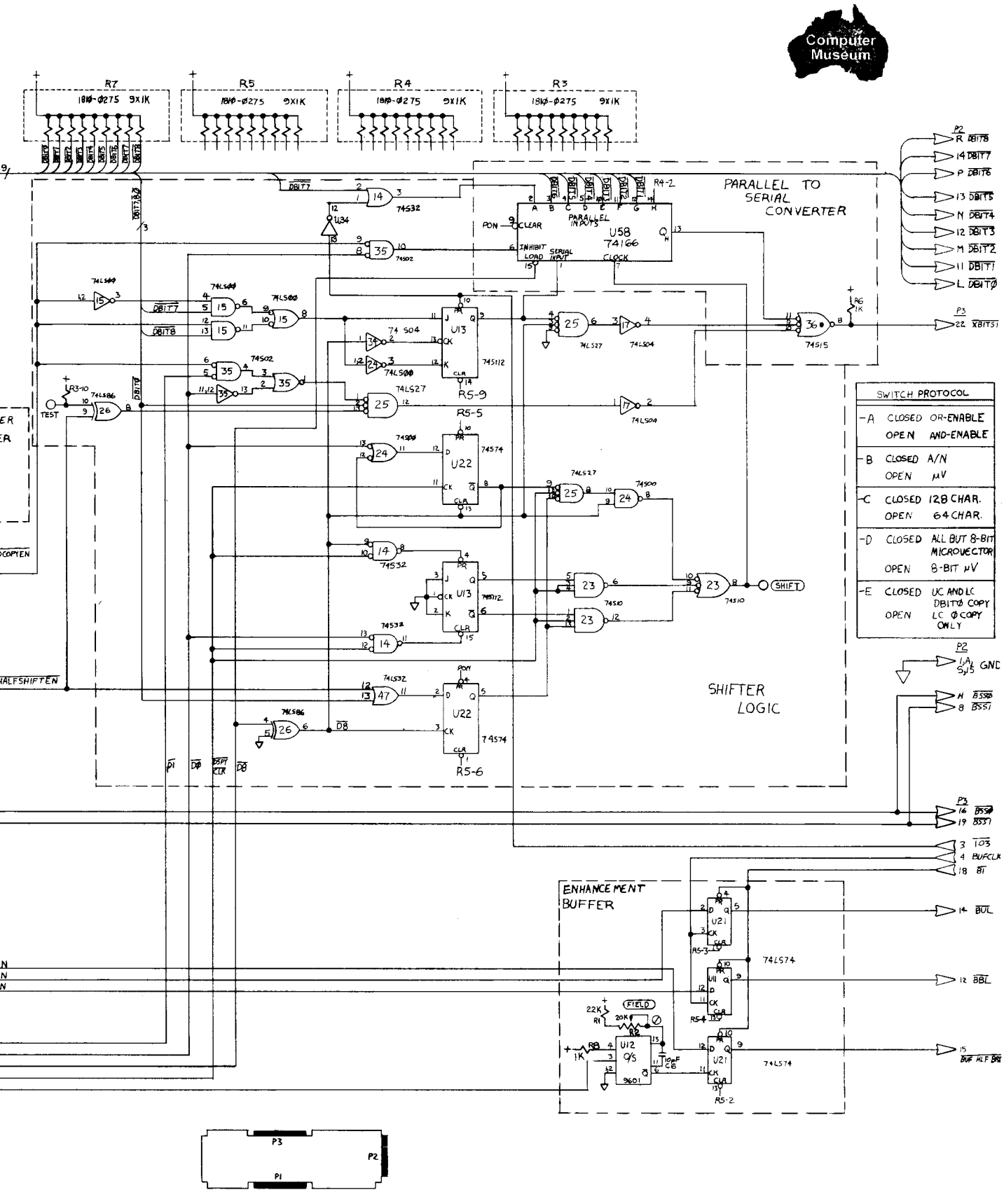
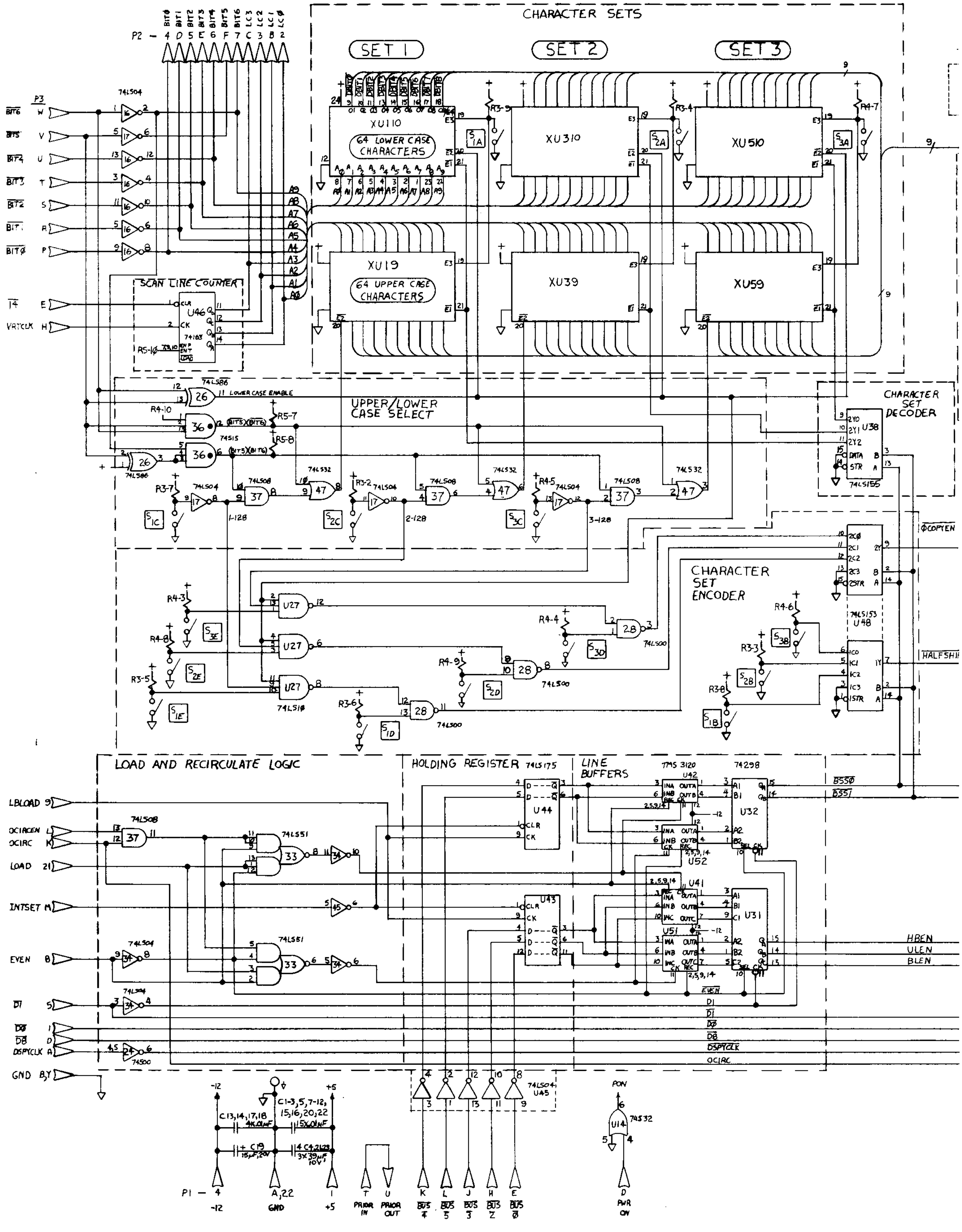


Figure 2
Display Enhancement PCA Schematic Diagram
FEB-14-80 13255-91024


CHARACTER SETS
SET 1
SET 2
SET 3
XU110
64 LOWER CASE CHARACTERS
XU310
XU510
XU19
64 UPPER CASE CHARACTERS
XU39
XU59
SCAN LINE COUNTER
U46
74163
UPPER/LOWER CASE SELECT
LOWER CASE ENABLE
CHARACTER SET DECODER
U38
74LS155
CHARACTER SET ENCODER
74LS153
U48
LOAD AND RECIRCULATE LOGIC
HOLDING REGISTER 74LS175
U44
U43
LINE BUFFERS
TMS 3120
U42
U52
U41
U51
74298
U32
U31
LBLOAD
OCIRCEN
OCIRC
LOAD
INTSET
EVEN
DSPYCLK
GND
HBEN
ULEN
BLEN
ΦCOPYEN
HALFSHIFT
BSSØ
BSS1
P1
P2
P3
-12
GND
+5
PRIOR IN
PRIOR OUT
BUS 4
BUS 5
BUS 3
BUS 2
BUS Ø
PWR ON
PON
U14
74S32
74LS04
U45
C13,14,17,18 4X.01μF
C19 15μF,20V
C1-3,5,7-12,15,16,20,22 15X.01μF
C4,21,23 3X39μF 10V

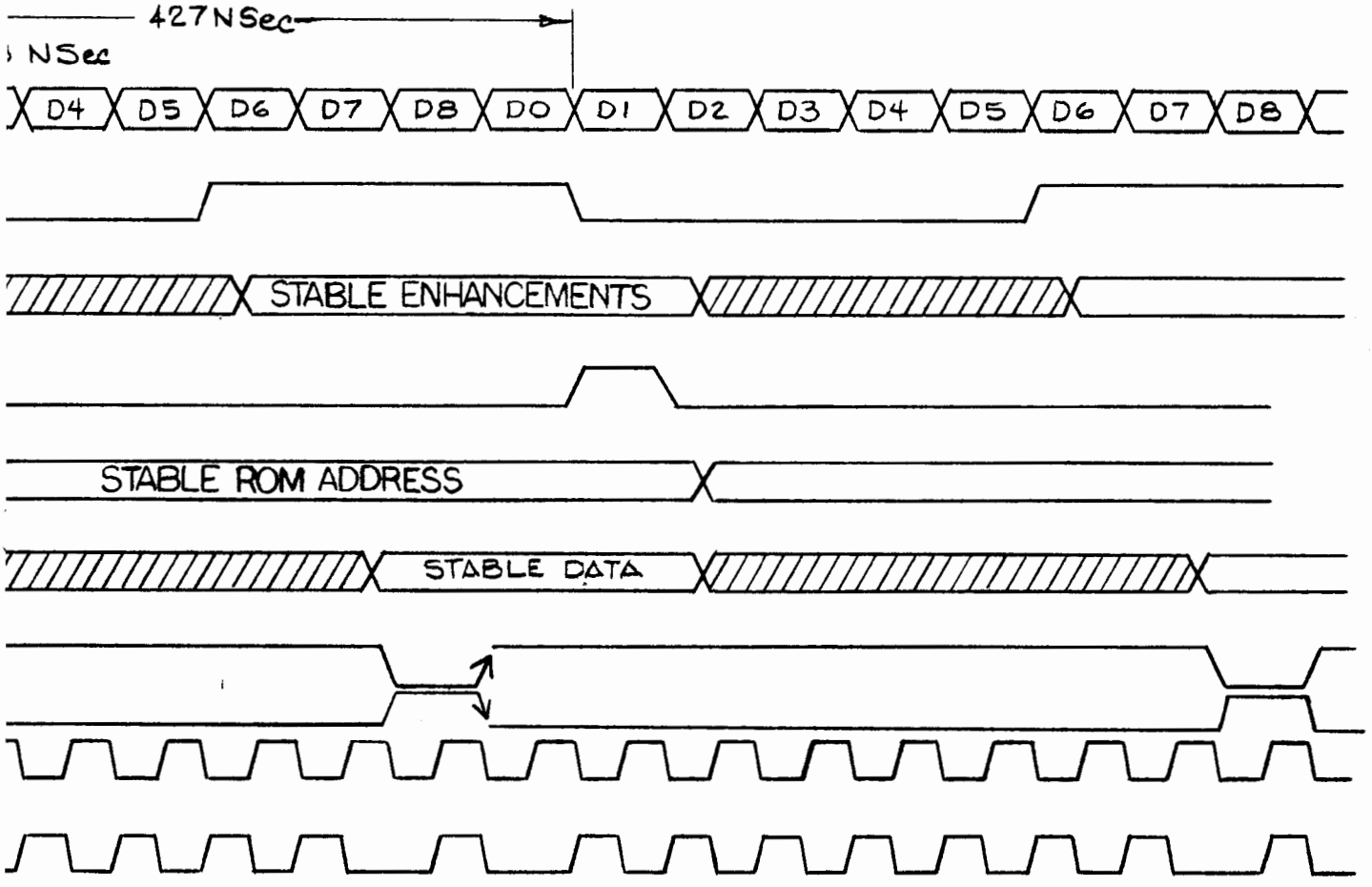
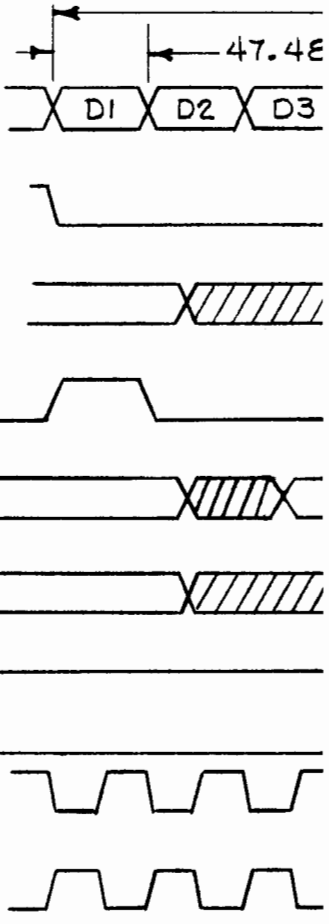


Figure 3
Display Expansion Timing Diagram
FEB-14-80 13255-91024

SIGNAL NAME	CONNECTOR & PIN NUMBER
Ø CIRC	P3, PIN K
(ENHANCEMENTS)	—
(MPXR LATCH)	U34, PIN4
(CHARACTER ROM ADDRESS)	—
(ROM DATA)	—
(D-8 P/S LOAD)	U58, PIN 15
(DBIT8 LOAD)	U13, PIN13
SHFT (WITHOUT HALF-SHIFT)	
SHFT (WITH HALF-SHIFT)	U23, PIN 8



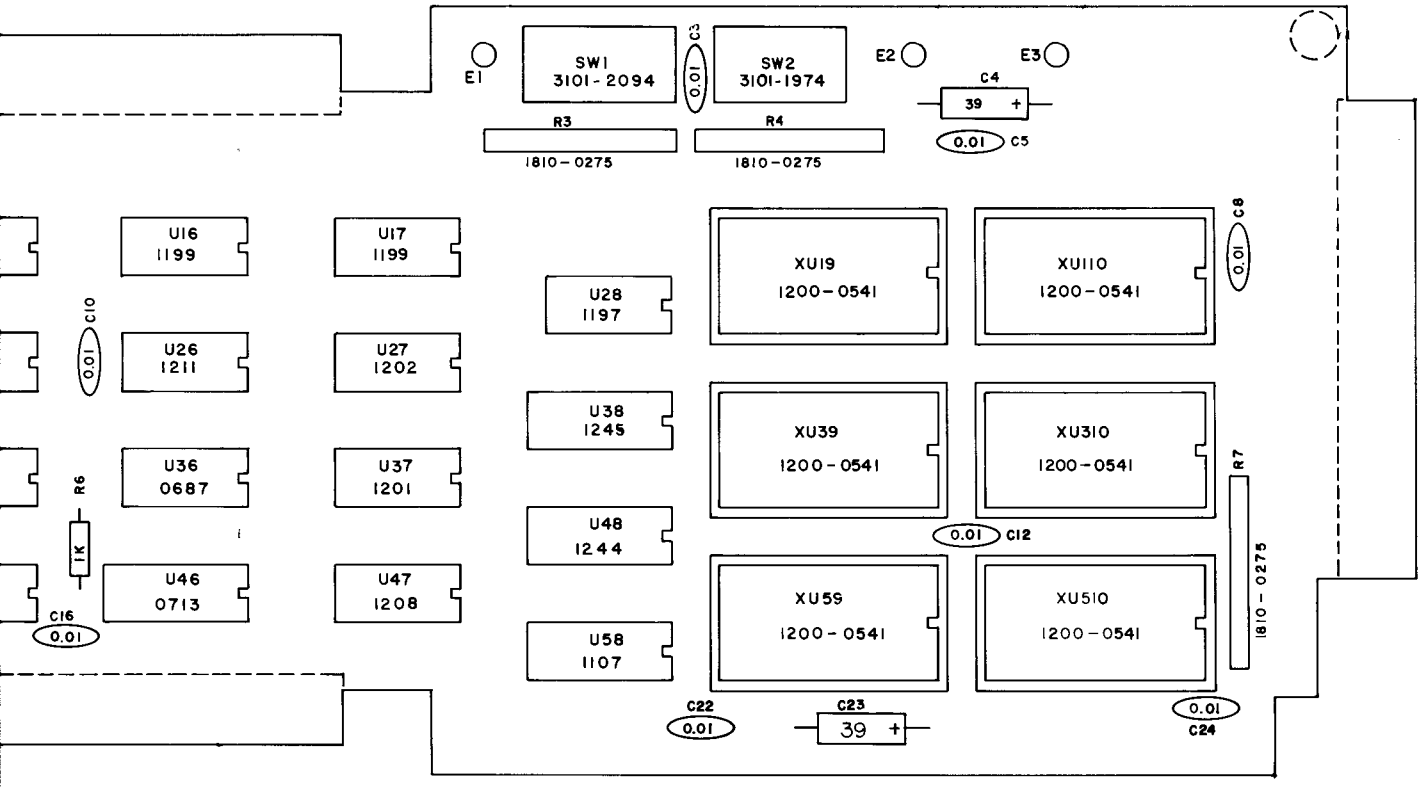
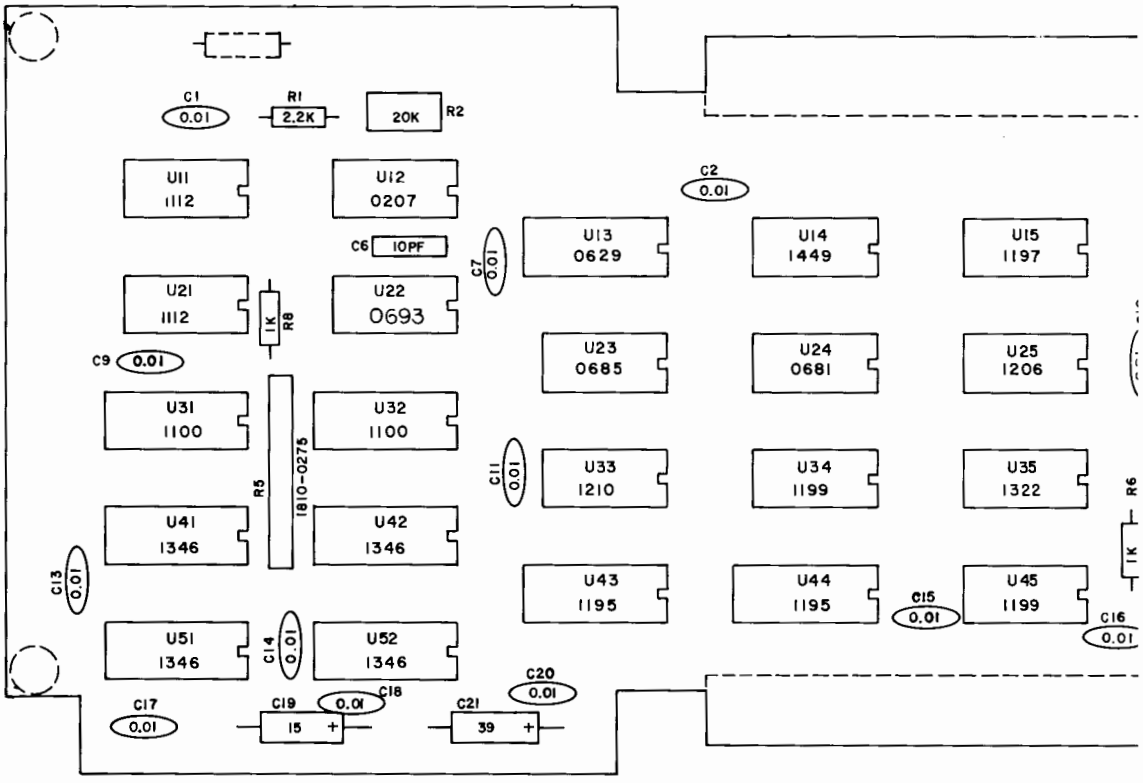


Figure 4
Display Enhancement PCA Component Location Diagram
FEB-14-80 13255-91024


C1
0.01
R1
2.2K
20K
R2
U11
1112
U12
0207
C2
0.01
C6
10PF
C7
0.01
U13
0629
U14
1449
U15
1197
U21
1112
1K
R8
U22
0693
U23
0685
U24
0681
U25
1206
C9
0.01
U31
1100
U32
1100
R5
1810-0275
C11
0.01
U33
1210
U34
1199
U35
1322
R6
1K
U41
1346
U42
1346
C13
0.01
U43
1195
U44
1195
C15
0.01
U45
1199
C16
0.01
U51
1346
C14
0.01
U52
1346
C20
0.01
C17
0.01
C19
0.01
C18
15
+
C21
39
+

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60022	6	4	CONNECTOR ASSEMBLY	28480	02640-60022
	0403-0243	9	4	BUMPER-RUBBER	28480	0403-0243
	1251-5564	5	4	CONNECTOR-EDGE	28480	1251-5564
	02640-60024	8	1	DISPLAY ENHANCEMENTS, PCA	28480	02640-60024
C1	0160-2055	9	19	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0180-0393	6	3	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C6	0160-2257	3	1	CAPACITOR-FXD 10PF +-5% 500VDC CER 0+-60	28480	0160-2257
C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C19	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0180-0393	6		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0180-0393	6		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
E1	0360-0124	3	3	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
E2	0360-0124	3		CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
E3	0360-0124	3		CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
R1	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R2	2100-3353	8	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	28480	2100-3353
R3	1810-0275	1	4	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R4	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R5	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R6	0683-1025	9	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R7	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R8	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
SW1	3101-2094	5	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2094
SW2	3101-1974	8	1	SWITCH-RKR DIP-RKR-ASSY 7-1A .05A 30VDC	28480	3101-1974
U11	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U12	1820-0207	0	1	IC MV TTL MONOSTBL RETRIG/RESET	04713	MC8601P
U13	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U14	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U15	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U16	1820-1199	1	4	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U17	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U21	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U22	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U23	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U24	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U25	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U26	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U27	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U28	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U31	1820-1100	4	2	IC MUXR/DATA-SEL TTL 2-TO-1-LINE QUAD	01295	SN74298N
U32	1820-1100	4		IC MUXR/DATA-SEL TTL 2-TO-1-LINE QUAD	01295	SN74298N
U33	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
U34	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U35	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U36	1820-0687	0	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S15N
U37	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U38	1820-1245	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
U41	1820-1346	0	4	IC SHF-RGTR PMOS SERIAL-IN SERIAL-OUT	01295	TMS3120NC
U42	1820-1346	0		IC SHF-RGTR PMOS SERIAL-IN SERIAL-OUT	01295	TMS3120NC
U43	1820-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U44	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U45	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U46	1820-0713	3	1	IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN74163N
U47	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U48	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U51	1820-1346	0		IC SHF-RGTR PMOS SERIAL-IN SERIAL-OUT	01295	TMS3120NC
U52	1820-1346	0		IC SHF-RGTR PMOS SERIAL-IN SERIAL-OUT	01295	TMS3120NC
U58	1820-1107	1	1	IC SHF-RGTR TTL R-S PRL-IN SERIAL-OUT	01295	SN74166N
XU19	1200-0541	1	6	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU39	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU59	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU110	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU310	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU510	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247