HP 13255

CONTROL MEMORY (AMD) MODULE

Manual Part No. 13255-91192

REVISED

SEP-06-77

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

The Control Memory (AMD) Module provides 256 bytes of RAM and space for 24K bytes of ROM. The module communicates with the processor over a top plane bus. This allows the processor to operate at its maximum rate by eliminating the bus contention and handshake protocol of the bottom plane bus.

The ROMs contain the operating firmware for the terminal. The RAM provides for a fast access scratchpad for stack operations and program variables.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Control Memory (AMD) Module is contained in tables 1.0 through 5.1.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60192	Control Memory PCA	12.5 x 4.0 x 0.5	0.56

Number of Backplane Slots Required: 1

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Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 0.750 (percent per 1000 hours) 2.110 (with 12 ROMs loaded on PCA)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 450 mA	@ 450 mA	@ mA	@ mA
		NOT APPLICABLE	NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: MHz

NOT APPLICABLE

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
ROM DISAB (0,2,4,...,22)	The corresponding 2K block of ROM is enabled.	The corresponding 2K block of ROM is disabled.
+24	This Control Memory ROM board responds to address starting at 0K. The RAM starts at 110400B.	This Control Memory ROM board starts at 24K. The RAM starts at 110000B.
RAM DISAB	The RAM is enabled.	The RAM is disabled.

(Note that when the +24K jumper is out, the ROMs at location 8K and 10K will not be accessable from the CPU. This is because 8-12K (+24K) map into 32-36K which is the I/O space for the 8080A-2 system.)

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
Pin -3 through Pin -22		Not Used
P1, Pin -A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
Pin -D through Pin -S		Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
Pin -V through Pin -Z		Not Used

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	GND	Ground
- 2	ADDR0	Address Bit 0
- 3	ADDR1	Address Bit 1
- 4	ADDR2	Address Bit 2
- 5	ADDR3	Address Bit 3
- 6	ADDR4	Address Bit 4
- 7	ADDR5	Address Bit 5
- 8	ADDR6	Address Bit 6
- 9	ADDR7	Address Bit 7
-10	ADDR8	Address Bit 8
-11	ADDR9	Address Bit 9
-12	ADDR10	Address Bit 10
-13	ADDR11	Address Bit 11
-14	ADDR12	Address Bit 12
-15	ADDR13	Address Bit 13
-16	ADDR14	Address Bit 14
-17	ADDR15	Address Bit 15
-18	$\overline{\text{TOP ACTIVE}}$	Negative True, (Low) Indicates Top Plane Module Address Recognition. (High Causes a Bottom Plane Bus Cycle)
-19	READ	High Indicates Top Plane Bus Data Should Be Gated On
-20	WRITE	High Indicates Top Plane Bus Data is Valid
-21		Not Used
-22	GND	Ground

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	GND	Ground
-B	DBIT0	Data Bit 0
-C	DBIT1	Data Bit 1
-D	DBIT2	Data Bit 2
-E	DBIT3	Data Bit 3
-F	DBIT4	Data Bit 4
-H	DBIT5	Data Bit 5
-J	DBIT6	Data Bit 6
-K	DBIT7	Data Bit 7
Pin -L through Pin -N		Not Used
-P	$\overline{I/O}$	Negative True, (Low) Indicates (A15 A14 A13 A12) = (1000)
Pin -R through Pin -S		Not Used
-T	WO	High Indicates Write or Output Cycle
-U	DISABLE ROM	High Indicates Future Read Cycles Should Be Acknowledged by PAM, not ROM
-V -W		Not Used
-X	MEMR	High Indicates Current Cycle is a Memory Read
-Y		Not Used
-Z	GND	Ground

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts list (02640-60192) located in the appendix.

The Control Memory (AMD) Module provides program storage in Read Only Memory (ROM) for the Processor (8080A-2) Module which controls the functions of the terminal. Via its communication over a top plane bus, this module permits the processor to operate without any wait states during instruction fetch and stack operations. The block diagram shows the functional configuration of the module.

3.1 DATA DRIVERS.

3.1.1 The data drivers are bidirectional buffers which present minimum loading to the CPU and synchronize the movement of data along a bidirectional bus on the PCA. The drivers are enabled only when the control logic determines that data is required at the CPU or at the local RAM. There is one set of drivers for transferring information from the PCA to the CPU and another for bringing data from the CPU to the local RAM.

3.1.2 Data on the top plane bus (P3 connector) is applied to the inputs of U46 and U36, inverted, and driven onto the internal bidirectional data bus (D0 through D7). Data from the ROMs (U17 through U49) is inverted in U34 and U44 and driven onto this same internal bidirectional bus. Address information is buffered on the Processor (8080A-2) PCA, driven onto the top plane bus, and then directly to the ROM and RAM input pins. The least significant 11 address lines distribute address information throughout the ROM and RAM arrays. The highest order bits are examined by exclusive NOR gates to determine whether or not the PCA is being addressed.

3.2 ROM AND RAM MEMORY.

3.2.1 The Control Memory PCA is designed to work with the Advance Micro Devices 16K ROM (part number AM9216), which can be ordered with two programmable chip selects. In order to function properly in this PCA, both programmable chip selects must be specified to be active low.

3.2.2 The ROM chips are mask programmed, 400 nanoseconds access time, 16K bits organized as 2K by 8 bits. The RAM chips are N-channel MOS 1K static RAMs organized as 256 by 4 bits.

3.3 ADDRESS SELECT.

3.3.1 The address select block contains exclusive NOR gates (U23, U24) and decoders which permit the ROM and RAM memory block to be assigned to either of two locations within memory. By removing the +24K jumper, the Control Memory PCA becomes a second ROM PCA in applications requiring more than 24K of ROM. The location of the fast RAM is also moved so that the 256 bytes on the second PCA can supplement the RAM available on the first ROM PCA.

3.3.2 The schematic illustrates the logic required to select one of the 12 ROMs on the PCA. The three most significant address lines are applied through an adder (U51) to a 3-to-8 decoder (U52). The next two most significant address lines drive a 2-to-4 decoder (U33). The negative going outputs from these two decoders are applied to the Chip Select inputs of the ROMs. When both Chip Select inputs of a ROM are set low, the ROM's output lines are enabled. This causes the contents of the addressed memory cell to be placed on the data bus.

3.3.2.1 Referring to the schematic, the three most significant address lines pass through an adder at U51. This adder, depending on whether or not the +24K jumper is in place, adds "0" (000) or "3" (011) to the address that is output by the CPU. The output of the adder is applied to decoder U52. The eight outputs of this decoder divide the 64K address space of the CPU into 8K chunks. Only the three outputs which correspond to the address space between 24K and 48K are used to enable chips on this PCA. Whenever the +24K jumper is out, the adder adds "0" to the three most significant address lines and the PCA responds directly to the references within the 24K to 48K address space. When the +24K jumper is in, the adder adds 011 to the three most significant address lines and in effect shifts the 0-24K addresses up to the 24-48K location. U33 is a 2-to-4 decoder which in effect divides each 8K block into 2K blocks. The negative going AND of these two decoders (U52 and U33), which occurs within each ROM, selects the ROM.

3.3.2.2 The 256-byte RAM is made up of two 256 by 4 static N-channel MOS chips. An 8-bit comparator determines when the RAM block is being addresssed. The CPU provides all the set up and hold times required by the memory

chips. Figure 3 shows the read and write timing relationships. The WO signal is used to disable the RAM outputs and to direct data from the processor to the RAMs. The WRITE pulse causes the RAMs to memorize the current state of the data lines and store that information at the location addressed by the address lines.

3.4 CHIP DE-SELECT.

3.4.1 Each of the 2K ROM chips may be individually disabled. This feature permits substitution of specialized firmware for specific applications without requiring a complete new set of mask programmed ROMs. If a 2K ROM is de-selected, the Control Memory (AMD) Module will not return a negative $\overline{\text{TOP ACTIVE}}$ signal when an access is made to that 2K block. Whenever the 8080A-2 Processor does not receive a $\overline{\text{TOP ACTIVE}}$ signal within about 175 nanoseconds after the address is asserted, it makes a request to the bottom bus (Backplane Assembly). It is possible to put a PROM PCA on the bottom bus and thus replace the missing 2K chunk in the Control Memory (AMD) Module.

3.4.2 The outputs of the 2K decoder (U33) are ORed (U22 and U21) together through a set of jumpers which, upon removal, permit the user to disable any one of the 2K ROM chips. In actual practice, the memory chip is still selected but all signals that go off the PCA are disabled. The CPU does not receive the $\overline{\text{TOP ACTIVE}}$ signal, so it defaults to the bottom bus.

3.5 CONTROL LOGIC.

3.5.1 The control logic receives address information, jumper selections, and chip de-select inputs. From these inputs it determines when a memory reference can be serviced by firmware instructions stored on its PCA and then communicates that information back to the Processor (8080A-2) PCA.

3.5.2 The control logic block NANDs together the outputs of U52 and U33 in U41 and U32. The chip de-select block opens the path for select information from U33 whenever a jumper has been removed and prevents the NAND gates (U41 and U32) from pulling $\overline{\text{TOP ACTIVE}}$ low. One input of each NAND gate receives the output of U52 which has been inverted to active high by U42. The other input becomes high whenever the appro-

priate output of U33 goes low (if the jumper is in place). Gates U21 and U22 in the chip de-select logic are 4-input OR gates used to combine four jumpers into a single output. The outputs of U41 are wire ORed and connect to the P3 connector at Pin 18 ($\overline{\text{TOP ACTIVE}}$). The output of U21, Pin 8 (BOARD SELECT) is used to enable the data drivers whenever the processor raises READ (P3, Pin 19).

4.0 TIMING CONSIDERATIONS.

4.0.1 The 8080A-2 Processor is driven by a clock which has a basic period of 400 nanoseconds. There are two clock signals which drive the CPU and are generated on the Processor (8080A-2) PCA. These clock signals govern the timing of addresses coming from the CPU and determine the set up times required for information that is returned from the memory to the processor. The timing diagram (figure 3), shows the timing for PHASE1 and PHASE2 and the resultant access time that is availabe at the pins of the CPU.

4.0.2 Addresses become valid at the pins of the processor a maximum of 175 nanoseconds after the rising edge of PHASE2. Data must be valid at the processor 130 nanoseconds before the leading edge of the second PHASE2. The time required from output of the address until the data must be valid at the CPU is less than 495 nanoseconds. There are four levels of buffering in the path from the processor address outputs to the processor data inputs. Assuming 20 nanoseconds per level of gating, this implies that 80 nanoseconds of delay must be added to the 400 nanoseconds worst case access time of the ROM chips. The timing required for TOP ACTIVE is also shown in the timing diagram. It is necessary to have this signal valid with at least 30 nanoseconds set up time before the falling edge of PHASE1. Three are about 175 nanoseconds available for this purpose.

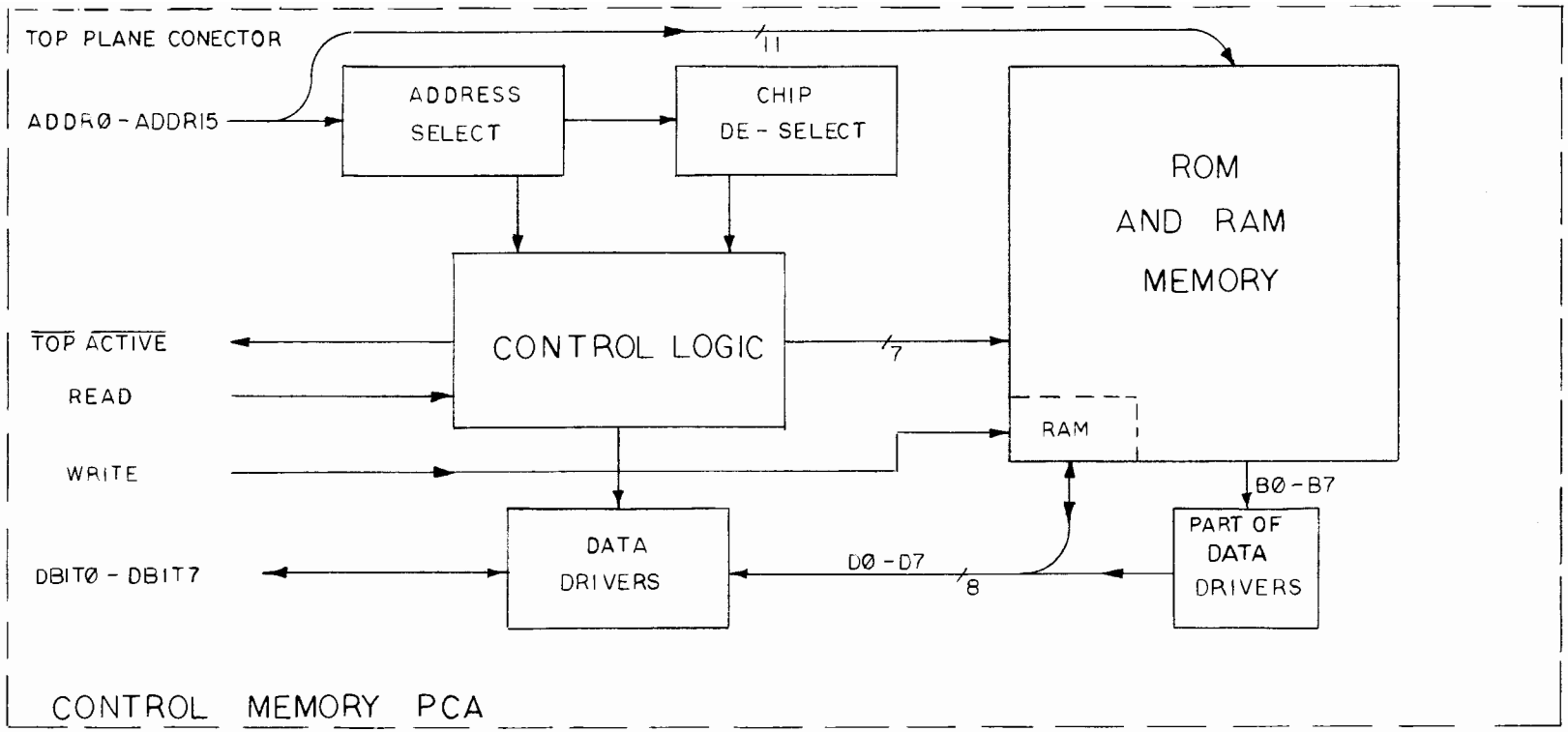

Figure 1
Control Memory Block Diagram
SEP-06-77 13255-91192

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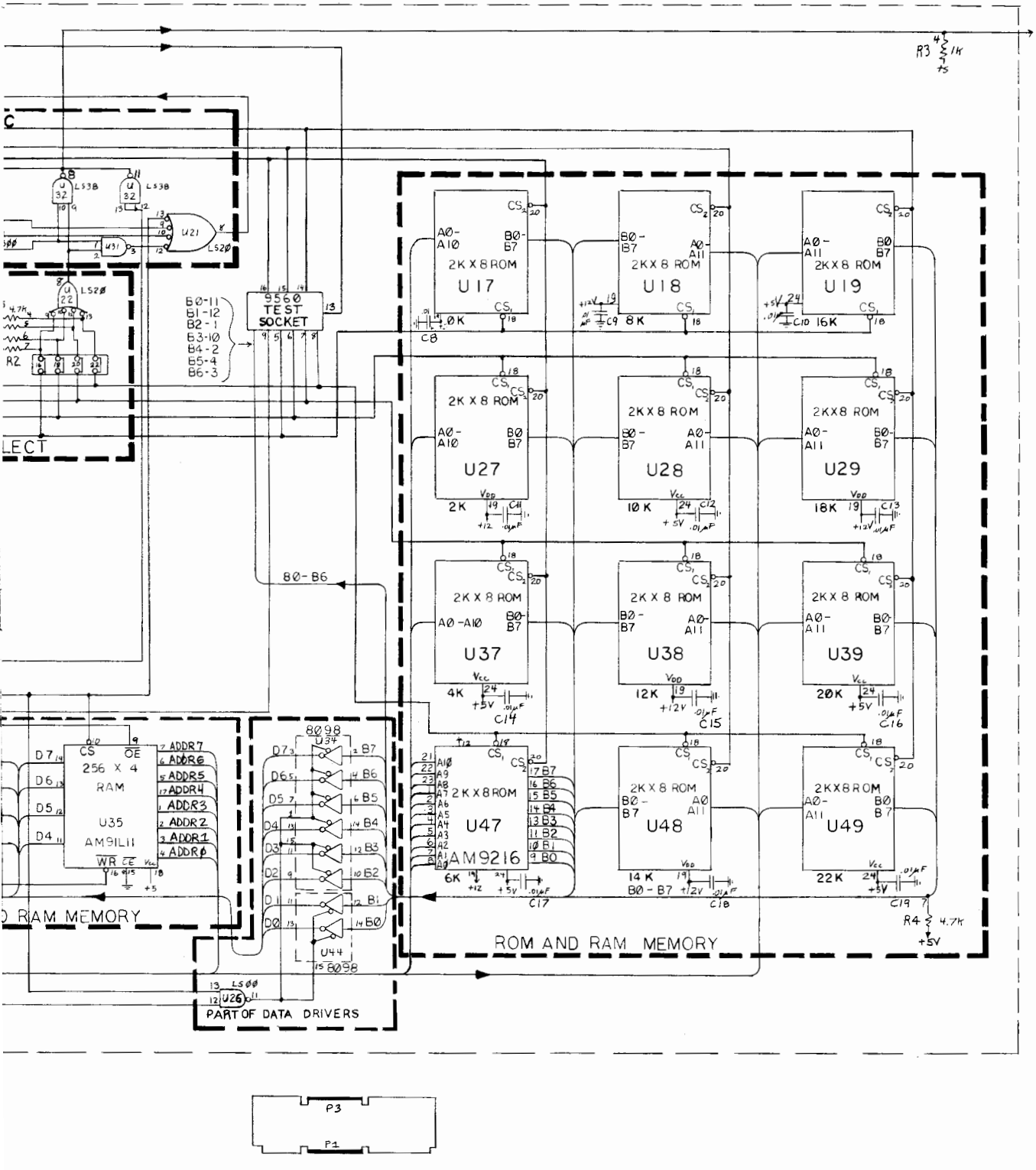
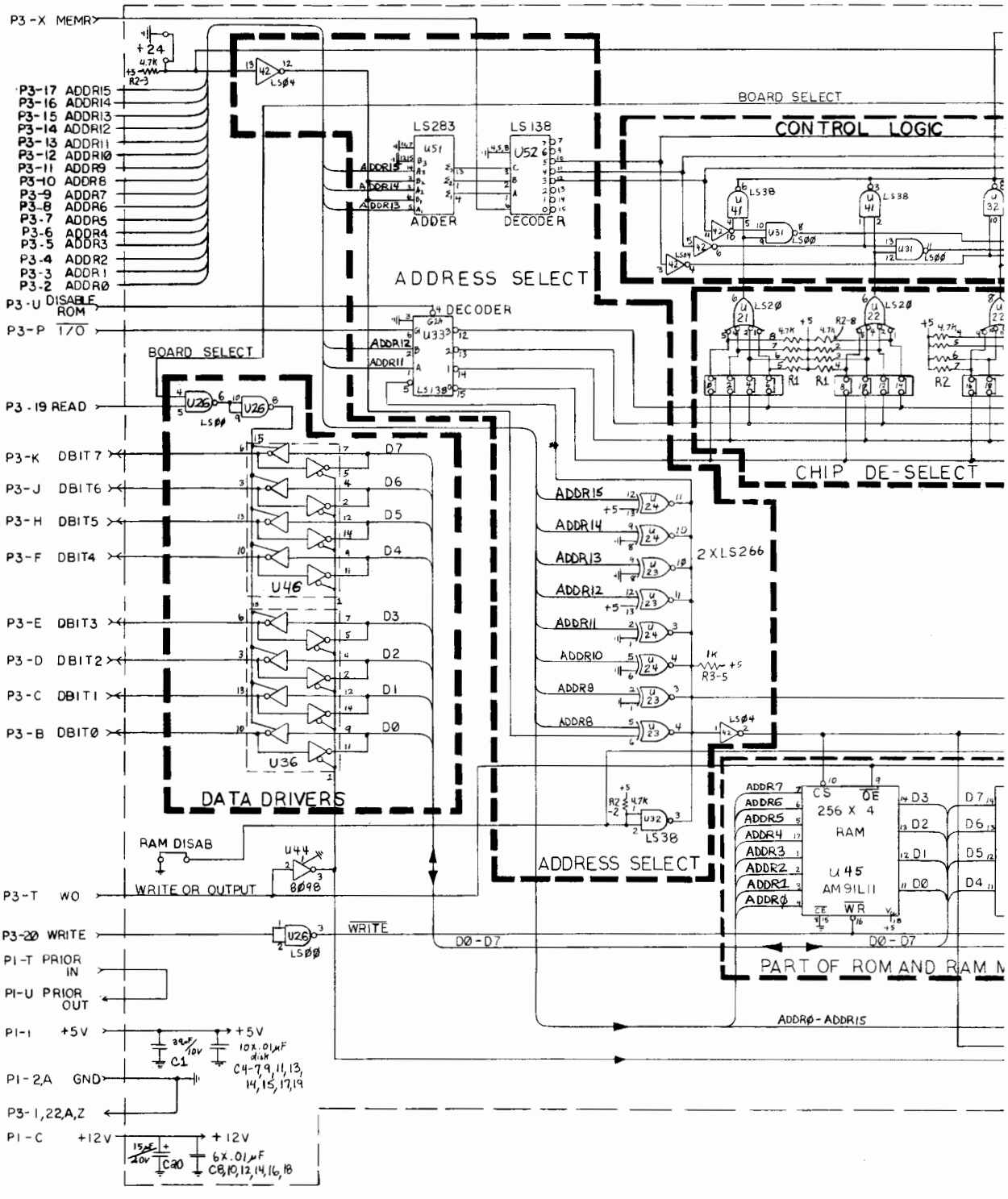
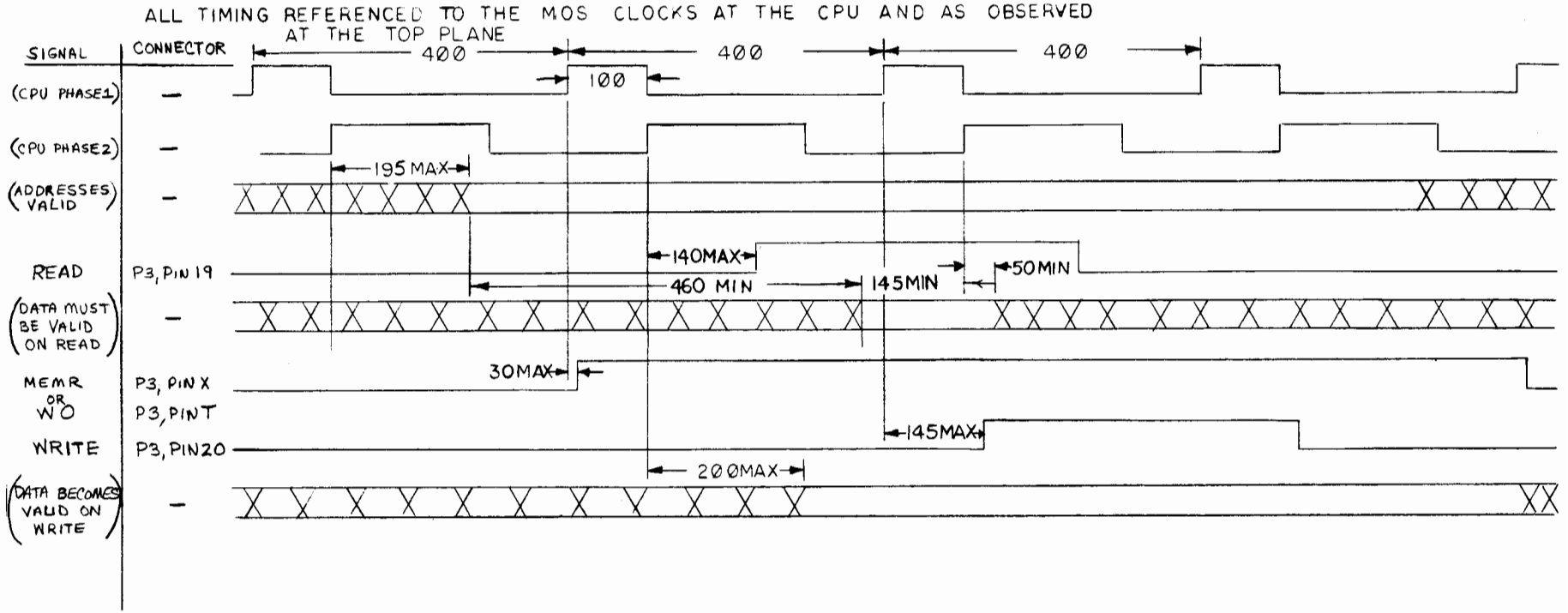


Figure 2
Control Memory PCA Schematic Diagram
SEP-06-77 13255-91192


P3-X MEMR
+24
4.7K
R2-3
P3-17 ADDR15
P3-16 ADDR14
P3-15 ADDR13
P3-14 ADDR12
P3-13 ADDR11
P3-12 ADDR10
P3-11 ADDR9
P3-10 ADDR8
P3-9 ADDR7
P3-8 ADDR6
P3-7 ADDR5
P3-6 ADDR4
P3-5 ADDR3
P3-4 ADDR2
P3-3 ADDR1
P3-2 ADDR0
P3-U DISABLE ROM
P3-P I/O
P3-19 READ
P3-K DBIT7
P3-J DBIT6
P3-H DBIT5
P3-F DBIT4
P3-E DBIT3
P3-D DBIT2
P3-C DBIT1
P3-B DBIT0
P3-T WO
P3-20 WRITE
P1-T PRIOR IN
P1-U PRIOR OUT
P1-1 +5V
P1-2,A GND
P3-1,22,A,Z
P1-C +12V
LS283
U51
ADDER
LS138
U52
DECODER
BOARD SELECT
CONTROL LOGIC
ADDRESS SELECT
CHIP DE-SELECT
DATA DRIVERS
U46
U36
D7
D6
D5
D4
D3
D2
D1
D0
2XLS266
RAM DISAB
WRITE OR OUTPUT
8098
WRITE
D0-D7
256 X 4
RAM
U45
AM 91L11
CS
OE
WR
PART OF ROM AND RAM
ADDR0-ADDR15
+5V
+12V
C1
C4-7,9,11,13,14,15,17,19
C20
C8,10,12,14,16,18



ALL TIMES IN NANOSECONDS

Figure 3
Control Memory Timing Diagram
SEP-06-77 13255-91192

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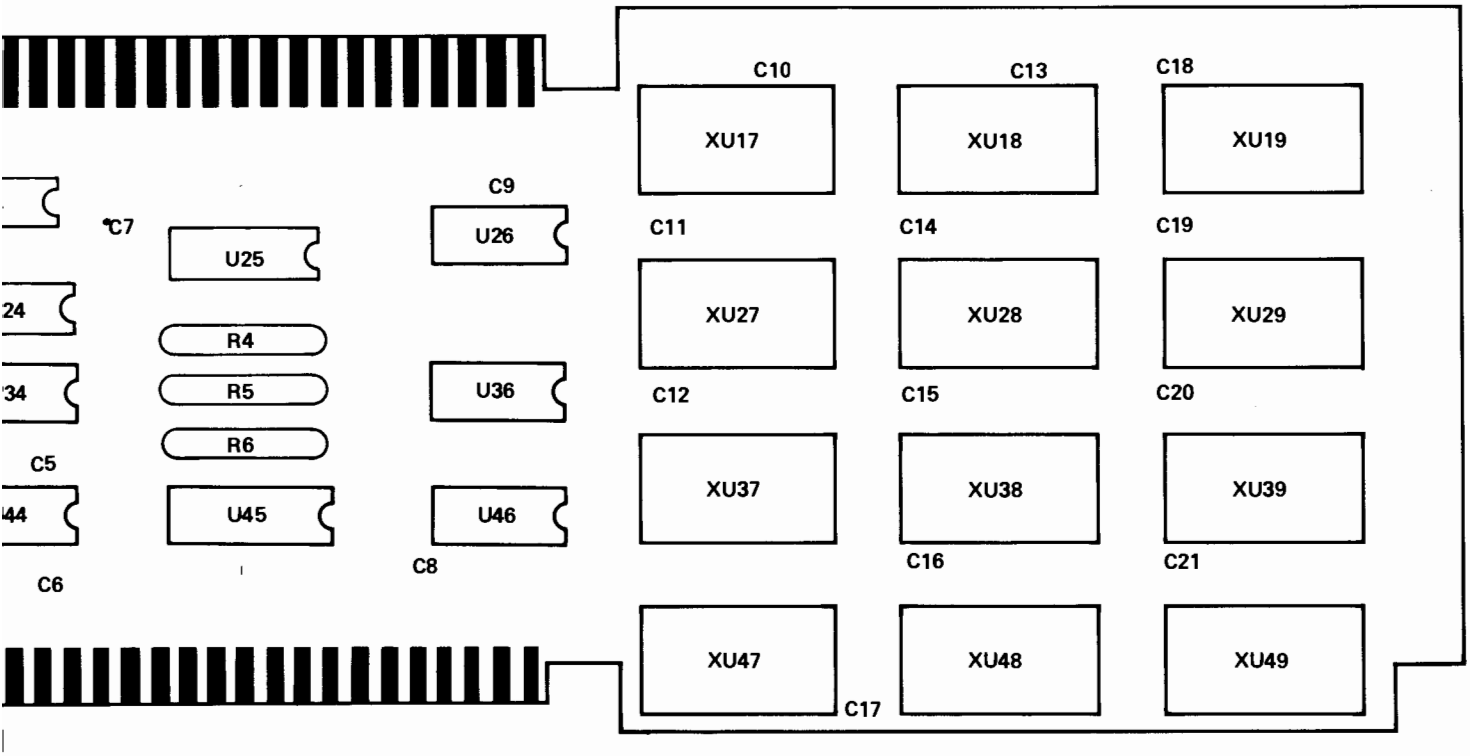
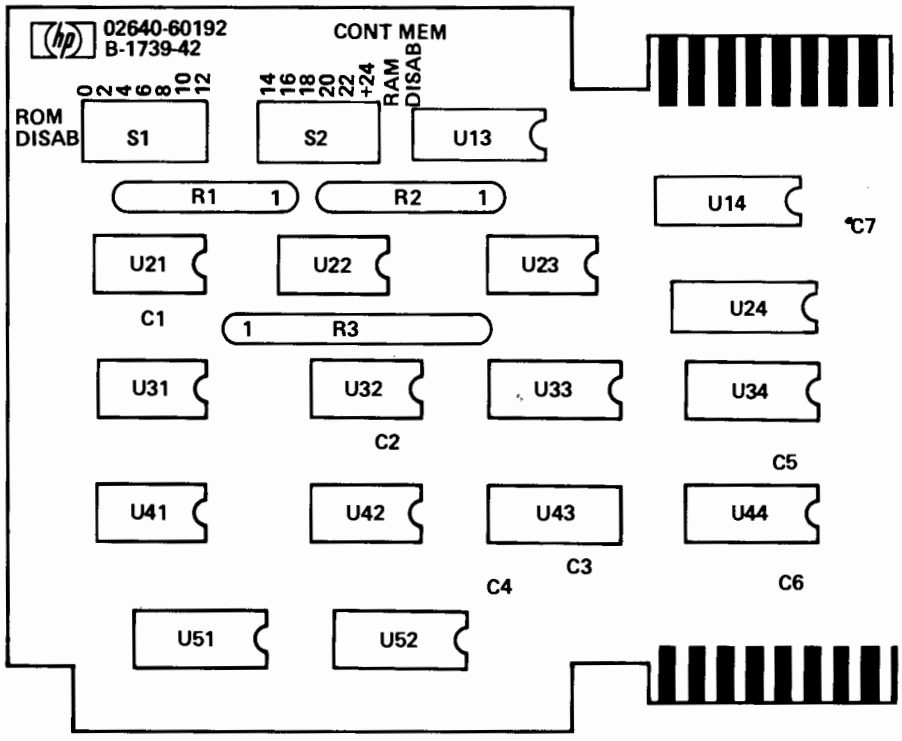


Figure 4
Control Memory PCA Component Location Diagram
SEP-06-77 13255-91192


02640-60192
B-1739-42
CONT MEM
0 2 4 6 8 10 12
14 16 18 20 22 +24
RAM DISAB
ROM DISAB
S1
S2
U13
R1 1
R2 1
U14
C7
U21
U22
U23
U24
C1
1 R3
U31
U32
U33
U34
C2
C5
U41
U42
U43
U44
C3
C4
C6
U51
U52

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60192	1	CONTROL MEMORY ASSEMBLY DATE CODE: B-1739-42 REVISION DATE: 10-26-77		
C1	0160-2055	15	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C2	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C3	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0180-0393	1	CAPACITOR-FXD 39UF +-10% 10VDC TA	56289	150D396X9010B2
C5	0150-0121	4	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C6	0180-1746	1	CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
C7	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C8	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C9	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C18	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C19	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C20	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C21	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
E1	0360-0124	1	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
J46	1200-0614	1	SOCKET-IC 18-CONT DIP-SLDR	91506	518-AG11D
R1	1810-0125	2	NETWORK-RESISTOR 8-PIN-SIP .125-PIN-SPCG	11236	75D
R2	1810-0125		NETWORK-RESISTOR 8-PIN-SIP .125-PIN-SPCG	11236	75D
R3	1810-0121	1	NETWORK-RESISTOR 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R4	1810-0350	3	NETWORK-RESISTOR 8-PIN-SIP .125-PIN-SPCG	28480	181D-D35D
R5	1810-0350		NETWORK-RESISTOR 8-PIN-SIP .125-PIN-SPCG	28480	1810-D350
R6	1810-0350		NETWORK-RESISTOR 8-PIN-SIP .125-PIN-SPCG	28480	1810-D350
S1	3101-1974	2	SWITCH-ASSEMBLY-ROCKER 7-SPST	04990	76YY2077
S2	3101-1974		SWITCH-ASSEMBLY-ROCKER 7-SPST	04990	76YY2077
U13	1820-1197	2	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U14	1820-1828	2	IC-DIGITAL TTL DRIVER	02910	8T28B
U17	1200-0541	12	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U18	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U19	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	12D0-0541
U21	1820-1204	2	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U22	1820-1204		IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U23	1820-1297	2	IC-DIGITAL SN74LS266N TTL LS QUAD 2	D1295	SN74LS266N
U24	1820-1828		IC-DIGITAL TTL DRIVER	02910	8T3128B
U25	1820-1049	2	IC-DIGITAL DM8097N TTL HEX BUFFER	01295	SN44585N
U26	1820-1297		IC-DIGITAL SN74LS266N TTL LS QUAD 2	01295	SN74LS266N
U27	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U28	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U29	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U31	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U32	1820-1209	2	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U33	1820-1208	1	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U34	1818-0197	2	IC AM91L11BPC 1K RAM NMOS	34335	AM91L11BPC
U36	1820-1216	2	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U37	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U38	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U39	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U41	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U42	1820-1199	1	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U43	1820-1213	1	IC-DIGITAL SN74LS113N TTL LS DUAL J-K	02195	SN74LS113N
U44	1818-0197		IC AM91L11BPC 1K RAM NMOS	34335	AM91L11BPC
U45	1820-1049		IC-DIGITAL DM8097N TTL HEX BUFFER	01295	SN44585N
U47	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U48	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U49	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
U51	1820-1441	1	IC-DIGITAL SN74LS283N TTL LS BIN	01295	SN74LS283N
U52	1820-1216		IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N