HP 13255

ASYNCHRONOUS MULTIPOINT INTERFACE MODULE

Manual Part No. 13255-91106

REVISED

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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1.0 INTRODUCTION.

The Asynchronous Multipoint Interface Module provides an RS232C compatible, asynchronous data communications interface. Hardware is provided (non RS232C) to permit multipoint daisy-chaining of terminals. A programmable baud rate generator is included as well as two bytes of program accessable switches. Refer to module section 13255-91086 for parts lists for the US Modem Cable Assembly (02640-60131) and the Data Comm Self Test Hood Assembly (02645-60002).

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Asynchronous Multipoint Interface Module is contained in tables 1.0 through 6.7.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60106	Async Multipoint I/F PCA	12.9 x 4.0 x 0.6	0.50

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.876 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 400 mA	@ 150 mA	@ 70 mA (An additional 200 mA required for 02640-60140 cable)	@ mA NOT APPLICABLE
115 volts ac @ A NOT APPLICABLE		220 volts ac @ A NOT APPLICABLE	
Clock Frequency: 4.915 MHz +/-0.1%			

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
INT	Interrupt on $\overline{ATN2}$	Interrupt on $\overline{ATN}$
PL6 thru PL0	Respond to an Interrupt poll on any one of these bus data bits	No Effect
A4,A11,A10,A9	Address Bit is a "0" in the Module Address	Address Bit is a "1" in the Module Address
-12	Connect -12V to P2, Pin N	No Effect
2SB	Transmit and receive characters framed with 1 start and 1 stop bit	Transmit and receive characters framed with 1 start and 2 stop bits

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7		Not Used
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17		}
		}
-18		}
		} Not Used
-19		}
		}
-20		}
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R	$\overline{\text{ATN2}}$	Negative True, CTU and Polled Interrupt Request
-S		Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	$\overline{\text{PROC ACTIVE}}$	Negative True, Processor Active (Controlling Bus)
-W		Not Used
-X		
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	BA0+	} Differential, Daisy-Chain Signal Carrying
-2	BA0-	} Data from the Terminals to a Modem or CPU
		} (output)
-3	BAI+	} Differential, Daisy-Chain Signal Carrying
-4	BAI-	} Data from the Terminals to a Modem or CPU
		} (input)
-5	CA0	} Daisy-Chain Signal Indicating that One of
		} the Terminals in the Chain is Requesting
		} to Send (output)
-6	CB0	} Daisy-Chain Signal Originating at the Modem
		} Indicating That it is Clear for the Termi-
		} nals to Transmit (output)
-7	CAI+	} Daisy-Chain Signal Indicating that One of
-8	CAI-	} the Terminals in the Chain is Requesting
		} to Send (input)
-9	CBI+	} Daisy-Chain Signal Originating at the Modem
-10	CBI-	} Indicating That it is Clear for the Termi-
		} nal to Transmit (input)
-15	BB0+	} Differential, Daisy-Chain Signal Carrying
-11	BB0-	} Data from a Modem to Terminals in the Chain
		} (output)
-12		}
		} Not Used
-13		}
-14	CE	RS232C Ring Indicator

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	GND	Frame Ground
-B	BA	RS232C Transmitted Data
-C	BB	RS232C Received Data
-D	CA	RS232C Request To Send
-E	CB	RS232C Clear To Send
-F	CC	RS232C Data Set Ready
-H	AB	RS232C Signal Ground
-J	CF	RS232C Carrier Detect
-K	BBI+	} Differential, Daisy-Chain Signal
-L	BBI-	} Carrying Data From the Modem to the Terminals (input)
-M	SCA	RS232C Secondary Channel Request To Send
-N	SCF	RS232C Secondary Channel Carrier Detect
-P	CD	RS232C Data Terminal Ready
-R	CH	RS232C Data Signal Rate Selector
-S		Not Used

Table 6.0 Module Bus Pin Assignments

Function Performed: Output Data for Transmission	Value	Bus Signal
	X	ADDR 15
Poll Bit: Switch Selectable (Bit 6-0)	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR3 = 0	X	ADDR 8
ADDR5 = 1	X	ADDR 7
ADDR6 = 1	1	ADDR 6
	1	ADDR 5
	A4	ADDR 4
	0	ADDR 3
Data Bus Bit Interpretation:	X	ADDR 2
	X	ADDR 1
	X	ADDR 0
B7		
Output Data Bit 7	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
B6	B4	BUS 4
Output Data Bit 6	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5	B0	BUS 0
Output Data Bit 5		
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4	X=Don't Care	
Output Data Bit 4		
B3		
Output Data Bit 3		
B2		
Output Data Bit 2		
B1		
Output Data Bit 1		
B0		
Output Data Bit 0		

Table 6.1 Module Bus Pin Assignments

Function Performed: Output Control Byte 1 (Configuration Byte)

Poll Bit: Switch Selectable (Bit 6-0)

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable
Data Comm = (1110)

Function Specifier: ADDR5 = 1
ADDR6 = 0

Data Bus Bit Interpretation:

B7, B6 set number of data bits per character

	Data Bits 5	6	7	8
B7	0	0	1	1
B6	0	1	0	1

B5
0 = Enable Parity
1 = Inhibit Parity

B4
0 = Odd Parity
1 = Even Parity

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
0	ADDR 6
1	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

BAUD RATE

	19200	50	75	110	134.5	150	300	600	200	1200	1800	2400	3600	4800	7200	9600
B3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
B2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
B1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
B0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Table 6.2 Module Bus Pin Assignments

Function Performed: Output Control Byte 2 (Modem Control Byte)

Poll Bit: Switch Selectable (Bit 6-0)

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Data Comm = (1110)

Function Specifier: ADDR5 = 0
ADDR6 = 1

Data Bus Bit Interpretation:

B7
0 = Enable Daisy-Chain CAI and CB0
1 = Inhibit Daisy-Chain CAI and CB0

B6 Not Used

B5 Not Used

B4
0 = Terminal Mode
1 = Channel Monitor Mode

B3
0 = CH On
1 = CH Off

B2
0 = CD On
1 = CD Off

B1
0 = SA On
1 = SA Off

B0
0 = CA On
1 = CA Off

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
0	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.3 Module Bus Pin Assignments

Function Performed: Output Control Bits

Poll Bit: Switch Selectable (Bit 6-0)

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable
Data Comm = (1110)

Function Specifier: ADDR5 = 0
ADDR6 = 0

Only one bit in each of the pairs A0,A1 and A3,A7 can be set to "1" for a given output command

A0
0 = No Effect
1 = Reset Timer

A1
0 = No Effect
1 = Set Timer

A3
0 = No Effect
1 = Enable Transmission Complete Interrupt

A7
0 = No Effect
1 = Enable Transmitter Ready Interrupt

Data Bus Bit Interpretation: Not Applicable

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
A7	ADDR 7
0	ADDR 6
0	ADDR 5
A4	ADDR 4
A3	ADDR 3
X	ADDR 2
A1	ADDR 1
A0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.4 Module Bus Pin Assignments

Function Performed: Input Received Character	Value	Bus Signal
	X	ADDR 15
Poll Bit: Switch Selectable (Bit 6-0)	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
ADDR6 = 0	X	ADDR 7
	0	ADDR 6
	0	ADDR 5
	A4	ADDR 4
	X	ADDR 3
Data Bus Bit Interpretation:	X	ADDR 2
	X	ADDR 1
	X	ADDR 0
B7		
Input Data Bit 7	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
B6	B4	BUS 4
Input Data Bit 6	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5	B0	BUS 0
Input Data Bit 5		
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4	X=Don't Care	
Input Data Bit 4		
B3		
Input Data Bit 3		
B2		
Input Data Bit 2		
B1		
Input Data Bit 1		
B0		
Input Data Bit 0		

Table 6.5 Module Bus Pin Assignments

Function Performed: Input Status Byte 1 (Interrupt Status)	Value	Bus Signal
	X	ADDR 15
Poll Bit: Switch Selectable (Bit 6-0)	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR3 = 0	X	ADDR 8
ADDR5 = 1	X	ADDR 7
ADDR6 = 0	0	ADDR 6
	1	ADDR 5
Data Bus Bit Interpretation: An interrupt is generated if any condition causes B0, B1, or B7 to be set to the "1" value. Values of B5 and B6 are valid only if B7 = 1	A4	ADDR 4
	0	ADDR 3
	X	ADDR 2
	X	ADDR 1
	X	ADDR 0
B7	B7	BUS 7
0 = Receiver Register Empty	B6	BUS 6
1 = Receiver Register Full (Cleared by inputting a character)	B5	BUS 5
	B4	BUS 4
B6	B3	BUS 3
0 = No Parity Error	B2	BUS 2
1 = Parity Error (Cleared by inputting status)	B1	BUS 1
	B0	BUS 0
B5	1=Logical 1=Bus Low	
0 = No Overrun Error	0=Logical 0=Bus High	
1 = Overrun Error (Cleared by inputting status or character)	X=Don't Care	
B4, B3, B2 Not Used		
B1		
0 = No Timer Interrupt		
1 = Timer Interrupt Active (Cleared by resetting the timer)		
B0		
0 = No Transmit Interrupt		
1 = Transmit Interrupt Active (Set when CB comes up, cleared by outputting character or dropping CA or CB)		

Table 6.6 Module Bus Pin Assignments

Function Performed: Input Status Byte 2 (Modem Status)

Poll Bit: Switch Selectable (Bit 6-0)

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable
Data Comm = (1110)

Function Specifier: ADDR3 = 1
ADDR5 = 1
ADDR6 = 0

Data Bus Bit Interpretation:

B7
Always 1
Indicates Multipoint PCA in System

B6
Always 0
Indicates Async Multipoint PCA in System

B5
0 = CAI Off (Downline CA)
1 = CAI On

B4
0 = CE On
1 = CE Off

B3
0 = SB On
1 = SB Off

B2
0 = CC On
1 = CC Off

B1
0 = CF On
1 = CF Off

B0
0 = CB On
1 = CB Off

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
0	ADDR 6
1	ADDR 5
A4	ADDR 4
1	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.7 Module Bus Pin Assignments

Function Performed: Input Jumper Settings	Value	Bus Signal
	X	ADDR 15
Poll Bit: Switch Selectable (Bit 6-0)	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
ADDR6 = 1	X	ADDR 7
	1	ADDR 6
A3	0	ADDR 5
0 = Select Jumper Character 0 (J00-J07)	A4	ADDR 4
1 = Select Jumper Character 1 (J10-J17)	A3	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
0 = Closed Switch	B7	BUS 7
1 = Open Switch	B6	BUS 6
	B5	BUS 5
B7	B4	BUS 4
Switch 7	B3	BUS 3
	B2	BUS 2
B6	B1	BUS 1
Switch 6	B0	BUS 0
	1=Logical 1=Bus Low	
B5	0=Logical 0=Bus High	
Switch 5	X=Don't Care	
B4		
Switch 4		
B3		
Switch 3		
B2		
Switch 2		
B1		
Switch 1		
B0		
Switch 0		

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), daisy-chain logical connection (figure 3), component location diagram (figure 4), and parts list (02640-60106) located in the appendix.

The purpose of the Asynchronous Multipoint Interface PCA is to transmit and receive start-stop serial data and provide modem control and status lines. Data character format is described in EIA RS404. The line interface is compatible with RS232C and the terminal's daisy-chain circuitry. Figure 3 illustrates the daisy-chain connection when more than one terminal is sharing an RS232C line. BA, BB, CA, and CB are RS232C signals; all others are daisy-chain signals.

3.1 UART AND DATA ROUTING.

3.1.1 The UART (Universal Asynchronous Receiver/Transmitter) is an LSI device used to convert from the 8-bit parallel data format of the terminal data bus to the serial, start-stop data format of the channel. The line monitor multiplexer determines whether data being transmitted from the modem or to the modem is sampled by the PCA.

3.1.2 The UART is a Western Digital TR1602B. The line monitor multiplexer (U58) is used to route received data to the UART. Normally it routes the BB (BBI) signal to the receiver input. However, if the channel monitor mode bit (Bit 4) is set in the control register and the CAI signal is high, the BAI signal will be routed to the UART receiver. This function is used when the terminal is operated as a passive line monitor.

3.2 BAUD RATE GENERATOR.

3.2.1 The baud rate generator uses the bus 4.915 MHz System Clock (SYS CLK) to generate a clock for the UART. The following rates are selectable programmatically: 50 (800 Hz), 75 (1200 Hz), 110 (1760 Hz), 134.5 (2152 Hz), 150 (2400 Hz), 200 (3200 Hz), 300 (4800 Hz), 600 (9600 Hz), 1200 (19.2 kHz), 1800 (28.8 kHz), 2400 (38.4 kHz), 3600 (57.6 kHz), 4800 (76.8 kHz), 7200 (115.2 kHz), 9600 (153.6 kHz), and 19200 (307.2 kHz).

3.2.2 The first stage of the baud rate generator (U31 and U32) is a divide-by-5 and 1/3 circuit which divides the 4.915 MHz bus clock to 921.6 kHz for the MM5307 (U33). The circuit contains a synchronous counter and two J-K flip-flops (U32). The counter is programmed as a divide-by-5 or a divide-by-6 circuit depending on the state of the flip-flops. When the Q output of the first flip-flop (U32, Pin 9) is high, the counter divides by 5; when low it divides by 6. The counter divides by 5 twice and by 6 once to produce an average divisor of 5 and 1/3. The flip-flops (U32, Pin 9 and U32, Pin 5) follow the 11-00-10 sequence repetitively.

3.2.3 A 4-bit program constant is loaded into the LS175 register (U34) to program the circuit. (Refer to table 6.1 for additional information.) All of the baud rates except 200 and 19200 are generated by U33. When the 1000 code (200 baud) is in the baud rate register (U34) it is decoded by several gates and converted to a 1010 by an OR gate before reaching U33. This decoding logic also programs another synchronous counter (U25) to divide by 9. The 1010 code (1800 baud) on U33 provides an 1800 baud clock to the counter which divides it by 9 to generate the 200 baud clock. The proper routing of these signals is done with an LS51 AND-OR-Invert (U24) pack. When the generator is programmed with an 0000 code, the counter functions as a divide-by-16 while being clocked at 4.915 MHz. The divide-by-16 counter outputs 307.2 kHz (19200 baud) which is routed to the UART by the LS51 (U24).

3.3 INSTRUCTION DECODER.

3.3.1 The instruction decoder consists of an LS138 3-to-8 decoder (U47) and several gates. This circuit uses control and address lines on the terminal data bus to generate control signals on the PCA.

3.3.2 Four exclusive-OR gates (U46) that can be programmed by the A4, and A11 through A9 switches on the PCA are used to decode the module's address and to enable U47. The control signals are decoded as follows:

ADDR6	ADDR5	ADDR3	WRITE	I/O	REQ	U47	
1	1	0	1	1	1	Y0	Output data.
0	1	X	1	1	1	Y2	Output configuration byte.
1	0	X	1	1	1	Y1	Output modem control byte.
0	0	X	1	1	1	Y3	Output control bits.
0	1	0	0	1	1	Y6	Input interrupt status.
0	1	1	0	1	1		Input modem status.
1	0	0	0	1	1	Y5	Input Jumper 0 byte.
1	0	1	0	1	1		Input Jumper 1 byte.
0	0	X	0	1	1	Y7	Input data.

3.3.3 The control bits output command does several things depending on addresses 0, 1, 3, and 7:

ADDR7	ADDR3	ADDR1	ADDR0	
X	X	X	1	Reset timer.
X	X	1	X	Set timer.
X	1	X	X	Enable transmission complete interrupt.
1	X	X	X	Enable transmitter ready interrupt.

3.3.4 Switch selectable interrupt polling is also provided. When a read operation is performed with $\overline{\text{POLL}}$ low, the PCA will drive one of the data bus lines (Bit0-6 switch selectable) low when an interrupt is active.

3.4 STATUS-JUMPER MULTIPLEXING.

3.4.1 This circuit is used to gate one of two status bytes (see tables 6.5 and 6.6) or one of two switch programmable bytes onto the terminal data bus. Four LS153 multiplexers (U22, U23, U13, and U12) are used for this function. The byte selection is as follows:

A	B	
0	0	Jumper 0
0	1	Jumper 1
1	0	Interrupt Status
1	1	Modem Status

3.5 CONTROL REGISTER. The control register is used to latch the RS232C outputs, control the line monitor multiplexer, and to inhibit or enable the daisy-chain control lines. Table 6.2 indicates the bit and polarity designation.

3.6 INTERRUPT LOGIC.

3.6.1 The interrupt network is primarily an AND-OR circuit. The AND function decides if an interrupt is active; the OR function directs the interrupt signal to the appropriate interrupt line. Interrupts can be directed to the $\overline{ATN}$ or $\overline{ATN2}$ line depending on the position of the INT switch (open = $\overline{ATN}$, closed = $\overline{ATN2}$). There are three possible interrupts: transmit, receive, and timer. Whenever the UART receives a character it generates a Data Ready (DR) interrupt at U51, Pin 19. The Output Control Bits command can condition the transmit interrupt (U36, Pin 12) to be a Transmission Complete (U37, Pin 6) or a Transmitter Ready (U37, Pin 3) interrupt. The Transmission Complete interrupt indicates that both the Transmitter Register and the Transmitter Holding Register of the UART are empty. The Transmitter Ready interrupt indicates that the Transmitter Holding Register of the UART is empty. A transmit interrupt can only be active when both CA (CA0) and CB (CBI) are turned on. A timer interrupt occurs about 45 milliseconds after the timer is set. If the timer is reset within this period no interrupt will occur.

3.6.2 The timer network consists of a one-shot (U38), a flip-flop (U49, Pin 6), and a gate. When the timer is set, the Q output (Pin 8) of the one-shot goes high. At the next bus System Clock, the flip-flop is cleared (U49, Pin 6 goes high). When the one-shot times out (U38, Pin 6 goes high) a timer interrupt is generated (U39, Pin 8 goes high). This circuit can be reset at any time.

3.7 LINE RECEIVERS.

3.7.1 Line receivers are provided for both daisy-chain and RS232C operation. The RS232C receivers are standard MC1489A's (U18, U19) with a 330 picofarad noise suppression capacitor. The daisy-chain data lines (BAI, BBI) are received with a high impedance (1.2K) Schottky (U410, U411) opto-isolator. These receivers are driven differentially. The daisy-chain control line receivers are high gain (4370) opto-isolators (U411, U511). The 470-ohm parallel input resistor is used to raise the threshold of the receiver to the midpoint of the received signal. All isolators are buffered with Schmitt inverters (U510).

3.8 LINE DRIVERS.

3.8.1 Line drivers are provided for both RS232C and daisy-chain operation. The RS232C drivers are standard (U512, U29) with a 330 picofarad slew rate limiting capacitor. The daisy-chain data line drivers (BA0, BB0) are peripheral driver chips (U110, U210) with active pullup networks. Two 3.3-ohm resistors and an NPN transistor (Q2, Q4, Q6, Q8,) are used for temporary short circuit protection. The line is driven with a 17 volt differential signal. This scheme is used to make the drive signal symmetrical with respect to the threshold of the receiver. Symmetry is critical on the data signals. Delay is harmless. The control lines are driven with peripheral driver chips with a 330-ohm output impedance. The control lines are driven slowly to eliminate transmission effects.

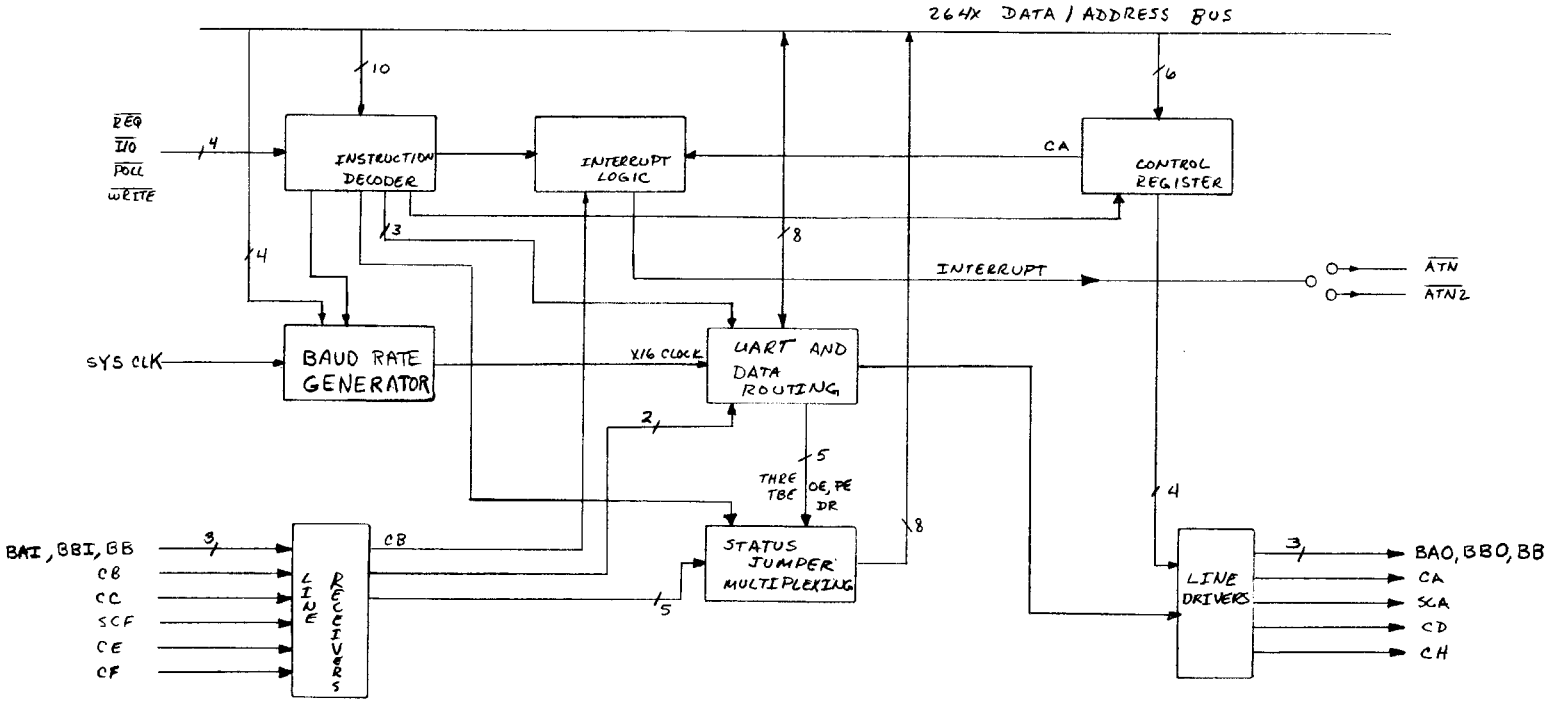


Figure 1
Asynchronous Multipoint Interface Block Diagram
APR-14-78 13255-91106

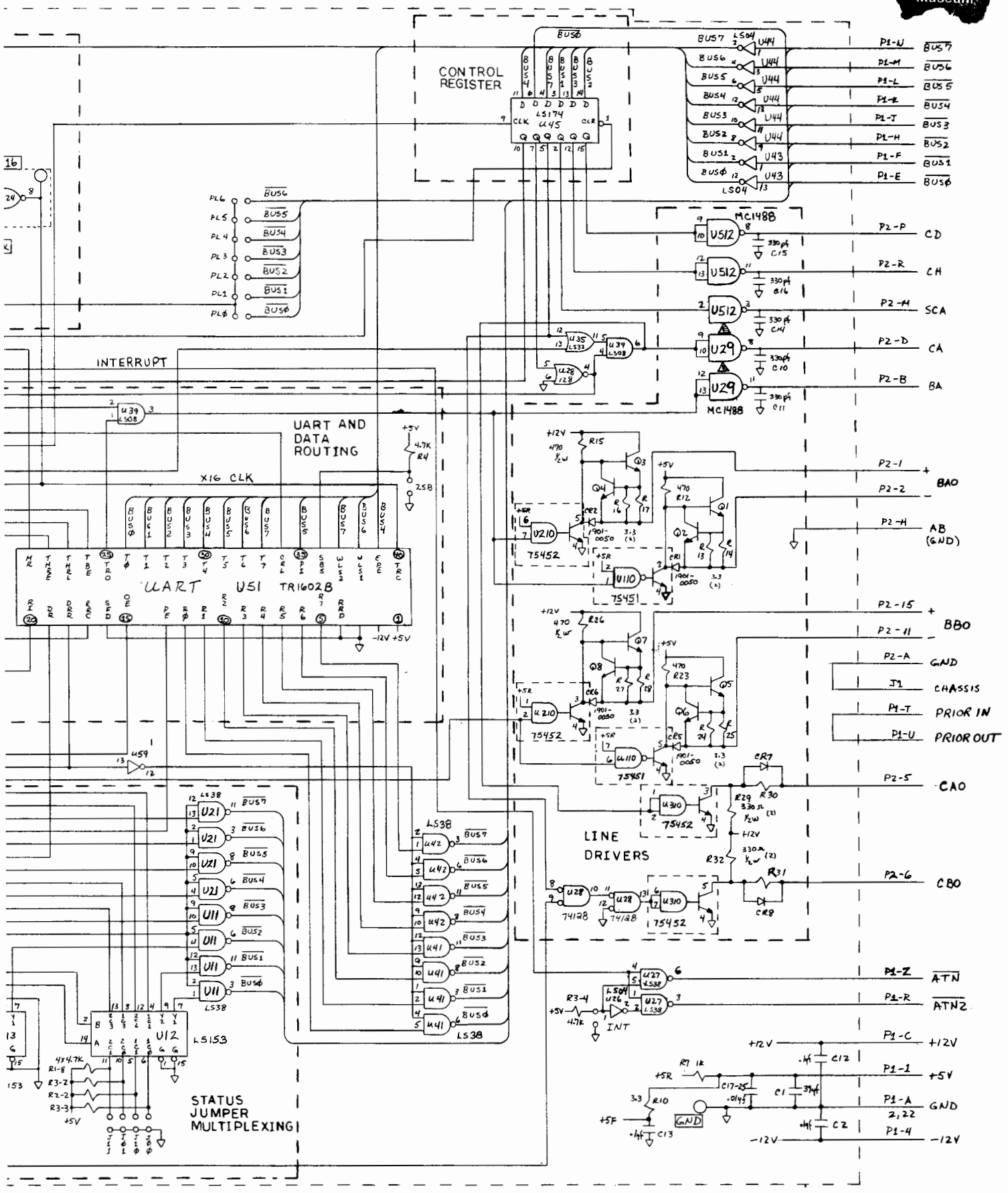
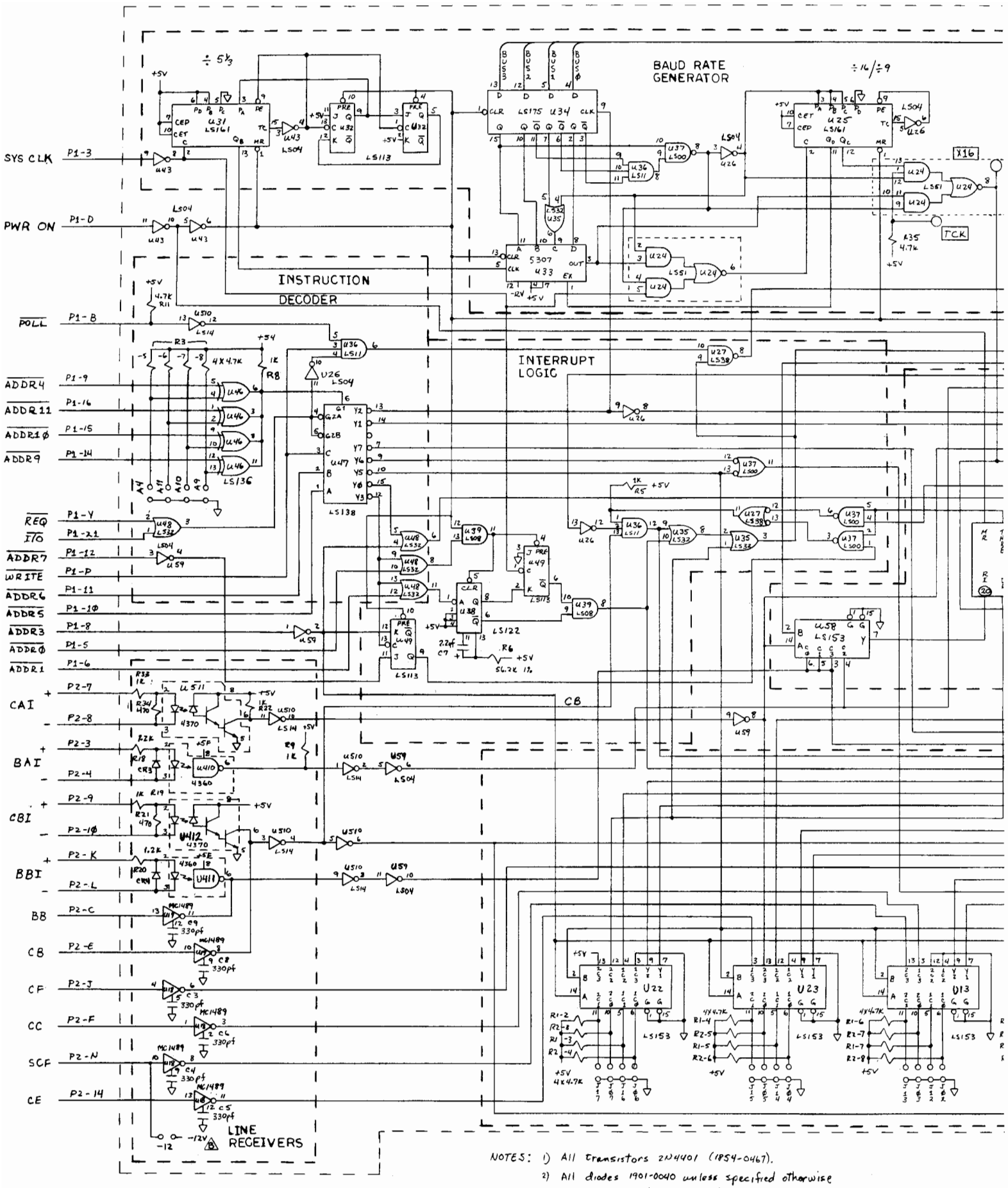


Figure 2
Asynchronous Multipoint Interface PCA
Schematic Diagram
APR-14-78 13255-91106



NOTES: 1) All transistors 2N4401 (1854-0467).
2) All diodes 1901-0040 unless specified otherwise
3) All resistors ¼W, 5% unless specified otherwise.

NOTE: The modem side signals can go directly to the modem or through other terminals to the modem.

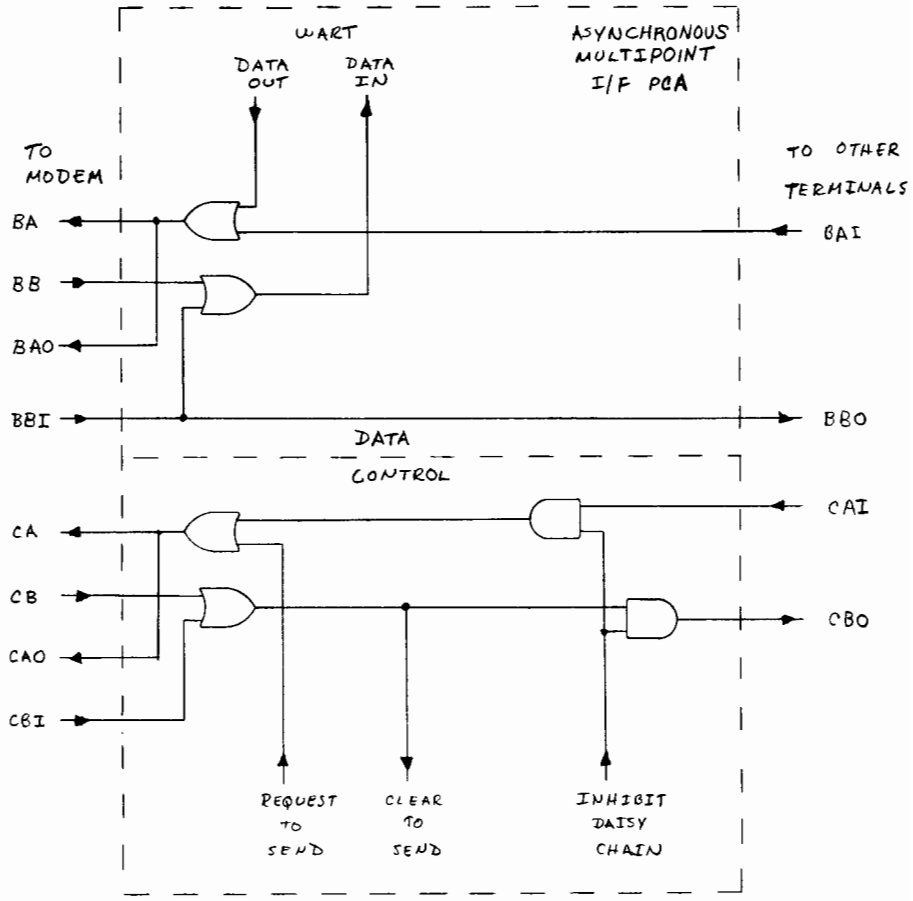


Figure 3
Daisy-Chain Logical Connection Diagram
APR-14-78 13255-91106

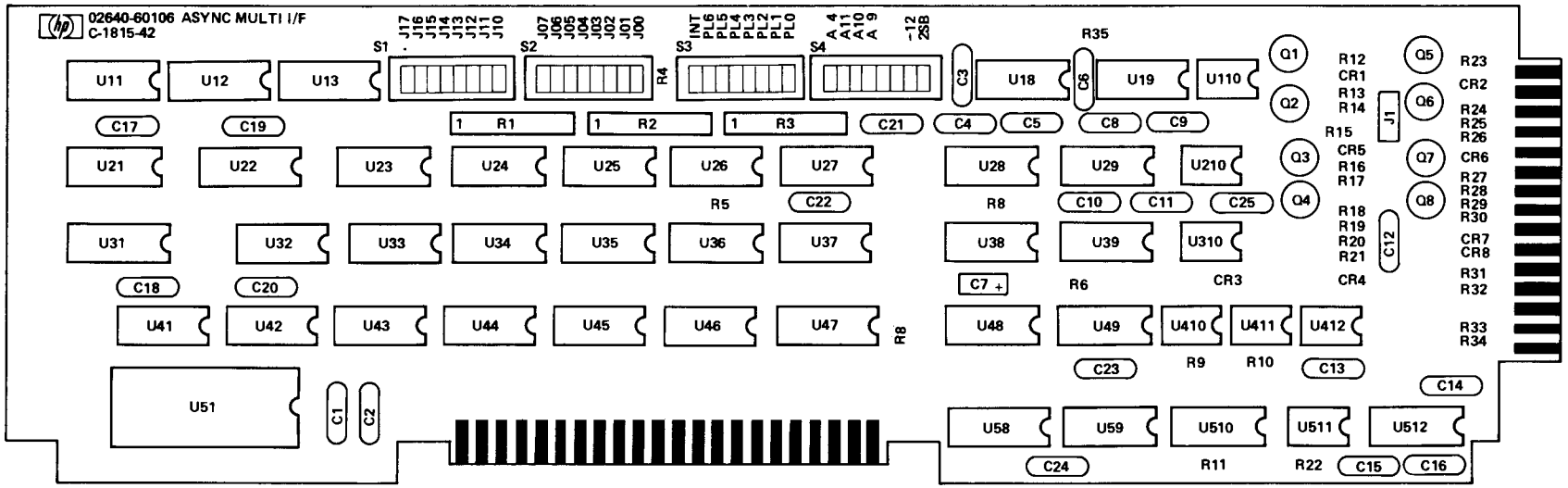


Figure 4
Asynchronous Multipoint Interface PCA
Component Location Diagram
APR-14-78 13255-91106

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60106	1	A SYNC MULTIPOINT INTERFACE AS: DATE CODE: C-1815-42 REVISION DATE: 06-05-78	28480	02640-60106
C1	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0150-0121	3	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C3	0160-3572	11	CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C4	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C5	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C6	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C7	0180-0197	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C8	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C9	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C10	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C11	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C12	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C13	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C14	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C15	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C16	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C17	0160-2055	9	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C18	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C19	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C20	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C21	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C22	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C23	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C24	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C25	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1901-0050	4	DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR2	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR3	1901-0040	4	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR5	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR6	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR7	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR8	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
E1	0360-0124	3	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
J1	1251-1126	1	CONNECTOR-SGL CONT SKT .08-IN-BSC-SZ RND	74970	105-0756-001
Q1	1854-0467	8	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q2	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q3	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q4	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q5	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q6	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q7	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q8	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
R1	1810-0125	3	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R3	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R4	0683-4725	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R5	0683-1025	7	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R6	0757-0459	1	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
R7	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R8	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R9	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R10	0683-0335	9	RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R11	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R12	0683-4715	4	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R13	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R14	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R15	0686-4715	2	RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R16	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R17	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R18	0683-1225	2	RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
R19	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R20	0683-1225		RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
R21	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R22	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R23	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R24	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R25	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			ASYNC MULTIPOINT INTERFACE ASSEMBLY CONT'D.		
R26	0686-4715		RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R27	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R28	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R29	0686-3315	4	RESISTOR 330 5% .5W CC TC=0+529	01121	EB3315
R30	0686-3315		RESISTOR 330 5% .5W CC TC=0+529	01121	EB3315
R31	0686-3315		RESISTOR 330 5% .5W CC TC=0+529	01121	EB3315
R32	0686-3315		RESISTOR 330 5% .5W CC TC=0+529	01121	EB3315
R33	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R34	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R35	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
S1	3101-2094	4	SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392	4	COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
S2	3101-2094		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392		COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
S3	3101-2094		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392		COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
S4	3101-2094		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392		COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
U11	1820-1209	5	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U12	1820-1244	5	IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U13	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U18	1820-0990	2	IC-DIGITAL MC1489AL DTL QUAD NAND	04713	MC1489AL
U19	1820-0990		IC-DIGITAL MC1489AL DTL QUAD NAND	04713	MC1489AL
U21	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U22	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U23	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U24	1820-1210	1	IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
U25	1820-1430	2	IC, DIGITAL SN74LS161N.	01295	SN74LS161N
U26	1820-1199	4	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U27	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U28	1820-1074	1	IC-DIGITAL SN74128N TTL QUAD 2 NOR	01295	SN74128N
U29	1820-0509	2	IC-DIGITAL MC1488L DTL QUAD LINE	04713	MC1488L
U31	1820-1430		IC, DIGITAL SN74LS161N	01295	SN74LS161N
U32	1820-1213	2	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U33	1820-1348	1	IC-DIGITAL MM5307 PMOS	27014	MM5307N
U34	1820-1195	1	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U35	1820-1208	2	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U36	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U37	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U38	1820-1422	1	IC-DIGITAL SN74LS122N TTL LS	01295	SN74LS122N
U39	1820-1201	1	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U41	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U42	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U43	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U44	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U45	1820-1196	1	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
U46	1820-1215	1	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U47	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U48	1820-1208		IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U49	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U51	1820-1219	1	IC-DIGITAL TR1602B TTL*	0026W	TR1602B
U58	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U59	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U110	1820-0535	1	IC-DIGITAL SN754518P TTL DUAL 2 AND	01295	SN754518P
U210	1820-0799	2	IC-DIGITAL SN754528P TTL DUAL 2 NAND	01295	SN754528P
U310	1820-0799		IC-DIGITAL SN754528P TTL DUAL 2 NAND	01295	SN754528P
U410	1990-0429	2	OPTO-ISOLATOR LED-IC GATE IF=10MA-MAX	28480	1990-0429
U411	1990-0429		OPTO-ISOLATOR LED-IC GATE IF=10MA-MAX	28480	1990-0429
U412	1990-0494	2	OPTO-ISOLATOR LED-PDIO/XSTR IF=20MA-MAX	28480	1990-0494
U510	1820-1416	1	IC-DIGITAL SN74LS14N TTL LS HEX 1 INV	01295	SN74LS14N
U511	1990-0494		OPTO-ISOLATOR LED-PDIO/XSTR IF=20MA-MAX	28480	1990-0494
U512	1820-0509		IC-DIGITAL MC1488L DTL QUAD LINE	04713	MC1488L