HP 13255

DISPLAY TIMING/CONTROL MODULE

Manual Part No. 13255-91267

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NOTE: This document is part of the 2647F DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION

The Display Timing/Control module is one printed circuit assembly (PCA) of a two PCA set. The second PCA is the Display Memory/DMA module (02640-60250). This board set interfaces into the terminal environment by performing the functions of display memory management, CRT drive signal generation, and video generation.

The Display Timing/Control module replaces two separate boards in the first generation 264X hardware (display timing and display control). Resident in this module are a CRT controller, recirculating line buffers, a character ROM, and video generation circuitry. This module takes the ASCII character information and enhancement data from the Display Memory/DMA module and creates a video bit stream and synchronized drive signals to be sent to the sweep PCA.

The Display Timing/Control module takes care of all tasks associated with drive signal generation, video generation, and informs the Display Memory/DMA module of such screen related events such as end-of-data row, start of frame, and refresh timing. Each data row of ASCII characters and associated enhancements are loaded into the recirculating line buffers under the control of the Display Memory/DMA module. Once the buffers are loaded with an entire row of characters, the data is recirculated fifteen times (once for each scan line per data row), and the ASCII data is used to "look-up" a bit pattern associated with each character in each scan line. The parallel video data coming out of the character ROM is serialized, dot shifted if necessary, summed with graphics, and subjected to any active character enhancements. Cursor generation is also taken care of by the Display Timing/Control module.

A private interface to the Display Memory/DMA module is provided over a topplane through which the two boards communicate timing information and memory data.

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2.0 OPERATING PARAMETERS

A summary of operating parameters for the Display Timing/ Control module is contained in tables 1.0 through 6.1.

Table 1.0 Physical Parameters

PART NUMBER	NOMENCLATURE	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60267	Display Timing/Control PCA	12.9 x 4.0 x 0.5	0.48

NUMBER OF BACKPLANE SLOTS REQUIRED: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 2.811 (percent per 100 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 1.7 A	@ 50. mA	@ 75. mA	N/A
115 volts ac		220 volts ac	
N/A		N/A	
Clock Frequency: 21.34 MHz			

Table 4.0 Switch Definitions

PCA Designation	Function	
	Closed	Open
Display Timing/ Control Module		
HZ	50 Hz mode	60 Hz mode
IV	Full screen inverse video	Normal mode
DT	Normal mode	Display tests invoked
A1,A2,A3, U1,U2,U3	These six switches allow any properly programmed character set to be displayed according to its correct format. See the text section on character set selection for further details.	
C1,C2,C3	These three switches allow the three "hardwired" alternate character sets in the character ROM to be accessed by any of the "A", "B", or "C" alternate character set select codes. See the text section on character set selection for further details.	

Table 5.0 Connector Information (Display Timing/Control PCA)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{ADDR0}$	Negative True, Address Bit 0
-6	$\overline{ADDR1}$	Negative True, Address Bit 1
-7	$\overline{ADDR2}$	Negative True, Address Bit 2
-8	$\overline{ADDR3}$	Negative True, Address Bit 3
-9	$\overline{ADDR4}$	Negative True, Address Bit 4
-10	$\overline{ADDR5}$	Negative True, Address Bit 5
-11	$\overline{ADDR6}$	Negative True, Address Bit 6

Table 5.1 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P1, PIN 12	$\overline{ADDR7}$	Negative True, Address Bit 7
-13	$\overline{ADDR8}$	Negative True, Address Bit 8
-14	$\overline{ADDR9}$	Negative True, Address Bit 9
-15	$\overline{ADDR10}$	Negative True, Address Bit 10
-16	$\overline{ADDR11}$	Negative True, Address Bit 11
-17	$\overline{ADDR12}$	Negative True, Address Bit 12
-18	$\overline{ADDR13}$	Negative True, Address Bit 13
-19	$\overline{ADDR14}$	Negative True, Address Bit 14
-20	$\overline{ADDR15}$	Negative True, Address Bit 15
-21	$\overline{I/O}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal

Table 5.2 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6

Table 5.3 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P1, PIN N	$\overline{BUS7}$	Negative True, Data Bus Bit 7
-P	$\overline{WRITE}$	Negative True, Read/Write Type Cycle
-R	$\overline{ATN2}$	Negative True, CTU and Polled Interrupt Request
-S	$\overline{WAIT}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	ADDR16	Positive true, Address Bit 16
-W	ADDR17	Positive True, Address Bit 17
-X	ADDR18	Positive True, Address Bit 18
-Y	$\overline{REQ}$	Negative True, Request (Bus Data Currently Valid)
-Z	ATN	Negative True, Data Comm Interrupt Request

Table 5.4 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	GND	Ground
-2	I/O STROBE	Cursor Control Strobe from Display Mem/DMA
-3	$\overline{103}$	Graphics Sync. signal--Character 103
-4	DSPCLK	Positive True form of 21.34 Mhz Dot clock
-5	$\overline{\text{I/O SELECT}}$	Negative True--Cursor control select line
-6	$\overline{AB6}$	Negative True--ASCII Bit 6
-7	$\overline{AB5}$	Negative True--ASCII Bit 5
-8	$\overline{AB4}$	Negative True--ASCII Bit 4
-9	$\overline{AB3}$	Negative True--ASCII Bit 3
-10	$\overline{AB2}$	Negative True--ASCII Bit 2
-11	$\overline{AB1}$	Negative True--ASCII Bit 1

Table 5.5 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, PIN 12	$\overline{AB0}$	Negative True--ASCII Bit 0
-13	GND	Signal Ground
-14	$\overline{MEMCYC}$	Clock with ~840 nsec. period defining display memory cycles
-15	EDROW	End of Data Row Pulse
-16	SHFTCLK	Line Buffer Load Clock
-17	Qa	Enhancement Alignment Clock
-18	$\overline{SLOAD}$	Negative True, (Low) Indicates that CRT Controller self-load is in progress
-19	VSCLK	Video Shift Clock--Line Buffer Display Clock
-20	$\overline{XBITS2}$	External Video Bit Stream (Graphics)
-21	GND	Signal Ground
-22	$\overline{XBITS1}$	External Video Bit Stream (Unused)

Table 5.6 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	$\overline{\text{DSPCLK}}$	Negative True form of 21.34 Mhz dot clock
-B	GND	Signal Ground
-C	$\overline{\text{D2}}$	Graphics Sync. signal--Dot 2
-D	GND	Signal Ground
-E	ZERO	Start Top-of-Frame Pulse
-F	CHARCLK	Character Rate Clock
-H	$\overline{\text{CHARCLK}}$	Character Rate Clock (negative true)
-J	VBLANK	Vertical Blanking--Graphics Sync. Signal
-K	EB5	Positive True--Enhancement Bit 5
-L	EB4	Positive True--Enhancement Bit 4
-M	EB3	Positive True--Enhancement Bit 3
-N	EB2	Positive True--Enhancement Bit 2
-P	EB1	Positive True--Enhancement Bit 1

Table 5.7 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, PIN R	EB0	Positive True--Enhancement Bit 0
-S	HSYNC	Horizontal Sync from CRT Controller
-T	GND	Signal Ground
-U	I/O BIT 5	Status Bit from Display Memory/DMA module
-V	I/O BIT 6	Statue Bit from Display Memory/DMA module
-W	DMAROW=CURROW	(high) indicates that the cursor is on the same character row as the DMA module
-X	SHFTEN	Enable signal for Line Buffer Loading
-Y	GND	Signal Ground
-Z	$\overline{\text{RFSHEN}}$	(low) indicates that Display Memory refresh is enabled

Table 5.8 Connector Information (Display Timing/Control PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P4, PIN 1	VIDEO	Serial Video Bit Stream
-2	$\overline{BUF}$ $\overline{HLF}$ $\overline{BRT}$	Negative True--Half Bright Enhancement signal
-3	GND	Signal Ground
-4	VDR	Vertical Drive
-5	HDR	Horizontal Drive
-6	GND	Signal Ground

Table 6.0 Module Bus Pin Assignments-Display Timing/Control PCA

Function Performed: Set Cursor Y Position
Turn Display On/Off
Turn DMA On/Off
Invoke Skipeol and Mayeop Modes

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0111)

Function Specifier: ADDR5 = 1

Data Bus Bit Interpretation:

B7 (high) Indicates Display Off

B6 (high) Indicates DMA Off

B5 (high) Indicates Skipeol or Mayeop mode may be invoked

B4 Cursor Y Position $\overline{BIT4}$

B3 Cursor Y Position $\overline{BIT3}$

B2 Cursor Y Position $\overline{BIT2}$

B1 Cursor Y Position $\overline{BIT1}$

B0 Cursor Y Position $\overline{BIT0}$

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
1	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.1 Module Bus Pin Assignments-Display Timing/Control PCA

Function Performed: Set Cursor X Position Turn Display Memory Refresh On/Off	Value	Bus Signal
	X	ADDR 15
	X	ADDR 14
	X	ADDR 13
Poll Bit: Not Applicable	X	ADDR 12
	0	ADDR 11
Module Address: (ADDR 11,10,9,4) = (0111)	1	ADDR 10
	1	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
	X	ADDR 7
	X	ADDR 6
	0	ADDR 5
	1	ADDR 4
	X	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
B7 (high) Indicates Display Memory Refresh Off		
	B7	BUS 7
B6 Cursor X Position $\overline{BIT6}$	B6	BUS 6
	B5	BUS 5
B5 Cursor X Position $\overline{BIT5}$	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
B4 Cursor X Position $\overline{BIT4}$	B1	BUS 1
	B0	BUS 0
B3 Cursor X Position $\overline{BIT3}$		
	1=Logical 1=Bus Low	
B2 Cursor X Position $\overline{BIT2}$	0=Logical 0=Bus High	
	X=Don't Care	
B1 Cursor X Position $\overline{BIT1}$		
B0 Cursor X Position $\overline{BIT0}$		

3.0 FUNCTIONAL DESCRIPTION

Refer to the block diagram (Figure 1), schematic diagram (Figures 2,3), timing diagram (Figures 4-10), component location diagram (Figure 11), and parts list located in the appendix.

3.1 DRIVE SIGNAL GENERATION

3.1.1 Four signals are generated by the Display Timing/Control module and sent to the sweep module. They are the video bit stream (VIDEO), a half bright enhancement signal (BUF HLF BRT), horizontal drive (HDR), and vertical drive (VDR).

3.1.2 Horizontal drive occurs once per scan line and causes the sweep board to perform horizontal left-to-right scans. This pulse is repetitive with an approximate 44. usec period. HDR is normally low, and goes high during characters twenty four through eighty.

3.1.3 Vertical drive occurs once per frame and causes vertical retrace by "resetting" an integrator in the sweep module. This signal coincides with the pertinent line rate (i.e. 50 Hz or 60 Hz) to prevent annoying perterbations of the CRT display. VDR is normally high, and goes low during vertical retrace.

3.1.4 Scan line and frame timing are determined through the following constraints:

60 Hz--one frame = 16.67 msec = 380 scan lines
380 scan lines = 24 character rows (data rows) of 15 scan lines each + 20 scan lines for vertical retrace

50 Hz--one frame = 20.0 msec = 456 scan lines
456 scan lines = 24 data rows of 15 scan lines each + 96 scan lines for vertical retrace.

3.2 CRT CONTROLLER

3.2.1 The CRT controller used in the Display Timing/Control module is a SMC 5027 (TMS 9927). It is a programmable device with nine internal registers that configure the chip to produce the proper modulus counts for scan lines per data row (R0 to R3--15), characters per data row (H0 to H6--104), and data rows per frame (DR0 to DR4--24). These registers also control the synchronization of the drive signal outputs HSYNC, VSYNC, and BLANK, and also control the positioning of the cursor within the frame (CRV). For a complete description of the registers see an SMC or TI data sheet.

3.2.2 The CRT controller registers are loaded with the proper data at power on under the control of the power on and two millesecond timer circuit block (see hardware description section). Note that the drive signal outputs of this chip are totally unlike those needed by the 264X sweep modules and hence are used as general timing signals. The actual drive signals are generated through hardware external to the CRT controller.

3.3 CURSOR CONTROL

3.3.1 Cursor control is accomplished through the internal registers of the aforementioned CRT controller. The terminal processor positions the cursor through two I/O ports, one for column and one for row. These port accesses are decoded and synchronized in the Display Memory/DMA module and a select line and CRT controller strobe ($\overline{\text{I/O SELECT}}$ and I/O STROBE) are sent over the topplane.

3.4 RECIRCULATING LINE BUFFERS

3.4.1 The recirculating line buffers are used to store one character row of information at a time. When an even character row is being displayed, U36-U39 are being recirculated every scan line, and U26-U29 are being loaded byte serially by the Display Memory/DMA module. When the display switches to the next row (an odd one), the reverse is true (i.e. U26-U29 are recirculated and U36-U39 are loaded). Note that these line buffers contain not only ASCII character data, but character by character enhancements as well. These enhancements include two bits for character set select, and one bit each for half bright, underline, inverse video, and blinking.

3.5 CHARACTER ROM AND CHARACTER SET SELECTION

3.5.1 The character ROM resident in this module is an 8Kx8 device and replaces five first generation character ROMs, which were each 1Kx8 or 1Kx9. The three-eighths of the ROM leftover are utilized to implement lower case blanking for 64 character sets and display tests. The character sets available in the 1818-1597 character ROM are as follows:

1) lower case English (and control codes),
2) upper case English,
3) math,
4) line drawing or micro-vector, and
5) large character.

3.5.2 Lower case blanking indicates that any reference to lower case ASCII codes (00 to 1F and 60 to 7F) while a 64 character set is invoked results in blanks being displayed on the CRT.

3.5.3 Two display tests are implemented with the character ROM and the character set select PROMs U21 and U22. These two are full screen crosshatch, and alternating @'s and del's. They are invoked with the switches labeled "DT" and "U3". When "DT" is closed, "U3" has a meaning which is discussed in depth in the hardware description. If "DT" is open, "U3" determines which display test is in effect. Note that even though the display is totally changed when display tests are invoked, this is strictly a hardware feature, and the original display will return unaltered when the display test conditions are removed.

3.6 DOT HALF SHIFT AND DOT REPEAT FUNCTIONS

3.6.1 The purpose of dot half shift is to effectively increase the resolution of the alpha display through the creation of "interstitial" dots. See any terminal character documentation for further details. Dot repeat functions are necessary to implement nine bit wide characters (i.e. line drawing and large characters) in an eight bit ROM. Nine bits of display are generated from eight bits of data through repeating the first bit of ROM data twice on the display.

3.6.2 Dot shift and dot repeat functions are all performed within a single parallel to serial shift register (U44). Dot shift is enabled by inverting the display clock "on the run", and dot repeat is accomplished by inhibiting certain clock edges to the shift register.

4.0 HARDWARE DESCRIPTION

4.1 POWER ON AND 2 MSEC TIMER FOR CRT CONTROLLER SELF LOAD CIRCUITRY

4.1.1 The circuit composed of one-half of U69, Q4, CR1, R27 and R28 implements a "power on preset" that is independent of five volt rail rise time and changes state once and only once upon the first rising edge of P1-D ($\overline{\text{RESET}}$). When the five volt rail is well below the zener voltage of CR1 (4.22v), Q4 is "off" and U69-10 is pulled low by R27. As the zener voltage is approached and finally achieved, a reverse current flows through CR1 and Q4 is driven to saturation, removing the preset condition from U69-10. This preset pulse is removed when the five volt rail is approximately 4.0 volts given the bias component values shown. Note that this circuit is dependent upon the theory that although TTL specs are not guaranteed with a rail below 4.75 volts, they are, in actuality, functional in a "static" sense at voltages well below that. Devices tested (74LS74's) exhibited functionality at 3.0 volts and below at room temperature, that value rising slightly as the temperature is dropped.

4.1.2 The CRT controller performs a "self load" during power on. This function takes approximately one msec. The SMC guys said that the CRT controller requires 256 clocks to U54-12 for each internal register of the controller. The circuit composed of R25, R26, Q3, and C33 provide a delay of approximately two msec. to allow this self load to occur correctly. When the RC circuit times out after U69-8,9 changes state, the self load address to the CRT controller is removed (U54-40), the self load data PROM (U62) is disabled, the data bus buffer (U56) is enabled, and the CRT controller starts counting and producing the SYNC outputs.

4.2 CRT CONTROLLER SELF LOAD STROBE GENERATOR

4.2.1 The self load strobe generating circuitry allows the CRT controller to be strobed (U54-9) by two sources. I/O STROBE (P3-2) strobes the CRT controller during normal cursor control. U712-5 and VSCLK (P3-19) are used to generate a single low going pulse to U54-9 immediately after power on/reset goes high for the first time. This strobe begins the power on self load sequence described above. The first rising edge of U510-4 after power on/reset causes U712-6 to change state and shuts down the self load strobe generator permanently.

4.2.2 Note that VSCLK is a repetitive clock and U54-9 is stobed continually until power on/reset, at which point one more strobe is generated to guarantee that the CRT controller self load sequence is begun.

4.3 CRT CONTROLLER SELF LOAD DATA PROM

4.3.1 The CRT controller self load data PROM contains the data necessary to configure the CRT controller for both 60 Hz and 50 Hz modes. Switch four of switch bank two (HZ) is left open for 60 Hz and closed for 50 Hz. During CRT controller self load, the raster line counter outputs (R0-R3) count from zero to fifteen and one half of the PROM is read. The first nine values read are latched internally within the CRT controller. The latched data configures the CRT controller and determines the mode in which it operates.

4.3.2 The following is a description of the contents of the self load data PROM part number 1816-1487. See a data sheet on the CRT controller for further details. Note that the PROM data is positive true except for bit seven, which is negative true.

ADDR. (HEX)	MODE	CONTENTS (HEX)	MEANING
00	50 Hz	E7	104 Character Times/Row
01	"	CB	Non-interlaced Mode 9 Character Time HSYNC Pulse 3 Character Time "Front Porch"
02	"	F5	15 Scan Lines/Row 80 Displayed Characters/Row
03	"	97	No skew characters 24 Rows/Frame
04	"	E4	456 Scan Lines/Frame
05	"	88	VSYNC Pulse Occurs 8 Scan Lines Before Video Foretrace
06	"	97	Row 24 is Last Row of Frame
07	"	80	Cursor Column Equals 0
08	"	80	Cursor Row Equals 0
09	"	FF	Unused
0A	"	FF	"
0B	"	FF	"
0C	"	FF	"
0D	"	FF	"
0E	"	FF	"
0F	"	FF	"
10	60 Hz	E7	Same as 50 Hz
11	"	CB	" " " "
12	"	F5	" " " "
13	"	97	" " " "
14	"	BE	380 Scan Lines/Frame
15	"	88	Same as 50 Hz
16	"	97	" " " "
17	"	80	" " " "
18	"	80	" " " "
19	"	FF	Unused
1A	"	FF	"
1B	"	FF	"
1C	"	FF	"
1D	"	FF	"
1E	"	FF	"
1F	"	FF	"

4.4 CRT CONTROLLER AND CURSOR ADDRESS AND DATA SELECTORS

4.4.1 The CRT controller is an SMC 5027 or a TMS 9927. Look elsewhere in this text and in a data sheet for more information.

4.4.2 The addresses for the CRT controller internal registers are controlled by inputs A0-A3 (pins 39,40,1,2). Following are the addresses pertinent to the CRT controller performance in this module:

ADDRESS A3,A2,A1,A0	FUNCTION
1111	CRT controller self load
1101	cursor row select
1100	cursor column select

4.4.3 Note that there are pullup resistors on all inputs of the CRT controller. This is due to the required Vih (minimum high input voltage) of the contoller.

4.4.4 Note also that data bit seven is active only during CRT controller self load and is forced low forever after. U25-1,2,3,11,12,13 mask imbedded status bits in the cursor row I/O byte.

4.5 DATA BUS BUFFER

4.5.1 U56 buffers data from the backplane onto this module. During CRT controller self load, U56 is held disabled by SELFLOAD (U411-10). When self load is complete, U56 is enabled and stays enabled forever after.

4.6 REFRESH ENABLE FLIP-FLOP

4.6.1 The refresh enable flip-flop provides a means by which memory refresh on the Display Memory/DMA module can be halted. An I/O write to the cursor column with the most significant bit set will turn refresh off and a write with bit seven not set will turn it on.

4.6.2 This feature is presently not used by any old software or the 2647F software, but has been provided in case extensive display memory testing becomes necessary.

4.7 VERTICAL RETRACE SYNC CIRCUIT

4.7.1 The circuit composed of U69-FF#1 and U45-11,12,13 synchronizes turning the display on during vetical retrace. A bit imbedded in the cursor row byte (bit seven) causes the display to be turned on and off. When the display is off, U69-4 is held low and display is turned off by U69-6, U69-5 is high and therefore P3-V (I/O BIT 6) is high. P3-V being high causes the DMA machine to stop DMA cycles.

4.7.2 When a write to cursor row with bit seven not set occurs, U57-19 goes high and the following VBLANK (U69-3) will turn the display on and restart the DMA machine (i.e. P3-V will go low).

4.8 CURSOR ROW AND DMA ROW COMPARISON CIRCUITRY

4.8.1 Two software modes described elsewhere, SKIPEOL and MAYEOP, need information concerning the relative positions of DMA and processor action within the display memory linked list. In particular, when the DMA row is the same as the cursor row, the display memory structure can be misinterpretted by the DMA state machine. The circuitry composed of U57, U710,U610, and 1/2 of U67 informs the DMA state machine in the Display Memory/DMA module when the DMA row equals cursor row.

4.8.2 The cursor row information is supplied by the processor during I/O writes to cursor row, and is stored in U57. The DMA row information is generated by U710, and eight bit counter that is reset by ZERO (P3-E) at the beginning of each frame, and increments by one at the end of each data row. U610 is a four bit comparator and along with U67-1,2,3,4,5,6 all five bits of the row values are compared. U610-6 is the final result of the comparison. This value is a one when the rows are equal and a zero when unlike. U610-6 is sampled by P3-F (CHARCLK) through U412-3,2 and sent over the topplane (P3-W) to the Display Memory/DMA module.

4.9 RASTER LINE DECODER

4.9.1 The raster line decoder (U52) monitors the raster line outputs of the CRT controller (R0-R3) and creates four output signals. These outputs are RL0, RL11, RL11 OR RL12, AND RL14. RL0 is used to

ADD FROM #TCL

create the signal EDROW (end of data row) by being summed with the character decoder output CHAR3 or CHAR4 (U66-11). RL11 is used to create an underline under enhanced characters. RL11 or RL12 is used to create the alphanumeric cursor. RL14 is used to end each frame and start vertical retrace. RL14 is summed with DATA ROW 23 (U72-6) at U612-8,9,10 and creates a signal that is high only on the last scan line of foretrace.

4.9.2 The contents of the raster line decoder PROM are as follows:

HP PART NUMBER: 1816-1488
USED ON ASSEMBLY 02640-60267 (DISPLAY TIMING/CONTROL) U52
FUNCTION: RASTER LINE DECODER
OUTPUT DEFINITION:

01--RASTER LINE ZERO	(POSITIVE TRUE)
02--RASTER LINE ELEVEN	(" ")
03--RASTER LINE ELEVEN OR TWELVE	(" ")
04--RASTER LINE FOURTEEN	(" ")

05 THROUGH 08 ARE UNUSED

ROM GENERIC PART NUMBER: 7603A (32X8)
ROM CONTENTS:

```
$A0000.
01,00,00,00,00,00,00,00,00,00,00,06,04,00,08,00,
FF,FF,FF,FF,FF,FF,FF,FF,FF,FF,FF,FF,FF,FF,FF,FF,

SUM=1003
```

4.9.3 Note that the data is displayed with Data I/O's Model 19 Prom Programmer Format.

4.10 CHARACTER DECODER

4.10.1 The character decoder (U66) monitors the character counter outputs of the CRT controller (H0-H6) and creates four output signals. These outputs are HORIZONTAL DRIVE, CHAR3 or CHAR4, VIDEO SHIFT ENABLE, AND $\overline{103}$.

4.10.2 HORIZONTAL DRIVE is synchronized to the character boundary by CHARCLK (P3-F) and U311-13,14,15 to create the HDR signal used by the sweep module.

4.10.3 CHAR3 or CHAR4 goes high during characters three and four and is used to create the signal EDROW by being summed with RL0 at U73-8,9,10.

4.10.4 VIDEO SHIFT ENABLE is a representation of horzontal foretrace and retrace, shifted in time by two character periods to account for pipelining in the Display Timing/ Control module. VIDEO SHIFT ENABLE is high for characters "-2" to 78 and low for the duration of the raster line. This signal goes over the topplane (P3-X==SHFTEN) to the Display Memory/DMA module and allows the creation of the VIDEO SHIFT CLOCK (VSCLK==P3-19) which is used by the recirculating line buffers in the Display Timing/Control module.

4.10.5 $\overline{103}$ is a graphics synchronization signal that goes over the topplane (P3-3) to the graphics module where it is summed with the signal D2 from the Display Memory/DMA module and used to create the signal 103.D2 for graphics operation.

4.10.6 The contents of the character decoder are as follows:

HP PART NUMBER: 1816-1483
USED ON ASSEMBLY 02640-60267 (DISPLAY TIMING/CONTROL) U66
FUNCTION: CHARACTER COUNT DECODER
OUTPUT DEFINITION:
01--HORIZONTAL DRIVE (POSITIVE TRUE)
02--CHARACTERS 3 OR 4 (" ")
03--VIDEO SHIFT ENABLE (" ")
04--CHARACTER 103 (NEGATIVE TRUE)
ROM GENERIC PART NUMBER: 7611A (256X4)
ROM CONTENTS:

```
$A0000,
C,C,C,E,E,C,C,C,C,C,C,C,C,C,C,C,
C,C,C,C,C,C,C,D,D,D,D,D,D,D,D,D,
D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,
D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,
D,D,D,D,D,D,D,D,D,D,D,D,D,D,9,9,
8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,
8,8,8,8,8,8,4,C,C,C,C,C,C,C,C,C,
C,C,C,C,C,C,C,C,C,C,C,C,C,C,C,C,

$A0080,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,
F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,F,

  SUM=0D55
```

4.11 CURSOR EXTEND ONE-SHOT

4.11.1 The cursor extend one-shot (U112) is used to prevent the "galloping" cursor effect when the cursor is moved continuously horizontally or vertically. Every positioning of the cursor is associated with a pulse on P3-2 (I/O STROBE). This pulse triggers U112 and causes the cursor blink to be masked "on" for approximately 300 msec.

4.12 SYNCHRONIZATION LATCH

4.12.1 The synchronization latch (U311) samples the outputs and "derived" outputs of the CRT controller and allow those signals to change state only on character boundaries (i.e. as a result of CHARCLK--P3-F).

4.13 VERTICAL DRIVE SIGNAL GENERATION

4.13.1 The vertical drive generation circuitry has been designed to be compatible with both the 264X sweep module and the 2647F sweep module (basically a revision of the 262X sweep module). Another important feature of this circuit block is that changing between 60 Hz drive mode and 50 Hz drive mode is accomplished through changing the position of switch "HZ" while the power is off.

4.13.2 The requirements of the two sweep modules differ so substantially that two distinct mode of operation are required. U611 (LS51--dual AND-OR-INVERT) provides for these two modes by allowing separate and distinct trigger events for 50 Hz and 60 Hz modes.

4.13.3 For 60 Hz operation, vertical drive (VDR) is brought low as a result of P3-J (VBLANK) going high. It is returned to the high state ten raster lines before video foretrace as a result of the CRT controller output VSYNC (U54-11). These ten raster lines are required for the 2647F sweep module to allow second order effects to "smooth" out.

4.13.4 For 50 Hz operation, VDR is brought low 32 raster lines into vertical retrace and returned high 10 raster lines before video foretrace.

4.13.5 U711 (FF#2) samples the output of U612-8 every raster line and changes state high when the last raster line of foretrace is reached. This change of state removes the "clear" condition from U512 and allows this eight bit counter to begin counting the raster lines of vertical retrace. This counter is decoded to form three pertinent outputs--32, $\overline{20}$, and $\overline{96}$. 32 (U512-10) starts 50 Hz VDR. $\overline{20}$ ($\overline{U512\text{-}5}$.AND.$\overline{U512\text{-}11}$) ends 60 Hz VBLANK. $\overline{96}$ ($\overline{U512\text{-}10}$.AND.$\overline{U512\text{-}9}$) ends 50 Hz VBLANK.

4.14 RECIRCULATING LINE BUFFERS

4.14.1 The eight recirculating line buffers are used to store one character row of information for video display output while allowing another row to be "created", or fetched from display memory. These eight parts are TMS3120's, 80X4 shift registers. They are MOS parts and have strange clock requirements--see a data sheet for more details.

4.14.2 U36-U39 is the even row bank of shift registers and U26-U29 is the odd bank. DRZERO (U51-7) selects the bank for vieo display through U210.

4.14.3 While an odd row is being displayed on the CRT, U36-U39 are being loaded with character information over the topplane through the action of SHFTCLK (P3-16) from the Display Memory/DMA module. The recirculate pins of the shift registers (2, 5, 9, 14) are held low and the registers are clocked exactly eighty times. This action loads these shift registers with the data for the next character row on the CRT.

4.14.4 During this loading action, the data contained in U26-U29 is being shifted exactly eighty times per raster line. Since the recirculate pins on the shift registers are held high during video display the output is fed back to the input, and the character cell information within the shift registers remains stationary through all fifteen raster lines of each character row.

4.14.5 When the end of a character row is reached, DRZERO changes states and the bank of shift registers that were displayed are now loaded, whereas the bank that was loaded is now displayed.

4.15 ODD/EVEN CLOCK SELECTOR

4.15.1 U210 controls the loading/recirculating action of the recirculating line buffers. U210 is simply a multiplexer with two clock inputs and two static inputs. These inputs are connected in a different order for each input bank. As DRZERO changes states, the four inputs are routed to the output pins in different order, thereby controlling which clock and recirculate level go to which bank of shift registers.

4.15.2 VSCLK (P3-19 video shift clock) is routed to the shift register bank that has the recirculate pins held high, and SHFTCLK (P3-16 shift clock from DMA) is impressed upon the bank with the recirculate pins low.

4.16 LINE BUFFER OUTPUT SELECTORS

4.16.1 The line buffer output selectors are multiplexing latches. Depending on the state of U210-7 (EVEN RECIRC.), the output of one bank of shift registers will be selected and latched every clock cycle of P3-H.

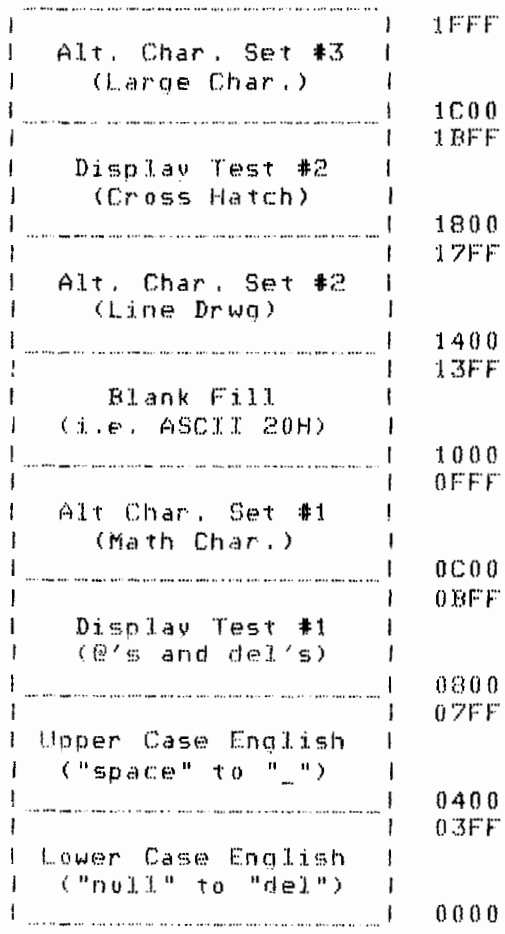
4.17 8K X 8 CHARACTER ROM

4.17.1 The 8K X 8 character ROM resident in this module (1818-1597) contains four complete character sets plus two display display test patterns.

4.17.2 The address lines to the ROM consist of four raster line counter bits, six ASCII bits, one upper/lower case bit, and two character set select bits. The raster line and character set select bits are positive true. The ASCII bits are negative true.

4.17.3 The chip enable is low true and is enabled only during the eighty foretrace character times. The outputs of the ROM are pulled high so that during the disabled retrace period, the "video output" of the character ROM is held "off".

4.17.4 The following is a memory map of the standard character ROM (1818-1597):



4.18 CHARACTER SET SELECT LOGIC

4.18.1 The character set select logic consists of some switches, two fast bipolar PROM's, and one nand gate (U11). These switches provide the "hardwired" character ROM with psuedo-soft capabilities.

4.18.2 Switches C1 to C3 map the character set select bits (U48-13,12) into any of the alternate character sets resident in the ROM.

4.18.3 Switches C1, C2, and C3 determine character set selection according to the following chart:

(C=closed, O=open)

Switch position C1	C2	C3	Logical Character Set	Set Actually Selected
C	C	C	A	Math
O	O	C	B	Line Drawing
	or		C	Large Character
O	O	O		
			A	Math
C	C	O	B	Large Character
			C	Line Drawing
			A	Line Drawing
C	O	C	B	Math
			C	Large Character
			A	Line Drawing
C	O	O	B	Large Character
			C	Math
			A	Large Character
O	C	C	B	Math
			C	Line Drawing
			A	Large Character
O	C	O	B	Line Drawing
			C	Math

4.18.4 Switches A1 to A3 determine whether the alternate character sets are treated as dot shift or dot repeat characters. An open switch indicates that the character ROM data will be treated as dot-shift data and conversely, a closed switch will cause the ROM data to be displayed under dot-repeat format.

4.18.5 Note that the mode selection output (U21-10) corresponds to the actual set selected and not necessarily to the logical A, B, or C inputs to the PROM. This means that these three switches correspond to defining the display mode of the alternate character sets within specific address ranges of the character ROM. The following truth table explains switches A1, A2, and A3:

Character ROM Address Range	Switch Position A1	A2	A3	Dot-shift (DS), or Dot-repeat (DR) mode
0000 to 07FF	X	X	X	DS
0C00 to 0FFF	0	X	X	DR
	1	X	X	DS
1400 to 17FF	X	0	X	DR
	X	1	X	DS
1C00 to 1FFF	X	X	0	DR
	X	X	1	DS

4.18.6 Switches U1 to U3 enable the character ROM to be programmed with 128 character alternate character sets as well as the 64 character alternate character sets the standard ROM contains. Note that expanding alternate character set #2 to 128 characters will destroy the ASCII blank fill in the character ROM address range of 1000 to 13FF. This will disrupt the proper display of lowercase input to 64 character alternate character sets and should be avoided if possible. Also note that expanding alternate character sets #1 and #3 to 128 character sets will delete the display test patterns resident in the ROM.

4.18.7 The switches U1, U2, and U3 correspond to the logical A, B, or C laternate character set selection and NOT to any specific address range within the character ROM. A closed "U" switch will cause display of a 128 character alternate character set, and an open switch will restrict alternate character set display to 64 characters.

4.18.8 These "U" switches perform according to the following truth table:

PROM INPUTS								PROM OUTPUTS			
										U22-	
CS0	CS1	$\overline{AB5}$	$\overline{AB6}$	U1	U2	U3	DT	-9	-10	-11	-12
A0	A1	A2	A3	A4	A5	A6	A7	O4	O3	O2	O1
0	0	0	0	X	X	X	0	0	0	0	0
0	0	1	0	X	X	X	0	1	0	0	0
0	0	0	1	X	X	X	0	1	0	0	0
0	0	1	1	X	X	X	0	0	0	0	0
1	0	0	0	0	X	X	0	0	0	0	0
1	0	0	0	1	X	X	0	1	0	0	0
1	0	1	0	X	X	X	0	1	0	0	0
1	0	0	1	X	X	X	0	1	0	0	0
1	0	1	1	0	X	X	0	0	0	0	0
1	0	1	1	1	X	X	0	0	1	0	1
0	1	0	0	X	0	X	0	0	0	0	0
0	1	0	0	X	1	X	0	1	0	0	0
0	1	1	0	X	X	X	0	1	0	0	0
0	1	0	1	X	X	X	0	1	0	0	0
0	1	1	1	X	0	X	0	0	0	0	0
0	1	1	1	X	0	X	0	0	1	0	1
1	1	0	0	X	X	0	0	0	0	0	0
1	1	0	0	X	X	1	0	1	0	0	0
1	1	1	0	X	X	X	0	1	0	0	0
1	1	0	1	X	X	X	0	1	0	0	0
1	1	1	1	X	X	0	0	0	0	0	0
1	1	1	1	X	X	1	0	0	1	0	1
X	X	X	X	X	X	0	1	0	1	1	0
X	X	X	X	X	X	1	1	0	1	0	0

4.18.9 The following are descritions of the contents of the two character set select PROM's (U21 and U22):

HP PART NUMBER: 1816-1490
USED ON ASSEMBLY 02640-60267 (DISPLAY TIMING/CONTROL) U21
FUNCTION: ALTERNATE CHARACTER SET SELECT PROM
OUTPUT DEFINITION:

O1--CHARACTER SET BIT0	(POSITIVE TRUE)
O2--CHARACTER SET BIT1	(" ")
O3--DOT SHIFT CHARACTER SET	(" ")
O4--DOT REPEAT CHARACTER SET (UNUSED)	(" ")

ROM GENERIC PART NUMBER: 7611A (256X4)
ROM CONTENTS:

```
$A0000.
7,A,9,8,7,8,A,9,7,9,A,8,7,A,9,8,
7,A,8,9,7,8,9,A,7,9,8,A,7,A,9,8,
7,6,9,8,7,8,6,9,7,9,6,8,7,6,9,8,
7,6,8,9,7,8,9,6,7,9,8,6,7,6,9,8,
7,A,5,8,7,8,A,5,7,5,A,8,7,A,5,8,
7,A,8,5,7,8,5,A,7,5,8,A,7,A,5,8,
7,6,5,8,7,8,6,5,7,5,6,8,7,6,5,8,
7,6,8,5,7,8,5,6,7,5,8,6,7,6,5,8,

$A0080.
7,A,9,4,7,4,A,9,7,9,A,4,7,A,9,4,
7,A,4,9,7,4,9,A,7,9,4,A,7,A,9,4,
7,6,9,4,7,4,6,9,7,9,6,4,7,6,9,4,
7,6,4,9,7,4,9,6,7,9,4,6,7,6,9,4,
7,A,5,4,7,4,A,5,7,5,A,4,7,A,5,4,
7,A,4,5,7,4,5,A,7,5,4,A,7,A,5,4,
7,6,5,4,7,4,6,5,7,5,6,4,7,6,5,4,
7,6,4,5,7,4,5,6,7,5,4,6,7,6,5,4,

  SUM=0700
```

HP PART NUMBER: 1816-1489
USED ON ASSEMBLY 02640-60267 (DISPLAY TIMING/CONTROL) U22
FUNCTION: DISPLAY TEST CHARACTER RANGE SELECT PROM
OUTPUT DEFINITION:

O1--CHARACTER SET BIT0	(POSITIVE TRUE)
O2--CHARACTER SET BIT1	(" ")
O3--DISPLAY TEST "ON"	(" ")
O4--UPPER CASE (LOWER CASE BAR)	(" ")

ROM GENERIC PART NUMBER: 7611A (256X4)
ROM CONTENTS:

```
$A0000.
0,0,0,0,8,8,8,8,8,8,8,8,0,0,0,0,
0,8,0,0,8,8,8,8,8,8,8,8,0,5,0,0,
0,0,8,0,8,8,8,8,8,8,8,8,0,0,5,0,
0,8,8,0,8,8,8,8,8,8,8,8,0,5,5,0,
0,0,0,8,8,8,8,8,8,8,8,8,0,0,0,5,
0,8,0,8,8,8,8,8,8,8,8,8,0,5,0,5,
0,0,8,8,8,8,8,8,8,8,8,8,0,0,5,5,
0,8,8,8,8,8,8,8,8,8,8,8,0,5,5,5,

$A0080.
6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,
6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,
6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,
6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,
4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,
4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,
4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,
4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,

  SUM=051C
```

4.19 ENHANCEMENT "PIPELINE AND ALIGNMENT" LATCHES

4.19.1 The enhancement pipeline latch (U412) stores the enhancements bits for one character time. This storage period ensures that the enhancements are aligned with the proper character cell.

4.19.2 The enhancement alignment latch (U312) delays the changing of enhancements by approximately 100 nsec. This time allows parallel to serial conversion of the video bit stream summation with graphics, and dot stretching to occur and still have the character centered within the enhancement boundaries.

4.20 CHARACTER ROM OUTPUT LATCH

4.20.1 The character ROM output latch (U34) samples the output of the character ROM every character time and ensures that the data to the parallel/serial converter is valid at the pertinent times.

4.20.2 Note that the character ROM outputs are pulled high so that when the ROM is disabled, only "high" values (blank on the CRT) are latched into U34.

4.21 PARALLEL TO SERIAL CONVERTER AND DOT CLOCK LOGIC

4.21.1 The circuit block consisting of U44, U24, U31 (FF#2), and parts of U25, U35, and U67 accomplish the conversion of character ROM data to a valid serial bit stream.

4.21.2 Under the control of the dot clock logic, U44 loads the outputs of U34 in a parallel fashion, and shifts out a serial video bit stream. The manner in which this feat is accomplished varies depending on two factors; is the character information a dot shift or a dot repeat character? and if a dot shift character, does this particular bit stream need to be dot shifted?

4.21.3 With dot repeat characters, U31-6 will go high and allow the first dot clock to U44-7 to be inhibited through the action of U25-4,5,6. This action doubles the width of the first dot of the character and allows nine bits of data to be extracted from an eight bit ROM. This dot repeat character mode is used for line drawing and large character sets.

4.21.4 Dot shift characters are indicated by U31-5 going high. U34-19 then determines whether normal mode, or dot shift mode will be invoked. A low value at U34-19 indicates that dot shift should be performed. When a high value is present, U31-8 remains high during the entire character time, and dots are shifted out with standard display clock timing. A low value at U34-19 causes U31-8 to switch states and the clock to U44 is inverted "on the run". This delays the dot stream output of U44 by one half clock time and creates an effective dot shift.

4.22 DISPLAY TEST GENERATOR

4.22.1 U31 (FF#1) allows the generation of display test patterns through the switches labeled "DT" and "U3". The normal operating state of "DT" is closed, and when opened, causes display test patterns to be displayed on the CRT according to the position of "U3". If "U3" is open, a full screen crosshatch pattern will be displayed. If "U3" is closed, the screen will display both @'s and del's.

4.22.2 Note that the @/del pattern is dependent upon the current display and varies with odd/even ASCII input. That is, even ASCII characters are replaced by @'s and odd ASCII characters are replaced by del's. Because of this constraint, the best display test pattern is achieved with a self test pattern resident on the CRT, where odd and even ASCII alternates automatically.

4.22.3 Note also that these display test patterns do not destroy the original CRT display which is totally recoverable by closing "DT". The display must be "on" (i.e. 69-6 must be high) in order for display test to be seen.

4.23 DOT STRETCHER

4.23.1 The purpose of the dot stretching transistor circuit (Q1, C2, R7, and R5) is to introduce a variable delay into the alpha and graphics video bit stream. This is a lopsided delay, causing only the "low" time at U212-4 to be lengthened according to the RC time constant. The pot in this circuit should set so that single dot wide vertical lines appear as wide and as bright as single raster horizontal lines.

4.24 FINAL VIDEO SUMMING CIRCUITRY

4.24.1 The discrete logic used in the final video summing circuitry takes all pertinent video information as input and creates a single VIDEO (P4-1) output. The inputs to this circuit include the character blink rate (U72-8), cursor blink rate (U71-14), cursor extend pulse (U112-4), alpha and graphics video (U212-16), the enhancement enable signals (U312-2,5,10,12), blanking (U612-3), and one or two others. These signals are logically combined to emulate the video construction techniques of the original 264X display module.

4.24.2 A switch has been provided ("IV") that, when closed, causes a full screen inverse video pattern to be displayed on the CRT.

4.24.3 The discrete delay introduced by Q2, C3, R9 and R10 allows the half-bright and inverse video fields to be aligned properly properly. As of Rev. A boards, the alignment has been correct for all possible pot positions and only slightly noticeable effects occur when the pot is changed from min to max.

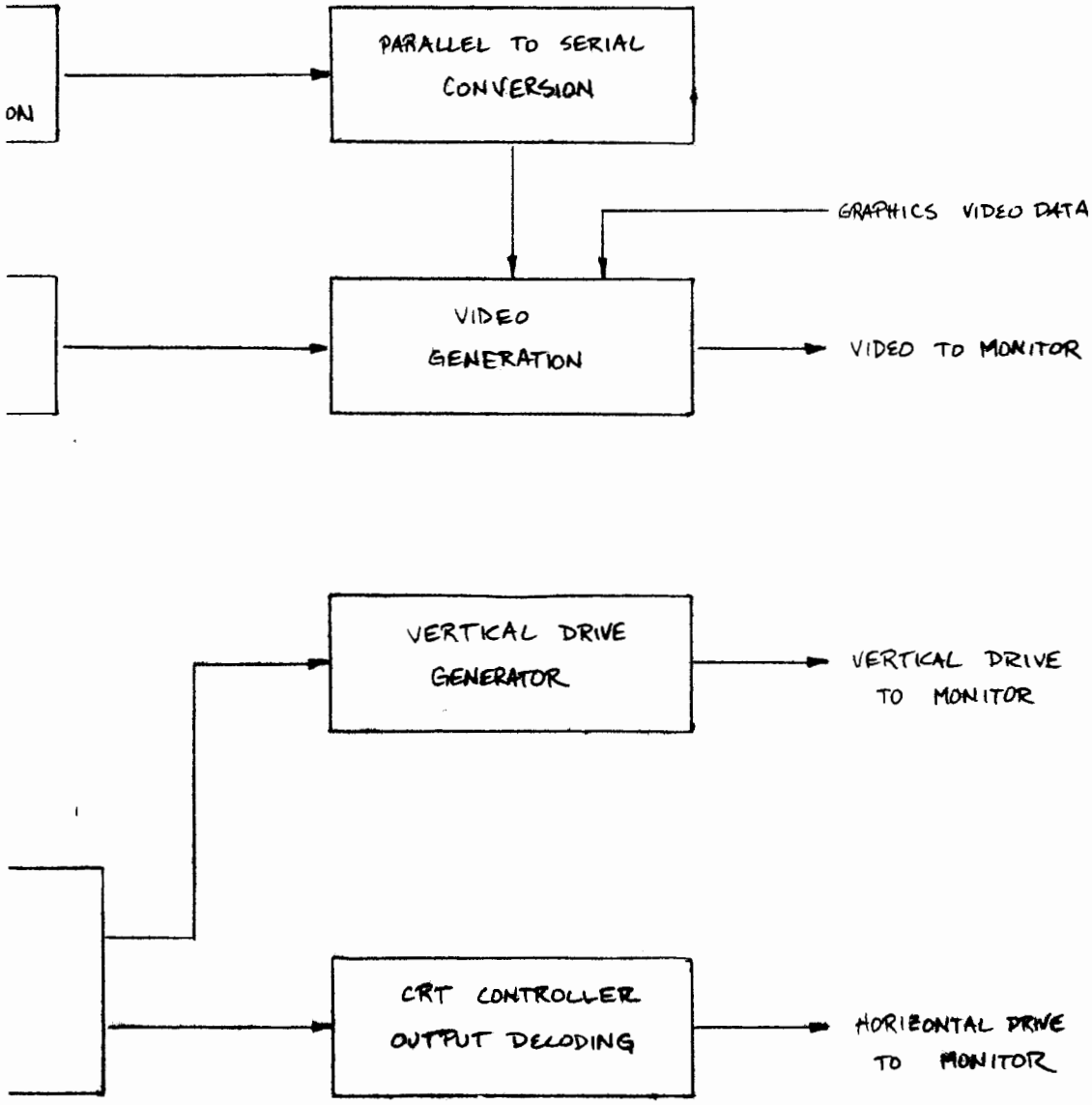
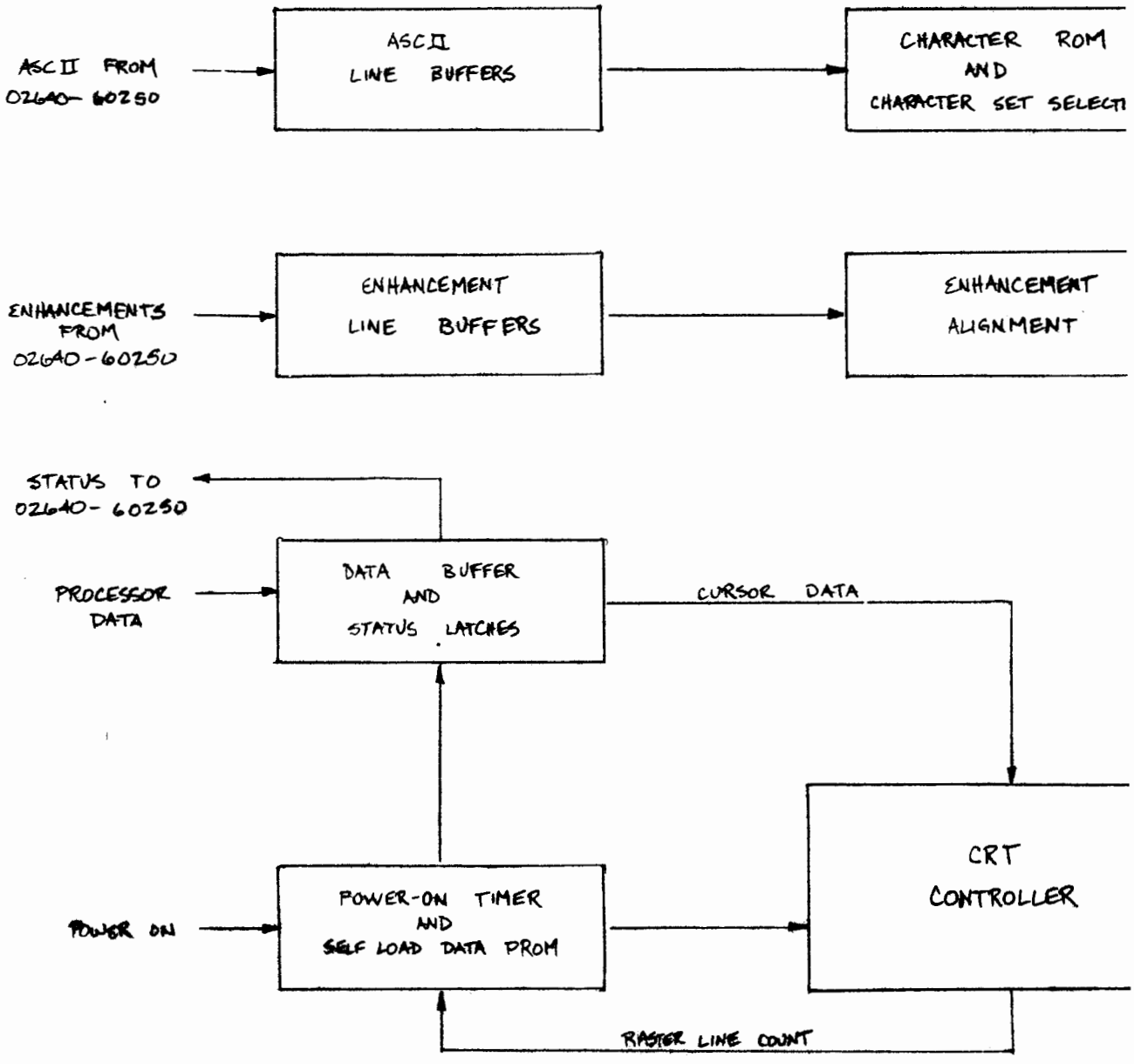


FIGURE 1
02640-60267 BLOCK DIAGRAM
FEB-01-82 13255-91267


ASCII FROM
02640-60250
ASCII
LINE BUFFERS
CHARACTER ROM
AND
CHARACTER SET SELECTI
ENHANCEMENTS
FROM
02640-60250
ENHANCEMENT
LINE BUFFERS
ENHANCEMENT
ALIGNMENT
STATUS TO
02640-60250
PROCESSOR
DATA
DATA BUFFER
AND
STATUS LATCHES
CURSOR DATA
CRT
CONTROLLER
POWER ON
POWER-ON TIMER
AND
SELF LOAD DATA PROM
RASTER LINE COUNT

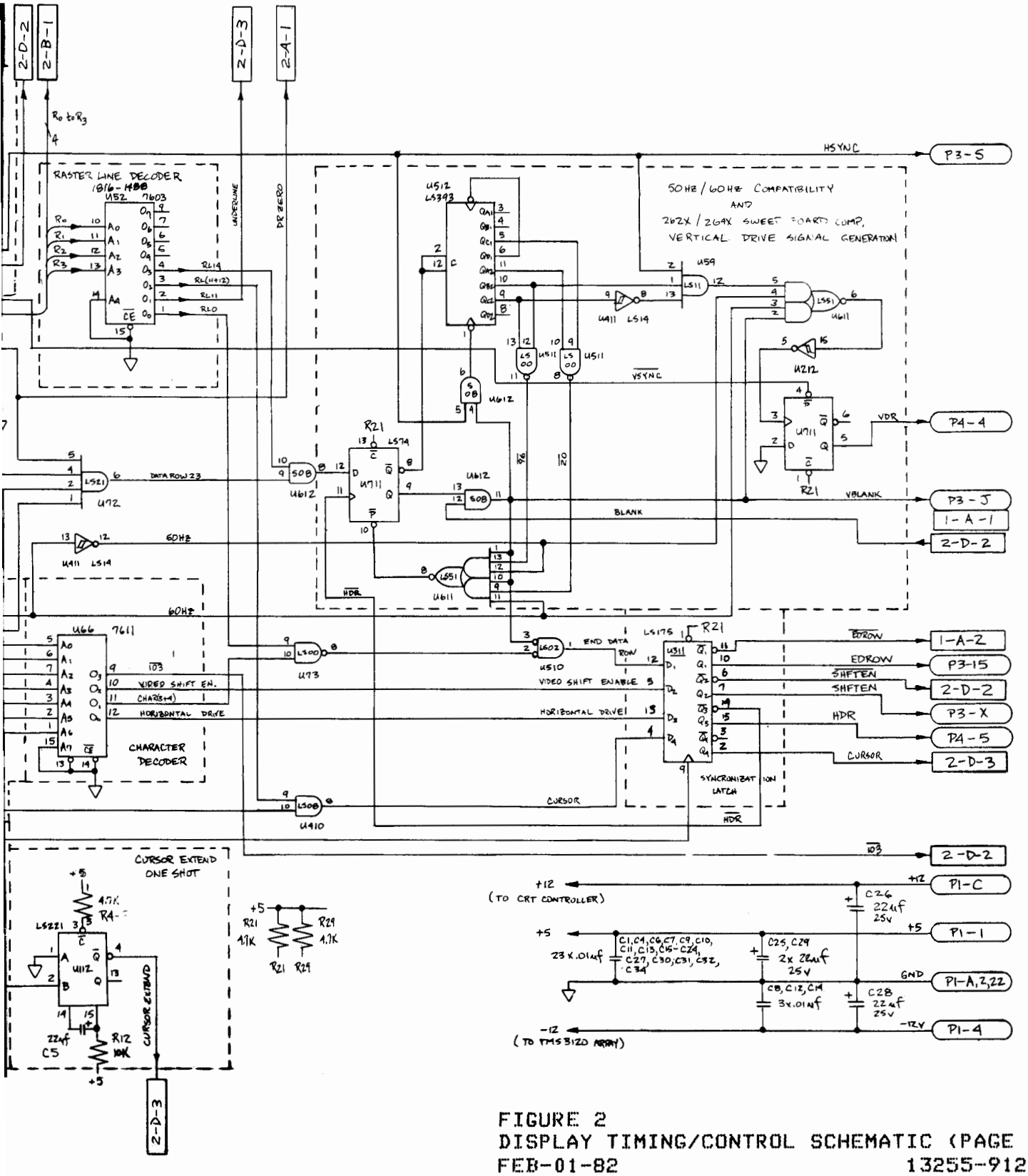
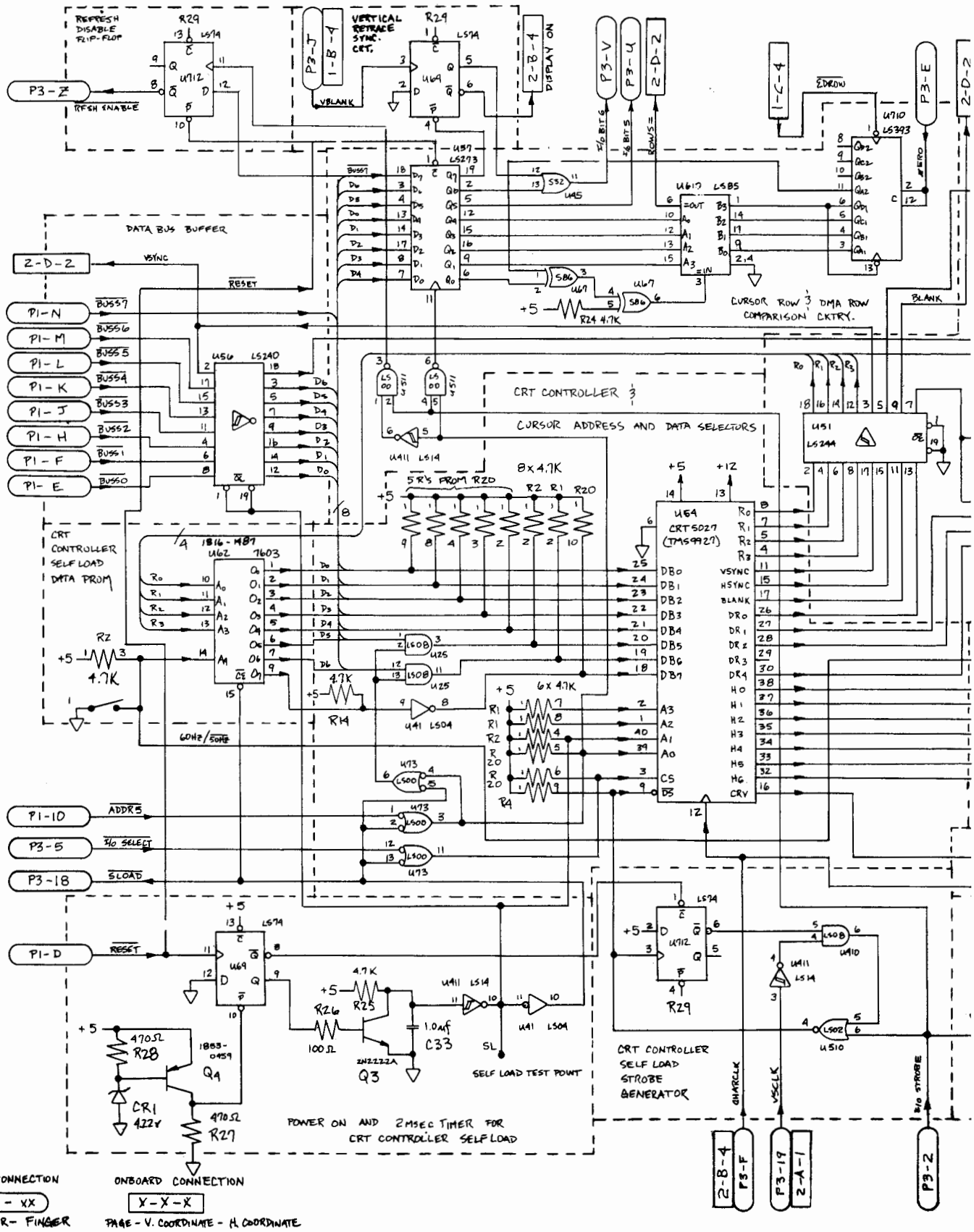


FIGURE 2
DISPLAY TIMING/CONTROL SCHEMATIC (PAGE 1)
FEB-01-82 13255-91267


REFRESH DISABLE FLIP-FLOP
P3-Z
RFSH ENABLE
VERTICAL RETRACE SYNC. CKT.
P3-J
1-B-4
VBLANK
2-B-4
DISPLAY ON
P3-V
P3-4
2-D-2
1-C-4
ZDROW
P3-E
ZERO
DATA BUS BUFFER
Z-D-Z
VSYNC
RESET
P1-N
P1-M
P1-L
P1-K
P1-J
P1-H
P1-F
P1-E
BUSS7
BUSS6
BUSS5
BUSS4
BUSS3
BUSS2
BUSS1
BUSS0
CURSOR ROW & DMA ROW COMPARISON CKTRY.
BLANK
CRT CONTROLLER
CURSOR ADDRESS AND DATA SELECTORS
CRT CONTROLLER SELF LOAD DATA PROM
8x4.7K
5 RS FROM R20
6x4.7K
4.7K
R24 4.7K
R14
RZ
60HZ/50HZ
P1-10
ADDR5
P3-5
I/O SELECT
P3-18
SLOAD
P1-D
R28 470Ω
Q4
CR1 4.2V
R27 470Ω
R26 100Ω
R25 4.7K
C33 1.0uf
Q3
SELF LOAD TEST POINT
POWER ON AND 2MSEC TIMER FOR CRT CONTROLLER SELF LOAD
CRT CONTROLLER SELF LOAD STROBE GENERATOR
CHARCLK
VSCLK
I/O STROBE
2-8-4
P3-F
P3-19
2-A-1
P3-2
EDGE CONNECTION
XX-XX
CONNECTOR- FINGER
ONBOARD CONNECTION
X-X-X
PAGE - V. COORDINATE - H. COORDINATE

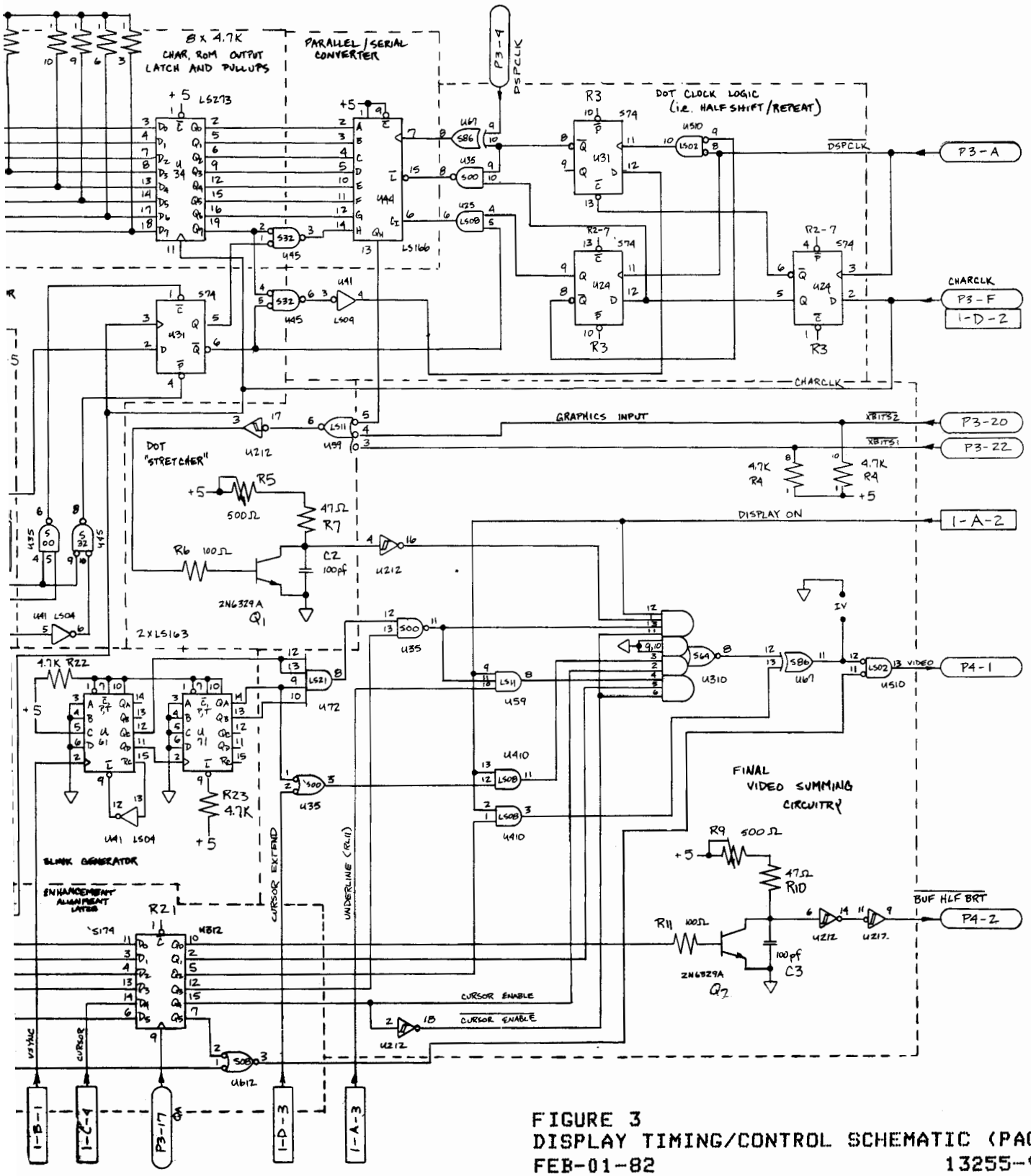
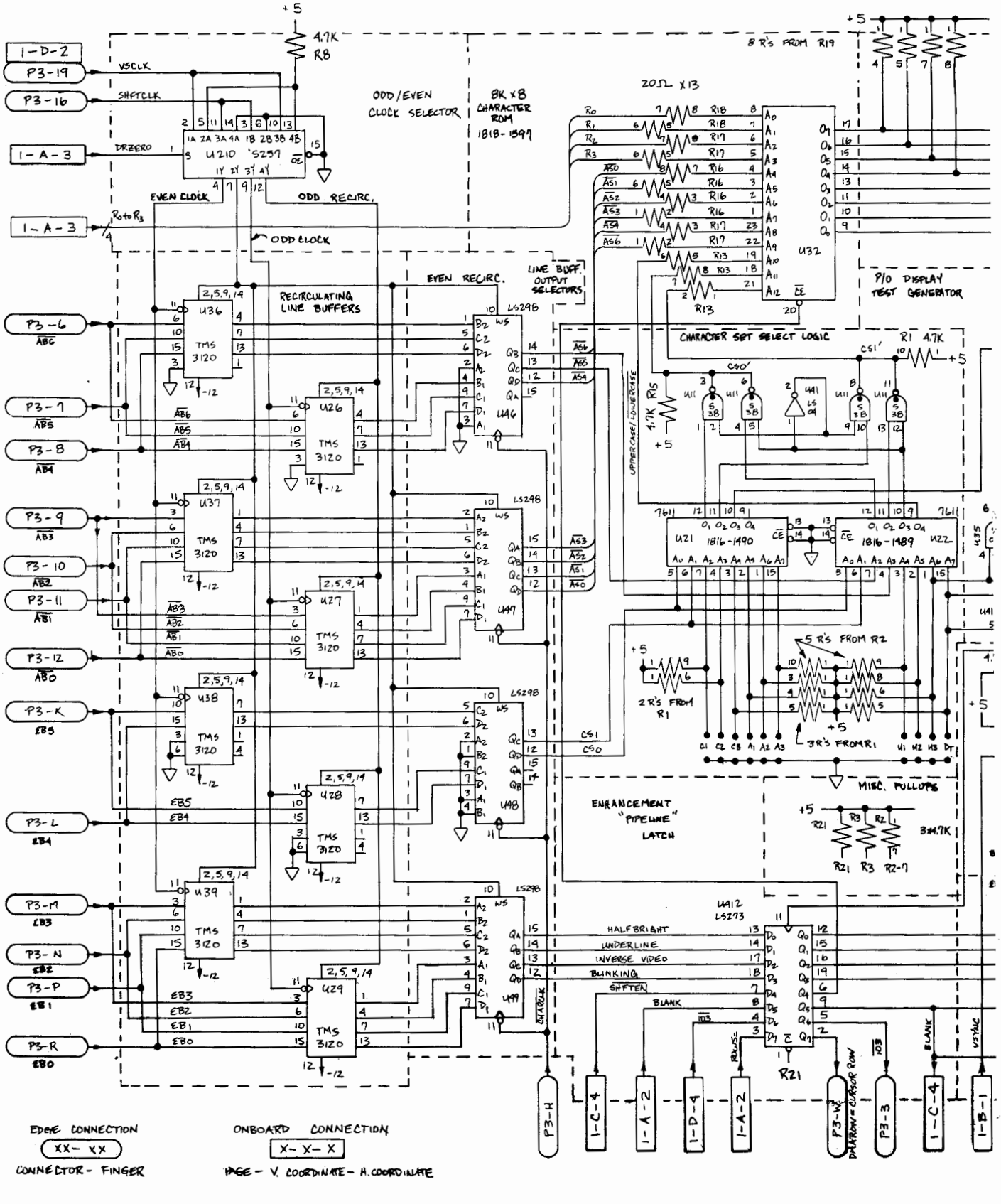


FIGURE 3
DISPLAY TIMING/CONTROL SCHEMATIC (PAGE 2)
FEB-01-82 13255-91267


+5
4.7K
R8
1-D-2
P3-19
VSCLK
P3-16
SHFTCLK
1-A-3
DRZERO
U210 'S257
EVEN CLOCK
ODD RECIRC.
1-A-3
R0 to R3
ODD CLOCK
ODD/EVEN CLOCK SELECTOR
8K x 8 CHARACTER ROM 1818-1597
8 R's FROM R19
20Ω X13
U32
P/O DISPLAY TEST GENERATOR
CHARACTER SET SELECT LOGIC
R1 4.7K
4.7K R15
UPPERCASE/LOWERCASE
EVEN RECIRC.
LINE BUFF. OUTPUT SELECTORS
RECIRCULATING LINE BUFFERS
U36
U26
U37
U27
U38
U28
U39
U29
TMS 3120
LS298
U46
U47
U48
U49
P3-6
P3-7
P3-8
P3-9
P3-10
P3-11
P3-12
P3-K
P3-L
P3-M
P3-N
P3-P
P3-R
U21 1816-1490
U22 1816-1489
5 R's FROM R2
2 R's FROM R1
3 R's FROM R1
MISC. PULLUPS
3x4.7K
ENHANCEMENT "PIPELINE" LATCH
U412 LS273
HALFBRIGHT
UNDERLINE
INVERSE VIDEO
BLINKING
SHIFTEN
BLANK
CHARCLK
P3-H
1-C-4
1-A-2
1-D-4
1-A-2
P3-W
P3-3
1-C-4
1-B-1
BLANK
VSYNC
EDGE CONNECTION
XX-XX
CONNECTOR-FINGER
ONBOARD CONNECTION
X-X-X
PAGE-V. COORDINATE-H. COORDINATE

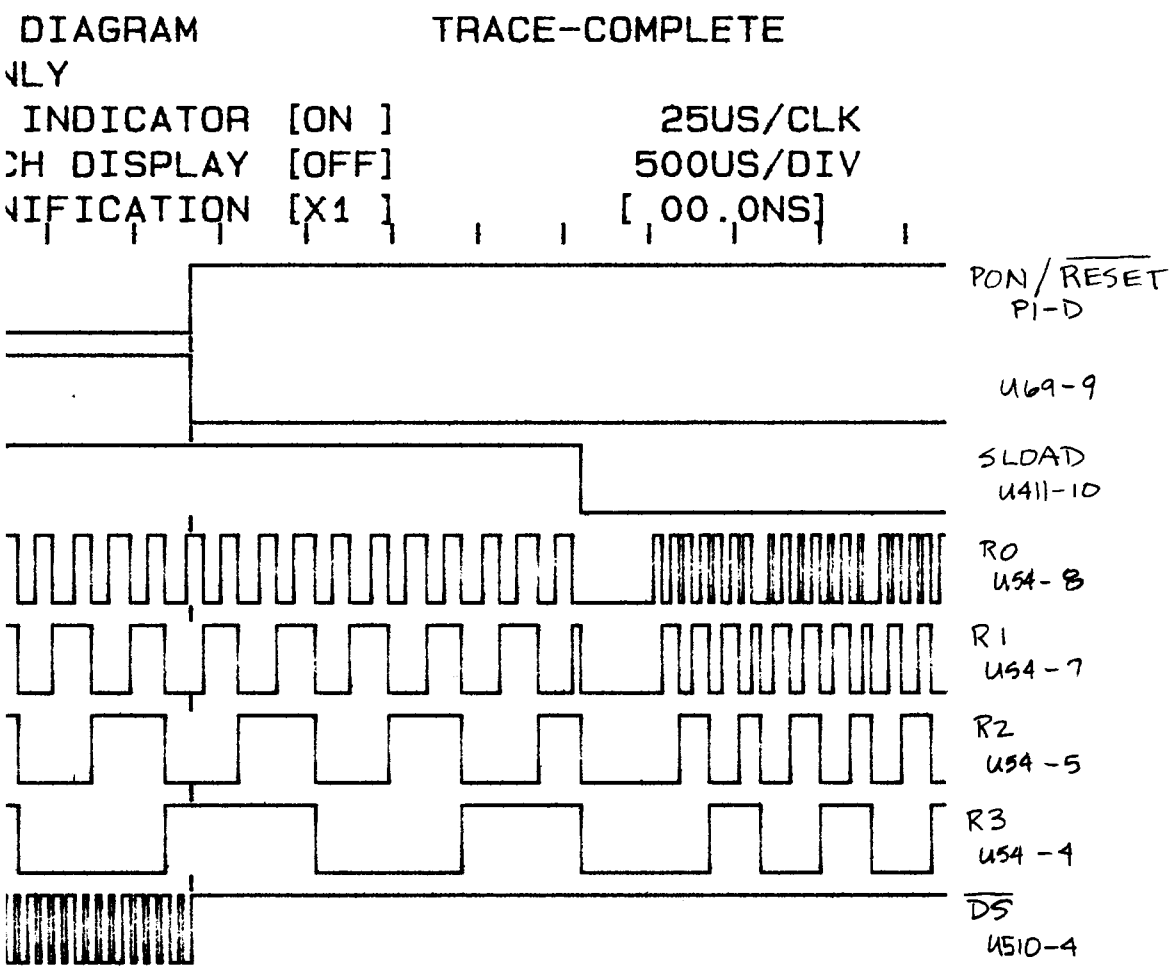


FIGURE 4
POWER-ON CRT CONTROLLER SELF-LOAD
FEB-01-82 13255-91267

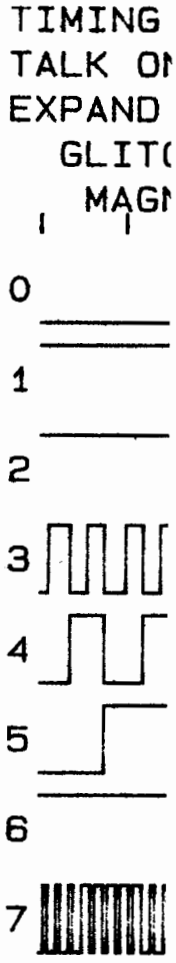
POWER-ON CRT CONTROLLER SELF LOAD

I. U69-9 IS ALWAYS PRESET AT POWER ON.

II. THE FIRST RISING EDGE OF P1-D CAUSES SLOAD TO BEGIN ITS TIMEOUT (~ 2msec) AND STOPS THE PROPOGATION OF $\overline{DS}$ THROUGH TO THE CRT CONTROLLER

III. WHEN SLOAD CHANGES STATE FROM HIGH TO LOW, THE CRT CONTROLLER CHANGES FROM SELF LOAD MODE TO DRIVE SIGNAL GENERATION MODE. THIS IS INDICATED BY THE RESETTING OF THE RASTER LINE COUNTER BITS R0 TO R3.

NOTE: R0 TO R3 COUNT 0 TO 15 IN SELF LOAD MODE AND 0 TO 14 IN SIGNAL GENERATION MODE.



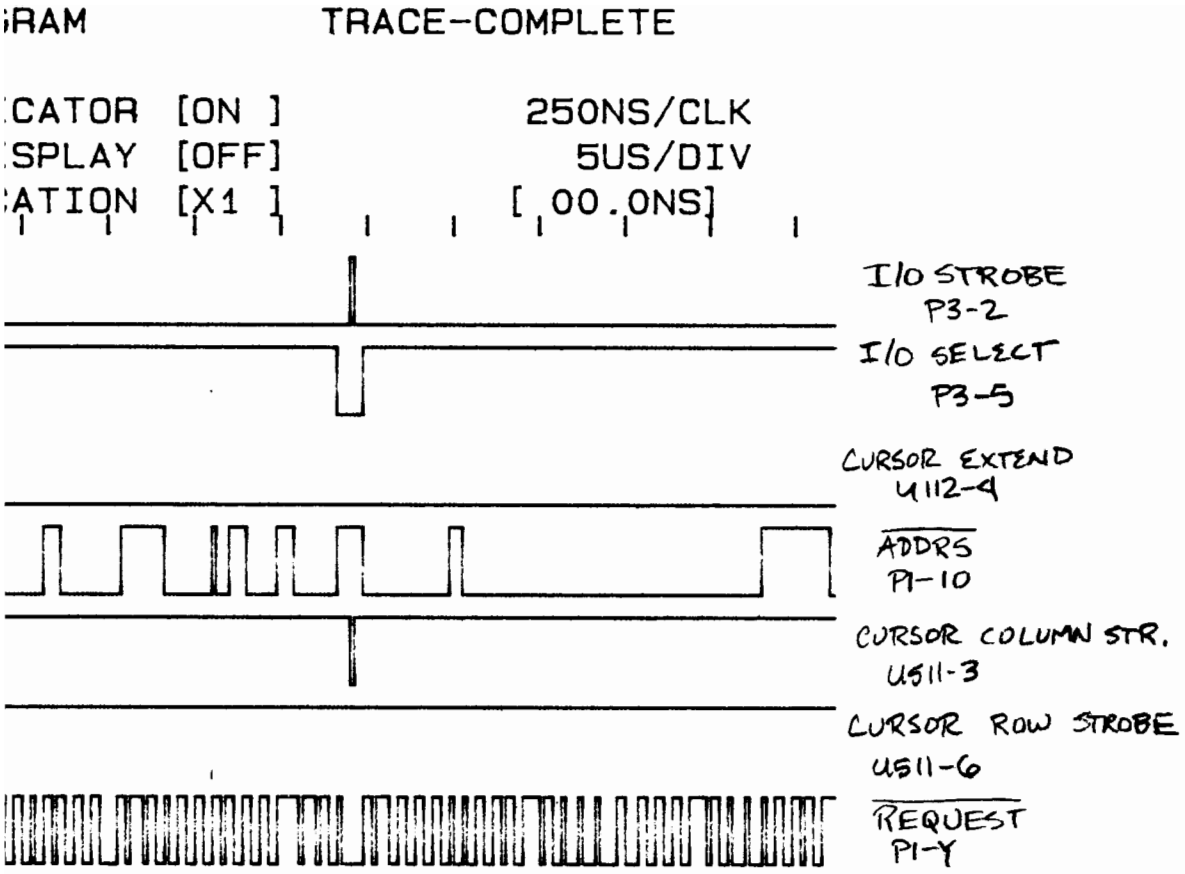
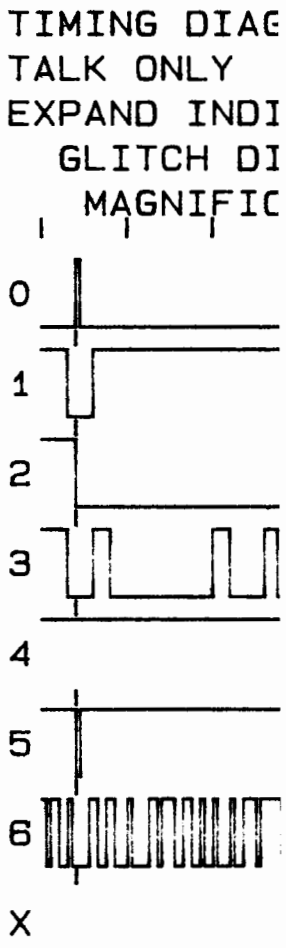


FIGURE 5
CURSOR CONTROL TIMING (A)
FEB-01-82 13255-91267

CURSOR CONTROL TIMING (MACROSCOPIC)

I. THIS DIAGRAM DISPLAYS TWO CURSOR CONTROL I/O WRITES. THE FIRST IS CURSOR ROW; THE SECOND IS CURSOR COLUMN.

II. NOTE THAT THE CURSOR EXTEND PULSE IS CLOSE TO 1/2 SECOND IN DURATION AND DOES RETURN TO A HIGH STATE WHEN U112 TIMES OUT.



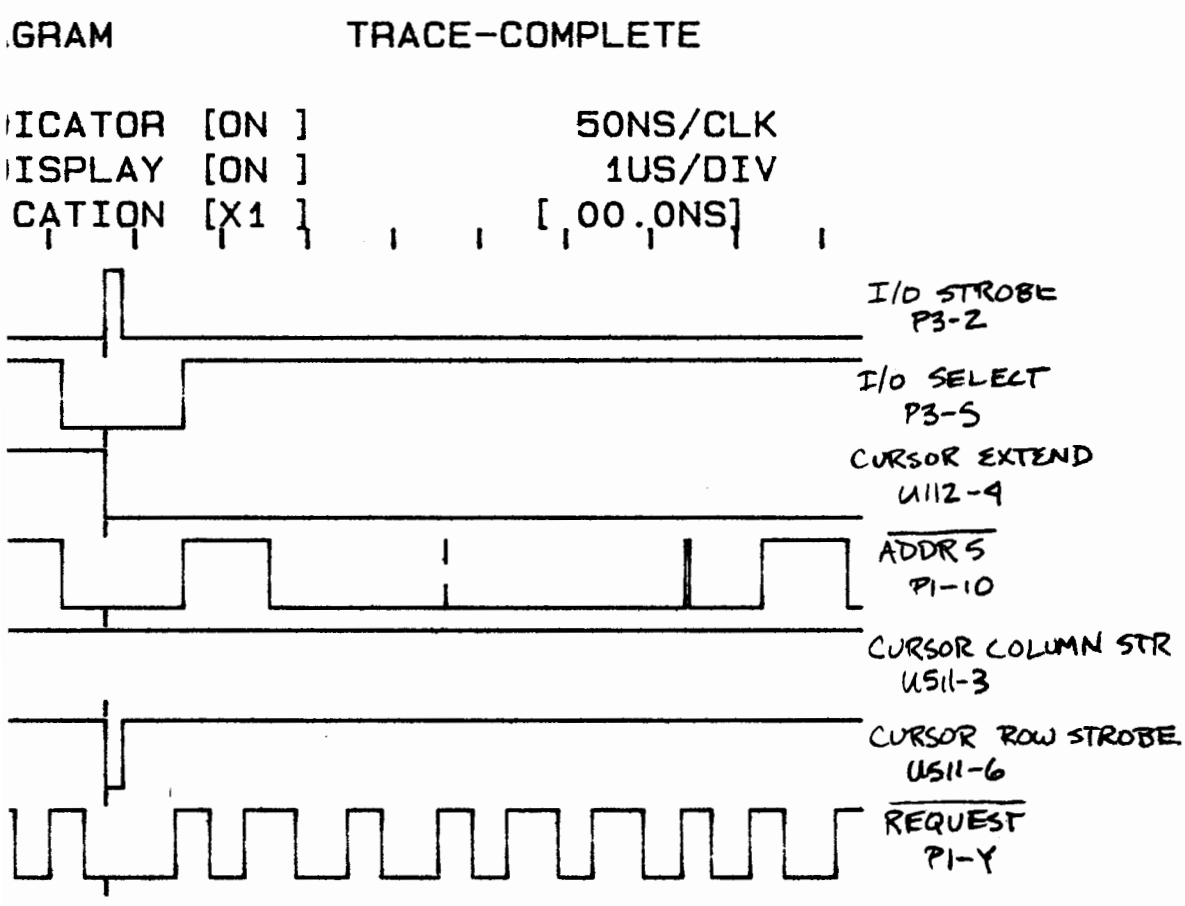


FIGURE 6
CURSOR CONTROL TIMING (B)
FEB-01-82 13255-91267

CURSOR CONTROL TIMING (MICROSCOPIC)

I. I/O SELECT IS A FUNCTION OF ADDRESSING ON THE DISPLAY MEMORY/DMA MODULE

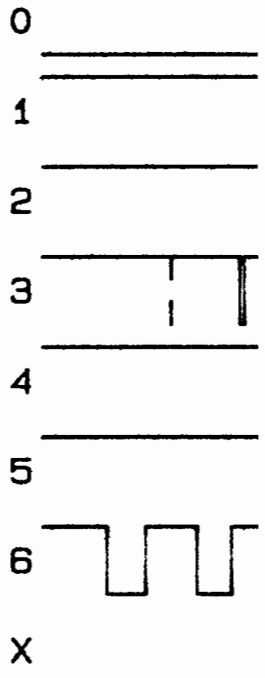
II. I/O STROBE LATCHES CURSOR INFO INTERNALLY IN THE CRT CONTROLLER, STARTS THE CURSOR EXTEND PULSE, AND CREATES A CURSOR COLUMN OR CURSOR ROW STROBE, DEPENDING ON THE PRESENT STATE OF $\overline{\text{ADDRS}}$.

$\overline{\text{ADDRS}} = 0 \Rightarrow$ CURSOR ROW

$\overline{\text{ADDRS}} = 1 \Rightarrow$ CURSOR COLUMN

III. NOTE THAT THE PROCESSOR $\overline{\text{REQUEST}}$ CYCLE IS SLIGHTLY LENGTHED DUE TO WAIT STATES CAUSED BY THE DISPLAY MEMORY / DMA MODULE

TIMING DIA
TALK ONLY
EXPAND IND
GLITCH D
MAGNIFI



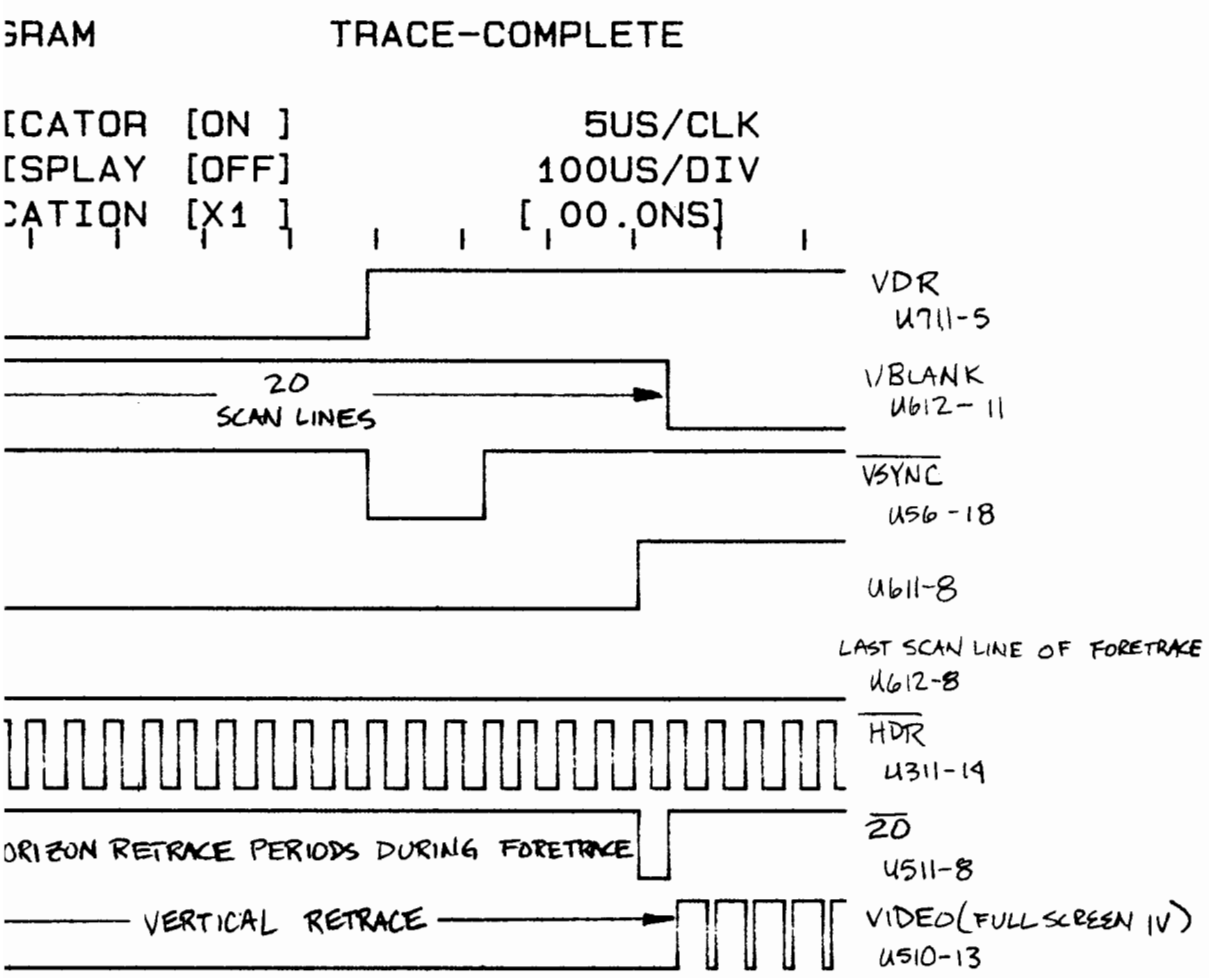


FIGURE 7
60 HZ VERTICAL RETRACE
FEB-01-82 13255-91267

60 Hz VERTICAL RETRACE

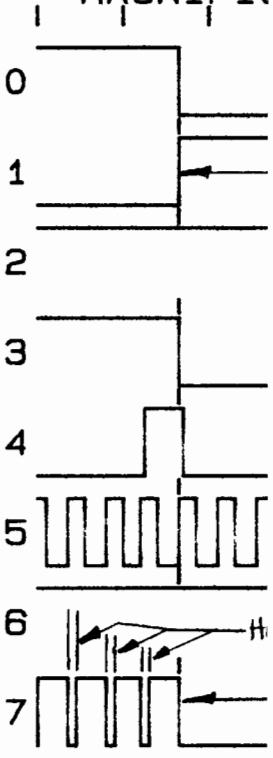
I. THE RISING EDGE OF VBLANK STARTS VDR LOW.

II. THE FALLING EDGE OF $\overline{\text{VSYNC}}$ RESETS VDR HIGH.

III. VBLANK STARTS AS A CONSEQUENCE OF THE LAST SCAN LINE OF FORETRACE.

IV. VBLANK STOPS AS A CONSEQUENCE OF $\overline{\text{ZD}}$ (i.e. $\overline{\text{ZD}}$ GOES LOW DURING THE TWENTIETH SCAN LINE OF VERTICAL RETRACE)

TIMING DIA(
TALK ONLY
EXPAND IND:
GLITCH D:
MAGNIFI(



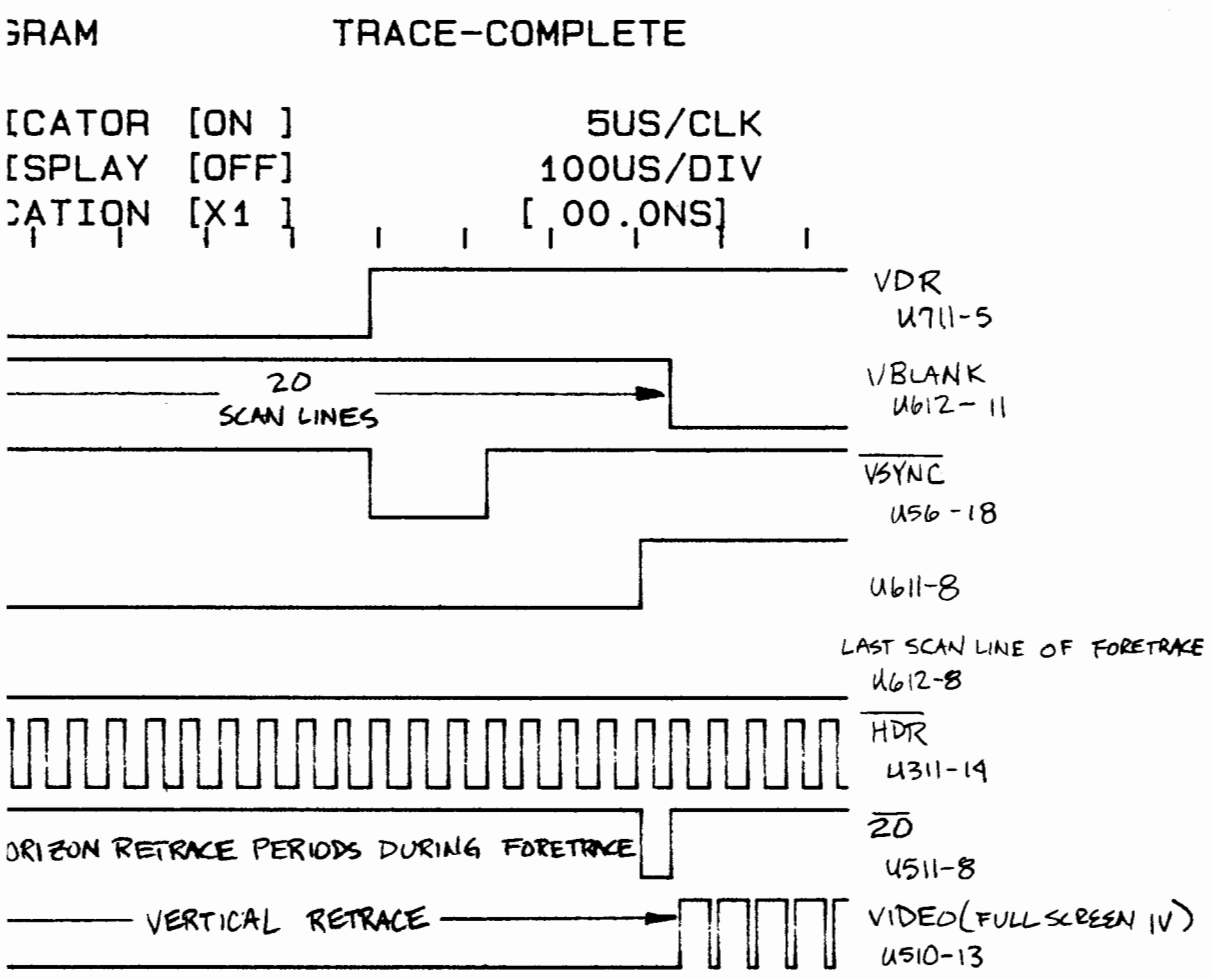


FIGURE 7
60 HZ VERTICAL RETRACE
FEB-01-82 13255-91267

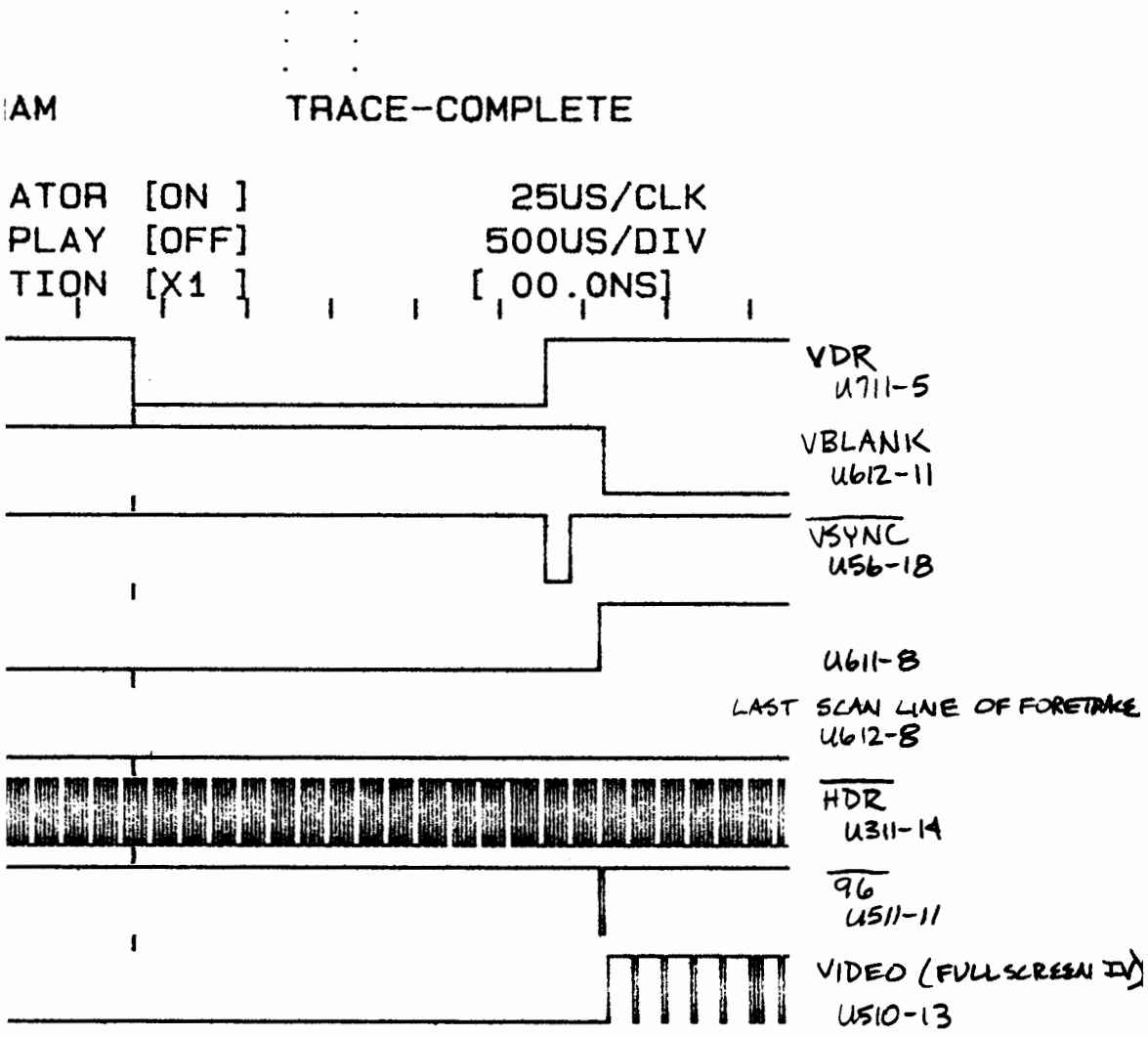


FIGURE 8
50 HZ VERTICAL RETRACE
FEB-01-82 13255-91267

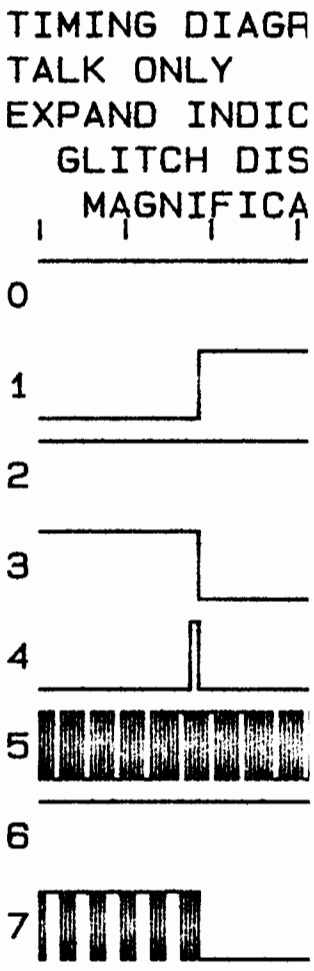
50 Hz VERTICAL RETRACE

I. VDR GOES LOW AS A RESULT OF THE THIRTY SECOND SCAN LINE OF VERTICAL RETRACE (NOT SHOWN).

II. THE FALLING EDGE OF $\overline{\text{VSYNC}}$ RESETS VDR HIGH.

III. VBLANK STARTS AS A CONSEQUENCE OF THE LAST SCAN LINE OF FORETRACE.

IV. VBLANK STOPS AS A CONSEQUENCE OF $\overline{96}$ (i.e. $\overline{96}$ GOES LOW DURING THE NINETY SIXTH SCAN LINE OF VERTICAL RETRACE).



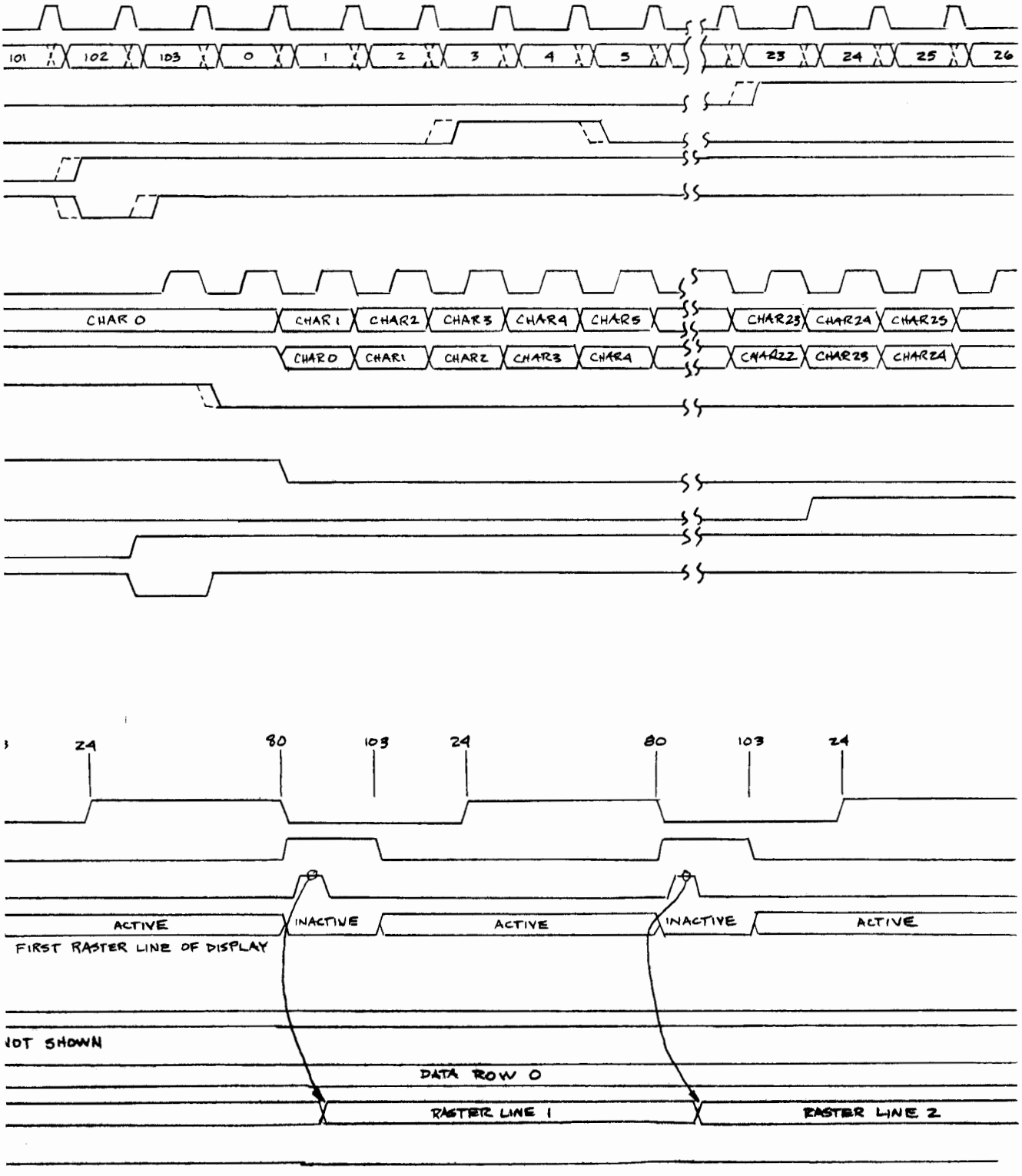
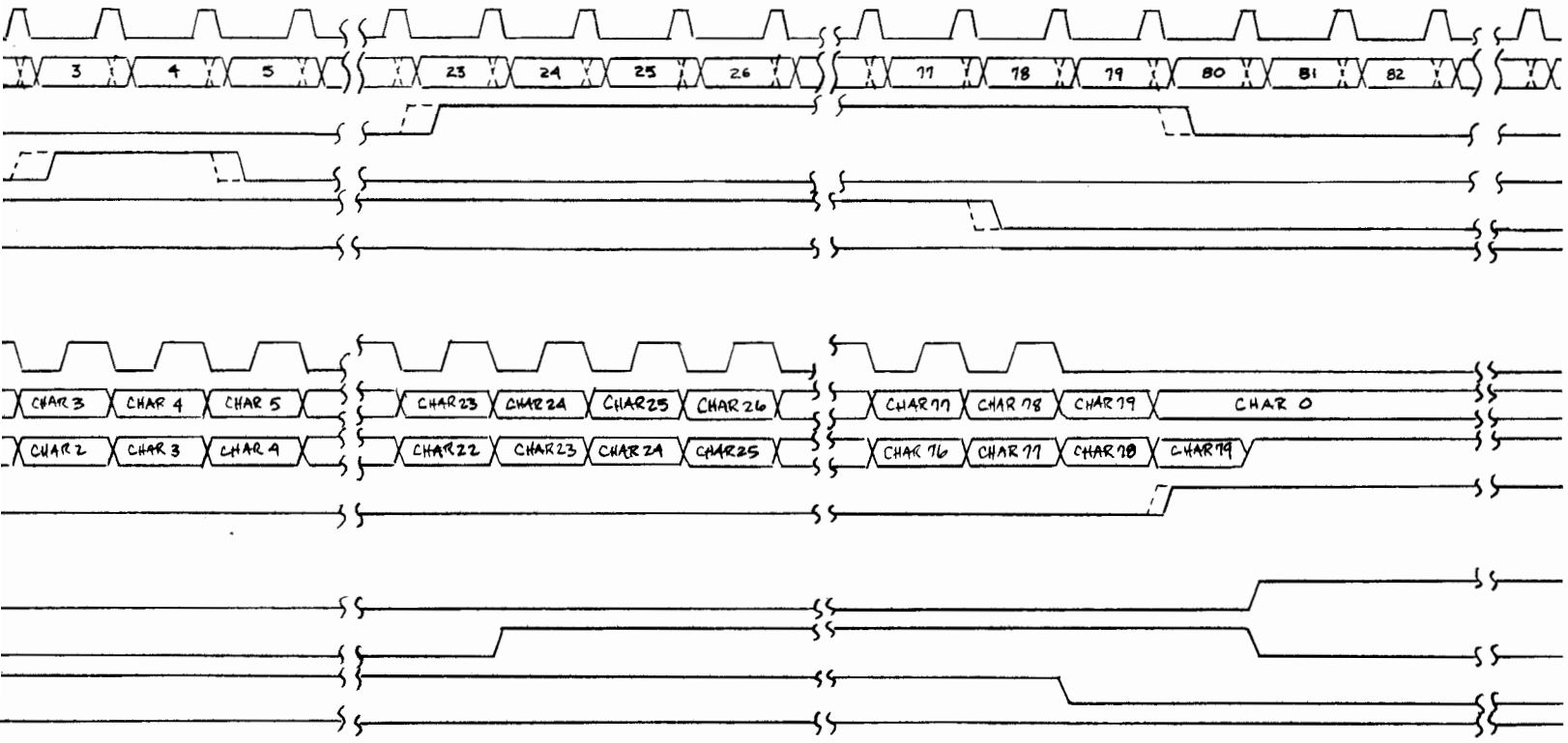
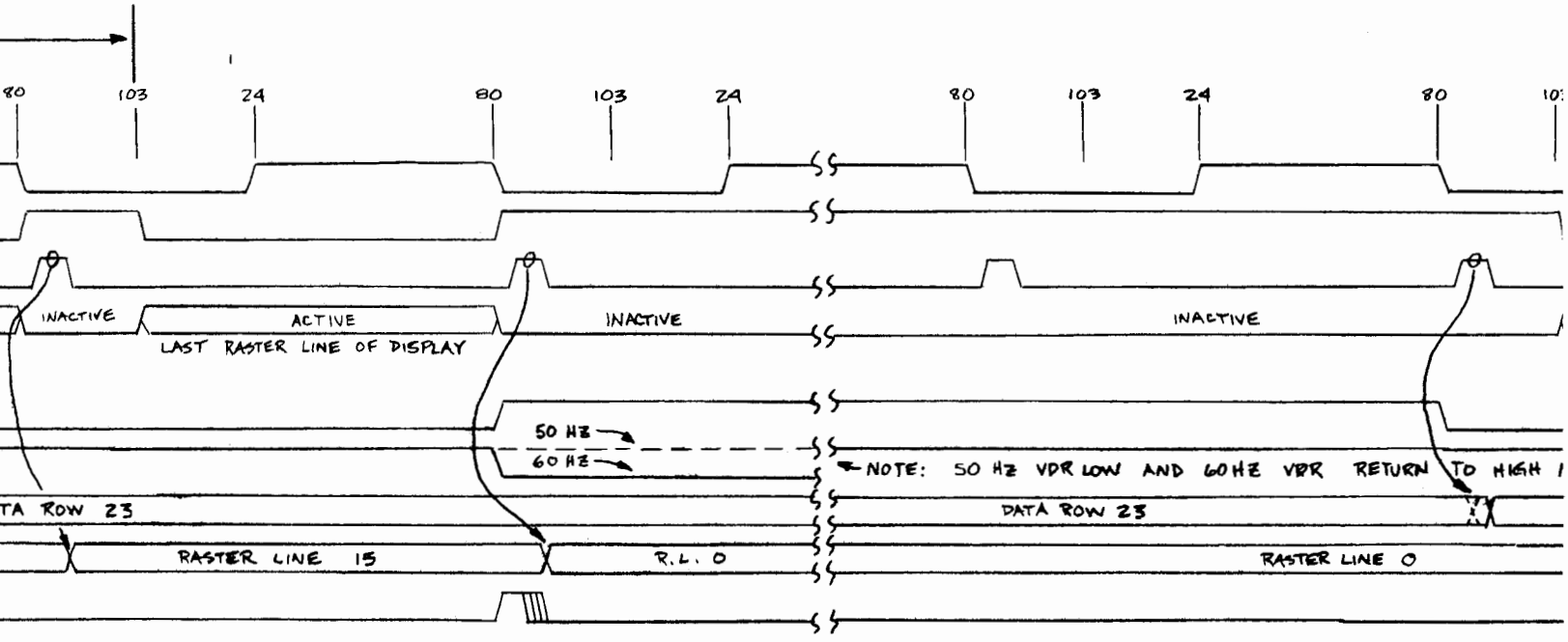
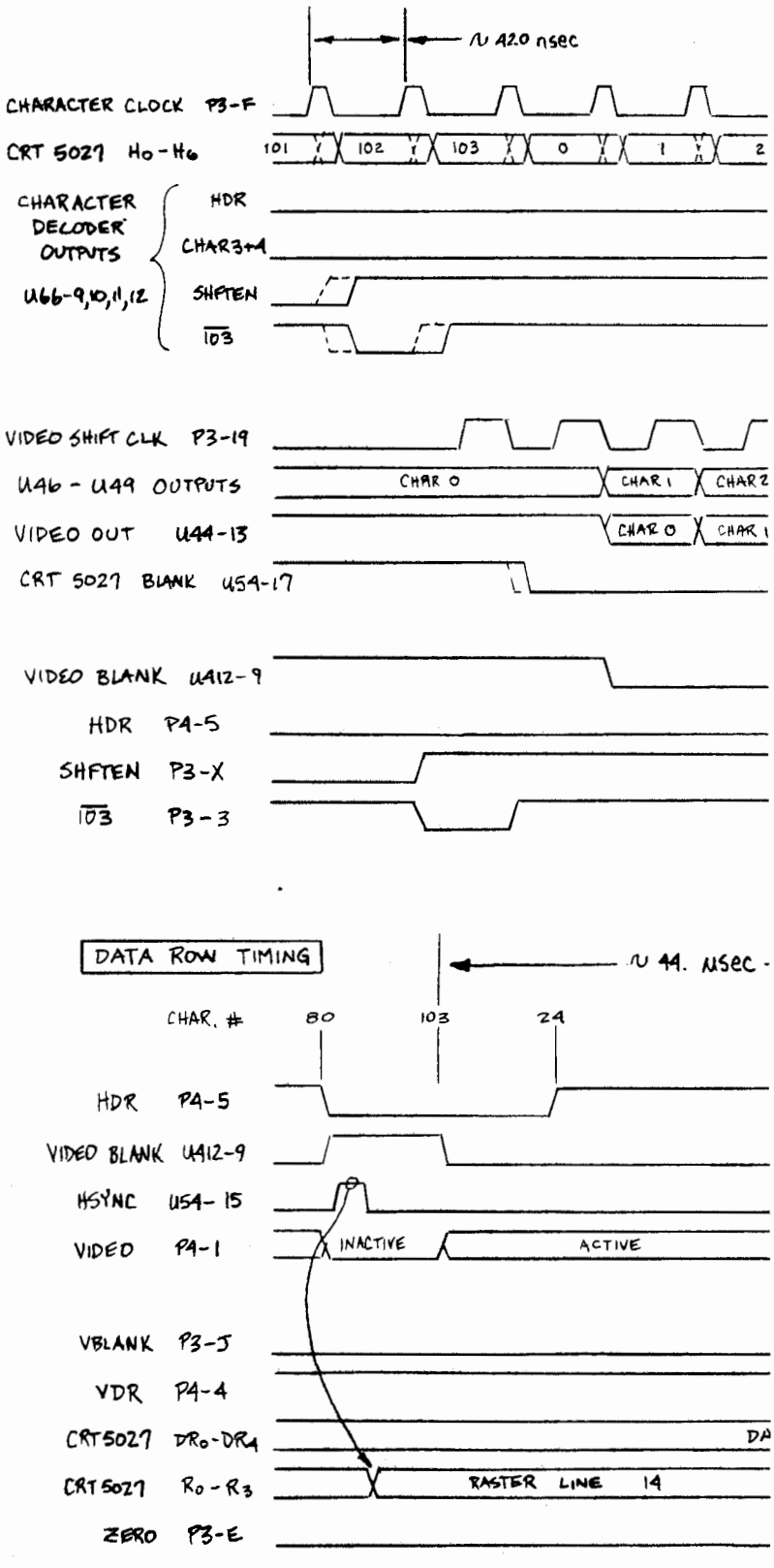


FIGURE 9
SCAN LINE AND DATA ROW TIMING
FEB-01-82 13255-91267


3
4
5
23
24
25
26
77
78
79
80
81
82
CHAR 3
CHAR 4
CHAR 5
CHAR 23
CHAR 24
CHAR 25
CHAR 26
CHAR 77
CHAR 78
CHAR 79
CHAR 0
CHAR 2
CHAR 3
CHAR 4
CHAR 22
CHAR 23
CHAR 24
CHAR 25
CHAR 76
CHAR 77
CHAR 78
CHAR 79


80
103
24
80
103
24
80
103
24
80
INACTIVE
ACTIVE
LAST RASTER LINE OF DISPLAY
INACTIVE
INACTIVE
50 HZ
60 HZ
NOTE: 50 Hz VDR LOW AND 60HZ VDR RETURN TO HIGH
TA ROW 23
RASTER LINE 15
R.L. 0
DATA ROW 23
RASTER LINE 0

SCAN LINE TIMING



DATA ROW TIMING

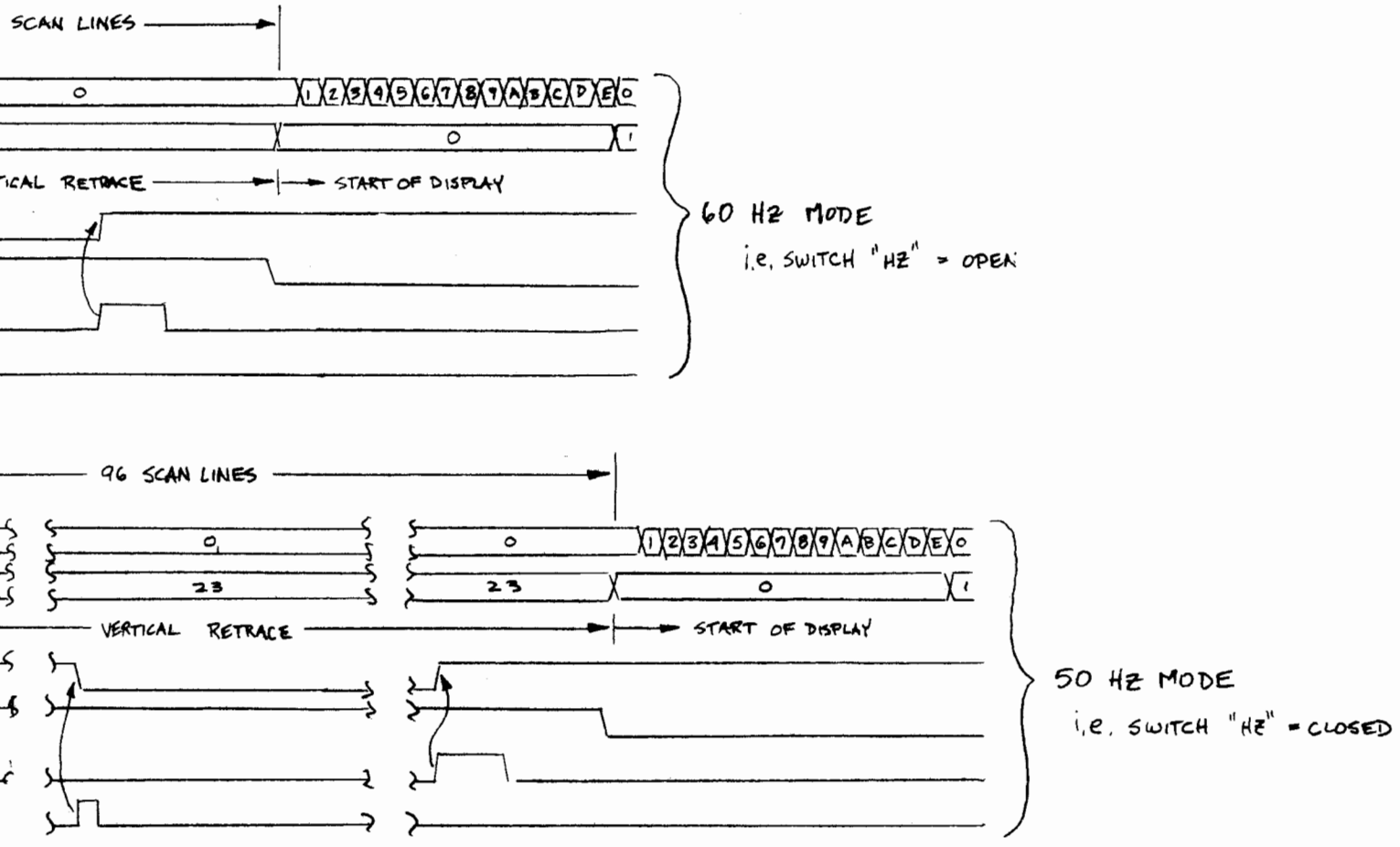
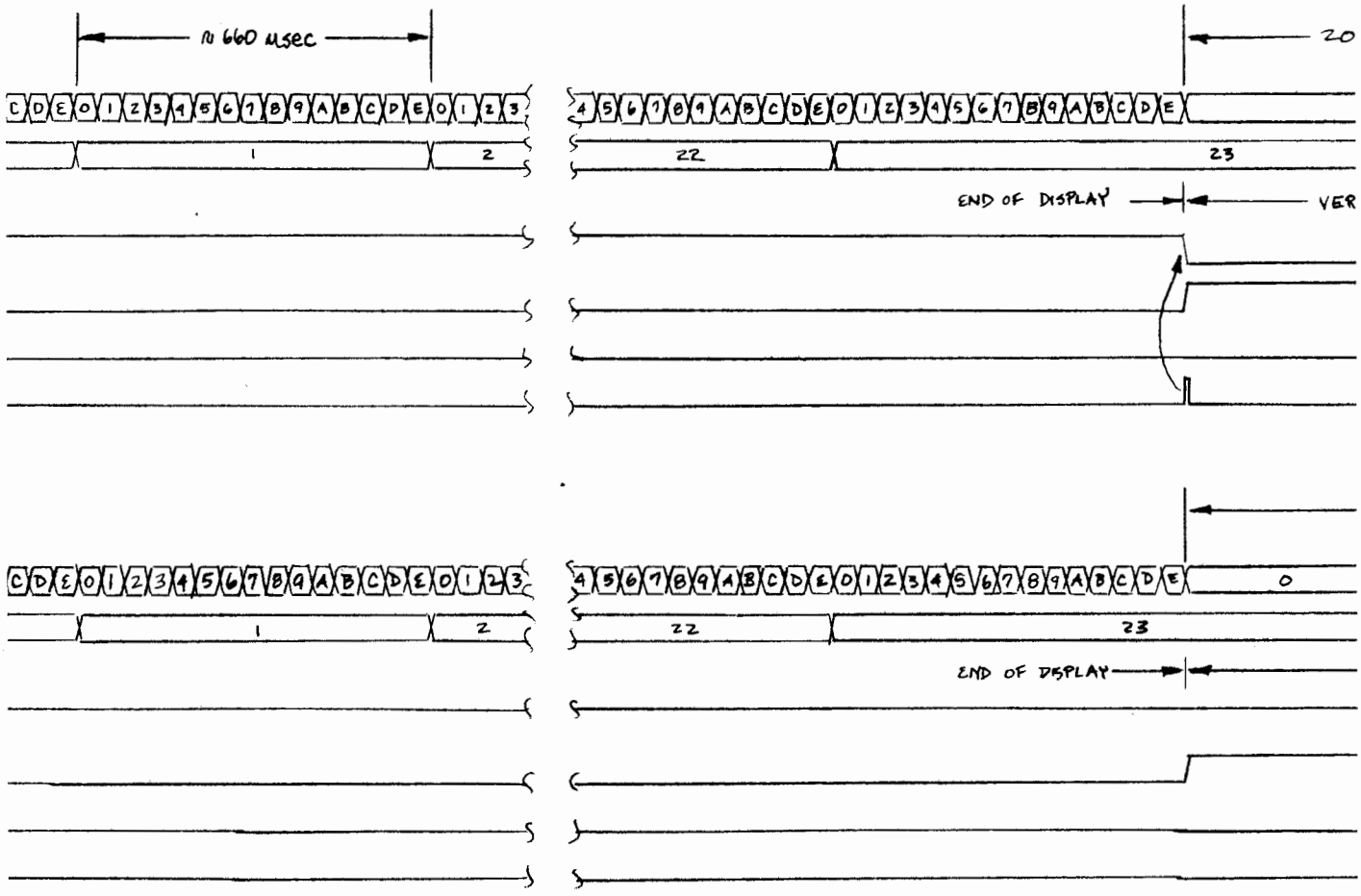
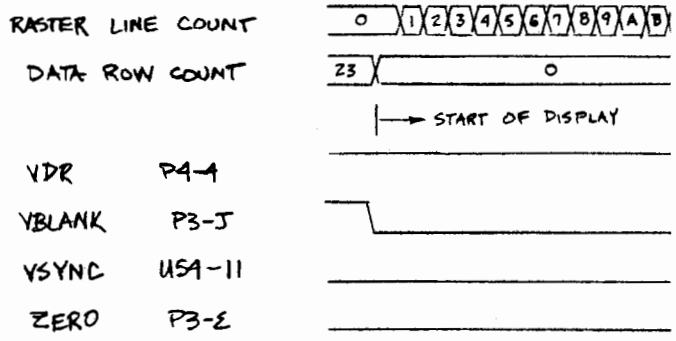
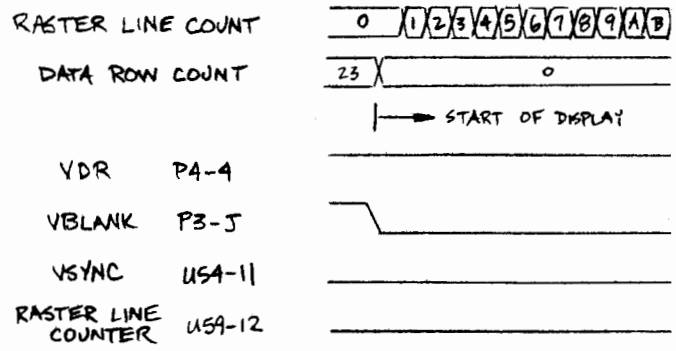


FIGURE 10
FRAME TIMING
FEB-01-82 13255-91267


≈ 660 μsec
20
END OF DISPLAY
VER
END OF DISPLAY
1
2
22
23
0

FRAME TIMING





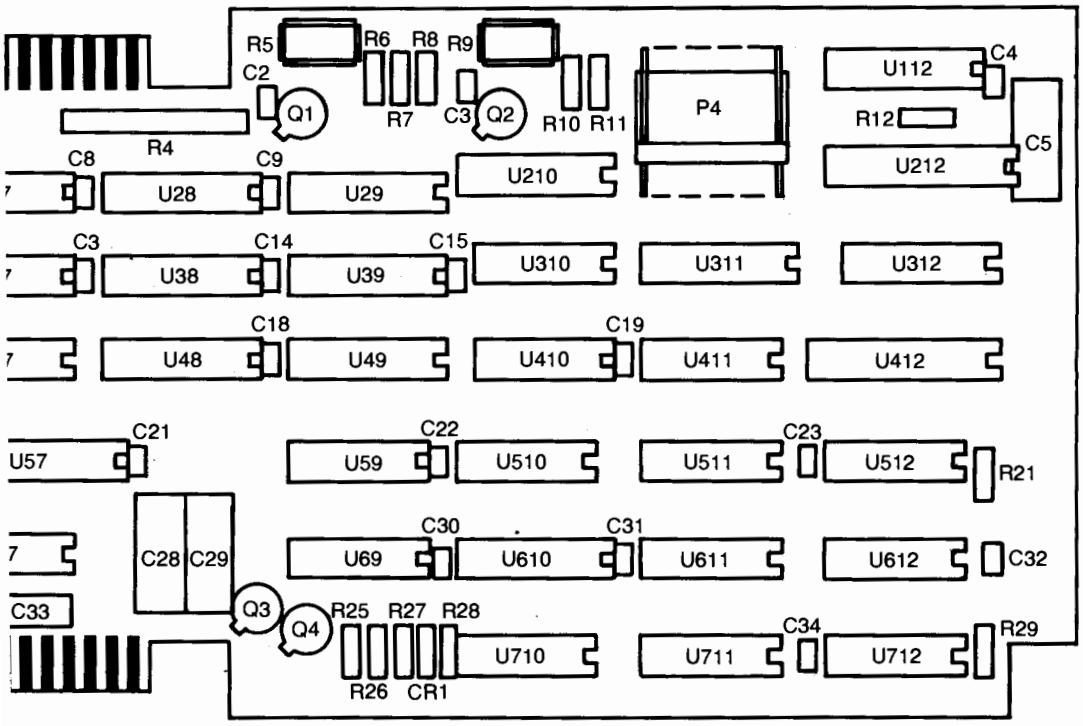
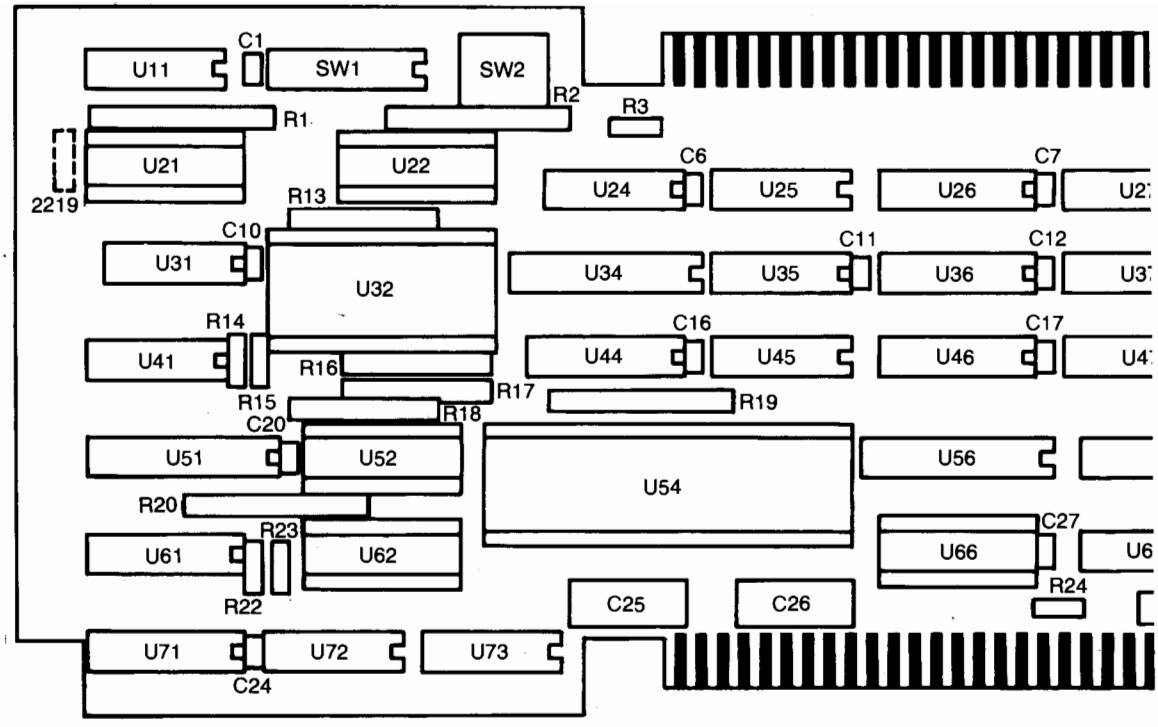


FIGURE 11
COMPONENT LOCATION DIAGRAM
FEB-01-82 13255-91267


C1
U11
SW1
SW2
R2
R3
R1
U21
U22
2219
R13
C6
C7
U24
U25
U26
C10
C11
C12
U31
U32
U34
U35
U36
R14
C16
C17
U41
U44
U45
U46
R16
R15
R17
R18
R19
C20
U51
U52
U54
U56
R20
R23
C27
U61
U62
U66
R22
R24
C25
C26
U71
U72
U73
C24

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	02640-60267	1	1	DISPLAY/TIMING/CONTROL PCA DATE CODE: B-2219-42	28480	02640-60267
C1	0160-4554	7	26	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C2	0160-4801	7	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C3	0160-4801	7		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C4	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C5	0180-2879	7	5	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C22	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C23	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C24	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C25	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C26	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C27	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C28	0180-2879	7	1	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C29	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C30	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C31	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C32	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C33	0160-4844	8	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-4844
C34	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
CR1	1902-3070	5	1	DIODE-ZNR 4.22V 5% DO-35 PD=.4W	28480	1902-3070
P4	1251-3766	5	1	CONNECTOR 6-PIN M POST TYPE	28480	1251-3766
Q1	1854-0019	3	2	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q2	1854-0019	3		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q3	1854-0477	7	1	TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
Q4	1853-0459	3	1	TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
R1	1810-0279	5	5	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R2	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R3	0683-4725	2	10	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R4	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R5	2100-3351	6	2	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
R6	0683-1015	7	3	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R7	0683-4705	8	2	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R8	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R9	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
R10	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R11	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R12	0683-1035	1	1	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R13	1810-0322	9	4	NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R14	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R15	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R16	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R17	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R18	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R19	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R20	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R21	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R22	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R23	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R24	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R25	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R26	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R27	0683-4715	0	2	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R28	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R29	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
SW1	3101-1983	9	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-1983
SW2	3101-2063	8	1	SWITCH-RKR DIP-RKR-ASSY 4-1A .05A 30VDC	28480	3101-2063