HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

MODEL 2640A INTERACTIVE DISPLAY TERMINAL

Manual part no. 02640-90012
Microfiche part no. 02640-90014

Printed: MAY 1976

OPTIONS COVERED

This manual covers options 001, 010, 015, and 020 as well as the standard model terminal.

ACCESSORIES COVERED

This manual covers the following terminal accessories:

13231A Display Enhancements
13231A-201 Mathematic Set
13231A-202 Line Drawing Set
13233A Terminal Memory Module (+2K)
13234A Terminal Memory Module (+4K)
13238A Terminal Duplex Register
13238A-001 HP 9866 Cable Assembly
13240A HP 2640 Option Slot Extender
13245A Character Set Generation Kit

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LIST OF EFFECTIVE PAGES

Changed pages are identified by a change number adjacent to the page number. Changed information is indicated by a vertical line in the outer margin of the page. Original pages do not include a change number and are indicated as change number 0 on this page. Insert latest changed pages and destroy superseded pages.

Change 0 (Original) ..... MAY 1976

PREFACE

This manual provides field service instructions for the Hewlett-Packard 2640A Interactive Display Terminal. The HP 2640A is a state-of-the-art product and, because of product design, a complete modular philosophy has been implemented to minimize on-site time for installing add-on accessories and for repair. Initial installation instructions for the terminal are contained in the *HP 2640A Interactive Display Terminal Owner's Manual*, part no. 02640-90011.

CONTENTS

ILLUSTRATIONS

TABLES

INSTALLATION

SECTION I

1-1. INTRODUCTION

This section contains instructions for selecting optional ac operating voltages (110 or 220V), selecting optional operating functions, instructions for installing terminal add-on accessories, and instructions for unpacking and repackaging the terminal.

WARNING

Hazardous voltages are present inside equipment. The procedures contained in this section shall be performed only by qualified service personnel.

VORSICHT

Innerhalb des Geräts bestehen gefährliche Spannungen. Die in diesem Abschnitt enthaltenen Arbeiten dürfen nur durch Betriebsfachpersonal durchgeführt werden.

ATTENTION

Des tensions dangereuses sont présentes à l'intérieur du matériel. Les opérations décrites dans cette section ne devront être effectuées que par un personnel qualifié.

AVVISO

Pericolo: Alta tensione presente in questa apparecchiatura. Le procedure contenute in questa sezione debbono essere effettuate soltanto da qualificato personale di servizio.

ADVERTENCIA

Hay voltaje peligroso en el interior de este equipo. Los procedimientos expuestos en esta sección sólo deberá llevarlos a cabo el personal de servicio calificado.

高圧危険

内部装置に危険な高電圧がきています。この章にある処置や手続に関しては、専門のサービスマンによってのみ行なって下さい。

1-2. OPENING THE TERMINAL

To gain access to the terminal internal components, open the terminal as follows:

a. Set mainframe rear panel AC POWER switch to OFF and disconnect power cord from LINE connector.

b. Using two access keys supplied with terminal, unlock mainframe top cover by inserting one key in each of the keyways located on right and left sides of top cover. (Pushing keys into keyways unlock top cover. No key rotation is required.)

c. From front of mainframe, carefully swing top cover up until it latches into the half open position.

Note: The half open position provides adequate room for performing most service routines. However, if extensive repairs are to be made or if components contained in the top cover are to be serviced, fully open mainframe in accordance with step d.

CAUTION

Mainframe top hinges are open hinge type. When fully opening terminals do not allow top hinges to slip off hinge pins.

d. Firmly grasp top cover in one hand and release safety latch (see figure 1-1) by pressing it inboard with other hand. Then, using both hands, swing top cover up and over to a full open position (resting on its top).

1-3. ACCESSORY INSTALLATION PROCEDURES

The standard model terminal provides the capability for adding two printed circuit assembly type accessories. If more than two accessories are added, the HP 13240A 2640 Option Slot Extender must be installed first to accommodate the additional accessories. Instructions for installing add-on accessories are contained in paragraphs 1-4 through 1-9.

Note: After installing any accessory, always use the terminal self-test feature (Section III) to ensure proper operation.

1-4. HP 13240A OPTION SLOT EXTENDER INSTALLATION

The option slot extender accessory consists of a Backplane Extender Assembly, a Fan and Cable Assembly, and required attaching hardware. Installation of this accessory requires a set of Allen wrenches and a Phillips-head screwdriver. Install the accessory as follows:

a. Open terminal to its full open position in accordance with paragraph 1-2.

b. The CRT shield (see figure 1-1) is secured in place with snap fasteners. Remove CRT shield by pulling fasteners out of top cover mounting holes (see figure 1-2) and sliding toward the front of the CRT.

c. Disconnect High Voltage Cable Assembly (see figure 1-2) from CRT.

d. Disconnect Yoke Cable Assembly from Sweep Printed Circuit Assembly (PCA) connector P3 (see figure 1-2).

e. Disconnect Sweep Cable Assembly from Sweep PCA connector P1 (see figure 1-2).

f. Unlatch two snap locks (see figure 1-2), raise Sweep PCA from mainframe, disconnect CRT Cable Assembly from Sweep PCA connectors P2 and P4, and remove Sweep PCA.

g. Remove two Phillips-head screws and lockwashers securing two cable clamps (see figure 1-2) and wire harness to mainframe top cover. Retain mounting hardware for installing the Fan Assembly. Do not remove cable clamps from wire harness. (Vacated cable clamp holes will be used to mount Fan Assembly.)

h. Carefully connect connector J16 of Backplane Extender Assembly, part no. 02640-60002, to Backplane Assembly connector P1 (see figure 1-1).

i. Visually align Backplane Extender Assembly mounting holes with the four mounting holes (see figure 1-1) in bottom of mainframe and secure in place with four lockwashers and four Phillips-head screws.

Note: Fan and Cable Assembly must be mounted so that cables from fan are closest to back of top cover and CRT. Fan AIRFLOW arrow must point toward the back of the top cover.

j. Visually align Fan Assembly mounting holes with the four mounting holes (see figure 1-2) in mainframe top cover.

Note: Fan cable ground lug must be attached to one of the fan Allen-head mounting screws.

k. Secure Fan in place with four lockwashers and four Allen-head screws.

l. Remove power supply housing (bottom left side of mainframe) by unlatching the two snap locks on front of housing and pulling housing up and out toward front of mainframe.

m. Connect Fan Cable connector to Power Supply PCA connector J3 (see figure 1-1) and route cables back to fan with existing wire harness. The cable should be placed inside the first (left) cable clamp along with the existing harness. See figure 1-2.

n. Replace power supply housing and secure in place with the two snap locks.

o. Using two Phillips-head screws, two lockwashers, and two nuts, secure two cable clamps and the wire harness to mounting holes in top of fan frame closest to back of mainframe.

p. Connect CRT Cable Assembly to Sweep PCA connectors P2 and P4.

q. Connect Yoke Cable Assembly to Sweep PCA connector P3.

r. Connect Sweep Cable Assembly to Sweep PCA connector P1.

s. Install Sweep PCA in mainframe top cover and secure in place with the two snap locks.

t. Connect High Voltage Cable Assembly to CRT.

u. Secure CRT shield in place by sliding the front of the shield over the CRT mounting bracket and pressing the snap fasteners into the mounting holes.

v. Check and, if necessary, adjust power supply in accordance with paragraph 3-9.

w. Firmly grasp mainframe top cover in both hands and carefully swing it up and over to its half open position assuring correct union of cover hinges.

x. Firmly grasp top cover in one hand and release safety latch by pressing it inboard with other hand. Then using both hands, carefully lower top cover to its closed position.

1-5. HP 13238A TERMINAL DUPLEX REGISTER INSTALLATION

These instructions apply to both the HP 13238A and HP 13238A-001 add-on accessories. To install the HP 13238A accessory, perform all the following steps except steps d and e. To install the HP 13238A-001 accessory, perform all the following steps.

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Configure jumpers in Terminal Duplex Register PCA jumper sockets as shown in figure 1-3.

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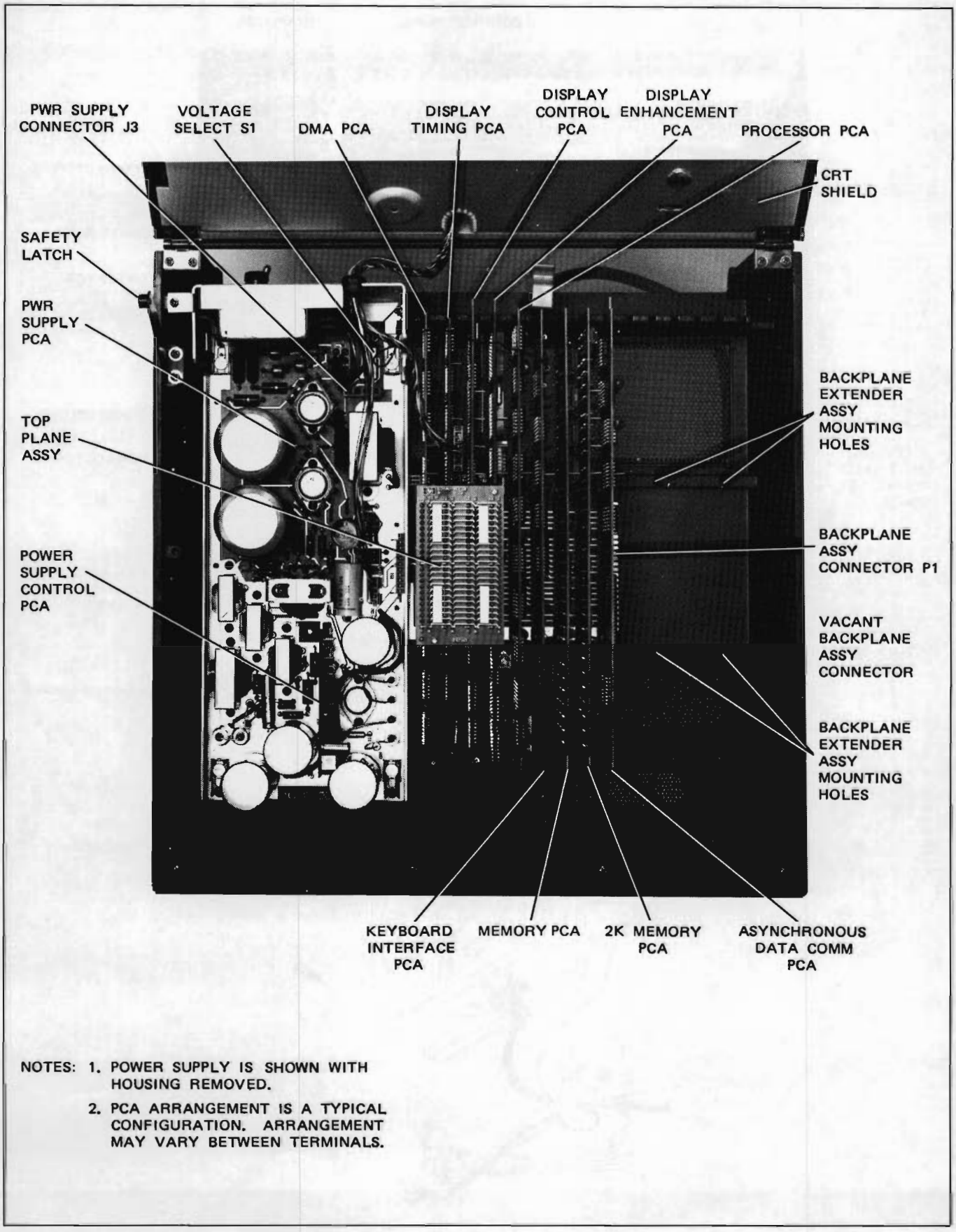
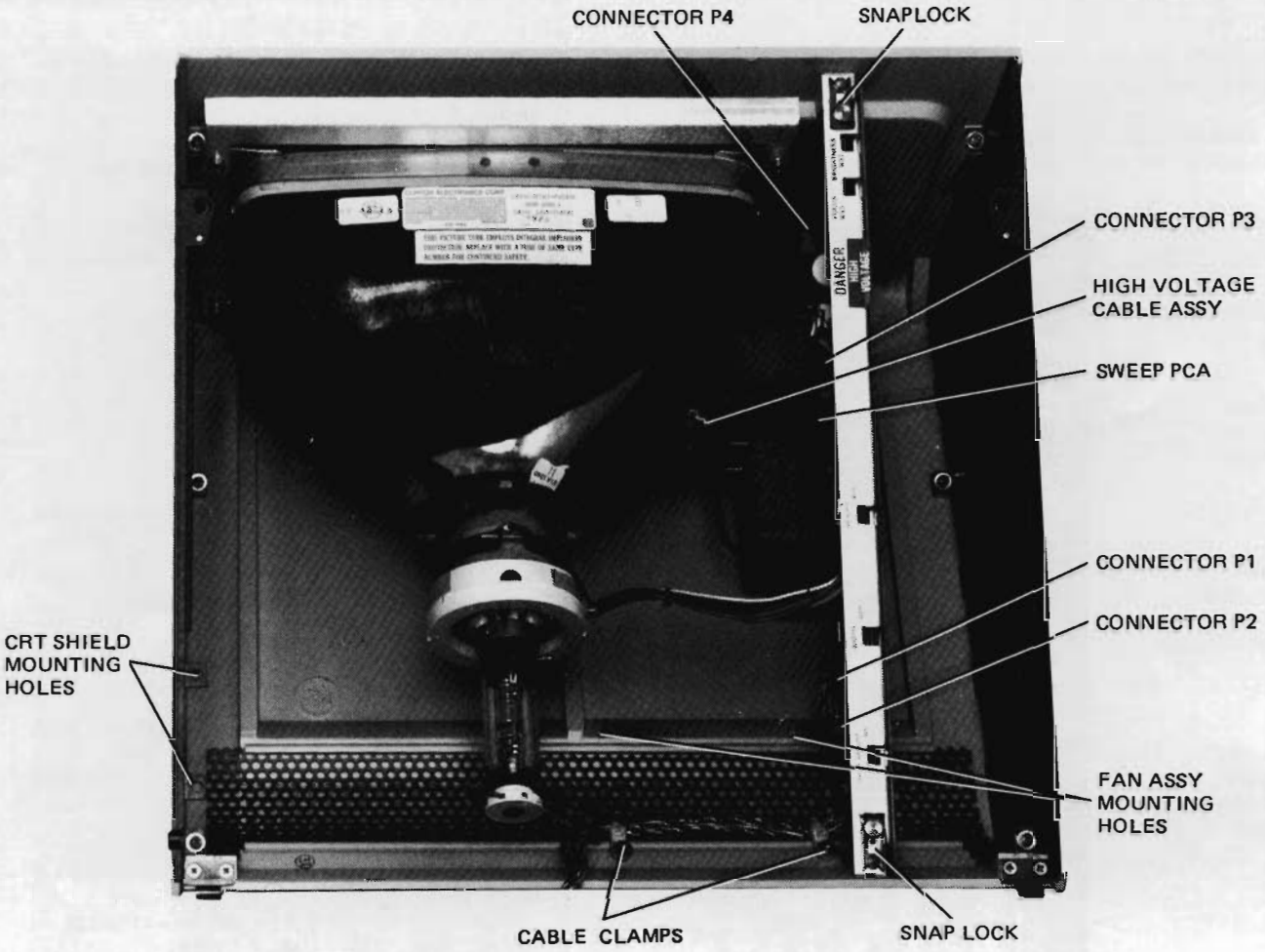
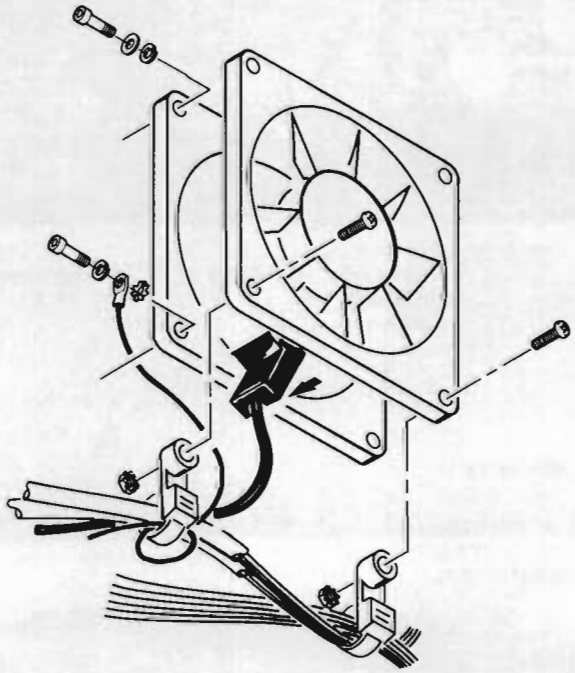


NOTES: 1. POWER SUPPLY IS SHOWN WITH HOUSING REMOVED.

2. PCA ARRANGEMENT IS A TYPICAL CONFIGURATION. ARRANGEMENT MAY VARY BETWEEN TERMINALS.

Figure 1-1. Mainframe Bottom Part Locations





Fan and Cable Assembly Installation

Figure 1-2. Mainframe Top Part Locations

c. Install Terminal Duplex Register PCA in first vacant Backplane Assembly connector adjacent to existing PCA's.

Note: To ensure proper terminal operation, all PCA's must be installed in adjacent Backplane Assembly connectors. There should never be vacant connectors between PCA's.

CAUTION

Do not attempt to force hood connector on PCA connector. Failure to comply may result in damage to both the hood connector and PCA.

d. Open mainframe rear door by twisting two lock extrusions.

e. Holding Terminal Duplex Register PCA firmly in place, carefully connect hood connector of HP 9866 Cable Assembly, part no. 13238-60001, to PCA connector P2.

Note: The hood connector and PCA connector P2 are identically keyed to prevent inadvertant erroneous connections. Connecting the two together requires minimal hand pressure. If excessive resistance is encountered, an incorrect connection is being attempted.

Note: For printer interfacing information refer to the *HP 9866A Printer Service Manual*, part no. 09866-90030.

f. Check and, if necessary, adjust power supply in accordance with paragraph 3-9.

g. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-6. HP 13246A PRINTER SUBSYSTEM (9866)

This accessory consists of a Terminal Duplex Register PCA, part no. 02640-60031; a 9866 Cable Assembly, part no. 13238-60001; and an HP 9866A Printer. To install this accessory, first perform the installation instructions contained in paragraph 1-5, steps a through g. After the PCA and cable assembly have been installed, install the printer in accordance with the instructions contained in the HP 9866A *Printer Peripheral Manual*, part no. 09866-90000 and the HP 9866A *Printer Service Manual*, part no. 09866-90030.

1-6a HP 13250A ASYNCHRONOUS DATA COMM/SERIAL PRINTER INTERFACE

This accessory consists of a Serial Printer Interface PCA (part number 02640-60089) and a cable. The cable used will vary according to peripheral device requirements. The interface can be used in RS232C and current loop data communication applications. A complete description of this accessory is contained in 13250A Data Communications/Serial Printer Interface Operating and Service Manual (part number 02640-90042).

Note: The 13250A accessory can be used as a serial printer interface with HP 2640A terminals having option 015 (50 Hz) with serial prefix 1551A or 1608A. Contact your nearest Hewlett-Packard Sales and Service Office for information on upgrading terminals with other prefix numbers.

1-7. HP 13231A DISPLAY ENHANCEMENTS INSTALLATION

These instructions apply to the HP 13231A-201 and HP 13231A-202 accessories as well as the HP 13231A accessory. The HP 13231A accessory consists of a Display Expansion PCA, part no. 02640-60024; a Top Plane Connector Assembly, part no. 02640-60022; and a Connector Removal Tool, part no. 02640-00029. The HP 13231A-201 and -202 accessories consist of the same three items with the applicable ROM IC's mounted on the Display Expansion PCA. Install any of these accessories as follows:

The alternate character sets are configured with jumpers located on the upper right corner of the Display Enhance-

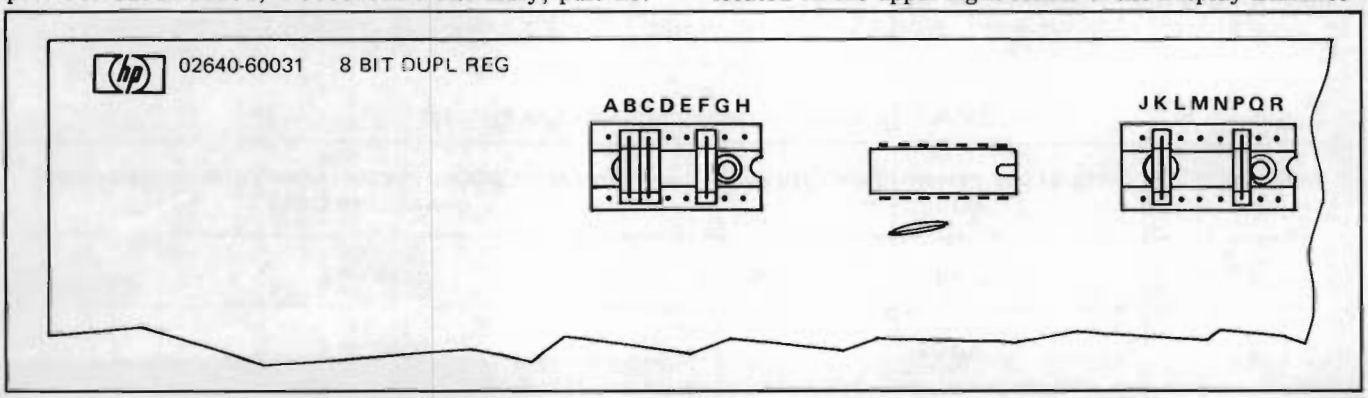


Figure 1-3. Terminal Duplex Register PCA Jumper Configuration

ment PCA. There are six jumpers, two for each of the three possible alternate character sets. Jumpers 1 and 2 are for alternate character set 1 (referred to as set A in the Owner's Manual), jumpers 3 and 4 are for alternate character set 2 (set B in the Owner's Manual), jumpers 5 and 6 are for alternate character set 3 (set C in the Owner's Manual).

The first jumper for each set (jumpers 1, 3, and 5) indicates whether the set is composed of 128 (jumper in) or 64 (jumper out) characters. The second jumper for each set (jumpers 2, 4, and 6) indicates whether the character set data is in alphanumeric (jumper in) or microvector (jumper out) format. A detailed description of data formats for alternate character sets is given in the application note: *2640 Series Character Set Generation* (part number 13245-90001).

When using the two standard alternate character sets (Math Set and Line Set) the jumpers would normally be configured as follows:

Math Set (placed in the first socket of set 1)

Jumper 1 = Out Since only 64 characters are used.

Jumper 2 = In Since character data is in alphanumeric format.

Line Set (placed in the first socket of set 2)

Jumper 3 = Out Since only 64 characters are used.

Jumper 4 = Out Since character data is in microvector form.

Note that the Math Set has been shown as alternate character set 1 (A in the Owner's Manual) and the Line Set as alternate 2 (B in the Owner's Manual). They could have been configured as any combination of the three possible alternate sets. There is no requirement that the sets be configured in any order.

Note: Do not confuse the 128/64 character jumpers for *alternate character sets* with the 128 character jumper for the *standard character set* discussed on page 1-8.

Effect of Improper Jumper Placement

128 Characters Strapped for 64. When a 128 character set is used and is jumpered for 64 characters, only the first 64 characters in the set will be accessed. This will cause the "q" character for example to access the same display character as the "Q" character.

64 Characters Strapped for 128. Any attempt to access one of the lower case 64 characters ("a", "q", etc) will result in a blank being displayed.

Alphanumeric Data Strapped as Microvector. Alphanumeric data strapped as microvector will normally result in characters that are skewed or fuzzy.

Microvector Data Strapped as Alphanumeric. Microvector data strapped as alphanumeric will display blanks for the microvector characters.

a. Using figure 1-4 and table 1-1 as a guide, check that Display Expansion PCA jumpers are arranged correctly for the ROM character set configuration. If there are no alternate character set ROM's installed (HP 13231A), all jumpers should be in the jumper socket.

b. Open terminal to its half open position in accordance with paragraph 1-2.

c. Insert connector removal tool under Top Plane Assembly as shown in figure 1-5.

d. Remove Top Plane Assembly by pressing down on connector removal tool handle. Retain Top Plane Assembly for possible future use.

e. If necessary, rearrange PCAs in Backplane Assembly so that an unused connector is available for the Display Expansion PCA adjacent to the Display Memory Access (DMA), Display Control, and Display Timing PCA's.

Note: PCA arrangement can be in any configuration with the following exceptions. The Keyboard Interface PCA should be installed in one of the first three Backplane Assembly connectors closest to the power supply.

Table 1-1. Display Expansion PCA Jumper Protocol

ALTERNATE SET	128/64 (JUMPER IN/JUMPER OUT) CHARACTERS	ALPHANUMERIC/MICROVECTOR (JUMPER IN/JUMPER OUT) CHARACTER DATA
A	JUMPER 1	JUMPER 2
B	JUMPER 3	JUMPER 4
C	JUMPER 5	JUMPER 6

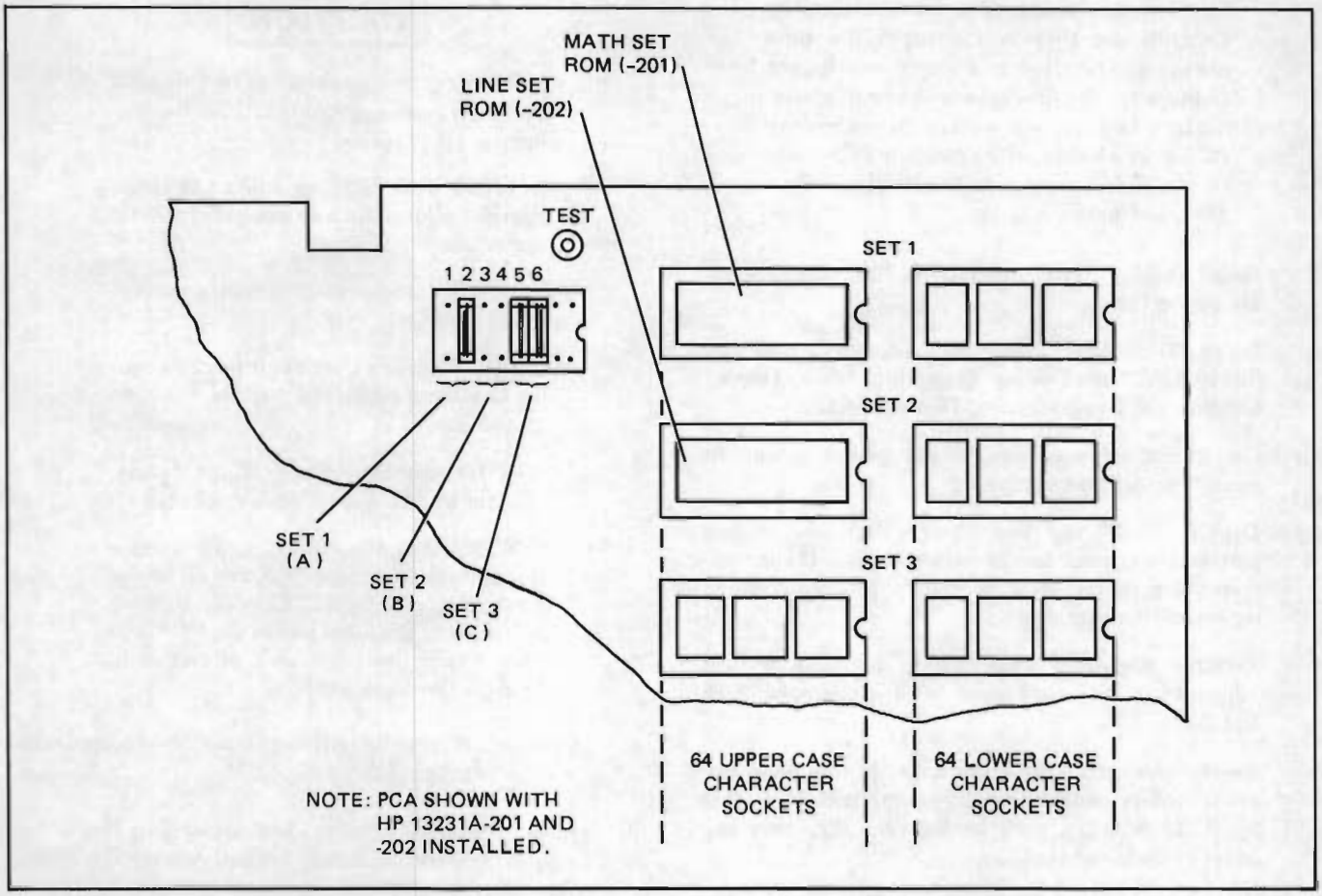


Figure 1-4. Display Expansion PCA Jumper and ROM Socket Locations

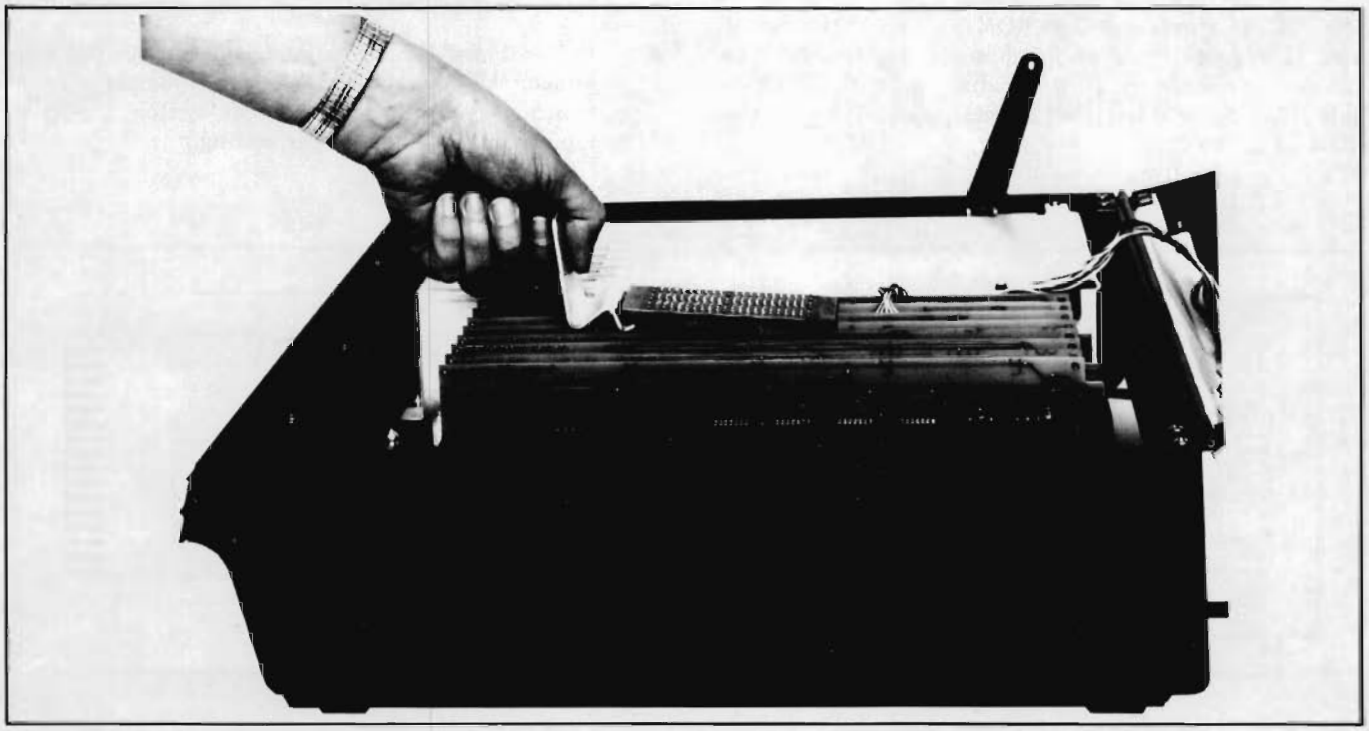


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Figure 1-5. Top Plane Assembly Removal

The Display Expansion, DMA, Display Control, and Display Timing PCA's must always be installed as a group in adjacent connectors. No Backplane Assembly connectors can be left vacant between any PCA's. In addition, the Processor PCA must be installed adjacent to the display PCA's described previously.

f. Install Display Expansion PCA in Backplane Assembly connector.

g. Install Top Plane Connector Assembly, part no. 02640-60022 on Display Expansion, DMA, Display Control, and Display Timing PCA connectors.

h. Check and, if necessary, adjust power supply in accordance with paragraph 3-9.

i. Depress TEST key and observe last line of test pattern for correct display enhancements. If enhancements are correct skip to step k. If adjustment is necessary, perform step j.

j. Perform brightness, half bright, focus, and field adjustments in accordance with paragraphs 3-10 and 3-11.

k. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-7a 64 CHARACTER LOWER CASE ROM

The 64 Character Lower Case ROM, part no. 1816-0613, is used to upgrade standard 64 character set terminals to 128 Roman characters. Do not confuse this with the alternate character sets described in paragraph 1-7. Install the ROM as follows:

CAUTION

MOS integrated circuits can be damaged by electrostatic discharge. Use the following precautions:

DO NOT wear clothing subject to static charge buildup, such as wool or synthetic materials.

DO NOT handle MOS circuits in carpeted areas.

DO NOT remove the circuit from its conductive foam pad until you are ready to install it.

AVOID touching the circuit leads. Handle by the plastic package only.

INSURE that the circuit, work surface (table, desk, etc.) and PCA are all at the same ground potential. This can be done by touching the foam pad to the PCA and then touch the foam pad, circuit, and PCA to the work surface.

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Insert connector removal tool under Top Plane Assembly as shown in figure 1-5 and remove Top Plane Assembly by pressing down on connector removal tool handle.

c. Locate and remove Display Control PCA from Backplane Assembly.

d. Using figure 1-5a as a guide, locate the 128 CH jumper W1 position and solder in a jumper. (If the board uses a jumper socket or switch, insert a jumper or make the proper setting.)

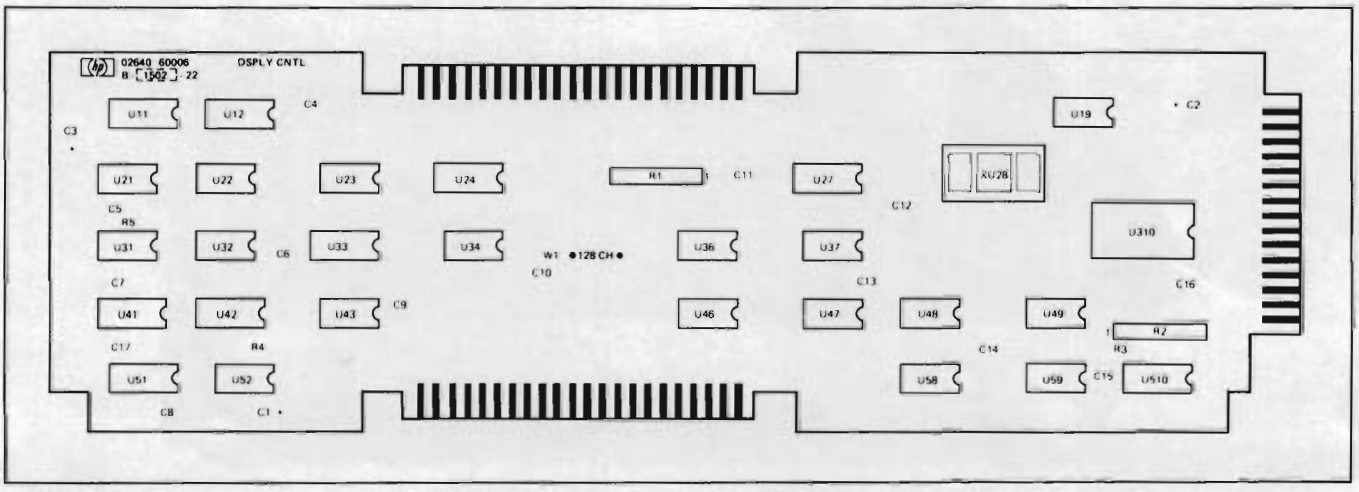

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Figure 1-5a. Display Control PCA Component Locations

e. Locate the vacant lower case ROM socket XU28.

f. Carefully insert 64 Character Lower Case ROM in socket XU28 so that ROM pin 1 is at upper right corner of XU28.

g. Reinstall Display Control PCA in Backplane Assembly connector from which it was removed.

h. Reinstall Top Plane Assembly on DMA, Display Timing, and Display Control PCA's top connectors.

i. Firmly grasp top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-8. HP 13233A AND HP 13234A TERMINAL MEMORY MODULES

Install the HP 13233A (+2K) and/or HP 13234A (+4K) memory accessories as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Locate and remove Control Store PCA, part no. 02640-60003, from Backplane Assembly (see figure 1-1).

c. Using figures 1-6, 1-7, and 1-8 as a guide, locate memory jumpers on Control Store, 2K Memory, and/or 4K Memory PCA's.

d. Using figures 1-9 and 1-10 as guides, arrange PCA starting address jumpers to select appropriate memory starting address for the size memory being configured.

Note: If a full 8K of memory is to be configured, the 1K block of basic memory is not used and must be located outside the zero to 16K of memory space.

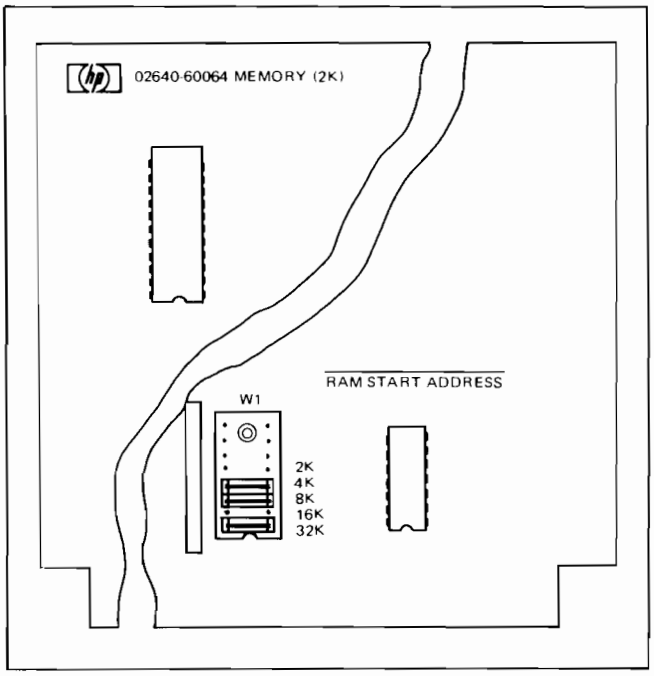


Figure 1-7. 2K Memory PCA Jumper Socket Location

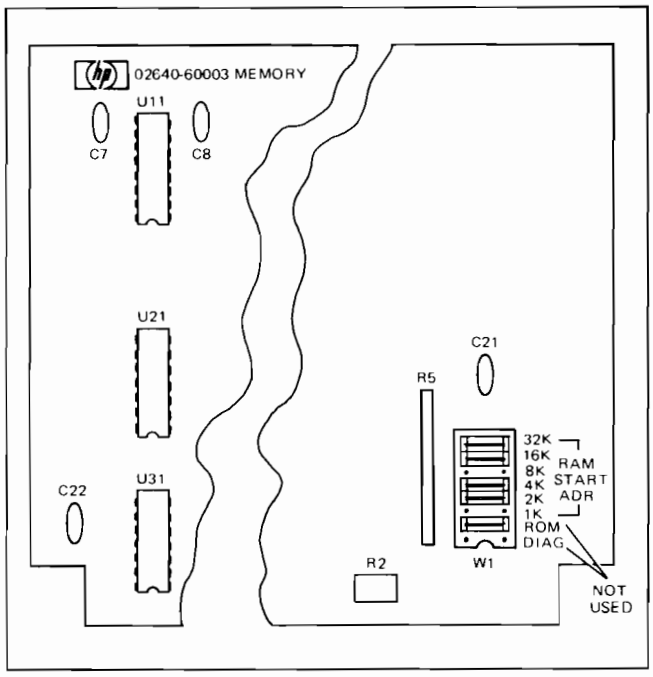


Figure 1-6. Control Store PCA Jumper Socket Location

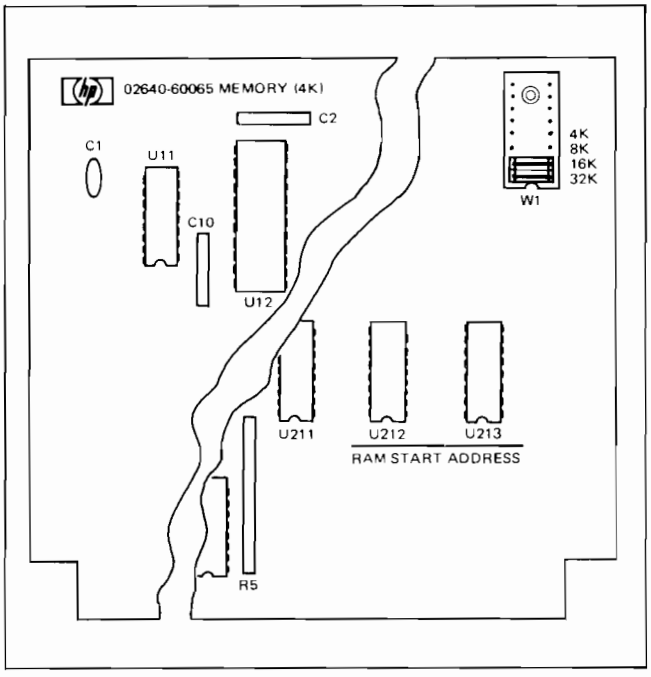


Figure 1-8. 4K Memory PCA Jumper Socket Location

e. Install memory PCA's in any vacant Backplane Assembly connectors ensuring that no connectors are left vacant between any PCA's.

f. Check and, if necessary, adjust power supply in accordance with paragraph 3-9.

g. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-9. HP 13245A CHARACTER SET GENERATION KIT

The Character Set Generation Kit Accessory consists of a PROM Character PCA, part no. 02640-60053 and a Connector Assembly, part no. 02640-60070. Install the HP 13245A accessory as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Rearrange PCA's in the Backplane Assembly so that an unused connector is available for the PROM Character PCA adjacent to either the Display Control PCA or Display Expansion PCA depending on the character set(s) to be replaced. If the base character set is to be replaced, vacate a connector adjacent to the Dis-

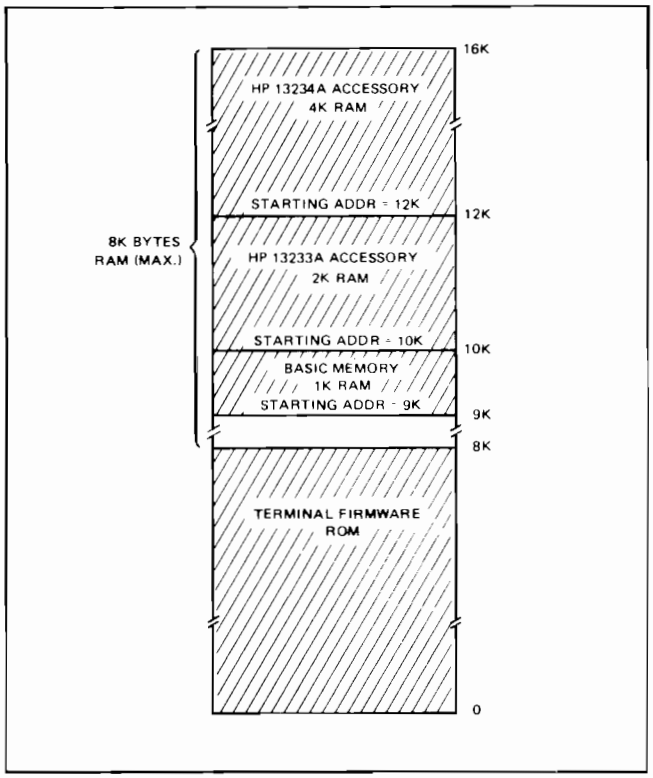
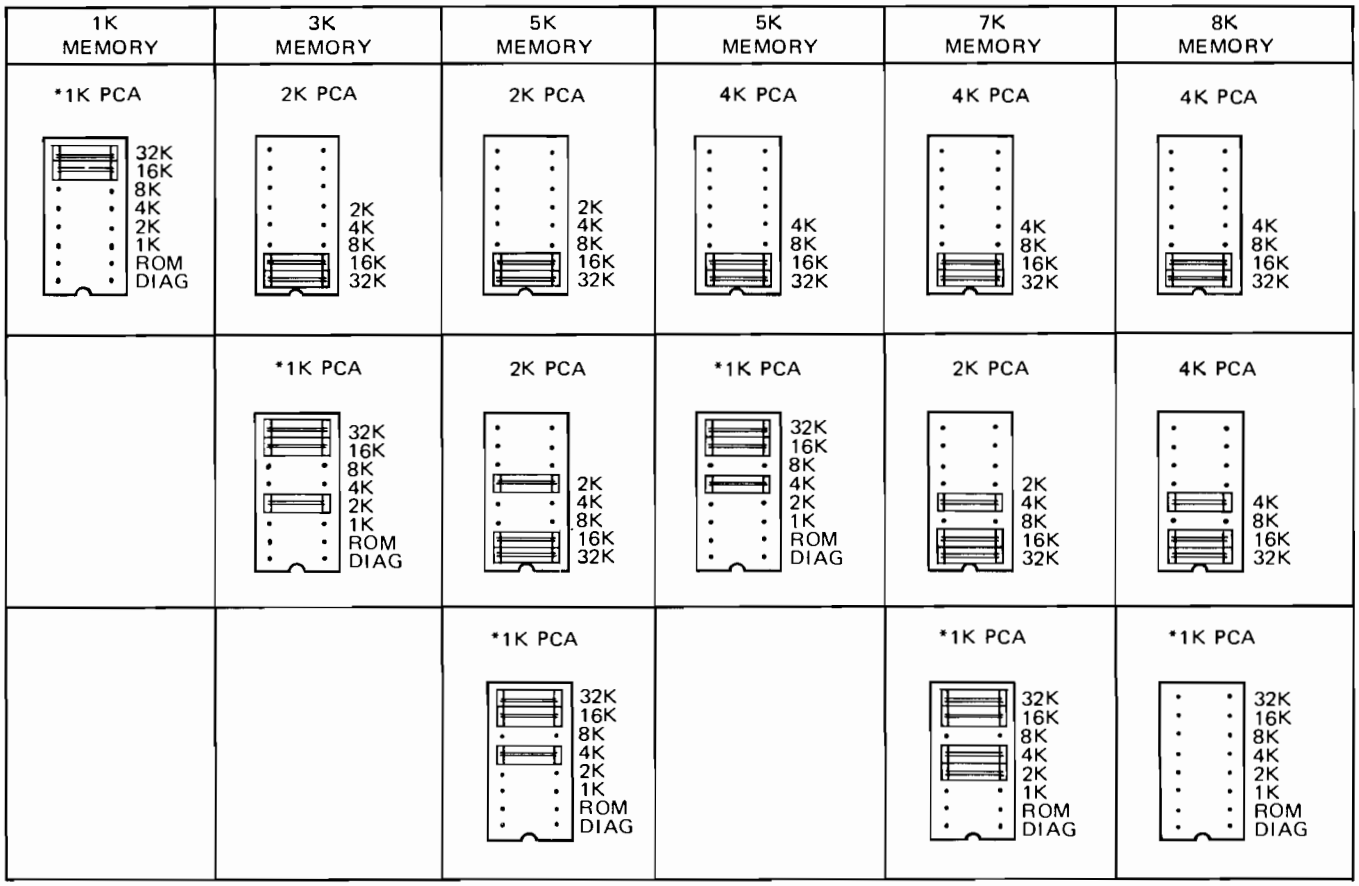


Figure 1-9. Typical Memory Map (7K)



* CONTROL STORE PCA

Figure 1-10. Memory Addressing Jumper Combinations

play Control PCA. If an alternate character set(s) is to be replaced, vacate a connector adjacent to the Display Expansion PCA.

Note: PCA arrangement can be in any configuration with the following exceptions. The Keyboard Interface PCA should always be installed in one of the first three slots in the Backplane Assembly connector closest to the power supply. This allows a short connection path for the keyboard ground strap. The Display Expansion, DMA, Display Control, and Display Timing PCAs must always be installed as a group in adjacent connectors to accommodate the Top Plane Connector Assembly. No Backplane Assembly connectors can be left vacant between any PCA's.

c. Install PROM Character PCA in vacated Backplane Assembly connector.

Note: The base or alternate character set ROM(s) to be replaced by the user generated PROM set(s) must be removed from the applicable PCA in accordance with the instructions contained in the *Character Set Generation Kit Application Note*, part no. 13245-90001.

d. When connected to the Display Expansion PCA, the PROM Character PCA character sets 1 and 2 replace the Display Expansion PCA character sets 1 and 2, respectively. If an alternate set(s) is to be replaced, first determine if the user generated PROM set(s) is alphanumeric or microvector. Then, using table 1-1 and figure 1-4 as a guide, correctly arrange Display Expansion PCA jumpers 2 and 4 for the PROM character set type(s). (Jumpers 1 and 3 can either be removed or left installed.)

e. Attach Connector Assembly, part no. 02640-60070 between the two interface connectors (P2) on the PROM Character PCA and Display Control PCA or Display Expansion PCA.

f. Check and, if necessary, adjust power supply in in accordance with paragraph 3-9.

g. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-10. SELECTING LINE VOLTAGE

The terminal can be operated from either 115 or 230V, 60 Hz line voltage (230V, 50 Hz optional). When shipped from the factory, the line voltage for which the terminal is configured is stamped on the mainframe rear panel identification label. If it is necessary to change the operating line voltage, ensure that power cord is disconnected and proceed as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Remove power supply housing (bottom left side of mainframe) by unlatching the two snap locks on front of housing and pulling housing up and out toward front of mainframe.

c. Using an access key or screwdriver, set voltage select switch S1 (see figure 1-1) to 115V or 230V as applicable.

d. Insert appropriate fuse for selected line voltage in rear panel fuse holder F1 and mark selected line voltage on identification label.

e. Check and, if necessary, adjust power supply in accordance with paragraph 3-9.

f. Replace power supply housing and secure in place with the two snap locks.

g. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

h. Perform terminal self-test.

1-11. SELECTING OPTIONAL OPERATING FUNCTIONS

The terminal is equipped with jumper selectable options that can be used to alter some of its operating functions. These options and their effects on terminal operation are discussed in paragraphs 1-12 through 1-16. To select an operating option, proceed as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Locate and remove Keyboard Interface PCA, part no. 02640-60019 from Backplane Assembly connector closest to power supply.

c. Using figure 1-11 as a guide, remove applicable jumper(s) from Keyboard Interface PCA jumper socket. Retain removed jumper(s) for possible future use.

d. Reinstall Keyboard Interface PCA in vacated Backplane Assembly connector closest to power supply.

e. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

f. Perform terminal self-test.

1-12. FUNCTION KEY TRANSMISSION OPTION

Normally, the Function Key Transmission Option is disabled (jumper A installed). Pressing such keys as ROLL UP, NEXT PAGE, etc., cause immediate execution of the function by the terminal but the applicable ASCII code for the function is not transmitted to the CPU. If Jumper A is removed, the ASCII codes for the functions are transmitted to the CPU as the keys are pressed and, if operating in half duplex, the function is also executed by the terminal.

1-13. SPACE OVERWRITE LATCH OPTION

Normally, the Space Overwrite Latch Option is disabled (jumper B installed) and the space overwrite latch is never set. In this case, when blanks (spaces) are entered into previously occupied character positions, the existing characters are overwritten. If jumper B is removed, the space overwrite latch is set by a carriage return and reset by a line feed, home, or horizontal tab. When set, blanks (spaces) typed or received are interpreted as cursor-right functions and and existing characters are not overwritten.

1-14. END-OF-LINE WRAP AROUND OPTION

Normally, the End-Of-Line Wrap Around Option is enabled (Jumper C installed) and when a character is typed or received into column 80 of a line, the terminal automatically generates a carriage return and line feed, and the cursor is moved to the beginning of the next lower line. If jumper C is removed, an automatic carriage return and line feed is not generated at the end of each line and the cursor remains in column 80. Any subsequent characters typed or received replace the existing 80th character until some cursor movement function is typed or received that moves the cursor out of column 80.

1-15. BLOCK MODE OPTION

Normally, the Block Mode Option is disabled (jumper D installed) and the terminal is set for line-field operation. When set for line-field, all block transmissions are terminated by a carriage return followed by an optional line feed. If jumper D is removed, the terminal is set for page operation and all block transmissions are terminated with an RS. This jumper is ignored when the terminal is operated in Character Mode.

1-16. ALTERNATE CONTROL ACTION KEY OPTION

Normally (jumper E installed), the terminal generates associated escape code sequences for the f_1 through f_8 keys when the keys are pressed while holding the CNTL key down. If the keys are pressed without using the CNTL key, the functions printed below the keys are performed. If jumper E is removed, the operations are reversed. The escape code sequences are generated when the keys are pressed without using the CNTL key and the printed functions are performed when the keys are pressed in conjunction with the CNTL key. It is suggested that the jumper be left installed if the terminal is generally used for program development. If the terminal is to be used primarily in an applications environment which uses the f_1 through f_8 keys, it is more convenient if the jumper is removed.

1-16a. 2640/2644 MODE (Jumper F)

The 2640/44 Mode strap (jumper F) alters the sequence of control signals sent to a computer during block data transfers. The action of the escape code sequence to reset the terminal is also changed.

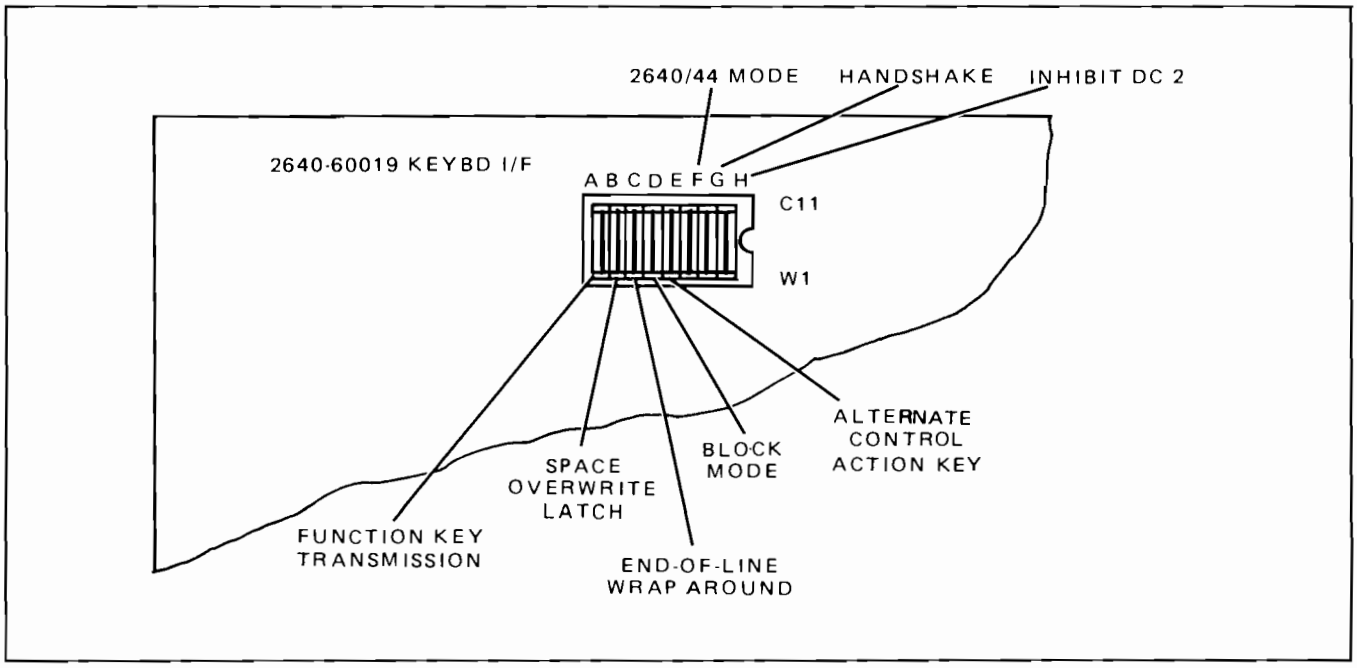


Figure 1-11. Keyboard Interface PCA Jumper Identifications

Note: This jumper is only effective on terminals having option 015 and a serial prefix of 1551A or 1608A. All other terminals will operate as if the jumper were in place, regardless of actual jumper position. Contact your nearest Hewlett-Packard Office for information on upgrading terminals with other prefix numbers.

DC2 Transmission

If the mode strap (jumper F) is in place and the ENTER key is pressed, the terminal will immediately send a DC2 character. Also, if the terminal is strapped for page mode (jumper D out) the terminal will immediately send the DC2 character when one of the function keys (f1 through f8) is pressed. The DC2 character is sent before the escape sequence associated with the function key is sent.

If the mode strap (jumper F) is out, the DC2 character is sent only after a DC1 character is received from a computer. (Note that a DC1 received just prior to the operator striking the ENTER or function keys (f1-f8) would be sufficient to cause the terminal to send the DC2 character.

ESCape E (Reset Terminal)

If the MODE strap (jumper F) is out, the ESC E character sequence will have the same effect as the RESET TERMINAL key. When the jumper is out and the escape sequence is received from a computer, the computer must then wait at least 200 milliseconds before sending additional data. This allows the terminal sufficient time to clear its RAM memory. Data sent to the terminal during this 200 millisecond interval may be lost.

If the MODE strap (jumper F) is in, the ESC E character sequence will not clear the terminal's memory. Only the electronically latching keys (MEMORY LOCK, FORMAT MODE, and INSERT CHARACTER) and transfer requests (terminal status, cursor sense, function key, and display transfer) are cleared. The terminal's memory is not cleared and it is not necessary to allow any delay time before sending additional data to the terminal.

1-16b. HANDSHAKE (Jumper G)

The Handshake strap (jumper G) controls the transmission of DC2 characters during block transfers. When jumper G is out, the terminal precedes all block transfers with the DC2 character, regardless of the setting of the BLOCK MODE key. Block transfers include cursor sensing, terminal status, display transfers initiated by pressing the ENTER key (or generating its escape sequence), or by pressing one of the function keys (f1 through f8). The DC2 character will be sent regardless of the setting of the BLOCK MODE key. (The function of the jumper can be disabled with the INHIBIT DC2 strap.)

Note: This jumper is only effective on terminals having option 015 and a serial prefix of 1551A or 1608A. All other terminals will operate as if the jumper were in place, regardless of actual jumper position. Contact your nearest Hewlett-Packard Office for information on upgrading terminals with other prefix numbers.

In the case of keyboard initiated block transfers (ENTER or function keys) the 2640/2644 MODE strap (jumper F) determines whether the DC2 character is sent immediately or in response to a DC1 character received from the computer. Block transfers triggered by escape sequences always require a DC1 character from the computer before the DC2 will be sent. (Note that a second DC1 must be received from the computer before the subsequent data can be sent.)

When jumper G is in place the DC2 character is only sent before transfers initiated by the ENTER key when the terminal is in BLOCK MODE or by the function keys (f1-f8) when the terminal is in the BLOCK MODE and is strapped for page mode (jumper D out).

1-16c. INHIBIT DC2 (Jumper H)

The INHIBIT DC2 strap (jumper H) can be used to stop the automatic transmission of the DC2 character. (Refer to the descriptions of other control strappings.) Normal operation occurs when jumper H is in place. This allows the DC2 character to be sent automatically depending on the position of the other control straps.

Note: This jumper is only effective on terminals having option 015 and a serial prefix of 1551A or 1608A. All other terminals will operate as if the jumper were in place, regardless of actual jumper position. Contact your nearest Hewlett-Packard Office for information on upgrading terminals with other prefix numbers.

When jumper H is out and an operation is performed that would normally send the DC2 character to the computer, the DC2 is not sent and the data is sent immediately instead. Even if the HANDSHAKE strap (jumper G) is out, the DC2 character will not be sent. For example, pressing one of the function keys (f1-f8) with the terminal in BLOCK MODE and strapped for PAGE operation (jumper D out), would normally cause a DC2 character to be sent before the escape sequence. The computer would respond with a DC1 which would cause the terminal to send the escape sequence associated with the function key.

With jumper H out, pressing a function key would cause the escape sequence to be sent immediately, without sending a DC2 character and without waiting for a DC1 character from the computer.

In addition, when jumper H is out, and the ENTER key is pressed while in BLOCK MODE, the cursor will be placed in the first column of the current line (line mode - jumper D in) or in the Home position (page mode - jumper D out) before the data is sent.

1-17. UNPACKING AND REPACKAGING FOR SHIPMENT

1-18. UNPACKING

The terminal has been carefully inspected and tested prior to shipment from the factory. Upon receipt, visually inspect the shipping carton for evidence of damage. If the shipping carton is damaged, request that the carrier's agent be present when the terminal is unpacked. Remove the terminal components from the shipping carton in accordance with the unpacking instructions listed below and check each item against the packing slip to ensure complete and correct delivery. Visually inspect all items for damage. If any of the items are damaged or fail to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. The HP Sales and Service Office will arrange for the repair or replacement of any damaged items without waiting for any claims against the carrier to be settled. Perform the unpacking instructions carefully so that the shipping carton can be retained for possible future use such as storage or reshipment of the terminal. Unpack your terminal as follows:

a. Open top of shipping carton and top of exposed inner keyboard carton.

b. Remove first foam liner from keyboard carton.

c. Remove owner's manual, installation and service manual, and, if supplied, data communication interface cable assembly from keyboard carton.

d. Remove second foam liner from keyboard carton.

e. Remove Keyboard and Cable Assembly, Power Cord Set, and two mainframe Access Keys from third foam liner in keyboard carton.

f. Replace two foam liners removed from keyboard carton and remove keyboard carton from shipping carton.

g. Remove cardboard tray from shipping carton.

h. Open top of floater carton and remove foam liner.

1-19. REPACKAGING FOR SHIPMENT

1-20. SHIPMENT USING ORIGINAL PACKAGING. The same containers and materials used in factory packaging can be used for reshipment of the terminal. Alternatively, containers and packing materials can be obtained from Hewlett-Packard Sales and Service Offices. If the terminal is being shipped to the factory for servicing, attach a tag to the terminal specifying the return address, the type of service required, the terminal model number, and the full serial number of the terminal. Mark the carton "FRAGILE" to ensure careful handling. In any correspondence, refer to the terminal by model number and full serial number.

Note: The terminal mainframe is shipped in a plastic bag, face down (back of mainframe visible), inside the floater carton with a cardboard filler wedged between the bottom of the mainframe and the floater carton foam liner.

i. Determine bottom of mainframe by locating cardboard filler and carefully tip over entire shipping carton so that mainframe is setting upright.

j. Remove cardboard filler and carefully slide mainframe out of floater carton and shipping carton.

k. Remove mainframe from plastic bag.

l. Return entire shipping carton to its upright position.

m. Place plastic bag, cardboard filler, and foam liner back inside floater carton and close cover.

n. Place cardboard tray inside shipping carton on top of floater carton and set keyboard carton in tray.

o. Close top cover of shipping carton and retain for possible future use.

p. Install the terminal in accordance with the initial installation instructions contained in the *HP 2640A Interactive Display Terminal Owner's Manual*, part no. 02640-90011.

1-21. SHIPMENT USING NEW PACKAGING. The following instructions should be followed when packaging the terminal with commercially available materials:

a. Wrap the terminal in heavy paper or sheet plastic. If shipping the terminal back to the factory, first attach a tag to the terminal with the return address and indicate the type of service required, the terminal model number, and full serial number.

b. Use a strong shipping carton. A double-wall carton of 350-pound test material is adequate.

c. Ship the terminal mainframe face down in the shipping carton.

d. Use enough shock absorbing material (3- to 4-inch layer) on all sides of the terminal and keyboard to provide a firm cushion and to prevent movement inside the carton. Use particular care to protect corners, top of keyboard, and front of mainframe.

e. Seal the carton securely and mark it "FRAGILE" to ensure careful handling.

f. In any correspondence with the factory, refer to the terminal by model number and full serial number.

FUNCTIONAL OPERATION

SECTION II

2-1. INTRODUCTION

This section contains a block diagram level theory of operation discussion for the terminal and a pin-to-pin wiring diagram of the terminal.

2-2. GENERAL DISCUSSION

As shown in figure 2-1, the terminal basically consists of a power supply section, display section, memory section, control section, and input/output section. The interaction of these sections to provide the terminal's capabilities is discussed briefly in the following paragraphs. (A more detailed discussion is contained in paragraphs 2-3 through 2-32.)

The power supply section consists of a Power Supply PCA and a Power Supply Control PCA that convert the primary power source into required operating voltages and basic clock pulses for the terminal. Except for the Sweep PCA, all interfacing between the power supply section and other terminal modules is provided by the Backplane Assembly.

The display section consists of a display controller subsection, Sweep PCA, CRT display, and, if installed, a Display Expansion PCA and PROM Character PCA. The display controller subsection generates all timing and control signals for the display section, provides drive signals for the Sweep PCA, initiates ASCII character (data) transfers from the memory section, and converts the ASCII characters into video drive signals. When installed, the Display Expansion PCA generates the required drive signals to add half bright, underline, and blinking display enhancements to the CRT and provides the capability for adding up to three additional 128 character sets to the terminal. (Refer to paragraph 1-7.) When installed, the PROM Character PCA provides the capability for adding up to two user generated character sets that can be used to replace the base character set on the Display Control PCA or two existing alternate character sets on the Display Expansion PCA. Set selection and data signal transfers between the PROM Character PCA and the Display Control or Display Expansion PCA's is provided by a separate connector assembly attached between the PCA's. The Sweep PCA is controlled by the Display Timing and Display Control PCA's (also the Display Expansion PCA when installed) and generates all drive signals, including filament and high voltages required by the CRT display. Timing and control signal interfacing between the display controller subsection modules (including the Display Expansion PCA when installed) is provided by the Top Plane Assembly. Data, associated transfer signals, and address interfacing between the subsection modules and other terminal modules is provided by the Backplane Assembly.

The control section is the central processing unit of the terminal and consists of the Processor PCA and part of the Control Store PCA. The Processor PCA fetches instructions from the operating system section (ROM) of the Control Store PCA and executes them; accessing the memory section, implementing input/output section modules or, if installed, implementing the Display Expansion PCA. In addition, the control section also controls and directs received byte information to the display section for translation from ASCII code into video signals. All signal interfacing between the control section and the other terminal modules is provided by the Backplane Assembly.

The memory section provides the operator with the usable RAM storage capability of the terminal. This section consists of part of the Control Store PCA (1K RAM) and, if installed, the +2K and +4K Memory PCA's. The +2K Memory PCA adds 2048 eight-bit bytes of random access memory to the terminal. The +4K Memory PCA adds 4096 bytes of memory to the terminal. All read/write memory is accessed by the Processor PCA through the Backplane Assembly.

The input/output section is divided into a keyboard subsection, computer subsection, and peripheral subsection. All three subsections are implemented by the control section through the Backplane Assembly. The keyboard subsection consists of the Keyboard Assembly and Keyboard Interface PCA which provide direct data and instruction entry by the terminal operator. The computer subsection consists of the Asynchronous Data Comm PCA and an interface cable assembly which provide a communication link between the terminal and an external computer. The peripheral subsection, if installed, consists of the Terminal Duplex Register PCA and an interface cable assembly which provide a communication link between the terminal and an external peripheral device such as a paper printer.

2-3. DETAILED DISCUSSION

The Functional operation discussion contained in the following paragraphs is keyed to the functional block diagram, figure 2-2. Figure 2-3 is a pin-to-pin wiring diagram of the terminal.

2-4. POWER SUPPLY SECTION

As shown in figure 2-2, the power supply section consists of a Power Supply PCA and a Power Supply Control PCA. The Power Supply PCA contains the voltage filter and conversion circuits and the Power Supply Control PCA contains the control, regulation, and basic system clock circuits.

The Power Supply PCA operates as a conventional chopped, choke-input supply and generates regulated +5V,

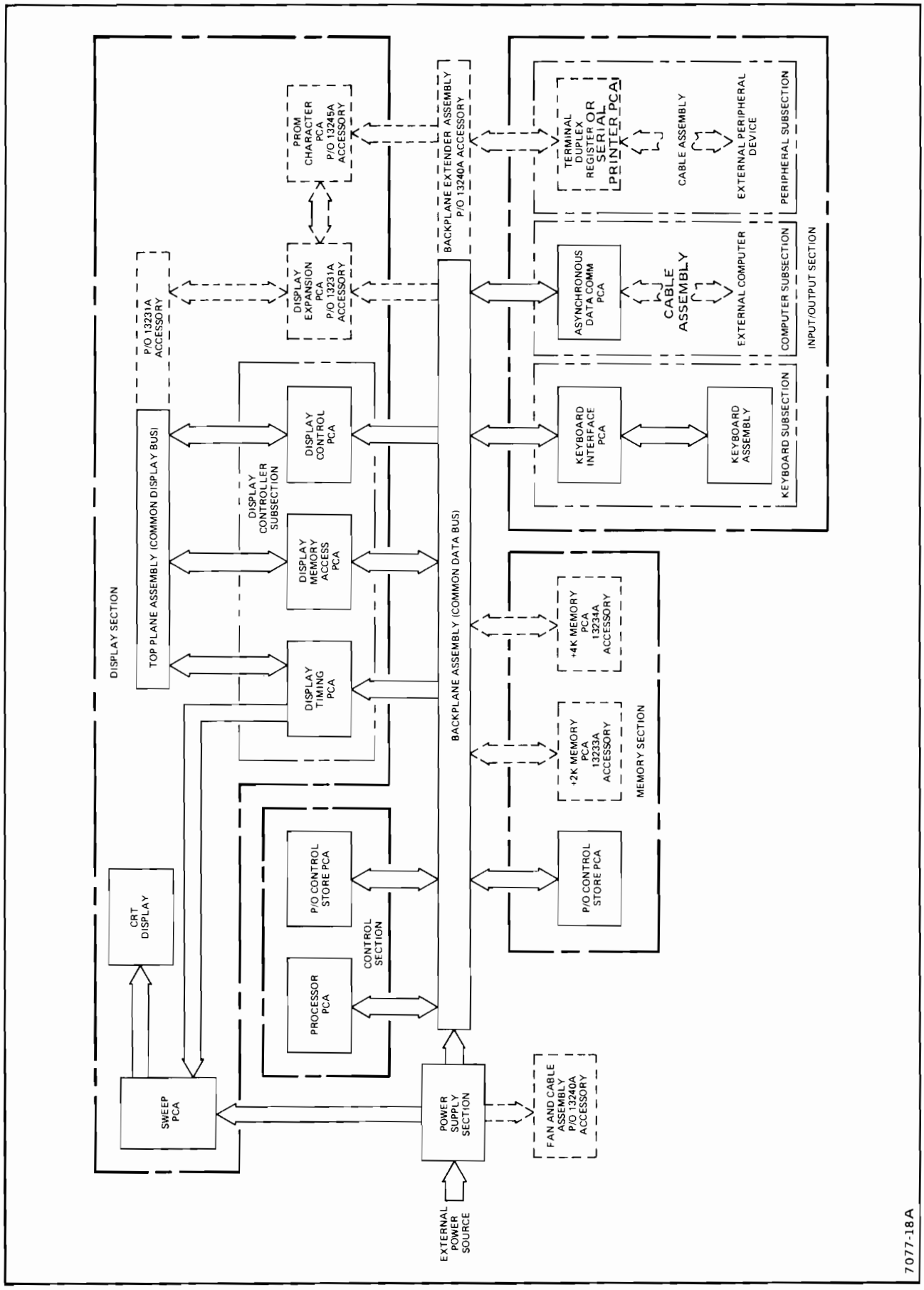


Figure 2-1. Basic Block Diagram

+12V, -12V, and -42V supplies for distribution to the other terminal modules. The +5V, +12V, and -12V supplies are applied to the Backplane Assembly for common distribution while the -42V supply is applied exclusively to the Sweep PCA. All supplies are protected from overvoltage and reverse polarity by Zener diodes. The Power Supply PCA also provides voltage and current sensing for the Power Supply Control PCA monitoring circuits. The 115/230 voltage select switch is also located on this PCA.

The Power Supply Control PCA provides the basic system clock (4.915 MHz) for distribution to the other terminal modules through the Backplane Assembly, regulates and controls the power supplies, and provides a logic reset signal for common distribution through the Backplane Assembly each time the terminal is energized. Regulation of the power supplies is obtained by the generation of the alternating base drive signals applied to the Power Supply PCA which control the on and off times of the two chopper transistors. Control is obtained by monitoring the voltage and current sense lines from the Power Supply PCA and, if line voltage goes excessively low or primary current excessively high, disabling the base drive signals to shut down the supply. The +5V ADJ R14 potentiometer is also located on this PCA.

2-5. DISPLAY SECTION

The display section consists of a CRT display, Sweep PCA, display controller subsection and, if installed, a Display Expansion PCA and PROM Character PCA. Basically, this section converts ASCII characters into a visual display. The full display capability is 24 rows of 80 characters each. The standard terminal can display 64 different characters and has one display enhancement, inverse video. Accessories provide an additional 64 character ROM for 128 character operation, three additional display enhancements (half bright, underline, and blinking), and the capability for adding up to three 128- character sets. (A 64-character mathematic set ROM and 64-character line drawing set ROM are currently available from Hewlett-Packard.)

2-6. SWEEP PCA AND CRT. The Sweep PCA receives all required operating voltages and display signals via the Sweep Cable Assembly and applies generated drive signals and voltages to the CRT via the CRT Cable Assembly, Yoke Cable Assembly, and High Voltage Cable Assembly. As shown in figure 2-2, the Sweep PCA consists of video, vertical, and horizontal drive circuits, a voltage regulator circuit, and a high voltage power supply.

The vertical drive circuit receives and amplifies 60 Hz Vertical Drive signals (VDR) from the Display Control PCA and generates vertical deflection yoke drive signals for the CRT. This circuit also contains the HEIGHT R10 adjustment. The frequency of VDR is used to obtain the CRT 60 Hz frame rate. VDR goes low at the bottom of the CRT screen for one row time during which vertical retrace occurs. The screen is blanked during retrace by a Vertical Blanking signal (VBLNK) also generated by the Display Control PCA.

The horizontal drive circuit receives 22.5 kHz Horizontal Drive signals (NHDR) from the Display Timing PCA and generates horizontal sweep drive signals for the CRT yoke. NHDR goes low at character column 81 to initiate horizontal retrace from right to left on the CRT screen. The screen is blanked during retrace by a Horizontal Blanking signal (HBLNK), also generated by the Display Timing PCA. Horizontal flyback pulses from this circuit are used as a source voltage for the high voltage power supply.

The video drive circuit receives Video signals (VIDEO) from the Display Timing PCA and Half Bright enhancement signals (NBHB) from the Display Expansion PCA accessory. These signals are combined and amplified to generate video drive signals for the CRT cathode. When VIDEO is high, the screen is on and, when VIDEO is low, the screen is off. When NBHB is high, full CRT brightness is displayed and, when NBHB is low, the half bright display enhancement is obtained. This circuit also contains the HALF BRIGHT R5 adjustment.

The voltage regulator circuit receives +5V, +12V, and -42V from the Power Supply PCA and provides voltage regulation and current limiting for the Sweep PCA. This circuit also contains the WIDTH R28 adjustment. The high voltage power supply rectifies and filters horizontal flyback pulses from the horizontal output transformer to generate +15 KV, +500V, +30V, and -100V for the CRT. The high voltage power supply circuit also contains the BRIGHTNESS R37 and FOCUS R33 adjustments.

2-7. DISPLAY CONTROLLER SUBSECTION. As shown in figure 2-2, the display controller subsection consists of a Display Control PCA, Display Timing PCA, and a Display Memory Access (DMA) PCA. The Display Control and Display Timing PCA's receive cursor position data from the Processor PCA and interact to generate drive signals for the Sweep PCA, initiate data transfers from the memory section to the DMA PCA, and to convert received ASCII characters into video signals for the Sweep PCA. The DMA PCA, under control of the Display Control and Display Timing PCA's, addresses the memory section, reads data from the memory section, and alternately refreshes and transmits received data for the Display Control and Display Expansion PCA's.

2-8. Basic Timing. Except for the DMA PCA bus cycle logic which use the 4.915 MHz System Clock (SYS CLK), all timing for the display section is derived from the Display Timing PCA 21.06 MHz display controller clock (CLK) which is the frequency at which character dots are written onto the CRT screen. As shown in figure 2-2, CLK is applied directly to the Display Expansion PCA (paragraph 2-15) and Display Control PCA dot generator. The dot generator is a nine-bit ring counter that divides CLK by nine and generates timing signals D0 through D8 that correspond to particular dot times within the character cell. D0 is used to clock the cursor generator and a 104-column counter which defines 104 character columns. The CRT displays 80 of these columns. The remaining 24 column

counts occur during horizontal retrace. The seven-bit output (horizontal column bits) of this counter is applied to the video logic along with timing signals D0, D2, D6 and D8 and column count 103 (N103) to derive Horizontal Drive (NHDR) for the Sweep PCA, Horizontal Blank (HBLNK) for the video generator logic, Circulation (0CIRC) and Circulation Enable (0CIRCEN) for the DMA and Display Expansion PCA's, Buffer Clock (BUFCLK), and Vertical Clock (VRTCLK). BUFCLK is the 2.34 MHz display enhancements clock. VRTCLK is used to clock scan line counters on the Display Expansion and Display Control PCA's. These counters define the 15 individual scan lines of a row for the character ROM's. The line count outputs (LC0 through LC3) are applied to the character generator (four least significant address bits) and to the cursor line enable logic to derive Cursor Line Enable (CLEN) and Line Count 11 (L11) for the composite video generator logic and Line Count 14 (N14). N14 is applied to a divide-by-25 row counter to define 25 separate rows. The CRT displays 24 of these rows. The remaining row count occurs during vertical retrace. The five-bit output of the row counter is applied to the video logic along with N103 to derive Vertical Drive (VDR) for the Sweep PCA, Vertical Blank (VBLNK) for the video generator logic, Interrupt Set (INT SET) for the DMA and Display Expansion PCA's, and 60 Hz Gated Vertical Sync (GVS). GVS is applied to the DMA PCA (paragraph 2-14) and to a counter in the Display Timing PCA which divides the frequency by 12 to obtain a 5 Hz clock for the blink generator. The blink generator provides the 2.5 Hz Cursor Blink (CBL) and 1.25 Hz Enhancement Blink (BLINK) signals for the video generator logic.

2-9. Character Generation. The seven-bit ASCII code (NBIT0 through NBIT6) from the DMA PCA (paragraph 2-12) is applied to the Display Control PCA character generator which consists of either an upper-case 64-character set ROM or an upper-case 64-character set ROM and a lower-case 64-character set ROM. The ROM's generate dot patterns corresponding to received ASCII codes. (Refer to paragraph 2-15 and 2-18.) NBIT5 and NBIT6 are first applied to the character select logic which determines if the generated character will be upper or lower case by enabling the applicable ROM. It should be noted that the 128 CH jumper located in this circuit must be installed if upper and lower case (128 characters) operation is desired and must be removed for upper case only (64 characters) operation. The character generator, under control of the character select logic, receives its six most significant bits of address (MSB) from the DMA PCA (NBIT0 through NBIT4 and NBIT6) and four least significant bits of address (LSB) from the divide-by-15 line scan counter (LC0 through LC3). Each output from the character generator is an eight-bit dot position word (DBIT0 through DBIT7). DBIT1 through DBIT7 correspond to the seven character dot positions and are applied to the parallel-to-serial converter for conversion into a serial bit stream (NBITS) for the video generator logic. The eighth bit (DBIT0) is applied to the dot shift generator as a normal/delay shift control signal. The dot shift generator provides a half shift capability of the character dot positions which enhances character resolution by producing smoother angles and curves. Depending on the logic level of DBIT0, the dot shift generator Shift Clock (SHFT CLK) output shifts DBIT1 through DBIT7 out of the converter either unshifted (DBIT0 = 1) or delayed one-half dot time (DBIT0 = 0) which shifts the character dots on the CRT screen to the right one-half dot width.

2-10. Cursor Generation. The position of the cursor on the CRT screen is controlled by the Processor PCA. When a new position is required, the position ($\overline{BUS0}$ through $\overline{BUS6}$) along with a blanking bit (BUS7) are applied to the "X" and "Y" holding registers. The holding register contents are constantly being compared in their respective comparators against the position of the character being written on the screen. Instruction and address signals are applied to the bus decoder network to derive the Cursor "X" Strobe (NCXS) and Cursor "Y" Strobe (NCYS) signals for the holding registers and blink generator. NCXS and NCYS are used to clock the new "X" and "Y" cursor positions from the holding registers to the "X" and "Y" comparators. NCYS also clocks Screen Blanking (NBLNK) from the "Y" holding register into the video generator logic. NCXS also momentarily inhibits CBL from the blink generator whenever the cursor is repositioned. The "X" comparator compares the seven "X" position bits against the character column position bits from the 104-column counter and applies a Cursor "X" Enable (CXEN) signal to the cursor generator whenever a compare exists. The "Y" comparator compares the five "Y" position bits against the character row position bits from the row counter and applies a Cursor "Y" Enable (CYEN) signal to the cursor generator whenever a compare exists. The cursor line enable logic monitors the scan line counter and decodes line count 11 and 12 to generate Cursor Line Enable (CLEN) for the cursor generator. Upon receipt of CXEN, CYEN, and CLEN, the cursor generator applies a Valid Cursor (VCSR) signal to the video generator logic.

2-11. Composite Video Generation. The Video (VIDEO) serial bit stream is generated by the composite generator logic tree and is applied directly to the Sweep PCA. Except for the Half Bright (NBHB) signal which is applied directly from the Display Expansion PCA to the Sweep PCA, all display enhancements, base and alternate character serial bit streams, horizontal and vertical blanking signals, and cursor position signals are combined by this generator. The Inverse Video (IV) signal is generated by the Display Timing PCA and is initiated by the Inverse Video Select (NIV) signal from the DMA PCA. The Blinking Video (NBBL), Underline Video (NBUL), and Alternate Character (NXBITS1) signals are supplied by the Display Expansion PCA. All other video generator inputs have been discussed previously.

2-12. Character Refreshing. The DMA PCA refresh operations are initially controlled by INT SET from the Display Control PCA and bit 6 ($\overline{BUS6}$) of the cursor ("Y" position from the Processor PCA. When $\overline{BUS6}$ is 0, the DMA flip-flop is set (DMA ON) which enables the bus cycle logic discussed in paragraph 2-14. INT SET resets the 80-character counter whose output (80) is then combined

with DMA ON to initiate the transfer of 80 characters from the memory section. The bus cycle logic clocks received data ($\overline{BUS0}$ through $\overline{BUS7}$) through the holding registers into one of two 80-character shift registers and their respective line buffers. Register and line buffer selection is determined by the EVEN signal from the Display Control PCA applied to the refresh logic which generates the EVEN and $\overline{EVEN}$ enabling signals and their corresponding clocks. While LOAD from the display function logic is loading a row of data into one line buffer, 0CIRC and 0CIRCEN from the Display Timing PCA are rotating the contents of the other shift register at 2.34 MHz to supply one character out of its buffer every nine dot positions as determined by clock D1 from the Display Control PCA. At the end of each row (80 characters), the load/refresh functions of the registers and corresponding buffers are reversed. Buffer outputs NBIT0 through NBIT6 are applied to the Display Control PCA as previously discussed and, if installed, to the Display Expansion PCA. The eighth bit, NIV, is applied to the Display Timing PCA as previously discussed.

2-13. Display Function Control. As received data from the memory section is clocked through the holding registers, it is edited by the display function priority encoder which applies a three-bit function code to the display function decoder. Depending on its input, the display function decoder applies a Control, Character, End-of-Line (EOL), End-of-Page (EOP), or Link function control signal to the display function logic. The display function logic, under control of the bus cycle logic, initiates execution of the decoded function. When a control function is decoded, the display function logic generates a Line Buffer Load (LBLOAD) signal which clocks the inverse video bit ($\overline{BUS1}$) into the line buffers and/or clocks other enhancement or alternate character select bits ($\overline{BUS0}$ and $\overline{BUS2}$ through $\overline{BUS5}$) through the Display Expansion PCA holding registers. (Refer to paragraph 2-15.) When a character function is decoded, a LOAD clock signal is generated for the refresh logic as previously discussed. When an end-of-line or end-of-page function is decoded, an EOL or EOP signal is applied to the upper and lower byte address registers to cause the remainder of the current line or page to be written with blanks. When a link function is decoded, the display function logic applies a LINK signal to the address registers which fetches the next byte of data from the memory section. The LINK plus the last byte become the next location address from which data is to be read.

2-14. Bus Cycle Control. The bus cycle is a six-state sequence controlled by the bus cycle logic. At the beginning of each new page of displayed data (bus cycle idle state), GVS resets the byte address registers to the starting address of the memory section and INT SET resets the 80-character counter. This initiates the second state of requesting control of the data bus. During this state, if Priority In (PRIOR IN) is high and no functions are being executed, the bus cycle logic advances to state three of getting the bus and to state four of requesting data. During this state, the contents of the byte address registers and a Request ($\overline{REQ}$) signal are applied to the memory section. If the display function logic is executing an end-of-line or end-of-page operation at this time, $\overline{REQ}$ is inhibited until the end of 80 characters or 24 rows, respectively. Once the memory section decodes its address from the byte address registers, the bus cycle logic advances to state five and data is clocked through the holding registers for decoding as discussed in paragraph 2-13. During this state, the bus cycle logic also decrements the byte address registers. During decoding, the bus cycle logic advances to state six, releases control of the bus, and returns to its idle state until INT SET is again applied to signal the start of another new line. After 24 lines have been fetched from the memory section, GVS is again applied and the complete cycle is repeated.

2-15. DISPLAY EXPANSION PCA. The Display Expansion PCA provides three additional display enhancements and the capability for adding up to three 128-character sets for the display section. All timing and control signals for this PCA are received from the display controller subsection as previously discussed.

2-16. Character Generation. As shown in figure 2-2, the same seven-bit ASCII code (NBIT0 through NBIT6) applied to the Display Control PCA from the DMA PCA (paragraph 2-12) is applied to the three 64/128 character set ROM's (if installed) on the Display Expansion PCA. These ROM's, if selected, generate dot patterns corresponding to received ASCII codes the same as the base character set ROM(s) on the Display Control PCA. NBIT5 and NBIT6 are first applied to the character select logic which determines whether the character will be generated by the upper or lower case ROM's of the selected character set. (Refer to paragraph 2-17.) It should be noted that jumpers are also contained in this circuit that must be properly configured for 64- or 128-character operation and for operating with alphanumeric and microvector sets. (Refer to paragraph 1-7.)

Once selected, the character set ROM's receive their six MSB (NBIT0 through NBIT4 and NBIT6) from the DMA PCA and four LSB (LC0 through LC3) from the divide-by-15 line scan counter. This counter is clocked by VRTCLK and reset by N14 the same as the Display Control PCA counter discussed in paragraph 2-8. The output of the character set ROM's is either an eight-bit or nine-bit dot position word (DBIT0 through DBIT7 or DBIT0 through DBIT8) that is applied to the shifter logic and parallel-to-serial converter for conversion into a serial bit stream (NXBITS1). If the selected character set is an alphanumeric ROM(s), its output is an eight-bit word that is shifted out of the parallel-to-serial converter under control of the shifter logic as discussed in paragraph 2-9. (Seven-bit data word with each bit shifted or unshifted as determined by DBIT0.) If the selected character set is a microvector ROM(s), its output is a nine-bit word, the half shift capability of the shifter logic is disabled, and DBIT0 and DBIT8 are merged into NXBITS1 along with DBIT1 through DBIT7. The character set encoder receives Sense signals (1SN, 2SN, and 3SN) from the character sets to interpret whether or not the selected set is an alphanumeric or microvector set. This signal is determined by the jumper configurations discussed in paragraph 1-7. The signal must be low (jumper installed) for alphanumeric operation and high

(jumper removed) for microvector operation. During alphanumeric operation, the character set encoder enables the shifter logic half shift capability as previously discussed. During microvector operation, the half shift capability is disabled and the shifter logic merges DBIT0 and DBIT8 into the serial bit stream along with the output from the parallel-to-serial converter.

2-17. Character Set and Display Enhancement Selection. The character set selection bits ($\overline{BUS4}$ and $\overline{BUS5}$) and display enhancement selection bits ($\overline{BUS0}$, $\overline{BUS2}$, and $\overline{BUS3}$) are clocked through the holding register by LBLOAD from the DMA PCA (paragraph 2-13) into the line buffers. The refresh and load logic, when enabled by LOAD from the DMA PCA, alternately loads and refreshes the line buffers by using the EVEN, 0CIRC, 0CIRCEN, LOAD, D1, and Buffer Select (BSEL) signals as discussed in paragraph 2-12. The line buffers set select outputs (NBSS0 and NBSS1) are decoded by the character set decoder and generates Set Enabling signals (1SEN, 2SEN, and 3SEN) for the appropriate character set ROM(s). (Refer to paragraph 2-18.) NBSS0 and NBSS1 are also applied to the Display Control PCA to enable or disable the base character set. If either signal is high, the base set is disabled by NE1, and the character set decoder enables the selected alternate character set. Display enhancement selection is determined by the logic levels of $\overline{BUS0}$, $\overline{BUS2}$, and $\overline{BUS3}$. When high, these bits become Underline Enable (ULEN), Half Bright Enable (HBEN), and Blinking Enable (BLEN) signals and are applied to the enhancement generator along with BUFCLK and 0CIRC clocks. Once enabled, the enhancement generator applies the selected enhancement signal(s) (NBHB, NBBL, and/or NBUL) to the Sweep PCA and Display Timing PCA as previously discussed. This circuit also contains the FIELD adjustment.

2-18. PROM CHARACTER PCA. The PROM Character PCA provides the capability for adding up to two user generated PROM character sets as described in the *HP Character Set Generation Kit Application Note*, part no. 13245-90001. When installed, the PROM Character PCA is connected directly to either the Display Control or Display Expansion PCA depending on the character set(s) to be replaced. The number of PROM character sets installed on the PCA depends upon the user application and design as does the number of PROM's contained in each set. Each 64 character set requires two PROM's; a 128 character set requires four PROMs; and, if the set is a microvector type, five PROM's are required. When the PROM Character PCA is connected to either the Display Control or Display Expansion PCA, the PROM character set(s) replaces the ROM character set(s) normally mounted on that PCA. It should be noted that the ROM character set(s) to be replaced must be removed from its PCA to obtain proper operation.

2-19. Character Set Selection. As shown in figure 2-2, character set selection is determined by the PROM Character PCA character set decoder. When the PCA is connected to the Display Control PCA, the Base Character Set Select signal (NSET0) is always low and the character set decoder applies four Base Set Enable signals (0/1SEN) to the PROM's in character set 0. Alternate character set select signals (NBSS0 and NBSS1) are also applied to the character set decoder and, if either or both signals go low, the character set decoder disables the PROM set by removing 0/1SEN. When this occurs, character set selection and character generation is performed by the Display Expansion PCA as discussed in paragraphs 2-16 and 2-17. When the PROM Character PCA is connected to the Display Expansion PCA, NSET0 is always high and NBSS0 and NBSS1 are decoded by the character set decoder into Set Enabling signals (0SEN and 1SEN or 2SEN) for the PROM's in character set 1 or 2. It should be noted that the character set decoder generates three enabling signals for the PROM sets when replacing Display Expansion PCA alternate character sets. This provides for the enabling of the fifth PROM required by the microvector type character sets.

2-20. Character Set Generation. Once enabled, the PROM character set(s) function the same as the replaced ROM character set(s) to generate dot patterns corresponding to received ASCII codes. (Refer to paragraphs 2-9 and 2-16.) BIT5 and BIT6 are applied to the character select decoder which determines individual PROM selection(s) within each character set. (BIT5 and BIT6 perform the same function for the character set encoder when a microvector character set is installed.) It should be noted that when a PROM set is used to replace an alternate character set that the Display Expansion PCA jumpers must be arranged to meet the requirements of the PROM character set configuration. Once selected, the character set PROM's receive their five MSB from BIT0 through BIT4 and their four LSB from LC0 through LC3. The PROM set output (DBIT0 through DBIT7) is an eight-bit dot position word that is applied back to the parallel-to-serial converter of either the Display Control or Display Expansion PCA. (DBIT0 provides shift control as previously discussed in paragraphs 2-9 and 2-16.) If a microvector character set is installed, the required fifth PROM of the set applies four Sensing output signals (1SN or 2SN) to the character set encoder which, along with BIT5 and BIT6, cause the generation of DBIT8 required for microvector character generation.

2-21. CONTROL SECTION

The control section consists of the Processor PCA and part of the Control Store PCA. As shown in figure 2-2, the Processor PCA contains the central processing and control logic and the Control Store PCA contains the 8K of ROM necessary for storing the basic operating system firmware.

2-22. MICROPROCESSOR. The microprocessor accesses and executes instructions stored in ROM. The microprocessor instruction set consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutines. The microprocessor communicates over an eight-bit data and address bus under control of the bus cycle logic. Three STATUS outputs to the cycle decoder are used to indicate the state of the microprocessor at any time during the execution of an instruction cycle. The cycle decoder constantly monitors the STATUS lines and generates the

ENABLE signals for the bus cycle logic, the T1I acknowledge signals for the interrupt generator, and the Upper and Lower Byte Clocks (UBCL and LBCL) for the address registers at the times required to coincide with the microprocessor operations. An Interrupt (INT) control signal from the interrupt generator is used to reset the microprocessor to the beginning of the ROM program. Two non-over-lapping clocks (PCL) from the clock generator are required to drive the microprocessor.

A typical instruction cycle consists of five states; T1 through T5. During T1 and T2 states, an address is sent to its address bus for addressing memory or an I/O module such as the DMA or Asynchronous Data Comm PCA. During T3 state, an instruction or data from memory or an I/O module can be received through the data bus. If an instruction is received, it is executed during T4 and T5 states. If an internal execution is not required, states T4 and T5 are omitted. If the terminal's data bus is busy ($\overline{\text{BUSY}}$ low), the microprocessor goes into a Wait state until the bus is free. If an INT is received, the cycle is interrupted and acknowledged by replacing state T1 with state T1I. Instructions can require from one to three cycles for complete execution. The first cycle is always an instruction fetch cycle. The second and third cycles are for reading data, writing data, or I/O operations. The cycle types are indicated by BIT6 and BIT7 present on the data and address bus during state T2.

2-23. BUS CYCLE CONTROL. Before the microprocessor can access memory, it must have control of the terminal's data bus. This is accomplished by the bus cycle logic which is synchronized with the instruction set by clocks ϕ11, ϕ12, and SYNC. Each bus cycle is a six-state sequence. At the beginning of each new instruction cycle (microprocessor state T1 and bus cycle Idle state), the cycle decoder applies an ENABLE signal to the bus cycle logic. This initiates the second bus cycle state of requesting control of the data bus. During this state, if PRIOR IN is high and the data bus is free ($\overline{\text{BUSY}}$ high), the bus cycle advances to state three of getting the bus and to state four of sending Request ($\overline{\text{REQ}}$) to the memory section or an I/O module. During these states, the contents of the address registers are strobed onto the data bus along with $\overline{\text{REQ}}$. It should be noted that two bus transfer signals ($\overline{\text{I/O}}$ and $\overline{\text{WRITE}}$ are applied to the bus along with the address signals. The combined logic levels of these two signals specify whether a read memory, write memory, input, or output bus transfer is to take place. During read cycles, $\overline{\text{REQ}}$ is applied to the data bus during microprocessor T2 state and requested data is received during T3 state. During write cycles, $\overline{\text{REQ}}$ is applied to the bus during microprocessor T3 state. Once the bus transfer is executed, the bus cycle advances through state five to state six, releases control of the data bus, and returns to its Idle state until ENABLE is again applied from the cycle decoder.

2-24. INITIAL START UP. When power is first applied to the terminal, it is detected by the interrupt generator which applies INT to the microprocessor. Upon receipt of INT, the microprocessor goes from its Halt or Wait state to its T1I state. This is monitored by the cycle decoder which applies T1I Acknowledge back to the interrupt generator. Upon receipt of T1I, the interrupt generator applies RESTART to the restart logic which applies the restart instruction to the microprocessor. This causes the microprocessor to fetch its next instruction from ROM memory location zero and the program begins. From here, the program can go anywhere in the available memory space. It should be noted that in order for the restart instruction to cause the microprocessor to jump to memory location zero, that the Attention ($\overline{\text{ATT}}$) signal from the Asynchronous Data Comm PCA must be low. If $\overline{\text{ATT}}$ is high, the restart logic changes the restart instruction into a microprocessor subroutine load instruction.

2-25. CONTROL STORE PCA. As shown in figure 2-2, the Control Store PCA contains 8K of ROM, 1K of RAM, a RAM select comparator, a ROM select decoder, and associated timing and control logic. The basic operating system is stored in ROM. The RAM is part of the memory section (paragraph 2-26) and provides 1,024 words of addressable read/write storage. The RAM select comparator applies a RAM Select (RAM SEL) signal to the timing and control logic when a RAM address is recognized. RAM SEL is determined by the combination of the address configuration jumper network and address bits $\overline{\text{ADDR10}}$ through $\overline{\text{ADDR15}}$. The ROM select decoder applies a ROM Select (ROM SEL) signal to the timing and control logic when a ROM address is recognized and, depending on the logic levels of $\overline{\text{ADDR11}}$ through $\overline{\text{ADDR15}}$, enables the appropriate 2K module of ROM. Three address control signals ($\overline{\text{REQ}}$, $\overline{\text{WRITE}}$, and $\overline{\text{I/O}}$) are also applied to the timing and control logic. As previously discussed, $\overline{\text{REQ}}$ must be low to start the memory access cycle and $\overline{\text{I/O}}$ must be high. When $\overline{\text{I/O}}$ is low, memory access is inhibited while the Processor PCA is writing or reading to an I/O module such as the DMA or Keyboard Interface PCA's. When $\overline{\text{WRITE}}$ is high, a read from memory cycle is initiated and, when $\overline{\text{WRITE}}$ is low, a write into memory cycle is initiated. The timing and control logic combines the ROM or RAM SEL signals with the control and SYS CLK signals and generates the appropriate address, enable, and clock signals to allow data to be read from ROM or RAM or to be written into RAM. The generated $\overline{\text{WAIT}}$ signal is low while a memory cycle is in progress and goes high when each cycle is completed.

2-26. MEMORY SECTION

The memory section consists of part of the Control Store PCA (paragraph 2-25) and, if installed, the +2K and/or +4K Memory PCA's. The basic 1K of RAM on the Control Store PCA can be expanded with the +2K and +4K Memory PCA's for a total memory space of up to 8K RAM as discussed in paragraph 1-8.

2-27. +2K MEMORY PCA. The +2K Memory PCA provides 2,048 words of addressable read/write storage. As shown in figure 2-2, the +2K Memory PCA contains an address comparator, 2K of RAM, an input multiplexer, output read registers, bus request logic, refresh logic, and associated timing and control logic. The address comparator applies an Access Request (ACS REQ) signal to the timing

and control logic whenever a RAM address within the assigned memory space (selected by the address configuration network) is recognized. ACS REQ is determined by the combination of the address jumper configurations and the five most significant address bits (ADDR11 through ADDR15). The remaining address bits (ADDR0 through ADDR10) are applied to the memory chips. Three address control signals (REQ, WRITE, and I/O) are also applied to the timing and control logic. As previously discussed in paragraph 2-25, REQ must be low and I/O must be high to start a memory access cycle and the logic level of WRITE determines whether a read or write cycle is to be initiated. Once the +2K Memory PCA has been selected for a memory access, the timing and control logic generates the necessary timing and enable signals required to allow data to be read from or written into RAM. The generated WAIT signal is low while a memory cycle is in progress and goes high when each cycle is completed.

Unlike the Control Store PCA RAM which is a 1K by 8 array, the 2K RAM is a 4K by 4 array. Therefore, in order to achive the required 2K by 8 bit organization, it is necessary to perform two read or write cycles for each memory request and then multiplex the outputs or inputs. During a write cycle, the timing and control logic applies a Write Enable signal (READ/WRITE low) to the multiplexer and a RAM Enable Clock (RAM ENCLK) to RAM. Initially, the timing and control logic also applies Least Significant Byte Select signals (LSB/MSB SEL low) to the multiplexer and RAM and the four least significant bits of data (BUS0 through BUS3) are gated through the multiplexer into RAM. When the first write cycle is complete, the timing and control logic applies Most Significant Byte Select signals (LSB/MSB SEL high) to the multiplexer and RAM and the four most significant bits of data (BUS4 through BUS7) are gated into memory. This results in the four least significant bits of data always being stored in even memory locations and the four most significant bits being stored in odd locations. During a read cycle, the timing and control logic applies RAM ENCLK and a Read Enable signal (READ/WRITE high) to RAM. The timing and control logic then strobes the accessed data byte out of RAM through the read registers four bits at a time (four least significant bits first) in much the same manner as for a write cycle. The timing and control logic also applies a Read Enable signal (READ EN) to the bus drivers to gate the eight-bit data byte (READ DATA) from the read registers onto the data bus.

The 2K RAM also requires periodic psuedo read cycles (memory locations accessed but data not released to bus) to ensure that no data is lost from its internal data storage mechanisms. This function is accomplished by the bus request, refresh, and timing and control logic that perform 32 double read cycles on RAM by gating five address bits onto the bus to cycle through the 64 memory locations. When the bus is not busy, no other module is requesting the bus, and a valid read or write cycle is not in progress, the bus request logic takes control of the bus by generating a Bus Busy signal (BUSY low) and initiates a refresh cycle by generating Bus Available signals (BUS AVAIL and BUS AVAIL) for the timing and control logic and refresh logic. Once control of the bus is established, the bus request logic maintains control of the bus until all 64 memory address locations have been accessed by the refresh and timing and control logic. BUS AVAIL clears the refresh logic address counter and also causes the timing and control logic to apply RAM ENCLK to RAM. BUS AVAIL gates the first psuedo read address (PADDR) from the refresh logic address counter through bus drivers onto the bus and back to RAM and remains high until the refresh and timing and control logic have cycled through 32 double read cycles. The timing and control logic keeps accessed data off the bus during refresh by disabling the read register bus drivers (READ ENCLK low). At the completion of 32 cycles, the refresh logic applies a Refresh Finished signal (RFSH FN high) to the timing and control and bus request logic, the refresh cycle is disabled (BUS AVAIL low and BUS AVAIL high), and the bus request logic releases control of the bus (BUSY high).

2-28. +4K MEMORY PCA. The +4K Memory PCA provides 4,096 words of addressable read/write storage. As shown in figure 2-2, the +4K Memory PCA contains an address comparator, 4K of RAM, an address multiplexer and buffers, refresh logic, and associated timing and control logic. The address comparator applies ACS REQ to the timing and control logic whenever a RAM address within the assigned memory space (selected by the address configuration network) is recognized. ACS REQ is determined by the combination of the address jumper configurations and the four most significant address bits (ADDR12 through ADDR15. The remaining address bits (ADDR0 through ADDR11) are applied to the memory chips through the address multiplexer and address buffers. Three address control signals (REQ, WRITE, and I/O) are also applied to the timing and control logic. As previously discussed in paragraph 2-25, REQ must be low and I/O must be high to start a memory access cycle and the logic level of WRITE determines if a read or write cycle is to be initiated. Once a memory cycle is initiated, WAIT is low and goes high when each cycle is completed.

The 4K RAM is a 4K by 8 array similar to the Control Store PCA 1K RAM, but requires refreshing similar to the +2K Memory PCA 2K RAM. Unlike the +2K Memory PCA which refreshes all 64 memory locations each time it gains control of the bus, the +4K Memory PCA refreshes in a cycle stealing fashion by reading one memory row (one address combination out of 64) every 32 microseconds while memory is not busy. When a memory read or write request is recognized by the address comparator and timing and control logic, the timing and control logic applies a Memory Request signal (MEM REQ) to the refresh logic to inhibit the start of any new memory refresh cycles. During a write cycle, the timing and control logic applies a Write Enable signal (READ/WRITE low) and RAM ENCLK to the 4K RAM. Simultaneously, the refresh logic applies an Address Select signal (ADDR SEL) to the address buffers and multiplexer to gate the memory address (ADDR0 through ADDR11) into RAM and data from the bus (BUS0 through BUS7) is written into the addressed memory space. During a read cycle, the operation is the same except the timing and control logic applies a Read Enable signal

(READ/WRITE high) to the 4K RAM and a READ EN to the bus drivers to gate the accessed eight-bit data byte (READ DATA) from memory onto the data bus.

The timing and control logic and refresh logic accomplish the required memory refresh function by performing 64 psuedo read (refresh) cycles to RAM every 32 microseconds when memory is not busy. When no other module is requesting a memory access and a read or write cycle is not in progress, a refresh cycle is initiated by the application of a high MEM REQ signal from the timing and control logic to the refresh logic. The high MEM REQ signal also causes the timing and control logic to apply a Read Enable signal (READ/WRITE high) to RAM. Once initiated, the refresh logic applies ADDR SEL to the address multiplexer which gates the first six-bit psuedo read address (PADDR) from the refresh logic address counter to RAM. Simultaneously, a Refresh In Progress signal (RFSH ON) from the refresh logic causes the timing and control logic to apply RAM ENCLK to RAM which refreshes the first memory location. The timing and control logic keeps accessed data off the bus by disabling the RAM bus drivers (READ EN low). At the completion of each refresh cycle, the refresh logic address counter is incremented by one. After 32 microseconds, another refresh cycle is initiated and the next memory location is refreshed. MEM REQ remains high until a memory access is requested. Once a request is recognized by the address comparator and timing and control logic (ACS REQ high, $\overline{I/O}$ high, and $\overline{REQ}$ low), MEM REQ goes low and the refresh logic is inhibited from starting the next refresh cycle until MEM REQ again goes high.

2-29. INPUT/OUTPUT SECTION.

The input/output section consists of a keyboard subsection, computer subsection, and peripheral subsection. Combined, these subsections provide a complete communication link between the terminal and the terminal operator, an external central processing unit, and external peripheral equipment.

2-30. KEYBOARD SUBSECTION. The keyboard subsection provides the communication link between the terminal operator and the terminal. The process of recognizing data entry from the keyboard is accomplished by the control section Processor PCA. All the keyboard keys are arranged in a matrix of 14 columns of eight key switches each. This matrix is constantly monitored by the Processor PCA one column at a time. As each column is scanned, it appears to the Processor PCA as an eight-bit word where each bit represents one key switch in the column. Depressed keys are represented by a logic "1" and released keys by a logic "0". Because the key columns are monitored sequentially, the present state of each key must be compared to its previous state when last scanned in order for the Processor PCA to recognize when a key has just been depressed, is being held depressed, or has just been released. The previous state of each key is stored in the memory section and applied to the keyboard subsection one column byte (one bit for each key in the column) at a time. Each previous state byte corresponds to the matrix column being scanned and is applied to the subsection for comparison just before the column is read.

As shown in figure 2-2, the keyboard subsection consists of the Keyboard Interface PCA and the Keyboard Assembly. The Keyboard Interface PCA contains the bus decoder logic, an option jumper network, a speaker alarm generator, and input and output data buffers. The Processor PCA accesses the subsection by applying $\overline{I/O}$, $\overline{REQ}$, and the keyboard address ($\overline{ADDR4}$, and $\overline{ADDR9}$ through $\overline{ADDR11}$) to the bus decoder logic. $\overline{ADDR0}$ through $\overline{ADDR3}$ and $\overline{ADDR5}$ are instruction addresses that determine the keyboard function to be performed. The logic level of $\overline{WRITE}$ determines if data is to be received or transmitted by the keyboard. When $\overline{WRITE}$ is low, the bus decoder logic applies a Data Input Enable signal (DATA IN EN) to the input buffers and previous state column data and alarm instructions can be applied to the Keyboard Assembly. When $\overline{WRITE}$ is high, the bus decoder logic applies a Data Output Enable signal (DATA OUT EN) to the output buffers and data from the subsection under control of the Processor PCA is applied back to the control and memory sections. Upon request from the Processor PCA ($\overline{WRITE}$ and $\overline{ADDR0}$ high and $\overline{ADDR1}$ through $\overline{ADDR3}$ low) the bus decoder logic applies a Read Jumper signal (RD JMPRS) to the option jumper network and an eight-bit data word defining the configuration of the operating option jumpers is applied through the output buffers onto the data bus. (A discussion of the jumper configurations is contained in section I of this manual.) The alarm generator is also under control of the processor PCA. Upon instruction ($\overline{WRITE}$ low and $\overline{ADDR5}$ and $\overline{BUS7}$ high), the bus decoder logic generates an Alarm Enable signal (ALARM EN) that enables the alarm generator which activates the Keyboard Assembly speaker. Other instructions decoded and applied to the Keyboard Assembly include Column Output Enable ($\overline{WRITE}$ and $\overline{ADDR5}$ low), Light Emitting Diode Enable ($\overline{WRITE}$ low and $\overline{ADDR5}$ high), and Read Columns 0 through 14 (WRITE high and $\overline{ADDR1}$ through $\overline{ADDR3}$ low).

As shown in figure 2-2, the Keyboard Assembly contains LED, input, and output registers, data comm logic, a column decoder, ramp generator, 8 by 14 key matrix, differential comparators, and column byte buffers. The light emitting diode (LED) register is loaded with seven data bits (BUS0 through BUS6) and applies these bits (one bit for each LED) to the keyboard LEDs when the LED Enable signal (LED EN) is applied from the bus decoder logic. The input register holds column previous state data (BUS0 through BUS7) and applies this previous column byte (PBIT0 through PBIT7) to the reference voltage input of the differential comparators upon receipt of the Column Output Enable signal (COL OUT EN) from the bus decoder logic. This occurs just before each new column is scanned. The output register holds the newly scanned differentiated column byte from the differential comparators and releases the eight-bit byte (COL OUT) to the data bus upon receipt of RD·$\overline{COL15}$ from the bus decoder logic. The data comm logic contains a baud rate encoder and the keyboard data communication switches (BAUD RATE, DUPLEX, and PARITY) which generate a six-bit data comm byte (BD RATE/PAR/DPLX). Each time the 14 columns of the 8 by 14 key matrix have been scanned, the column decoder generates a Read Column 15 signal (RD·COL15) which

releases the data comm byte to the data bus. (BUS1 through BUS3 define baud rate; BUS4 and BUS5 define parity; and BUS7 defines duplex.)

The column decoder, 8 by 14 key matrix, ramp generator, and differential comparators work in conjunction to generate the eight-bit scanned column byte (COL OUT) applied to the output register. When the Processor PCA issues instructions to read a column of the key matrix, the column decoder decodes the correct column address from ADDR0 through ADDR3 and applies the appropriate Column Select signal (COL SEL) to the key matrix. When RD·$\overline{\text{COL15}}$ goes high, the ramp generator is enabled and applies Drive Current (DR CUR) to the key matrix drive wires. Depressed keys in the selected column couple the drive wire signals to the sense wires which apply the signals (CBIT0 through CBIT7) to their respective differential comparators. As previously discussed, before a column is read, the previous state of that column is applied to the differential comparators by the Processor PCA through the input register. The differential comparators (one comparator for each row in the matrix) compare the previous and current state of each switch in the selected column and set corresponding bits in the output register. When RD·$\overline{\text{COL15}}$ from the bus decoder logic goes high, the eight-bit contents of the output register are gated through column byte buffers onto the data bus.

2-31. COMPUTER SUBSECTON. The computer subsection provides the communication link between the terminal and an external computer. The subsection consists of the Asynchronous Data Comm PCA and an interface cable assembly. The PCA transmits and receives bit serial data to and from the external computer through the interface cable assembly, provides parallel-to-serial and serial-to-parallel conversion, and transmits and receives bit parallel data to and from the terminal through the Backplane Assembly (data bus). The interface cable assembly determines if the terminal is to be connected directly to the computer or to data sets for remote communication with the computer through telephone lines.

As shown in figure 2-2, the Asynchronous Data Comm PCA contains RS-232-C receivers and drivers, bus decoder logic, a baud rate generator, control logic, and a universal asynchronous receiver/transmitter (UAR/T). The RS-232-C receivers and drivers provide the RS-232-C standard voltage interface for serial data transfers and interface control between the terminal and external computer. The drivers convert output signals from TTL levels (H= > 2.0V; L = < 0.8V) to RS-232-C levels (H = > +3.0V; L = < -3.0V). The receivers convert input signals from RS-232-C levels to TTL levels. There are six interface output signals. The Request To Send signal (CA) is generated by the control logic and is used when the terminal is connected to a data set to begin a transmit operation. The Data Terminal Ready signal (CD) is generated at the driver and is always true (high) as long as power is applied to the terminal. The Secondary Channel Transmit signal (SA) is generated by the control logic and is high unless a Break signal is generated. The Break signal is used by the terminal for remote interrupt to the computer and controls transmission of Serial Data Out (BA) from UAR/T. As long as $\overline{\text{BREAK}}$ is high, SA is high and BA can be transmitted from UAR/T. When $\overline{\text{BREAK}}$ is low, SA is low, the BA driver is disabled, and data cannot be transmitted to the computer. The remaining two interface outputs are TTL level clocks (EXT CLK OUT X8 and EXT CLK OUT X16) used only for special interface requirements. There are five interface input signals. The Serial Data In (BB) is applied directly to UAR/T. The Carrier Detect (CF), Clear To Send (CB), and Secondary Received Data (SB) are data set status signals and are applied directly to their respective terminal bus drivers. The remaining interface input is a TTL level clock (EXT CLK IN X16) used only for special interface requirements.

The processor accesses the subsection by applying $\overline{\text{I/O}}$, $\overline{\text{REQ}}$, and the PCA address ($\overline{\text{ADDR9}}$ through $\overline{\text{ADDR11}}$ high and $\overline{\text{ADDR4}}$ low) to the bus decoder logic. $\overline{\text{ADDR5}}$ and $\overline{\text{ADDR6}}$ are instruction addresses that determine the PCA function to be performed. The logic level of $\overline{\text{WRITE}}$ determines if data is to be received from or transmitted to the data bus. When $\overline{\text{WRITE}}$ is low, data is received from the data bus for transmission to the computer. When $\overline{\text{WRITE}}$ is high, data received from the computer is transmitted to the data bus. When $\overline{\text{WRITE}}$, $\overline{\text{ADDR5}}$, and $\overline{\text{ADDR6}}$ are low, the bus decoder logic generates a Transmit Strobe (XMIT STRB) which loads data from the bus (BUS0 through BUS7) into UAR/T. When $\overline{\text{WRITE}}$ and $\overline{\text{ADDR5}}$ are low and $\overline{\text{ADDR6}}$ is high, the bus decoder logic generates a low Control Load signal ($\overline{\text{CNTL LD}}$) which loads control data from the bus (BUS0 through BUS6) through the control logic register into UAR/T. When $\overline{\text{WRITE}}$ and $\overline{\text{ADDR6}}$ are high and $\overline{\text{ADDR5}}$ is low, the bus decoder logic generates a Status Enable signal (STAT EN) which gates seven status bits onto the data bus. When $\overline{\text{WRITE}}$, $\overline{\text{ADDR5}}$, and $\overline{\text{ADDR6}}$ are high, the bus decoder logic generates a Receive Reset signal which resets the UAR/T data received flag and, simultaneously, gates UAR/T data (DBIT0 through DBIT7) onto the data bus.

The baud rate generator defines bit timing during transmit/receive operations. Depending on the Baud Rate Select Code signals (BD RATE SEL) from the control logic, the baud rate generator generates one of eight baud rate clocks for the UAR/T (XMIT/RECEIVE CLK) and external computer (EXT CLK OUT X8 and EXT CLK OUT X16). Seven of the baud rates (110 to 9,600) are derived from the System Clock (SYS CLK) and one is derived from an external input (EXT CLK IN X16).

The control logic receives seven control bits (BUS0 through BUS6) from the bus and applies the bits to the baud rate generator, UAR/T, and RS-232-C drivers when $\overline{\text{CNTL LD}}$ is received from the bus decoder logic. BUS0 is the Request To Send bit ($\overline{\text{CA}}$) and is applied directly to its RS-232-C driver. BUS1 through BUS3 are the baud rate code bits (BD RATE SEL) applied to the baud rate generator. When the select code for 110 baud is detected, the control logic also applies a high 110 Baud signal (110 BD) to UAR/T indicating the need for two stop bits in the character format. For all other select codes, 110 BD is low indicating the format

requirement of one stop bit. BUS4 and BUS5 are the Parity Select Code bits (PAR SEL) applied to UAR/T to select even, odd, or no parity. BUS6 is the interrupt bit and, when high, causes $\overline{SA}$ to go high and $\overline{BREAK}$ to go low disabling the data out RS-232-C driver.

The UAR/T is a full duplex device that can transmit and receive simultaneously. When transmitting to the computer, it receives parallel data (BUS0 through BUS7) from the data bus when XMIT STRB is applied. It converts the parallel data to serial information, appends the required asynchronous character formatting bits (start, stop, and parity) according to the inputs from the control logic (110 BD and PAR SEL), and transmits the information at the selected baud rate of XMIT/RECEIVE CLK from the baud rate generator. When transmitting to the terminal, UAR/T starts receiving serial data from the computer when it detects a valid start bit. It checks character parity, removes the start and stop bits, converts the data to parallel information, and transmits the information to the terminal bus. The UAR/T also generates four status outputs that indicate when it can receive parallel data from the data bus for transmission, when serial data has been received from the external computer, when a received character has incorrect parity, and when an overrun condition exists (UAR/T receive buffer full and a new character is loaded into it).

2-32. PERIPHERAL SUBSECTION. The peripheral subsection provides the communication link between the terminal and an associated external peripheral device. The subsection consists of the Terminal Duplex Register PCA or the Serial Printer PCA and an interface cable assembly. A description of the Serial Printer PCA is contained in the 13250A Data Communications/Serial Printer Interface Accessory Operating and Service Manual (part number 02640-90042).

The Terminal Duplex Register PCA is a general purpose, parallel input/parallel output, interface device that provides eight data outputs, input/output commands, and an external strobe for its associated peripheral. The PCA accepts eight data inputs, input/output control-in, and eight status inputs from the peripheral. Data and instructions from the terminal are applied to the PCA through the Backplane Assembly (data bus). Communication between the PCA and external peripheral is provided by an interface cable assembly that is compatible with both the PCA edge connector and selected external peripheral. (A 9866 Cable Assembly is currently available from Hewlett-Packard to interface between the PCA and an HP 9866A Printer.)

As shown in figure 2-2, the Terminal Duplex Register PCA contains an address comparator, bus decoder logic, a strobe generator, control logic, an input register, and an output register. In addition, the PCA contains 15 jumper options that provide the user with the means to configure the PCA as required for specific interface requirements. Table 2-1 contains a list of the jumpers and a definition of each jumper function.

The address comparator applies an Address Enable signal (ADDR) to the bus decoder logic whenever a valid module address from the control section is recognized. ADDR is determined by the combination of the address jumper configuration (table 2-1) and four address bits ($\overline{ADDR4}$ and $\overline{ADDR9}$ through $\overline{ADDR11}$). The remaining address bits ($\overline{ADDR0}$ through $\overline{ADDR2}$) are instruction addresses and are applied to the bus decoder logic along with three address control signals ($\overline{REQ}$, $\overline{I/O}$, and $\overline{WRITE}$) to determine the Terminal Duplex Register PCA function to be performed. In addition to the correct address, both $\overline{REQ}$ and $\overline{I/O}$ must be low in order for the bus decoder logic to decode function instructions from the control section. Depending on the combined logic levels of $\overline{ADDR0}$, $\overline{ADDR1}$, $\overline{ADDR2}$, and $\overline{WRITE}$, the bus decoder logic generates one of nine output signals that initiate the execution of received control section instructions. The instruction codes and the resulting bus decoder logic output signals are listed in table 2-2. When triggered by PULSE OUT from the bus decoder logic, the strobe generator generates a buffered one-microsecond pulse for the external peripheral. The polarity of the pulse is determined by strobe jumpers P and Q as discussed in table 2-1.

The control logic consists of a Command Out flip-flop, Command In flip-flop, and associated logic circuits and jumper networks. Both flip-flops are enabled by SYS CLK and both are configured so that if a conflict occurs between an instruction to set the flip-flop and an instruction to reset the flip-flop, the set instruction will always take precedence. The Command Out flip-flop can be set by either SET OUT FF from the bus decoder logic or by $\overline{OUTPUT}$ if jumper C (table 2-1) is installed. When set, the flip-flop generates a true Command Out signal (table 2-1, jumper M) for the external peripheral and, if jumper N (table 2-1) is installed, applies an Output Enable signal (OUTPUT EN) to the data output buffers. The flip-flop can be reset by either RESET OUT FF from the bus decoder logic or a Device Out signal (table 2-1, jumper K) from the external peripheral.

When set by SET IN FF from the bus decoder logic, the Command In flip-flop generates a true Command In signal (table 2-1, jumper L) for the external peripheral and simultaneously clocks input data ($\overline{DBIT0}$ through $\overline{DBIT7}$) into the input register with DATA IN CLK. The flip-flop can be reset by either RESET IN FF from the bus decoder logic or a Device In signal (table 2-1, jumper J) from the external peripheral. The status of the Command Out and Command In flip-flops (OUT FF STATUS and IN FF STATUS) are applied to the terminals data bus ($\overline{BUS0}$ and $\overline{BUS7}$ respectively) whenever CMD FF STATUS is decoded by the bus decoder logic and applied to the control logic.

As previously discussed, parallel data from the external peripheral ($\overline{DBIT0}$ through $\overline{DBIT7}$) is clocked into the input register with DATA IN CLK from the control logic. The input register inverts the data and

Table 2-1. Terminal Duplex Register PCA Jumper Options

JUMPER	FUNCTION
A, B	Jumpers A and B are used to tie the input registers eight data input bias resistors to either +5V or ground. When jumper is installed, the resistors are tied to +5V. When jumper A is installed, the resistors are tied to ground. Jumpers A and B *cannot* be installed at the same time. If both jumpers are installed, a short between +5V and ground is created.
C	When jumper C is installed, the control logic Command Out flip-flop is set (Command Out signal true) each time output data is clocked into the output register. (Refer to jumper M.) When jumper C is removed, the Command Out flip-flop is set only when the bus decoder logic decodes the appropriate I/O instruction.
D	Not used.
E–H	Jumpers E through H correspond to $\overline{\text{ADDR4}}$, $\overline{\text{ADDR9}}$, $\overline{\text{ADDR10}}$, and $\overline{\text{ADDR11}}$, respectively, and are used to select the address to which the PCA will respond. (For 9866 Printer interface addressing jumper F should be installed and jumpers E, G, and H removed.
J, K	Jumpers J and K are used to select the polarity of the Device In (jumper J) and Device Out (jumper K) signals that will reset the control logic Command In and Command Out flip-flops. When the jumpers are installed, the flip-flops will be reset by low Device In/Out signals. When the jumpers are removed, the flip-flops will be reset by high Device In/Out signals.
L, M	Jumpers L and M are used to select the polarity of the Command In (jumper L) and Command Out (jumper M) signals when their respective flip-flops are set. When the jumpers are installed, the Command In/Out signals are high when their flip-flops are set. When the jumpers are removed, the Command In/Out signals are low when the flip flops are set.
N	Jumper N controls the output registers eight data output buffers. When jumper N is removed, the output buffers are always enabled and data from the output register is inverted as it is applied to the external peripheral. When jumper N is installed, the output buffers are enabled only when the control logic Command Out flip-flop is set. When the jumper is installed and the flip-flop is reset, the outputs from the buffers are always high.
P–R	Jumpers P, Q, and R are used to select the Strobe signal applied to the external peripheral. When jumpers P or Q are installed, a one microsecond pulse is applied to the peripheral when the bus decoder logic decodes the appropriate I/O instruction. When jumper P is installed, a positive pulse is generated and, when jumper Q is installed, a negative pulse is generated. When jumper R is installed, the Strobe signal is always +5V. When no jumpers are installed, the Strobe signal line is open. Only one of jumpers P, Q, and R can be installed at the same time. If more than one jumper is installed, the strobe generator circuits may be damaged.

applies it through the input buffers onto the data bus whenever the buffers are enabled by an Input Enable signal (INPUT EN) which is derived from the bus decoder logic $\overline{\text{INPUT DATA}}$ signal. Parallel data from the terminal ($\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$) is clocked into the output register with a Data Out Clock signal (DATA OUT CLK) which is derived from the bus decoder logic $\overline{\text{OUTPUT}}$ signal. The output register inverts the data and applies it through the output buffers to the external peripheral whenever the buffers are enabled (table 2-1, jumper N). Eight status inputs ($\overline{\text{SBIT0}}$ through $\overline{\text{SBIT7}}$) from the external peripheral can be gated onto the data bus by applying a Status Enable signal (STATUS EN) to the eight status input buffers. STATUS EN is generated whenever $\overline{\text{INPUT STATUS}}$ is decoded by the bus decoder logic. It should be noted that two of the status bits ($\overline{\text{SBIT0}}$ and $\overline{\text{SBIT1}}$) are inverted before they are applied to their respective input buffers.

Table 2-2. Bus Decoder Logic Instruction Codes

INPUT SIGNAL AND LOGIC LEVEL				OUTPUT SIGNAL
$\overline{\text{WRITE}}$	$\overline{\text{ADDR2}}$	$\overline{\text{ADDR1}}$	$\overline{\text{ADDR0}}$	
L	H/L	H/L	H/L	$\overline{\text{OUTPUT}}$
H	H	H	H	$\overline{\text{INPUT STATUS}}$
H	H	H	L	$\overline{\text{INPUT DATA}}$
H	H	L	H	PULSE OUT
H	H	L	L	CMD FF STATUS
H	L	H	H	RESET OUT FF
H	L	H	L	RESET IN FF
H	L	L	H	SET OUT FF
H	L	L	L	SET IN FF

H = High
L = Low

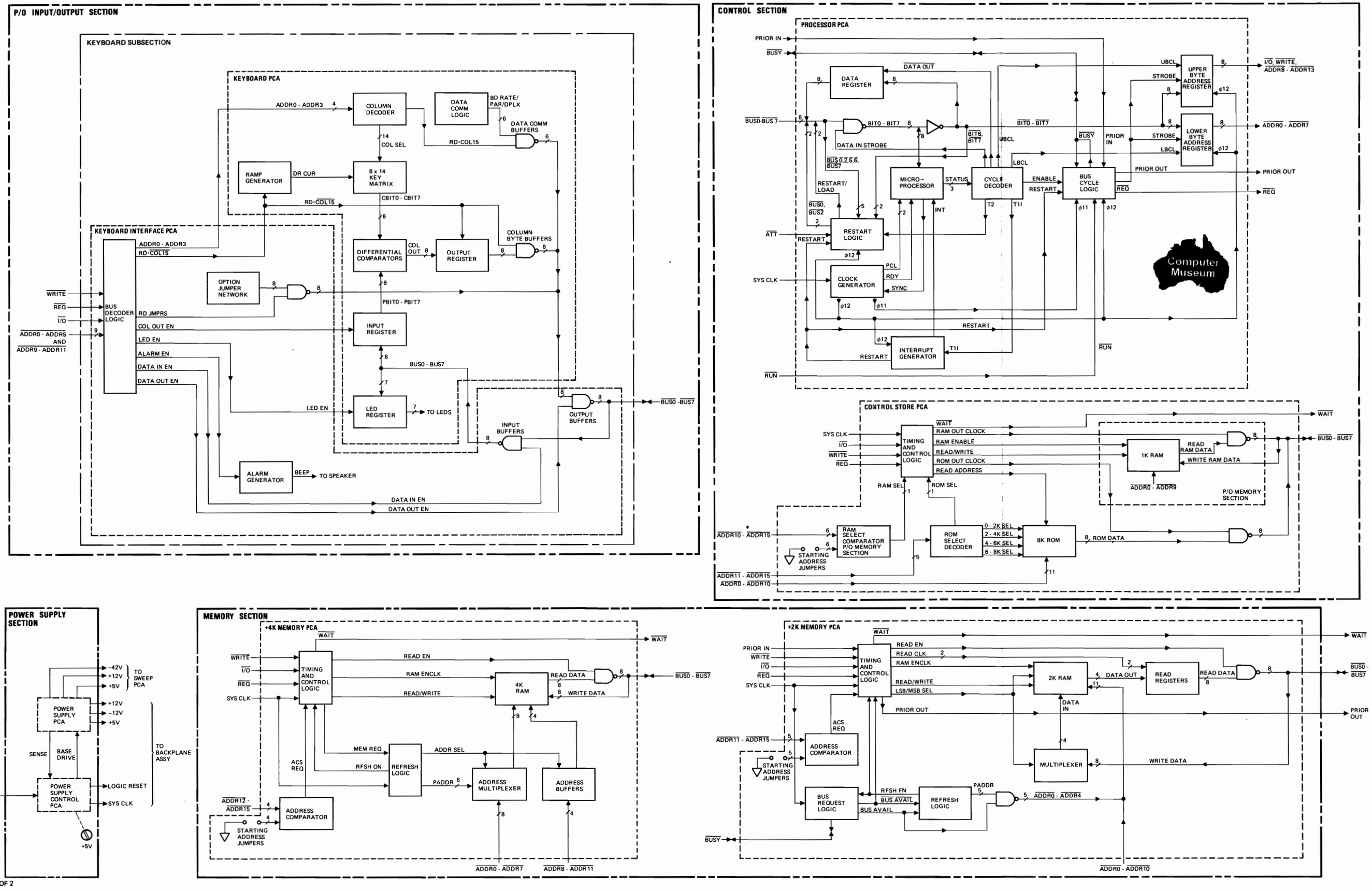


Figure 2-2. Detailed Block Diagram (Sheet 1 of 2)

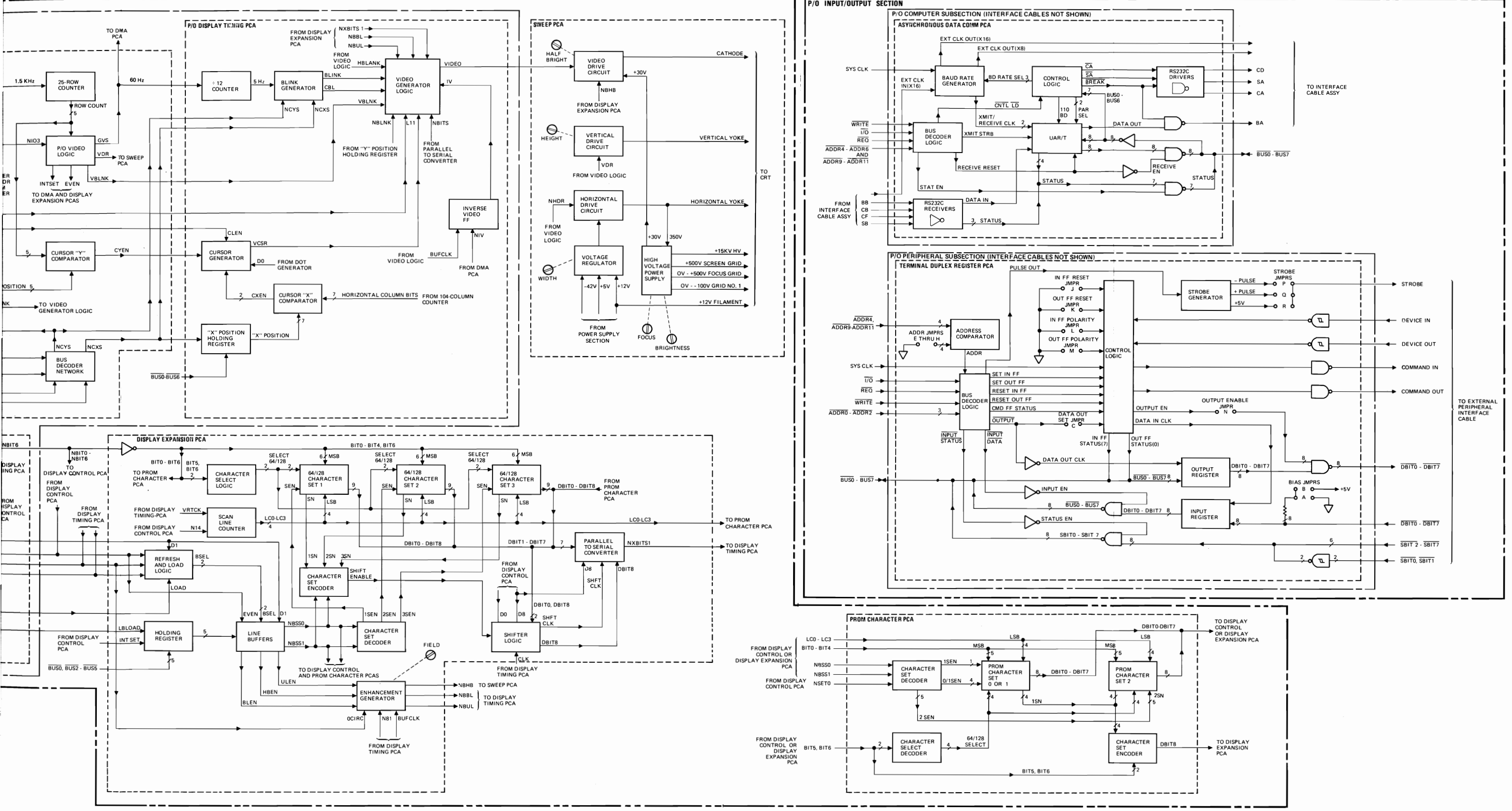
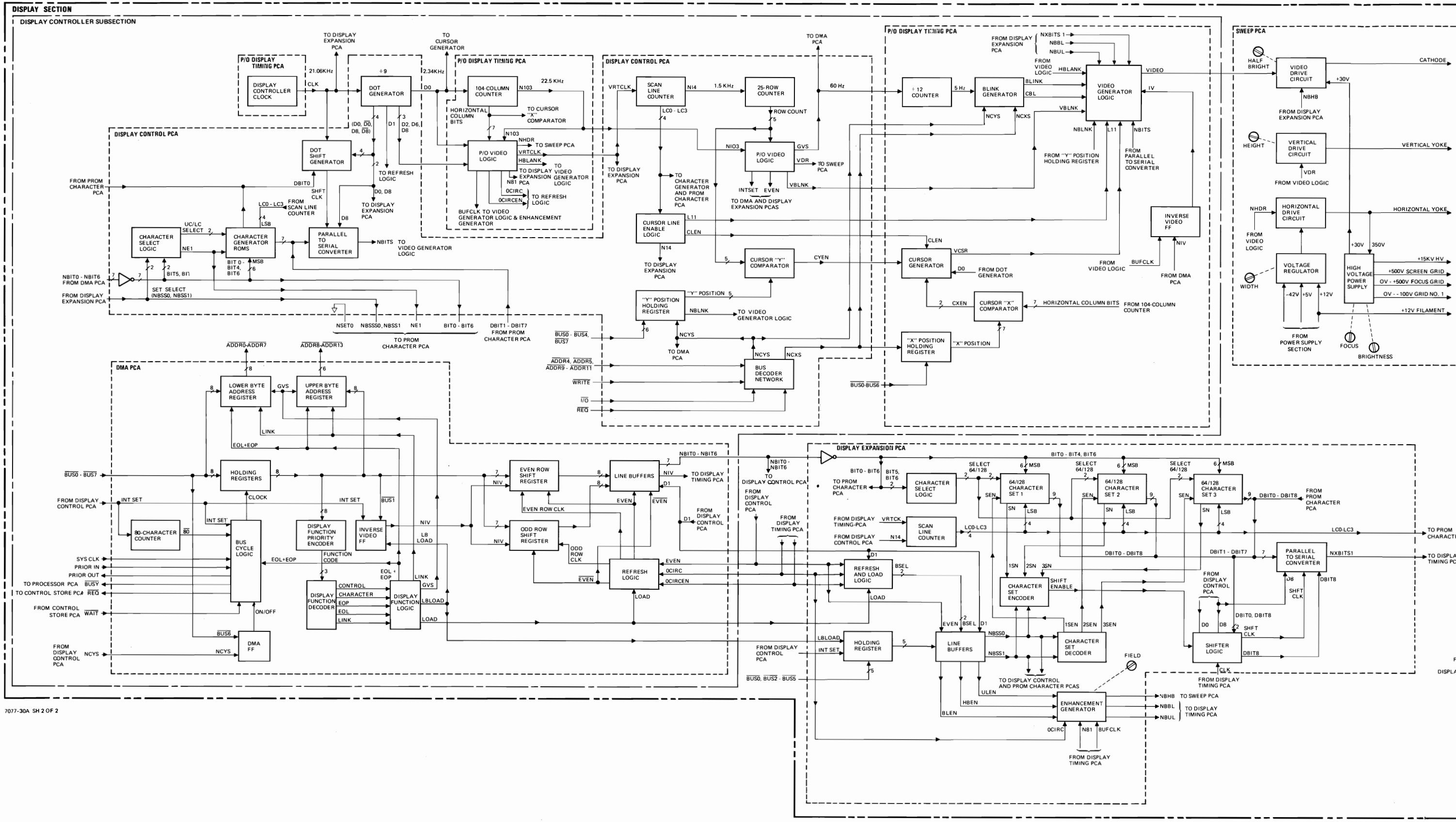


Figure 2-2. Detailed Block Diagram (Sheet 2 of 2)

DISPLAY SECTION

DISPLAY CONTROLLER SUBSECTION



7077-30A SH 2 OF 2

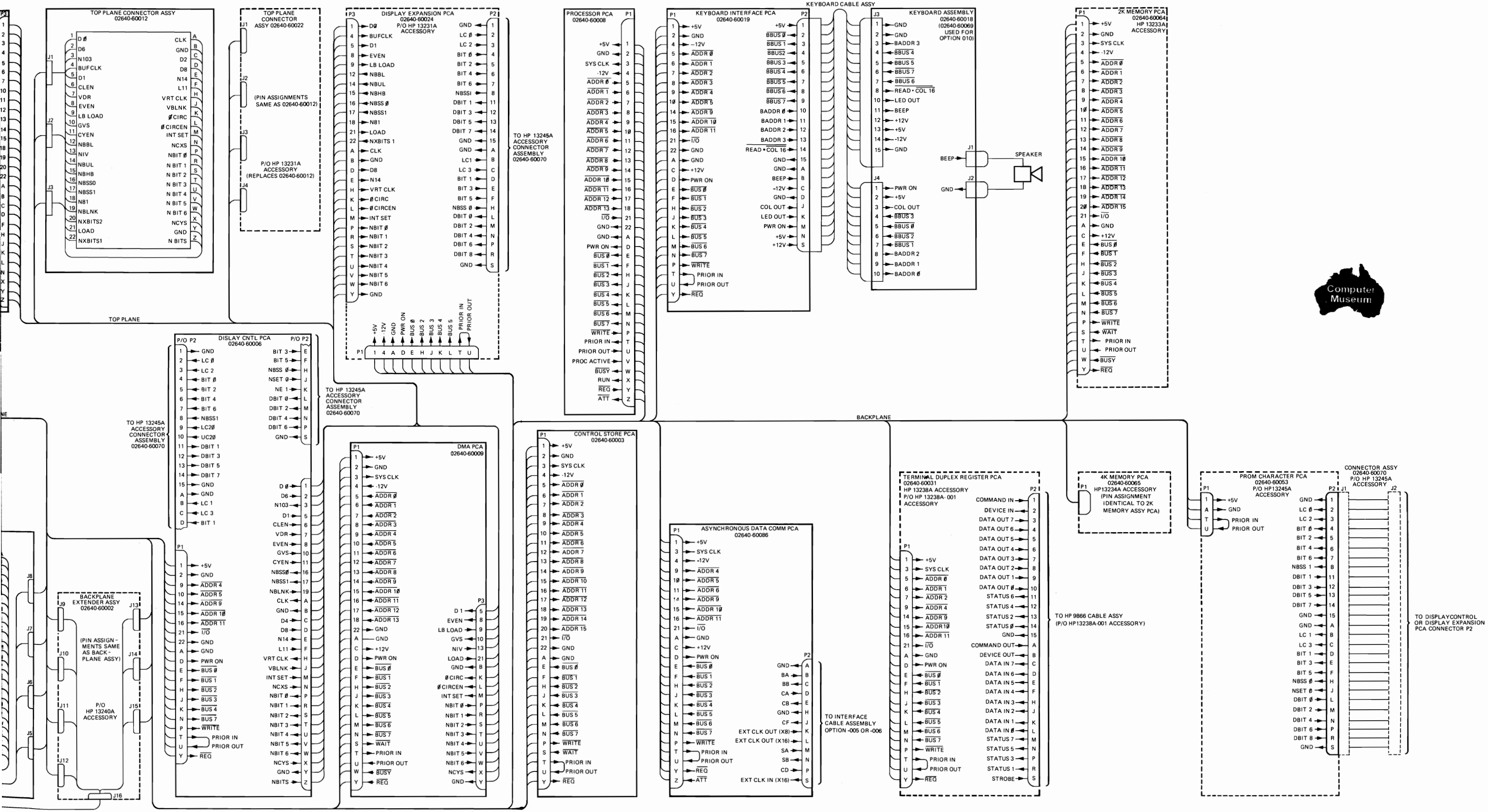
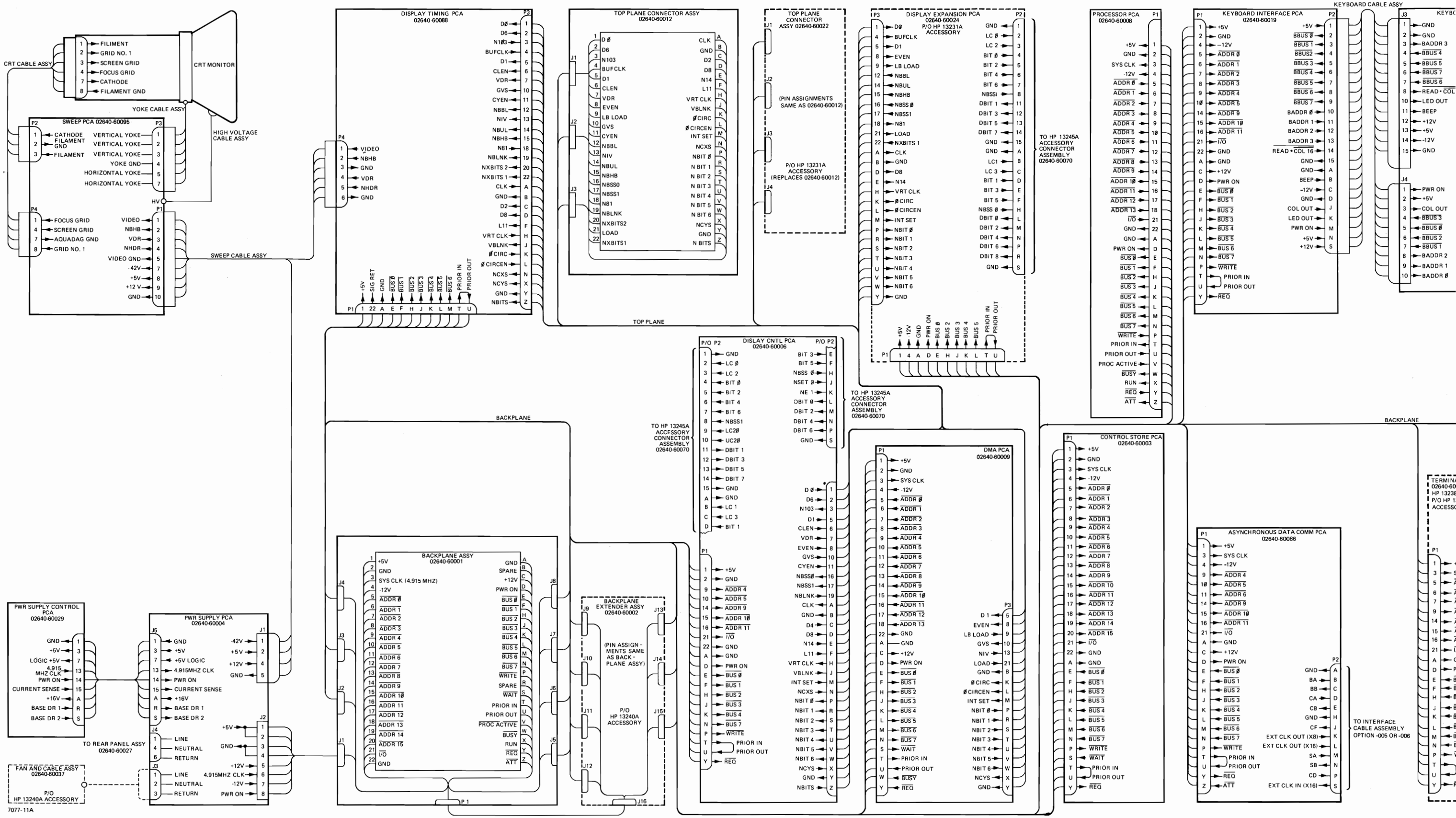


Figure 2-3. Terminal Interconnecting Cabling Diagram


CRT CABLE ASSY
CRT MONITOR
FILIMENT
GRID NO. 1
SCREEN GRID
FOCUS GRID
CATHODE
FILAMENT GND
YOKE CABLE ASSY
HIGH VOLTAGE CABLE ASSY
SWEEP PCA 02640-60095
CATHODE
FILAMENT
GND
FILAMENT
VERTICAL YOKE
VERTICAL YOKE
VERTICAL YOKE
YOKE GND
HORIZONTAL YOKE
HORIZONTAL YOKE
HV
FOCUS GRID
SCREEN GRID
AQUADAG GND
GRID NO. 1
VIDEO
NBHB
VDR
NHDR
VIDEO GND
-42V
+5V
+12 V
GND
SWEEP CABLE ASSY
DISPLAY TIMING PCA
02640-60088
VIDEO
NBHB
GND
VDR
NHDR
GND
+5V
SIG RET
GND
BUS Ø
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
PRIOR IN
PRIOR OUT
TOP PLANE CONNECTOR ASSY
02640-60012
TOP PLANE CONNECTOR ASSY 02640-60022
(PIN ASSIGNMENTS SAME AS 02640-60012)
P/O HP 13231A ACCESSORY (REPLACES 02640-60012)
DISPLAY EXPANSION PCA
02640-60024
P/O HP 13231A ACCESSORY
TO HP 13245A ACCESSORY CONNECTOR ASSEMBLY 02640-60070
PROCESSOR PCA
02640-60008
KEYBOARD INTERFACE PCA
02640-60019
KEYBOARD CABLE ASSY
TOP PLANE
BACKPLANE
DISLAY CNTL PCA
02640-60006
TO HP 13245A ACCESSORY CONNECTOR ASSEMBLY 02640-60070
DMA PCA
02640-60009
CONTROL STORE PCA
02640-60003
BACKPLANE ASSY
02640-60001
SYS CLK (4.915 MHZ)
BACKPLANE EXTENDER ASSY
02640-60002
(PIN ASSIGN-MENTS SAME AS BACK-PLANE ASSY)
P/O HP 13240A ACCESSORY
ASYNCHRONOUS DATA COMM PCA
02640-60086
TO INTERFACE CABLE ASSEMBLY OPTION -005 OR -006
PWR SUPPLY CONTROL PCA
02640-60029
PWR SUPPLY PCA
02640-60004
TO REAR PANEL ASSY 02640-60027
FAN AND CABLE ASSY
02640-60037
P/O HP 13240A ACCESSORY
7077-11A

3-1. INTRODUCTION

This section contains troubleshooting information for isolating malfunctions to a replaceable assembly and alignment and adjustment procedures.

WARNING

Hazardous voltages are present inside equipment. The procedures contained in this section shall be performed only by qualified service personnel.

VORSICHT

Innerhalb des Geräts bestehen gefährliche Spannungen. Die in diesem Abschnitt enthaltenen Arbeiten dürfen nur durch Betriebsfachpersonal durchgeführt werden.

ATTENTION

Des tensions dangereuses sont présentes à l'intérieur du matériel. Les opérations décrites dans cette section ne devront être effectuées que par un personnel qualifié.

AVVISO

Pericolo: Alta tensione presente in questa apparecchiatura. Le procedure contenute in questa sezione debbono essere effettuate soltanto da qualificato personale di servizio.

ADVERTENCIA

Hay voltaje peligroso en el interior de este equipo. Los procedimientos expuestos en esta sección sólo deberá llevarlos a cabo el personal de servicio calificado.

高圧危険

内部装置に危険な高電圧がきています。この章にある処置や手続に関しては、専門のサービスマンによってのみ行なって下さい。

3-2. TROUBLESHOOTING

3-3. GENERAL TROUBLE ISOLATION PROCEDURES

The majority of apparent terminal malfunctions are caused by incorrect operation. Therefore, before attempting any detailed trouble isolation procedures, verify that a terminal malfunction truly exists as follows:

a. Ensure that terminal is properly installed (power cord connected and fuse properly installed) and is set to correct operating mode.

b. Ensure that special function keys are being used correctly and in correct sequence.

c. Determine whether or not any recent service routines (accessory installation, cables removed or installed, adjustments performed, etc.) have been performed on terminal. If so, check workmanship.

d. Check all connections in accordance with paragraph 3-4.

e. Check keyboard and communication group in accordance with paragraph 3-5.

f. Perform terminal self test in accordance with paragraph 3-6.

3-4. CONNECTION INSPECTION

Set mainframe rear panel AC POWER switch to OFF, disconnect power cord, and inspect cable connections as follows:

a. Ensure that Keyboard Cable Assembly hood connector is firmly connected to Keyboard Interface PCA.

b. Ensure that interface cable assembly hood connector is firmly connected to Asynchronous Data Comm PCA.

c. If installed, ensure that peripheral interface cable assembly hood connector is firmly connected to Terminal Duplex Register PCA.

d. Open terminal mainframe to its full open position in accordance with paragraph 1-2 and check that all PCA's are firmly seated in Backplane Connector Assembly and, if installed, Backplane Extender Assembly connectors.

e. Remove power supply housing (bottom left side of mainframe) by unlatching the two snap locks on front of housing and pulling housing up and out toward front of mainframe. Ensure that Power Supply Control PCA is firmly seated in Power Supply PCA connector J5.

f. Ensure that all internal cable assembly connectors are correctly and firmly connected.

3-5. KEYBOARD AND COMMUNICATION GROUP CHECKOUT

The major part of the terminal keyboard can be quickly checked for proper operation by setting the terminal for local operation (REMOTE key up), pressing each of the keys listed in table 3-1, and obtaining the listed results. If an incorrect result is observed, a malfunction exists in either the Keyboard Interface PCA or Keyboard PCA. (Removal and replacement procedures are contained in section IV.) The communication group including the Asynchronous Data Comm PCA can be quickly checked for proper operation as follows:

a. Replace existing cable assembly hood connector connected to Asynchronous Data Comm PCA with HP Test Hood, part no. 02640-60077. The keyboard TRANSMIT indicator will light.

b. Depress REMOTE key, set BAUD RATE switch to 110, and DUPLEX switch to FULL.

c. Hold down any character key and check that associated character is repeatedly displayed across display monitor at a slow rate of speed for as long as the key is held down.

Note: Delete symbol (white square) may appear on display monitor when switching baud rates.

d. While holding down character key, increase baud rate to 150 and then to 300 and check that displayed character repetition rate increases as baud rate increases. If operation is not as stated, a malfunction probably exists in Asynchronous Data Comm PCA or Keyboard Assembly. (Baud rates above 300 will not increase character repetition rate.)

e. Set DUPLEX switch to HALF.

f. Depress any character key once and check that associated charater is displayed twice on display monitor. If operation is not as stated, a malfunction probably exists in Asynchronous Data Comm PCA or Keyboard Assembly.

Table 3-1. Keyboard Checkout Keys

KEY	RESULTS
DISPLAY FUNCTIONS	DISPLAY FUNCTIONS indicator lights
1	1 is displayed
Q or q	Q or q is displayed
Z or z	Z or z is displayed
L	L is displayed
Numeric Pad 1	1 is displayed
Numeric Pad 4	4 is displayed
CNTL G	⏃ is displayed
Release DISPLAY FUNCTIONS key and again press CNTL G keys	Audible "Beep" is generated

3-6. SELF TEST

The self-test feature provides a check of the entire terminal making it possible to quickly analyze and isolate most terminal malfunctions. (Removal and replacement procedures are contained in Section IV.) Perform the test as follows:

a. Set mainframe rear panel AC POWER switch to ON position and check that some keyboard indicators flash on and then off. This verifies that power supply section is operating correctly. If any indicators with the exception of TRANSMIT indicator remain lighted, a malfunction exists in Processor PCA.

b. Check that blinking cursor appears in upper left corner of display monitor approximately seven seconds after terminal is energized. This verifies that Processor, Control Store, Display Memory Access (DMA), Display Control, and Display Timing PCA's are operating correctly. If cursor does not appear, malfunction probably exists in Sweep PCA.

c. Press Keyboard TEST key and observe following sequence of events:

(1) Keyboard indicators light. If no indicators light, malfunction probably exists in Power Supply or Power Supply Control PCA.

(2) Control Store PCA ROMs are checked. In most cases, if a ROM malfunction is encountered, monitor will display "ROM TEST FAILED", indicating a defective Control Store PCA.

(3) Entire display including cursor momentarily blanks which checks display portions of Processor, DMA, Display Control, and Display Timing PCA's. If display does not clear (blank), malfunction probably exists in Display Control PCA.

(4) While display is still blanked, Control Store, 2K Memory, and 4K Memory PCA RAMs are checked. In most cases, if a RAM malfunction is encountered, monitor will display "RAM TEST FAILED" indicating a defective Control Store, 2K Memory, or 4K Memory PCA.

(5) An audible "beep" is generated. If not, keyboard speaker may be defective or a malfunction probably exists in Processor PCA.

(6) Entire character set is displayed and, after printout, blinking cursor appears in first column of next lower line. The test pattern contains all available symbols and display enhancements. Last line of test pattern displays status of terminal. Refer to *HP 2640A Interactive Display Terminal Owner's Manual* for status byte definitions and correct test pattern displays. If test pattern is incorrect, refer to paragraph 3-7.

3-7. DETAILED TROUBLE ISOLATION PROCEDURES

Any terminal malfunctions not isolated and corrected by the procedures contained in paragraphs 3-3 through 3-6 can be isolated to a replaceable assembly by performing in sequence the procedures presented in figure 3-1. Some corrective action procedures in figure 3-1 consist of more than one replacement instruction. When these are encountered, replace the first assembly listed and *check if the malfunction has been corrected.* (Removal and replacement procedures are contained in Section IV.) If the malfunction persists, reinstall the first assembly listed, replace the second assembly listed, and again check if the malfunction has been corrected. As an additional troubleshooting aid, figure 2-3 provides a terminal interconnecting cabling diagram illustrating source and destination signal flow between replaceable assemblies. After any malfunction has been corrected, use the terminals self-test feature to ensure proper operation.

3-8. ALIGNMENT AND ADJUSTMENT

All alignment and adjustment procedures for the terminal and its add-on accessories are contained in the following paragraphs. Unless otherwise specified, these procedures can be performed individually or in any desired sequence.

Note: After performing any alignment or adjustment procedures, alwyas use the terminals self-test feature (paragraph 3-6) to ensure proper terminal operation.

3-9. POWER SUPPLY VOLTAGE ADJUSTMENT

This procedure requires the use of an HP 34740A Multimeter or equivalent. Adjust the power supply as follows:

a. Open terminal mainframe to its half open position in accordance with paragraph 1-2.

b. Remove power supply housing (bottom left side of mainframe) by unlatching the two snap locks on front of housing and pulling housing up and out toward front of mainframe.

c. Connect multimeter between +5V diode CR17 (see figure 3-2) and chassis ground.

d. Connect power cord between ac power source and mainframe rear panel LINE connector.

e. Set rear panel AC POWER switch to ON position.

f. Adjust +5V potentiometer R14 (see figure 3-2) for a multimeter indication between +4.85V and +5.25V.

g. Using multimeter, check for -40V to -46V at diode CR9 (see figure 3-2), +11.4V to +12.6V at diode CR13, and -11.4V to -12.6V at diode CR14.

h. If necessary, repeat step f until all voltage levels are those specified in step g.

i. Set rear panel AC POWER switch to OFF and disconnect multimeter leads from power supply.

j. Replace power supply housing and secure in place with the two snap locks.

k. Close terminal mainframe.

3-10. BRIGHTNESS, HALF BRIGHT, AND FOCUS ADJUSTMENTS

Due to product design, these adjustments seldom need be performed. However, minor adjustment can be made to each potentiometer (see figure 3-3) to suit individual preferences by opening the terminal mainframe to its half open position in accordance with paragraph 1-2, removing the CRT shield (see figure 1-2), energizing the terminal, and adjusting the applicable potentiometer for the desired display appearance. If extensive repair or replacement procedures have been performed on the terminal, it is suggested that the adjustment procedure below be performed in its entirety to ensure optimum terminal performance.

This procedure requires the use of the HP Display Test Module, part no. 02640-60063. The brightness, half bright, and focus adjustments are interactive and, therefore, must be performed together. Perform the adjustments using a nonconductive tool as follows:

a. Open terminal mainframe to its full open position in accordance with paragraph 1-2.

b. Insert connector removal tool under Top Plane Connector Assembly as shown in figure 1-5 and remove assembly by pressing down on removal tool handle.

c. Remove Display Memory Access (DMA) PCA from Backplane Assembly.

d. If necessary, rearrange backplane PCA configuration so that Keyboard Interface PCA is installed in Backplane Assembly connector closest to power supply, the next connector is vacant, and Display Timing and Display Control PCA's are installed in the third and fourth connectors.

e. Install Display Test Module on top connectors of Display Timing and Display Control PCA'S so that test module cable is toward front of mainframe.

f. Connect test module cable plug to Display Timing PCA +5V red test jack located on top front of PCA.

g. Connect power cord between ac power source and mainframe rear panel LINE connector.

h. Set rear panel AC POWER switch to on position.

i. Set test module HALF BRIGHT switch to off position, INVERSE VIDEO switch to off position, and DOTS/CROSSHATCH switch to DOTS.

j. Adjust BRIGHTNESS R37 (see figure 3-3) for desired display brightness.

k. Set test module HALF BRIGHT switch to on position, remove button covering CRT shield HALF BRIGHT adjustment access hole, and adjust HALF BRIGHT R5 for desired display half brightness.

l. Repeat steps i, j, and k until desired display contrast is obtained between full bright and half bright.

m. Set test module HALF BRIGHT switch to off position.

n. Adjust FOCUS R33 (see figure 3-3) for best overall display sharpness.

o. If desired focus cannot be obtained, adjust display brightness slightly lower and repeat steps i through n.

p. Set rear panel AC POWER switch to OFF.

q. Reinstall button to cover HALF BRIGHT adjustment access hole.

r. Disconnect test module cable plug from Display Timing PCA and disconnect test module from Display Timing and Display Control PCA's.

s. Reinstall DMA PCA into vacated Backplane Assembly connector and reinstall Top Plane Connector Assembly on DMA, Display Timing, and Display Control PCA's.

t. Close terminal mainframe.

3-11. DISPLAY EXPANSION FIELD ADJUSTMENT

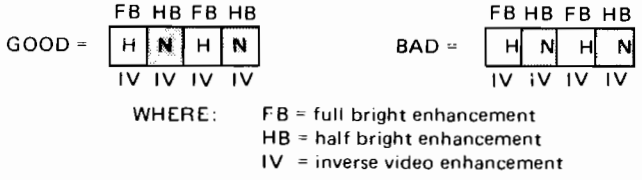
After initial installation of the HP 13231A Display Enhancements Accessory, check and, if necessary, adjust the Display Expansion PCA as follows:

a. Open terminal mainframe to its half open position in accordance with paragraph 1-2.

b. Connect power cord between ac power source and mainframe rear panel LINE connector.

c. Set rear panel AC POWER switch to on position.

d. Using keyboard, set terminal for local operation (REMOTE key up) and press each of the following keys once: CAPS LOCK, ENHANCE DISPLAY, B, H, ENHANCE DISPLAY, J, N, ENHANCE DISPLAY, B, H, ENHANCE DISPLAY, J, N. Compare display against examples below.



e. If necessary, adjust Display Expansion PCA FIELD potentiometer R10 to center full bright and half bright enhancements over characters displayed on monitor.

f. Set rear panel AC POWER switch to OFF and close terminal mainframe.

3-12. DISPLAY RASTER ALIGNMENT AND ADJUSTMENT

This procedure requires the use of the HP Display Test Module, part no. 02640-60063. Align and adjust the display raster as follows:

a. Open terminal mainframe to its full open position in accordance with paragraph 1-2. Remove CRT shield (see paragraph 1-46).

b. Insert connector removal tool under Top Plane Connector Assembly as shown in figure 1-5 and remove assembly by pressing down on removal tool handle.

c. Remove DMA PCA from Backplane Assembly.

d. If necessary, rearrange backplane PCA configuration so that Keyboard Interface PCA is installed in Backplane Assembly connector closest to power supply, the next connector is vacant, and Display Timing and Display Control PCA's are installed in the third and fourth connectors.

e. Install Display Test Module on top connectors of Display Timing and Display Control PCA's so that test module cable is toward front of mainframe.

f. Connect test module cable plug to Display Timing PCA red test jack located on top front of PCA.

g. Connect power cord between ac power source and mainframe rear panel LINE connector.

h. Set rear panel AC POWER switch to on position.

i. Set test module HALF BRIGHT switch to off position, INVERSE VIDEO switch to on position, and DOTS/CROSSHATCH switch to center off position.

j. The monitor should display an inverse video rectangular pattern. If no pattern is displayed, adjust BRIGHTNESS R37 (see figure 3-3) until pattern is displayed. If this step is required, perform brightness and focus adjustments in accordance with paragraph 3-10 after completing raster alignment and adjustment procedures.

WARNING

High voltage is present on exposed portions of Yoke Cable Assembly.

VORSICHT

An den offenen Stellen des Joch-Kabelsatzes (Yoke Cable Assembly) besteht Hochspannung!

ATTENTION

Du courant haute tension passe dans les parties exposées de l'ensemble de câbles de culasse (Yoke Cable Assembly).

AVVISO

Voltaggio ad alta tensione presente su parti scoperte della linea montaggio di cavo collegamento (Yoke Cable Assembly).

ADVERTENCIA

Hay voltaje peligroso en las partes al descubierto del conjunto de cable de horquilla (Yoke Cable Assembly).

高圧危険

ヨーク・ケーブルアセンブリの露出部には、高電圧がかかってます。

k. Rotate Yoke Cable Assembly (see figure 3-3) until displayed rectangle is horizontal and parallel to monitor frame.

l. Rotate centering magnets (black tabs) until displayed rectangle is centered on monitor screen.

m. Adjust WIDTH R28 until displayed rectangle is 9.5 in. (24 cm) wide. This should give a border of approximately 0.5 in. (1.2 cm) on either side.

n. Adjust HEIGHT R10 until displayed rectangle is 4.75 in. (12 cm) high. This should give a border of approximately 0.25 in. (.6 cm) at the top and bottom.

o. Set rear panel AC POWER switch to OFF and replace the CRT shield.

p. Disconnect test module cable plug from Display Timing PCA and disconnect test module from Display Timing and Display Control PCA's.

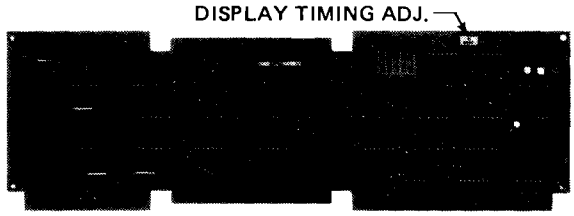
q. Reinstall DMA PCA into vacated Backplane Assembly connector and reinstall Top Plane Connector Assembly on DMA, Display Timing, and Display Control PCA's.

r. Close terminal mainframe and check for correct raster alignment.

3-13 DISPLAY TIMING ADJUSTMENT

After installation of the Display Timing PCA (part no. 02640-60088), check and, if necessary, adjust the CRT dot size for equal brightness of vertical and horizontal lines. Before performing the adjustment, check that the BRIGHTNESS, HALF BRIGHT, and FOCUS are adjusted properly (refer to paragraph 3-10).

a. With the terminal mainframe in its half open position and power applied to the terminal, locate the display timing adjustment (see figure below).



b. Press and hold the "E" key to produce a row of uppercase E's on the display.

c. Adjust display timing so that the vertical and horizontal lines of the E's are of equal brightness (see figure below).

d. Again, check that the BRIGHTNESS, HALF BRIGHT, and FOCUS are adjusted for proper display.

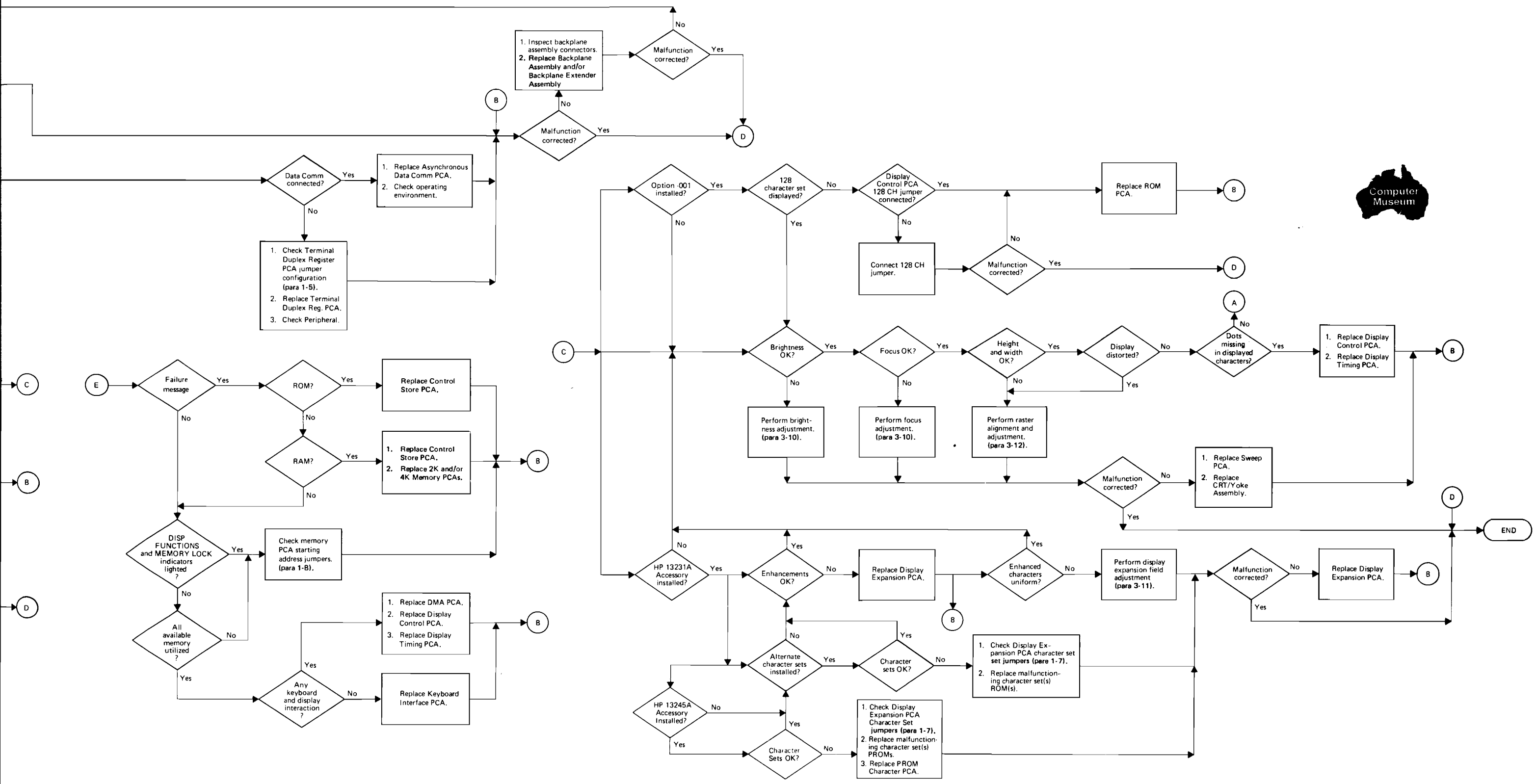
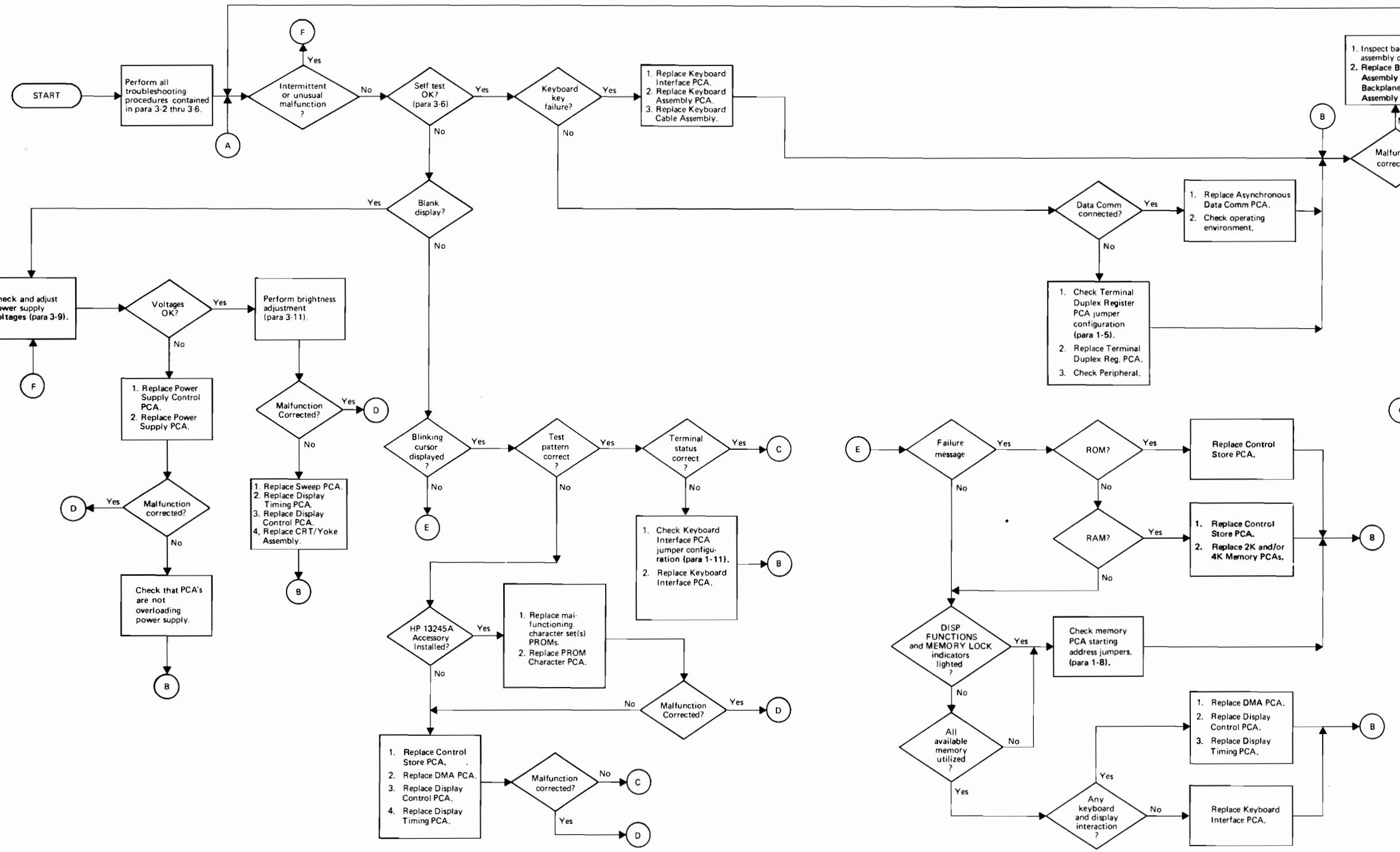


Figure 3-1. Troubleshooting Flowchart


START
Perform all troubleshooting procedures contained in para 3-2 thru 3-6.
Intermittent or unusual malfunction ?
Yes
No
F
A
Self test OK? (para 3-6)
Yes
No
Keyboard key failure?
Yes
No
1. Replace Keyboard Interface PCA.
2. Replace Keyboard Assembly PCA.
3. Replace Keyboard Cable Assembly.
Blank display?
Yes
No
Check and adjust power supply voltages (para 3-9).
Voltages OK?
Yes
No
F
1. Replace Power Supply Control PCA.
2. Replace Power Supply PCA.
Malfunction corrected?
Yes
No
D
Check that PCA's are not overloading power supply.
B
Perform brightness adjustment (para 3-11).
Malfunction Corrected?
Yes
No
D
1. Replace Sweep PCA.
2. Replace Display Timing PCA.
3. Replace Display Control PCA.
4. Replace CRT/Yoke Assembly.
B
Blinking cursor displayed ?
Yes
No
E
Test pattern correct ?
Yes
No
Terminal status correct ?
Yes
No
C
1. Check Keyboard Interface PCA jumper configuration (para 1-11).
2. Replace Keyboard Interface PCA.
B
HP 13245A Accessory Installed?
Yes
No
1. Replace malfunctioning character set(s) PROMs.
2. Replace PROM Character PCA.
Malfunction Corrected?
Yes
No
D
1. Replace Control Store PCA.
2. Replace DMA PCA.
3. Replace Display Control PCA.
4. Replace Display Timing PCA.
Malfunction corrected?
No
C
Yes
D
Data Comm connected?
Yes
No
1. Replace Asynchronous Data Comm PCA.
2. Check operating environment.
1. Check Terminal Duplex Register PCA jumper configuration (para 1-5).
2. Replace Terminal Duplex Reg. PCA.
3. Check Peripheral.
B
1. Inspect backplane assembly connectors.
2. Replace Backplane Assembly and/or Backplane Extender Assembly
Malfunction corrected?
No
Yes
D
Malfunction corrected?
No
Yes
D
E
Failure message
Yes
No
ROM?
Yes
No
Replace Control Store PCA.
RAM?
Yes
No
1. Replace Control Store PCA.
2. Replace 2K and/or 4K Memory PCAs.
B
DISP FUNCTIONS and MEMORY LOCK indicators lighted ?
Yes
No
Check memory PCA starting address jumpers. (para 1-8).
All available memory utilized ?
No
Yes
1. Replace DMA PCA.
2. Replace Display Control PCA.
3. Replace Display Timing PCA.
B
Any keyboard and display interaction ?
Yes
No
Replace Keyboard Interface PCA.
C
Option -001 installed?
Yes
No
128 character set displayed?
Yes
No
Brightness OK?
Yes
No
Perform brightness adjustment. (para 3-10).
HP 13231A Accessory installed?
Yes
No
Enhancements OK?
Yes
No
Alternate character sets installed?
Yes
No
HP 13245A Accessory Installed?
Yes
No
Character Sets OK?
Yes
No

7077-14A

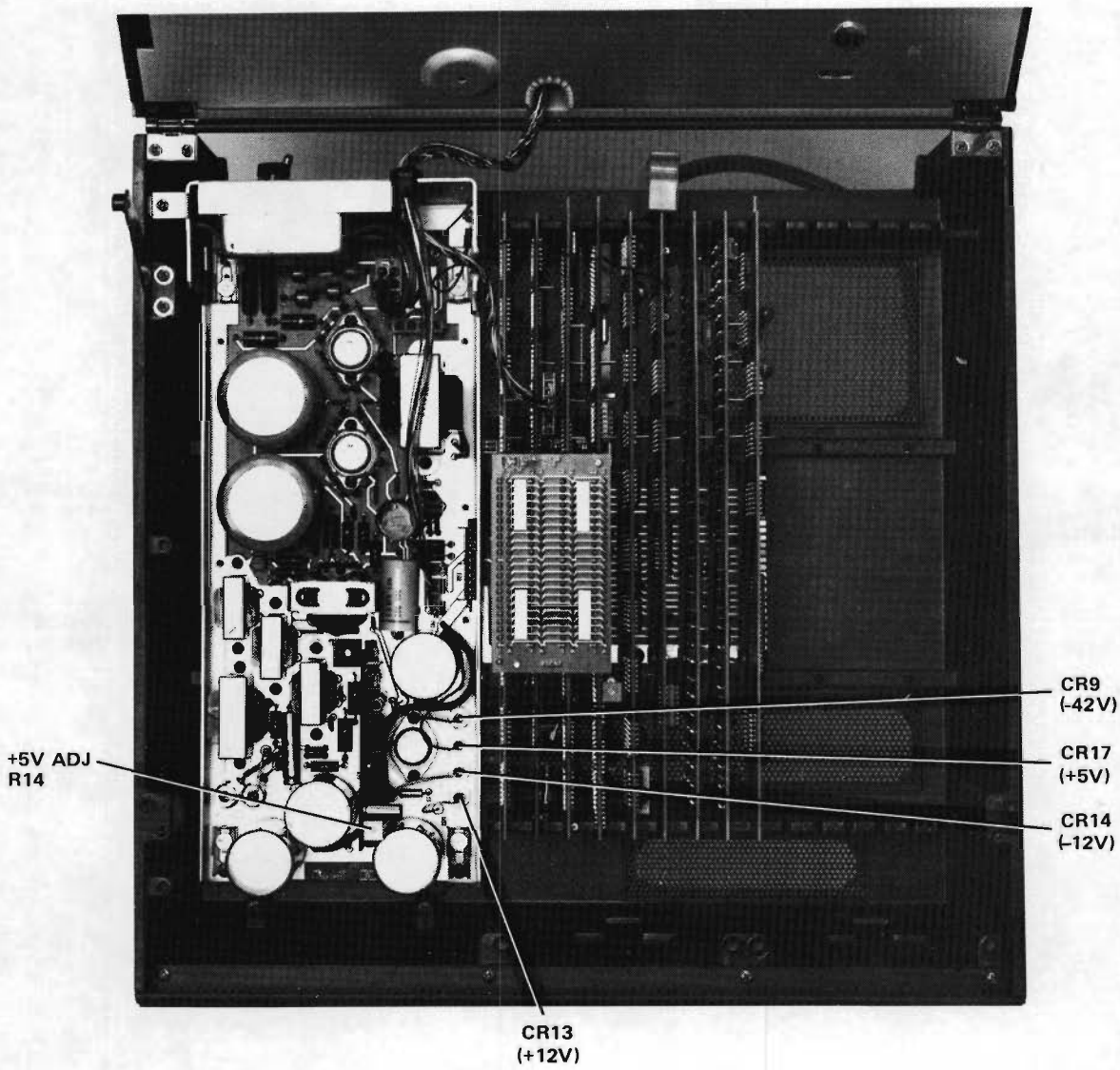


Figure 3-2. Power Supply Test Point and Adjustment Locations

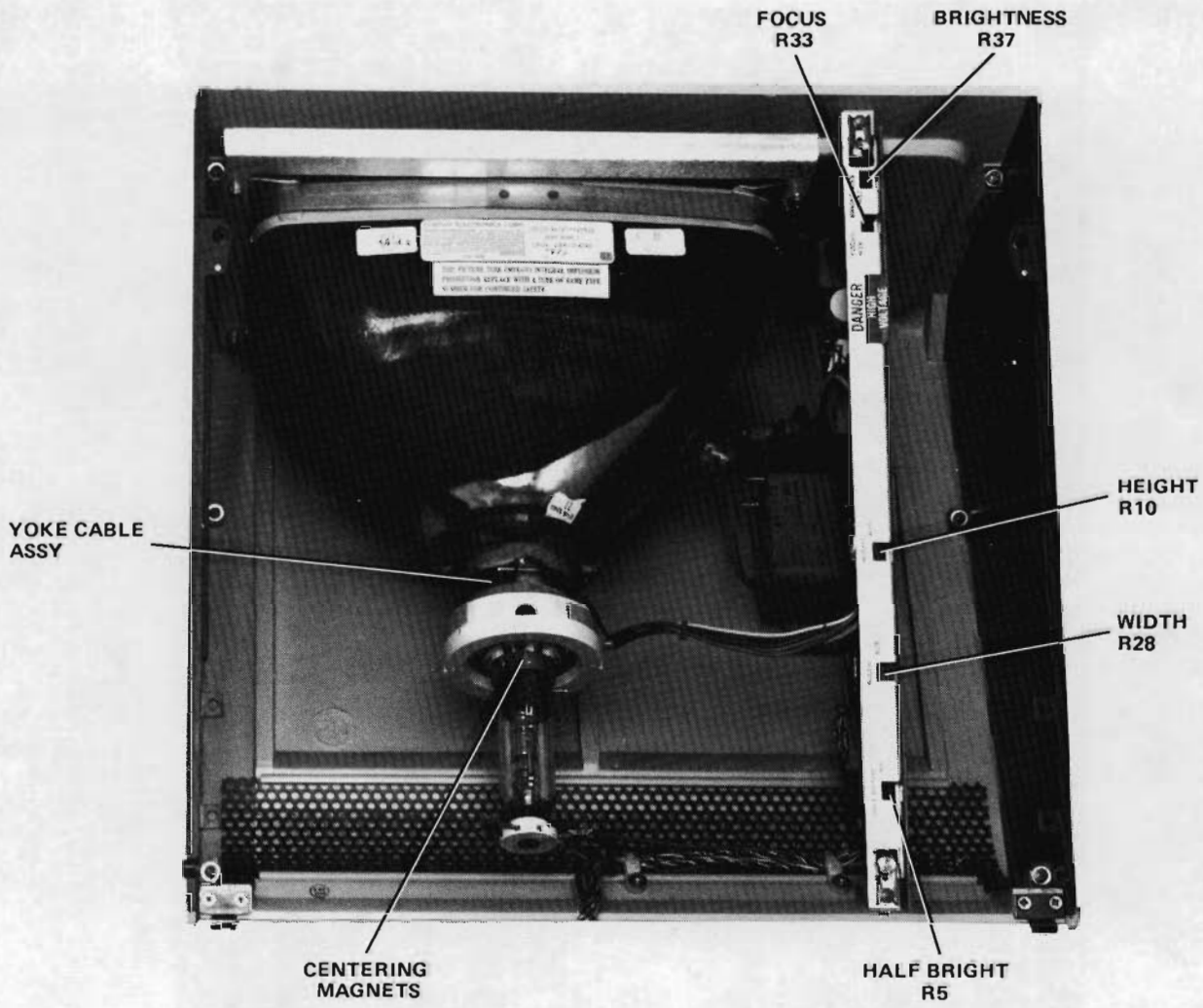


Figure 3-3. Mainframe Top Adjustment Locations

REPAIR

SECTION IV

4-1. INTRODUCTION

This section contains instructions for removing and replacing terminal assemblies and a listing of field-replaceable parts.

WARNING

Hazardous voltages are present inside equipment. The procedures contained in this section shall be performed only by qualified service personnel.

VORSICHT

Innerhalb des Geräts bestehen gefährliche Spannungen. Die in diesem Abschnitt enthaltenen Arbeiten dürfen nur durch Betriebsfachpersonal durchgeführt werden.

ATTENTION

Des tensions dangereuses sont présentes à l'intérieur du matériel. Les opérations décrites dans cette section ne devront être effectuées que par un personnel qualifié.

AVVISO

Pericolo: Alta tensione presente in questa apparecchiatura. Le procedure contenute in questa sezione debbono essere effettuate soltanto da qualificato personale di servizio.

ADVERTENCIA

Hay voltaje peligroso en el interior de este equipo. Los procedimientos expuestos en esta sección sólo deberá llevarlos a cabo el personal de servicio calificado.

高圧危険

内部装置に危険な高電圧がきています。この章にある処置や手続に関しては、専門のサービスマンによってのみ行なって下さい。

4-2. REMOVAL AND REPLACEMENT

WARNING

Always remove AC power from terminal before attempting any parts replacements. Use extreme caution when working near the CRT, Yoke Cable Assembly, and Sweep PCA high voltage sections.

VORSICHT

Vor Auswechseln von Einzelteilen ist jeweils der Wechselstromanschluss von der Klemme zu trennen. Bei Arbeiten in der Nähe der Hochspannungsteile von Kathodenstrahlröhre (CRT), Joch-Kabelsatz (Yoke Cable Assembly) sowie der gedruckten Schaltung für den Kipposzillator (Sweep PCA) ist grösste Vorsicht zu beachten.

ATTENTION

Toujours couper l'arrivée de courant alternatif des bornes avant d'entreprendre tout remplacement de pièces. Redoubler de prudence lorsqu'on travaille à proximité des sections haute tension du tube cathodique (CRT), de l'ensemble de câbles de culasse (Yoke Cable Assembly), et de l'ensemble de tableau de circuit oscillant (Sweep PCA).

AVVISO

Isolare sempre la tensione c.a. dal morsetto prima di procedere alla sostituzione di qualsiasi parte. Usare estrema cautela durante operazioni in prossimità delle sezioni ad alta tensione del tubo a raggi catodici (CRT), della linea montaggio cavo collegamento (Yoke Cable Assembly), e della linea del circuito stampato per l'oscillatore di base di tempi (Sweep PCA).

ADVERTENCIA

Desconéctese siempre la corriente alterna del terminal antes de intentar reemplazar cualquier pieza. Téngase sumo cuidado al trabajar cerca de las secciones de alta tensión del tubo de rayos catódicos (CRT), del conjunto de cable de horquilla (Yoke Cable Assembly), y del circuito impreso del oscilador de base de tiempo (Sweep PCA).

⚠ **高圧危険** ⚠

どんな部品でも交換する場合は、その前にＡＣの電源コードを機器よりはずして下さい。ＣＲＴ、ヨーク・ケーブルアセンブリ、スイープＰＣＡなどの高電圧がかかっている部分の近くでは、危険ですから特に注意を払って下さい。

Due to the modular design of the terminal, no special instructions are required for removing and replacing parts except for those discussed in paragraphs 4-3 through 4-6. To remove most replaceable parts, first refer to figure 4-1 and the replaceable parts list to determine how the part is attached and the number of attaching parts involved. Once this is accomplished, removal procedures for the part will be obvious. Always disconnect any attached cable assemblies before attempting to remove a part. Replacing a part is simply a matter of reversing the removal procedure.

4-3. DISPLAY CONTROL PCA

The Display Control PCA is manufactured with a jumper installed for use with a 128 character set terminal (Option 001). When replacing the Display Control PCA, first determine whether the terminal is equipped with a 64 character set (standard model) or a 128 character set. For standard model terminals, disconnect the soldered in 128 CH jumper located approximately in the center of the Display Control PCA before installing it in the terminal. For Option 001 terminals, install the PCA in the terminal as shipped from the factory.

4-4. FAN AND FAN CABLE ASSEMBLY

When removing the Fan and Fan Cable Assembly 65, figure 4-1), first open the terminal mainframe to its full open position in accordance with paragraph 1-2. Then, disconnect the assembly's connector from the Power Supply PCA and remove the two cable clamps and wire harness attached to the fan. After removing the assembly's cable from the existing wire harness and cable clamps, remove the four screws and washers securing the assembly to the mainframe top and remove the assembly from the terminal. Installing the Fan and Fan Cable Assembly is accomplished by performing the removal procedures in reverse order. However, care should be taken to ensure that the assembly's cable is secured within the left cable clamp. Also, the assembly must be mounted so that its cable is closest to the back of the mainframe top and CRT, and the fan AIRFLOW arrow must point toward the back of the mainframe top. Refer to the installation procedures in paragraph 1-4.

4-5. PROM CHARACTER PCA

The PROM Character PCA consists entirely of field-replaceable parts. After removing the PCA from the terminal (figure 4-1), refer to figure 4-2 for component location and identification information.

4-6. KEYBOARD OVERLAY AND KEYBOARD

The keyboard overlay (84, figure 4-1) is tension mounted on the keyboard top (86) by means of the overlay's hooked left end and a tension spring attached under its right end. To remove and replace the overlay, proceed as follows:

a. Locate keyway on right side of keyboard top and insert access key supplied with terminal.

b. Push access key into keyway (no key rotation is required) until overlay tension spring is released.

c. When the tension spring is released, the right end of the overlay will raise up high enough to grasp. If not, the right end of the overlay can be pried up with a small screwdriver or similar tool.

d. Unhook the left end of the overlay from the keyboard top by sliding it to the left and remove overlay from keyboard top.

e. When replacing the overlay, hook the left end of the overlay in place on the keyboard top, guide the overlay down over the switch keys, and press down on the right end of the overlay until the tension spring snaps into place.

The keyboard is disassembled by removing five screws and ten washers from keyboard bottom, and lifting off keyboard top. After keyboard top is off, the Keyboard Assembly can be removed by disconnecting it from the two Keyboard Cable Assembly connectors and Loudspeaker Assembly, and lifting it out of the keyboard bottom.

4-7. POWER SUPPLY CONTROL, POWER SUPPLY, AND SWEEP PCA'S

In addition to its mating connector, the Power Supply Control PCA (2, figure 4-1) is attached to the Power Supply PCA (3) with two slotted PCA mounting guide posts that contain detents to lock the PCA in place. To remove the Power Supply Control PCA, first pull one of the mounting guide posts slightly away from the PCA's edge to free the detent and then, carefully rock the PCA up and out of its mating connector on the Power Supply PCA. To replace the PCA, align the PCA's edges with the mounting guide post slots and press down firmly on the PCA until it is seated in its mating connector and locked in place by the mounting guide post slot detents.

To remove the Power Supply PCA (3, figure 4-1), first remove the power supply housing (1) by unlatching the two snap locks on front of housing and pulling the housing up and out toward the front of the mainframe shell (51). Then, after disconnecting the three wire harness connectors from the PCA, unlatch the snap locks in each of the

four corners of the PCA and lift the entire PCA up and out of the mainframe shell. Installing the Power Supply PCA is basically accomplished by performing the removal procedures in reverse order. However, care should be taken not to damage the Backplane Assembly (45) connector pins that mate with the Power Supply PCA bottom connector J2.

To remove the Sweep PCA (63, figure 4-1), first open the terminal mainframe to its full open position in accordance with paragraph 1-2. Then, unlatch the snap locks at each end of the Sweep PCA and move the PCA up and to the right far enough to gain easy access to all cable connectors. Disconnect the High Voltage Cable Assembly from the CRT by pressing the cable assembly connector sides together and pulling it out of the CRT. Disconnect the remaining four cable connectors from the Sweep PCA and completely remove the PCA from the terminal. It is recommended that the cable connectors be disconnected in the order of P1, P2, P4, and P3.

4-8. ACCESSORIES

No special instructions are required to remove any terminal accessories. However, before attempting to replace an accessory, refer to the detailed installation instructions for the applicable accessory in Section I of this manual or if available, the accessory manual.

4-9. REPLACEABLE PARTS

Replaceable parts for the terminal are listed in tables 4-1 and 4-2. The replaceable parts in table 4-1 are referenced to the exploded view (figure 4-1) of the terminal by index numbers which are in disassembly order, except attaching parts are listed immediately after the parts they attach. Items in the DESCRIPTION column of table 4-1 are indented to indicate item relationship. In addition, the symbol "— — — X — — —" follows the last of one or more attaching parts. Indention is as follows:

MAJOR ASSEMBLY

- · Replaceable Assembly
- · Attaching Parts for Replaceable Assembly
- ·· Subassembly Parts
- ·· Attaching Parts for Subassembly Parts

Table 4-1 provides the following information for each part:

a. FIG & INDEX NO. The figure and index where the replaceable parts are shown in the exploded view.

b. HP PART NO. The Hewlett-Packard part number for each replaceable part.

c. DESCRIPTION. The description and any special applications (accessories and options) for each replaceable part.

d. UNITS PER ASSY. The total quantity of each part used in the major assembly.

Table 4-2 provides the reference designation, Hewlett-Packard part number, and description for each PROM Character PCA replaceable part. In addition, table 4-2 provides the original manufacturer's part number for each replaceable part and a manufacturer code number which is cross-referenced to the code list of manufacturers contained in table 4-3. Table 4-3 contains each manufacturer's name, address, and code number. The code numbers are from the

Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and *H4-2*, and the latest supplements.

4-10. ORDERING INFORMATION

To order replaceable parts for the terminal or options and accessories, address the order to the local Hewlett-Packard Sales and Service Office listed at the end of this manual.

The following information should be included in the order for each part.

a. Complete terminal model number (including options and accessories) and serial number.

b. Hewlett-Packard part number.

c. Complete part description as provided in the replaceable parts list.

Table 4-1. Terminal Replaceable Parts List (Sheet 1 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
4-1	2640A	**Interactive Display Terminal**	
1	02640-00001	• Housing	1
2	02640-60029	• Power Supply Control Assembly	1
3	02640-60004	• Power Supply Assembly	1
4	8120-1378	• Power Cord Set, 250V, 6A	1
	8120-1351	• Power Cord Set, 250V, 13A	1
	8120-1369	• Power Cord Set, 250V, 10A	1
	8120-1689	• Power Cord Set, 250V, 10/16A	1
	8120-2104	• Power Cord Set, 250V, 6A	1
	02640-60027	• Rear Panel Assembly	1
		(Attaching Parts)	
5	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	2
6	2190-0918	• Washer, Lock, split, no. 6	2
7	3050-0066	• Washer, Flat, no. 6	2
		– – – X – – –	
8	*2110-0470	•• Fuseholder Body	1
		(Attaching Parts)	
	1400-0090	•• Washer, Neoprene, 5/8 in. OD	1
	2190-0037	•• Washer, Lock, int-tooth	1
	2950-0054	•• Nut, Hex, 1/2-28	1
		– – – X – – –	
	2110-0465	•• Fuseholder Cap	1
	2110-0365	•• Fuse, 4A, SB, 250V (F1)	1
	2110-0303	•• Fuse, 2A, SB, 250V (F1) (used for Option 015)	1
9	3101-0646	•• Power Switch	1
		(Attaching Parts)	
	0590-0012	•• Nut, Self, locking, knurled, no. 15/32-32	1
	2190-0102	•• Washer, Lock, int-tooth, 7/16 in. ID	1
	2950-0035	•• Nut, Hex, 15/32-32	1
		– – – X – – –	
10	9135-0028	•• Line Filter	1
		(Attaching Parts)	
11	2420-0003	•• Nut, Plain, no. 6	2
		– – – X – – –	
12	02640-60083	•• Ground Wire	1
	0890-0006	•• 4" Hi shrink Tubing	1
		(Attaching Parts)	
	0362-0332	•• Ring Lug	1
	2190-0008	•• Washer, Lock, ext-tooth	1
		– – – X – – –	
13	02640-0042	•• Rear Panel and Connector Housing	1
14	02640-00010	• Support	1
		(Attaching Parts)	
15	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	2
16	2190-0918	• Washer, Lock, split, no. 6	2
17	3050-0066	• Washer, Flat, no. 6	2
		– – – X – – –	
18	**4040-1023	• Front Bezel	1
19	7120-1254	• Logo	1
20	02640-00047	• Insert	1
		(Attaching Parts)	
21	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	4
22	2190-0918	• Washer, Lock split, no. 6	4
23	3050-0066	• Washer, Flat, no. 6	4
		– – – X – – –	

*Order part no. 2110-0470 to replace part no. 2110-0464.

**Order part no. 4040-1023 to replace part no. 02640-20008.

Table 4-1. Terminal Replaceable Parts List (Sheet 2 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
24	02640-20007	• Rear Door	1
25	3101-0100	• Hinge Support, Right	1
	3101-0101	• Hinge Support, Left	1
26	02640-20011	• Hinge Bottom	2
		• (Attaching Parts)	
27	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	4
28	2190-0012	• Washer, Lock, int. tooth, no. 6	4
		– – – X – – –	
29	02640-60019	• Keyboard Interface Assembly	1
30	02640-60022	• Top Plane Connector Assembly (used for Accessory 13231A)	1
31	02640-60070	• Connector Assembly (used for Accessory 13245A)	1
32	02640-60053	• PROM Character Assembly (used for Accessory 13245A) See figure 4-2	1
33	02640-60006	• Display Control Assembly	1
	1816-0613	•• I.C., 128 Character ROM (used for Option 001)	1
34	* 02640-60088	• Display Timing Assembly	1
	0410-0647	•• Crystal, 21.06 MHz (Y1)	1
	0410-0646	•• Crystal, 17.55 MHz (Y1) (used for Option 015)	1
35	02640-60009	• Display Memory Access Assembly	1
36	02640-60024	• Display Expansion Assembly (used for Accessory 13231A)	1
	1816-0642	•• Math Character Set (used for Accessory 13231A-201)	1
	1816-0641	•• Line Drawing Set (used for Accessory 13231A-202)	1
37	02640-60003	•• Control Store Assembly	1
	1818-0130	•• I.C., ROM, MOS — For option 015 terminals with prefix 1551 or 1608 replace with: 1818-0172	1
	1818-0131	•• I.C., ROM, MOS — For option 015 terminals with prefix 1551 or 1608 replace with: 1818-0173	1
	1818-0132	•• I.C., ROM, MOS — For option 015 terminals with prefix 1551 or 1608 replace with: 1818-0174	1
	1818-0133	•• I.C., ROM, MOS — For option 015 terminals with prefix 1551 or 1608 replace with: 1818-0175	1
38	02640-60008	• Processor Assembly	1
39	02640-60043	• 103/202 Modem Cable Assembly (used for Option 005)	1
	02640-60058	• 12531/12880 Interface Cable Assembly (used for Accessory 13232B)	1
	02640-60059	• R232C Cable Assembly (used for Option 006)	1
40	** 02640-60086	• Asynchronous Data Comm Assembly	1
41	13238-60001	• 9866 Cable Assembly (used for Accessories 13238A-001 and 13246A and Option 012)	1
42	02640-60031	• Terminal Duplex Register Assembly (used for Accessories 13238A and 13246A and Option 012)	1
43	02640-60064	• +2K Memory Assembly (used for Accessory 13233A)	2
44	02640-60065	• +4K Memory Assembly (used for Accessory 13234A)	2
45	02640-60001	• Backplane Assembly	1
		(Attaching Parts)	
46	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	4
47	2190-0918	• Washer, Lock, split, no. 6	4
		– – – X – – –	
48	02640-60002	• Backplane Extender Assembly (used for Accessory 13240A)	1
		(Attaching Parts)	
49	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	4
50	2190-0918	• Washer, Lock, split, no. 6	4
		– – – X – – –	
51	02640-40001	• Mainframe Shell	1
52	02640-00021	• Access Key	2
53	02640-40002	• Display Top	1
54	3110-0099	• Hinge Top	2
		(Attaching Parts)	
55	2360-0196	• Screw, Machine, flh, no. 6-32, 3/8 in.	2
		– – – X – – –	

NOTE: *Order part no. 02640-60088 to replace part no. 02640-60005 or part no. 02640-60072.
**Order part no. 02640-60086 to replace part no. 02640-60013.

Table 4-1. Terminal Replaceable Parts List (Sheet 3 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
56	02640-00054	• CRT Shield	1
		(Attaching Parts)	
57	0510-0554	• Snap Fastener	2
		– – – X – – –	
58	02640-40022	• Right Side	1
		(Attaching Parts)	
59	2360-0121	• Screw, Machine, ph, no. 6-32, 3/8 in.	3
60	2190-0918	• Washer, Lock, split, no. 6	3
61	3050-0066	• Washer, Flat, No. 6	3
		– – – X – – –	
62	02640-40023	• Left Side	1
		(Attaching Parts)	
	2360-0121	• Screw, Machine, ph, no. 6-32, 3/8 in.	3
	2190-0918	• Washer, Lock, split, no. 6	3
	3050-0066	• Washer, Flat, no. 6	3
		– – – X – – –	
63	*02640-60095	• Sweep Assembly	1
	02640-60039	• Sweep Cable Assembly (not shown)	1
64	02640-60042	• CRT Cable Assembly	1
65	** 3160-0208	• Fan (used for Accessory 13240A)	1
66	02640-60138	• Fan, Cable Assembly (used for Accessory 13240A)	1
		(Attaching Parts)	
67	3030-0064	• Screw, Cap, no. 6-32, 5/8 in.	4
68	2190-0918	• Washer, Lock, split, no. 6	4
69	2360-0205	Screw, Machine, ph, no. 6-32, 3/4 in.	2
70	2420-0003	Nut, Plain, no. 6	2
71	1400-0440	Cable Clamp (used for Accessory 13240A)	2
		– – – X – – –	
72	***02640-60084	• CRT Yoke Assembly	1
		(Attaching Parts)	
73	2510-0107	• Screw, Machine, ph, no. 8-32, 1/2 in.	4
74	2190-0017	• Washer, Spring, no. 8	4
75	3050-0001	• Washer, Flat, no. 8	4
76	–	Static ground wire (P/O item 64)	–
77	2190-0010	• Washer, Lock, ext-tooth, no. 8	1
78	02640-00055	• Support Retainer	1
	02640-60030	• Keyboard and Cable Assembly	1
	02640-60068	• Limited Keyboard and Cable Assembly (used for Option 010)	1
79	****02640-60081	•• Keyboard Cable Assembly	1
		(Attaching Parts)	
80	2360-0201	•• Screw, Machine, ph, no. 6-32, 1/2 in.	1
81	2190-0918	•• Washer, Lock, split, no. 6	1
82	3050-0066	•• Washer, Flat, no. 6	1
83	1400-0440	•• Cable Clamp	1
		– – – X – – –	
84	02640-00004	•• Keyboard Overlay	1
	02640-00022	•• Limited Keyboard Overlay (used for Option 010)	1

NOTE: *Order part no. 02640-60095 to replace part no. 02640-60020.

**Fan (part no. 3160-0208) and cable (part no. 02640-60138) replace fan and cable assembly (part no. 02640-60037).

***Order part no. 02640-60084 to replace either part no. 2090-0028 or 02640-60040.

****Order part no. 02640-60081 to replace part no. 02640-60038.

Table 4-1. Terminal Replaceable Parts List (Sheet 4 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
85	7120-4403	•• Baud Rate Overlay	1
86	02640-40008	•• Keyboard Top	1
	02640-40021	•• Limited Keyboard Top (used with option 010)	1
		(Attaching Parts)	
87	2360-0203	•• Screw, Machine, ph, no. 6-32, 5/8 in.	5
88	2190-0918	•• Washer, Lock, split, no. 6	5
89	3050-0066	•• Washer, Flat, no. 6	5
		– – – X – – –	
90	02640-60018	•• Keyboard Assembly	1
	02640-60069	•• Keyboard Assembly (used for Option 010)	1
91	1990-0486	••• Light Emitting Diode	5
	0370-1129	••• BAUD RATE Knob	1
	0370-2646	••• ESC Keycap	1
	0370-2260	••• 1 ! Keycap	1
	0370-2261	••• 2 " Keycap	1
	0370-2262	••• 3 # Keycap	1
	0370-2263	••• 4 $ Keycap	1
	0370-2264	••• 5 % Keycap	1
	0370-2265	••• 6 & Keycap	1
	0370-2266	••• 7 ' Keycap	1
	0370-2267	••• 8 (Keycap	1
	0370-2268	••• 9) Keycap	1
	0370-2641	••• 0 Keycap	1
	0370-2648	••• – = Keycap	1
	0370-2654	••• Λ ~ Keycap	1
	0370-2651	••• \ ¦ Keycap	1
	0370-2649	••• LINE FEED Keycap	1
	0370-2637	••• CNTL Keycap	1
	0370-2286	••• Q Keycap	1
	0370-2292	••• W Keycap	1
	0370-2274	••• E Keycap	1
	0370-2287	••• R Keycap	1
	0370-2289	••• T Keycap	1
	0370-2294	••• Y Keycap	1
	0370-2290	••• U Keycap	1
	0370-2278	••• I Keycap	1
	0370-2284	••• O Keycap	1
	0370-2285	••• P Keycap	1
	0370-2655	••• @ ` Keycap	1
	0370-2653	••• [{ Keycap	1
	0370-2650	••• _ DEL Keycap	1
	0370-2647	••• LOCK Keycap	1
	0370-2270	••• A Keycap	1
	0370-2288	••• S Keycap	1
	0370-2273	••• D Keycap	1
	0370-2275	••• F Keycap	1
	0370-2276	••• G Keycap	1
	0370-2277	••• H Keycap	1

Table 4-1. Terminal Replaceable Parts List (Sheet 5 of 6)

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
	0370-2279	··· J Keycap	1
	0370-2280	··· K Keycap	1
	0370-2281	··· L Keycap	1
	0370-2324	··· ; + Keycap	1
	0370-2325	··· : * Keycap	1
	0370-2652	···] } Keycap	1
	0370-2635	··· RETURN Keycap	1
	0370-2636	··· SHIFT Keycap	2
	0370-2295	··· Z Keycap	1
	0370-2293	··· X Keycap	1
	0370-2272	··· C Keycap	1
	0370-2291	··· V Keycap	1
	0370-2271	··· B Keycap	1
	0370-2283	··· N Keycap	1
	0370-2282	··· M Keycap	1
	0370-2296	··· , < Keycap	1
	0370-2297	··· . > Keycap	1
	0370-2298	··· / ? Keycap	1
	02640-00019	··· Space Bar Keycap	1
	0370-0620	··· 0 Keycap (Numeric Pad)	1
	0370-2312	··· 1 Keycap	1
	0370-2313	··· 2 Keycap	1
	0370-2314	··· 3 Keycap	1
	0370-2315	··· 4 Keycap	1
	0370-2316	··· 5 Keycap	1
	0370-2317	··· 6 Keycap	1
	0370-2318	··· 7 Keycap	1
	0370-2319	··· 8 Keycap	1
	0370-2320	··· 9 Keycap	1
	0370-2322	··· . Keycap (Numeric Pad)	1
	0370-2656	··· CLEAR TAB Keycap	1
	0370-2657	··· SET TAB Keycap	1
	0370-2643	··· CLEAR DSPLY Keycap	1
	0370-2658	··· ROLL UP Keycap	1
	0370-2659	··· ROLL DOWN Keycap	1
	0370-2638	··· NEXT PAGE Keycap	1
	0370-2639	··· PREV PAGE Keycap	1
	0370-2642	··· ↖ (Home) Keycap	1
	0370-2640	··· Arrow Keycap	1
	0370-2644	··· Operating Function Keycap	18
	0370-2765	··· f_1 Keycap	1
	0370-2766	··· f_2 Keycap	1
	0370-2767	··· f_3 Keycap	1
	0370-2768	··· f_4 Keycap	1
	0370-2769	··· f_5 Keycap	1
	0370-2770	··· f_6 Keycap	1
	0370-2771	··· f_7 Keycap	1

Table 4-1. Terminal Replaceable Parts List (Sheet 6 of 6)

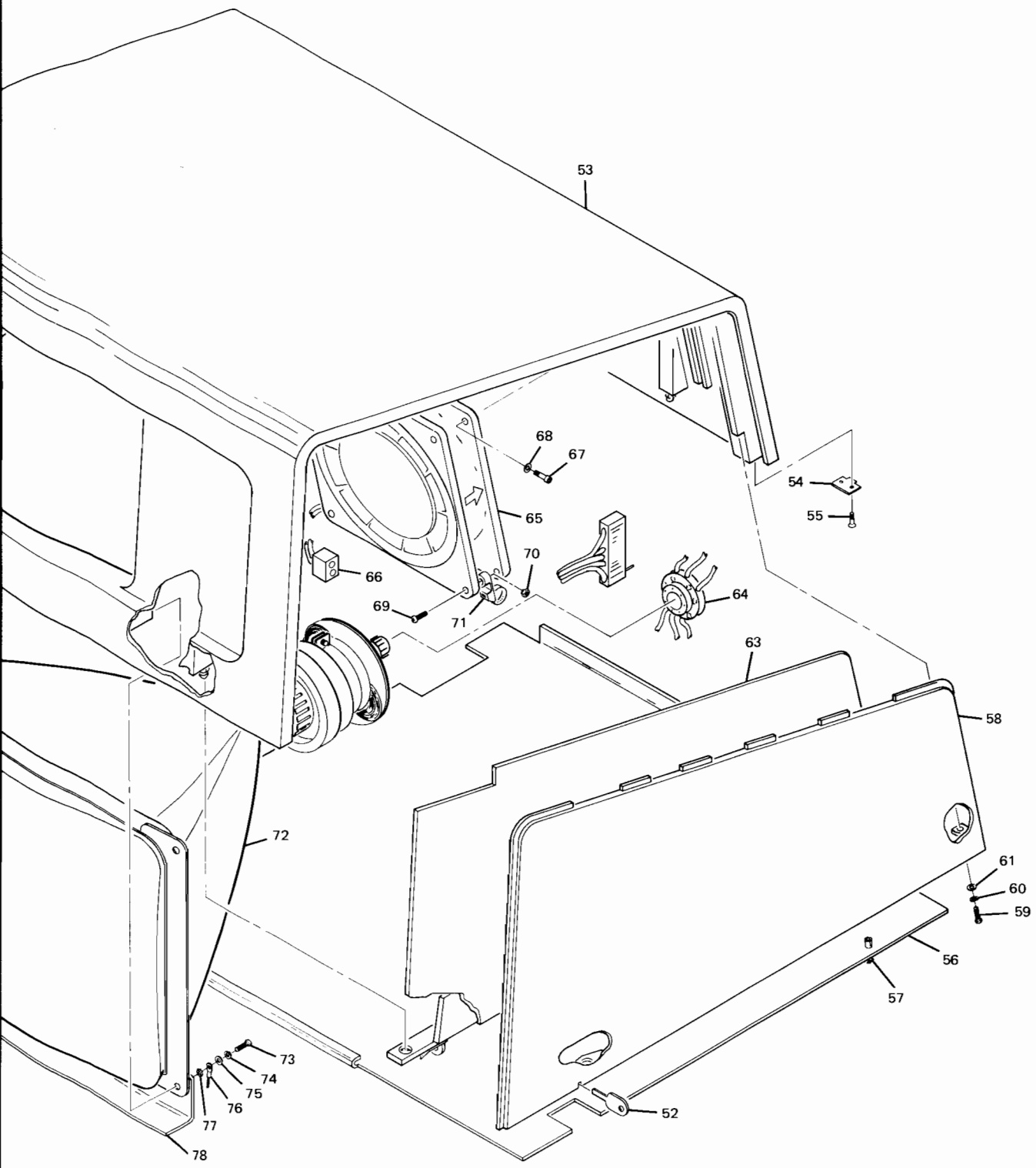
FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
	0370-2772	••• f_8 Keycap	1
92	9160-0233	•• Loudspeaker Assembly	1
		(Attaching Parts)	
–	02640-60041	•• Speaker Cable Assembly	1
93	2360-0193	•• Screw, Machine, ph, no. 6-32, 1/4 in.	2
94	2190-0918	•• Washer, Lock, split, no. 6	2
95	1400-0054	•• Mounting Clamp	2
		– – – X – – –	
96	0403-0324	•• Rubber Bumper	4
97	02640-40007	•• Keyboard Bottom	1
	5040-7433	•• Keycap Removal Tool (not shown)	1
	9866A	Printer (not shown) Used for Accessory 13246A and Option 012	1

Table 4-2. PROM Character PCA Replaceable Parts List

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 2	0180-0393	C:Fxd Ta 39 μF ±10%, 10 VDCW	56289	150D396X9010B2-DYS
C3 thru C16	0160-2055	C:Fxd Cer 0.01 μF +80 −20%, 100 VDCW	56289	C023F101F103ZS22-CDH
R1, 2	1810-0121	R:Fxd network 8 x 1K ohms 5%	56289	200C-1855-CRR
R3, 4	0683-4725	R:Fxd 4.7K ohms 5% 1/4W	01121	CB4725
U6, 16	1820-1245	IC:TTL 2-Bit decoder	01245	SN74LS155N
U7, 9	1820-1208	IC:TTL Quad 2-input OR gate	01245	SN74LS32N
U8	1820-1244	IC:TTL 4-Bit encoder	01245	SN74LS153N
U10, 17, 19	1820-1246	IC:TTL Quad 2-input AND gate, open collector	01245	SN74LS09N
U18	1820-1144	IC:TTL Quad 2-input NOR gate	01245	SN74LS02N
XU1 thru XU5, XU11 thru XU15	1200-0541	Socket, IC, 24-pin	09922	DILB24P-1

Table 4-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS ADDRESS
01121	Allen Bradley Co.	Milwaukee, Wisc.
01245	Texas Instruments, Inc., Component Group	Dallas, Texas
09922	Burndy Corp.	Norwalk, Conn.
56289	Sprague Electric Co.	North Adams, Mass.



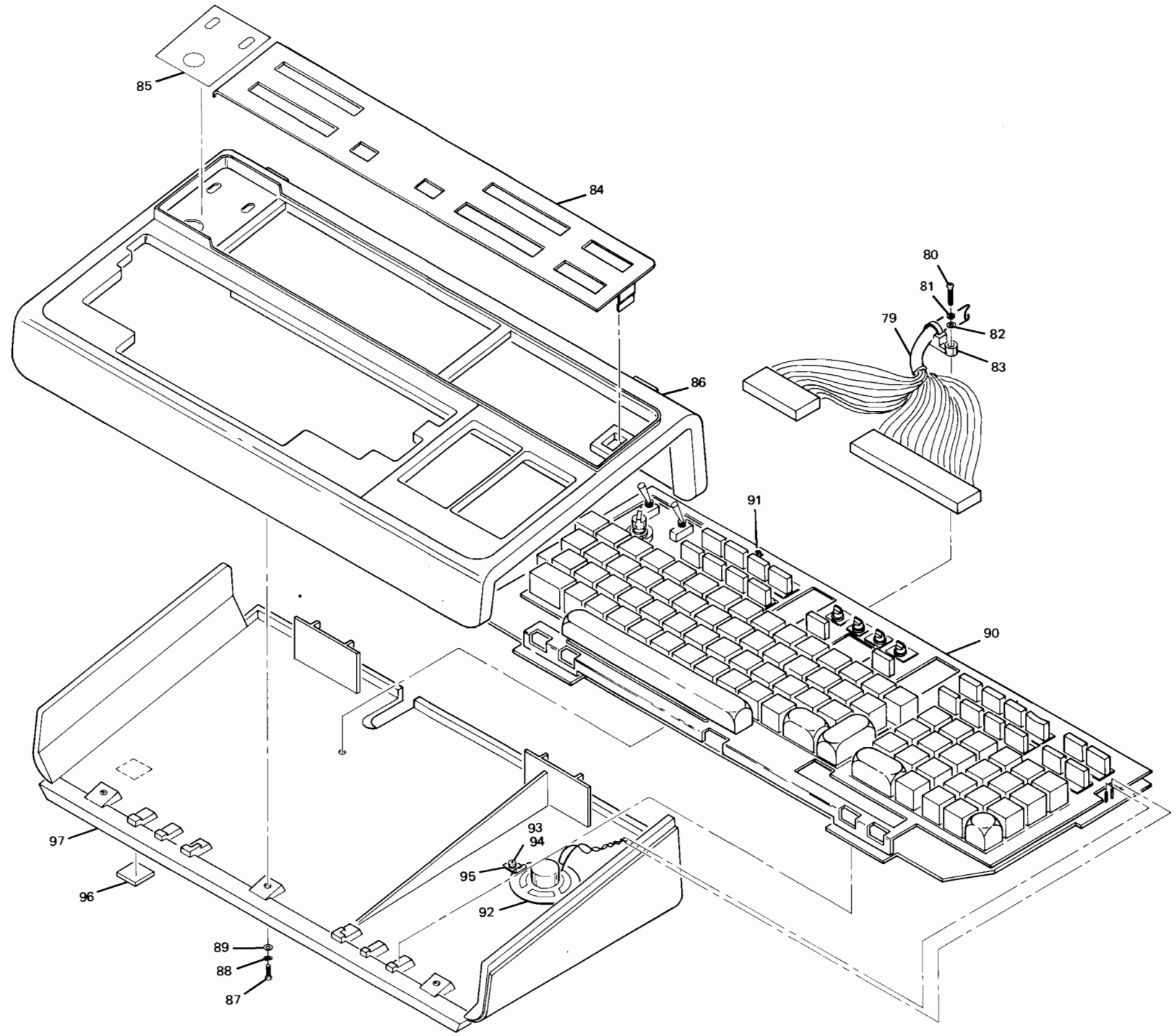
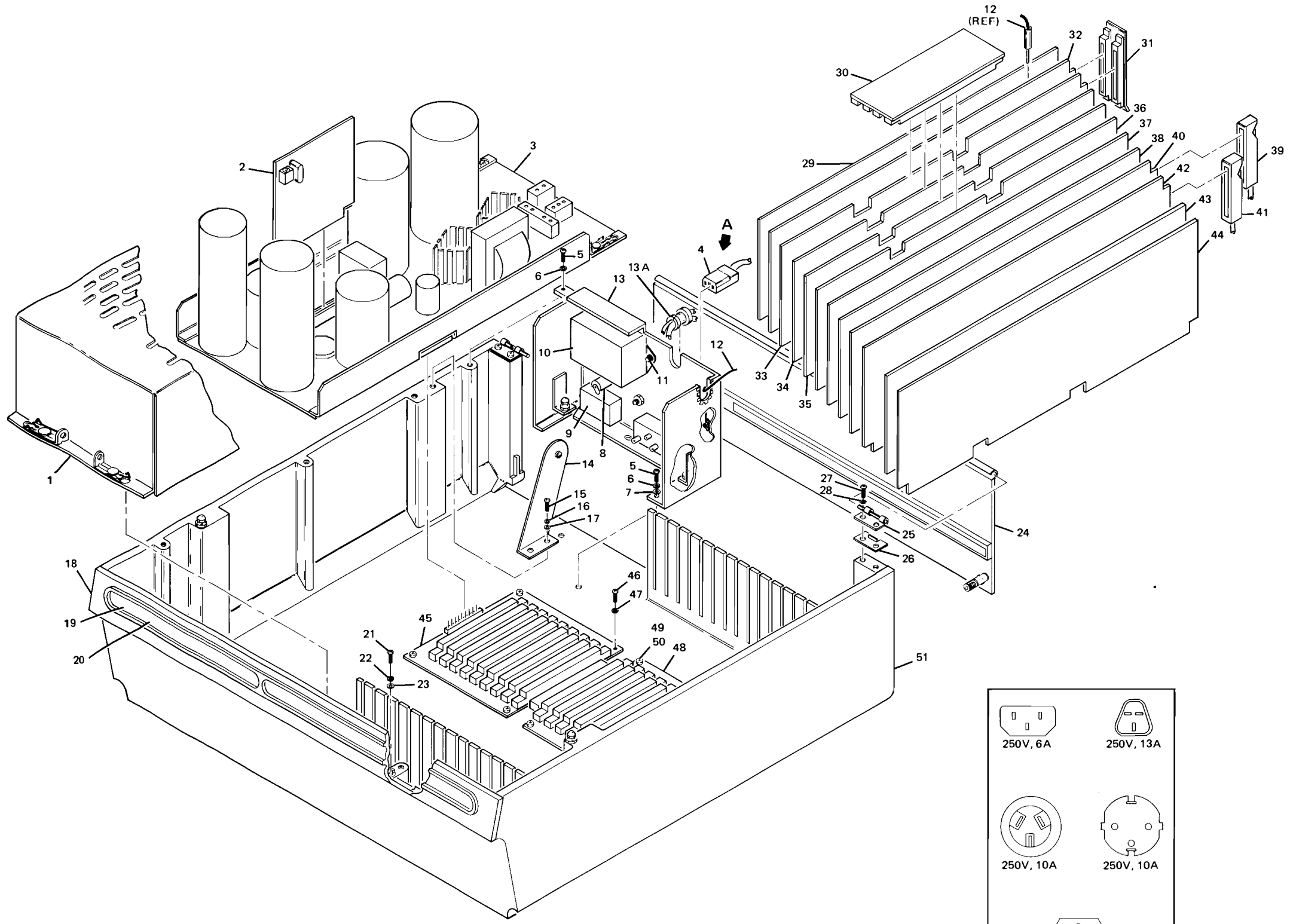


Figure 4-1. HP 2640A Terminal Exploded View


12 (REF)
30
32
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A
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13
13 A
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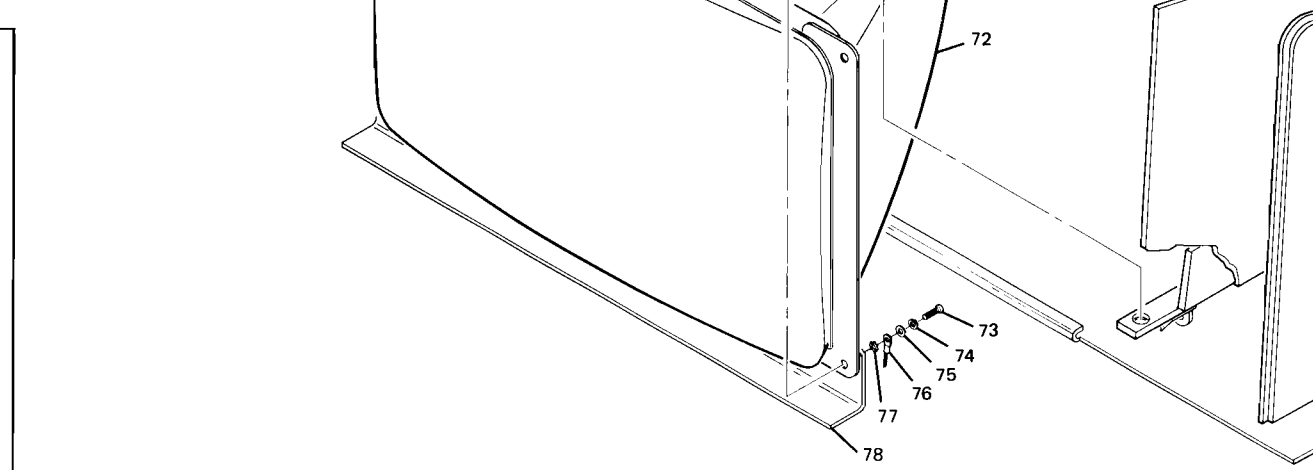
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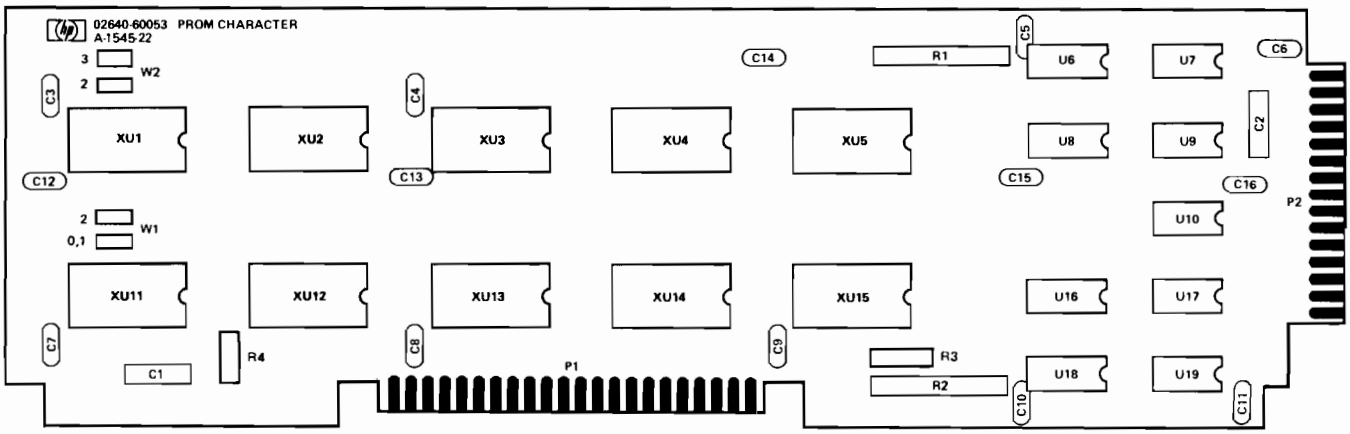
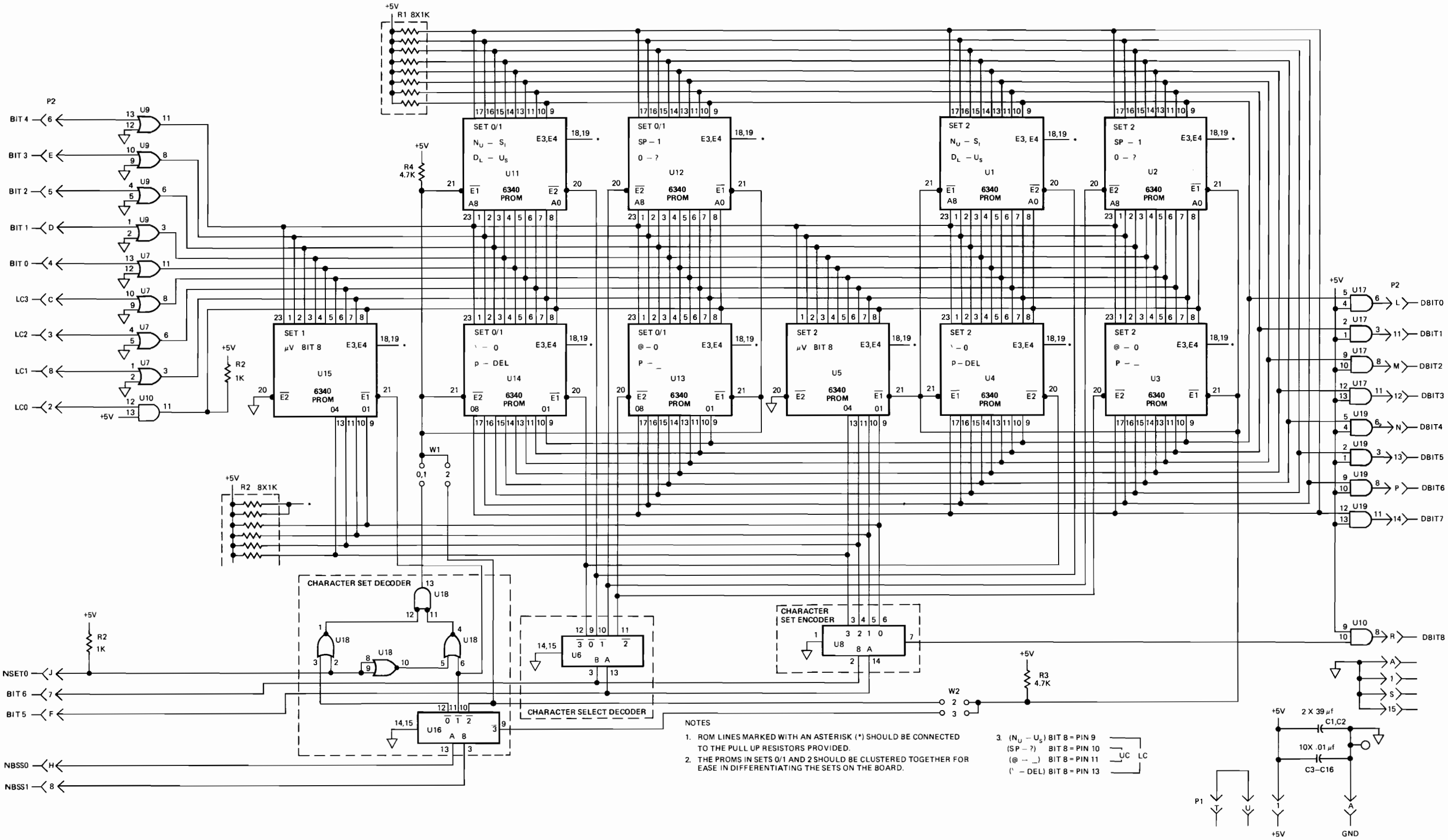
250V, 6A
250V, 13A
250V, 10A
250V, 10A
250V, 6A
A


02640-60053 PROM CHARACTER
A-1545-22
3
2
W2
2
W1
0,1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
R1
R2
R3
R4
P1
P2
XU1
XU2
XU3
XU4
XU5
XU11
XU12
XU13
XU14
XU15
U6
U7
U8
U9
U10
U16
U17
U18
U19

7077 19



NOTES

1. ROM LINES MARKED WITH AN ASTERISK (*) SHOULD BE CONNECTED TO THE PULL UP RESISTORS PROVIDED.
2. THE PROMS IN SETS 0/1 AND 2 SHOULD BE CLUSTERED TOGETHER FOR EASE IN DIFFERENTIATING THE SETS ON THE BOARD.
3. ($N_U - U_S$) BIT 8 = PIN 9
   (SP – ?) BIT 8 = PIN 10
   (@ – _) BIT 8 = PIN 11
   (\ – DEL) BIT 8 = PIN 13
   — UC LC

Figure 4-2. PROM Character PCA, Schematic Diagram

7077-25A