ABSOLUTE BINARY PROGRAM NO. 24395-16002

21MX MICROCODED MEMORY DIAGNOSTIC

reference manual

HEWLETT PACKARD

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, 95014

MANUAL PART NO. 24395-90003
MICROFICHE PART NO. 24395-90004

Printed: JAN 1977
Printed in U.S.A.

LIST OF EFFECTIVE PAGES

Changed pages are identified by a change number adjacent to the page number. Changed information is indicated by a vertical line in the outer margin of the page. Original pages do not include a change number and are indicated as change number 0 on this page. Insert latest changed pages and destroy superseded pages.

Change 0 (Original) . . . . . JAN 1977

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SECTION I
INTRODUCTION

1-1. GENERAL

The HP 21MX Microcoded Semiconductor Memory Diagnostic is designed to test HP 21MX E-Series and M-Series Computer memory modules that use 4096 bit RAM Integrated Circuits. Since much of this diagnostic is executed in microcode, a Writable Control Store (WCS) board is required. The microcoded tests are designed to be used where the execution time of the software semiconductor memory diagnostic, part no. 24395-16001 (DSN 102104), would be prohibitive.

For the case of a 21MX computer with at least 8K of memory, a standard operating procedure is given in Section II. More specific information pertaining to the operation of the diagnostic and additional operating features is given in sections III and IV.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. HP 21MX E- or M-Series Computer with a minimum of 4K memory.

b. A loading device for the media on which the diagnostic is distributed.

c. HP 13197A 1K WCS or HP 12978A 256 Word WCS. (The HP 12978A is compatible only with the 21MX M-Series Computer.)

The following hardware is optional:

a. HP 12892A/B Memory Protect

b. HP 12976A Dynamic Mapping System for 21MX M-Series computer (memory protect is included)

c. HP 13305A Dynamic Mapping System for 21MX E-Series computer (memory protect is included)

d. A console for message reporting is recommended.

1-3. REQUIRED SOFTWARE

The following software is required:

Microcoded Semiconductor Memory Diagnostic	Absolute Binary Program No. 24395-16002
Diagnostic Configurator	Absolute Binary Program No. 24296-60001.

The Microcoded Semiconductor Memory Diagnostic described in this manual is available on one or more media (e.g., paper tape, mini-cartridge tape, discs, or magnetic tape). For corresponding part numbers associated with these media, refer to appendix A in the Diagnostic Configurator Reference Manual, part no. 02100-90157, dated January 1977 or later.

1-4. DIAGNOSTIC SERIAL NUMBER

The Diagnostic Serial Number (DSN) of this diagnostic resides in memory location 126 (octal). The DSN is 102006 (octal).

OPERATING PROCEDURE

SECTION II

This section of the manual provides a standard operating procedure for a 21MX computer with at least 8K of memory. For information on program organization and additional program features, or procedures to run the diagnostic on a computer with 4K of memory, refer to the appropriate paragraphs in sections III and IV. A complete operating procedure flowchart is provided in figure 2-2.

2-1. HARDWARE CONFIGURATION

2-2. MEMORY PROTECT

If Memory Protect is installed in the computer under test, Parity Error/Memory Protect switch A1S1 on the CPU board should be in the INT/IGNORE position. If Memory Protect is not installed, Parity Error/Memory Protect switch A1S1 should be in the HALT position. (When viewed from the rear of the computer, the left hand position is the INT/IGNORE position, and the right hand position is the HALT position.)

2-3. WCS CONFIGURATION

An HP 13197A or 12978A WCS board must be installed in one of the I/O slots in the rear of the computer with the WCS cable connected. If the 12978A WCS is used, it must be configured to control store module 12 (octal) by installing jumpers as shown in figure 2-1. No additional configuration is necessary for the HP 13197A WCS.

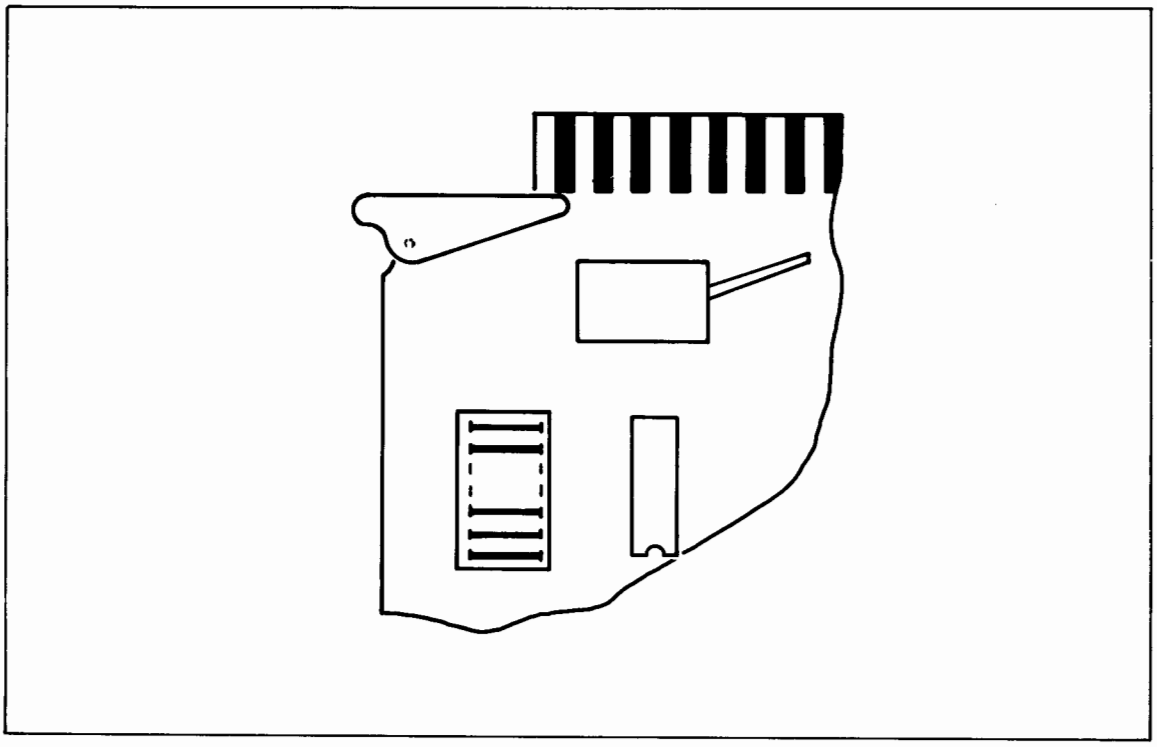


Figure 2-1. HP 12978A WCS Configuration

2-4. STANDARD OPERATING PROCEDURE

The following standard operating procedure assumes a 21MX computer with at least 8K of memory. A complete operating procedure flowchart of the diagnostic is given in figure 2-2. A console device is highly recommended. Paragraph 2-9 describes special procedures if Memory Protect is not installed. Paragraph 3-4 describes the operating procedure if only 4K of memory is installed in the computer. To run the Microcoded Semiconductor Memory Diagnostic, proceed as follows:

1. Configure hardware as described above.

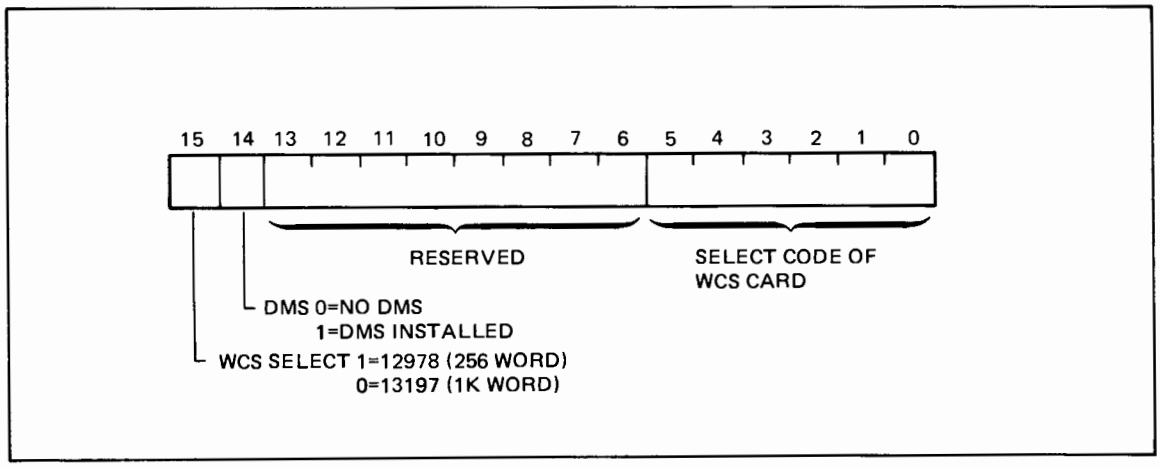
2. Load and configurator Configurator. (Refer to the Diagnostic Configurator Reference Manual, part no. 02100-90157.)

3. Load the diagnostic with the configurator binary loader.

4. Either a Halt 102077 or 102073 will result. (The Halt 102073 occurs if automatic configuration was specified.)

5. Set S-register as shown in table 2-1. Press STORE.

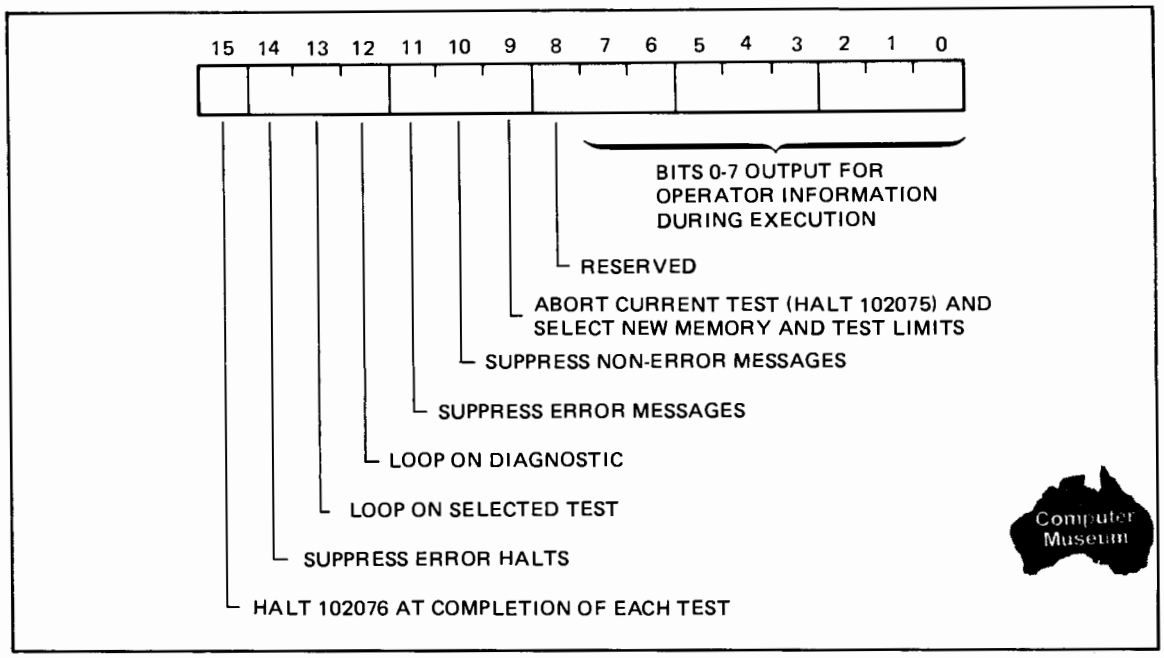
Table 2-1. S-Register Configuration Information



6. Press PRESET, RUN; should get HALT 102074.

7. S-register bits may be set to select program options as shown in table 2-2. Press STORE. For standard operation (i.e., one execution of the diagnostic), the S-register should be clear.

Table 2-2. S-Register Program Options



8. Press PRESET, RUN. Execution should proceed as follows:

   a. The message "MICROCODED SEMICONDUCTOR MEMORY DIAGNOSTIC" will be displayed on the console, if present.

   b. Bits 0-7 of the S-register will display the current 4K module under test. The S-register, starting at 001, will count up through the number of 4K modules present in the computer as the diagnostic executes a preliminary check on memory.

NOTE

Throughout this manual, memory locations will be referred to by "4K module number;" memory should be thought of as being divided into 4K blocks (modules). Therefore, a 16K array board contains four 4K modules, an 8K array board contains two 4K modules.

   c. The S-register bits 0-7 will start at 001 and count up again, only much more slowly, during the execution of the major part of the diagnostic. This will be repeated four times. Refer to table 4-2 for approximate execution times.

   d. S-register bits 0-7 will then be cleared while the diagnostic tests Module 0. Refer to table 4-2 for approximate execution times.

9. If HALT 102077 occurs, the diagnostic passes. Press RUN to execute another pass. Refer to table 4-2 for approximate execution time. At the end of each pass, the message "H077 PASS NNNNN," where NNNNN is the pass number, will be output to the console.

10. If a HALT other than 102077 occurs, refer to table 4-1. If Memory Protect is not installed, the special procedures described in paragraph 2-10 must be used to determine where the failure occurred.

2-5. RESTARTING

The program may be restarted by setting the P-register to 2000 and proceeding with step 7 of the standard operating procedure (paragraph 2-2).

NOTE

If Test 05 was in progress when the diagnostic was halted, set the P-register to 10000 (octal) in order to relocate the program back to module 0. Test 05 was in execution if S-Register bits 0-7 are clear following the halt.

The program may be reconfigured (change WCS select code, DMS, or WCS type) by setting the P-register to 100, and proceeding with step 5 of the standard operating procedure (paragraph 2-2).

2-6. OPERATOR COMMUNICATION

2-7. CONSOLE MESSAGES

If a console is available and was configured by the Configurator, messages can be output to the console. S-Register bits 10 and 11 control the suppression of these messages. The messages output will be the title message, pass count and data error messages. The title message is output once when the diagnostic begins execution. The pass count message "H077 PASS NNNNN," where NNNNN is the pass count, is output at the end of each pass.

The following is an example of an error message:

E013 GAL.READ	SOFT ERROR
ACTUAL DATA (READ)	VVVVVV
EXPECTED DATA (WRITTEN)	WWWWWW
ADDR OF DATA FAILURE	YYY XXXX
TEST CELL ADDR	YYY XXXX

where:

E013 indicates a Halt 102013 or Halt 106013 (1060xx for soft error)

GAL.READ is the routine in which the error occurred

SOFT ERROR is only output if data could be restored (refer to paragraph 3-3)

XXXX is the address within the 4K module

YYY is the 4K module in which the error occurred

TEST CELL ADDR is the test cell address (only applies in Galloping Read Recovery); this is useful in determining if a background or foreground location failed (refer to paragraph 4-3).

2-8. MANUAL ERROR REPORTING

If a console is not available, all communications with the operator must be via halt codes and hardware registers.

When a Data Error Halt occurs (refer to table 4-1) the registers contain the following values:

T-Register = 1020XX (or 1060XX for soft error) where

A-Register = Actual data (read)
B-Register = Expected data (written)
X-Register = 4K module in which error occurred
Y-Register = Test Cell 4K module number (only applies to Galloping Read Recovery; refer to paragraph 4-3).

See appendix A for special procedures to display X- and Y-registers on the M-Series computer.

2-9. SPECIAL PROCEDURE FOR HANDLING PARITY ERRORS IF MEMORY PROTECT IS NOT INSTALLED

If Memory Protect is not installed, the following special procedures must be used to determine the location of the error:

1. Compare the M- and X-registers. (On an M-Series computer it will be necessary to write down the value of the M-register, as it is used to display the X-register.) See Appendix A for procedure to display the X-register on the M-Series computer.

2. If the M- and X-registers are equal, the A-register contains the actual data (read), and the B-register contains the expected data (written). If the A- and B-registers are equal, the parity bit has failed. Otherwise, the failing bit can be easily observed by comparing the A- and B-registers.

3. If the M- and X-registers are not equal, the parity error occurred in the program area.

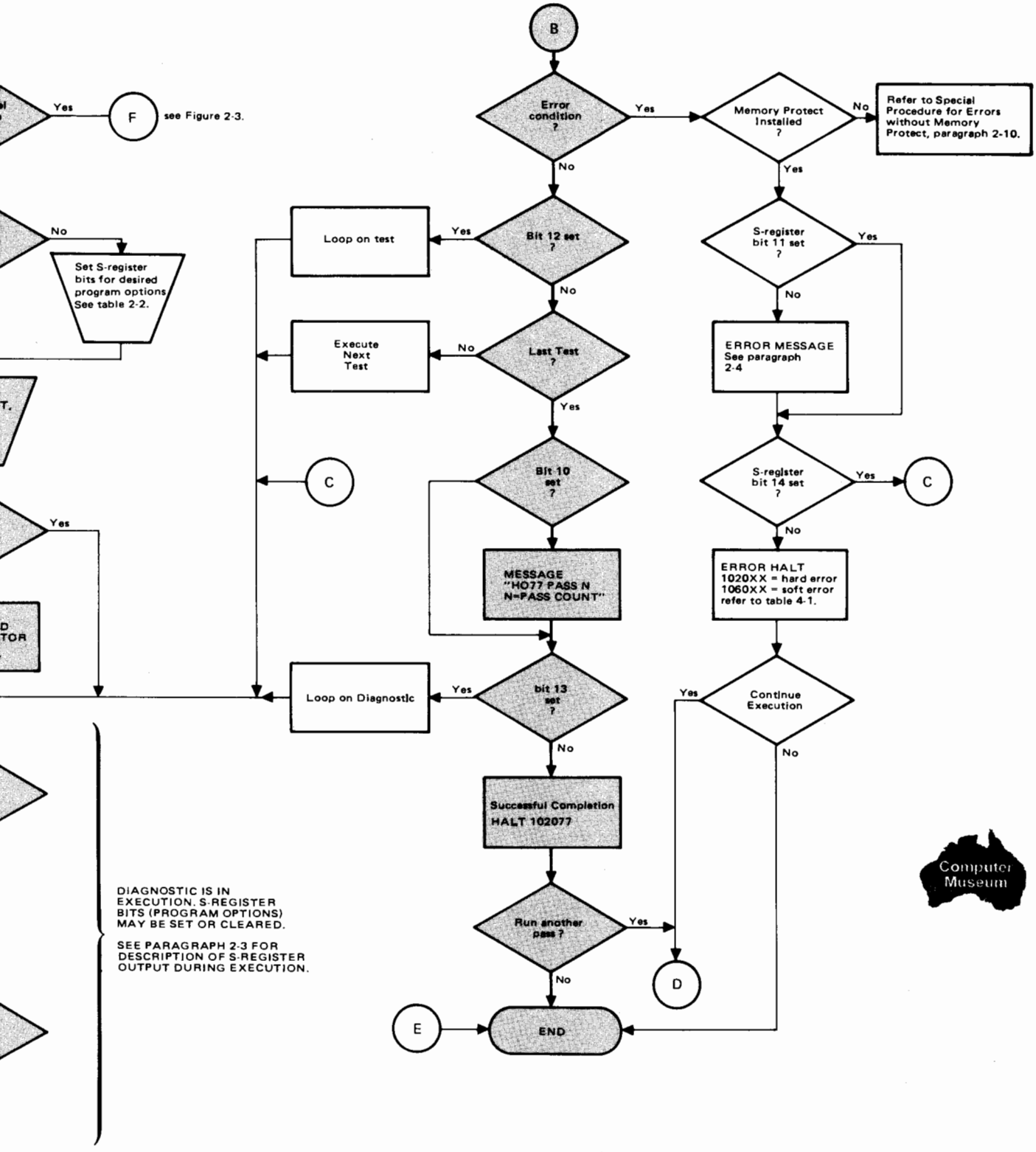
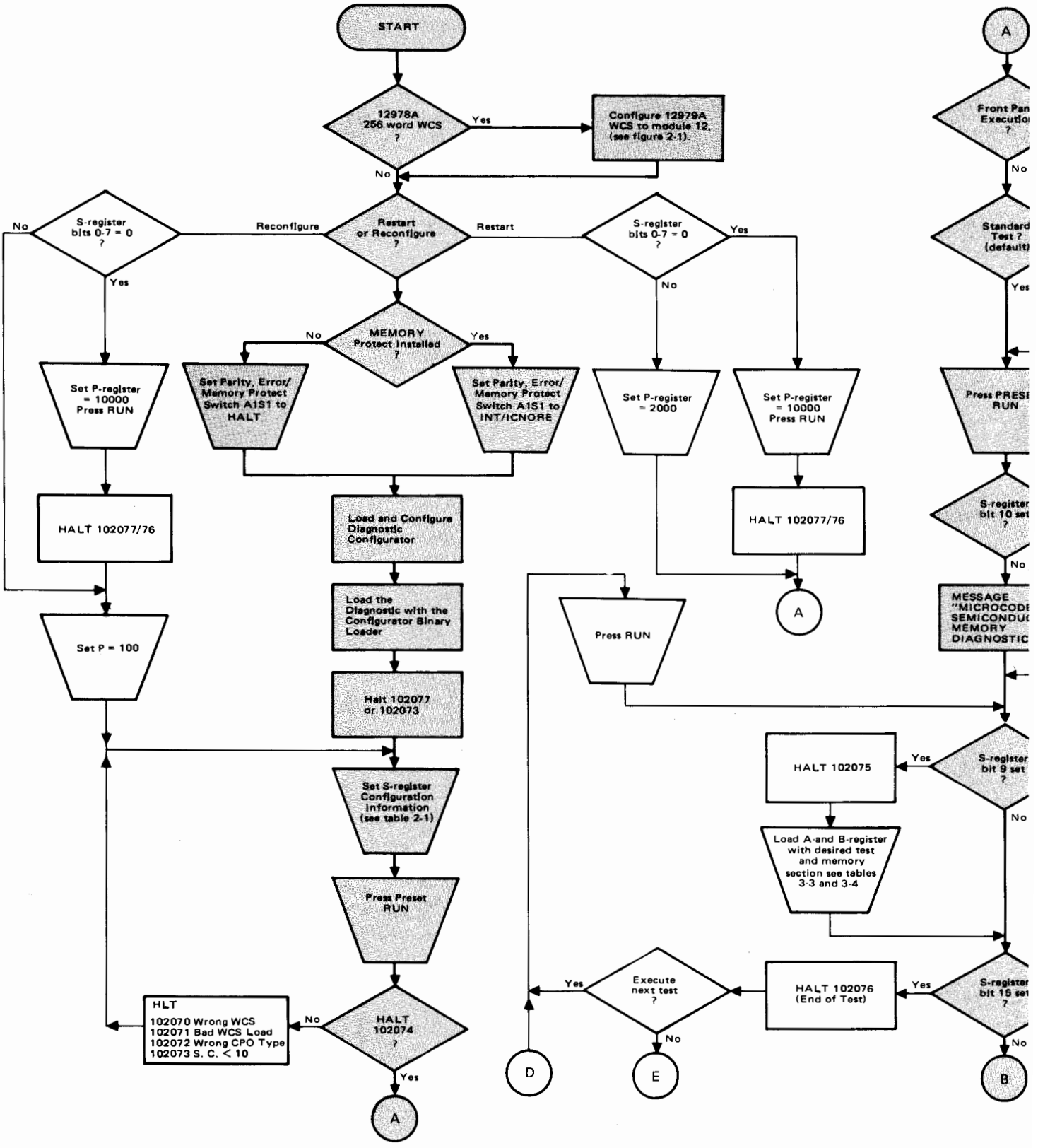


Figure 2-2. Operating Procedure Flowchart


START
12978A 256 word WCS ?
Yes
Configure 12979A WCS to module 12, (see figure 2-1).
No
S-register bits 0-7 = 0 ?
No
Yes
Reconfigure
Restart or Reconfigure ?
Restart
S-register bits 0-7 = 0 ?
Yes
No
MEMORY Protect Installed ?
No
Yes
Set P-register = 10000 Press RUN
Set Parity, Error/ Memory Protect Switch A1S1 to HALT
Set Parity, Error/ Memory Protect Switch A1S1 to INT/ICNORE
Set P-register = 2000
Set P-register = 10000 Press RUN
HALT 102077/76
Load and Configure Diagnostic Configurator
Load the Diagnostic with the Configurator Binary Loader
Halt 102077 or 102073
Set P = 100
Set S-register Configuration Information (see table 2-1)
Press Preset RUN
HALT 102074 ?
No
Yes
HLT
102070 Wrong WCS
102071 Bad WCS Load
102072 Wrong CPO Type
102073 S. C. < 10
A
Press RUN
A
D
Execute next test ?
Yes
No
E
HALT 102076 (End of Test)
Yes
HALT 102075
Yes
No
Load A-and B-register with desired test and memory section see tables 3-3 and 3-4
B
A
No
Yes
No
MESSAGE "MICROCODE SEMICONDUC MEMORY DIAGNOSTIC

24395-1A

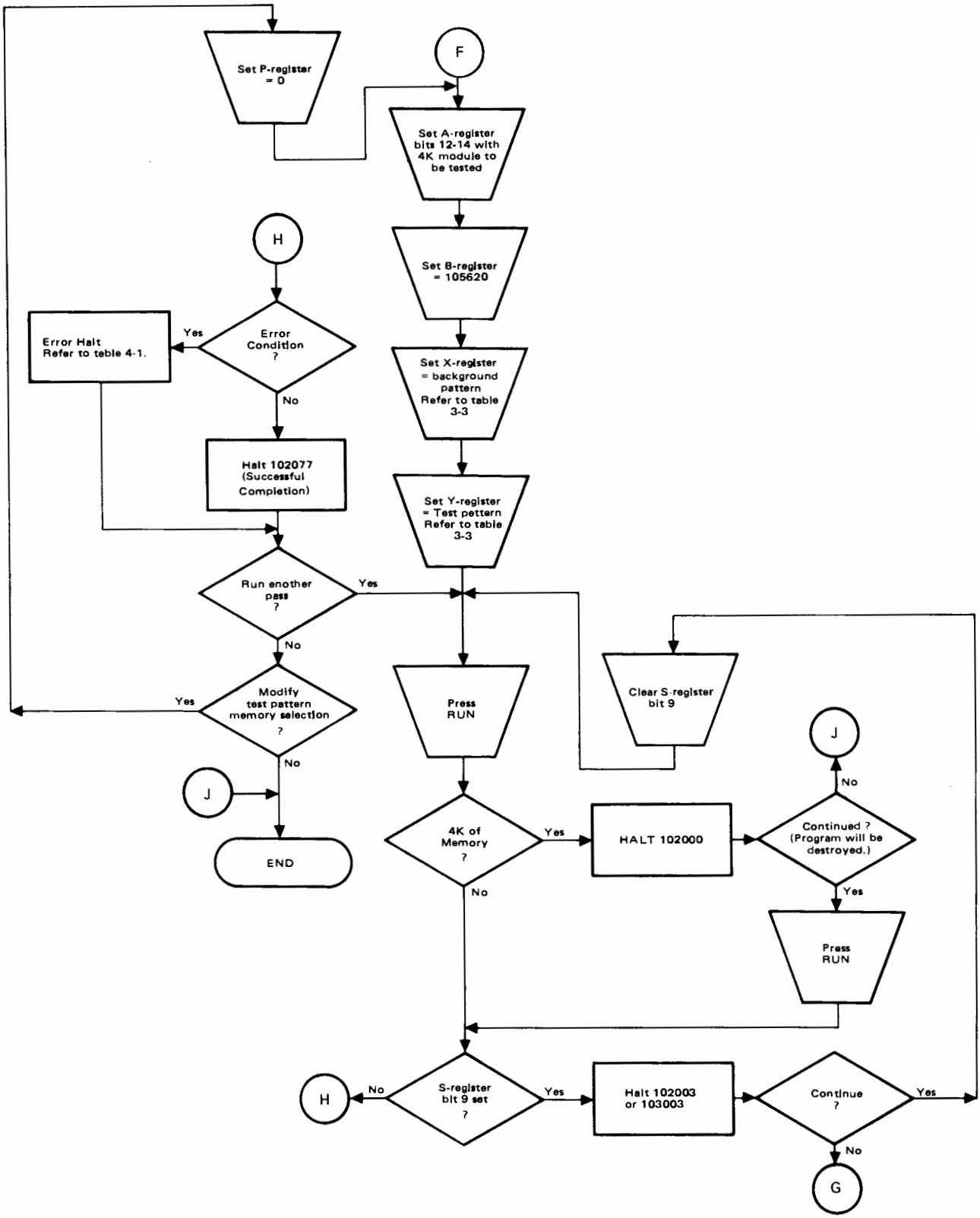


Figure 2-3. Front Panel Execution Operating Procedure Flowchart

24395-2A

ADDITIONAL PROGRAM FEATURES

SECTION III

3-1. PROGRAM ORGANIZATION

The diagnostic contains an initialization section, a control section and 6 tests. The initialization section loads the microcoded routines into WCS. The microcode used depends on the type of computer being tested (M-Series or E-Series); this is determined by the Configurator. The control section executes the selected tests and sets up DMS if that option is selected. Then the actual tests are executed.

The initialization section uses the select code and type of WCS board, specified by the operator, to configure a driver routine for WCS. It then loads the microcode for the appropriate computer from memory into WCS and verifies that the WCS was loaded correctly.

The control section executes the selected tests and, if specified by the operator, will loop or halt after each test, loop on all selected tests, or suppress error halts.

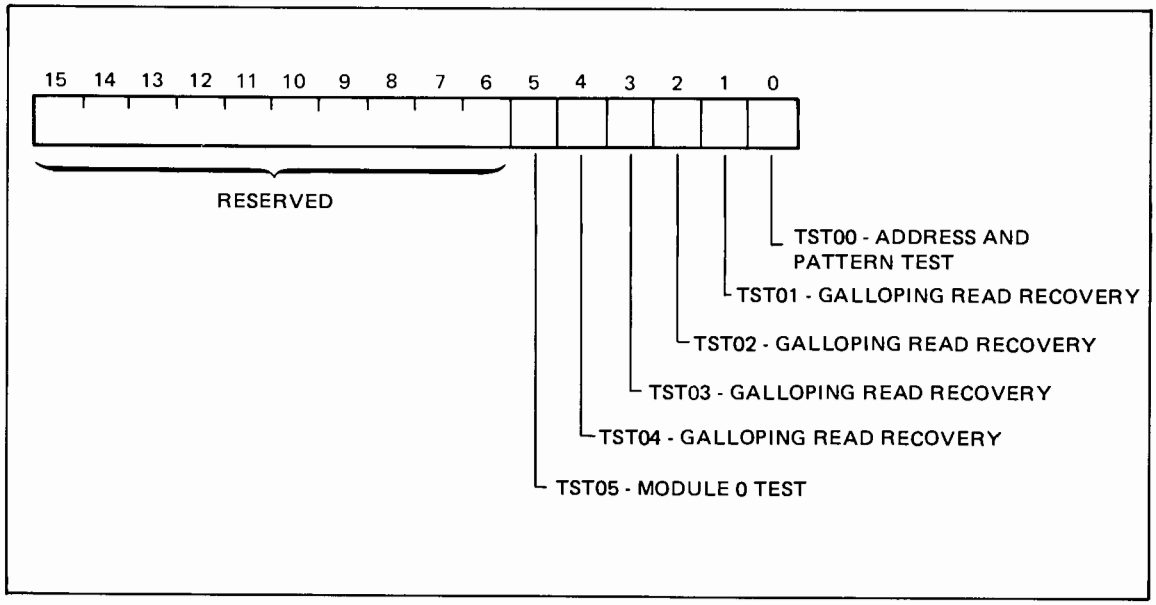
3-2. TEST AND MEMORY MODULE SELECTION

The control portion of the program allows the operator to select a test or sequence of tests to be run and the memory module(s) to be tested. To select a particular sequence of tests, or a particular area of memory to be tested, perform the following:

1. Set S-register bit 9, either after a halt 102074, or during execution of the diagnostic. If the diagnostic is in execution, the current test will be aborted and the program will halt 102075.

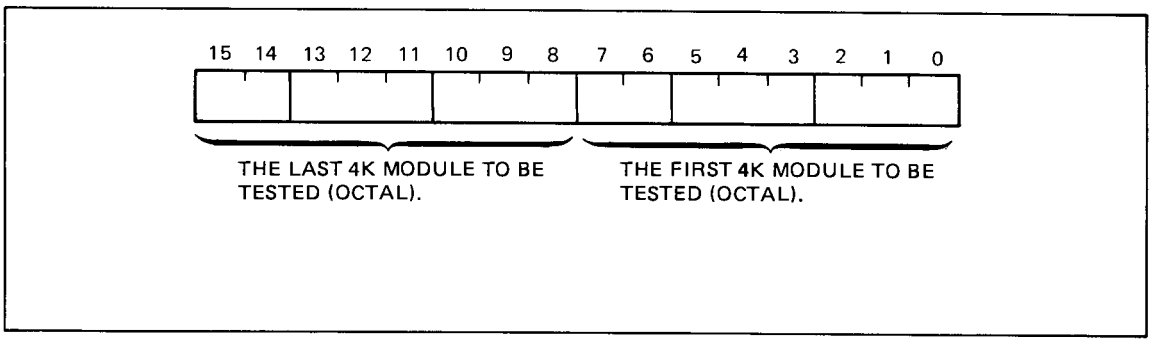
2. Refer to table 3-1 and set appropriate A-register bits to select desired tests.

Table 3-1. A-Register Test Selection



3. Refer to table 3-2 and set appropriate B-Register bits to select memory modules to be tested.

Table 3-2. B-Register Memory Module Test Selection



4. Press PRESET, RUN.

Defaults are as follows:

If the A-register is cleared, all tests are executed.

If the B-register is cleared, the entire memory is tested.

If only the first 4K module to be tested is specified, only that module will be tested.

When using this feature if the first module number is greater than the last module number, the program will continue to halt 102075 again until the entry is correct.

3-3. SOFT ERROR REPORTING CAPABILITY

The program has routines designed specifically to report soft errors. For any data error, an immediate attempt is made to restore the data. If the data is successfully restored, the error is reported as a soft error. On the console, this is accomplished through the message "SOFT ERROR." In the case of manual error reporting, a halt code of 1060XX corresponds directly to a code of 1020XX, but indicates the error, defined in table 4-1, is a soft error.

3-4. FRONT PANEL EXECUTION

Front panel execution capability has been provided to allow the operator to exercise the microcoded routines with the use of the registers available from the front panel. This procedure can be used to test any 4K base memory module. If only 4K of memory is available, this is the only procedure to test memory. If module 0 is tested (this is the only possibility for a computer with only 4K of memory) the diagnostic program will be destroyed.

The operator must load and configure the diagnostic in order to use this feature. The operation is as follows (refer to figure 2-3 for operating procedure flowchart):

1. Load and configure the diagnostic by performing steps 1-6 of the standard operating procedure described in paragraph 2-3. If the diagnostic has already been loaded and executed, just set the P-register to 2000.

2. Load the A-register bits 12-14 with the 4K module number to be tested. If Module 0 is specified, the program will be destroyed when it is executed.

3. Load the B-register with 105620 (octal). This is the macroinstruction to enter the microcode.

4. Load the X-register with the background pattern desired (refer to table 3-3). See Appendix A for special procedures to load X- and Y-registers on the M-Series computer.

Table 3-3. Galloping Read Test Patterns

TEST	BACKGROUND PATTERN	TEST PATTERN
TST01	125252	052525
TST02	052525	125252
TST03	000003	177776 (parity chip pattern)
TST04	177776	000003 (parity chip pattern)

5. Load the Y-register with the test pattern for Galloping Read Recovery Test desired (refer to table 3-3).

6. Press RUN. Do not press PRESET; this may disable WCS.

7. If only 4K of memory is installed in the computer, a Halt 102000 will occur. Press RUN to continue; the program will be destroyed.

8. A Halt 102077 indicates that the diagnostic passes. Refer to table 4-1 for other error halts.

During Front Panel Execution, the microcode can interrupted by setting bit 9 of the S-register. The program will come to a halt 103003 (this is a halt 102003 with bit 9 held high; if the T-register is selected after other registers have been examined, a halt 102003 will appear) with bit 15 set in the Y-register. To continue, clear S-register bit 9 and press RUN. (Do not press PRESET; this may disable WCS.)

After an error halt in Front Panel Execution, the X- and Y-registers contain the following information. (Note that addresses given are absolute addresses; not 4K module number.)

X-Register = Failing address

Y-Register = Test Cell address (only for Galloping Read Recovery)

When observing the X- and Y-registers during Galloping Read Recovery, if bit 15 is set in the X-register, the halt was caused by a data error; if bit 15 is set in the Y-register, the halt was caused by a parity bit error or the operator pressing HALT.

The A- and B-registers contain halt and re-entry information and must not be modified; to determine the nature of the error, one must examine the contents of the memory locations specified in the X- and Y-register. None of the above registers may be modified if re-entry to the microcode is desired.

To run another pass, press RUN. To modify 4K module number and test patterns, set the P-register to 0 and return to step 2.

3-5. DIAGNOSTIC LIMITATIONS

The program cannot detect if the memory modules are configured incorrectly (incorrect jumper settings on the memory board).

If only 4K is being tested the operator must use the optional Front Panel method described in section 3-4.

Memory locations 0-5 are never completely tested. To run a complete check, exchange Module 0 with another module of a higher order, by changing the appropriated jumpers on each board.

While loading the WCS board, the program checks if the correct WCS board was selected. However it can not verify that the WCS board is capable of exercising the loaded microcode correctly. If the flat cable to the WCS board is disconnected, the diagnostic will reach a halt 102077 after less than 2 seconds per 4K module.

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. GENERAL

The following paragraphs describe how the tests are used to diagnose memory. Each test (except TST05) is executed on the base memory in 4K increments, starting with the second 4K, up to the last 4K in base memory. If DMS is installed, each test continues to check memory above 32K in 4K increments by enabling the Dynamic Mapping System (only the system map is used). Then the next test is executed.

4-2. ADDRESS AND PATTERN TEST TST00

This is a cursory software test prior to entering the mirocoded routines. TST00 is an address and pattern test. The address test is accomplished by writing the address of a location in that location. When this is done throughout the module, the test verifies that each location contains it's address. The pattern test alternately places a 125252 and 025252 in each memory location and then vertifies the pattern.

4-3. GALLOPING READ RECOVERY TST01 TO TST04

The Galloping Read Recovery Test exercises memory such that each chip will see a one in a field of 4095 zeros or a zero in a field of 4095 ones for all memory locations. The test sequence and test patterns are shown in table 3-3.

Following is a description of the Galloping Read Recovery Test. Note that the console error messages refer to the routines within the Galloping Read Recovery (WRT.READ, READ, GAL.READ, and REFRESH); this is useful in determining the cause of the error.

1. Write all locations to background pattern (WRT.READ)

2. Verify background (READ)

3. Do Galloping Read Recovery (GAL.READ)

   a. Read location 0 — should be Background

   b. Write location 0 to test pattern (this becomes the test cell)

   c. Read Test Cell — should be the test pattern

   d. Read location 1 — should be background

   e. Read Test Cell — should be test pattern

   f. Read location 2 — should be background

   g. Read Test Cell — should be test pattern

      — continue to read each cell for background and then back to the test cell for the test pattern for the entire 4K module.

   h. Write Test Cell to background

   i. Make the Test Cell the next memory location in ascending order repeat the tests starting at step 3

   j. Repeat above sequence until test cell becomes the highest 4K address.

4. Write all locations to background (WRT.READ)

5. Delay in microcode to allow refresh to occur (REFRESH)

6. Verify background (READ).

4-4. MODULE 0 TEST TST05

This test is the combination of tests 0 through 4 performed on the first 4K of memory. It is accomplished by moving all of the program from the first 4K to the second 4K and then executing the test on the first 4K of memory. This test does not test memory locations 0 through 5 (memory location 5 is the parity error trap cell).

Table 4-1. Error and Information Halts

Halt Code	Test Section	Meaning or Routine where a failure occurred
102000	FRONT PANEL	Only occurs when 4K of memory is installed. This halt precedes the entry of the Front Panel microcoded routine, resulting in destruction of the diagnostic program. Press RUN to continue.
102001	FRONT PANEL	Data error (WRT.READ). Refer to paragraph 3-4.
102002	FRONT PANEL	Data error (READ). Refer to paragraph 3-4.
102003	FRONT PANEL	Data error (GAL.READ) if X-register bit 15 is set. Otherwise, operator has interrupted microcode by setting bit 9 of the S-register.
102004	FRONT PANEL	Data error (WRT.READ). Refer to paragraph 3-4.
102005	FRONT PANEL	REFRESH routine was interrupted.
102006	FRONT PANEL	Data error (READ). Refer to paragraph 3-4.
102007	——	Reserved.
102010	TST00	Data error *. Address and Pattern test Failed.
102011	TST01 through TST04	Data error* (WRT.READ)
102012	TST01 through TST04	Data error.* (READ)
102013	TST01 through TST02	Data error.* (GAL.READ)
102014	TST01 through TST04	Data error.* (WRT.READ)
102015	TST01 through TST04	REFRESH routine was interrupted.
102016	TST01 through TST04	Data error.* (READ)

*Refer to paragraphs 2-6 and 2-7 for explanation of console device and hardware register information.

Table 4-1. Error and Information Halts (Continued)

Halt Code	Test Section	Meaning or Routine where a failure occurred
102017	——	Reserved.
102020	TST05	Data error.* Address and Pattern Test failed in Module 0.
102021	TST05	Data error* in Module 0 (WRT.READ).
102022	TST05	Data error* in Module 0 (READ).
102023	TST05	Data error* in Module 0 (GAL.READ).
102024	TST05	Data error* in Module 0 (WRT.READ).
102025	TST05	REFRESH routine was interrupted
102026	TST05	Data error* in Module 0 (READ).
102027 to 102063	——	Reserved.
102064	TST05	Parity Error interrupt during the Module 0 Test.
102065	TST00 through TST04	Parity Error* interrupt caused by the parity chip (bit 16).
102066	All	Parity Error interrupt occurred and the address of the parity error was not the test address (the A-Register contains the address)
102067	All	Memory Protect interrupt.
102070	INITIAL-IZATION	HP 12978A 256 word WCS cannot be used on a 21MX E-Series computer.
102071	INITIAL-IZATION	WCS did not load correctly (check WCS board) or wrong WCS select code may have been used. Set the P-register to 100 and reenter WCS select code.
102072	INITIAL-IZATION	Computer type specified is not a 21MX. Irrecoverable.
102073	INITIAL-IZATION	Select code specified in the S-register is less than 10 (octal). Correct S-register and press RUN.
102074	INITIAL-IZATION	Configuration complete. Set the S-register according to table 3-2 and press RUN.
102075	CONTROL	Operator has aborted current test and requested test and memory module selection by setting S-register bit 9. Refer to paragraph 3-2.

*Refer to paragraphs 2-6 and 2-7 for explanation of console device and hardware register information.

Table 4-1. Error and Information Halts (Continued)

Halt Code	Test Section	Meaning or Routine where a failure occurred
102076	CONTROL	Operator has requested to halt after each test by setting S-register bit 15. The A-register contains the number of the test last executed. Press RUN to continue.
102077	CONTROL	Successful termination. The A-register contains the number of passes completed. Press RUN to execute another pass.
103003	FRONT PANEL	Operator has requested to abort current test by setting bit 9 of the S-register. See paragraph 3-4.
106010	TST00	Soft Error*. Address and Pattern test failed. Refer to paragraph 3-3.
106011	TST01 through TST04	Soft Error* (WRT.READ). Refer to paragraph 3-3.
106012	TST01 through TST04	Soft Error* (READ). Refer to paragraph 3-3.
106013	TST01 through TST04	Soft Error* (GAL.READ). Refer to paragraph 3-3.
106014	TST01 through TST04	Soft Error* (WRT.READ). Refer to paragraph 3-3.
106016	TST01 through TST04	Soft Error*. (READ)
106065	TST00 through TST05	Soft Error*. Parity Error Interrupt caused by the parity chip.

*Refer to paragraphs 2-6 and 2-7 for explanation of console device and hardware register information.

Table 4-2. Approximate Test Execution Times

Test	Approximate Execution Time	
	E-Series	M-Series
TST00	1.2 sec/4K module	2 sec./4K module
TST01	1 min. 10 sec. per 4K module	2 min. 15 sec. per 4K module
TST02	1 min. 10 sec. per 4K module	2 min. 15 sec. per 4K module
TST03	1 min. 10 sec. per 4K module	2 min. 15 sec. per 4K module
TST04	1 min. 10 sec. per 4K module	2 min. 15 sec. per 4K module
TST05	5 min. 30 sec.	9 min.

Quick Calculation for standard test:

Execution time = (no. of 4K modules) × 5.5 minutes (E-Series)
(no. of 4K modules) × 9.0 minutes (M-Series)

APPENDIX

A

SPECIAL PROCEDURES TO DISPLAY AND LOAD THE X- AND Y-REGISTERS ON THE M-SERIES COMPUTER.

To display the X-register on the M-Series computer:

1. Set the M-register to 100000. Do not press STORE.
2. Select the T-register; the contents of the X-register are displayed.
3. To change the value of the X-register, set the appropriate bits in the T-register and press STORE.

To display the Y-register on the M-Series Computer:

1. Set the M-register to 100001. Do not press STORE.
2. Select the T-register; the contents of the Y-register are displayed.
3. To change the value of the Y-register, set the appropriate bits in the T-register and press STORE.