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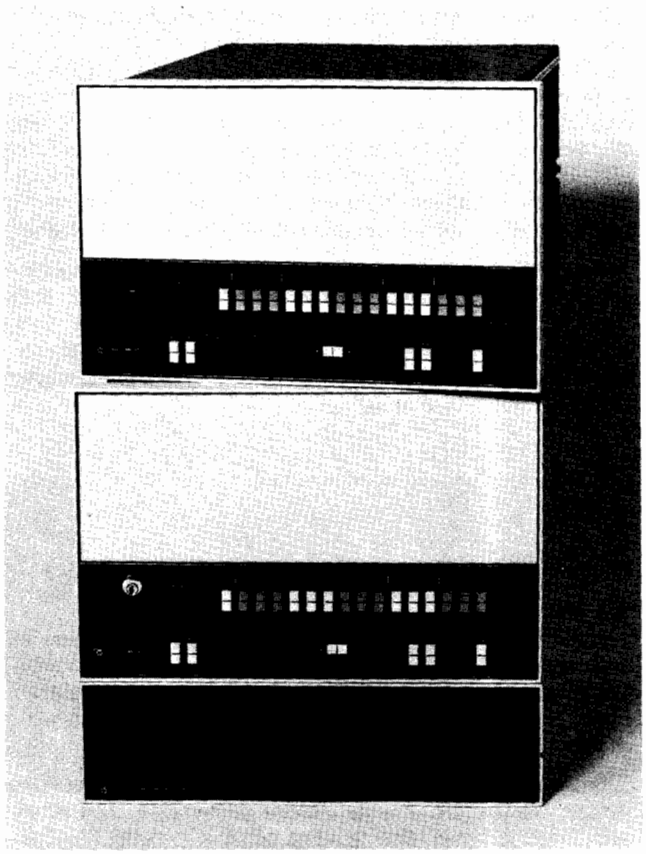
HP 1000
F-Series computers

models 2111F and 2117F

The F-Series are the most powerful HP 1000 Computers offered by Hewlett-Packard. These new machines combine the basic speed of the E-Series Computers with a new, high-performance Floating Point Processor, Scientific Instruction Set, and the FORTRAN accelerator routines of the Fast FORTRAN Processor to provide a high level of processing speed in a compact, economical package. The F-Series Computers are suitable for real-time applications that require exceptional processing speed and extended arithmetic precision.

A comprehensive range of software is available for both F-Series models, including program development support software and operating systems. Particularly noteworthy for computational applications involving large data arrays is HP's new disc-based RTE-IV operating system which can be used to equip the largest F-Series computer to process megabyte-sized data arrays. For additional information, see the HP 1000 Computers and Systems Active Software Data book, which is available from your Hewlett-Packard representative.

In addition, a full line of HP-manufactured peripherals and data communications interface kits is offered, enabling complete systems to be tailored around these new members of the HP 1000 family of computers.



Features

- High performance for computation intensive applications, provided by a unique combination of a high speed central processor, a high speed floating point processor, and a new set of instructions that further speed up processing in scientific and industrial computer applications
- High performance floating point processor dedicated to floating point operations. The processor works with both single-precision (32-bit) and extended precision (48-bit) numbers, and performs a single precision multiply in 6.2 microseconds.
- Scientific Instruction Set, a set of nine instructions for extremely fast computation of trigonometric and logarithmic functions. SIN(X), for example, requires less than 52 microseconds
- Fast FORTRAN Processor, a set of instructions that greatly accelerates FORTRAN operations by performing such jobs as array address calculations at hardware speed
- Powerful HP 1000 architecture and base instruction set, featuring variable microcycle timing for optimum price/performance
- High performance main memory, featuring a cycle time of 350 nanoseconds, is standard; 64k bytes in the 2111F, 128k bytes in 2117F. Fault control capability is optional
- Dynamic mapping system, optional in 2111F, standard in 2117F, provides for accessing up to 2 megabytes of memory (1.8 million bytes with fault control) in 2117F computer plus extender
- High speed direct memory access available via the Dual Channel Port Controller, with transfer rates up to 2.3 million bytes per second
- Fully user microprogrammable
  - — Complete microprogramming support software available
  - — Floating point processor is available as a computing resource to the microprogrammer
- Two models to choose from:
  - — 2111F, with space for up to 640k bytes of memory and nine I/O channels in 12-1/4 inch mainframe
  - — 2117F, with space for up to 1280k bytes of memory and fourteen I/O channels, in 17-1/2 inches of panel space
- Auto bootup and remote program load capability
- Self test for CPU and memory
- Disc loader program, contained in non-volatile Read-Only Memory is standard

The new HP 1000 F-Series — more processing speed and precision for your computational applications

A **new hardware-implemented Floating Point Processor,** included with the F-Series, slashes processing times for single-precision and extended precision operations. Add/subtract takes as little as 4.9 microseconds; multiply/divide in as little as 6.2 microseconds, thus providing the high level of floating point computational performance required for many real-time applications.

A new Scientific Instruction Set consisting of nine instructions works with the new Floating Point Processor to achieve execution speeds for trigonometric, logarithmic and other transcendental functions 6 to 24 times faster than equivalent software routines. Execution time for square root averages only 30.9 microseconds; sine and cosine average less than 48 microseconds. In addition, by taking advantage of the extended precision capabilities of the Floating Point Processor, the Scientific Instruction Set provides a single-precision result with accuracy superior to software libraries.

A Fast-FORTRAN Processor, a set of routines that accelerate the performance of FORTRAN programs, is also standard in the F-Series computers. Parameter passing, array address calculation floating point conversion operations, and other commonly-used FORTRAN routines are speeded up by a factor of 2 to 20.

Architecture

The HP 1000 F-Series architecture features a fully-microprogrammable control processor, which includes all arithmetic functions in addition to the calculation capabilities described above, I/O, self test, and full operator control panel. Four general-purpose registers are available, two of which may be used as index registers.

Standard F-Series instructions include indexed instructions; integer, single and double integer conversion, and single and extended-precision floating point arithmetic; trigonometric and logarithmic functions; data communications; I/O; and a full complement of instructions for logical operations and bit/byte manipulation.

The F-Series offers extensive software program and I/O compatibility with HP 1000 M- and E-Series Computers. F-Series processors have been optimized for performance with a microprogrammed control processor that directs operations of the other functional units. The control processor speed has been increased for certain operations by a sophisticated technique that varies microinstruction cycle time, depending on the complexity of the operation.

Efficiency of the microprogrammed routines that determine the machine language operation has also been increased through the mechanism of instruction and operand prefetch. The result is a high performance computer that retains both instruction set compatibility with earlier HP computers, and flexibility of user-microprogramming. The CPU-memory interface is totally asynchronous in the F-Series, adding flexibility to the powerful memory structure.

All I/O channels are fully-powered, buffered, and bi-directional. Because of modular design, mainframe memory capacity is completely independent of I/O capacity, so that either memory or I/O modules may be added without taking valuable mainframe space from the other. Mainframe memory capacity is 640k bytes in the 2111F and 1280k bytes in the 2117F (512 and 1024k bytes, respectively, with fault control). Up to nine additional modules may be added in the HP 12990B Memory Extender for a total capacity of 1792k bytes (1280k bytes with fault control) in a 2111F and 2048k bytes (1792k bytes with fault control) in a 2117F.

A full line of interface controllers is available to interface HP-manufactured peripherals, instrumentation, communications devices, or specialized devices.

For applications which demand even higher performance, F-Series users can expand their instruction repertoire with HP-supplied microprogrammed subroutines. Optional enhancements include the dynamic mapping system (standard in the 2117F) for expanded memory management, DS/1000 firmware for DS/1000 network communications, and RTE-IV Extended Memory Area (EMA) firmware.

User microprogramming

The advantage of microprogramming. The power and flexibility of control processor microprogramming is readily available to F-Series users. Control processor access provides users with the ability to perform commonly-used software routines 2 to 20 times faster in microcode. Control processor routines are written in an assembly-like language, stored in control processor memory, and called directly from Assembly, FORTRAN, or BASIC programs.

The control processor and control store capacity. Control processor programmers have access to a powerful processor within F-Series computers that executes instructions in 175-to-280 nanoseconds, and provides multi-level nested subroutines, 211 instructions, 12 high-speed scratchpad registers, and a 5k word address space available to the user. Up to 3k words of user microprograms may be implemented in Writable Control Store for microprogram development and dynamic loading of microprograms. Fully-developed microprograms may be stored in Programmable Read-Only Memory (PROM), a more permanent and secure storage medium for microprograms.

Microprogrammed use of the Floating Point Processor. Microprogrammers can use the Floating Point Processor (FPP) as a control processor computing resource to obtain significant performance increases over normal microprogramming. To the microprogrammer, the FPP provides a very high speed processor for floating point and extended precision integer operations. An example of the combined power of the Floating Point Processor and direct microprogramming is given by execution of a Sine(X) library function. With FPP, the execution time is 127.5 microseconds. With FPP and direct microprogramming, the execution time is 51.8 microseconds, more than 2.5 times faster.

Software support for microprogram development. Control processor program development is aided by HP's complete software development tools, which include a micro-assembler, microdebug editor, program overlay load utility, and PROM tape generator, as well as a complete documentation package.

Memory system

Much of the speed of the F-Series Computer is due to the high speed of its primary memory systems. The F-Series Computer includes a memory system that cycles in 350 nanoseconds and with a capacity up to 2 million bytes. Parity checking is standard in all HP 1000 memory systems. Fault control memory systems, which are capable of detecting and correcting all single-bit memory errors, and detecting all double bit errors, are optionally available (fault control reduces maximum memory capacity to about 1.8 million bytes).

For efficient handling of large memory systems, the Dynamic Mapping System (DMS) is available in the 2111F, standard in the 2117F. A combination of hardware and control processor programs, DMS is a powerful memory manager that allows F-Series users to address up to 2.048M (2048k) bytes of memory and provides read and/or write protection of each individual 2048-byte page. Four independent memory maps are provided — one for the operating system, one for the user, and two port controller maps for direct memory access operations. DMS adds 38 powerful memory management instructions to the standard F-Series instruction set. This capability is fully supported by HP's RTE-M and RTE-IV real-time executive operating systems which offer multi-user access to as many as 64 multi-user program partitions. In RTE-IV, support of large-memory systems also gives the user access to data arrays up to megabyte size in one or more Extended Memory Areas (EMAs).

Input/output

The F-Series I/O system features a multi-level, vectored priority interrupt structure. There are 50 distinct interrupt levels, each with a unique priority assignment.Any I/O device can be selectively enabled or disabled, or the entire interrupt system (except power fail and parity error interrupts) can be enabled or disabled under program control.

Data transfer between the computer and I/O devices may take place under program control, dual channel port controller (DCPC) control, or microprogram control. The DCPC provides two direct links between memory and I/O devices, and is program assignable to any two devices. DCPC transfers occur on an I/O cycle-stealing basis, not subject to the I/O priority interrupt structure.

For applications where higher transfer rates are desirable, The F-Series has a special Microprogrammable Block I/O capability that allows transfer rates up to 3.1 million bytes/second. This capability can be implemented through user-designed I/O cards and block I/O control microprograms.

Remote and local program load

The initial binary loading (IBL) function is easily performed on F-Series Computers. For local bootstrap loading, a 64-word ROM-resident IBL program is called by a push-button switch on the front panel. Paper tape and disc loader ROMs are standard. Up to two additional HP or user-supplied loader ROMs may be added to any F-Series Computer. The user can plug in up to four different loader ROMs if the standard loader ROMs are removed.

Computers at remote sites can be force-loaded from a central location through the use of a remote program load (RPL) capability. Information normally keyed into the front panel is set in switches on the CPU board, so the bootstrapping sequence may be initiated from a remote site, or automatically initiated on power-up from a local peripheral.

Self test

A comprehensive set of diagnostic routines permanently stored in read-only memory (ROM) is standard in the F-Series. Two of these routines, executed each time the IBL/TEST function is executed, provide quick tests of the processor and first 64k bytes of physical memory for verification of operating condition. A third test, executed whenever the machine is powered up, thoroughly tests the processor and all installed memory. This test may also be run manually. Two other tests, executed from the front panel, provide quick verification checks of the Floating Point Processor and the Scientific Instruction Set.

Power fail recovery system

The optional power fail recovery system provides a minimum of 1.6 hours of memory sustaining power for the largest memory configuration in the event of complete power failure.

Software

The HP 1000 F-Series maintains extensive program compatibility with earlier members of the HP 1000 family, so users can take advantage of many man-years of software development. This includes compatibility of the Floating Point Processor with the standard firmware floating point instructions of previous machines.

A wide range of operating system software is available. Real-time executive (RTE) systems, available in disc and main memory-resident versions, are multiprogramming systems that permit priority scheduling of several real-time programs while concurrent background processing also takes place.

The memory-based RTE-M and disc-based RTE-IV operating systems can support up to 2.048 megabytes of memory, managed by DMS. Comprehensive software systems are also available for computer networking.

Languages supported by HP operating systems include FORTRAN IV, HP real-time BASIC, Assembly language, and micro-assembly language. Utility software includes a debugging routine, interactive editors, and an extensive library of commonly-used computational routines.

F-Series users may also take advantage of a wide variety of thoroughly-tested and documented programs that have been contributed to the HP Library of Contributed User Software (LOCUS).

Functional specifications

Processor architecture

Implementation: Diagonally microprogrammed in MSI and SSI hardware, supplemented by the Floating Point Processor

Data path width: 16 bits

Standard registers:
Accumulators: 2 (A and B), 16 bits each, addressable as registers or memory locations
Index: 2 (X and Y), 16 bits each
Memory control: 3 (T,P) 16 bits each; (M), 15 bits
Supplementary: 2 (overflow and extend), 1 bit each
Manual data: 1 16-bit (display)

Instruction types:

Memory-to-accumulator	Accumulator-to-I/O
Memory-to-memory	Device control
Direct register modification	

Instruction formats:

Combined single word	Single-precision floating point
Single word	Extended-precision floating point

Instruction expansion: 176 instruction codes are available to the microprogrammer for instruction set additions.

Addressing modes:

Direct	Triple word
Multi-level indirect	Double word
Indexed	Single word
Indirect indexed	Byte
Register implicit	Bit

Bus structure: Separate memory data, memory address, and I/O buses tied to the unified internal processor's S Bus

Memory structure: 32 pages of 2048 bytes, with direct access to current or base page (page 0) pages; indirect or indexed access to all pages

Memory expansion: Paged memory address space expandable to 1024 pages of 2048 bytes using the 13305A Dynamic Mapping System

Input/Output: Vectored priority interrupt structure for up to 50 I/O and system devices, such as DCPC, power fail, parity, and memory protect.

Control processor

Implementation: Hardwired MSI and SSI TTL

Instruction execution time: Variable, 175 or 280 nsec

Control path: 24 bits

Data path: 16 bits

Registers:
Standard registers: 4 (A,B,X,Y)
Scratch registers: 12 16-bit registers accessible to the microprogrammer
Iteration counter: 8 bits
Instruction register: 16 bits
Latch register: 16 bits
Status flag: 1 bit
Subroutine levels stack: 3 — 14 bits each

Bus structure: Unified single bus with program access to memory data, memory address, and I/O buses

Bus speed: 11.4M bytes/sec

Instruction formats:
TYPE 1 Data transfer and modification
TYPE 2 Constant formation
TYPE 3 Conditional branch
TYPE 4 Unconditional branch

Control memory structure:
Type: Bipolar LSI semiconductor R/W or ROM
Address space: 16,384 words; 64 modules of 256-words each
Word size: 24 bits
Cycle time: Variable, 175 or 280 nsec

Module assignments
(1 module = 256 words of control memory):
0 to 3 assigned to F-Series base instruction set, including the new Floating Point Processor instructions
4 through 19 reserved for HP enhancements
20-31 reserved for HP instruction set enhancements or user microprogramming
32 reserved for Dynamic Mapping instruction set Instructions
33 through 35 reserved for Fast FORTRAN Processor
36 and 37 reserved for Extended Memory Area mapping instructions
38 and 39 reserved for DS/1000 firmware
40 through 43 reserved for Scientific Instruction Set
44 and 45 reserved for HP instruction set enhancements
46 through 63 reserved for user microroutines

Control processor instructions: 211 total; up to 5 may be combined in 1 instruction
Operations: 15 total
Special: 32 total
ALU and conditional: 68 total
Store (destination): 32 total
S-bus (source): 32 total
Reverse Sense: 32 total

Memory parity check

Operation: Monitors all words read from memory. Utilizes 17th bit in memory. Switch programmable to halt or ignore parity error when detected. Interrupt on error requires memory protect option. Parity error indication is displayed on the front panel.

Power fail interrupt

Priority: Highest priority interrupt

Power failure: Detects power failure and generates an interrupt to memory location 4 for vector to user-written power failure routine. A minimum of 500 microseconds is provided for execution of the user-written system state save routine.

Microprogrammable block I/O

I/O control lines: 3 special lines on I/O backplane

NOTE: Requires user designed I/O cards

Maximum synchronous transfer rate: 3.18M bytes/sec (input); 2.72M bytes/sec (output).

Remote program load

Load device selection: 1 of 9 devices in a 2111F; 1 of 14 devices in a 2117F

Loader selection: One of 2 optional loader ROMs

Operating modes: A) Automatically on power-up; B) Remote forced load with 12966A or 12968A interface (Hardwired); C) Load after certain halts under program control.

Compatibility

Instruction set: The HP 1000 F-Series instruction set is backwards compatible with all previous HP 1000 and 2100 Series computers

Program: Most programs written for HP 1000 and 2100 Series computers are compatible with the F-Series, except those with timing loop dependence.

Approximate instruction execution times

Instruction	Execution Time (μsec) with High Performance Memory Min.	Typ.	Max.	MNI*
Single-precision Floating Point Instructions (8 total)				
Add/Subtract	4.9	4.9	6.5	
Multiply	6.2	6.3	6.5	
Divide	6.2	7.5	9.0	
Conversion to single integer	3.7	4.0	4.8	
Conversion to double integer	3.5	3.8	5.9	
Conversion from single integer	3.4	3.7	4.5	
Conversion from double integer	3.3	3.7	5.2	
Extended-precision Floating Point Instructions (8 total)				
Add/Subtract	10.7	10.7	13.3	
Multiply	12.6	12.9	13.3	
Divide	12.6	14.8	17.1	
Conversion to single integer	5.8	6.1	6.9	
Conversion to double integer	6.4	6.4	8.4	
Conversion from single integer	5.9	6.0	6.6	
Conversion from double integer	6.6	6.6	7.3	
Scientific Instruction Set Instructions (9 total)				
SIN (Sine) function		47.6	51.8	8.0
COS (Cosine) function		47.9	52.0	9.0
TAN (Tangent) function		48.4	53.7	8.0
ATAN (Arc Tangent) function		42.4	52.6	12.0
TANH (Hyperbolic Tangent) function		57.2	66.5	9.0
SQRT (Square Root) function		30.9	37.8	11.0
EXP (e^x) function		44.7	51.9	8.0
ALOG (Natural Logarithm) function		43.3	46.3	8.0
ALOGT (Base 10 Logarithm) function		49.4	52.6	8.0
Fast FORTRAN Processor Instructions (9 total)				
Moves to new locations:				
— Extended precision variable	8.96		12.81	
— Address of parameters from calling sequence into subroutine list	13.9 +3.7*NP		13.9 +3.7*NP	
Calculation of X*2N for real X and integer N	8.4		8.4	
Unpacking of real variable	3.1		3.1	
Normalization, rounding, and packing of mantissa of extended precision variable	18.9		29.5	11.6
Complementing of extended precision variable	11.7		12.1	
Complementing and normalization of extended precision variable	22.1		33.4	12.2
Transfer of control to destination of FORTRAN computed GOTO statement	10.6		10.6	
Computes address of specified element of 2 or 3-dimensional array	17.7		27.2	
Memory reference group (14 total)				
Add/load/AND/IOR/XOR			0.91	
Store			1.26	
Jump			0.74	
Jump to subroutine			1.61	
Compare (normal/skip)			1.09/1.43	
Increment, skip if zero			1.54/1.61	
Indirect address, per level			0.46	
Register reference group (43 total)				
Normal/skip			0.91/1.26	
I/O group (13 total)				
SFS/SFC/SOS/SOC (normal/skip)	1.58/1.96		2.28/2.66	
All others	1.58		2.28	

Approximate instruction execution times, continued

Instruction	Execution Time (μsec) with High Performance Memory Min.	Typ.	Max.	MNI*
Extended instruction group (10 total)				
Integer multiply	5.3		6.0	
Integer divide	7.7		9.1	
Double load			2.07	
Double store			2.7	
Shift/rotate (basic)			1.47	
Additional per shift			0.175	
Indirect addressing/level			0.81	
Index instructions (32 total)				
Copy			1.29	
Exchange			1.92	
Decrement/increment (normal/skip)			1.75/2.0	
Load or add index			2.66	
Store index			2.94	
Load indexed			3.19	
Store indexed			3.46	
Jump and load Y			2.67	
Jump and index X			2.28	
Data communications (10 total)				
Load byte			3.36	
Store byte			3.89	
Move bytes (basic)			3.75	
Additional per byte			4.05	
Move words (basic)			3.75	
Additional per word			1.68	
Compare bytes (basic)			3.75	
Additional per byte	3.5		3.78	
Compare words (basic)			3.75	
Additional per word			2.38	
Scan for byte (basic)			1.92	
Additional per byte			2.735	
Set or clear bits			4.48	
Test bits (normal/skip)			4.73/4.94	

NOTES:

**MNI = Maximum Non-Interruptible time.*

Fault control memory and dynamic mapping system may each add 0 to 0.2 microseconds to these instruction execution times.

Asynchronous memory may cause variations of ±0.035 microseconds per memory reference.

More detailed instruction times are supplied in the HP 1000 F-Series reference manual (02111-90001)

Scientific instruction set

Data format: Single-precision

Execution times and function definitions: See Approximate instruction execution times table

Accuracy: RMS relative error for the various Scientific Instruction Set functions is as follows:

Function	RMS Rel. Error	Function	RMS Rel. Error
SIN	8.80E-8	SQRT	6.74E-8
COS	8.82E-8	EXP	1.38E-7
TAN	1.99E-7	ALOG	1.28E-7
ATAN	1.34E-7	ALOGT	1.39E-7
TANH	1.33E-7		

Floating Point Processor (FPP)

Floating point data formats:
Single-precision: 32 bits (4 bytes), providing at least 6 significant decimal digits in mantissa
Extended-precision: 48 bits (6 bytes), providing at least 11 significant decimal digits in mantissa

Exponent range: Exponent range: 2^{-128} to 2^{+127} in all floating point data formats; decimal equivalent is $10^{\mp 38}$.

Fixed point data formats:
Single-precision: 16 bits (2 bytes), twos complement integer
Double-precision: 32 bits (4 bytes), twos complement integer

Execution times: See Approximate instruction execution times table

Computation times applicable to direct, chained microprogramming use of the Floating Point Processor: The following computation times apply to directly microprogrammed use of the Floating Point Processor for chained floating point calculations in which intermediate results are not transferred to and from the F-Series Computer memory.

	Computation Time (μsec)		
Instruction	Min.	Typ.	Max.
Single-precision Floating Point Operations (8 total)			
Add/Subtract	0.55	0.63	3.15
Multiply	1.55	1.78	2.5
Divide	1.65	3.03	4.9
Conversion to single integer	0.33	0.88	1.45
Conversion to double integer	0.33	1.48	2.65
Conversion from single integer	0.28	0.6	1.45
Conversion from double integer	0.28	0.6	1.45
Extended-precision Floating Point Operations (8 total)			
Add/Subtract	0.55	0.68	4.8
Multiply	2.4	2.75	3.3
Divide	2.5	4.88	7.7
Conversion to single integer	0.33	0.88	1.45
Conversion to double integer	0.33	1.48	2.65
Conversion from single integer	0.28	0.6	1.45
Conversion from double integer	0.28	0.6	1.45

Fast FORTRAN processor (FFP)

Data formats and exponent range: Same as Hardware Floating Point Processor.

Execution times: See Approximate instruction execution times table

Configuration information:

Input/output capacity:	2111F	2117F
I/O channels in mainframe	9	14
With first I/O extender	25	30
With two I/O extenders	41	46
Standard memory:	64kb	128kb
Memory module spaces		
In computer only	5	10
In computer & extender	14	19
Max. non-fault control memory*		
In computer only	0.640Mb	1.280Mb
In computer & extender	1.792Mb	2.048Mb
Max. fault control memory*		
In computer only	0.512Mb	1.024Mb
In computer & extender	1.280Mb	1.792Mb

Based on use of 128k byte memory modules.

Control processor address space:
Total address space: 16k 24-bit words
PROM address space available on FAB board: 1k, exclusive of space dedicated to Dynamic Mapping Instructions*†
WCS overlay address space using 1k WCS boards: 3k**
User PROMs address space using 2k UCS board: 2k**

** Subtract 0.5k each for Extended Memory Area mapping instructions (with 92067A RTE-IV) and DS/1000 firmware (with 91740B DS/1000 Network software-formware).*

† Mounted on 3.5k firmware accessory board under CPU board.

*** Mounted on board(s) in CPU I/O backplane, using I/O slots*

Electrical specifications

AC power required

2111F Line voltage: 88-132V (110V ± 20%); 176-264V 220V ± 20%) with option 015. Input line voltage range is easily changed in the field by moving jumper connections.

2117F Line voltage: Computer mainframe is same as 2111F; Floating Point Processor voltage selector offers choice of 90-110V (100V ± 10%), 108-132V (120V ± 10%), 198-242V (220V ± 10%), and 216-264V (240V ± 10%) input line voltage ranges.

Line frequency: 47.5-66 Hz.

Maximum power required:
2111F: 625W
2117F: 825W

Current available (+) required (−) for memory, I/O interfaces and accessories

See power specifications and applicability summary tables pages 10-0 and 10-1.

Power supply

Storage after line failure: Sustains computer through a line loss of 8 milliseconds when operating at the minimum ac line voltage

Input line overvoltage protection: Circuit breaker protects against surge caused by connecting computer to twice nominal line voltage

Input line transients: Withstands power line transients up to ±500V for 50μsec wide pulse, up to ±1000V for 100 nsec wide pulse, without damage

Output voltage regulation: ±5%, except −2V is ±10%

Output protection: All voltages are protected for over-voltage and over-current

Thermal sensing: Monitors internal temperature and automatically shuts down computer if temperature exceeds specified level.

Safety

Models 2111F and 2117F are recognized by Underwriters Laboratories, Inc., and certified by the Canadian Standards Association (with the exception of option 015).

Physical characteristics

Dimensions, cm & (in)	**2111F**	**2117F**
Panel width:	48.3 (19)	48.3 (19)
Behind-panel width:	42.6 (16-3/4)	42.6 (16-3/4)
Overall depth:	62.2 (24-1/2)	62.2 (24-1/2)
Depth behind panel:	58.4 (23)	58.4 (23)
Height	31.1 (12-1/4)	44.5 (17-1/2)

Weight, kg & (lb)

2111F: 30 (66)
2117F: 50 (110)

Ventilation

Air intake is on the left side, exhaust is on the right hand side.

Heat dissipation

2111F: 580 kilogram-calories/hour (2303 BTU/hour)

2117F: 752 kilogram-calories/hour (2986 BTU/hour)

Air flow	2111F	2117F*
Cubic meters/minute:	7.9	11
Cubic feet/minute:	280	390

** 2117F air flow includes flow through the computer mainframe and through the floating point processor, which is a separate package of the 2117F.*

Ordering information

2111F Computer

The 2111F Computer consists of:

1. 2111B Computer with paper tape and disc loader ROMs.
2. 2102E High performance memory controller and two 12741A 32k byte High performance memory modules.
3. 12943-16001 and 16002; 24396-12001, 12002, and 12003; 12740-16001; 12977-16004 and 16005; and 24296-60001 Diagnostics and configurator on paper tape.
4. 02111-90001 HP 1000 F-Series computers operating and reference manual.
5. 02109-90014 Microprogramming manual.
6. 2111-90002 HP 1000 F-Series installation and service manual.
7. 12943-90004, 24396-140001, 12740-90001, and 12977-90002 diagnostic manuals.

2117F Computer

The 2117F Computer consists of:

1. 2117B Computer with separate mainframe, including paper tape and disc loader ROMs, and 02117-60001 Floating Point Processor.
2. 12788A 128k byte High performance memory package, including 2102E Memory controller, 12747H 128k byte High performance memory module, and 13305A Dynamic mapping system.

3-7. Same as items 3 through 7 of 2111F Computer, listed above.

8. 12740-90007 Floating Point Processor installation and service manual.

2111F and 2117F Option

014: Deletes standard memory, item 2, above, from 2111F or 2117F, to permit its replacement, with another HP high performance memory system, with or without fault control, which must be ordered separately.

015: 220V operation (applies only to 2111F and computer mainframe of 2117F; Floating Point Processor input voltages are switch selectable).

2111F and 2117F accessories

For list of accessories that are compatible with the 2111F and 2117F computers, see the power specifications and applicability summary on pages 10-0 and 10-1, referring to the Series F applicability column.