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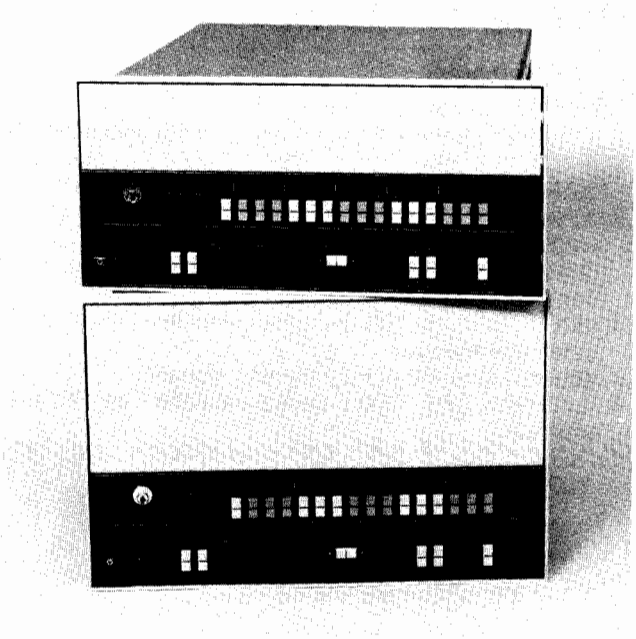
HP 1000 E-series computers

models 2109E and 2113E

The HP 1000 E-Series computers are intermediate-performance members of the HP 1000 Computer Family. Combining successful HP 1000 architecture with a unique design philosophy, the E-Series has the power to meet tough computing demands.

A comprehensive range of software is available for both models, including compilers, and operating systems. In addition, a full line of HP-manufactured peripherals and data communications interface kits is offered, enabling complete systems to be tailored around these members of the HP 1000 Family.



Features

- Proven HP 1000 architecture, providing extensive compatibility with HP 1000 Series processor options, peripherals, operating systems, and software
- Variable microcycle timing (VMT) for maximum processor speed
- Powerful instruction set with 128 instructions
- 2.28 million byte/second direct memory access transfer rate available with Dual Channel Port Controller (DCPC)
- User microprogrammable, with complete user-microcode support
- Two models to choose from:
  - — 2109E, with space for up to 640k bytes of memory and nine I/O channels in 8-3/4 inch mainframe
  - — 2113E, with space for up to 1280k bytes of memory and fourteen I/O channels in 12-1/4 inch mainframe
- Standard performance main memory is standard: 64k bytes in 2109E, 128k bytes in 2113E. 350 nanosecond High performance memory and/or fault control capability is optional
- Dynamic mapping system, optional in 2109E, standard in 2113E, provides for accessing up to two megabytes of memory (1.8 million bytes with fault control) in 2113E computer plus memory extender
- Remote program load capability
- Self test for CPU and memory
- Microprogrammable processor port, permitting external processors to be interfaced directly to the E-Series control processor
- Microprogrammable block I/O for intelligent microprogrammed I/O channels
- Paper tape and disc loader ROM's are standard

Description

Architecture

HP 1000 E-Series architecture features a fully-microprogrammed processor, which includes all arithmetic functions, I/O, and full operator control panel. Four general-purpose registers are available, two of which may be used as index registers.

Standard E-Series instructions include indexed instructions, integer and floating point arithmetic, data communications, I/O, and a full complement of instructions for logical operations and bit/byte manipulation.

The E-Series offers extensive software program and I/O compatibility with other HP 1000 computers. E-Series processors have been optimized for performance with a microprogrammed control processor that directs operations of the other functional units. The control processor speed has been increased for certain operations by a sophisticated technique that varies microinstruction cycle time, depending on the complexity of the operation.

Efficiency of the microprogrammed routines that determine the machine language operation has also been increased through the mechanisms of instruction and operand prefetch. The result is a high-performance computer that retains both instruction set compatibility with earlier HP computers, and flexibility of user-microprogramming. The CPU-memory interface is totally asynchronous in the E-Series, adding flexibility to the powerful memory structure.

All I/O channels are fully-powered, buffered, and bidirectional. Because of modular design, mainframe memory capacity is completely independent of I/O capacity, so that either memory or I/O modules may be added without taking valuable mainframe space from the other. Mainframe memory capacity is 640k bytes in the 2109E and 1280k bytes in the 2113E (512 and 1024k bytes, respectively, with fault

control). Up to nine additional modules may be added in the HP 12990B Memory Extender for a total capacity of 1792k bytes (1280k bytes with fault control) in a 2109E and 2048k bytes (1792k bytes with fault control) in a 2113E.

A full line of I/O interface controllers is available to interface HP-manufactured peripherals, instrumentation, communications devices, or specialized devices.

For applications which demand even higher performance, E-Series users can expand their instruction repetoire with HP-supplied microprogrammed subroutines. Enhancements include the dynamic mapping system, available in 2109E, standard in 2113E, for expanded memory management, and Fast FORTRAN processor for fast handling of scientific routines.

User-microprogramming

The power and flexibility of control processor microprogramming is readily available to E-Series users. Control processor access provides users with the ability to perform commonly-used subroutines 2-to-20 times faster than with conventional computing techniques. Control processor subroutines are written in a simple assembly language, stored in control processor memory, and called directly from Assembly, BASIC, or FORTRAN programs.

Control processor programmers have access to a powerful processor within E-Series computers that executes instructions in 175-to-280 nanoseconds, and provides multilevel nested subroutines, 211 instructions, 12 high-speed scratchpad registers, and an 8.5k word user address space. Up to 5.5k words of commonly-used control processor programs may be stored in programmable read-only memory (PROM). The additional 3k word address space provides a control processor program overlay area implemented with writable control store. Program overlays provide a flexible system able to react to dynamic changes in speed requirements dictated by user program mix.

Control processor program development is aided by HP's complete software development tools, which include an assembler, debug editor, program overlay utility, and PROM tape generator, as well as a complete documentation package.

Memory system

The E-Series includes a standard performance memory system that utilizes the same field-proven semiconductor memory modules as the HP 1000 M-Series. Based on 4k or 16k bit MOS/RAM semiconductor chips, this system combines speed, reliability, and economy. High-speed, 350 ns cycle time memory is available to increase performance by up to 30%. For data integrity, memory parity check is standard and fault control capability may be added to improve the MTBF of memory systems. Memory is easily expandable by plug-in 32k and 128k byte modules.

For efficient handling of large memory systems, the dynamic mapping system (DMS) is available in the 2109E, standard in the 2113E. A combination of hardware and control processor programs, DMS is a powerful memory manager that allows E-Series users to address up to 2048k bytes of memory, and provides read and/or write protection of each individual 2,048 byte page. Four independent memory maps are provided — one for the system, one for the user, and two port controller maps for direct memory access operations. DMS adds 38 powerful memory management instructions to the standard E-Series instruction set. This capability is fully supported by HP's RTE-M and RTE-IV real-time executive operating systems which offer multi-user access to as many as 64 multi-user program partitions. In RTE-IV, support of large-memory systems also gives the user access to megabyte-sized data arrays in one or more Extended Memory Areas (EMAs).

Input/output

The E-Series I/O system features a multilevel vectored priority interrupt structure. There are 50 distinct interrupt levels, each with a unique priority assignment. Any I/O device can be selectively enabled or disabled or, the entire interrupt system (except power fail and parity error interrupts) can be enabled or disabled under program control.

Data transfer between the computer and I/O devices may take place under program control, dual channel port controller (DCPC) control, or microprogram control. The DCPC provides two direct links between memory and I/O devices, and is program-assignable to any two devices. DCPC transfers occur on an I/O cycle-stealing basis, not subject to the I/O priority interrupt structure.

For applications where higher transfer rates are desirable, the E-Series has a special Microprogrammable Block I/O capability that allows transfer rates up to 3.1 million bytes/second. This capability can be implemented through user-designed I/O cards and block I/O control microprograms.

Remote and local program load

The initial binary-loading (IBL) function is easily performed on E-Series computers. For local bootstrap loading, a 64-word ROM-resident IBL program is called by a push-button switch on the front panel. Paper tape and disc loader ROM's are standard. Up to two additional HP or user-supplied loader ROMs may be added to any E-Series computer. The user can plug in up to four different loader ROMs if the standard loader ROMs are removed.

Computers at remote sites can be force-loaded from a central location through the use of a remote program load (RPL) capability. Information normally keyed into the front panel is set in switches on the CPU board, so the bootstrapping sequence may be initiated from a remote site, or automatically initiated on power-up from a local peripheral.

Self test

A comprehensive set of diagnostic routines permanently stored in read-only memory (ROM) is standard in the E-Series. Two of these routines, executed each time the IBL/TEST function is executed, provide quick tests of the processor and first 64k bytes of physical memory for verification of operating condition. A third test, executed whenever the machine is powered up, thoroughly tests the processor and all installed memory. This test may also be run manually.

Microprogrammable processor port (MPP)

The microprogrammable processor port provides a direct interface to the CPU for user-designed hardware processors. The MPP provides address, data, and control capability, so external processors can be controlled and can transfer data at burst rates up to 11.4M bytes/second.

Power system

HP 1000 E-Series power systems will operate normally in environments where power fluctuates widely. Input line voltages and frequencies may vary considerably without affecting computer operations. The optional power fail recovery system provides a minimum of 1.6 hours of memory sustaining power for the largest memory configuration, in the event of complete power failure.

Software

The HP 1000 E-Series maintains extensive program compatibility with earlier members of the HP 1000 Family, so users can take advantage of many man-years of software development.

A wide range of operating system software is available. Real-time executive (RTE) systems, available in disc and main memory-resident versions, are multi-programming systems that permit priority scheduling of several real-time programs while concurrent background processing takes place.

The memory-based RTE-M and disc-based RTE-IV operating systems can support up to 2.048M bytes of memory, managed by DMS. Comprehensive software systems are also available for computer networking.

Languages supported by HP operating systems include FORTRAN IV, HP BASIC, Assembler, and user microprogramming. Utility software includes a debugging routine, a symbolic editor, and an extensive library of commonly-used computational routines.

E-Series users may also take advantage of a wide variety of thoroughly-tested and documented programs that have been contributed to the HP User Library.

Functional specifications

Processor architecture

Implementation: Diagonally microprogrammed in MSI and SSI hardware

Data path width: 16 bits

Standard Registers:
Accumulators: 2 (A and B), 16 bits each, addressable as registers or memory locations
Index: 2 (X and Y), 16 bits each
Memory control: 3 (T,P), 16 bits each; (M), 15 bits
Supplementary: 2 (overflow and extend), 1 bit each
Manual data: 1 16-bit (display)

Instruction types:

Memory-to-accumulator	Accumulator-to-I/O
Memory-to-memory	Device control
Direct register modification	

Instruction formats:

Combined single-word	Single-precision floating point
Single-word	Extended precision floating point

Instruction expansion: 176 instruction codes are available to the microprogrammer for instruction set additions.

Addressing modes:

Direct	Double word
Multilevel-indirect	Single word
Indexed	Byte
Indirect indexed	Bit
Register implicit	

Bus structure: Separate memory data, memory address, and I/O buses tied to the unified internal processor's S Bus

Memory structure: 32 pages of 2048 bytes, with direct access to current or base (page 0) pages; indirect or indexed access to all pages

Memory expansion: Paged memory address space expandable to 1024 pages of 2048 bytes using the 13305A Dynamic Mapping System

Input/output: Vectored priority interrupt structure for up to 50 I/O and system devices, such as DMS, power fail, parity, and memory protect.

Control processor

Implementation: Hardwired MSI and SSI TTL

Instruction execution time: Variable, 175 or 280 nsec

Control path: 24 bits

Data path: 16 bits

Registers:
Standard registers: 4 (A,B,X,Y)
Scratch registers: 12 16-bit registers accessible to the microprogrammer
Iteration counter: 8 bits
Instruction register: 16 bits
Latch register: 16 bits
Status flag: 1 bit
Subroutine levels stack: 3-14 bits each

Instruction formats:
TYPE 1 Data transfer and modification
TYPE 2 Constant formation
TYPE 3 Conditional branch
TYPE 4 Unconditional branch

Bus structure: Unified single bus with program access to memory data, memory address, and I/O buses

Bus speed: 11.4M bytes/sec

Control memory structure:
Type: Bipolar LSI semiconductor R/W or ROM
Address space: 16,384 words; 64 modules of 256-words each
Word size: 24 bits
Cycle time: Variable: 175 or 280 nsec

Module assignments (1 module =256 words of control memory):
0 to 3 assigned to E-Series base instruction set
Modules 4 to 19 reserve for HP instruction set enhancements.
Modules 20-31 reserved for HP instruction set enhancements or user microprogramming
Module 32 reserved for DMS instructions
Modules 33 through 35 reserved for Fast FORTRAN Processor
Modules 36 and 37 reserved for RTE-IV Extended Memory Area mapping instructions
Modules 38 and 39 reserved for DS/1000 firmware
Modules 40 through 43 reserved for Scientific Instruction Set
Modules 44 and 45 reserved for future HP instruction set enhancements
Modules 46 to 63 reserved for user microroutines

Control processor instructions: 211 total; up to 5 may be combined in 1 instruction
Operations: 15 total
Special: 32 total
ALU and conditional: 68 total
Store (destination): 32 total
S bus (source): 32 total
Reverse Sense: 32 total

Memory parity check

Operation: Monitors all words read from memory. Utilizes 17th bit in memory. Switch programmable to halt or ignore parity error when detected. Interrupt on error requires memory protect option. Parity error indication is displayed on the front panel.

Approximate instruction execution times

Instruction	Execution Time (μsec) With Std Performance Memory	With High Performance Memory
Memory reference group (14 total)		
Add/load/AND/IOR/XOR	1.19	0.91
Store	1.85	1.26
Jump	0.74	0.74
Jump to subroutine	1.85	1.61
Compare (normal/skip)	1.23/1.72	1.09/1.43
Increment, skip if zero	2.03	1.54/1.61
Indirect addr/level	0.575	0.46
Register reference group (43 total)		
Normal/skip	1.19/1.29	0.91/1.26
Input/Output group (13 total)		
SFS/SFC/SOS/SOC (normal)	1.58-2.28	1.58-2.28
SFS/SFC/SOS/SOC (skip)	2.03-2.73	1.96-2.66
All others	1.58-2.28	1.58-2.28
Extended instruction group (10 total)		
Multiply	5.74-6.72	5.3-6.0
Divide	8.09-9.63	7.7-9.1
Double load	3.185	2.07
Double store	3.71	2.7
Shift/rotate (basic)	2.065	1.47
Additional per shift	0.175	0.175
Indirect addressing	1.19	0.81
Index instructions (32 total)		
Copy	1.435	1.29
Exchange	2.065	1.92
Decr./increment (normal)	2.03	1.75
Decr./increment (skip)	2.52	2.00
Load/add index	3.05	2.66
Store index	3.43	2.94
Load indexed	3.745	3.19
Store indexed	3.815	3.46
Jump and load Y	2.8	2.67
Jump and index X	2.625	2.28
Data communications (10 total)		
Load byte	3.5/3.78	3.36
Store byte	4.45/4.83	3.89
Move bytes (basic)	4.27	3.75
Additional per byte	4.235	4.05
Move words (basic)	4.27	3.75
Additional per word	1.75	1.68
Compare bytes (basic)	4.27	3.75
Additional per byte	3.5/3.78	3.5/3.78
Compare words (basic)	4.27	3.75
Additional per word	2.87	2.38
Scan for byte (basic)	2.17	1.92
Additional per byte	2.735	2.735
Set or clear bits	5.215	4.48
Test bits (normal/skip)	5.36/5.67	4.73/4.94
Floating point instructions (6 total)		
Add	13.13-27.65	12.91-27.44
Subtract	13.83-29.44	13.61-29.22
Multiply	25.48-35.11	25.27-34.90
Divide	34.02-47.32	33.18-47.11
Fix	4.31-7.6	4.06-7.35
Float	6.97-10.82	6.97-10.82

NOTES:

Fault control memory and dynamic mapping system may each add 0 to 0.14 microseconds to these instruction execution times.

Asynchronous memory may cause variations of ±0.035 μsec per memory reference.

More detailed instruction execution times are supplied in the E-Series reference manual (02109-90014).

Power fail interrupt

Priority: Highest priority interrupt

Power failure: Detects power failure and generates an interrupt to memory location 4 for vector to user-written power failure routine. A minimum of 500 microseconds is provided for execution of the user-written system state save routine.

Microprogrammable processor port

Addressable devices: 2

I/O Lines: 16

Control lines: 9

Maximum burst transfer rate: 11.4 M bytes/sec for 32 bytes.

Maximum continuous transfer rate: 3.18M bytes/sec*

Maximum cable length: 1.2m (4 ft), properly terminated.

**User-microprogram dependent.*

Microprogrammable block I/O

I/O control lines: 3 special lines on I/O backplane

NOTE: Requires user-designed I/O cards

Maximum synchronous transfer rate: 3.18M bytes/sec (input); 2.72M bytes/sec (output).

**User-microprogram dependent.*

Remote program load

Load device selection: 1 of 9 devices in a 2109B; 1 of 14 devices in a 2113B

Loader selection: One of 2 optional loader ROMS.

Operating modes: A) Automatically on power-up; B) Remote forced load with 12966A or 12968A interface (Hardwired); C) Load after certain halts under program control.

Compatibility

Instruction set: The HP 1000 E-Series instruction set is backwards compatible with other HP 1000 and 2100 Series computers.

Program: Most programs written for other HP 1000 and 2100 Series computers are compatible with the HP 1000 E-Series except those with timing loop dependence.

Configuration information

Input/output capacity:	**2109E**	**2113E**
I/O channels in mainframe	9	14
With first extender	25	30
With two extenders	41	46
Standard memory:	**64kb**	**128kb**
Memory capacity		
Memory module spaces		
In Computer only	5	10
In Computer & extender	14	19
Max. non-fault control memory*		
In Computer only	0.640Mb	1.280Mb
In Computer & extender	1.792Mb	2.048Mb
Max. fault control memory*		
In Computer only	0.512Mb	1.024Mb
In Computer & extender	1.280Mb	1.792Mb

**Based on use of 128k byte memory modules.*

Control processor address space

Total address space: 16k 24-bit words

User PROM address space on FAB board: 3.5k*†

WCS overlay address space using 1k WCS boards: 3k**

User PROMs address space using 2k UCS board: 2k**

**Subtract 0.5k each for RTE-IV Extended Memory Area Mapping instructions and DS/1000 firmware, 1k for Scientific Instruction Set, and 1.5k for Dynamic Mapping Instructions and/or Fast FORTRAN Processor.*

†Mounted on 3.5k firmware accessory board under cpu board.

***Mounted on board(s) in cpu I/O backplane, using I/O slots.*

Electrical specifications

AC power required

Line voltage: 88-132V (110V ± 20%); 176-264V (220V ± 20%), with option 015. Input line voltage range is easily changed in the field by moving jumper connections.

Line frequency: 47.5 - 66Hz.

Maximum power required: 625W

Current available (+) required (−) for memory, I/O interfaces and accessories

See power specifications and applicability summary tables, pages 10-0 and 10-1.

Power supply

Storage after line failure: Sustains computer through a line loss of 8 msec when operating at the minimum ac line voltage.

Input line overvoltage protection: Circuit breaker protects against surge caused by connecting computer to twice nominal line voltage.

Input line transients: Withstands power line transients up to ±500V for 50 μsec wide pulse, up to ±1000V for 100 nsec wide pulse, without damage.

Output voltage regulation: ±5%, except −2V is ±10%.

Output protection: All voltages are protected for over-voltage and over current.

Thermal sensing: Monitors internal temperature and automatically shuts down the computer if temperature exceeds specified level.

Safety

Models 2109E and 2113E are recognized by Underwriters Laboratories, Inc. and certified by the Canadian Standards Association (with the exception of Option 015).

Physical characteristics

Dimensions

Width: 48.3 cm (19 in) panel; 42.6 cm (16-3/4 in) behind panel casting.
Depth: 62.2 cm (24-1/2 in) overall; 58.4 cm (23 in) behind panel casting.
2109E Height: 22.2 cm (8-3/4 in).
2113E Height: 31.1 cm (12-1/4 in).

Weight

2109E: 20.4 kg (45 lb).
2113E: 29.5 kg (65 lb).

Ventilation

Air intake is on the left side, exhaust is on the right hand side.

Heat dissipation

580 kilogram-calories/hour (2303 BTU/hour).

Air flow	2109E	2113E
Cubic metres/minute	5.7	7.9
Cubic feet/minute	200	280

Ordering information

2109E Computer

The 2109E includes:

1. 2109B computer.
2. 2102B standard performance memory controller and two 13187B 32k byte standard performance memory modules
3. 12943-16001 and 16002, 24396-12001 through 12003 and 24296-60001 diagnostics and configurator, and 12943-90004, 24396-14001 and 02100-90157 diagnostic and diagnostic configurator manuals.
4. 02109-90001 HP 1000 E-Series reference manual.
5. 02109-90014 HP 1000 E-Series microprogramming manual.
6. 02109-90002 HP 1000 E-Series installation and service manual.

2113E Computer

The 2113E Computer includes:

1. 2113B computer.
2. 12786A 128k byte Standard performance memory package, including 2102B Memory controller, 12747A 128k byte memory module, and 13305A Dynamic mapping system.

3-6. Same as items 3 through 6 of 2109E Computer, above.

2109E and 2113E option

014: Deletes standard memory, item 2, above, from 2109E or 2113E, to permit its replacement with another HP 1000 E-Series compatible standard performance or high performance memory system, with or without fault control, which must be ordered separately.

015 220V (176-264V) operation

2109E and 2113E accessories

See power specifications and applicability summary, pages 10-0 and 10-1, referring to the E-Series applicability column.