HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

HP 21MX E-SERIES COMPUTER

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PREFACE

This manual provides installation and field service instructions for the Hewlett-Packard 21MX E-Series Computer. The HP 21MX E-Series Computer is a high technology product and, because of the product design, a modular replacement philosophy has been implemented to minimize on-site repair time.

Supporting documentation for the HP 21MX E-Series Computer are as follows:

a. *HP 21MX E-Series Computer Operating and Reference Manual*, part no. 02109-90001.

b. *HP 21MX E-Series Computer Installation and Service Manual*, part no. 02109-90002.

c. *HP 21MX E-Series Computer Microprogramming Reference Manual*, part no. 02109-90004.

d. *HP 12979A Input/Output Extender Installation and Service Manual*, part no. 12979-90006.

e. *HP 12979A Input/Output Extender Operating and Reference Manual*, part no. 12979-90007.

f. *HP 12990A Memory Extender Installation and Service Manual*, part no. 12990-90003.

g. *Long Diagnostic Reference Manual*, part no. 24390-90001.

An Engineering Supplement Package, part no. 02109-90007, is also available to those who wish indepth knowledge about the architecture and logic elements of the HP 21MX E-Series Computer. Consult your local Hewlett-Packard Sales and Service Office for details regarding this package. A list of HP Sales and Service Offices is provided at the back of this manual.

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SAFETY CONSIDERATIONS

KEEP WITH MANUAL

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

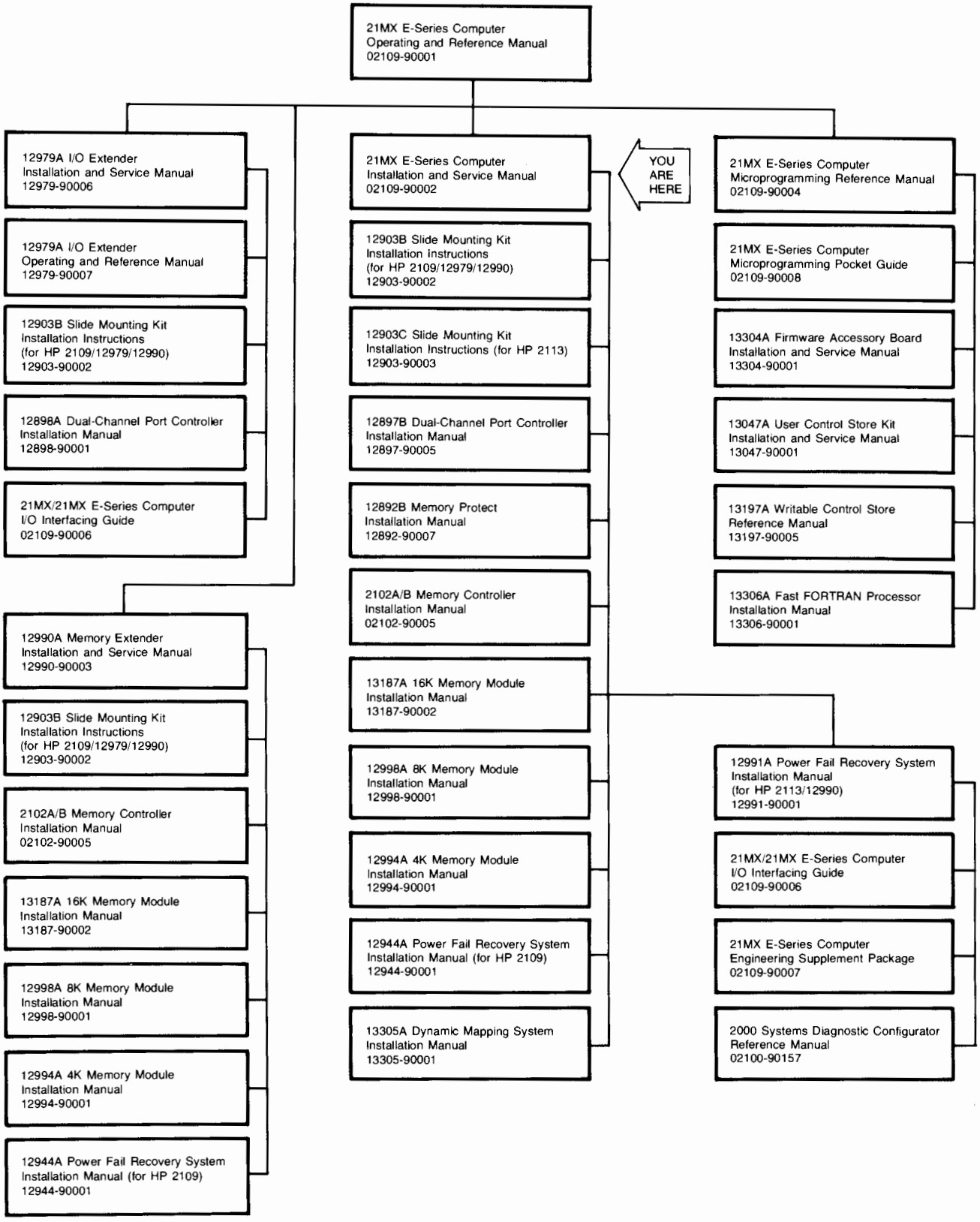
Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

DOCUMENTATION MAP



SECTION I

INSTALLATION

This section provides installation instructions for the computer mainframe. Included in these instructions are site preparation data, unpacking and inspection, configuration requirements, installation procedures, performance verification, and recommended packing and shipping methods.

1-1. SITE PREPARATION

Site preparation information for the computer mainframe includes environmental limitations, power requirements, and mounting considerations. If the computer is purchased as part of a computer system, disregard the contents of paragraphs 1-2 through 1-5 herein and refer instead to the *Hewlett-Packard 2000 Computer Systems Site Preparation Manual*, part no. 02000-90097.

1-2. ENVIRONMENTAL LIMITATIONS

Environmental limitations for operating and nonoperating conditions of the computer are specified in table 1-1. The environmental limitations imposed by peripheral devices and associated components must be taken into consideration when the computer is located in the same area.

Table 1-1. Computer Environmental Limitations

AMBIENT TEMPERATURE

Operating: 0° to 55°C (32° to 131°F)
Nonoperating: −40° to 75°C (−40° to 167°F)

ALTITUDE

Operating: 15,000 feet (4,573 meters)
Nonoperating: 40,000 feet (12,199 meters)

RELATIVE HUMIDITY

20 to 95% at 25° to 40°C (77° to 104°F) without condensation.

1-3. POWER REQUIREMENTS

The computer is shipped with the power supply configured to operate from a single-phase power source of 110 ±20% volts (standard) or 220 ±20% volts (option 015) as specified in the purchase order. Maximum power consumption of the HP 2109A and HP 2113A is 525 watts and 800 watts, respectively. Reconfiguring from 110V ac operation to 220V ac operation (or vice versa) is described in paragraphs 2-59 and 2-60.

Various safety codes require that instrument chassis, panels, and housings be grounded to protect operating and service personnel. A grounded three-conductor female power outlet must be made available to satisfy this requirement.

The computer is shipped without +28V dc at the I/O backplane connectors. If required, +28V dc can be supplied by performing the procedure described in paragraph 1-34.

1-4. COOLING REQUIREMENTS

There are no external cooling requirements for the computer. The internal fans provide adequate ventilation when operated within the environmental limitations specified in table 1-1. Adequate space must be allowed on each side to ensure full intake and exhaust of ventilating air.

1-5. MOUNTING CONSIDERATIONS

The computer may be used either as a freestanding device or mounted in a standard 19-inch (483-millimeter) equipment rack. When used in a mobile environment, the computer should be installed in a shock-mounted equipment rack. Rack-mounting dimensions for the computer are specified in table 1-2.

Table 1-2. Rack-Mounting Dimensions

COMPUTER	HEIGHT	WIDTH*	DEPTH**
HP 2109A	8-3/4 in. (223 mm)	16-3/4 in. (425 mm)	24-1/2 in. (622 mm)
HP 2113A	12-1/4 in. (311 mm)	16-3/4 in. (425 mm)	24-1/2 in. (622 mm)

*Behind rack mount.
**Required rack depth.

1-6. UNPACKING AND INSPECTION

The computer and accessories may be shipped in more than one container. When the shipment arrives, check to ensure the receipt of all containers as specified by the carrier's papers. Inspect each shipping container immediately upon receipt for evidence of mishandling during transit. If any container is damaged, or if any container is waterstained, request the carrier's agent be present when that container is opened.

Open the shipping container(s) and locate the envelope marked "CUSTOMER RECORDS." One of the items in this envelope is a list of equipment supplied. Compare this list against the purchase order to verify that the shipment is correct. Unpack the shipping container(s) and inspect each item for external damage. Look for damage such as broken controls and connectors, dented corners, bent panels, scratches, and loose components. Check also the rigid foam-plastic cushioning (if used) for signs of deformation which could be indicative of rough handling during transit.

If an HP 2109A or HP 2113A Computer is being installed and the computer includes a power fail recovery system, proceed as follows:

a. Loosen screw located in rear fold of top cover.

b. Slide top cover approximately 6 inches (15 centimeters) toward rear of computer to expose battery PCA(s). For HP 2109A Computer, see figure 3-1 index numbers 12A, 12B, and 12C; for HP 2113A Computer, see figure 3-2 index number 12A.

c. Remove foam-plastic shipping block from top of battery PCA(s).

d. Ensure that bettery PCA(s) is seated fully into mating receptacle(s) on lower power supply PCA.

e. Slide top cover into place and tighten screw in rear fold.

If the visual examination reveals any damage to the computer or accessories, follow the damage claim procedure described in paragraph 1-37. Retain the shipping container(s) and packing material for examination in the settlement of claims or for future reuse.

1-7. PHYSICAL INVENTORY

1-8. MANUALS

Check to ensure that all manuals listed in the "CUSTOMER RECORDS" envelope have been received.

1-9. EQUIPMENT

1-10. COMPUTER. The computer model number and serial number are stamped on an identification label affixed to the rear panel. Ensure that both the model number and serial number are identical with those specified in the "CUSTOMER RECORDS" envelope. A typical identification label is illustrated in figure 1-1.

If the computer 220V ac option is specified in the purchase order, it is installed and tested at the factory, and identified by the three-digit number 015 stamped on the identification label. Ensure that this number is identical with that specified in the "CUSTOMER RECORDS" envelope.

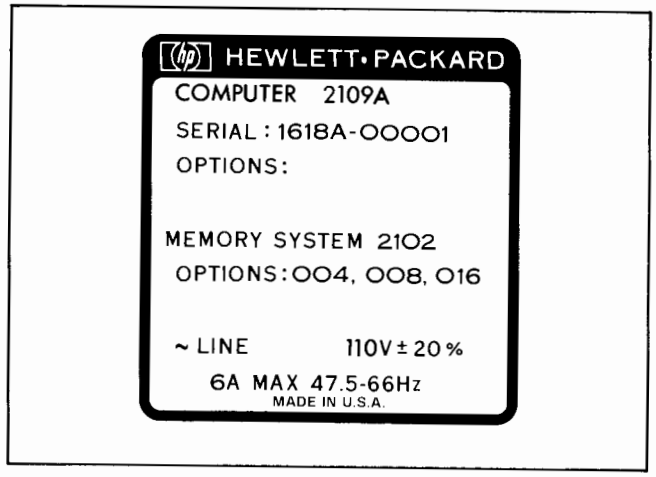


Figure 1-1. Typical Identification Label

1-11. MEMORY SYSTEM. The memory system and memory options specified in the purchase order are installed and tested at the factory. As shown in figure 1-1, the memory configuration is identified by the memory system model number and one or more three-digit option numbers (e.g., 004, 008, 016, . . .). Check these numbers to ensure the inclusion of the proper memory configuration specified in the "CUSTOMER RECORDS" envelope.

Loosen the quarter-turn fasteners on the operator panel, lower the panel assembly to the memory access position, and remove the two memory PCA cage cover retaining screws and lockwashers. Remove the memory PCA cage cover and notice that the memory slot numbers are stamped on the right-hand side of the memory PCA cage. (See figure 1-2.) These slot numbers are allocated to the functions listed in table 1-3, which shows that the memory controller PCA can be installed in any slot from 113 and higher. However, it is recommended that the memory controller PCA be installed in slot 118 for an HP 2109A and slot 123 for an HP 2113A. If an HP 2102 Memory System is installed, the memory module PCA's may be configured for either 4K, 8K, or 16K of memory. Note that only one 4K memory module is allowed per configuration. Verify that all connectors are seated firmly onto the PCA front edge connectors. Replace the memory PCA cage cover and operator panel assembly and tighten the quarter-turn fasteners.

1-12. INPUT/OUTPUT INTERFACES. If input/output (I/O) interface PCA's have been ordered and integrated into the computer system, remove the I/O PCA cage cover at the rear of the computer. (Figure 1-3 shows the rear panel of the computer with the I/O PCA cage cover removed.) Verify that the proper I/O interface PCA's have been furnished in accordance with the purchase order and as specified in the "CUSTOMER RECORDS" envelope. Replace the I/O PCA cage cover.

If I/O interface PCA's have been ordered separately, ensure that they have been furnished with the shipment and in accordance with the purchase order and as specified in the "CUSTOMER RECORDS" envelope.

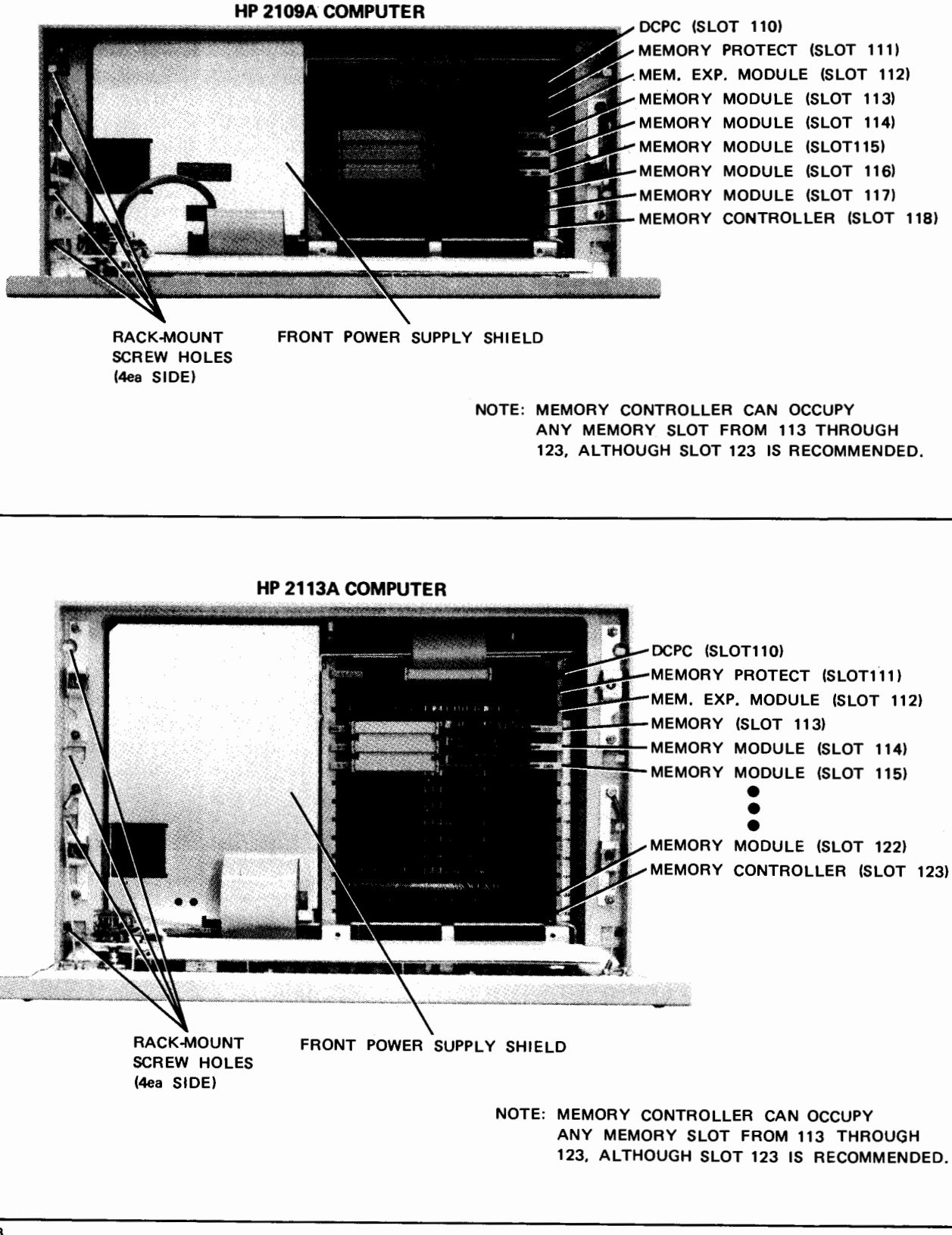


Figure 1-2. Computer Memory PCA Cage (Cage Cover Removed)

Table 1-3. Memory Slot Assignments

HP 2109A SLOT	HP 2113A SLOT	ASSIGNMENT
110	110	Dual-Channel Port Controller
111	111	Memory Protect PCA
112	112	Memory Expansion Module
113	113	Memory Module or Memory Controller
114	114	Memory Module or Memory Controller
115	115	Memory Module or Memory Controller
116	116	Memory Module or Memory Controller
117	117	Memory Module or Memory Controller
118*	118	Memory Module or Memory Controller
—	119	Memory Module or Memory Controller
—	120	Memory Module or Memory Controller
—	121	Memory Module or Memory Controller
—	122	Memory Module or Memory Controller
—	123*	Memory Module or Memory Controller

*Memory Controller must be installed in highest numbered slot (slot 118 for HP 2109A and slot 123 for HP 2113A) when the installation is to include an HP 12990A Memory Extender.

1-13. DIAGNOSTIC PROGRAM TAPES

Check the punched tapes received with the shipment to ensure that all tapes listed in the "CUSTOMER RECORDS" envelope are present.

1-14. CONFIGURATION REQUIREMENTS

1-15. INTERNAL SWITCH SETTINGS

Remove the I/O PCA cage cover and locate the two toggle switches (A1S1 and A1S2) mounted on the rear of the central processor unit PCA. (See figures 1-3 and 1-4.) The position of switch A1S1 determines the action that the computer will take in the event of a parity error (or memory protect violation assuming that a memory protect PCA is installed) and the position of switch A1S2 will enable or disable the power fail/automatic restart capability. The proper setting of each switch depends on whether or not a user-written subroutine will be included to accommodate the required computer action. Therefore, refer to paragraphs 1-16 and 1-17 and then consult with the system programmer to determine the proper switch settings. Programming considerations concerning these switches are given in the *HP 21MX E-Series Computer Operating and Reference Manual*, part no. 02109-90001.

Also mounted on the central processor unit (CPU) PCA are the remote program load (RPL) configuration switches. (See figure 1-5.) These switches are used as follows:

a. Enable the remote program load (RPL) capability.

b. Select one of four loader ROM's.

c. Specify the select code of the loading device.

Configuration of these switches is described in paragraph 1-18.

1-16. PARITY ERROR/MEMORY PROTECT SWITCH A1S1. The action that the computer will take when a parity error or a memory protect violation occurs is determined by the following alternative switch settings:

NOTE

Memory protect is an accessory available with the HP 2109A and HP 2113A Computers. As shown in table 1-3, the memory protect PCA is dedicated to memory slot 111.

a. HALT. When switch A1S1 is in the HALT position and a parity error is detected during a read cycle, the computer will halt and light the PARITY indicator on the operator panel. The PARITY indicator will remain lighted until the PRESET switch is pressed.

b. INT/IGNORE. When switch A1S1 is in the INT/IGNORE position and a parity error or a memory protect violation occurs, the computer will take one of the following two actions depending on whether or not the memory protect PCA is installed:

(1) If the memory protect PCA is installed and not disabled by a CLF 05 instruction, an interrupt to memory location 00005 is generated.

(2) If the memory protect PCA is not installed, or if the memory protect PCA is installed but the parity error logic has been disabled by a CLF 05 instruction, the parity error will be ignored and the PARITY indicator will light.

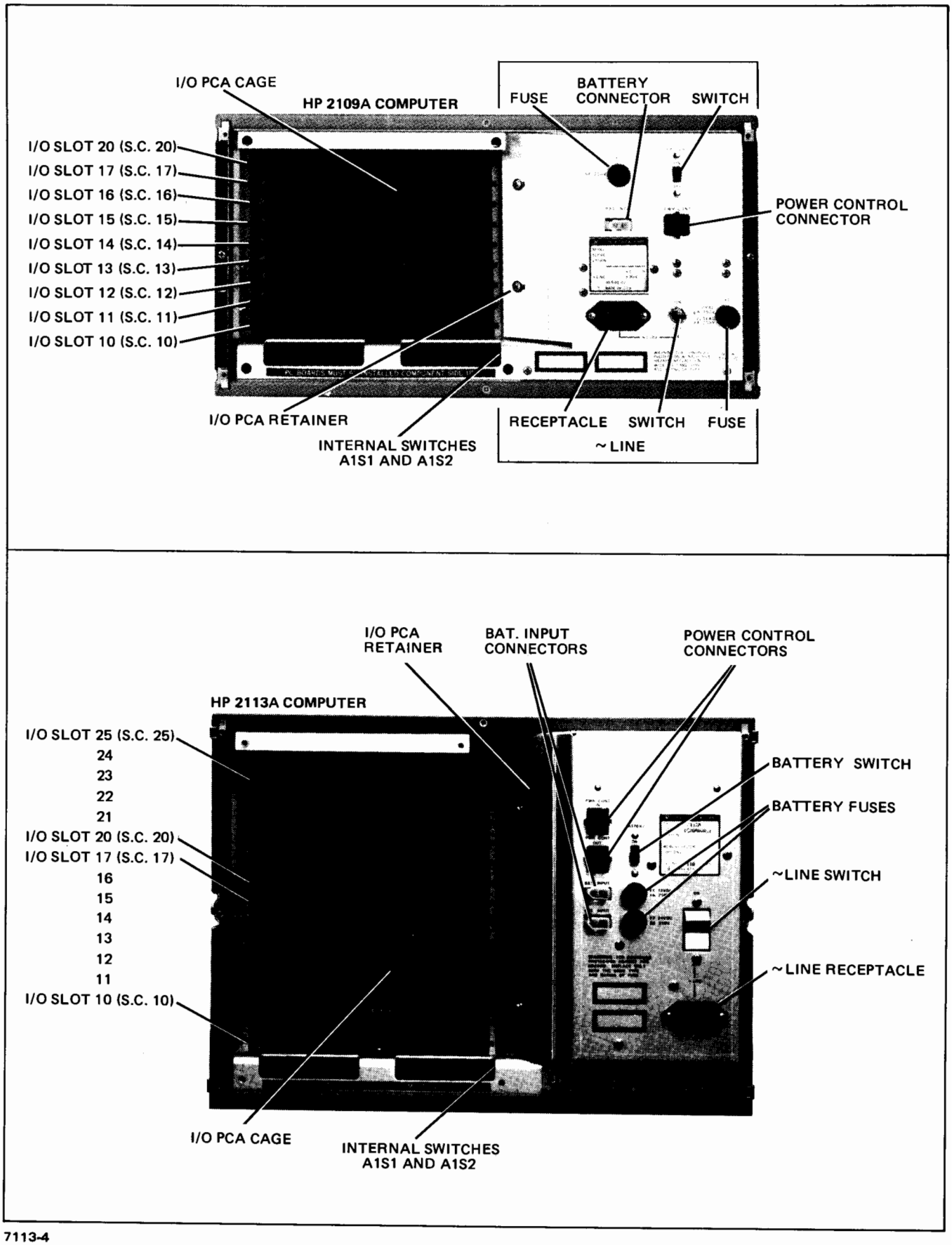


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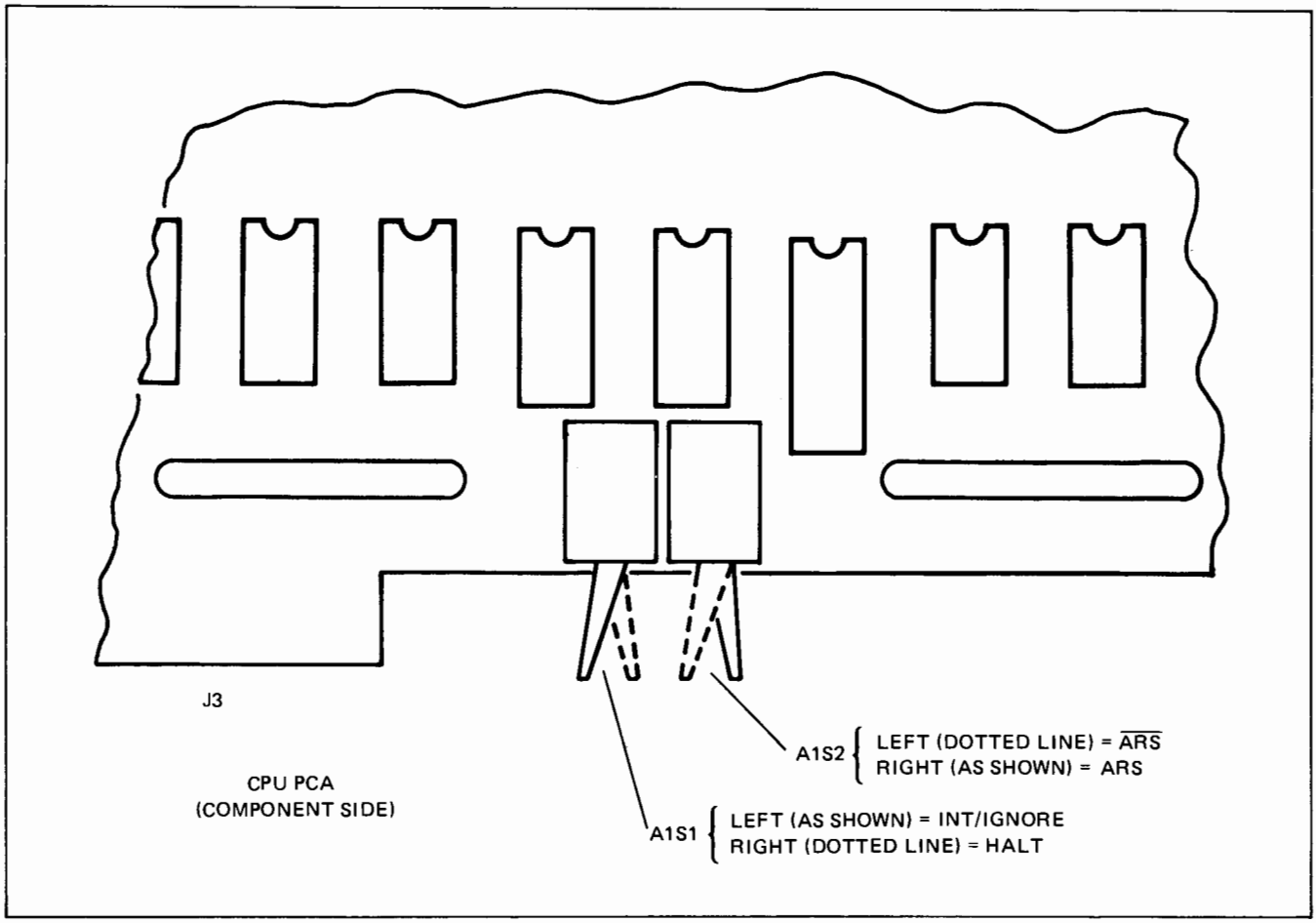
Figure 1-3. Computer I/O PCA Cage and Rear Panel



7113-5

Figure 1-4. Internal Switch Configuration

1-17. AUTOMATIC RESTART SWITCH A1S2. The action that the computer will take upon the restoration of primary power (following a momentary or prolonged power failure) is determined by the following alternative switch settings:

a. ARS. The automatic restart feature is enabled when switch A1S2 is in the ARS position. After a built-in time delay of about half a second following the return to normal power levels, the computer will go into the RUN mode and interrupt to memory location 00004_8 provided that the memory was sustained. This permits entry into a restart program. The POWER FAIL indicator will light when power is restored regardless of whether or not memory was sustained.

b. $\overline{\text{ARS}}$. The automatic restart feature is disabled when switch A1S2 is in the $\overline{\text{ARS}}$ position. The computer is halted immediately regardless of whether the computer was running or halted when the power failure occurred.

1-18. REMOTE PROGRAM LOAD CONFIGURATION SWITCHES. As shown in figure 1-5, the remote program load (RPL) configuration switches consist of eight miniature rocker switches mounted on the CPU PCA at location U173S1-S8. These switches are shipped from the factory unconfigured and set to the closed position. The user does not need to alter the RPL configuration switches if the RPL feature is not to be employed. If the RPL capability is desired, these switches are set to match the system's bootstrap loader configuration as follows:

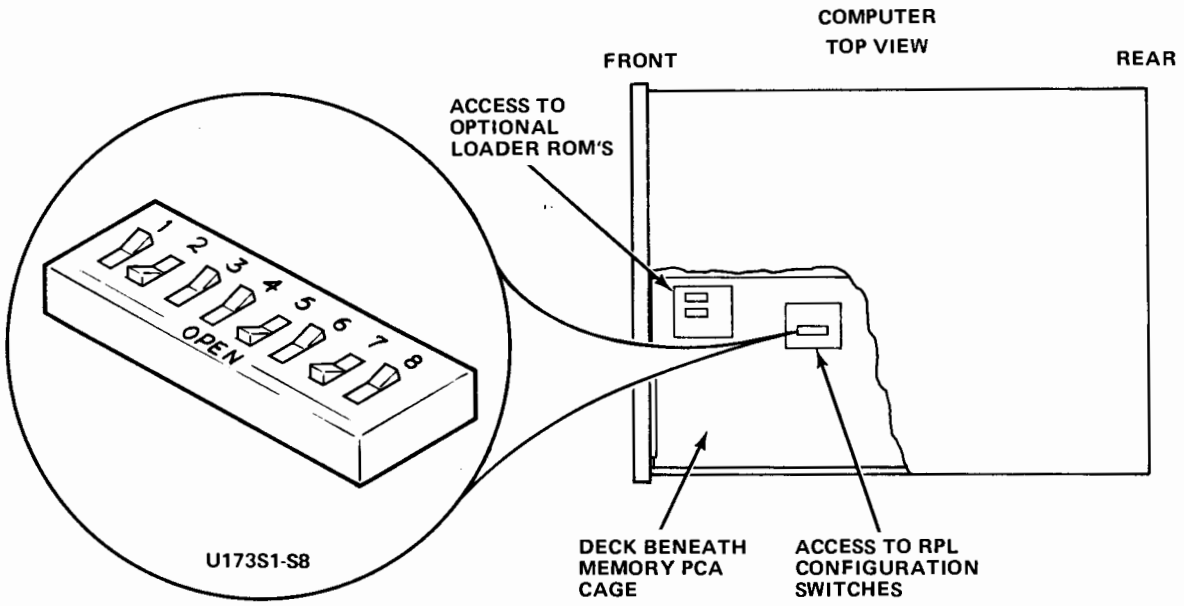
NOTE

All contents of the memory will be lost when a PCA is removed from or installed in the memory PCA cage. Therefore, before turning off line and battery power, ensure that any memory contents to be saved are stored in another device for later retrieval.

a. Set ~LINE and BATTERY switches to OFF.

b. Loosen quarter-turn fasteners on operator panel and lower it to the access position.

c. Remove the two screws and lockwashers securing memory PCA cage cover to the memory PCA cage; remove memory PCA cage cover.



TYPICAL CONFIGURATION

SWITCH	FUNCTION
U173S1	Open position (as shown) enables remote program load (RPL) capability; closed position selects standard operator panel capability.
U173S2 (LSB) U173S3 U173S4 U173S5 U173S6 (MSB)	Decodes the five bit octal select code of the input device (S.C. 10-37). Switches shown set to select code 11_8 (01001_2).
U173S7 U173S8	Selects one of four loader ROM's. Select desired loader ROM as follows:

SWITCHES		LOADER SELECTED
U173S8	U173S7	
0	0	Standard paper tape loader ROM
1	0	Standard disc loader ROM
0	1	Optional loader ROM 0
1	1	Optional loader ROM 1

Switches shown set to loader ROM 0.

Note: Open position = logic 0
Closed position = logic 1

7113-6

Figure 1-5. Remote Program Load Configuration Switches

d. Disconnect cable assembly from all memory PCA's and DCPC cable assembly (if installed) from DCPC PCA.

e. Remove all PCA's from memory PCA cage by pulling outward on extractor levers.

f. At bottom of memory PCA cage, locate opening in deck for the RPL configuration switches (U173S1-S8). (See figure 1-5.)

g. Consult with the system programmer and configure the RPL configuration switches to match the system's bootstrap loader configuration.

Figure 1-5 gives the function of each switch and an example of a typical configuration. The RPL capability is selected by switch U173S1 set to the open position. The input/output (I/O) select code of the input device (e.g., photo reader, magnetic tape, disc, or system console) is configured as select code 11 (octal) by switches U173S2 through U173S6. Loader ROM 0 is selected by switches U173S7 and U173S8.

After setting the RPL configuration switches, replace all PCA's in memory PCA cage, reconnect cable assemblies, and reinstall memory PCA cage cover and operator panel.

1-19. I/O PRIORITY ASSIGNMENT

Each peripheral device in the system must be connected to the computer through an interface PCA installed in the I/O PCA cage. A priority chain connects all interface PCA's in series to prevent simultaneous interrupt requests from two or more peripherals. The priority of the interface PCA is determined by the I/O slot that the PCA occupies, with slot 10 (select code 10_8) having the highest priority; the highest numbered I/O slot has the lowest priority. (See figure 1-3.) Interrupts from a higher priority device inhibit lower priority interrupts by breaking the priority chain. If the interrupt mode is used, there can be no vacant slots from select code 10_8 to the highest select code used due to the priority chaining scheme.

From a standpoint of time, it is more economical to assign the higher priorities to high-speed devices. However, if a subsystem could suffer catastrophic information loss if not serviced immediately, then that subsystem should be assigned the highest priority regardless of speed.

Refer to the individual interface or subsystem documentation for installation details concerning I/O PCA jumper assignments (if any) and priority considerations. Then confer with the system programmer to establish the desired I/O device priority and configure the I/O PCA cage accordingly.

1-20. INSTALLATION PROCEDURE

1-21. MANUAL UPDATING

Before installing the computer, perform any updating that may be required for the HP 21MX E-Series Computer documentation. (A list of directly related hardware and software documentation is provided in the preface to this manual.) Updating instructions (if any) are provided in a supplement supplied with the appropriate document.

1-22. TOOLS AND TEST EQUIPMENT REQUIRED

1-23. TOOLS. No installation tools other than ordinary handtools are required.

1-24. TEST EQUIPMENT. Test equipment required to verify the adequacy of the ac power outlet and the proper adjustments of the computer power supply are listed in table 1-4.

1-25. AC POWER OUTLET AND EXTERNAL GROUND

The female power outlet to be used to supply ac power to the computer must be checked by a qualified electrician to ensure that it furnishes the proper voltage for which the computer is configured. The outlet and its associated wiring and fuses (or circuit breakers) must be capable of carrying the current specified on the identification label on the computer rear panel. (See figure 1-1.)

Figures 1-6 and 1-7 illustrate and provide the necessary details of the various ac power cord configurations. If the computer is to be installed in a building, make sure that the local electrical code permits the use of the type of power cord furnished with the computer.

Have a qualified electrician check the power outlet with an ac voltmeter to ensure that the required single-phase voltage is present. If the computer is configured for 110-volt operation, the line voltage must be in the range of 88 to 132 volts ac (rms); for 220-volt operation, the line voltage must be in the range of 176 to 264 volts ac (rms). Bear in mind that the electrical load imposed by the computer and its accessories may reduce the line voltage below the no-load value.

If the line voltage is in the correct range, have the electrician also check the power outlet to ensure that it is wired correctly with respect to ac high potential, ac neutral, and earth ground. If the outlet is wired improperly, correction must be made by a qualified electrician. Local electrical codes must be observed if the installation is inside a building.

For safety reasons, it is *mandatory* that a connection be made between the computer chassis and earth ground. For installation in a mobile environment (e.g., ship, aircraft, or train), the earth ground wire in the computer ac power cord must be connected to the hull or metal frame of the vehicle.

Table 1-4. Installation Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Digital Voltmeter	At least four-digit readout. Minimum input impedance 10 megohms; full-scale ranges of 0.999 and 99.99 volts dc.	HP 3439A Digital Voltmeter with HP 3441A Range Selector.
AC Voltmeter	Expanded-scale or digital-readout type capable of measuring ac line voltage to ±1.0%. Voltage range must be from 88 to 132 volts ac (standard) or 176 to 264 volts ac (option 015).	HP 3445 AC/DC Range Unit. (Also performs functions of HP 3441A Range Selector listed above. Requires an HP 3449A Digital Voltmeter.)
Variable Autotransformer	Capable of reducing computer input line voltage to 80 volts ac (standard) or 160 volts ac (option 015); rated at least 1100 voltamperes.	None.
Vacuum Device	Hand-operated vacuum device to remove molten solder.	Soldapulldt DS017 (HP part no. 8690-0060).

1-26. COMPUTER MOUNTING

1-27. BENCH MOUNTING. As stated in paragraph 1-5, the computer may be used as a freestanding instrument in a land-based environment. The only consideration here is that adequate space be allowed on each side to ensure full intake and exhaust of ventilating air and that all covers are installed. Bear also in mind that a minimum 12 inches (30.5 centimeters) of clearance behind the computer rear panel is required when removing and installing input/output interface PCA's.

1-28. RACK MOUNTING. The following chassis slide kits are available for rack mounting the computers:

COMPUTER	CHASSIS SLIDE KIT
HP 2109A	HP 12903B
HP 2113A	HP 12903C

If a chassis slide kit has been ordered, mount the components to the sides of the computer and to the inside of the rack according to the instructions furnished with the kit. Then install the computer in the rack and secure the computer in place with screws inserted through the mounting holes identified in figure 1-2. The HP 2109A is light enough to allow installation in the rack without being supported by any means other than the rack-mounting screws; however, it is strongly recommended that additional support be provided by chassis slides or slide rails. It is recommended that the HP 2113A be supported by chassis slides or slide rails.

WARNING

Ensure cabinet or system stability before extending computer on its chassis slides.

1-29. POWER SUPPLY CHECK

Verify the tolerances of the various power supply voltages and the setting of the power fail threshold as described in the following paragraphs.

1-30. HP 2109A POWER SUPPLY ACCURACY. Energize the digital voltmeter and allow sufficient warmup to reach its rated accuracy. Plug the computer power cord into the power outlet and proceed as follows:

a. Loosen the two quarter-turn fasteners on operator panel and lower it to the access position. Remove memory PCA cage cover.

WARNING

Hazardous voltages are exposed when the front power supply shield is removed.

b. Remove the three screws and lockwashers securing front power supply shield to computer mainframe.

c. Disconnect key-operated switch assembly cable from lower power supply PCA connector and remove front power supply shield. Reconnect key-operated switch assembly cable.

d. On computer rear panel, set ~LINE switch to ON.

e. On operator panel, rotate key-operated switch to R (reset) and then to OPERATE.

f. Connect positive lead of digital voltmeter to J8-5 (+5V test point) and connect common lead to J8-2 (common test point). (See figure 1-8.)

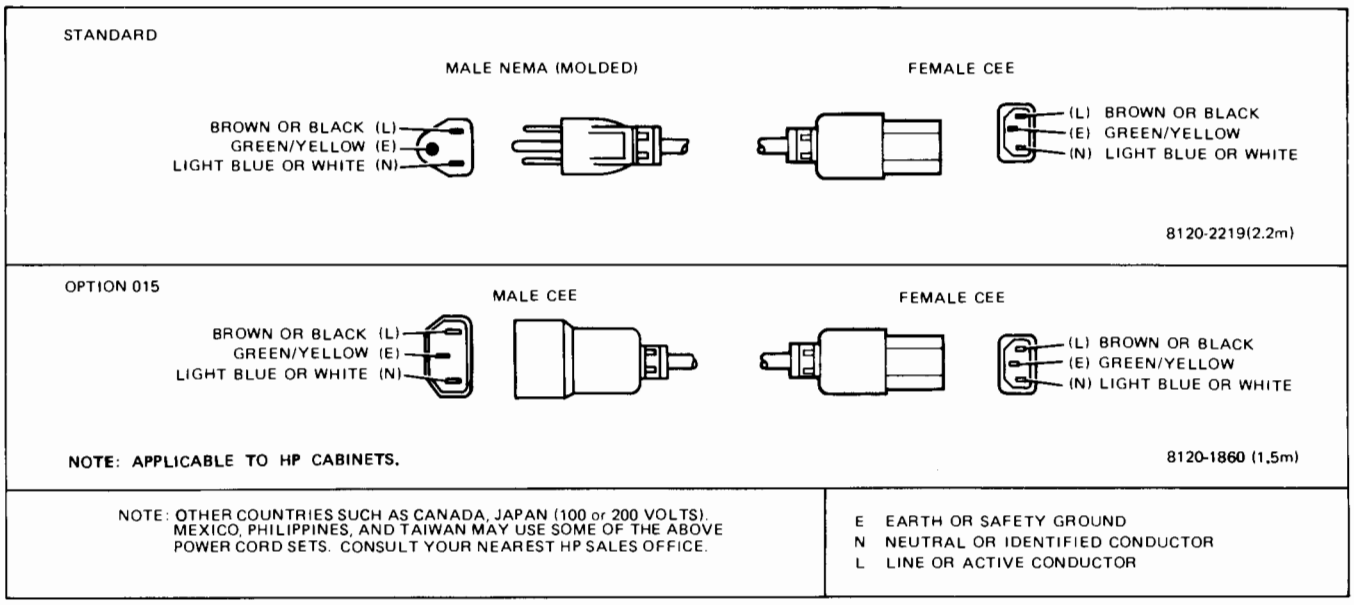


Figure 1-6. AC Power Cord Sets (USA)

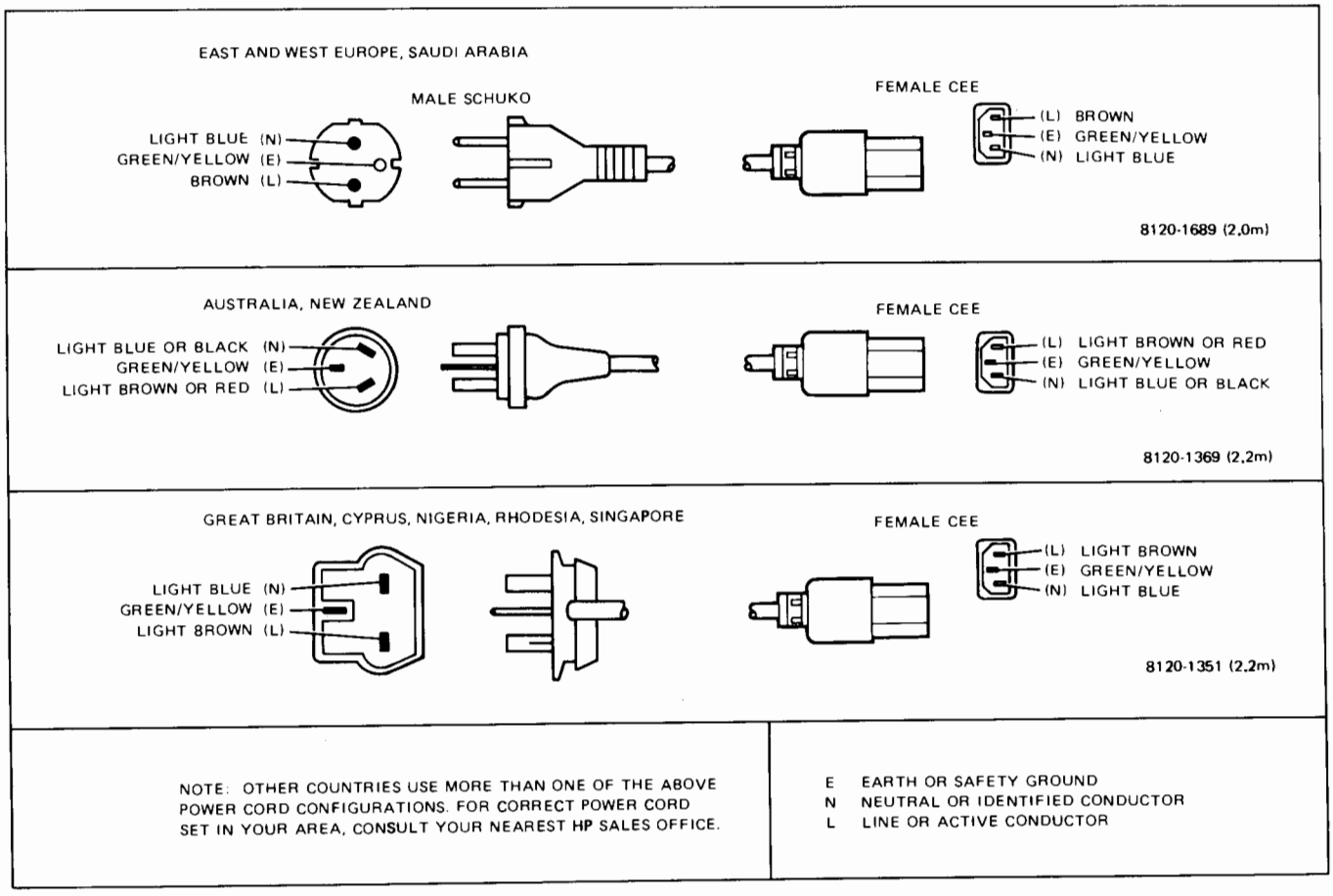


Figure 1-7. AC Power Cord Sets (Non-USA)

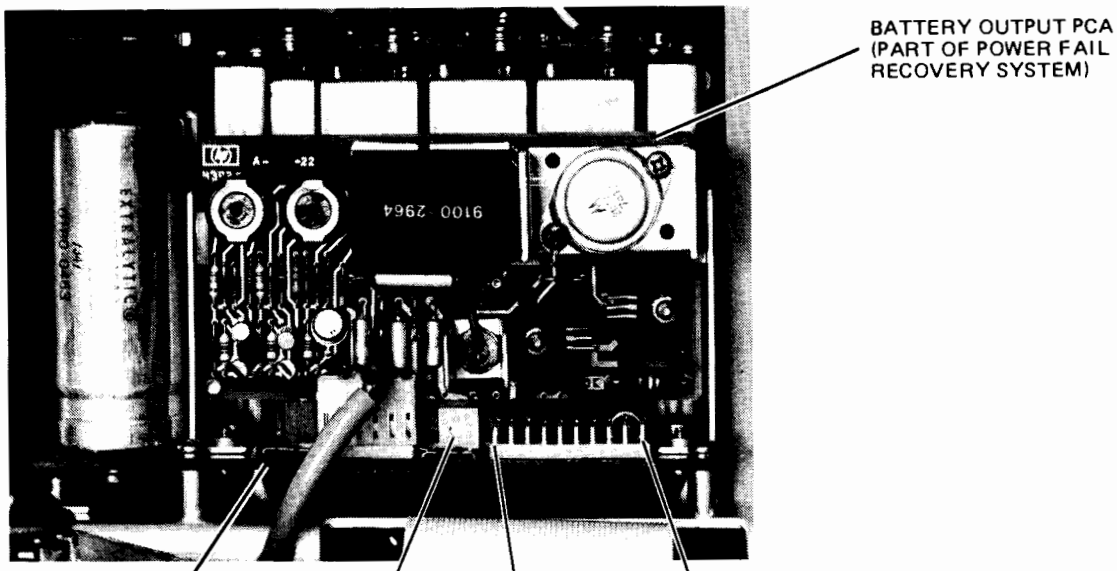


Figure 1-8. HP 2109A Computer Power Supply Field Adjustment and Test Points

g. Adjust +5V ADJ potentiometer to obtain voltmeter indication of +5.00 ±0.05 volts.

h. Check tolerances of the remaining supplies; test points and tolerances are listed in table 1-5.

i. Set key-operated switch to STANDBY and set ~LINE switch to OFF.

j. Disconnect voltmeter and key-operated switch assembly cable. Replace front power supply shield and reconnect key-operated switch assembly cable.

k. Replace memory PCA cage cover.

l. Replace operator panel assembly and tighten the two quarter-turn screws.

NOTE

If one or more power supplies are out of tolerance, notify the nearest Hewlett-Packard Sales and Service Office. A list of Sales and Service Offices is provided at the rear of this manual.

Table 1-5. HP 2109A Computer Power Supply Voltage Tolerances

SUPPLY	TEST POINT*	TOLERANCE
−12V	J8-1	±0.6V
Common	J8-2	—
+12V	J8-3	±0.6V
−2.3V	J8-4	±0.2V
+5V	J8-5	±0.25V
+5VM	J8-6	±0.25V
V+ (BAT)	J8-7	—
$\overline{\text{PUUP}}$	J8-8	—
+12VM	J8-9	±0.6V
−12VM	J8-10	±0.6V

*J8 is mounted on lower power supply PCA.

1-31. HP 2113A POWER SUPPLY ACCURACY. Energize the digital voltmeter and allow sufficient warmup to reach its rated accuracy. Plug the computer power cord into the power outlet and proceed as follows:

a. Loosen the four quarter turn fasteners on operator panel and lower it to the access position. Remove memory PCA cage cover.

WARNING

Hazardous voltages are exposed when the front power supply shield is removed.

b. Remove the three screws and lockwashers securing front power supply shield to computer mainframe. Remove the one screw and lockwasher attaching shield to battery PCA guide.

c. Disconnect key-operated switch assembly cable from lower power supply PCA connector and remove front power supply shield. Reconnect key-operated switch assembly cable.

d. On computer rear panel, set ~LINE switch to ON.

e. On operator panel, rotate key-operated switch to R (reset) and then to OPERATE.

f. Connect positive lead of digital voltmeter to J6-5 (+5V test point) and connect common lead to J6-2 (common test point). (See figure 1-9.)

g. Adjust +5V ADJ potentiometer to obtain voltmeter indication of +5.00 ±0.05 volts.

h. Connect positive lead of digital voltmeter to J6-6 (+5VM test point). Adjust +5VM ADJ potentiometer to obtain voltmeter indication of +5.00 ±0.05 volts.

i. Check tolerances of the remaining supplies; test points and tolerances are listed in table 1-6.

j. Set key-operated switch to STANDBY and set ~LINE switch to OFF.

k. Disconnect voltmeter and key-operated switch assembly. Replace front power supply shield and reconnect key-operated switch assembly cable.

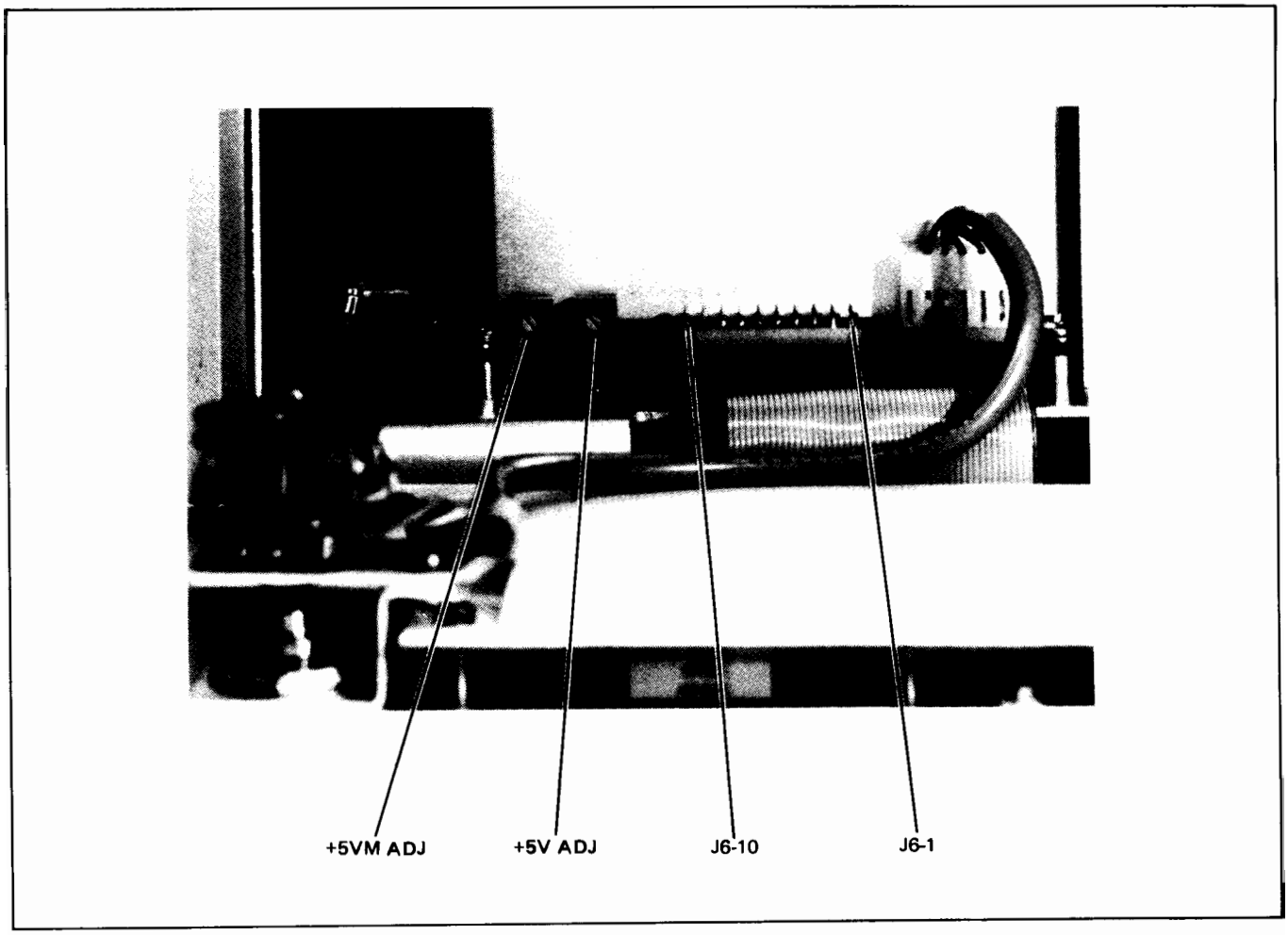


Figure 1-9. HP 2113A Computer Power Supply Field Adjustments and Test Points

l. Replace memory PCA cage cover.

m. Replace operator panel assembly and tighten the four quarter-turn screws.

NOTE

If one or more power supplies are out of tolerance, notify the nearest Hewlett-Packard Sales and Service Office. A list of Sales and Service Offices is provided at the rear of this manual.

Table 1-6. HP 2113A Computer Power Supply Voltage Tolerances

SUPPLY	TEST POINT*	TOLERANCE
$\overline{\text{PUUP}}$	J6-1	—
Common	J6-2	—
+28V**	J6-3	±2.8V
−2.3V	J6-4	±0.2V
+5V	J6-5	±0.25V
+5VM	J6-6	±0.25V
+12VI/O	J6-7	±0.6V
−12VI/O	J6-8	±0.6V
+12VM	J6-9	±0.6V
−12VM	J6-10	±0.6V

*J6 is mounted on lower power supply PCA.

**+28V is present if jumper is installed on upper power supply PCA. (See figure 2-8.)

1-32. POWER-UP THRESHOLD. The computer is shipped with the power-up threshold set at the lower limit of the line voltage configuration. That is, if the computer is configured for 110-volt operation, the power-up threshold is set at 88 volts rms; if the computer is configured for 220-volt operation, the power-up threshold is set at 176 volts rms. If one or more peripheral devices in the computer system will not operate properly when the line voltage drops below say 100 volts rms (standard) or 200 volts rms (option 015), it may be necessary to raise the power-up threshold to this level. Verify and, if desired, re-adjust the power-up threshold as follows:

WARNING

Hazardous voltages are exposed when the top cover is removed and ac power is applied.

a. Loosen the screw in the rear center fold of the top cover. Slide top cover rearward approximately 6 inches (15 centimeters) to access the power-up threshold potentiometer. (See detail A in figure 3-1 or 3-2 as appropriate.)

b. Energize ac voltmeter and allow sufficient warmup to reach its rated accuracy.

c. Connect ac voltmeter leads across autotransformer output. Plug autotransformer power cord into power outlet and set its output to approximately 110 volts rms (standard) or 220 volts rms (option 015).

d. Plug computer power cord into autotransformer power output receptacle. Set computer ~LINE switch to ON and rotate key-operated switch to R (reset) and then to OPERATE.

e. Slowly reduce autotransformer output until all operator panel indicators extinguish, indicating that the computer has switched automatically to the standby mode. The voltmeter should indicate 75 ±5 volts rms (standard) or 150 ±10 volts rms (option 015).

f. If a power fail recovery system is installed, omit this step. If a power fail recovery system is not installed:

(1) Set autotransformer output to 85 ±0.1 volts rms (standard) or 170 ±0.2 volts rms (option 015). Rotate key-operated switch to R (reset) and then to OPERATE. Operator panel indicators should remain extinguished.

(2) Set autotransformer output 87 ±0.1 volts rms (standard) or 174 ±0.2 volts rms (option 015). Rotate key-operated switch to R (reset) and then to OPERATE. Operator panel indicators should light. Proceed with step h.

NOTE

There is up to a 1-second delay from the time that the upper threshold is detected until the operator panel indicators light. Perform the following step very carefully.

g. *Slowly* increase autotransformer output until the operator panel indicators light. The voltmeter should indicate 87 ±0.5 volts rms (standard) or 174 ±1.0 volts rms (option 015).

h. If the upper threshold is not within tolerance, or if it is desired to adjust both thresholds to a higher voltage, continue with step i. Otherwise, disconnect the test setup and continue with the installation.

i. Reduce autotransformer output until operator panel indicators extinguish. Set power-up threshold potentiometer fully clockwise.

j. Set autotransformer output to the desired upper threshold. Adjust power-up threshold potentiometer *slowly* counterclockwise until operator panel indicators light.

k. *Slowly* decrease autotransformer output until operator panel indicators extinguish. The ac voltmeter should indicate 10 to 20 volts lower than the desired upper threshold.

After verifying that the power-up threshold has been properly adjusted, disconnect the test setup, set the ~LINE switch to OFF, and close the top cover.

NOTE

The difference between the upper and lower thresholds varies with the computer configuration. A more heavily loaded computer configuration will change to standby at a higher line voltage than a less heavily loaded configuration, even though both configurations change from standby to operate at the same line voltage.

1-33. INTERFACE PCA

1-34. I/O BACKPLANE DC POWER. If an I/O interface PCA requires +28V dc operating voltage, a jumper (W2) must be installed on the upper power supply PCA. To provide +28V dc to the I/O backplane, proceed as follows:

WARNING

Hazardous voltages are present with the ac power cord connected. Ensure that the ac power cord is disconnected before proceeding.

a. Set ~LINE and BATTERY switches to OFF and remove power cord.

b. Remove top cover of computer.

c. Using a 30W soldering iron, install jumper W2 on the top (circuit) side of the upper power supply PCA as shown in figure 2-8.

d. Check for solder shorts and clean PCA with a flux remover such as Freon TF Degreaser or equivalent.

e. Replace top cover of computer.

1-35. INTERFACE CABLING. Cable requirements to interconnect interface PCA's and associated peripherals are specified in the appropriate interface kit or subsystem documentation. After all interface cables have been assembled, set the key-operated switch to STANDBY, disconnect battery cable(s) if present, and remove the input/output PCA cage cover. Install the hooded connector of each cable onto the edge connector of the interface PCA's. Connect the opposite end of each cable to the appropriate peripheral device, replace the I/O PCA cage cover, and connect the battery cable(s), if present, to the BAT. INPUT connector(s). Set the key-operated switch to OPERATE and, if a power fail recovery system is installed, set the BATTERY switch to ON.

1-36. PERFORMANCE VERIFICATION CHECK

Verify the system installation and operation by running the diagnostic programs outlined in figure 2-1 of this manual. The following hardware is required for the diagnostic:

a. At least 4K of memory.

b. A paper tape reader subsystem.

1-37. CLAIMS PROCEDURE

If the shipment is incomplete or if the equipment is damaged or fails to meet specifications, notify the nearest Hewlett-Packard Sales and Service Office. If damage occurred in transit, notify the carrier also. Hewlett-Packard will arrange for replacement or repair without waiting for settlement of claims against the carrier. In the event of damage in transit, retain the packing carton and packaging materials for inspection.

1-38. REPACKAGING FOR SHIPMENT

CAUTION

When shipping the computer with a power fail recovery system installed, the following procedure must be followed:

a. The battery box cover must be securely fastened to the computer.

b. The battery must be discharged before shipment. This can best be accomplished by disconnecting the power cord, setting the BATTERY switch to ON, and allowing the battery to discharge into memory for approximately 3 hours.

c. After the battery is discharged, disconnect the battery cable(s) from the BAT. INPUT connector(s) and place protective sleeving or masking tape over the battery leads.

d. Place protective sleeving or masking tape over the BAT. INPUT connector(s).

e. Secure the battery PCA(s) in place with either a foam plastic shipping block or with masking tape.

When shipping a power fail recovery system that is not installed in the computer, follow steps b and c above.

1-39. SHIPMENT USING ORIGINAL PACKAGING

The same containers and materials used in factory packaging can be used for reshipment of the computer. Alternatively, containers and packing materials may be obtained from Hewlett-Packard Sales and Service Offices. If the computer is being returned for servicing, attach a tag to the computer specifying the type of service required together with the computer model number and full serial number. Mark the container "FRAGILE" to ensure careful handling. In any subsequent correspondence, refer to the computer by model number and full serial number.

1-40. SHIPMENT USING NEW PACKAGING

The following instructions should be used as a guide when packaging the computer with commercially available materials:

a. Wrap the computer in heavy paper or sheet plastic. If shipping the computer back to Hewlett-Packard, first attach a tag to the computer with the return address and indicating the type of service required. Include the computer model number and full serial number.

b. Use a strong shipping container. A double-wall carton constructed of 350-pound test material is adequate.

c. Use sufficient shock-absorbing material on all sides of the computer to provide a firm cushion and to prevent movement inside the container. Use particular care to protect the computer corners and front and rear panels.

d. Seal the shipping container securely and mark it "FRAGILE".

e. In any subsequent correspondence with Hewlett-Packard refer to the computer by model number and full serial number.

This section includes preventive maintenance; a troubleshooting flowchart for isolating malfunctions to the subassembly level; procedures for removing and replacing the various computer subassemblies; and a listing of the backplane signal sources and destinations, signal mnemonics, and mnemonic definitions. Also included are a simplified block diagram and a power distribution diagram.

2-1. PREVENTIVE MAINTENANCE

The preventive maintenance outlined in table 2-1 should be performed on a bimonthly basis.

Table 2-1. Preventive Maintenance

1.	Clean equipment exterior and interior.
2.	Using digital voltmeter (table 1-4), check power supply voltages as specified in paragraph 1-30 (HP 2109A) or paragraph 1-31 (HP 2113A).
3.	Check fans for proper operation.
4.	Check operation of all operator panel switches and indicators.
5.	Perform verification check as specified in paragraph 1-36.

2-2. TROUBLESHOOTING

2-3. SUBASSEMBLY LEVEL

Computer malfunctions can be isolated to the subassembly level by performing in sequence the procedure presented in figure 2-1. When a malfunction is encountered, replace the first suspect subassembly and repeat that portion of the procedure where the malfunction occurred. (Subassembly removal and replacement procedures are given in following paragraphs.) If the malfunction persists, reinstall the original subassembly, replace the next suspect subassembly, and again repeat the procedure. After the malfunction is cleared, contact the nearest Hewlett-Packard Sales and Service Office for instructions regarding shipment of the defective subassembly.

2-4. COMPONENT LEVEL

Computer subassemblies designated component level replaceable are the operator panel PCA and memory modules. Troubleshooting the defective operator panel PCA down to the faulty component(s) is accomplished by using the parts location and schematic diagrams in figure B-1 while verifying the controls and indicators. (Refer to the *HP 21MX E-Series Computer Operating and Reference Manual*, part no. 02109-90001.) Troubleshooting the defective memory module down to the faulty component(s) is accomplished by performing the self-test firmware or software diagnostics.

2-5. FIRMWARE DIAGNOSTIC. The computer is furnished with a standard microprogrammed base set that includes three tests that quickly test the computer and memory. These firmware diagnostics are not designed as a substitute for more complex software diagnostics and it may frequently be the case that you require a more thorough and detailed testing than provided by these standard self-test routines.

Test 1 tests most of the computer registers and functions. This test will not alter or destroy the contents of any working register or memory. An error condition will set all display register indicator bits (A, B, M, T, P, S) and the overflow register. The execution time is negligible.

Test 2 is a fast microprogrammed memory test that checks the presently enabled memory space (up to 32K words). The microprogram reads each memory location, complements the data and writes it back, reads it, compares it to expected data, then complements it and writes it back into memory. The execution time is negligible and is nondestructive to memory data. An error condition is usually accompanied by a parity error indication and will set all display register indicator bits and clear the overflow register. The A-register will contain the expected (good) data, the B-register will contain the actual (bad) data, and the M-register will contain the logical memory location of the failure.

Test 3 is a significantly more sophisticated microprogrammed memory test. All memory installed in the computer will be tested. Execution time is dependent on the amount of memory installed; approximately one second per 32K words. The display register will increment as memory in each 32K word space is tested. Error reporting is the same as in Test 2 except the S-register will contain the number of the 32K word space where the memory failure occurred.

On a cold power-up (as described below), Tests 1 and 3 will

each be executed once. Pressing the IBL/TEST switch on the operator panel will not only perform the loader function, it will also cause the execution of Tests 1 and 2.

Executing the octal instruction 100000 via the INSTR STEP switch on the operator panel with the key-operated switch in the OPERATE position will execute Tests 1 and 3 once. The information contained in the S-register (when selected) will be the final background pattern used to test memory. This may also be used to easily load the entire memory with the same bit pattern. *While* the tests are executing, the key-operated switch may be set to the LOCK position and the microprogrammed diagnostics will loop continuously until the key-operated switch is returned to the OPERATE position. A memory failure, of course, will terminate the test and report the error.

To check most computer registers and functions and all physical memory, perform the cold power-up procedure as follows:

a. Set key-operated switch to STANDBY. If computer is equipped with an optional power fail recovery system, set BATTERY switch to OFF.

b. Set ~LINE switch to OFF. Wait approximately one second for HP 2109A or six seconds for HP 2113A and then set ~LINE switch to ON.

c. Set BATTERY switch to ON. Rotate key-operated switch first to R (reset), then to STANDBY, and finally to OPERATE.

d. The diagnostic will begin execution and the Display Register can be observed incrementing if a dynamic mapping system (DMS) is installed.

e. Upon successful completion, the T-register will automatically be selected for display.

f. If a computer failure is detected, the Display Register, all six working register indicators (A, B, M, T, P, S), and the OVERFLOW indicator are lighted. Troubleshoot computer failure by performing the procedure presented in figure 2-1.

g. If a memory failure is detected, the Display Register, and all six working register indicators (A, B, M, T, P, S) are lighted and the OVERFLOW indicator is not lighted. The PARITY indicator is lighted for odd number of bit failures and not lighted for even number of bit failures. The S-register will contain the octal number of the 32K word space where the memory failure occurred. To isolate the memory failure, perform the following:

   (1) Select the M-register which contains the logical memory location of the failure.

   (2) Select the A-register which contains the expected (good) data.

   (3) Select the B-register which contains the actual (bad) data.

   (4) Compare bit by bit the A-register with the B-register to isolate the bad bit(s).

   (5) Locate the bad bit(s) in figure B-2, B-3, or B-4 (see Appendix B); replace memory integrated circuit(s) as described in paragraph 2-24.

Figure 2-2 provides an example and reference information to aid in isolating memory failures on a memory module. If further testing is required or if the firmware diagnostic is unable to locate the memory failure, use the software diagnostic procedure described in paragraph 2-6.

2-6. SOFTWARE DIAGNOSTIC. The Semiconductor Memory Diagnostic binary tape, part no. 24395-16001, and *Semiconductor Memory Diagnostic Reference Manual*, part no. 24395-90001, are required if additional testing of computer memory is desired. Procedures for loading and running the diagnostic are given in the reference manual. Included also in the reference manual is a list of error and information halts. To isolate memory failures, perform the diagnostic procedures as outlined in the reference manual.

2-7. SUBASSEMBLY REMOVAL AND REPLACEMENT

WARNING

Hazardous voltages are present inside the computer mainframe. Use extreme care when working around the power supply area. Heed all WARNING — HAZARDOUS VOLTAGE labels.

The following paragraphs, which describe procedures for removing and replacing the various computer and memory system subassemblies shown in figures 3-1 and 3-2, assume that the computer is installed as a freestanding device. If the computer is rack mounted, read the entire subassembly removal procedure and refer to figures 3-1 or 3-2 as appropriate. When it is obvious that the procedure cannot be performed with the computer in the rack, proceed as follows:

a. On the rear panel, set BATTERY and ~LINE switches to OFF; disconnect power cord.

b. Disconnect all I/O cables, including the I/O extender cable if present.

c. Remove computer from rack.

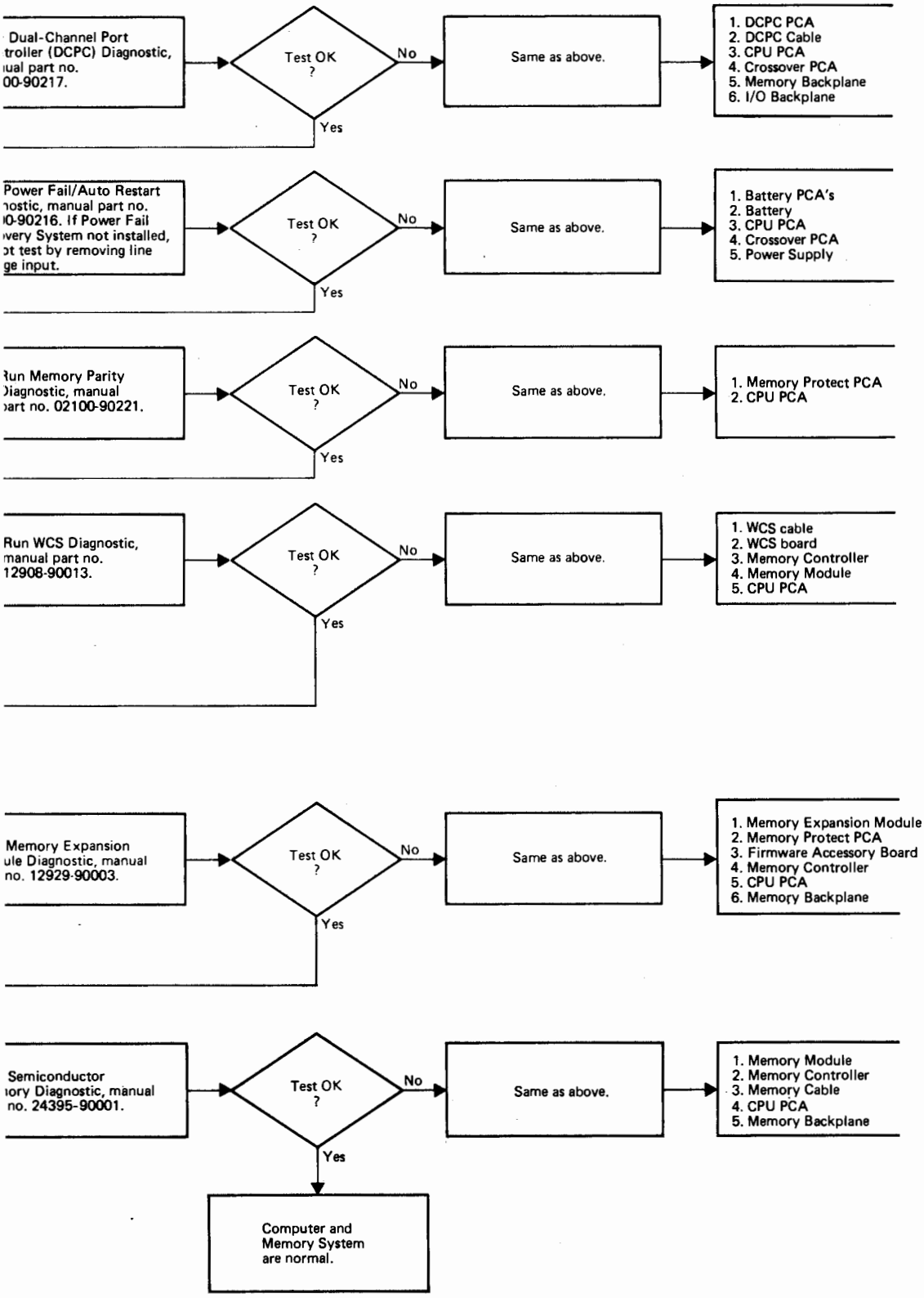
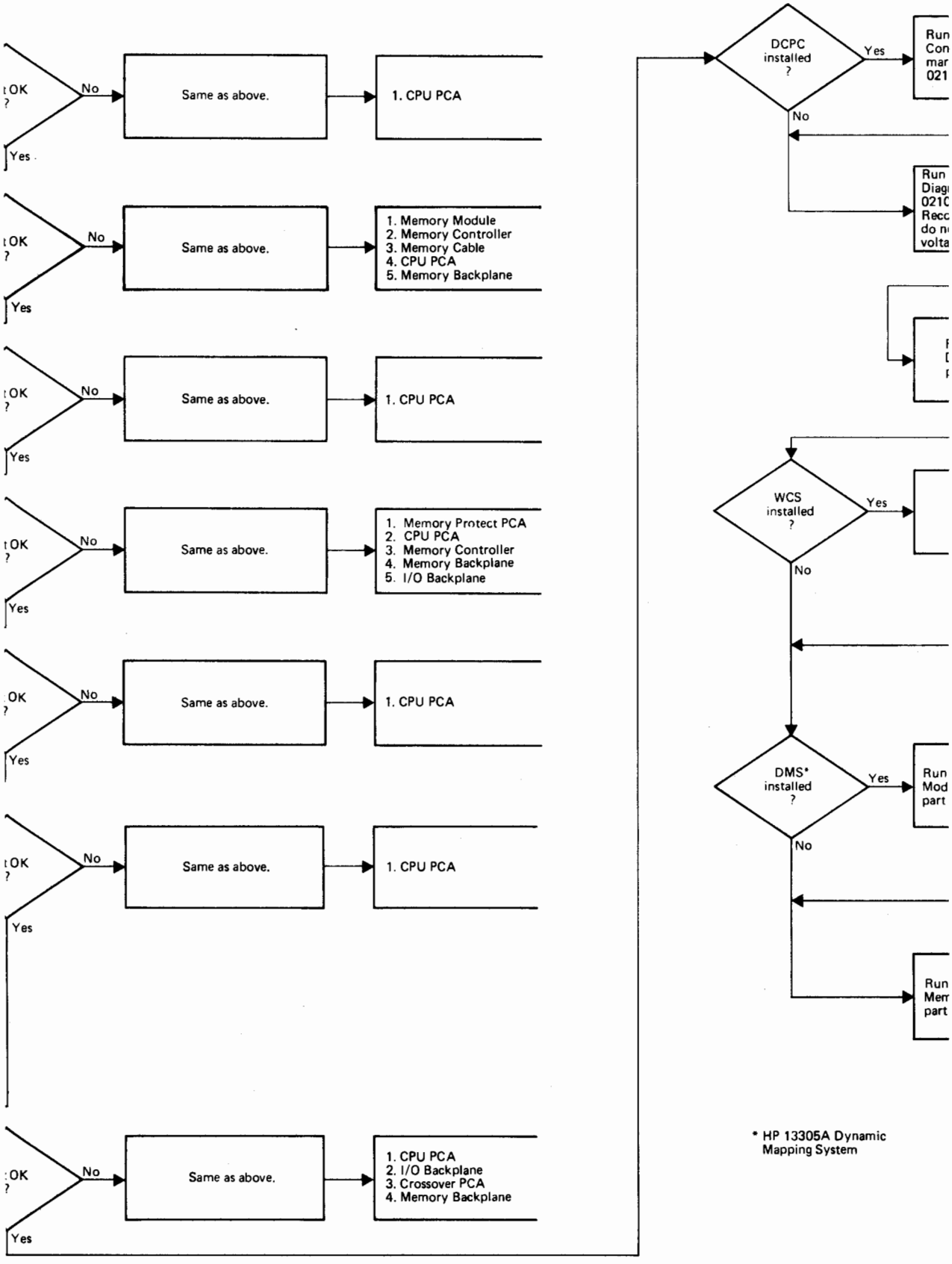
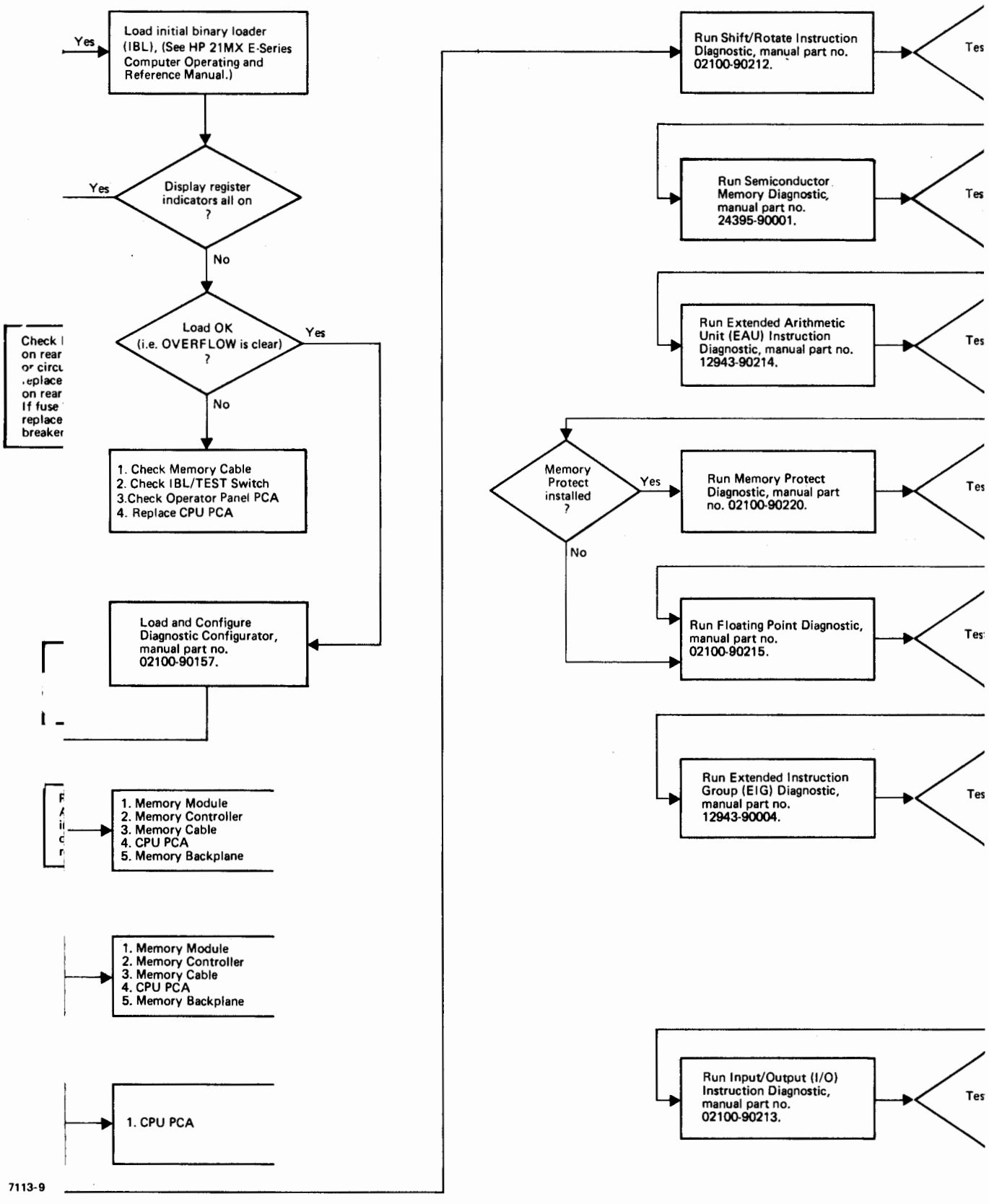
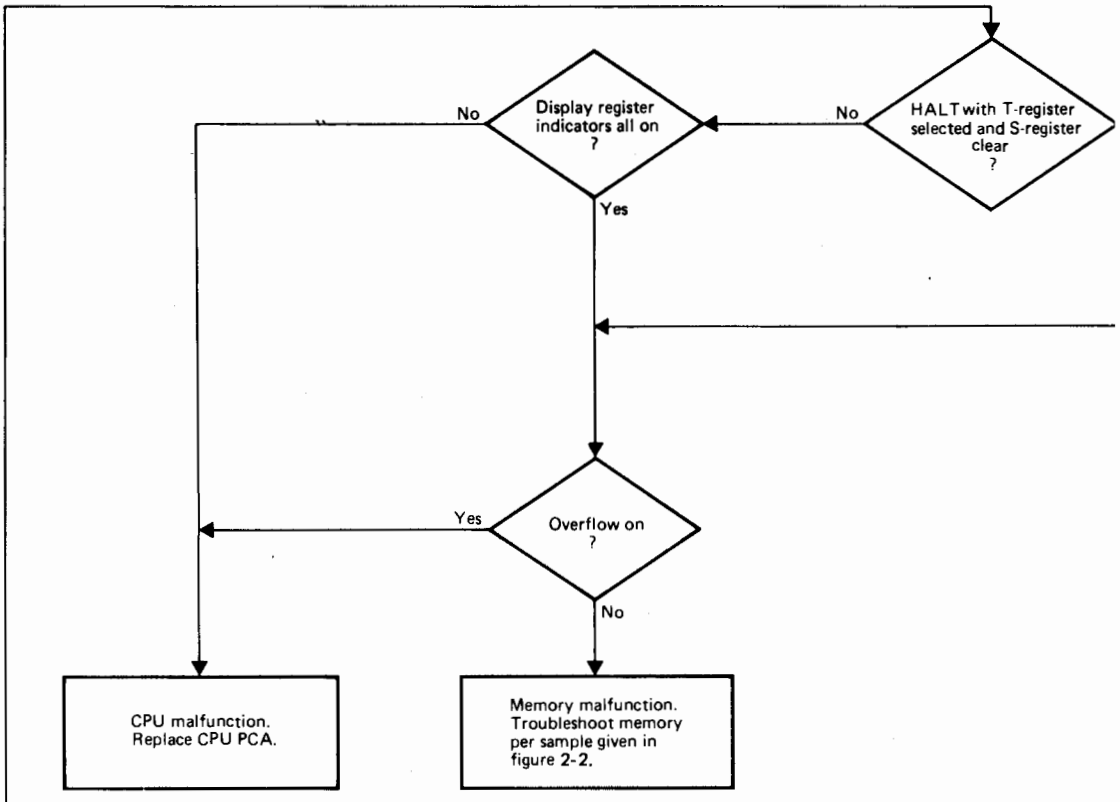


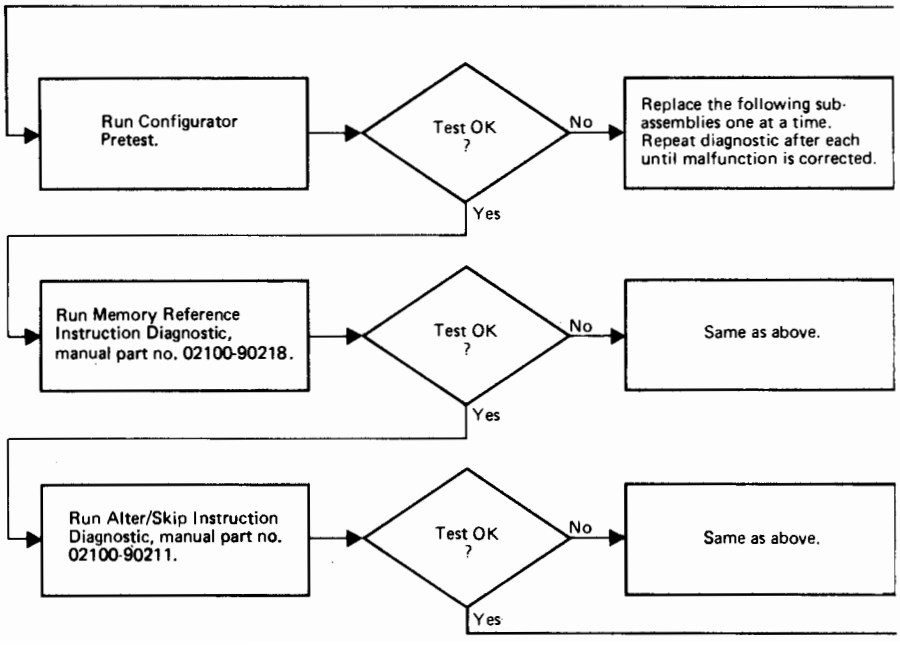
Figure 2-1. Troubleshooting Flowchart

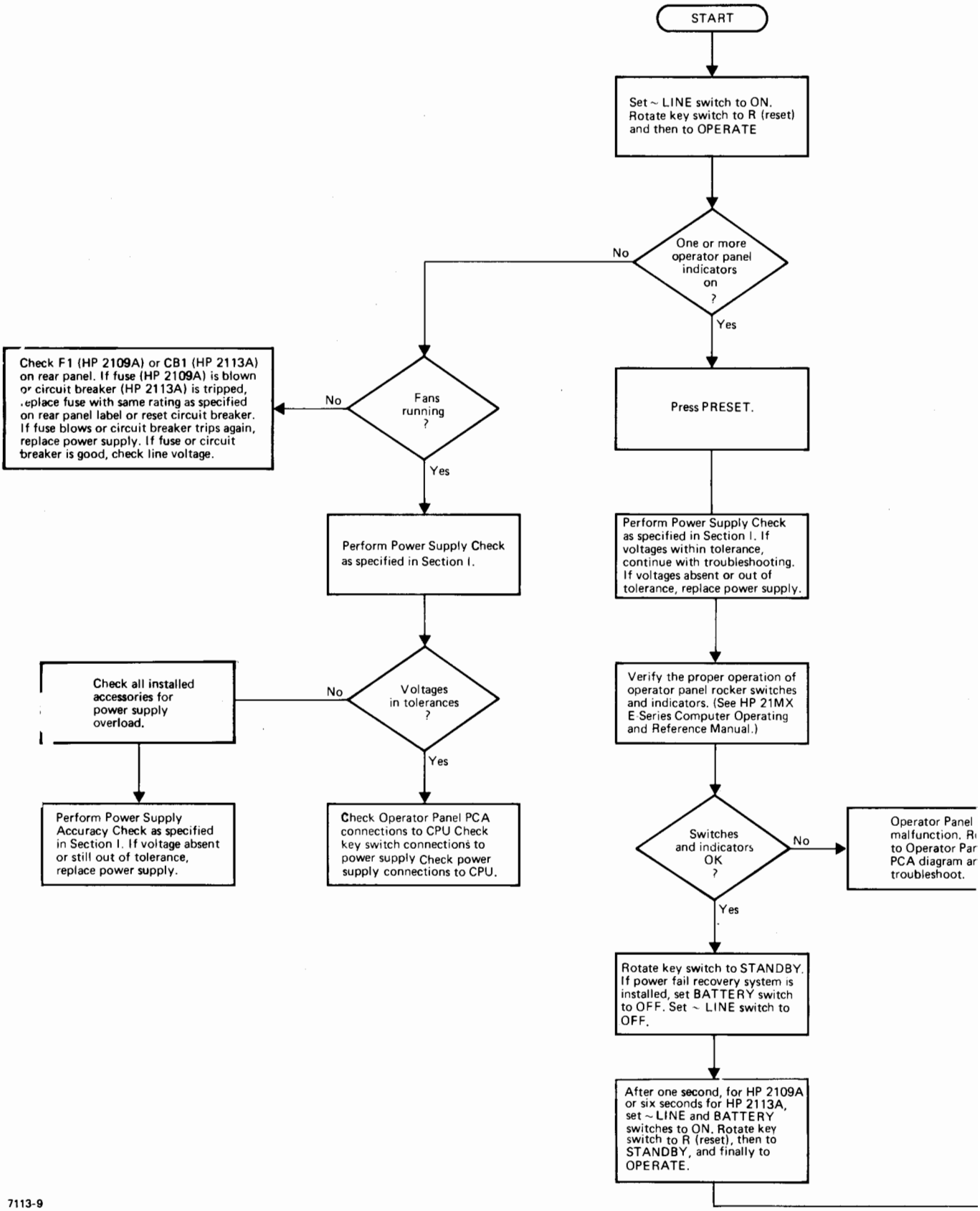


* HP 13305A Dynamic Mapping System


Yes
Load initial binary loader (IBL), (See HP 21MX E-Series Computer Operating and Reference Manual.)
Yes
Display register indicators all on ?
No
Load OK (i.e. OVERFLOW is clear) ?
Yes
No
Check I
on rear
or circu
replace
on rear
If fuse
replace
breaker
1. Check Memory Cable
2. Check IBL/TEST Switch
3.Check Operator Panel PCA
4. Replace CPU PCA
Load and Configure Diagnostic Configurator, manual part no. 02100-90157.
1. Memory Module
2. Memory Controller
3. Memory Cable
4. CPU PCA
5. Memory Backplane
1. Memory Module
2. Memory Controller
3. Memory Cable
4. CPU PCA
5. Memory Backplane
1. CPU PCA
Run Shift/Rotate Instruction Diagnostic, manual part no. 02100-90212.
Tes
Run Semiconductor Memory Diagnostic, manual part no. 24395-90001.
Tes
Run Extended Arithmetic Unit (EAU) Instruction Diagnostic, manual part no. 12943-90214.
Tes
Memory Protect installed ?
Yes
No
Run Memory Protect Diagnostic, manual part no. 02100-90220.
Tes
Run Floating Point Diagnostic, manual part no. 02100-90215.
Tes
Run Extended Instruction Group (EIG) Diagnostic, manual part no. 12943-90004.
Tes
Run Input/Output (I/O) Instruction Diagnostic, manual part no. 02100-90213.
Tes
7113-9


HALT with T-register selected and S-register clear ?
No
Display register indicators all on ?
No
Yes
Overflow on ?
Yes
No
CPU malfunction. Replace CPU PCA.
Memory malfunction. Troubleshoot memory per sample given in figure 2-2.


Run Configurator Pretest.
Test OK ?
No
Replace the following sub-assemblies one at a time. Repeat diagnostic after each until malfunction is corrected.
Yes
Run Memory Reference Instruction Diagnostic, manual part no. 02100-90218.
Test OK ?
No
Same as above.
Yes
Run Alter/Skip Instruction Diagnostic, manual part no. 02100-90211.
Test OK ?
No
Same as above.
Yes


START
Set ~ LINE switch to ON. Rotate key switch to R (reset) and then to OPERATE
One or more operator panel indicators on ?
No
Yes
Press PRESET.
Perform Power Supply Check as specified in Section I. If voltages within tolerance, continue with troubleshooting. If voltages absent or out of tolerance, replace power supply.
Verify the proper operation of operator panel rocker switches and indicators. (See HP 21MX E-Series Computer Operating and Reference Manual.)
Switches and indicators OK ?
No
Operator Panel malfunction. R to Operator Par PCA diagram ar troubleshoot.
Yes
Rotate key switch to STANDBY. If power fail recovery system is installed, set BATTERY switch to OFF. Set ~ LINE switch to OFF.
After one second, for HP 2109A or six seconds for HP 2113A, set ~ LINE and BATTERY switches to ON. Rotate key switch to R (reset), then to STANDBY, and finally to OPERATE.
Fans running ?
No
Check F1 (HP 2109A) or CB1 (HP 2113A) on rear panel. If fuse (HP 2109A) is blown or circuit breaker (HP 2113A) is tripped, replace fuse with same rating as specified on rear panel label or reset circuit breaker. If fuse blows or circuit breaker trips again, replace power supply. If fuse or circuit breaker is good, check line voltage.
Yes
Perform Power Supply Check as specified in Section I.
Voltages in tolerances ?
No
Check all installed accessories for power supply overload.
Perform Power Supply Accuracy Check as specified in Section I. If voltage absent or still out of tolerance, replace power supply.
Yes
Check Operator Panel PCA connections to CPU Check key switch connections to power supply Check power supply connections to CPU.

7113-9

S-REGISTER* BITS 2:0	MEMORY MODULE NUMBERS**
000	0, 1, 2, 3
001	4, 5, 6, 7
010	8, 9, 10, 11
011	12, 13, 14, 15
100	16, 17, 18, 19
101	20, 21, 22, 23
110	24, 25, 26, 27
111	28, 29, 30, 31

*S-register will be zero if DMS is not installed in computer.

**Each module number represents 8K of memory.

In the example shown in the shaded areas, the computer halts on a cold power-up with the register "dots" lighted and with 000003 (octal) in the S-register. This signifies that a memory failure has occurred somewhere in the fourth contiguous 32K block of memory in memory module number 12, 13, 14, or 15.

The M-register is now selected and displays some value between 34000 and 35777 (octal). Examining the memory module column shows that module 13 matches one of the module numbers identified by the S-register. If module 13 is an 8K memory board, the failing address is in the second 4K segment of that board; if module 13 is a 16K memory board, the failing address is in the fourth 4K segment of that board.

Now the A-register is selected and its octal contents noted as shown below. (The A-register will always contain the expected, or good, data.)

Next, the B-register is selected and its contents noted as shown below. (The B-register will always contain the actual data which, in this example, is bad data.)

Finally, a bit-by-bit comparison is made and shows that B-register bit 9 is a logical "1" instead of a logical "0". After module 13 is identified by the jumper configurations shown in figures 2-5 through 2-7, the failing chip associated with bit 9 on that memory module may be replaced.

A-REGISTER (EXPECTED DATA)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	0	0	1	1	0	1	1	1	0	0	1

B-REGISTER (ACTUAL DATA)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	1	1	0	1	1	1	0	0	1

M-REGISTER ADDRESS	MEMORY MODULE NUMBERS	8K MM	16K MM
00000 to 01777 02000 to 03777 04000 to 05777 06000 to 07777	0, 4, 8, 12, 16, 20, 24, 28	1st 4K	1st 4K
10000 to 11777 12000 to 13777 14000 to 15777 16000 to 17777		2nd 4K	2nd 4K
20000 to 21777 22000 to 23777 24000 to 25777 26000 to 27777	1, 5, 9, 13, 17, 21, 25, 29	1st 4K	3rd 4K
30000 to 31777 32000 to 33777 34000 to 35777 36000 to 37777		2nd 4K	4th 4K
40000 to 41777 42000 to 43777 44000 to 45777 46000 to 47777	2, 6, 10, 14, 18, 22, 26, 30	1st 4K	1st 4K
50000 to 51777 52000 to 53777 54000 to 55777 56000 to 57777		2nd 4K	2nd 4K
60000 to 61777 62000 to 63777 64000 to 65777 66000 to 67777	3, 7, 11, 15, 19, 23, 27, 31	1st 4K	3rd 4K
70000 to 71777 72000 to 73777 74000 to 75777 76000 to 77777		2nd 4K	4th 4K

7113-11

Figure 2-2. Memory Chip Malfunction Isolation

2-8. TOP, SIDE, AND BOTTOM COVERS

WARNING

Hazardous voltages are exposed when the covers are removed and ac power applied.

2-9. REMOVAL. Remove the top, side, and bottom cover as follows:

a. Loosen screw located in rear fold of top cover. Slide top cover toward rear and remove.

b. Remove chassis slide(s), if present. On an HP 2109A, loosen screw in rear fold of side cover; slide cover toward rear and remove. On an HP 2113A, remove the two screws and washers from center of side cover; slide cover toward rear and remove.

c. Remove all I/O cables, including I/O extender cable if present. Loosen screw located in rear fold of bottom cover and slide cover toward rear and remove.

2-10. REPLACEMENT. Replace covers in the reverse order of the removal procedure.

2-11. FIRMWARE ACCESSORY BOARD

2-12. REMOVAL. Set the ~LINE and BATTERY switches to OFF, remove the bottom cover, and proceed as follows:

a. Disconnect the connector assembly from firmware accessory board and CPU PCA.

b. Remove the four screws and lockwashers securing firmware accessory board to CPU PCA and remove.

2-13. REPLACEMENT. Replace firmware accessory board in reverse order of the removal procedure.

2-14. CENTRAL PROCESSOR UNIT PCA

2-15. REMOVAL. Set the ~LINE and BATTERY switches to OFF, remove the bottom cover, and proceed as follows:

a. Disconnect operator panel cable assembly from CPU PCA front edge connector; remove firmware accessory board (if installed) and connector assembly.

b. Remove the 12 screws and lockwashers securing CPU PCA to bottom of computer mainframe.

c. Remove the three nuts and six washers from power terminals located in center of CPU PCA. (See figure 2-3.)

d. Carefully disengage CPU PCA from memory and I/O backplanes.

2-16. REPLACEMENT. Install CPU PCA in the computer mainframe as follows:

a. Carefully insert power terminals in center of CPU PCA as shown in figure 2-3. Secure power terminals to CPU PCA with the three nuts and six washers.

b. Position CPU PCA with receptacles A1XA4 and A1XA5 in contact with I/O backplane and memory backplane connectors.

c. Press inward on back of A1XA4 and A1XA5 to seat backplanes fully into CPU PCA receptacles.

d. Replace the 12 screws and lockwashers securing CPU PCA to bottom of computer mainframe.

e. Replace the firmware accessory board (if installed) and connector assembly, and connect operator panel cable assembly to CPU PCA front edge connector. Replace bottom cover.

f. Set ~LINE and BATTERY switches to ON.

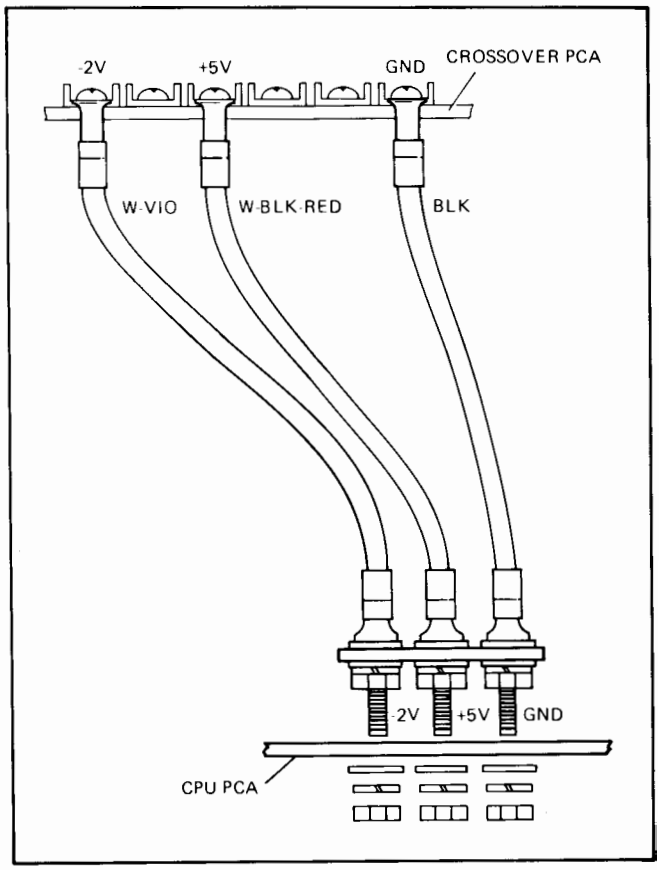


Figure 2-3. CPU Power Connections

2-17. OPTIONAL LOADER ROM'S

Optional loader ROM's, if installed, are mounted in 16-pin IC sockets on the component side of the CPU PCA. (See figure 2-4.) Optional loader ROM's may be removed or replaced by performing the following:

CAUTION

Optional loader ROM's may be damaged if ac power is present when removing or replacing ROM's.

NOTE

All contents of the memory will be lost when a PCA is removed from or installed in the memory PCA cage. Therefore, before turning off line and battery power, ensure that any memory contents to be saved are stored in another device for later retrieval.

a. Set ~LINE and BATTERY switches to OFF.

b. Loosen quarter-turn fasteners on operator panel and lower it to the access position.

c. Remove the two screws and lockwashers securing memory PCA cage cover to the memory PCA cage; remove memory PCA cage cover.

d. Disconnect cable assembly from all memory PCA's and DCPC cable assembly (if installed) from DCPC PCA.

e. Remove all PCA's from memory PCA cage by pulling outward on extractor levers.

f. At bottom of memory PCA cage, locate opening in deck for the optional loader ROM sockets. (See figure 2-4.)

g. Remove or replace optional loader ROM integrated circuit(s). Ensure that the ROM integrated circuit is oriented with the notched end facing in the same direction as the other integrated circuits on the CPU PCA.

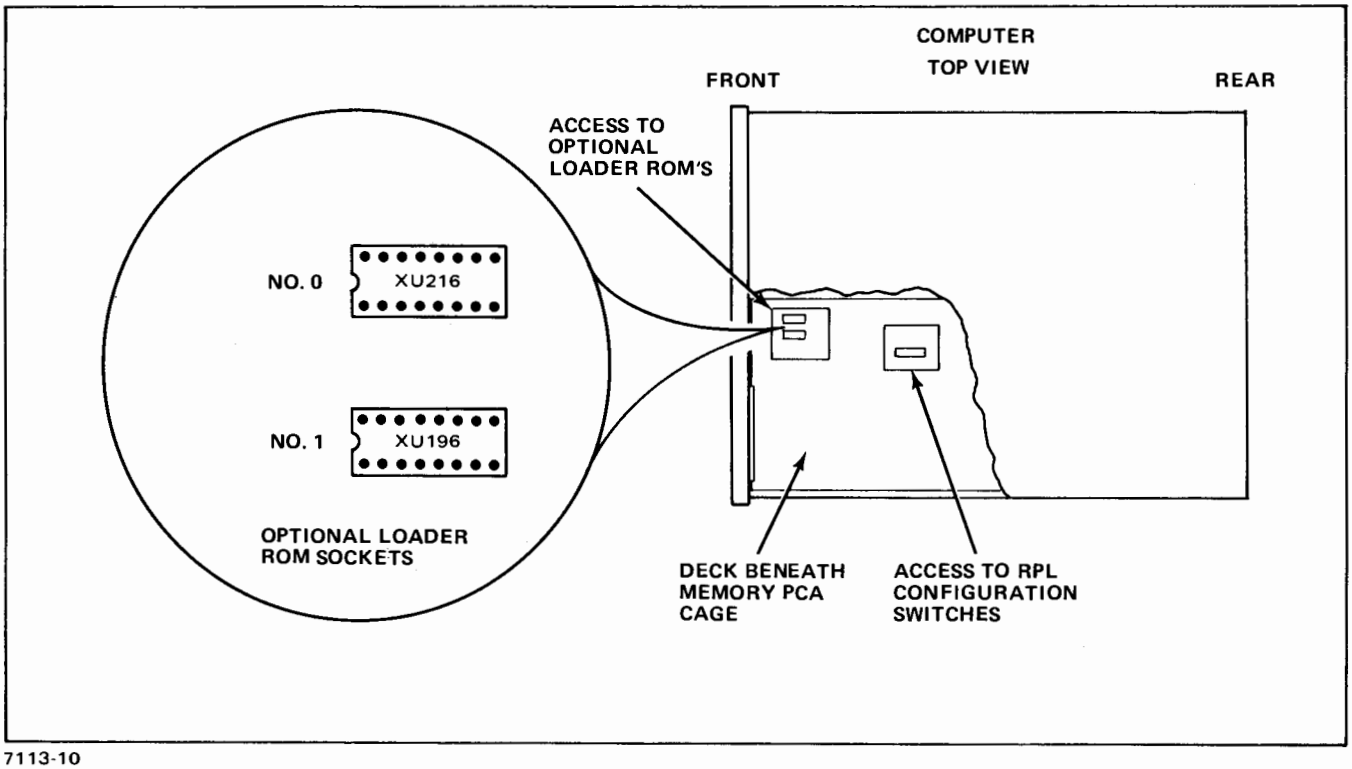
After removing or replacing optional loader ROM, replace all PCA's in memory PCA cage, reconnect cable assemblies, and reinstall memory PCA cage cover and operator panel.

2-18. OPERATOR PANEL PCA

2-19. REMOVAL. Set the key-operated switch to STANDBY and remove the operator panel PCA as follows:

a. Loosen quarter-turn fasteners on operator panel and lower it to the access position.

b. Disconnect operator panel cable assembly from CPU PCA front edge connector.



7113-10

Figure 2-4. Optional Loader ROM Sockets

c. Remove the four screws and lockwashers from operator panel PCA cover; remove operator panel PCA cover.

d. Remove the eight screws and lockwashers securing operator panel PCA to operator panel; remove operator panel PCA.

2-20. ROCKER SWITCH CONTACTS. Defective rocker switch contacts on the operator panel PCA are replaced as follows:

a. Loosen adhesive securing rocker switch to operator panel PCA.

b. Grasp rocker switch assembly and pull straight out from operator panel PCA.

c. Separate defective spring contacts from rocker switch assembly.

d. Clean replacement spring contacts with the Freon TF Degreaser (or equivalent) and position replacement spring contacts onto operator panel PCA.

e. Place rocker switch assembly over spring contacts; press inward on rocker switch assembly until it snaps into place.

2-21. REPLACEMENT. Install the operator panel PCA as follows:

a. Carefully place operator panel PCA into position and replace the eight screws and lockwashers.

b. Place operator panel PCA cover over operator panel PCA and secure in place with the four screws and lockwashers.

c. Connect operator panel cable assembly to CPU PCA front edge connector.

d. Replace operator panel and secure in place by tightening quarter-turn fasteners.

e. Set key-operated switch to OPERATE.

2-22. MEMORY CAGE PCA'S

2-23. REMOVAL. Remove the printed-circuit assemblies (PCA's) from the memory cage as follows:

a. Set ~LINE and BATTERY switches to OFF. Loosen quarter-turn fasteners on operator panel and lower it to the access position.

b. Remove the two memory PCA cage cover retaining screws and lockwashers; remove memory PCA cage cover.

c. Disconnect cable assembly from front edge connector. (The memory protect PCA does not have a front edge connector.) If removing the DCPC, do not disconnect the cable assembly from the crossover PCA; if removing the memory controller or memory module, disconnect the cable assembly from all PCA's.

d. Remove PCA by pulling outward on extractor levers.

2-24. MEMORY INTEGRATED CIRCUITS. Memory malfunctions may be isolated to an integrated circuit on a memory module as described in paragraph 2-5. Replace faulty integrated circuit as follows:

a. Using diagonal cutters, clip the integrated circuit pins close to the integrated circuit pack. Remove and discard integrated circuit.

b. Using a 30W soldering iron with a small soldering tip, unsolder and remove each clipped pin from the PCA.

c. Using a Soldapulldt hand-operated vacuum device (part no. 8690-0060) or a rubber bulb with a suction tube, withdraw molten solder from each hole in the PCA.

d. Mount the new integrated circuit on the PCA and solder each pin. Observe proper orientation of integrated circuit.

e. Clean PCA with a flux remover such as Freon TF Degreaser or equivalent.

2-25. REPLACEMENT. Replace memory cage PCA's in the reverse order of the removal procedure. When installing a replacement memory module, be sure to configure the memory module address jumpers correctly. Figures 2-5 through 2-7 illustrate the jumper requirements for the HP 2102 16K, 8K, and 4K memory modules.

2-26. I/O INTERFACE PCA'S

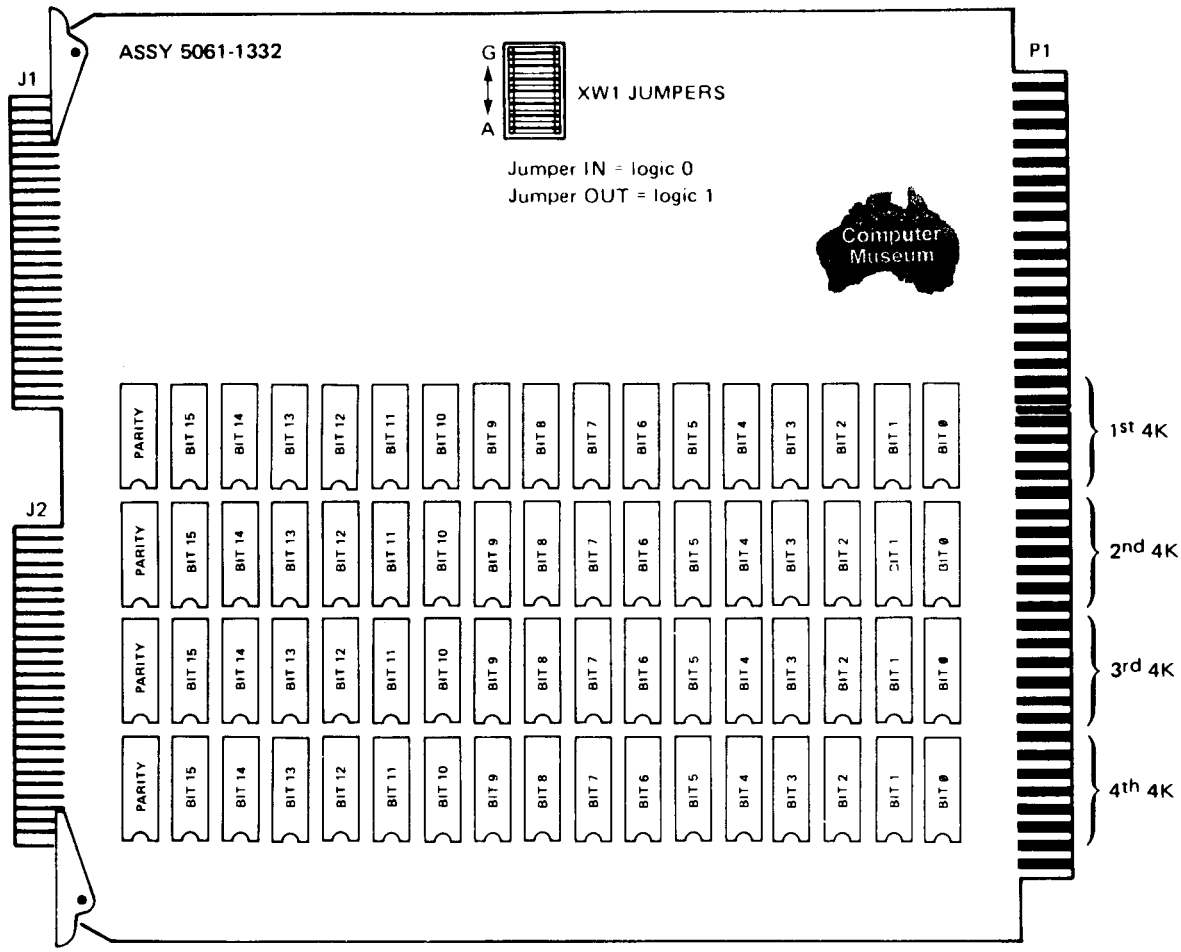
2-27. REMOVAL. Remove an I/O interface PCA from the I/O PCA cage as follows:

a. Set key-operated switch to STANDBY. Do not set ~LINE switch to OFF unless this procedure is used in conjunction with the procedure to remove the I/O backplane. (Refer to paragraph 2-32.)

b. If power fail recovery system is installed, set BATTERY switch to OFF and disconnect battery cable(s) from BAT. INPUT connector(s).

c. Remove I/O PCA cage cover and loosen the screw(s) securing I/O PCA retainer. Slide retainer to the right.

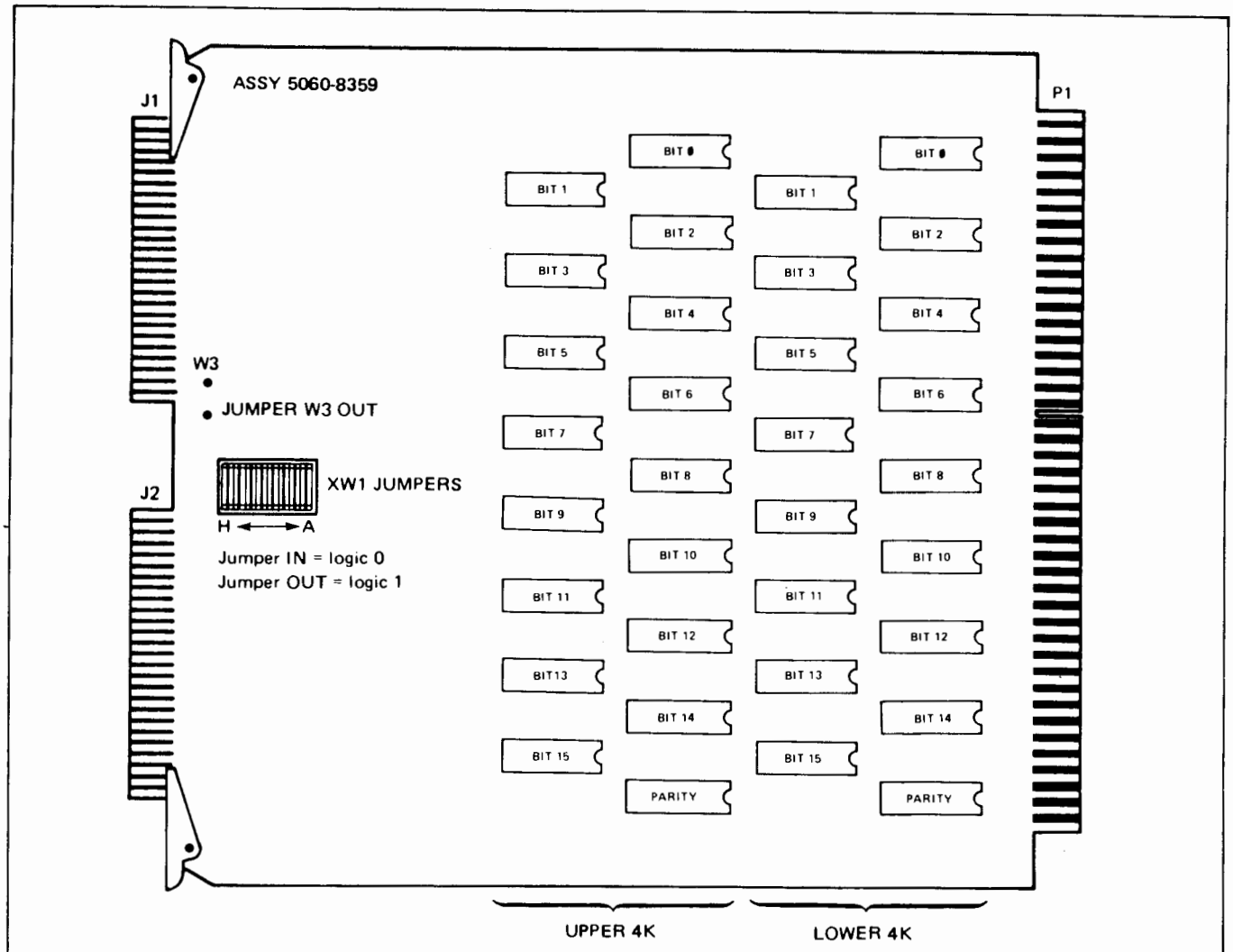
d. Remove I/O cable connector hood from I/O interface PCA. Remove I/O interface PCA by pulling outward on the PCA extractor levers.



MEMORY MODULE NO.	XW1 JUMPERS						
	A (2^0)	B (2^1)	C (2^2)	D (2^3)	E (2^4)	F (2^5)	G
0,1	IN	IN	IN	IN	IN	IN	ALWAYS OUT
2,3	OUT	IN	IN	IN	IN	IN	
4,5	IN	OUT	IN	IN	IN	IN	
6,7	OUT	OUT	IN	IN	IN	IN	
8,9	IN	IN	OUT	IN	IN	IN	
10,11	OUT	IN	OUT	IN	IN	IN	
12,13	IN	OUT	OUT	IN	IN	IN	
14,15	OUT	OUT	OUT	IN	IN	IN	
16,17	IN	IN	IN	OUT	IN	IN	
18,19	OUT	IN	IN	OUT	IN	IN	
20,21	IN	OUT	IN	OUT	IN	IN	
22,23	OUT	OUT	IN	OUT	IN	IN	
24,25	IN	IN	OUT	OUT	IN	IN	
26,27	OUT	IN	OUT	OUT	IN	IN	
28,29	IN	OUT	OUT	OUT	IN	IN	
30,31	OUT	OUT	OUT	OUT	IN	IN	
32,33	IN	IN	IN	IN	OUT	IN	

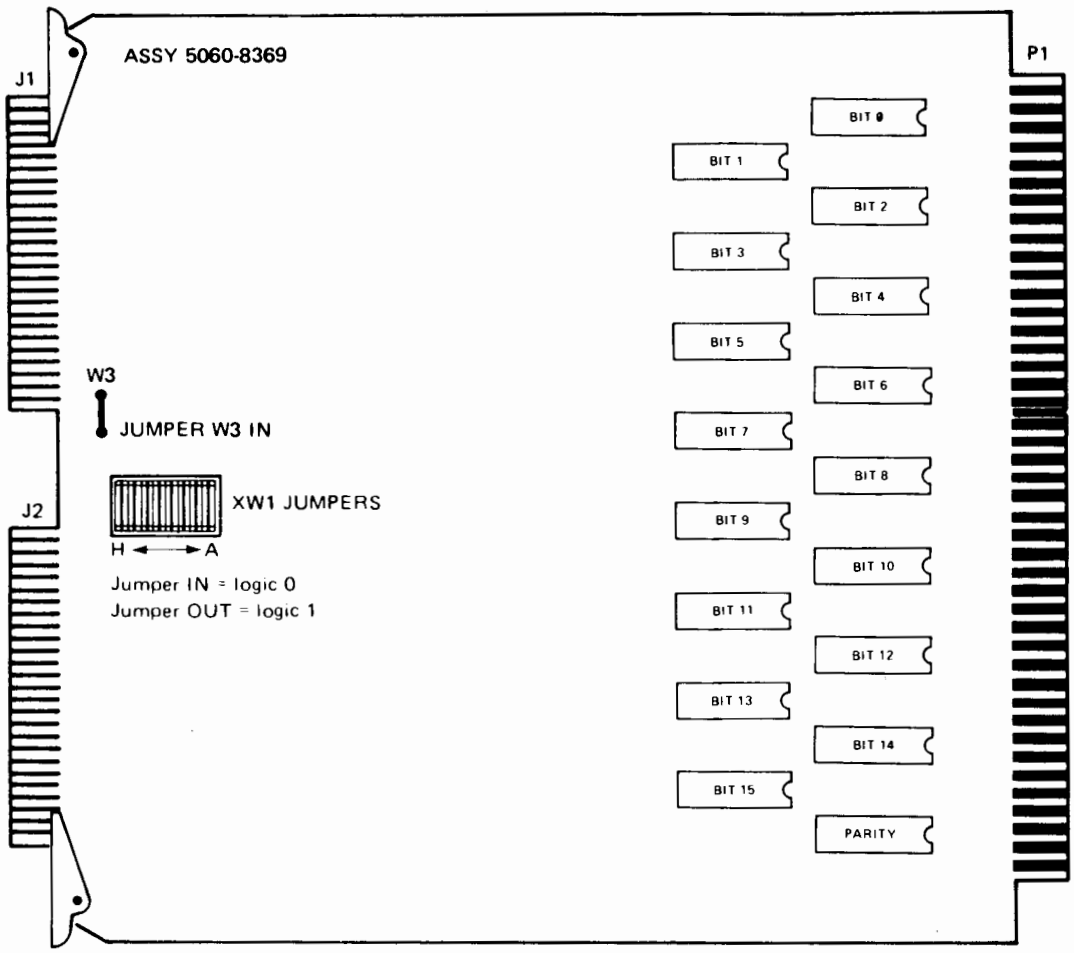
Note: The 16K modules are equivalent to two contiguous 8K modules.

Figure 2-5. HP 2102 16K Memory Module Address Jumpers



MEMORY MODULE NO.	W3	XW1 JUMPERS							
		A	B (2^0)	C (2^1)	D (2^2)	E (2^3)	F (2^4)	G (2^5)	H 2^6)
0	ALWAYS OUT	DON'T CARE	IN	IN	IN	IN	IN	IN	IN
1			OUT	IN	IN	IN	IN	IN	IN
2			IN	OUT	IN	IN	IN	IN	IN
3			OUT	OUT	IN	IN	IN	IN	IN
4			IN	IN	OUT	IN	IN	IN	IN
5			OUT	IN	OUT	IN	IN	IN	IN
6			IN	OUT	OUT	IN	IN	IN	IN
7			OUT	OUT	OUT	IN	IN	IN	IN
8			IN	IN	IN	OUT	IN	IN	IN
9			OUT	IN	IN	OUT	IN	IN	IN
10			IN	OUT	IN	OUT	IN	IN	IN
11			OUT	OUT	IN	OUT	IN	IN	IN
12			IN	IN	OUT	OUT	IN	IN	IN
13			OUT	IN	OUT	OUT	IN	IN	IN
14			IN	OUT	OUT	OUT	IN	IN	IN
15			OUT	OUT	OUT	OUT	IN	IN	IN
16			IN	IN	IN	IN	OUT	IN	IN

Figure 2-6. HP 2102 8K Memory Module Address Jumpers



MEMORY MODULE NO.	W3	XW1 JUMPERS							
		A	B (2^0)	C (2^1)	D (2^2)	E (2^3)	F (2^4)	G (2^5)	H (2^6)
0	ALWAYS IN	ALWAYS IN	IN	IN	IN	IN	IN	IN	IN
1			OUT	IN	IN	IN	IN	IN	IN
2			IN	OUT	IN	IN	IN	IN	IN
3			OUT	OUT	IN	IN	IN	IN	IN
4			IN	IN	OUT	IN	IN	IN	IN
5			OUT	IN	OUT	IN	IN	IN	IN
6			IN	OUT	OUT	IN	IN	IN	IN
7			OUT	OUT	OUT	IN	IN	IN	IN
8			IN	IN	IN	OUT	IN	IN	IN
9			OUT	IN	IN	OUT	IN	IN	IN
10			IN	OUT	IN	OUT	IN	IN	IN
11			OUT	OUT	IN	OUT	IN	IN	IN
12			IN	IN	OUT	OUT	IN	IN	IN
13			OUT	IN	OUT	OUT	IN	IN	IN
14			IN	OUT	OUT	OUT	IN	IN	IN
15			OUT	OUT	OUT	OUT	IN	IN	IN
16			IN	IN	IN	IN	OUT	IN	IN

Note: This 4K module must be assigned the highest used memory module number regardless of the memory configuration. Only one 4K module allowed per configuration.

Figure 2-7. HP 2102 4K Memory Module Address Jumpers

2-28. REPLACEMENT. Replace I/O interface PCA in reverse order of the removal procedure. Be sure to configure the I/O interface PCA jumpers (if used) if a replacement PCA is being installed.

2-29. CROSSOVER PCA

2-30. REMOVAL. Remove the crossover PCA from the computer mainframe as follows:

a. Set ~LINE and BATTERY switches to OFF.

b. Remove computer top cover and disconnect DCPC cable assembly (if used) from edge connector J1. (See figure 2-8.) Disconnect power supply cable assembly from edge connector J2.

c. Each wire connected to TB1 is terminated with a spade lug. Loosen the 12 screws on TB1 and disconnect each wire.

d. Remove the four screws and lockwashers securing crossover PCA to PCA cage covers.

e. Carefully lift crossover PCA to free it from backplane edge connectors.

2-31. REPLACEMENT. Install the crossover PCA as follows:

a. Position crossover PCA with receptacles A6XA4 and A6XA5 in contact with I/O and memory backplane connectors.

b. Press inward on back of A6XA4 and A6XA5 to seat backplanes fully into crossover PCA receptacles. Secure crossover PCA to PCA cage covers using the four screws and lockwashers.

c. Slide spade lug of each wire under washer of appropriate connection point on terminal block and tighten screw.

d. Connect DCPC cable assembly (if used) to edge connector J1. Connect power supply cable assembly to J2.

e. Replace computer top cover and set ~LINE and BATTERY switches to ON.

2-32. MEMORY AND I/O BACKPLANES

2-33. REMOVAL. Remove the memory and I/O backplanes from the computer mainframe as follows:

a. Set ~LINE and BATTERY switches to OFF.

b. Remove top cover and disconnect DCPC cable assembly (if used) from crossover PCA edge connector J1.

c. Withdraw all memory PCA's approximately 2 inches (5 centimeters) to clear rear connectors from memory backplane receptacles.

d. Withdraw all I/O interface PCA's approximately 2 inches (5 centimeters) to clear rear connectors from I/O backplane receptacles.

e. Remove the four screws and lockwashers securing crossover PCA to PCA cage covers. Carefully lift cross over PCA to free it from backplane edge connectors.

f. Grasp memory backplane and lift up and out of memory PCA cage assembly.

g. Grasp I/O backplane and lift up and out of I/O PCA cage assembly.

2-34. REPLACEMENT. Replace the memory and I/O backplanes in reverse order of the removal procedure. Be sure to reconnect DCPC cable assembly (if used) after all PCA's have been seated firmly into their mating receptacles.

CAUTION

Note markings on backplanes to ensure proper orientation. Improper orientation can damage the computer.

2-35. POWER FAIL RECOVERY SYSTEM FOR HP 2109A

2-36. BATTERY REMOVAL. Set the BATTERY switch to OFF and disconnect the battery cable from the BAT. INPUT connector. Remove the four screws and lockwashers securing the cover to the battery housing. Remove the battery assembly.

2-37. BATTERY PCA REMOVAL. Slide the computer top cover back to access the battery PCA's. Grasp battery output PCA and pull upward out of the battery board guides. Remove battery control I PCA and the battery control II PCA in the same manner as indicated for the battery output PCA.

2-38. REPLACEMENT. Replace the battery and the battery PCA's in the reverse order of the removal procedures.

2-39. POWER FAIL RECOVERY SYSTEM FOR HP 2113A

2-40. BATTERY REMOVAL. Set the BATTERY switch to OFF and disconnect the battery cables from the BAT. INPUT connectors. Remove the eight screws and lockwashers from the battery housing cover. Remove the housing cover and battery assemblies.

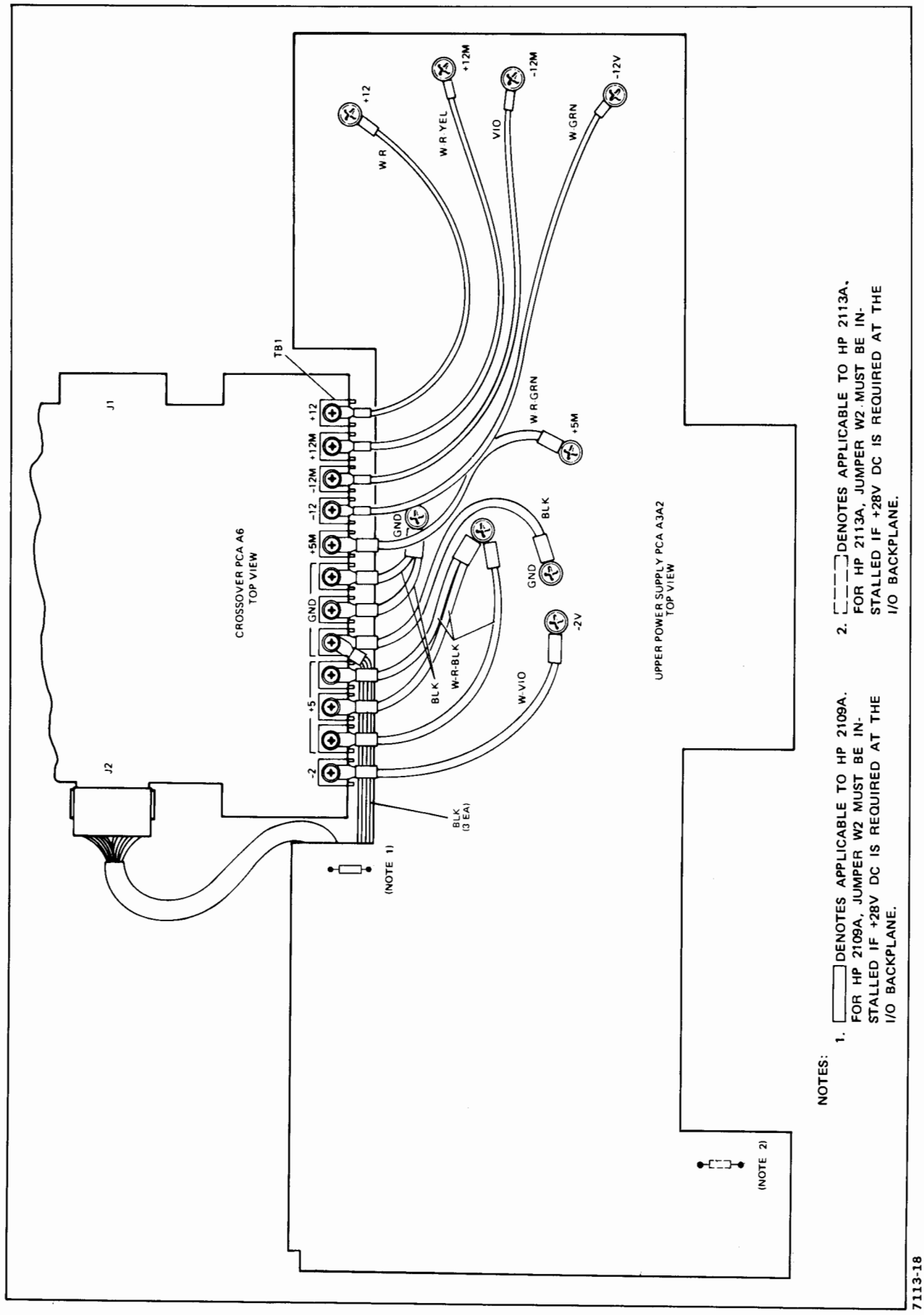


Figure 2-8. Crossover PCA Power Connections

2-41. BATTERY PCA REMOVAL. Slide the computer top cover back to access the battery PCA. Grasp battery PCA and pull upward out of the battery PCA guide.

2-42. REPLACEMENT. Replace the batteries and the battery PCA in the reverse order of the removal procedures.

2-43. POWER SUPPLY FOR HP 2109A

WARNING

Hazardous voltages are present with the ac power cord connected. Ensure that ac power cord is disconnected before proceeding.

2-44. REMOVAL. Remove the top cover and the crossover PCA and proceed as follows:

a. Loosen the two quarter-turn screws and lower operator panel to the access position. Remove memory PCA cage cover.

b. Remove the three screws and lockwashers securing front power supply shield to computer mainframe.

c. Disconnect key-operated switch assembly cable from lower power supply PCA.

d. If power fail recovery system is installed, set BATTERY switch to OFF and disconnect battery cable from BAT. INPUT connector. Remove I/O PCA cage cover and loosen I/O PCA retainer; slide retainer to the right.

e. Remove the four screws and lockwashers securing rear panel to computer mainframe.

f. Disconnect battery cable assembly from upper power supply PCA.

g. Remove the eight long screws and lockwashers securing upper power supply PCA to computer mainframe.

h. Remove battery output PCA.

i. Remove the two screws and lockwashers securing lower power supply PCA to computer mainframe.

j. Disconnect power supply cable assembly from crossover PCA.

k. Disconnect ac power cable assembly from lower power supply PCA.

l. Lift power supply up and out of computer mainframe.

2-45. REPLACEMENT. The HP 2109A Computer and the HP 12979A I/O Extender employ identical power supplies and differ only in jumper configurations. If installing a replacement power supply, ensure that the jumpers located on the component side of upper power supply PCA are configured as required for the HP 2109A Computer. (See figure 2-9.) After configuring the power supply jumpers, replace power supply in the reverse order of the removal procedure. Attach the crossover PCA to the upper power supply PCA as shown in figure 2-8.

2-46. POWER SUPPLY FOR HP 2113A

WARNING

Hazardous voltages are present with the ac power cord connected. Ensure that ac power cord is disconnected before proceeding.

2-47. REMOVAL. Remove the top cover and the crossover PCA and proceed as follows:

a. Loosen the four quarter-turn screws and lower operator panel to the access position. Remove memory PCA cage cover.

b. Remove the three screws and lockwashers securing front power supply shield to computer mainframe. Remove the one screw and lockwasher attaching shield to battery PCA guide.

c. Remove front power supply shield and disconnect key-operated switch assembly cable from lower power supply PCA.

d. If power fail recovery system is installed, set BATTERY switch to OFF and disconnect battery cables from BAT. INPUT connectors. Remove I/O PCA cage cover and loosen I/O PCA retainer; slide retainer to the right.

e. Remove the four screws and lockwashers securing rear panel to computer mainframe.

f. Disconnect battery cable assembly from upper power supply PCA.

g. Remove the six screws and lockwashers securing the three power supply support brackets to right side of computer.

h. Remove the eight long screws and lockwashers securing upper power supply PCA to computer mainframe.

i. Remove the two short screws and lockwashers securing lower power supply PCA to computer mainframe.

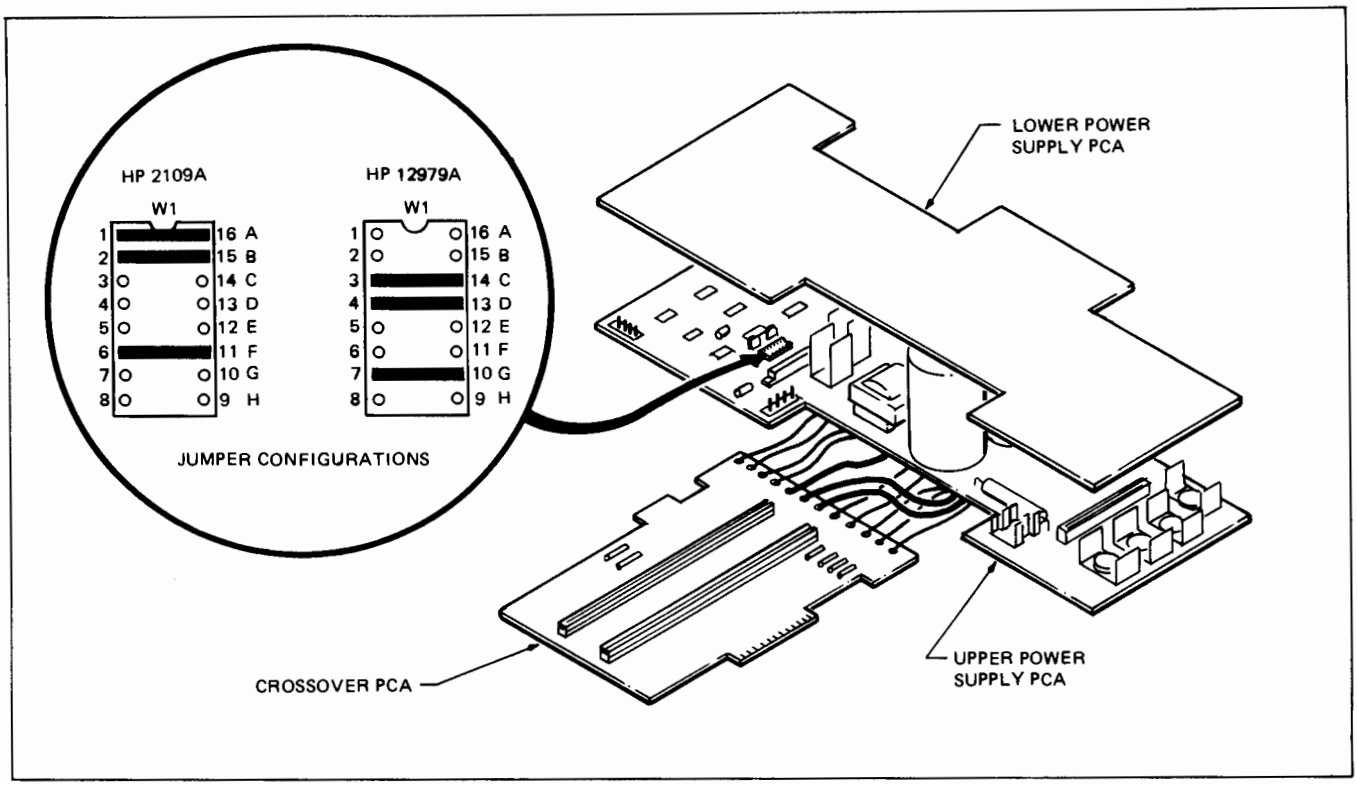


Figure 2-9. Power Supply Jumper Configurations

j. Disconnect power supply cable assembly from crossover PCA.

k. Disconnect power leads from upper fans.

l. Lift power supply up and out of computer mainframe.

m. Disconnect ac power cable assembly from lower power supply PCA.

2-48. REPLACEMENT. Replace the power supply in the reverse order of the removal procedure.

2-49. VENTILATING FANS FOR HP 2109A

2-50. REMOVAL. Remove the computer top, bottom, and right side covers and proceed as follows:

WARNING

Hazardous voltages are present with the ac power cord connected. Ensure that ac power cord is disconnected before proceeding.

a. Disconnect the two power leads at top of fan.

b. Remove the 14 screws securing left side frame to computer mainframe.

c. Remove the four self-tapping screws securing fan to computer mainframe. Pull fan upward and out of the mainframe.

2-51. REPLACEMENT. Replace the ventilating fan(s) in reverse order of the removal procedure.

2-52. VENTILATING FANS FOR HP 2113A

WARNING

Hazardous voltages are present with the ac power cord connected. Ensure that ac power cord is disconnected before proceeding.

2-53. REMOVAL. Remove computer top and right side covers and proceed as follows:

a. Remove power supply assembly and power leads from appropriate fan.

b. Remove the four self-tapping screws securing fan to computer mainframe; remove fan.

2-54. REPLACEMENT. Replace the ventilating fan(s) in reverse order of the removal procedure.

2-55. MEMORY RECONFIGURATION

If desired or necessary, the HP 2102 Memory System may be reconfigured. Reconfiguration requires assigning memory module numbers, reconfigurating module address jumpers, reinstallation, and verification.

2-56. MODULE NUMBER ASSIGNMENT

A 16K memory module is equivalent to two contiguous 8K memory modules; therefore, two module numbers must be allocated to each 16K memory module as shown in figure 2-5. Notice that the module numbers must first be an even number followed by the next sequential odd number. This poses one minor restriction on module number assignments when a mixture of 8K and 16K memory modules reside in the same system.

Table 2-2 lists a typical memory system in which a 16K memory module is being added. The "old configuration" included three 8K modules, one 4K module (a 4K module is a half-loaded 8K module), and zero 16K modules. The considerations given to the "new configuration" are as follows:

a. The 8K module formerly assigned module number 2 must be reassigned as module number 4 because the 16K module is assigned module numbers 2 and 3.

b. The 4K module must be reassigned as module number 5 because a half-loaded module must be assigned the highest module number in a given memory system.

It should be noted in table 2-2 that the 16K module could have alternatively been assigned modules 0 and 1, but this would have required that two of the 8K modules (0 and 1) be reassigned memory module numbers instead of the one given in the "new configuration" example.

Table 2-3 lists another typical memory system in which a 16K memory module is being added. The "old configuration" included two 16K modules, three 8K modules, and one 4K module. The considerations given to this "new configuration" are as follows:

a. To allow for a minimum of memory module number reassignment, the new 16K module is assigned module numbers 6 and 7. This allows two of the 8K module numbers (4 and 5) to remain unchanged.

b. The 8K module formerly assigned module 6 must be reassigned as module number 8 and the 4K module must be reassigned as module 9.

It should be noted in table 2-3 that the 16K module could have alternatively been assigned modules 4 and 5, but this would have required that two of the 8K modules (4 and 5) be reassigned memory module numbers instead of the one given in the "new configuration" example.

Table 2-2. Typical Memory Configuration (Example 1)

OLD CONFIGURATION			NEW CONFIGURATION			ALTERNATE CONFIGURATION		
MEM MOD.	QTY	MOD. NO.	MEM MOD.	QTY	MOD. NO.	MEM MOD.	QTY	MOD. NO.
8K	3	0,1,2	8K	3	0,1,4	8K	3	2,3,4
4K*	1	3	4K*	1	5	4K*	1	5
16K	0	—	16K	1	2,3	16K	1	0,1

*Must always be highest numbered module in memory.

Table 2-3. Typical Memory Configuration (Example 2)

OLD CONFIGURATION			NEW CONFIGURATION			ALTERNATE CONFIGURATION		
MEM MOD.	QTY	MOD. NO.	MEM MOD.	QTY	MOD. NO.	MEM MOD.	QTY	MOD. NO.
16K	2	0,1,2,3	16K	3	0,1,2,3,6,7	16K	3	0,1,2,3,4,5
8K	3	4,5,6	8K	3	4,5,8	8K	3	6,7,8
4K*	1	7	4K*	1	9	4K*	1	9

*Must always be highest numbered module in memory.

2-57. INSTALLATION IN COMPUTER

Install the 16K memory module in the computer memory PCA cage as follows:

CAUTION

All contents of memory will be lost when the line and battery voltages are both off. Therefore, before proceeding with the installation, ensure that any contents of memory to be saved are stored in another medium for later retrieval.

a. On computer rear panel, set ~LINE and BATTERY switches to OFF.

b. Loosen quarter-turn fasteners on computer operator panel and lower it to the access position. Remove memory PCA cage cover by removing the two screws and lockwashers.

c. Remove memory system cable from memory controller and existing memory modules.

d. Assign memory module numbers to 16K memory module and install XW1 jumpers as specified in figure 2-5.

e. If necessary, reassign memory module number(s) to displaced 8K memory module(s) by installing XW1 jumpers as specified in figure 2-6.

f. Reassign memory module number to displaced 4K memory module (if present) by installing XW1 jumpers as specified in figure 2-7.

g. Connect memory system cable to memory controller and memory modules. Replace memory PCA cage cover and operator panel.

h. On rear panel, set ~LINE and BATTERY switches to ON. On operator panel, set key-operated switch to R (reset) and then to STANDBY.

i. Perform checkout as described in paragraph 2-58.

2-58. VERIFICATION

After installing a memory PCA, verify proper operation by performing the firmware, semiconductor memory, and memory parity diagnostic tests. Part numbers for the diagnostic manuals and diagnostic tapes are listed below.

DIAGNOSTIC	MANUAL	TAPE
Semiconductor Memory Diagnostic Test	24395-90001	24395-16001
Memory Parity Diagnostic Test	24390-90001	24390-16003

If the diagnostic tests are completed without an error halt, the memory PCA is operating correctly. If the diagnostic tests indicate an error halt, refer to figure 2-1 and troubleshoot.

2-59. 110/220 VAC RECONFIGURATION FOR HP 2109A

To reconfigure the HP 2109A Computer to operate from 220-volt power source instead of 110-volt power source (or vice versa), refer to figures 2-10 and 2-11 and proceed as follows:

WARNING

Hazardous voltages are present inside the computer mainframe!! Before changing from 110V ac to 220V ac configuration, or vice versa, set ~LINE and BATTERY switches to OFF and disconnect the power cord!! Failure to observe this precaution can result in serious injury or death!!

a. Set ~LINE and BATTERY switches to OFF and remove power cord.

b. Remove top cover of computer and disconnect fan lead wires from fans.

c. Remove the four mounting screws and lockwashers that secure rear panel to computer frame. (Two screws are located at the top of the panel and two screws are located at the bottom of the panel.)

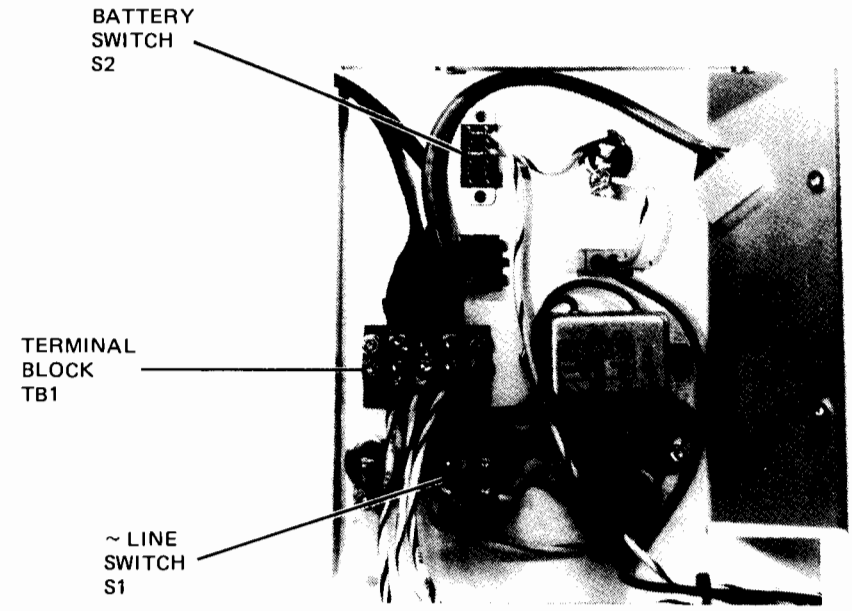
d. Carefully swing rear panel outward to expose terminal block TB1 and other components.

e. For *110V ac* operation, connect a jumper wire between the WHT-YEL-GRA and WHT-BLU-GRA lead wires on terminal block. Connect one side of each fan to the WHT-BRN-GRA lead wire on terminal block; connect other side of each fan to the WHT-BLU-GRA lead wire on terminal block. Replace fuse F1 with the type and rating specified in table 3-1.

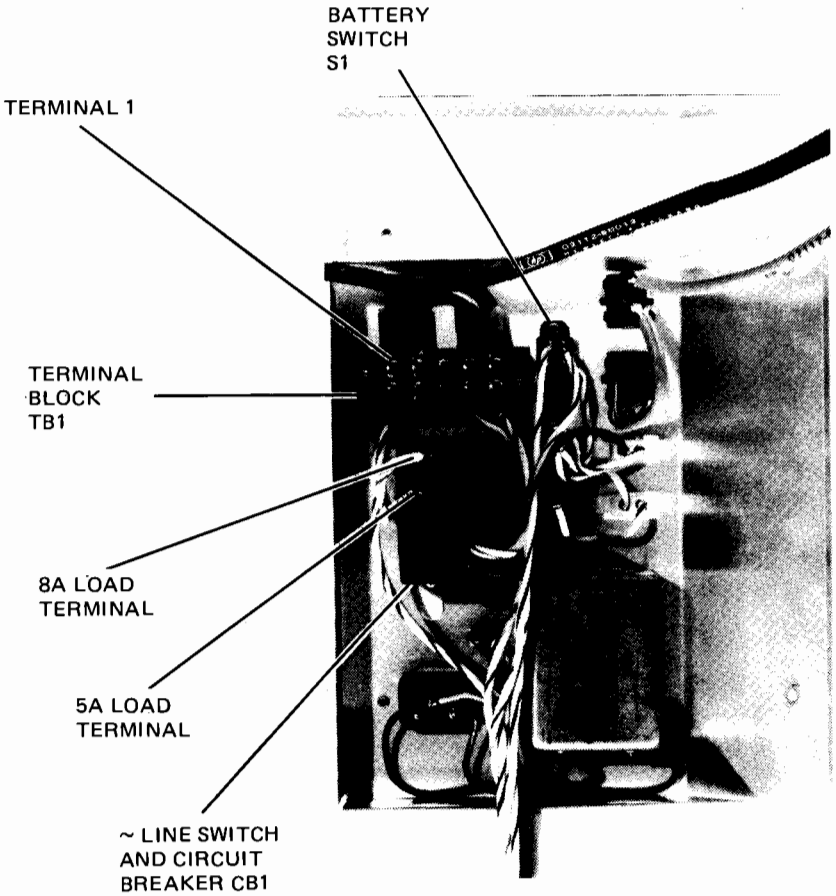
f. For *220V ac* operation, remove jumper wire between the WHT-YEL-GRA and WHT-BLU-GRA lead wires on terminal block. Connect one fan across WHT-BRN-GRA and WHT-YEL-GRA lead wires; connect other fan across the WHT-YEL-GRA and WHT-BLU-GRA lead wires. Replace fuse F1 with the type and rating specified in table 3-1.

g. Position rear panel in place and secure with the four mounting screws and lockwashers. Ensure that wires are not pinched or damaged. Connect fan lead wires to fans and replace top cover of computer.

h. Ensure that the correct power cord set is used in the new configuration. (See figure 1-6 or 1-7.)



HP 2109A



HP 2113A

7113-12

Figure 2-10. Computer Rear Panel (Inside View)

2-60. 110/220 VAC RECONFIGURATION FOR HP 2113A

To reconfigure the HP 2113A Computer to operate from 220-volt power source instead of 110-volt power source (or vice versa), refer to figures 2-10 and 2-12 and proceed as follows:

WARNING

Hazardous voltages are present inside the computer mainframe!! Before changing from 110V ac to 220V ac configuration, or vice versa, set ~LINE and BATTERY switches to OFF and disconnect the power cord!! Failure to observe this precaution can result in serious injury or death!!

a. Set ~LINE and BATTERY switches to OFF and remove power cord.

b. Remove top cover of computer and disconnect fan lead wires from fans.

c. Remove the four mounting screws and lockwashers that secure rear panel to computer frame. (Two screws are located at the top of the panel and two screws are located at the bottom of the panel.)

d. Carefully swing rear panel outward to expose terminal block TB1 and other components.

e. For *110V ac* operation, disconnect WHT-BRN-GRA lead wire from 5A LOAD terminal on circuit breaker CB1; reconnect this lead wire to 8A LOAD terminal. Disconnect WHT-YEL-GRA lead wire and the four fan lead wires from center terminal (terminal 3) on terminal block. Connect WHT-YEL-GRA lead wire to terminal 4. Connect one pair of fan lead wires to terminal 2 and the second pair of fan lead wires to terminal 4.

f. For *220V ac* operation, disconnect WHT-BRN-GRA lead wire from 8A LOAD terminal on circuit breaker CB1; reconnect this lead wire to 5A LOAD terminal. Disconnect WHT-YEL-GRA lead wire from terminal 4 and reconnect to terminal 3. Disconnect fan leads from terminals 2 and 4; connect the two pair of fan leads to terminal 3.

g. Position rear panel in place and secure with the four mounting screws and lockwashers. Ensure that wires are not pinched or damaged. Connect fan lead wires to fans and replace top cover of computer.

h. Ensure that the correct power cord set is used in the new configuration. (See figure 1-6 or 1-7.)

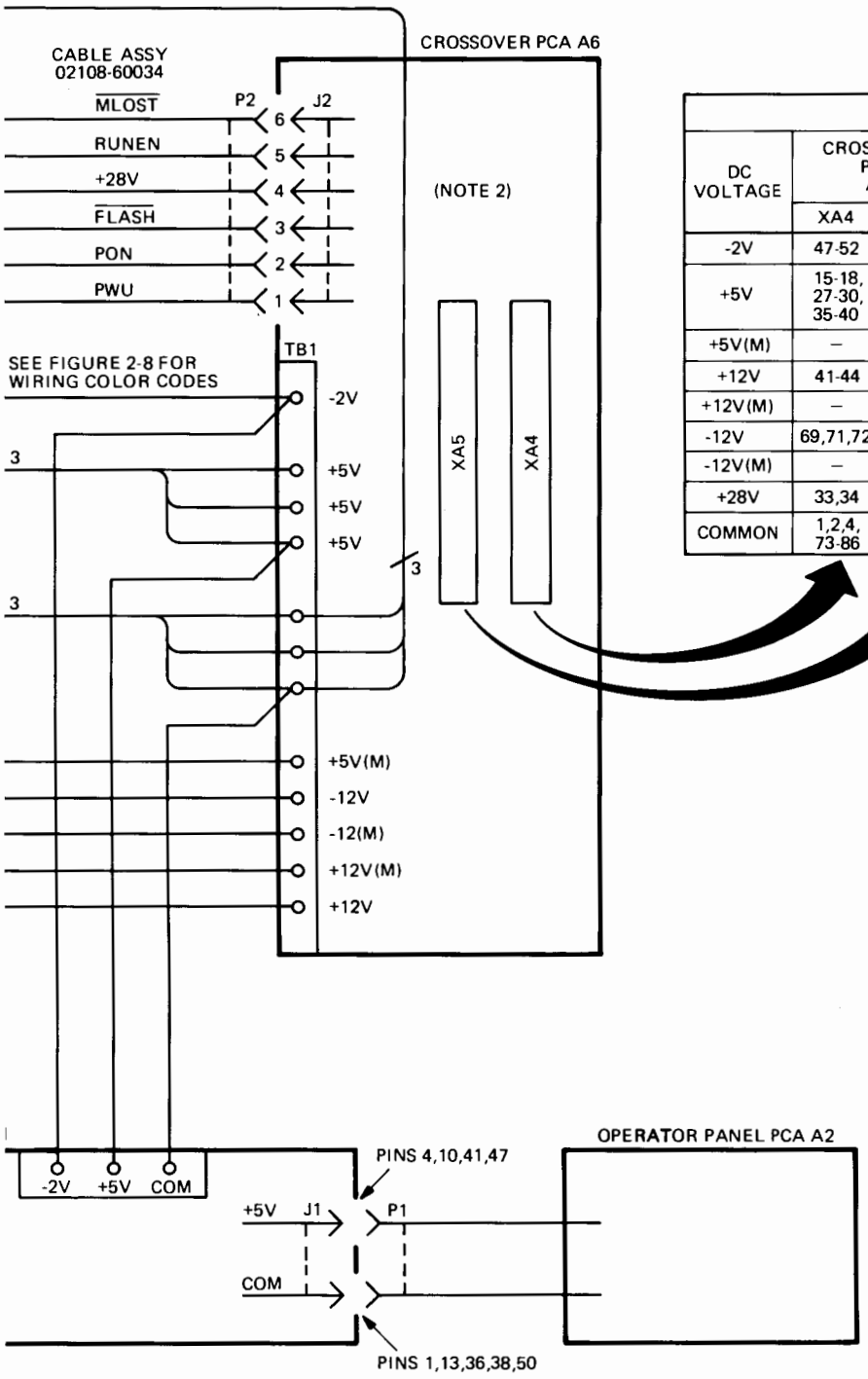
2-61. BACKPLANE SIGNALS

Table 2-4 is a listing of signals transferred to and from the various computer subassemblies. The reference number appearing to the right of the signal definition are cross-indexes to the signal distribution listing provided in table 2-5. Table 2-5 lists these signals in alphanumeric order and indicates both the signal source and signal destination.

2-62. DIAGRAMS

Figure 2-13 is a simplified block diagram of the HP 21MX E-Series Computer. The power distribution diagrams are provided in figures 2-11 and 2-12.

Figures B-1 through B-4 are the parts location and schematic diagrams for the printed-circuit assemblies designated component level replaceable in the computer. (See Appendix B.) The parts locations diagram for each PCA is located adjacent to the schematic diagram and shows the location and appearance of electrical parts on each PCA. The parts are identified by reference designations used on the schematic diagrams. The PCA part number and identification code are shown on the parts location diagram as it is marked on the PCA itself.



BACKPLANE DC POWER DISTRIBUTION						
DC VOLTAGE	CROSSOVER PCA A6		INPUT/OUTPUT BACKPLANE A4	MEMORY BACKPLANE A5		
	XA4	XA5	XA10-XA20	XA110	XA111	XA112-XA118
-2V	47-52	47-52	47,48	47,48	47,48	47,48
+5V	15-18, 27-30, 35-40	33-40	39,40	39,40	39,40	39,40
+5V(M)	–	25-32	–	–	–	29,30
+12V	41-44	–	43,44	–	–	–
+12V(M)	–	43-46	–	43,44	43,44	43,44
-12V	69,71,72	–	69,70	–	–	–
-12V(M)	–	69-72	–	69,70	69,70	69,70
+28V	33,34	–	36			
COMMON	1,2,4, 73-86	1-14, 83,85,86	1,2,85,86	1,2,85, 86	1,2,85, 86	1,2,85,86

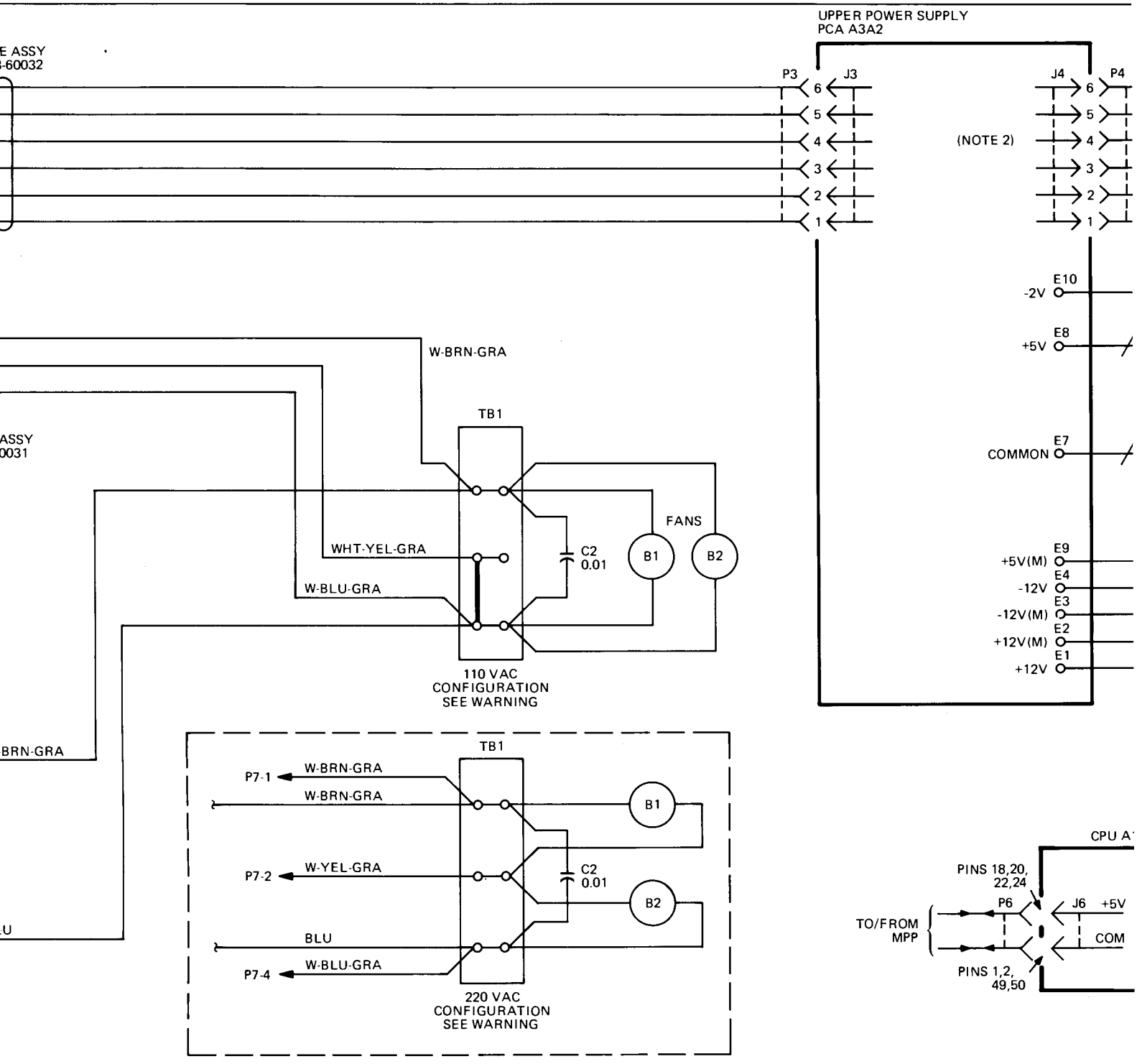
1. FUSE F1 IS 6A FOR 110V AND 4A FOR 220V.
2. JUMPER W2 MUST BE INSTALLED ON A3A2 IF +28V DC IS REQUIRED AT THE I/O BACKPLANE.
3. [ ] DENOTES REAR PANEL NOMENCLATURE

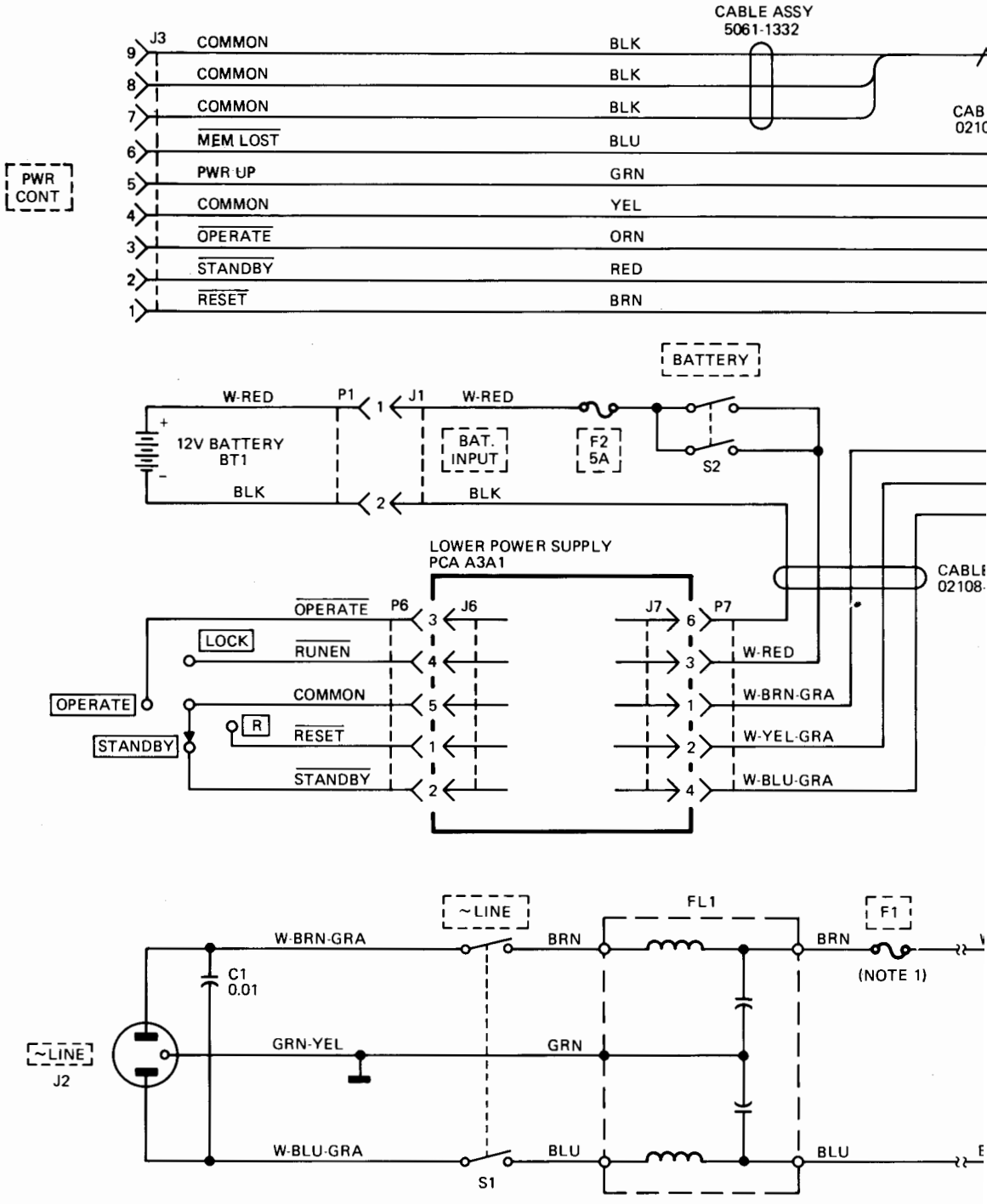
[ ] DENOTES OPERATOR PANEL NOMENCLATURE

[redacted]

HAZARDOUS VOLTAGES ARE PRESENT INSIDE THE COMPUTER MAINFRAME! BEFORE CHANGING FROM 110 VAC TO 220 VAC CONFIGURATION, OR VICE VERSA, SET [~LINE] AND [BATTERY] SWITCHES TO OFF AND DISCONNECT THE POWER CORD!! FAILURE TO OBSERVE THIS PRECAUTION CAN RESULT IN SERIOUS INJURY OR DEATH!

Figure 2-11. HP 2109A Power Distribution Diagram


E ASSY
3-60032
UPPER POWER SUPPLY
PCA A3A2
P3
J3
6
5
4
3
2
1
J4
P4
(NOTE 2)
E10
-2V
E8
+5V
E7
COMMON
E9
+5V(M)
E4
-12V
E3
-12V(M)
E2
+12V(M)
E1
+12V
W-BRN-GRA
TB1
ASSY
0031
WHT-YEL-GRA
W-BLU-GRA
C2
0.01
B1
B2
FANS
110 VAC
CONFIGURATION
SEE WARNING
BRN-GRA
LU
TB1
P7-1
W-BRN-GRA
W-BRN-GRA
P7-2
W-YEL-GRA
C2
0.01
B1
B2
BLU
P7-4
W-BLU-GRA
220 VAC
CONFIGURATION
SEE WARNING
CPU A
PINS 18,20,
22,24
P6
J6
+5V
TO/FROM
MPP
COM
PINS 1,2,
49,50


CABLE ASSY
5061-1332
J3
9 COMMON BLK
8 COMMON BLK
7 COMMON BLK
6 MEM LOST BLU
5 PWR UP GRN
4 COMMON YEL
3 OPERATE ORN
2 STANDBY RED
1 RESET BRN
PWR CONT
BATTERY
W-RED
P1
1
J1
W-RED
12V BATTERY
BT1
BAT. INPUT
F2
5A
S2
BLK
2
BLK
LOWER POWER SUPPLY
PCA A3A1
OPERATE
P6
J6
J7
P7
LOCK
RUNEN
W-RED
OPERATE
COMMON
W-BRN-GRA
R
RESET
W-YEL-GRA
STANDBY
STANDBY
W-BLU-GRA
~LINE
FL1
F1
W-BRN-GRA
BRN
BRN
C1
0.01
(NOTE 1)
~LINE
J2
GRN-YEL
GRN
W-BLU-GRA
BLU
BLU
S1

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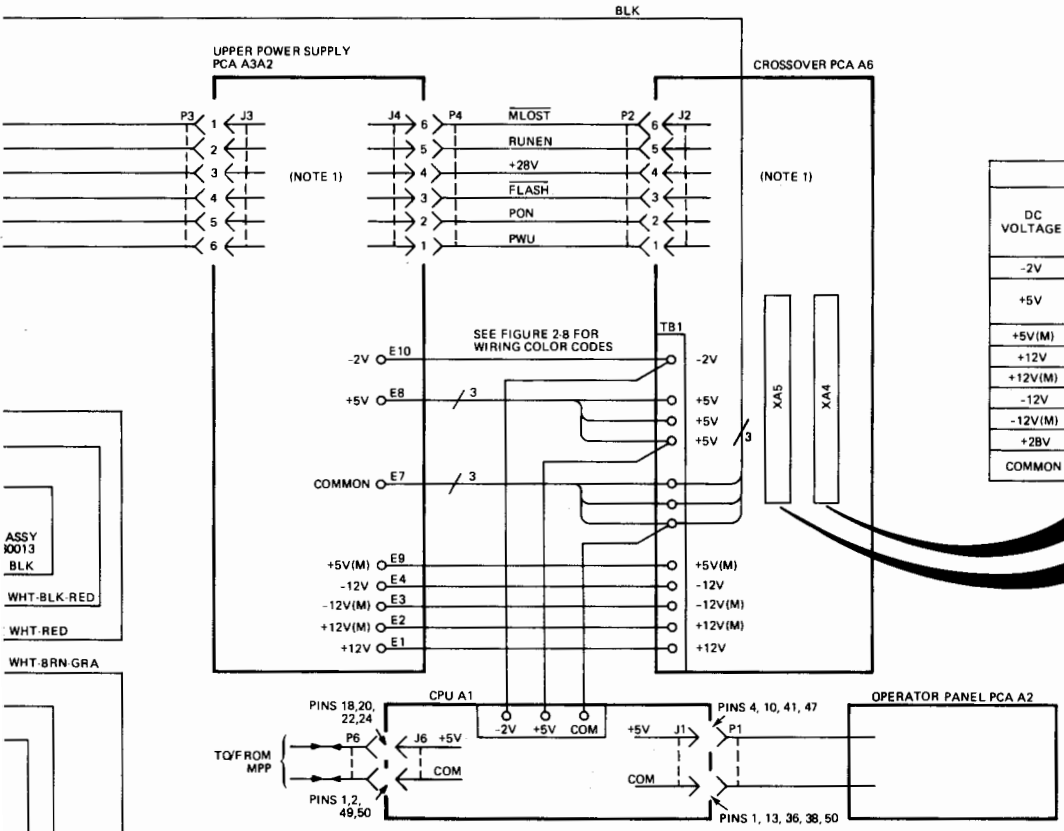


BACKPLANE DC POWER DISTRIBUTION						
DC VOLTAGE	CROSSOVER PCA A6		INPUT/OUTPUT BACKPLANE A4	MEMORY BACKPLANE A5		
	XA4	XA5	XA10-XA25	XA110	XA111	XA112-XA123
-2V	47-52	47-52	47,48	47,48	47,48	47,48
+5V	15-18, 27-30, 35-40	33-40	39,40	39,40	39,40	39,40
+5V(M)	—	25-32	—	—	—	29,30
+12V	41-44	—	43,44	—	—	—
+12V(M)	—	43-46	—	43,44	43,44	43,44
-12V	69,71,72	—	69,70	—	—	—
-12V(M)	—	69-72	—	69,70	69,70	69,70
+28V	33,34	—	36	—	—	—
COMMON	1,2,4 73-86	1-14 83,85,86	1,2,85,86	1,2,85, 86	1,2,85, 86	1,2,85,86

NOTES: 1. JUMPER W2 MUST BE INSTALLED ON A3A2 IF +28V DC IS REQUIRED AT THE I/O BACKPLANE.

2. [- - -] DENOTES REAR PANEL NOMENCLATURE

[ ] DENOTES OPERATOR PANEL NOMENCLATURE

WARNING

HAZARDOUS VOLTAGES ARE PRESENT INSIDE THE COMPUTER MAINFRAME! BEFORE CHANGING FROM 110 VAC TO 220 VAC CONFIGURATION' OR VICE VERSA,SET [~LINE] AND [BATTERY] SWITCHES TO OFF AND DISCONNECT THE POWER CORD!! FAILURE TO OBSERVE THIS PRECAUTION CAN RESULT IN SERIOUS INJURY OR DEATH!

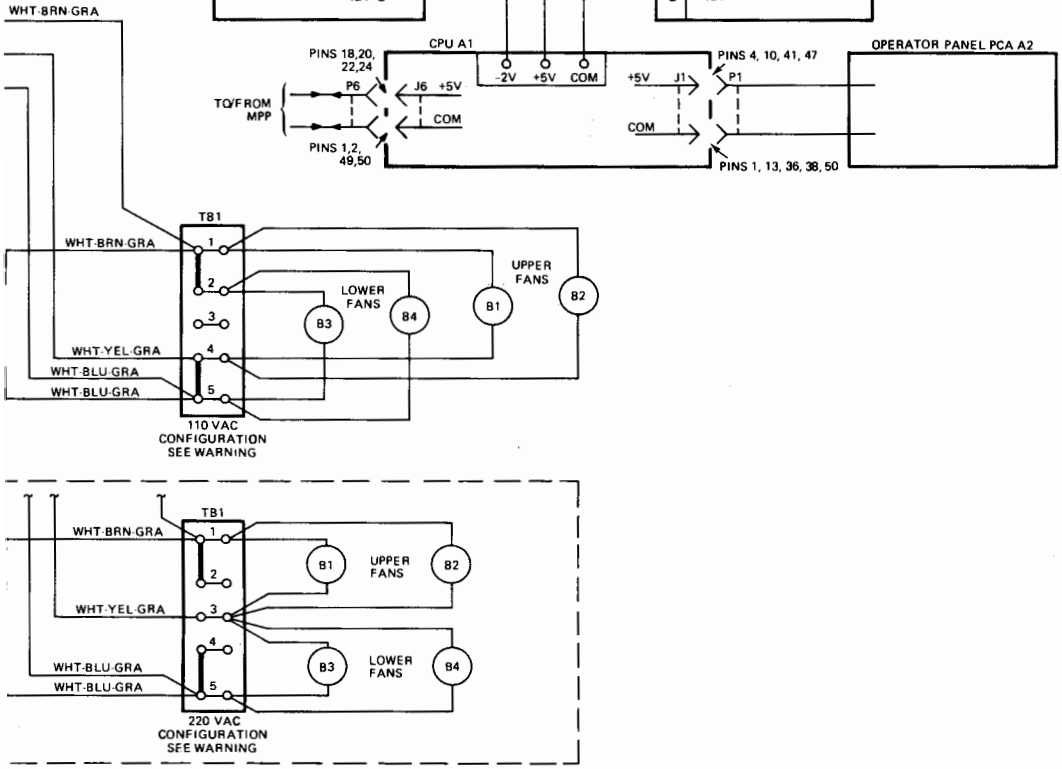
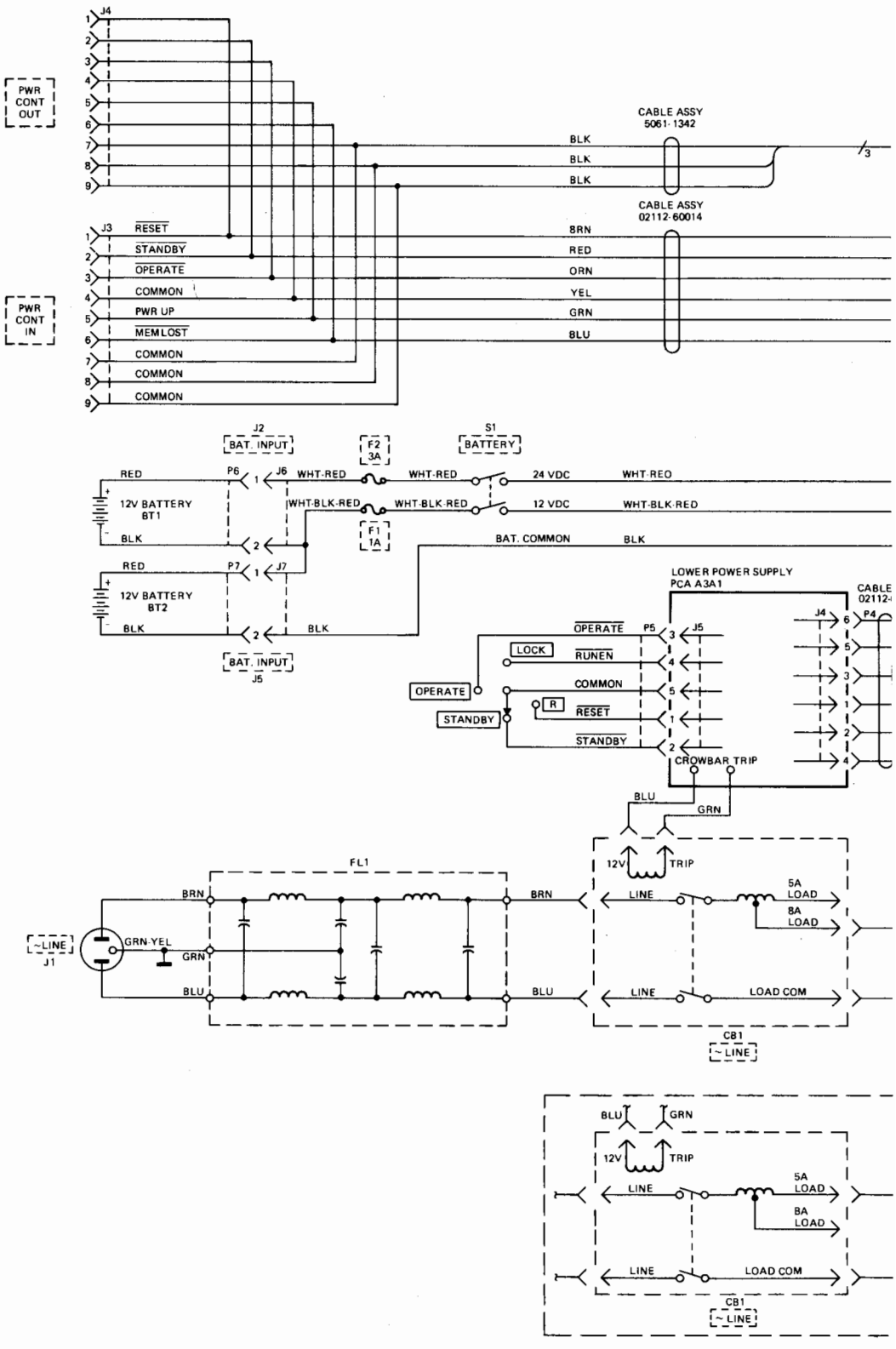


Figure 2-12. HP 2113A Power Distribution Diagram


PWR CONT OUT
J4
CABLE ASSY 5061-1342
BLK
BLK
BLK
CABLE ASSY 02112-60014
PWR CONT IN
J3
RESET
STANDBY
OPERATE
COMMON
PWR UP
MEMLOST
COMMON
COMMON
COMMON
BRN
RED
ORN
YEL
GRN
BLU
J2
BAT. INPUT
F2 3A
S1
BATTERY
RED
12V BATTERY BT1
BLK
WHT-RED
WHT-BLK-RED
24 VDC
12 VDC
F1 1A
BAT. COMMON
12V BATTERY BT2
LOWER POWER SUPPLY PCA A3A1
OPERATE
LOCK
RUNEN
COMMON
RESET
STANDBY
CROWBAR TRIP
FL1
~LINE
J1
GRN-YEL
LINE
LOAD COM
5A LOAD
8A LOAD
12V
TRIP
CB1

7113-15

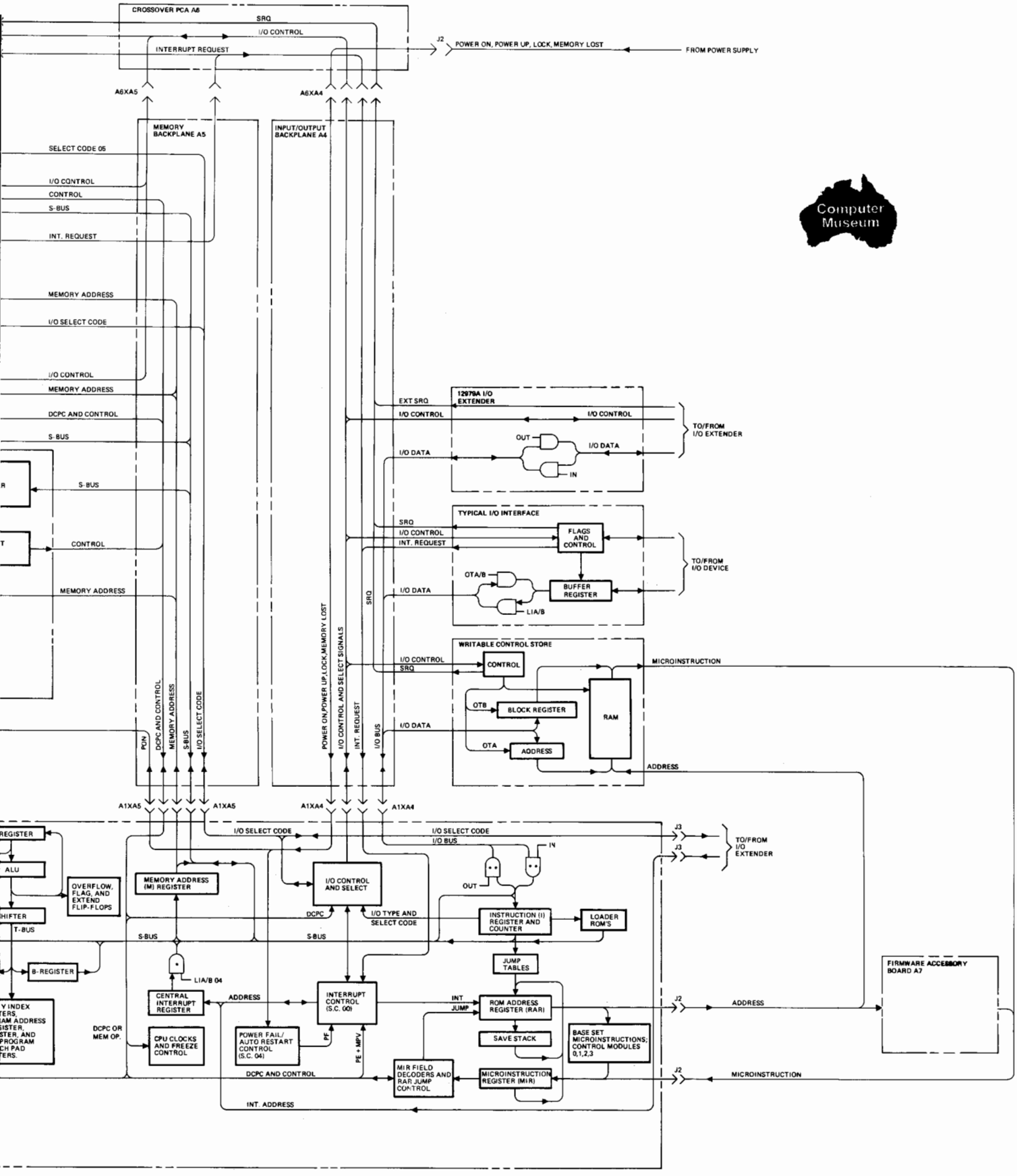
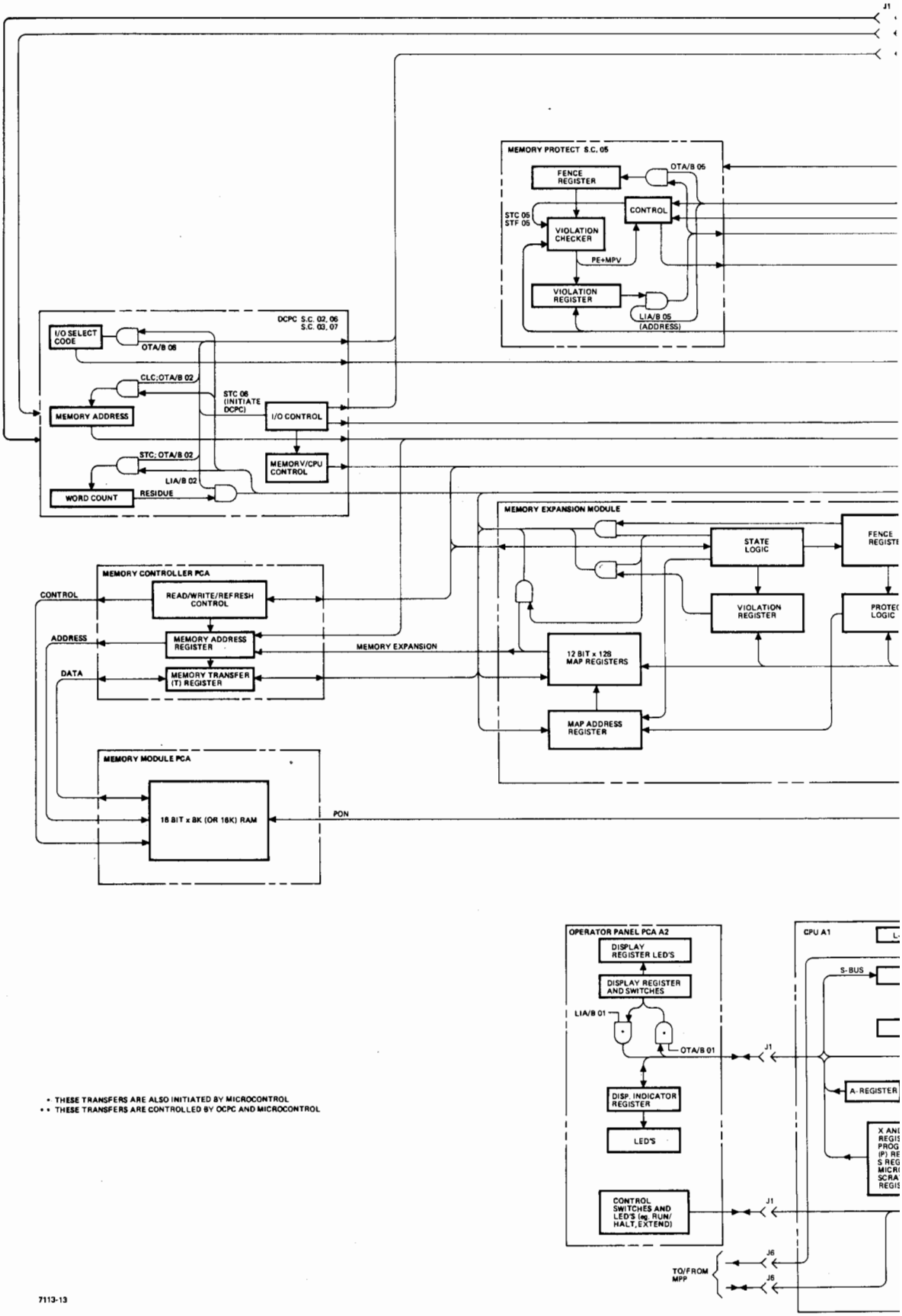


Figure 2-13. HP 21MX E-Series Computer Simplified Block Diagram



* THESE TRANSFERS ARE ALSO INITIATED BY MICROCONTROL
** THESE TRANSFERS ARE CONTROLLED BY OCPC AND MICROCONTROL

7113-13

Table 2-4. Signal Name Index

SIGNAL MNEMONIC	DEFINITION	REF NO.
$\overline{\text{BIOI}}$	"Not" Block Input/Output Input	1
$\overline{\text{BIOO}}$	"Not" Block Input/Output Output	2
$\overline{\text{BIOS}}$	"Not" Block Input/Output Strobe	3
$\overline{\text{BSEN}}$	"Not" Base Set Enable	280
CLC	Clear Control	4
CLF	Clear Flag	5
$\overline{\text{CLKX}}$	"Not" Clock, External	6
$\overline{\text{CLXEN}}$	"Not" Clock, External, Enable	7
CRS	Control Reset	8
$\overline{\text{CTL5}}$	"Not" Control 5	9
$\overline{\text{DECM}}$	"Not" Decrement M-register	10
$\overline{\text{DIEN}}$	"Not" Display Enable	11
$\overline{\text{DISPLAY}}$	"Not" Display	12
$\overline{\text{DIST}}$	"Not" Display Store	13
$\overline{\text{DMACYC}}$	"Not" DMA Cycle	14
$\overline{\text{DMAEN}}$	"Not" DMA Enable	15
$\overline{\text{DMAFRZ}}$	"Not" DMA Freeze	16
$\overline{\text{DMAIOI}}$	"Not" DMA I/O Input	17
$\overline{\text{DMAIOO}}$	"Not" DMA I/O Output	18
$\overline{\text{DMALCH}}$	"Not" DMA Latch	19
$\overline{\text{DMALO}}$	"Not" DMA Lockout	20
$\overline{\text{DMAREAD}}$	"Not" DMA Read	21
$\overline{\text{DMARQ1}}$	"Not" DMA Request 1	22
$\overline{\text{DMARQ2}}$	"Not" DMA Request 2	23
$\overline{\text{DMARQ3}}$	"Not" DMA Request 3	24
$\overline{\text{DMASTRB}}$	"Not" DMA Strobe	25
$\overline{\text{DSPCL}}$	"Not" Display Clear	26
$\overline{\text{DSPEN}}$	"Not" Display Enable	27
$\overline{\text{DSPST}}$	"Not" Display Store	28
$\overline{\text{ECSEN}}$	"Not" External Control Enable	29
EDT	End Data Transfer	30
ENF	Enable Flag	31
EXFF	Extend Flip-Flop	32
$\overline{\text{FTCH}}$	"Not" Fetch	34

Table 2-4. Signal Name Index (Continued)

SIGNAL MNEMONIC	DEFINITION	REF NO.
$\overline{\text{FLASH}}$	"Not" Flash	35
FLG1	Flag bit 1	36
FLG2	Flag bit 2	37
$\overline{\text{FLG5}}$	"Not" Flag s.c. 5 (memory protect)	38
HLTB	Halt Button	39
$\overline{\text{HLTPE}}$	"Not" Halt Parity Error	40
IAK	Interrupt Acknowledge	41
$\overline{\text{IA0}}$	"Not" Interrupt Address bit 0	42
$\overline{\text{IA1}}$	"Not" Interrupt Address bit 1	43
$\overline{\text{IA2}}$	"Not" Interrupt Address bit 2	44
$\overline{\text{IA3}}$	"Not" Interrupt Address bit 3	45
$\overline{\text{IA4}}$	"Not" Interrupt Address bit 4	46
$\overline{\text{IA5}}$	"Not" Interrupt Address bit 5	47
$\overline{\text{IBL}}$	"Not" Initial Binary Loader	48
IEN5	Interrupt Enable s.c. 5	49
IEN10	Interrupt Enable s.c. 10	50
IEN20	Interrupt Enable s.c. 20	51
$\overline{\text{INCI}}$	"Not" Indirect Counter Increment	52
$\overline{\text{INCM}}$	"Not" Increment M-register	53
$\overline{\text{INSTEP}}$	"Not" Instruction Step	54
INTL	Interrupt Light	55
$\overline{\text{INTX}}$	"Not" Interrupt, External	56
IOB0	Input/Output Bus bit 0	57
IOB1	Input/Output Bus bit 1	58
IOB2	Input/Output Bus bit 2	59
IOB3	Input/Output Bus bit 3	60
IOB4	Input/Output Bus bit 4	61
IOB5	Input/Output Bus bit 5	62
IOB6	Input/Output Bus bit 6	63
IOB7	Input/Output Bus bit 7	64
IOB8	Input/Output Bus bit 8	65
IOB9	Input/Output Bus bit 9	66
IOB10	Input/Output Bus bit 10	67
IOB11	Input/Output Bus bit 11	68
IOB12	Input/Output Bus bit 12	69

Table 2-4. Signal Name Index (Continued)

SIGNAL MNEMONIC	DEFINITION	REF NO.
IOB13	Input/Output Bus bit 13	70
IOB14	Input/Output Bus bit 14	71
IOB15	Input/Output Bus bit 15	72
IOG	Input/Output Group	73
$\overline{\text{IOGSP}}$	"Not" Input/Output Group, Special	74
IOI	I/O Input	75
IOO	I/O Output	76
IRQ1	Interrupt Request bit 1	77
IRQ2	Interrupt Request bit 2	78
IRQ3	Interrupt Request bit 3	79
IRQ4	Interrupt Request bit 4	80
IRQ5	Interrupt Request bit 5	81
IRQ6	Interrupt Request bit 6	82
IRQ7	Interrupt Request bit 7	83
$\overline{\text{IRST}}$	"Not" Instruction Register Store	84
$\overline{\text{LEFT}}$	"Not" Left	85
LR0	L-Register bit 0	86
LR1	L-Register bit 1	87
LR2	L-Register bit 2	88
LR3	L-Register bit 3	89
$\overline{\text{MBEN}}$	"Not" Memory Bus Enable	90
$\overline{\text{MBUSY}}$	"Not" Memory Busy	91
MB0	Memory Bus bit 0	92
MB1	Memory Bus bit 1	93
MB2	Memory Bus bit 2	94
MB3	Memory Bus bit 3	95
MB4	Memory Bus bit 4	96
MB5	Memory Bus bit 5	97
MB6	Memory Bus bit 6	98
MB7	Memory Bus bit 7	99
MB8	Memory Bus bit 8	100
MB9	Memory Bus bit 9	101
MB10	Memory Bus bit 10	102
MB11	Memory Bus bit 11	103
MB12	Memory Bus bit 12	104

Table 2-4. Signal Name Index (Continued)

SIGNAL MNEMONIC	DEFINITION	REF NO.
MB13	Memory Bus bit 13	105
MB14	Memory Bus bit 14	106
MB15	Memory Bus bit 15	107
$\overline{\text{MEBEN}}$	"Not" Memory Expansion Bus Enable	108
MEB10	Memory Expansion Bus bit 10	109
MEB11	Memory Expansion Bus bit 11	110
MEB12	Memory Expansion Bus bit 12	111
MEB13	Memory Expansion Bus bit 13	112
MEB14	Memory Expansion Bus bit 14	113
MEB15	Memory Expansion Bus bit 15	114
MEB16	Memory Expansion Bus bit 16	115
MEB17	Memory Expansion Bus bit 17	116
MEB18	Memory Expansion Bus bit 18	117
MEB19	Memory Expansion Bus bit 19	118
$\overline{\text{MEEN}}$	"Not" Memory Expansion Enable	119
$\overline{\text{MESP}}$	"Not" Memory Expansion Special	120
$\overline{\text{MEST}}$	"Not" Memory Expansion Store	121
$\overline{\text{METDIS}}$	"Not" Memory Expansion: T-register Disabled	122
$\overline{\text{MEV}}$	"Not" Memory Expansion Violation	123
$\overline{\text{MLOST}}$	"Not" Memory Lost	124
$\overline{\text{MPCND}}$	"Not" Memory Protect Conditional	125
$\overline{\text{MPCK}}$	"Not" Memory Protect Check	126
$\overline{\text{MPINTON}}$	"Not" Memory Protect Interrupt On	127
MPPCND	Microprogrammable Processor Port Conditional	128
$\overline{\text{MPPAEN}}$	"Not" Microprogrammable Processor Port A Enable	129
$\overline{\text{MPPBEN}}$	"Not" Microprogrammable Processor Port B Enable	281
$\overline{\text{MPPAST}}$	"Not" Microprogrammable Processor Port A Store	130
$\overline{\text{MPPBST}}$	"Not" Microprogrammable Processor Port B Store	282
MPP1SP	Microprogrammable Processor Port 1 Special	131
$\overline{\text{MPP2SP}}$	"Not" Microprogrammable Processor Port 2 Special	132
$\overline{\text{MPV}}$	"Not" Memory Protect Violation	133
OVERFF	Overflow Flip-Flop	135
PARFF	Parity Flip-Flop	136
$\overline{\text{PE}}$	"Not" Parity Error	137
PF	Power Fail	138

Table 2-4. Signal Name Index (Continued)

SIGNAL MNEMONIC	DEFINITION	REF NO.
PLX1	Priority Low Extender 1	139
PLX2	Priority Low Extender 2	140
PON	Power On	141
POPIO	Power On Preset I/O	142
PRH6	Priority High s.c. 6	143
PRH10	Priority High s.c. 10	144
PRL4/PRH5	Priority Low s.c. 4/Priority High s.c. 5	145
PRL7	Priority Low s.c. 7	146
PRL10/PRH11	Priority Low s.c. 10/Priority High s.c. 11	147
PRL11/PRH12	Priority Low s.c. 11/Priority High s.c. 12	148
PRL12/PRH13	Priority Low s.c. 12/Priority High s.c. 13	149
PRL13/PRH14	Priority Low s.c. 13/Priority High s.c. 14	150
PRL14/PRH15	Priority Low s.c. 14/Priority High s.c. 15	151
PRL15/PRH16	Priority Low s.c. 15/Priority High s.c. 16	152
PRL16/PRH17	Priority Low s.c. 16/Priority High s.c. 17	153
PRL17/PRH20	Priority Low s.c. 17/Priority High s.c. 20	154
PRL20/PRH21	Priority Low s.c. 20/Priority High s.c. 21	155
PRL21/PRH22	Priority Low s.c. 21/Priority High s.c. 22	156
PRL22/PRH23	Priority Low s.c. 22/Priority High s.c. 23	157
PRL23/PRH24	Priority Low s.c. 23/Priority High s.c. 24	158
PRL24/PRH25	Priority Low s.c. 24/Priority High s.c. 25	159
PRL25	Priority Low s.c. 25	160
$\overline{\text{PRSTB}}$	"Not" Preset Button	161
PWU	Power Up	162
$\overline{\text{P4NF}}$	"Not" Period 4 Not Freezable	163
$\overline{\text{P5}}$	"Not" Period 5	164
RAR0	ROM Address Register bit 0	166
RAR1	ROM Address Register bit 1	167
RAR2	ROM Address Register bit 2	168
RAR3	ROM Address Register bit 3	169
RAR4	ROM Address Register bit 4	170
RAR5	ROM Address Register bit 5	171
RAR6	ROM Address Register bit 6	172
RAR7	ROM Address Register bit 7	173

Table 2-4. Signal Name Index (Continued)

SIGNAL MNEMONIC	DEFINITION	REF NO.
RAR8	ROM Address Register bit 8	174
RAR9	ROM Address Register bit 9	175
RAR10	ROM Address Register bit 10	176
RAR11	ROM Address Register bit 11	177
RAR12	ROM Address Register bit 12	178
RAR13	ROM Address Register bit 13	179
$\overline{\text{READ}}$	"Not" Read	180
$\overline{\text{REFRESH}}$	"Not" Refresh	181
$\overline{\text{RSPE}}$	"Not" Reset Parity Error	182
$\overline{\text{RIGHT}}$	"Not" Right	183
RME	Reset Memory Expansion	184
$\overline{\text{RMX}}$	"Not" ROM, External	185
ROM0	ROM bit 0	186
ROM1	ROM bit 1	187
ROM2	ROM bit 2	188
ROM3	ROM bit 3	189
ROM4	ROM bit 4	190
ROM5	ROM bit 5	191
ROM6	ROM bit 6	192
ROM7	ROM bit 7	193
ROM8	ROM bit 8	194
ROM9	ROM bit 9	195
ROM10	ROM bit 10	196
ROM11	ROM bit 11	197
ROM12	ROM bit 12	198
ROM13	ROM bit 13	199
ROM14	ROM bit 14	200
ROM15	ROM bit 15	201
ROM16	ROM bit 16	202
ROM17	ROM bit 17	203
ROM18	ROM bit 18	204
ROM19	ROM bit 19	205
ROM20	ROM bit 20	206
ROM21	ROM bit 21	207
ROM22	ROM bit 22	208

Table 2-4. Signal Name Index (Continued)

SIGNAL MNEMONIC	DEFINITION	REF NO.
ROM23	ROM bit 23	209
RUN	Run	210
RUNB	Run Button	211
RUNEN	Run Enable	212
RUNFF	Run Flip-Flop	213
SB0	S-Bus bit 0	214
SB1	S-Bus bit 1	215
SB2	S-Bus bit 2	216
SB3	S-Bus bit 3	217
SB4	S-Bus bit 4	218
SB5	S-Bus bit 5	219
SB6	S-Bus bit 6	220
SB7	S-Bus bit 7	221
SB8	S-Bus bit 8	222
SB9	S-Bus bit 9	223
SB10	S-Bus bit 10	224
SB11	S-Bus bit 11	225
SB12	S-Bus bit 12	226
SB13	S-Bus bit 13	227
SB14	S-Bus bit 14	228
SB15	S-Bus bit 15	229
SCB0	Select Code Bit 0	230
SCB1	Select Code Bit 1	231
SCB2	Select Code Bit 2	232
SCB3	Select Code Bit 3	233
SCB4	Select Code Bit 4	234
SCB5	Select Code Bit 5	235
SCL0	Select Code Least significant bit 0	236
SCL1	Select Code Least significant bit 1	237
SCL2	Select Code Least significant bit 2	238
SCL3	Select Code Least significant bit 3	239
SCL4	Select Code Least significant bit 4	240
SCL5	Select Code Least significant bit 5	241
SCL6	Select Code Least significant bit 6	242
SCL7	Select Code Least significant bit 7	243

Table 2-4. Signal Name Index (Continued)

SIGNAL MNEMONIC	DEFINITION	REF NO.
SCM1	Select Code Most significant bit 1	244
SCM2	Select Code Most significant bit 2	245
SFC	Skip if Flag is Clear	246
$\overline{\text{SFP}}$	"Not" Standard Front Panel	247
SFS	Skip if Flag is Set	248
SIR	Set Interrupt Request	249
SKF	Skip on Flag	250
SRQ10	Service Request s.c. 10	253
SRQ11	Service Request s.c. 11	254
SRQ12	Service Request s.c. 12	255
SRQ13	Service Request s.c. 13	256
SRQ14	Service Request s.c. 14	257
SRQ15	Service Request s.c. 15	258
SRQ16	Service Request s.c. 16	259
SRQ17	Service Request s.c. 17	260
SRQ20	Service Request s.c. 20	261
SRQ21	Service Request s.c. 21	262
SRQ22	Service Request s.c. 22	263
SRQ23	Service Request s.c. 23	264
SRQ24	Service Request s.c. 24	265
SRQ25	Service Request s.c. 25	266
STC	Set Control	267
STF	Set Flag	268
$\overline{\text{STORE}}$	"Not" Store	269
$\overline{\text{STOV}}$	"Not" Set Overflow	270
$\overline{\text{STROBE}}$	"Not" Strobe	271
$\overline{\text{SYNX}}$	"Not" Synchronize, External	272
TA	Time A	273
TB	Time B	274
TC	Time C	275
$\overline{\text{TEN}}$	"Not" T-register Enable	276
$\overline{\text{TST}}$	"Not" T-register Store	277
T3	Time 3	278
$\overline{\text{WRITE}}$	"Not" Write	279

Table 2-5. Signal Distribution List

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
														1
														2
														3
											22	65		4
									32		8	79		5
														6
														7
											14	73		8
														9
														10
														11
														12
														13
56	56	56	56	56	56	56	56	56						14
51	51	51	51	51	51	51	51	51						15
10	10	10	10	10	10	10	10	10						16
														17
														18
														19
57	57	57	57	57	57	57	57	57						20
81	81	81	81	81	81	81	81	81						21
														22
														23
														24
														25

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
A12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
3	73	73	73	73	73	73	73	73	73	73	73					
67	67	67	67	67	67	67	67	67	67	67	67					
8	18	18	18	18	18	18	18	18	18	18	18					
21	21	21	21	21	21	21	21	21	21	21	21	66				
7	7	7	7	7	7	7	7	7	7	7	7		80			
3	13	13	13	13	13	13	13	13	13	13	13	74				
													13	18		
												56		56	56	56
												41		51	51	51
												10		10	10	10
												25				
												14				
												83				
												67		57	57	57
												81		81	81	81
												55				
												59				
												17				

ENOTES SIGNAL SOURCE.  DENOTES BIDIRECTIONAL SIGNAL. DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3	I/O S.C. 10	I/O S.C. 11	I/O
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP							
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
1	$\overline{\text{BIOI}}$					44				73	73	
2	$\overline{\text{BIOO}}$					67				67	67	
3	$\overline{\text{BIOS}}$					31				18	18	
4	CLC					29				21	21	
5	CLF					17				7	7	
6	$\overline{\text{CLKX}}$			30								
7	$\overline{\text{CLXEN}}$			32								
8	CRS					23				13	13	
9	$\overline{\text{CTL5}}$											
10	$\overline{\text{DECM}}$	20						20				
11	$\overline{\text{DIEN}}$	27						27				
12	$\overline{\text{DISPLAY}}$	24						24				
13	$\overline{\text{DIST}}$	26						26				
14	$\overline{\text{DMACYC}}$						26					
15	$\overline{\text{DMAEN}}$						23					
16	$\overline{\text{DMAFRZ}}$						4					
17	$\overline{\text{DMAIOI}}$						20					
18	$\overline{\text{DMAIOO}}$						7					
19	$\overline{\text{DMALCH}}$						83					
20	$\overline{\text{DMALO}}$						69					
21	$\overline{\text{DMAREAD}}$											
22	$\overline{\text{DMARQI}}$			20			24					
23	$\overline{\text{DMARQ2}}$			18			31					
24	$\overline{\text{DMARQ3}}$			28			40					
25	$\overline{\text{DMASTRB}}$			26			28					

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

D

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
														26
														27
														28
														29
									10		61			30
											45	42		31
														32
														34
									3	63				35
														36
														37
														38
														39
														40
77	77	77	77	77	77	77	77	77		9	78			41
														42
														43
														44
														45
														46
														47
														48
														49
														50

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
A12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
2	62	62	62	62	62	62	62	62	62	62	62					
6	46	46	46	46	46	46	46	46	46	46	46		41			
													57			
49	4 / 49	4 / 49	4 / 49	4 / 49	4											
					49	4 / 49	4 / 49	4 / 49	4 / 49	4 / 49	4 / 49					
													29			
													17			
0	10	10	10	10	10	10	10	10	10	10	10	77	77	77	77	77
												79	79			
8	8	8	8	8	8											

NOTES SIGNAL SOURCE. DENOTES BIDIRECTIONAL SIGNAL . DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
26	$\overline{\text{DSPCL}}$	35						35				
27	$\overline{\text{DSPEN}}$	33						33				
28	$\overline{\text{DSPST}}$	34						34				
29	$\overline{\text{ECSEN}}$		38									
30	EDT					63				62	62	
31	ENF					58				46	46	
32	EXFF	29						29				
34	$\overline{\text{FTCH}}$						27					
35	$\overline{\text{FLASH}}$					49			J4-3			
36	FLG1					61				4 / 49	4 / 49	4
37	FLG2					45						
38	$\overline{\text{FLG5}}$						16					
39	HLTB	31						31				
40	$\overline{\text{HLTPE}}$						8					
41	IAK					16				10	10	
42	$\overline{\text{IA0}}$			48								
43	$\overline{\text{IA1}}$			46								
44	$\overline{\text{IA2}}$			44								
45	$\overline{\text{IA3}}$			42								
46	$\overline{\text{IA4}}$			40								
47	$\overline{\text{IA5}}$			33								
48	$\overline{\text{IBL}}$	17						17				
49	IEN5						79					
50	IEN10					20				8	8	

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
														51
														52
														53
														54
														55
														56
														57
														58
														59
														60
														61
														62
														63
														64
														65
														66
														67
														68
														69
														70
														71
														72
											20	67		73
														74
											23	64		75

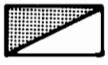
2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
						8	8	8	8	8	8					
													76			
35	26 35	26 35	26 35	26 35	26 35	26 35	26 35	26 35	26 35	26 35	26 35					
38	29 38	29 38	29 38	29 38	29 38	29 38	29 38	29 38	29 38	29 38	29 38					
41	30 41	30 41	30 41	30 41	30 41	30 41	30 41	30 41	30 41	30 41	30 41					
45	64 45	64 45	64 45	64 45	64 45	64 45	64 45	64 45	64 45	64 45	64 45					
42	77 42	77 42	77 42	77 42	77 42	77 42	77 42	77 42	77 42	77 42	77 42					
51	80 51	80 51	80 51	80 51	80 51	80 51	80 51	80 51	80 51	80 51	80 51					
53	81 53	81 53	81 53	81 53	81 53	81 53	81 53	81 53	81 53	81 53	81 53					
52	84 52	84 52	84 52	84 52	84 52	84 52	84 52	84 52	84 52	84 52	84 52					
54	27 54	27 54	27 54	27 54	27 54	27 54	27 54	27 54	27 54	27 54	27 54					
56	28 56	28 56	28 56	28 56	28 56	28 56	28 56	28 56	28 56	28 56	28 56					
58	31 58	31 58	31 58	31 58	31 58	31 58	31 58	31 58	31 58	31 58	31 58					
55	60 55	60 55	60 55	60 55	60 55	60 55	60 55	60 55	60 55	60 55	60 55					
57	78 57	78 57	78 57	78 57	78 57	78 57	78 57	78 57	78 57	78 57	78 57					
61	79 61	79 61	79 61	79 61	79 61	79 61	79 61	79 61	79 61	79 61	79 61					
65	82 65	82 65	82 65	82 65	82 65	82 65	82 65	82 65	82 65	82 65	82 65					
74	83 74	83 74	83 74	83 74	83 74	83 74	83 74	83 74	83 74	83 74	83 74					
5	15	15	15	15	15	15	15	15	15	15	15	68	68			
													66			
4	24	24	24	24	24	24	24	24	24	24	24	63	63			

NOTES SIGNAL SOURCE.



DENOTES BIDIRECTIONAL SIGNAL.

DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
51	IEN20					7						
52	$\overline{\text{INCI}}$						74					
53	$\overline{\text{INCM}}$	19						19				
54	$\overline{\text{INSTEP}}$	18						18				
55	INTL	44						44				
56	$\overline{\text{INTX}}$			36								
57	IOB0					68				26 / 35	26 / 35	26
58	IOB1					66				29 / 38	29 / 38	29
59	IOB2					72				30 / 41	30 / 41	30
60	IOB3					71				64 / 45	64 / 45	64
61	IOB4					74				77 / 42	77 / 42	77
62	IOB5					73				80 / 51	80 / 51	80
63	IOB6					76				81 / 53	81 / 53	81
64	IOB7					75				84 / 52	84 / 52	84
65	IOB8					78				27 / 54	27 / 54	27
66	IOB9					77				28 / 56	28 / 56	28
67	IOB10					80				31 / 58	31 / 58	31
68	IOB11					79				60 / 55	60 / 55	60
69	IOB12					82				78 / 57	78 / 57	78
70	IOB13					81				79 / 61	79 / 61	79
71	IOB14					84				82 / 65	82 / 65	82
72	IOB15					83				83 / 74	83 / 74	83
73	IOG					25				15	15	1
74	$\overline{\text{IOGSP}}$						70					
75	IOI					30				24	24	2

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

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Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
											19	68		76
														77
														78
														79
														80
											3	84		81
									34		5			82
									38		7			83
33	33	33	33	33	33	33	33	33						84
														85
														86
														87
														88
														89
25	25	25	25	25	25	25	25	25						90
73	73	73	73	73	73	73	73	73						91
72	72	72	72	72	72	72	72	72						92
61	61	61	61	61	61	61	61	61						93
54	54	54	54	54	54	54	54	54						94
52	52	52	52	52	52	52	52	52						95
50	50	50	50	50	50	50	50	50						96
46	46	46	46	46	46	46	46	46						97
42	42	42	42	42	42	42	42	42						98
37	37	37	37	37	37	37	37	37						99
32	32	32	32	32	32	32	32	32						100

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
0	20	20	20	20	20	20	20	20	20	20	20	67	67			
						33	6									
							33	6								
3	6							33	6							
	33	6							33	6						
		33	6							33	6		83			
			33	6							33					
				33	6											
													25		33	33
														25	25	25
															73	73
												72	72	72	72	72
												61	61	61	61	61
												54	54	54	54	54
												52	52	52	52	52
												50	50	50	50	50
												46	46	46	46	46
												42	42	42	42	42
												37	37	37	37	37
												32	32	32	32	32

NOTES SIGNAL SOURCE.

DENOTES BIDIRECTIONAL SIGNAL.

DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3	I/O S.C. 10	I/O S.C. 11	I/O
		Δ OPREATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP							
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
76	IOO					26				20	20	2
77	IRQ1					38				33	6	
78	IRQ2					36					33	
79	IRQ3					10						3
80	IRQ4					8						
81	IRQ5					4						
82	IRQ6					13						
83	IRQ7					11						
84	$\overline{\text{IRST}}$				36		12					
85	$\overline{\text{LEFT}}$	22						22				
86	LR0				46							
87	LR1				44							
88	LR2				42							
89	LR3				40							
90	$\overline{\text{MBEN}}$						29					
91	$\overline{\text{MBUSY}}$						73					
92	MB0						67					
93	MB1						65					
94	MB2						63					
95	MB3						61					
96	MB4						59					
97	MB5						57					
98	MB6						55					
99	MB7						53					
100	MB8						51					

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

DE

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
28	28	28	28	28	28	28	28	28						101
24	24	24	24	24	24	24	24	24						102
20	20	20	20	20	20	20	20	20						103
16	16	16	16	16	16	16	16	16						104
12	12	12	12	12	12	12	12	12						105
8	8	8	8	8	8	8	8	8						106
4	4	4	4	4	4	4	4	4						107
67	67	67	67	67	67	67	67	67						108
83	83	83	83	83	83	83	83	83						109
79	79	79	79	79	79	79	79	79						110
75	75	75	75	75	75	75	75	75						111
68	68	68	68	68	68	68	68	68						112
62	62	62	62	62	62	62	62	62						113
55	55	55	55	55	55	55	55	55						114
21	21	21	21	21	21	21	21	21						115
17	17	17	17	17	17	17	17	17						116
13	13	13	13	13	13	13	13	13						117
5	5	5	5	5	5	5	5	5						118
														119
														120
34	34	34	34	34	34	34	34	34						121
36	36	36	36	36	36	36	36	36						122
														123
										6		80		124
														125

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
												28	28	28	28	28
												24	24	24	24	24
												20	20	20	20	20
												16	16	16	16	16
												12	12	12	12	12
												8	8	8	8	8
												4	4	4	4	4
														67	67	67
														83	83	83
														79	79	79
														75	75	75
														68	68	68
														62	62	62
														55	55	55
														21	21	21
														17	17	17
														13	13	13
														5	5	5
														22		
														33		
														34	34	34
														36	36	36
													73	73		
													5	6		

ENOTES SIGNAL SOURCE. DENOTES BIDIRECTIONAL SIGNAL . DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
101	MB9						49					
102	MB10						46					
103	MB11						43					
104	MB12						41					
105	MB13						37					
106	MB14						35					
107	MB15						33					
108	$\overline{\text{MEBEN}}$											
109	MEB10											
110	MEB11											
111	MEB12											
112	MEB13											
113	MEB14											
114	MEB15											
115	MEB16											
116	MEB17											
117	MEB18											
118	MEB19											
119	$\overline{\text{MEEN}}$						48					
120	$\overline{\text{MESP}}$						32					
121	$\overline{\text{MEST}}$						39					
122	$\overline{\text{METDIS}}$											
123	$\overline{\text{MEV}}$											
124	$\overline{\text{MLOST}}$						77		J4-6			
125	$\overline{\text{MPCND}}$											

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

DI

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
														126
														127
														128
														129
														130
														131
														132
14	14	14	14	14	14	14	14	14						133
														135
														136
59	59	59	59	59	59	59	59	59						137
														138
														139
														140
26	26	26	26	26	26	26	26	26		2	65	22		141
74	74	74	74	74	74	74	74	74			13	74		142
														143
														144
									40			82		145
														146
														147
														148
														149
														150

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
													56	66		
													18			
													14		14	14
													59	59	59	59
5	66	66	66	66	66	66	66	66	66	66	66			26	26	26
	17	17	17	17	17	17	17	17	17	17	17	73	74	74	74	74
												13				
													81			
												5				
	23															
	3	23														

NOTES SIGNAL SOURCE. DENOTES BIDIRECTIONAL SIGNAL. DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
126	$\overline{\text{MPCK}}$						25					
127	$\overline{\text{MPINTON}}$						10					
128	MPPCND				6							
129	$\overline{\text{MPPAEN}}$				38							
130	$\overline{\text{MPPAST}}$				26							
131	MPP1SP				34							
132	$\overline{\text{MPP2SP}}$				32							
133	$\overline{\text{MPV}}$						14					
135	OVERFF	28						28				
136	PARFF	32						32				
137	$\overline{\text{PE}}$						72					
138	PF	7						7				
139	PLX1			22								
140	PLX2			24								
141	PON					65			J4-2	66	66	6
142	POPIO					27				17	17	1
143	PRH6						5					
144	PRH10					32				23		
145	PRL4/PRH5						81					
146	PRL7						3					
147	PRL10/PRH11									3	23	
148	PRL11/PRH12										3	2
149	PRL12/PRH13											
150	PRL13/PRH14					3						

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

DE

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
														151
														152
														153
														154
														155
														156
														157
														158
														159
														160
														161
										1	68			162
63	63	63	63	63	63	63	63	63						163
														164
													33	166
													31	167
													29	168
													23	169
													22	170
													21	171
													19	172
													17	173
													46	174
													48	175

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
		3	23													
			3	23												
				3	23											
					3	23										
						3	23									
							3	23								
								3	23							
									3	23						
										3	23					
											3					
												76	21	63	63	63

NOTES SIGNAL SOURCE. DENOTES BIDIRECTIONAL SIGNAL . DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
151	PRL14/PRH15											
152	PRL15/PRH16											
153	PRL16/PRH17											
154	PRL17/PRH20					9						
155	PRL20/PRH21											
156	PRL21/PRH22											
157	PRL22/PRH23											
158	PRL23/PRH24											
159	PRL24/PRH25											
160	PRL25											
161	$\overline{\text{PRSTB}}$	16						16				
162	PWU					55			J4 1			
163	$\overline{\text{P4NF}}$						47					
164	$\overline{\text{P5}}$	37						37				
166	RAR0		33									
167	RAR1		31									
168	RAR2		29									
169	RAR3		29									
170	RAR4		22									
171	RAR5		21									
172	RAR6		19									
173	RAR7		17									
174	RAR8		46									
175	RAR9		48									

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

DE

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
													18	176
													20	177
													30	178
													34	179
9	9	9	9	9	9	9	9	9						180
78	78	78	78	78	78	78	78	78						181
														182
														183
														184
														185
													26	186
													27	187
													24	188
													25	189
													8	190
													7	191
													6	192
													5	193
													11	194
													12	195
													13	196
													15	197
													41	198
													39	199
													37	200

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
A12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
												9	9	9	9	9
														78	78	78
													60			
													6	14		

ENOTES SIGNAL SOURCE. DENOTES BIDIRECTIONAL SIGNAL. DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
176	RAR10		18									
177	RAR11		20									
178	RAR12		30									
179	RAR13		34									
180	$\overline{\text{READ}}$						9					
181	$\overline{\text{REFRESH}}$						78					
182	$\overline{\text{RESPE}}$						30					
183	$\overline{\text{RIGHT}}$	21						21				
184	RME											
185	$\overline{\text{RMX}}$		40									
186	ROM0		26									
187	ROM1		27									
188	ROM2		24									
189	ROM3		25									
190	ROM4		8									
191	ROM5		7									
192	ROM6		6									
193	ROM7		5									
194	ROM8		11									
195	ROM9		12									
196	ROM10		13									
197	ROM11		15									
198	ROM12		41									
199	ROM13		39									
200	ROM14		37									

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

D

Table 2-5. Signal Distribution List (Continued)

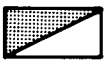
MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
													35	201
													10	202
													9	203
													4	204
													3	205
													47	206
													45	207
													43	208
													42	209
														210
														211
										5		75		212
														213
71	71	71	71	71	71	71	71	71						214
64	64	64	64	64	64	64	64	64						215
58	58	58	58	58	58	58	58	58						216
53	53	53	53	53	53	53	53	53						217
49	49	49	49	49	49	49	49	49						218
45	45	45	45	45	45	45	45	45						219
38	38	38	38	38	38	38	38	38						220
35	35	35	35	35	35	35	35	35						221
31	31	31	31	31	31	31	31	31						222
27	27	27	27	27	27	27	27	27						223
23	23	23	23	23	23	23	23	23						224
19	19	19	19	19	19	19	19	19						225

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
0	50	50	50	50	50	50	50	50	50	50	50					
												71	71	71	71	71
												64	64	64	64	64
												58	58	58	58	58
												53	53	53	53	53
												49	49	49	49	49
												45	45	45	45	45
												38	38	38	38	38
												35	35	35	35	35
												31	31	31	31	31
												27	27	27	27	27
												23	23	23	23	23
												19	19	19	19	19

ENOTES SIGNAL SOURCE.  DENOTES BIDIRECTIONAL SIGNAL . DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
201	ROM15		35									
202	ROM16		10									
203	ROM17		9									
204	ROM18		4									
205	ROM19		3									
206	ROM20		47									
207	ROM21		45									
208	ROM22		43									
209	ROM23		42									
210	RUN					60				50	50	5
211	RUNB	14						14				
212	RUNEN						75		J4-5			
213	RUNFF	15						15				
214	SB0	49					68	49				
215	SB1	48					66	48				
216	SB2	46					64	46				
217	SB3	45					62	45				
218	SB4	43					60	43				
219	SB5	42					58	42				
220	SB6	40					56	40				
221	SB7	39					54	39				
222	SB8	12					52	12				
223	SB9	11					50	11				
224	SB10	9					46	9				
225	SB11	8					44	8				

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

DI

Table 2-5. Signal Distribution List (Continued)

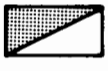
MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
15	15	15	15	15	15	15	15	15						226
11	11	11	11	11	11	11	11	11						227
7	7	7	7	7	7	7	7	7						228
3	3	3	3	3	3	3	3	3						229
														230
														231
														232
														233
														234
														235
														236
														237
														238
														239
														240
														241
														242
														243
														244
														245
									36		6	81		246
														247
											26	61		248
											31	56		249
											11	76		250

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
												15	15	15	15	15
												11	11	11	11	11
												7	7	7	7	7
												3	3	3	3	3
												22	22			
												26	26			
												30	30			
												33	33			
												34	34			
												51	51			
					34	16										
						34	16									
6							34	16								
4	16							34	16							
	34	16							34	16						
		34	16							34	16					
			34	16							34					
				34	16											
37	14 / 37	14 / 37	14 / 37	14 / 37	14											
					37	14 / 37	14 / 37	14 / 37	14 / 37	14 / 37	14 / 37					
	5	5	5	5	5	5	5	5	5	5	5		82			
5	25	25	25	25	25	25	25	25	25	25	25	62	62			
2	32	32	32	32	32	32	32	32	32	32	32		55			
2	12	12	12	12	12	12	12	12	12	12	12	75	75			

NOTES SIGNAL SOURCE.  DENOTES BIDIRECTIONAL SIGNAL . DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
226	SB12	6					42	6				
227	SB13	5					38	5				
228	SB14	3					36	3				
229	SB15	2					34	2				
230	SCB0			16			11					
231	SCB1			14			13					
232	SCB2			12			15					
233	SCB3			10			17					
234	SCB4			8			19					
235	SCB5			6			21					
236	SCL0					24				16		
237	SCL1					42				34	16	
238	SCL2					34					34	1
239	SCL3					43						3
240	SCL4					41						
241	SCL5					39						
242	SCL6					37						
243	SCL7					35						
244	SCM1					46				14 / 37	14 / 37	14
245	SCM2					15						
246	SFC					14				5	5	5
247	$\overline{\text{SFP}}$	30						30				
248	SFS					33				25	25	2
249	SIR					40				32	32	3
250	SKF					22				12	12	1

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

DE

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
									30		24			253
									28		25			254
									26		46			255
									24		56			256
									22		55			257
									20		58			258
									18		57			259
									16		60			260
									14		59			261
														262
														263
														264
														265
														266
											21	66		267
											10	77		268
														269
														270
														271
														272
60	60	60	60	60	60	60	60	60						273
18	18	18	18	18	18	18	18	18						274
22	22	22	22	22	22	22	22	22						275

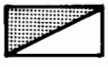
2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
9																
	19															
		19														
			19													
				19												
					19											
						19										
							19									
								19								
									19							
										19						
											19					
2	22	22	22	22	22	22	22	22	22	22	22	65	65			
9	9	9	9	9	9	9	9	9	9	9	9	78	78			
												60		60	60	60
												18			18	18
												21			22	22

:NOTES SIGNAL SOURCE.



DENOTES BIDIRECTIONAL SIGNAL .

DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3	I/O S.C. 10	I/O S.C. 11	I/O
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP							
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
253	SRQ10									19		
254	SRQ11										19	
255	SRQ12											
256	SRQ13											
257	SRQ14											
258	SRQ15											
259	SRQ16											
260	SRQ17											
261	SRQ20											
262	SRQ21											
263	SRQ22											
264	SRQ23											
265	SRQ24											
266	SRQ25											
267	STC					28				22	22	
268	STF					19				9	9	
269	$\overline{\text{STORE}}$	23						23				
270	$\overline{\text{STOV}}$				16							
271	$\overline{\text{STROBE}}$	25						25				
272	$\overline{\text{SYNX}}$			34								
273	TA						71					
274	TB						18					
275	TC						22					

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

D

Table 2-5. Signal Distribution List (Continued)

MEMORY BACKPLANE A5									CROSSOVER PCA A6					
MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	MEMORY PCA P1	DCPC PCA J1	POWER SUPPLY A3			FIRMWARE ACCESSORY BOARD A7	REF. NO.
XA115	XA116	XA117	XA118	XA119	XA120	XA121	XA122	XA123	J1	J2	XA4*	XA5*	J1	
80	80	80	80	80	80	80	80	80						276
82	82	82	82	82	82	82	82	82						277
														278
6	6	6	6	6	6	6	6	6						279
														280
														281
														282

2109A.

Δ SEE FIGURE B-1 FOR J2 AND J3 MPP SIGNAL DISTRIBUTION.

INPUT/OUTPUT BACKPLANE A4

S.C. 12	I/O S.C. 13	I/O S.C. 14	I/O S.C. 15	I/O S.C. 16	I/O S.C. 17	I/O S.C. 20	I/O S.C. 21	I/O S.C. 22	I/O S.C. 23	I/O S.C. 24	I/O S.C. 25	DCPC PCA P1	MEMORY PROTECT PCA P1	MEMORY EXP. MODULE P1	MEMORY PCA P1	MEMORY PCA P1
12	XA13	XA14	XA15	XA16	XA17	XA20	XA21	XA22	XA23	XA24	XA25	XA110	XA111	XA112	XA113	XA114
												80		80	80	80
												82		82	82	82
1	11	11	11	11	11	11	11	11	11	11	11					
												6			6	6

NOTES SIGNAL SOURCE. DENOTES BIDIRECTIONAL SIGNAL . DENOTES SLOTS NOT AVAILABLE IN HP

REF. NO.	SIGNAL	CPU PCA A1						FRONT PANEL PCA A2	POWER SUPPLY A3			
		Δ OPERATOR PANEL PCA A2	FIRMWARE ACCESSORY BOARD A7	I/O EXT HP 12979A	MPP					I/O S.C. 10	I/O S.C. 11	I/O
		J1	J2	J3	J6	XA4	XA5	P1	**	XA10	XA11	XA
276	$\overline{\text{TEN}}$						80					
277	$\overline{\text{TST}}$						82					
278	T3					21				11	11	1
279	$\overline{\text{WRITE}}$						6					
280	$\overline{\text{BSEN}}$		32									
281	$\overline{\text{MPPBEN}}$				28							
282	$\overline{\text{MPPBST}}$				30							

*PINS ACCESSIBLE FOR MAINTENANCE AT TOP OF CROSSOVER PCA A6.

**SEE FIGURE 2-11.

DI

REPLACEABLE PARTS

SECTION III

This section provides a field-replaceable parts listing and an illustrated parts breakdown of the HP 2109A and HP 2113A Microprogrammable Computers. Components parts of most printed-circuit assemblies (PCA's) are not included, since these parts are considered replaceable only at the factory or a depot. Also included in this section is a listing of subassemblies that comprise the HP 2102 Memory System.

3-1. COMPUTER REPLACEABLE PARTS

Tables 3-1 and 3-2, and figures 3-1 and 3-2 list and illustrate the field-replaceable parts of the HP 2109A and HP 2113A Microprogrammable Computers. The replaceable parts are referenced to the exploded views by index numbers. The columns in the index numbered lists provide the following information for each part:

a. FIG & INDEX NO. The figure and index number where the replaceable parts are shown in an exploded view.

b. HP PART NO. The HP part number for each replaceable part.

c. DESCRIPTION. The description of each replaceable part and its applicable reference designation.

d. MFR CODE. A five digit code that denotes the manufacturer of the part. Refer to table 3-4 for a listing of the manufacturers that correspond to the codes.

e. MFR PART NO. The manufacturer's part number for each replaceable part. Commercially obtainable parts are designated OBD (order by description).

f. UNITS PER ASSY. The total quantity of each replaceable part of the computer or memory system.

3-2. MEMORY SYSTEM REPLACEABLE PARTS

Table 3-3 lists the field-replaceable parts of the HP 2102 Memory System. Tables B-2 through B-4 list the replaceable parts for the 16K memory module, 8K memory module, and 4K memory module, respectively. (See Appendix B.)

3-3. OPERATOR PANEL PCA REPLACEABLE PARTS

Table B-1 lists the replaceable parts for the operator panel PCA. (See Appendix B.)

3-4. ORDERING INFORMATION

To order replaceable parts, address the order to the local Hewlett-Packard Sales and Service Office listed at the end of this manual. (For I/O interface PCA or I/O device ordering information, refer to their respective manuals.) The following information should be included in the order for each replaceable parts:

a. Complete model number (including options and accessories) and serial number.

b. Hewlett-Packard part number for each part.

c. Complete description for each part as provided in the replaceable parts lists.

Table 3-1. HP 2109A Computer Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR. PART NO.	UNITS PER ASSY.
3-1-	2109A	MICROPROGRAMMABLE COMPUTER	28480	2109A	1
1	5061-1341	*Central Processor Unit A1	28480	5061-1341	1
2	02108-60023	*Power Supply A3	28480	02108-60023	1
3	Note 1	*Operator Panel PCA A2	28480	5061-1343	1
3A	5040-6076	**Switch (Mint Gray)	28480	5040-6076	13
—	5040-6077	**Switch (Jade Gray)	28480	5040-6077	9
3B	02108-00014	**Contact, Spring	28480	02108-00014	22
3C	1990-0325	**Light Emitting Diode	28480	1990-0325	28
4	02108-60007	*Input/Output Backplane A4	28480	02108-60007	1
5	02108-60021	*Memory Backplane A5	28480	02108-60021	1
6	5060-8345	*Crossover PCA A6	28480	5060-8345	1
7	5061-1336	*Connector Assembly	28480	5061-1336	1
8	Note 2	*Firmware Accessory Board A7	28480	13304-60001	1
9	Note 3	*I/O PCA Cage	28480		1
10	Note 3	*Memory PCA Cage	28480		1
11	3160-0224	*Fan, Tubeaxial	28480	3160-0224	2
	12944A	*Power Fail Recovery System	28480	12944A	1
12A	5060-8346	**Battery Output PCA	28480	5060-8346	1
12B	5060-8347	**Battery Control I PCA	28480	5060-8347	1
12C	5060-8353	**Battery Control II PCA	28480	5060-8353	1
12D	1420-0206	**Battery Pack	28480	1420-0206	1
—	2110-0010	**Fuse, 5A, NB	28480	2110-0010	1
13	02108-60028	*Rear Panel Assembly	28480	02108-60028	1
	02108-00005	**Rear Panel (includes J2, J3, and S2)	28480	02108-00005	1
	0360-0556	**Terminal Block TB1	75382	670A-3	1
	2110-0470	**Fuseholder XF1	75915	345001-010	1
	2110-0056	**Fuse F1, 6A, Fast-Blow (110V operation)	71400	MTH-6	1
	2110-0055	**Fuse, F1, 4A, Fast-Blow (220V operation)	71400	MTH-4	1
	2110-0470	**Fuseholder XF2	75915	345001-010	1
	2110-0010	**Fuse F2, 5A, Normal Blow	71400	MTH-5	1
	3101-0646	**Toggle Switch S1	28480	3101-0646	1
	9135-0018	**Line Filter FL1	28480	9135-0018	1
	1251-3408	**Battery Input Jack J1	27264	03-09-2021	1
14	5068-9836	*Top Cover	28480	5068-9836	1
15	02108-00017	*Side Covers	28480	02108-00017	2
16	02108-00011	*I/O Cage Cover	28480	02108-00011	1
17	5060-9836	*Bottom Cover	28480	5060-9836	1
18	5020-8838	*Strut	28480	5020-8838	4
19	5020-8808	*Rear Frame	28480	5020-8808	1
20	5020-7335	*Front Frame	28480	5020-7335	1
21	4040-0572	*Operator Panel PCA Cover	28480	4040-0572	1
22	1390-0302	*Key	81741	H2007	2
23	1390-0301	*Lock	81741	2242V	1
24	02108-60033	*Switch Assembly	28480	02108-60033	1
25	02108-00032	*Front Shield, Power Supply	28480	02108-00032	1

NOTES:
1. Component level replaceable; see table B-1.
2. HP accessory; shown only for reference.
3. Not field replaceable; shown only for reference.

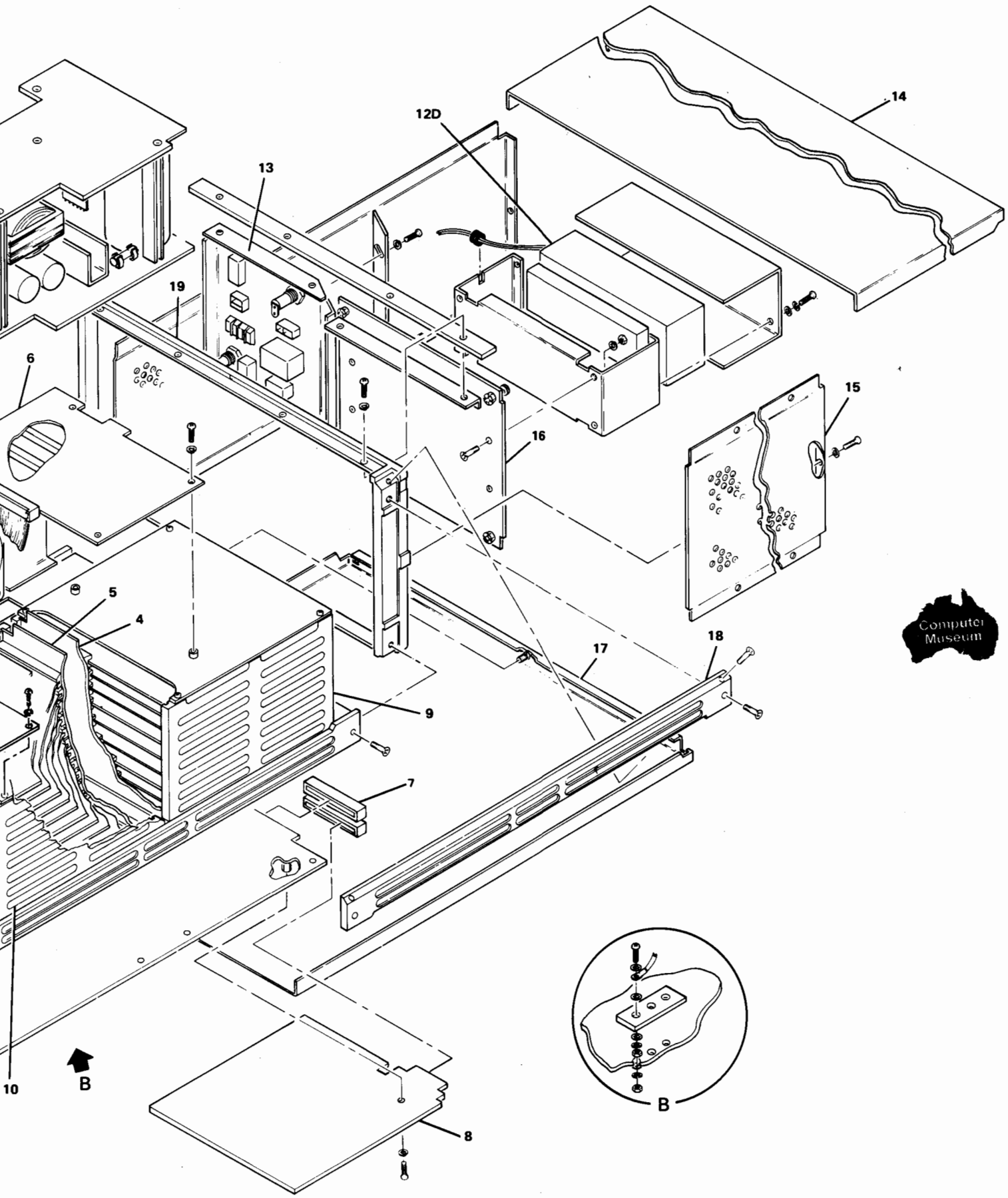


Figure 3-1. HP 2109A Computer Exploded View

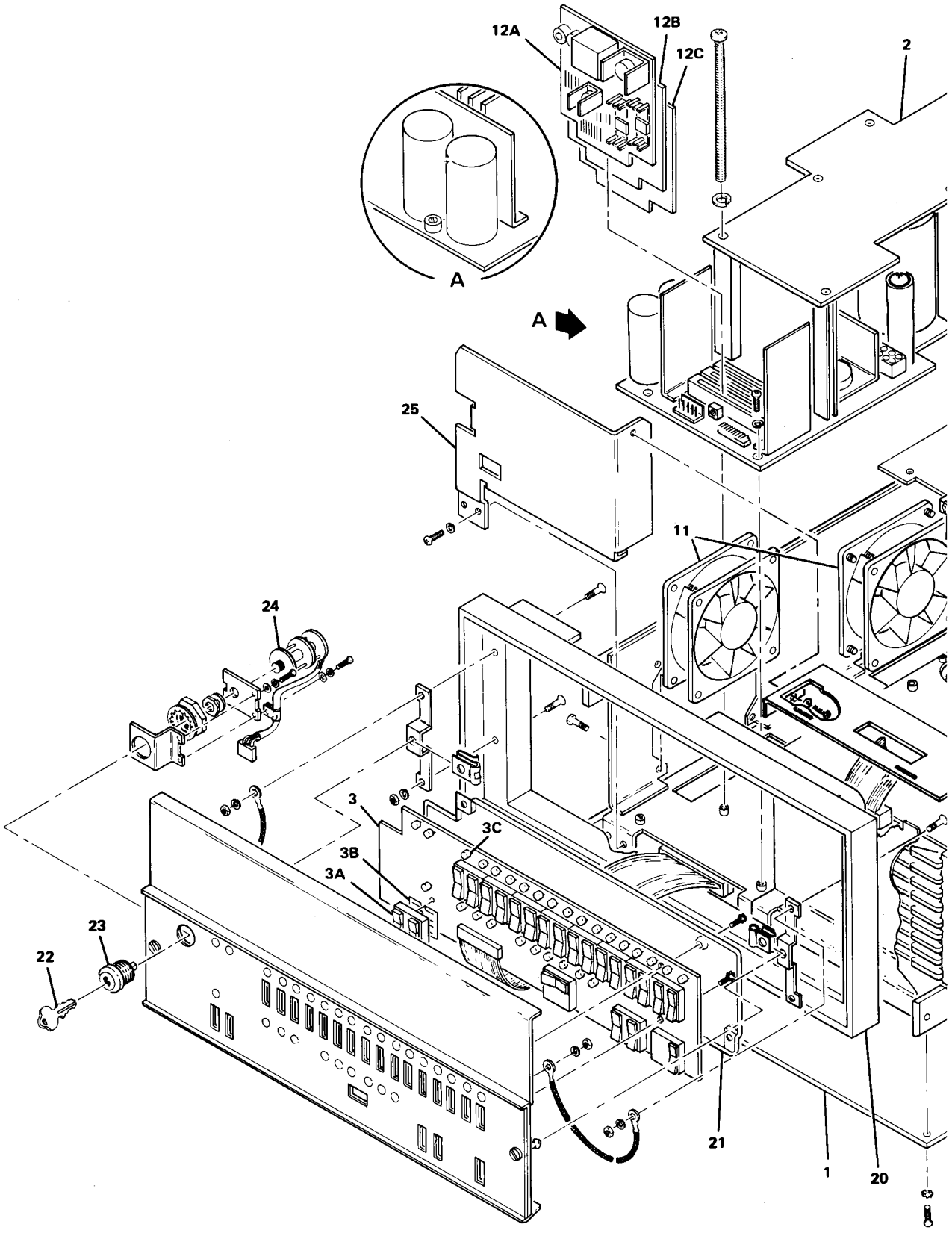

12A
12B
12C
2
A
A
25
11
24
3
3C
3B
3A
23
22
21
1
20

Table 3-2. HP 2113A Computer Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR. PART NO.	UNITS PER ASSY.
3-2-	2113A	MICROPROGRAMMABLE COMPUTER	28480	2113A	1
1	5061-1341	*Central Processor Unit PCA A1	28480	5061-1341	1
2	02112-60006	*Power Supply A3	28480	02112-60006	1
3	Note 1	*Operator Panel PCA A2	28480	5061-1343	1
3A	5040-6076	**Switch (Mint Gray)	28480	5040-6076	13
—	5040-6077	**Switch (Jade Gray)	28480	5040-6077	9
3B	02108-00014	**Contact Spring	28480	02108-00014	22
3C	1990-0325	**Light Emitting Diode	28480	1990-0325	28
4	02112-60001	*Input/Output Backplane A4	28480	02112-60001	1
5	02112-60002	*Memory Backplane A5	28480	02112-60002	1
6	5060-8345	*Crossover PCA A6	28480	5060-8345	1
7	Note 2	*Connector Assembly	28480	5061-1336	1
8	Note 2	*Firmware Accessory Board A7	28480	13304-60001	1
9	Note 3	*I/O PCA Cage	28480		1
10	Note 3	*Memory PCA Cage	28480		1
11	3160-0224	*Fan, Tubeaxial	28480	3160-0224	4
	12991A	*Power Fail Recovery System	28480	12991A	1
12A	02112-60003	**Battery Inverter PCA	28480	02112-60003	1
12B	1420-0206	**Battery Pack	28480	1420-0206	2
—	2110-0001	**Fuse 1A, NB	28480	2110-0001	1
—	2110-0003	**Fuse 3A, NB	28480	2110-0003	1
13	02112-60009	*Rear Panel Assembly	28480	02112-60009	1
	02112-00001	**Rear Panel (includes J1, J3, J4, S1)	28480	02112-00001	1
	0360-0624	**Terminal Block	75382	620A-25	1
	2110-0470	**Fuseholder XF1 and XF2	75915	345001-010	2
	2110-0001	**Fuse F1, 1A, NB	71400	AGC-1	1
	2110-0003	**Fuse F2, 3A, NB	71400	AGC-3	1
	3105-0051	**Circuit Breaker CB1, two-pole, 8A	28480	3105-0051	1
	9135-0030	**Line Filter FL1	28480	9135-0030	1
	1251-3408	**Battery Input Jacks J2 and J5	27264	03-09-2021	2
14	5060-9836	*Top Cover	28480	5060-9836	1
15	5060-9958	*Side Covers	28480	5060-9958	2
16	02112-00013	*I/O Cage Cover	28480	02112-00013	1
17	5060-9836	*Bottom Cover	28480	5060-9836	1
18	5020-8838	*Strut	28480	5020-8838	4
19	5020-8812	*Rear Frame	28480	5020-8812	1
20	5020-7333	*Front Frame	28480	5020-7333	1
21	4040-0572	*Operator Panel PCA Cover	28480	4040-0572	1
22	1390-0302	*Key	81741	H2007	1
23	1390-0301	*Lock	81741	2242V	1
24	02108-60033	*Switch Assembly	28480	02108-60033	1
25	02112-00011	*Front Shield, Power Supply	28480	02112-00011	1

NOTES:
1. Component level replaceable; see table B-1.
2. HP accessory; shown only for reference.
3. Not field replaceable; shown only for reference.

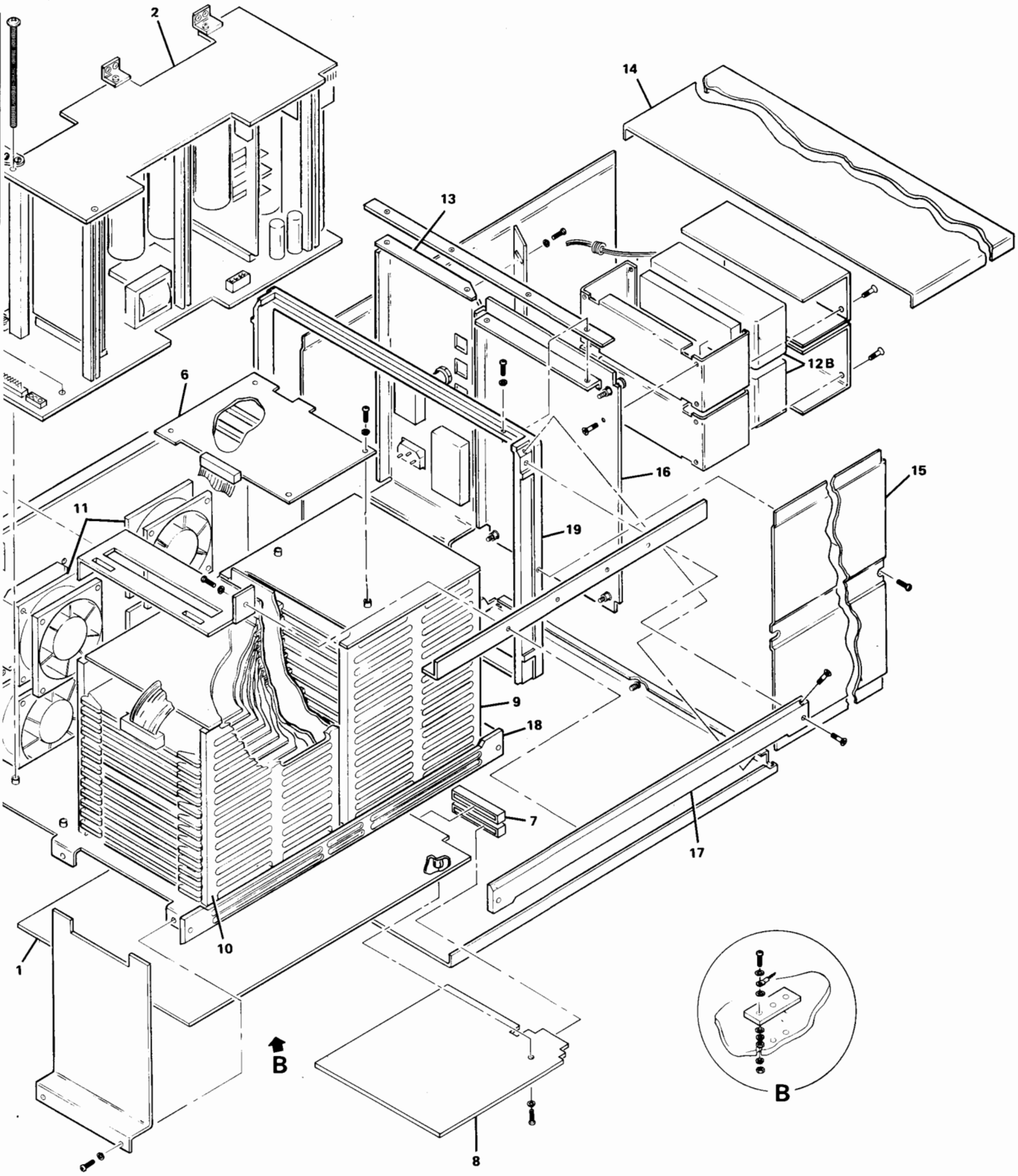
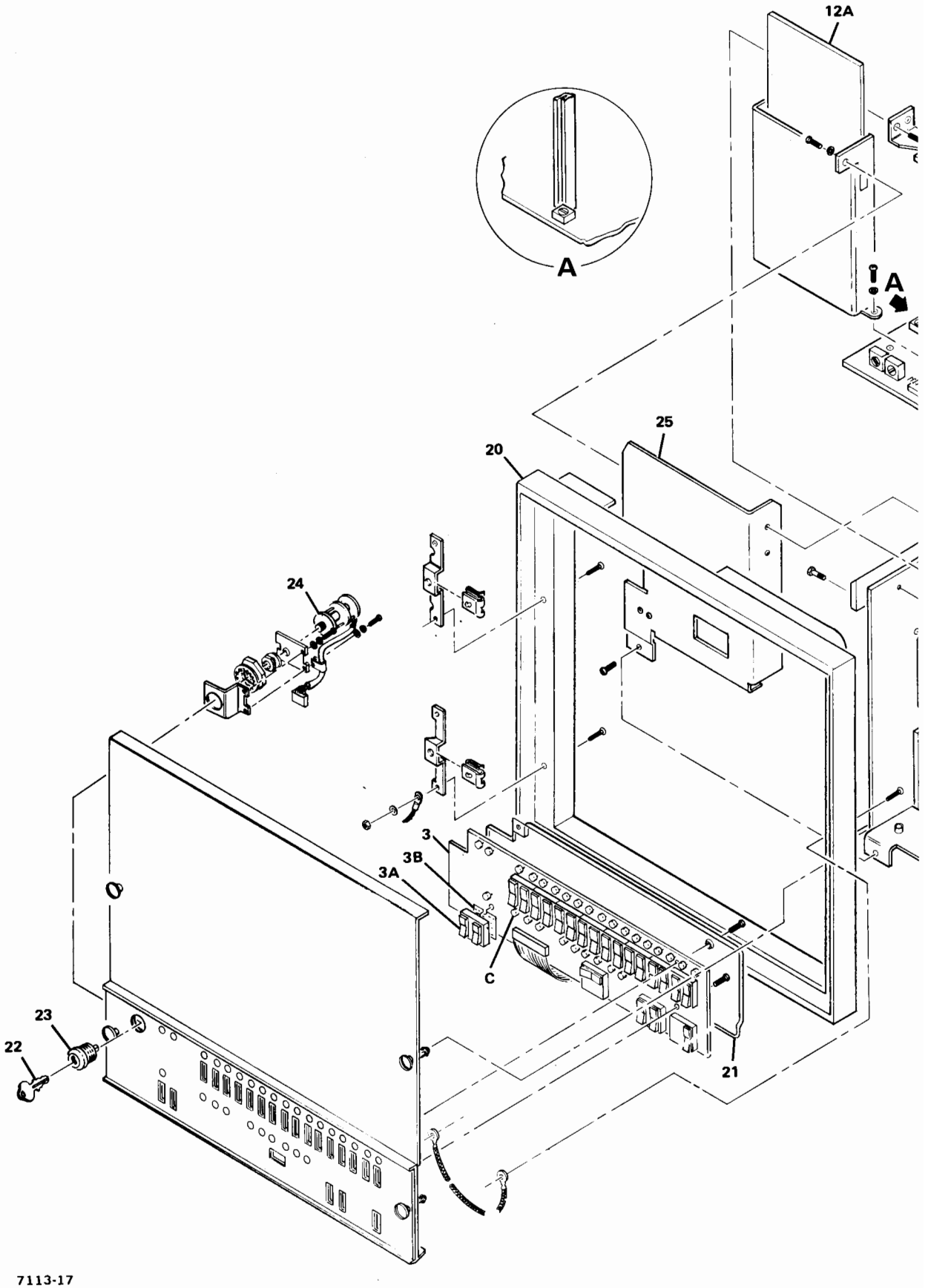


Figure 3-2. HP 2113A Computer Exploded View



7113-17

Table 3-3. Memory System and Accessories Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR. CODE	MFR. PART NO.	UNITS PER ASSY.
—	2102	MOS MEMORY SYSTEM	28480	2102	1
—	5060-8360	*Memory Controller PCA	28480	5060-8360	1
—	Note 1	*16K Memory Module	28480	5061-1332	Note 2
—	Note 3	*8K Memory Module	28480	5060-8359	Note 2
—	Note 4	*4K Memory Module	28480	5060-8369	Note 2
—	02112-60015	*Memory System Cable	28480	02112-60015	1
—	12892B	*Memory Protect	28480	12892-60003	1
—	12897A	*Dual-Channel Port Controller	28480	12897-60001	1
—	12897-60002	**Cable Assembly	28480	12897-60002	1

NOTES:
1. Component level replaceable; see table B-2.
2. Depends on particular installations.
3. Component level replaceable; see table B-3.
4. Component level replaceable; see table B-4.

Table 3-4. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their latest supplements.

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
01-00	Hewlett-Packard Co.		15818	Teledyne Semiconductor Div.	Mt. View, Calif.
	Hewlett-Packard Associates	Palo Alto, Calif.	18324	Signetics Corp.	Sunnyvale, Calif.
02-86	Hewlett-Packard Co.		19701	Mepco/Electra Corp.	Mineral Wells, Tex.
	Santa Clara Division	Santa Clara, Calif.	27264	Molex Products Co.	Downers Grove, Ill.
00736	Gettig Engr & Mfg Co., Inc.	Spring Mills, Penn.	28480	Hewlett-Packard Co.	Palo Alto, Calif.
01121	Allen Bradley Co.	Milwaukee, Wisc.	56289	Sprague Electric Co.	North Adams, Mass.
01295	Texas Instruments Inc.		71400	Bussman Manufacturing Div.,	
	Semiconductor Component Div.	Dallas, Texas		McGraw-Edison Co.	St. Louis, Mo.
04713	Motorola Inc.		75382	Kulka Electric Corp.	Mt. Vernon, NY
	Semiconductor Products Div.	Phoenix, Ariz.	75915	Littlefuse, Inc.	DesPlaines, Ill.
07263	Fairchild Camera and Inst. Corp.		81741	Chicago Lock Co.	Chicago, Ill
	Semiconductor Div.	Mt. View, Calif.	91506	Augat, Inc.	Attleboro, Mass.
07716	TRW Inc., Burlington Div.	Burlington, Iowa			

HP 2102 MEMORY SYSTEM

APPENDIX A

A-1. INTRODUCTION

Appendix A provides theory of operation for the HP 2102 MOS Memory System used in the HP 21MX E-Series Computer. Included are a general description of the memory system and a functional description of the memory PCA.

A-2. GENERAL DESCRIPTION

The memory system consists physically of one memory controller PCA and one or more memory PCA's. The system functions in three cycles; read, write, and refresh.

The read cycle reads out a 16-bit data word from the memory address supplied to it by the CPU and supplies it to the S-bus. The write cycle writes a 16-bit data word into the memory address supplied to it by the CPU. In the write mode, the controller derives a parity bit from the data word supplied to it and stores the parity bit, with the 16-bit data word, in memory. When the data is retrieved in the read mode, the controller again derives the parity of the 16-bit word and checks it against the parity bit supplied from memory. If they disagree, the CPU is notified with an error signal.

The memory is composed of semiconductor integrated circuits (IC's) which require refreshing at least every 2 milliseconds. This is done with a refresh cycle which occurs, automatically, approximately every 32 microseconds. Each refresh cycle refreshes 1/64th of the memory so that the total memory is refreshed, according to requirement, every 2 milliseconds.

The refresh cycle is performed, normally, in I/O "T" periods 2 and 3 but, when it occurs while memory is under DCPC control, it is performed in periods 4 and 5. This leaves periods 2 and 3 for the DCPC read cycle.

The refresh cycle is performed automatically, without external stimulation. When a refresh cycle is started, the CPU is notified so that read and write cycles are inhibited until the refresh cycle is complete.

A-3. READ CYCLE

The read cycle is initiated when the Read signal from the CPU becomes active. The memory address, from the CPU, is supplied to the M-register (on the controller) and memory. It is stored in the M-register to be continually supplied to memory until the data is read out from the stored memory address. The 16-bit data word is read out from memory and stored in the T-register and the parity bit is supplied to the parity circuits. The parity circuits check parity and, after the result of the check is ready, the S-bus gates are opened to enable passage of the memory data word to the S-bus. Also the parity error status is generated to the CPU. Then the controller and memory circuits are restored to the ready-for-new-cycle state.

A-4. WRITE CYCLE

A write cycle begins with data supplied to memory and to the T-register and parity circuits on the memory controller. The T-register stores the data and a parity bit is derived from it by the parity circuits. The address into which the data is to be written is supplied to memory and the M-register and the Write signal to the memory controller is activated by the CPU. Then the memory controller enables writing into memory and the M-register stores the address and becomes the address source for memory. The controller opens the memory gates to pass the data from the T-register to memory and the data is written into the selected address of memory.

A-5. REFRESH CYCLE

A refresh cycle is initiated automatically by an oscillator on the controller PCA. When a refresh cycle starts, reading or writing is disabled by the controller and the CPU is notified that a refresh cycle is in process. A 0-to-63 counter on the controller PCA selects a different row of memory elements to be refreshed by each refresh cycle. Essentially, in a refresh cycle, the controller only indicates the row of memory elements to be refreshed. Refreshing of the memory elements is performed within the memory IC.

A-6. MEMORY ADDRESSING

Memory for the computer is contained on one or more PCA's. Each PCA contains either one or two or four rows of memory IC's. There are 17 IC's in a row, one IC for each bit of the 17-bit memory word. A one-row PCA is referred to as a 4K PCA; the two-row PCA is referred to as an 8K PCA; and the four-row PCA is referred to as a 16K PCA. The 4K, 8K, and 16K descriptions refer to the approximate number of 17-bit memory words the PCA is capable of storing.

NOTE

The word "row" is used in this discussion to refer to two different items: (1) a group of 17 memory IC's arranged in a row on a PCA and (2) a row of 64 memory elements within an IC.

Each IC contains a 64-row by 64-column matrix of memory elements for a total of 4,096 (approximately 4K) memory elements within each IC. A row of 17 such IC's is capable of storing 4,096 17-bit memory words, with each bit of the memory word stored in a separate IC dedicated to that bit. The bits are stored in identical elements in the IC's; that is, the same column and row are addressed on each IC to form the 17-bit word.

A 20-bit address word is used to select a 17-bit word stored in memory. To select a memory word, four items must be identified; the PCA, the row of IC's on the PCA (row 0, 1, 2, or 3), the row of elements within each IC, and the column of elements within each IC. These items and the bits of the memory address used to identify them are listed below.

MEMORY ADDRESS BITS	ITEM IDENTIFIED
13 through 19	PCA
12 and 13	Row (0 through 3) of IC's on the PCA
6 through 11	Column of elements within each IC
0 through 5	Row of elements within each IC

Bits 6 through 11, which identify the column of memory elements, form a 6-bit binary word. The same is true of bits 0 through 5 which identify the row of memory elements. The column and row words are supplied to each IC and are decoded within each IC to select the single designated memory element.

For purposes of refreshing memory, only the 64 rows on each IC are addressed (it isn't necessary to address each individual memory element for refreshing).

A-7. SIGNAL DESCRIPTION

Table A-1 lists all control and status signals used in the memory and provides a brief description of their function.

A-8. MEMORY PCA FUNCTIONAL DESCRIPTION

The following paragraphs describe the operation of each functional unit on a memory PCA. These are the PCA select circuits, the control circuits, the memory IC's, and the bus drivers/receivers.

A-9. PCA SELECT CIRCUITS

The PCA select circuits decode memory address bits 13 through 19 to determine if the PCA on which they are located is the PCA selected for the read or write operation to be performed. The PCA select circuits are composed mainly of miniature switch assembly XW1 and eight exclusive "nor" gates.

Memory address bits 13 through 19 form the PCA select word. One exclusive "nor" gate and one switch are assigned to each bit of the PCA select word. (Bit 12 can be included in the PCA select word by connecting strapping terminals CC on an 8K or 4K memory PCA.) The identity of each memory PCA is established by setting switches A through G for a 16K memory PCA, and switches B through H for an 8K or 4K memory PCA (also switch A if bit 12 is to be included in the PCA select word) to a unique combination of switch settings.

The outputs of all exclusive "nor" gates are tied to a common signal line which supplies the signal to the control circuits which indicates the local PCA is selected. For this signal to be active (high) the outputs of all contributing gates must be high. This occurs only when each bit of the PCA select word matches the input to the exclusive "nor" gate from the associated switch. Thus, the signal from the exclusive "nor" gates which enables the control circuits is only active when the PCA select word matches the PCA identity.

A-10. CONTROL CIRCUITS

The control circuits enable readout from the memory IC's to the T-register, in a read cycle, and supply one of two enabling signals to the memory IC's under conditions determined from the input signals to the control circuits. The enabling signal to the memory IC's is the clock signal, supplied to pin 7 for 16K memory PCA and pin 17 for 8K or 4K memory PCA on the IC. It, together with the CS signal from the controller, is required to enable read, or write operations in the IC's. The CS is not required for refresh operations in the IC's.

The input signals to the control circuits are the CLK, MREF, R/W RR, R/W WR, bit 12 of the memory address word stored in the M-register, and the PCA select signal from the PCA select circuits. The five outputs from the control circuits are four clock signals, one to memory IC row 0, one to row 1, one to row 2, and one to row 3, and the Input Enable (16K) or Transmit Enable signal (8K or 4K) to the bus drivers/receivers. All five signals must be enabled by the PCA select signal which indicates this PCA contains the memory address in the M-register.

The Input Enable (16K) or Transmit Enable signal (8K or 4K) is active (high) when the PCA select signal, CLK signal, and R/W WR signals are active.

The control circuits supply a clock signal to either the row 0, row 1, row 2, or row 3 IC's on a 16K memory PCA when the CLK signal from the controller is active and the MREF signal from the CPU is not active. Memory address bits 12 and 13 select the IC row. If bit 13 and bit 12 are low, row 0 is selected to receive a clock signal; if bit 13 is low and bit 12 is high, row 1 receives a clock signal; if bit 13 is high and bit 12 is low, row 2 receives a clock signal; and if bit 13 and bit 12 are high, row 3 receives a clock signal. On an 8K memory PCA which has two rows (row 0 and row 1), memory address bit 12 selects the IC row. If bit 12 is low, row 0 is selected to receive a clock signal; if bit 12 is high, row 1 receives the clock signal. On a 4K mem-

Table A-1. Memory System Signals

SIGNAL	FUNCTION
$\overline{\text{Read}}$	Initiates a memory read cycle.
$\overline{\text{Write}}$	Initiates a memory write cycle.
$\overline{\text{MPV}}$	Indicates a memory protect violation to the controller. In a DCPC operation, it has no effect. In a normal write mode, no write cycle occurs.
$\overline{\text{DMAEN}}$	Indicates that a DCPC read or write cycle is going to occur. The DCPC is free to read and write in the protected area of memory.
$\overline{\text{DMAREAD}}$	Delays a refresh cycle which might be ready to begin until time periods T4 and T5. (The refresh cycle normally occurs during T2 and T3.) This leaves T2 and T3 for the DCPC read cycle.
$\overline{\text{P4NF}}$ and $\overline{\text{P5NF}}$	The last two P periods occurring in a T period. $\overline{\text{P4NF}}$, together with $\overline{\text{TST}}$, enables read in of data into the T-register in a write cycle. The $\overline{\text{P5NF}}$, which occurs in time period T6 (or T3, if a DCPC read cycle is beginning), enables the refresh cycle to begin if one is due.
TA, TB, and TC	These signals are a binary word which, when decoded, indicate the current T period.
PON	Indicates that the power supply is receiving ac line power and is operating properly. When PON becomes inactive, reading and writing is inhibited and refresh cycles occur every 32 microseconds, independent of conditions external of the memory system.
$\overline{\text{TEN}}$	Opens the S-bus gates to pass data from the T-register to the S-bus after the $\overline{\text{Read}}$ signal has become inactive in a read cycle.
$\overline{\text{TST}}$	Together with the $\overline{\text{P4NF}}$ signal, enables the T-register to store the data from the S-bus in a write operation.
R/W RR	Either this signal or R/W WR is jumpered, on the memory PCA, to select read mode or write refresh mode for the memory IC's. The IC, when enabled by active $\overline{\text{CLK}}$ and $\overline{\text{CS}}$ signals, will read when the jumpered signal is high and write when it is low.
R/W WR	Either this signal or R/W RR is jumpered, on the memory PCA, to select read mode or write refresh mode for the memory IC's. The IC, when enabled by active $\overline{\text{CLK}}$ and $\overline{\text{CS}}$ signals, will read when the jumpered signal is high and write when it is low.
$\overline{\text{CS}}$ and $\overline{\text{CLK}}$	Both signals are required to enable the memory IC's to read or write. Reading or writing is selected by the R/W RR or R/W RW signal.
$\overline{\text{MREF}}$	Informs memory PCA that a refresh cycle is in progress. Used, on the memory PCA, together with the $\overline{\text{CLK}}$ signal, to activate the CLOCK input to the memory IC's during a refresh cycle.
A0 thru A5	These six bits of the memory address word are used, by the refresh circuits, to select the row of memory elements to be refreshed. The bits are in the form of a binary code which is decoded, in the IC, to identify the row of memory elements.
$\overline{\text{MBUSY}}$	Indicates, to the CPU, that the memory system is available for another memory cycle.
$\overline{\text{REFRESH}}$	Indicates, to the CPU, that a refresh cycle is about to begin. Read and write cycles are inhibited during a refresh cycle.
$\overline{\text{PE}}$	Indicates, to the CPU, that the data word read from memory, during the current cycle, contains a parity error.
$\overline{\text{METDIS}}$	Signal generated by DMS for READ protection.

ory PCA, which has only one row (row 0), the clock signal to the IC's is active when bit 12 is low.

The clock signal is supplied to the IC's during all three cycles; read, write, and refresh. If the MREF signal is active (low), as would be the case during a refresh period, rows 0 through 3 will receive a CLK signal.

A-11. MEMORY INTEGRATED CIRCUITS

The memory IC's store the 16 bits of data from the T-register and the parity bit from the controller parity circuits. The row and column in the IC which identifies the individual all into which a "1" or "0" is to be written is specified by bits 0 through 5 (row) and 6 through 11 (column) of the memory address word from the M-register, as previously described. Reading or writing must be enabled by an active (high) clock signal at pin 7 for 16K memory PCA and at pin 17 for 8K or 4K memory PCA and an active (low) CS signal at pin 5 for 8K or 4K memory PCA (SELECT). Reading out the data ("1" or "0") from the selected address is done when the signal at pin 6 for 16K and at pin 12 for 8K or 4K (READ/WRITE) is high (provided the clock and CS signals are active). When the signal at pin 6 for 16K and at pin 12 for 8K or 4K is low and the clock and CS signals are active, a "1" or "0" from the T-register can be written into the selected memory cell.

The signal at pin 6 for 16K memory PCA and at pin 12 for 8K or 4K memory PCA is connected to either the R/W RR or R/W WR signal from the controller, depending on whether terminals AA or BB are connected at strapping option W2 on the 8K memory PCA. If terminals AA are connected, pin 12 is connected to the R/W RR signal and reading out from the memory IC is enabled and writing is inhibited during a refresh cycle. (Actually, no data from the memory IC's reach the T-register during a refresh cycle because the bus drivers/receivers are not transmit-enabled during a refresh cycle.) If terminals BB are connected, the R/W WR signal is connected to pin 12 on the memory IC and writing into the memory IC is enabled and reading out of it is inhibited during a refresh cycle. No data will be written because the CS signal is not active during a refresh cycle.

During a read operation, the data bit is read out through pin 2 for 16K memory PCA and pin 7 for 8K or 4K memory PCA and supplied to the T-register through the bus drivers/receivers. In a write operation, the data bit from the T-register (or parity circuits) is supplied through the bus drivers/receivers to pin 2 for 16K memory PCA and pin 6 for 8K or 4K memory PCA of the memory IC.

A-12. BUS DRIVERS/RECEIVERS

The bus drivers/receivers isolate the T-register, on the memory controller PCA, from the memory IC's. They are constantly enabled for receiving but must be enabled, by the control circuits, to transmit data to the T-register. (Although the bus drivers/receivers never inhibit data from the T-register from being supplied to the memory IC's, the memory gates on the controller PCA allow the T-register to transmit data to the memory IC's only under certain conditions during a write cycle. Also, the memory IC's themselves must be enabled, by the control circuits on the memory PCA, to accept data.)

Transmission of memory data to the T-register, through the bus drivers/receivers, is enabled by the control circuits when the PCA is selected by the memory address word and a read cycle is in progress or if an attempt is being made, while not in DCPC mode, to read out of a protected area of memory which is located on this PCA (CLK signal active (low), R/W WR signal high, and this PCA selected). (Reading out of a protected area is enabled during a DCPC read operation.)

A-13. MEMORY PROTECT VIOLATIONS

The action taken by the memory system when a protected area of memory is addressed depends on several factors: whether the current cycle is a read or write cycle and whether the cycle is a normal CPU-requested cycle or one initiated by the DCPC. In any case, when a memory protect violation occurs, the memory makes no direct attempt to inform the CPU of the violation. That will be done by the memory protect PCA.

A-14. NORMAL READ CYCLE

When a memory protect violation occurs in a normal read cycle, the cycle is completed.

A-15. DCPC READ OR WRITE CYCLE

A DCPC-initiated read or write cycle is completed normally. (The DCPC is allowed to access the protected area of memory.)

A-16. NORMAL WRITE CYCLE

If a protected area of memory is addressed for a normal write cycle, the cycle is not started; because the Write FF will not be set by the Write signal from the CPU. The DMAEN and MPV signals supplied to the memory controller are combined in Nand gate U66B to produce a low level signal to the J input of the Write FF. Then, when the Write signal from the CPU clocks the flip-flop, the flip-flop remains in the reset condition. Since the write cycle must be started by setting the Write FF, the write cycle does not begin.

COMPONENT LEVEL REPAIR

APPENDIX B

Appendix B provides parts location and schematic diagrams and replaceable parts tables for computer assemblies designated for repair at the component level. Assemblies included in this appendix are the operator panel PCA, 16K memory module, 8K memory module, and 4K memory module.

Table B-1. Operator Panel PCA Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru 4, 15, 18	0180-2125	CAPACITOR, fxd, elec, Ta, 15μF, 5%	56289	150D156X5020B2-DYS
C5, 9, 14, 17	0160-0127	CAPACITOR, fxd, cer, 1.0 μF, 20%, 25 VDCW	56289	5C[illegible]C-CML
C6, 8, 10, 11, 13	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80-20%, 100 VDCW	56289	C023F101F[illegible]03ZS22-CDH
C7	0180-0393	CAPACITOR, fxd, elec, Ta, 0.68 μF, 10%, 35 VDC	56289	150D684X[illegible]035A2-DYS
C12, 16	0180-0374	CAPACITOR, fxd, elec, Ta, 10 μF, 10%, 20 VDC	56289	150D106X9020B2-DYS
CR1 thru 28	1990-0529	DIODE, light emitter	01-00	1990-0529
Q1	1854-0477	TRANSISTOR, silicon, NPN	07263	2N2222A
R1 thru 3, 6 thru 10, 13	1810-0080	RESISTOR NETWORK, met flm, 7 × 500 ohms, 5%	56289	200C-1854-CRR
R4, 11	0757-0442	RESISTOR, fxd, flm, 10K, 1%, 0.125W	19701	MF4C, T-O
R5, 12	0757-0280	RESISTOR, fxd, flm, 1K, 1%, 0.125W	07716	CEA, T-O
U1, 3, 12, 26, 27	1820-1624	INTEGRATED CIRCUIT, octal buffer/line driver, TTL	01295	SN74S241N
U2, 4	1820-1677	INTEGRATED CIRCUIT, octal "D" flip-flop, TTL	01295	SN745374N
U5, 13, 28	1820-1633	INTEGRATED CIRCUIT, octal inverting buffer/line driver, TTL	01295	SN74S240N
U6, 10, 11	1820-0661	INTEGRATED CIRCUIT, guad 2-input "or" gate, TTL	01295	SN7432N
U7, 8	1820-0174	INTEGRATED CIRCUIT, hex inverter, TTL	01295	SN7404N
U9	1820-1130	INTEGRATED CIRCUIT, 13-input "nand" gate, TTL	01295	SN74S133N
U14 thru 21	1820-0054	INTEGRATED CIRCUIT, guad 2-input "nand" gate, TTL	01295	SN7400N
U22	1820-1112	INTEGRATED CIRCUIT, dual "D" flip-flop, TTL	01295	SN74LS74N
U23	1820-1416	INTEGRATED CIRCUIT, hex Schmitt-trigger inverter, TTL	01295	SN74LS14N
U24	1820-0511	INTEGRATED CIRCUIT, quad 2-input "and" gate, TTL	01295	SN7408N
U25	1820-1461	INTEGRATED CIRCUIT, octal "D" flip-flop, TTL	01295	SN74273N

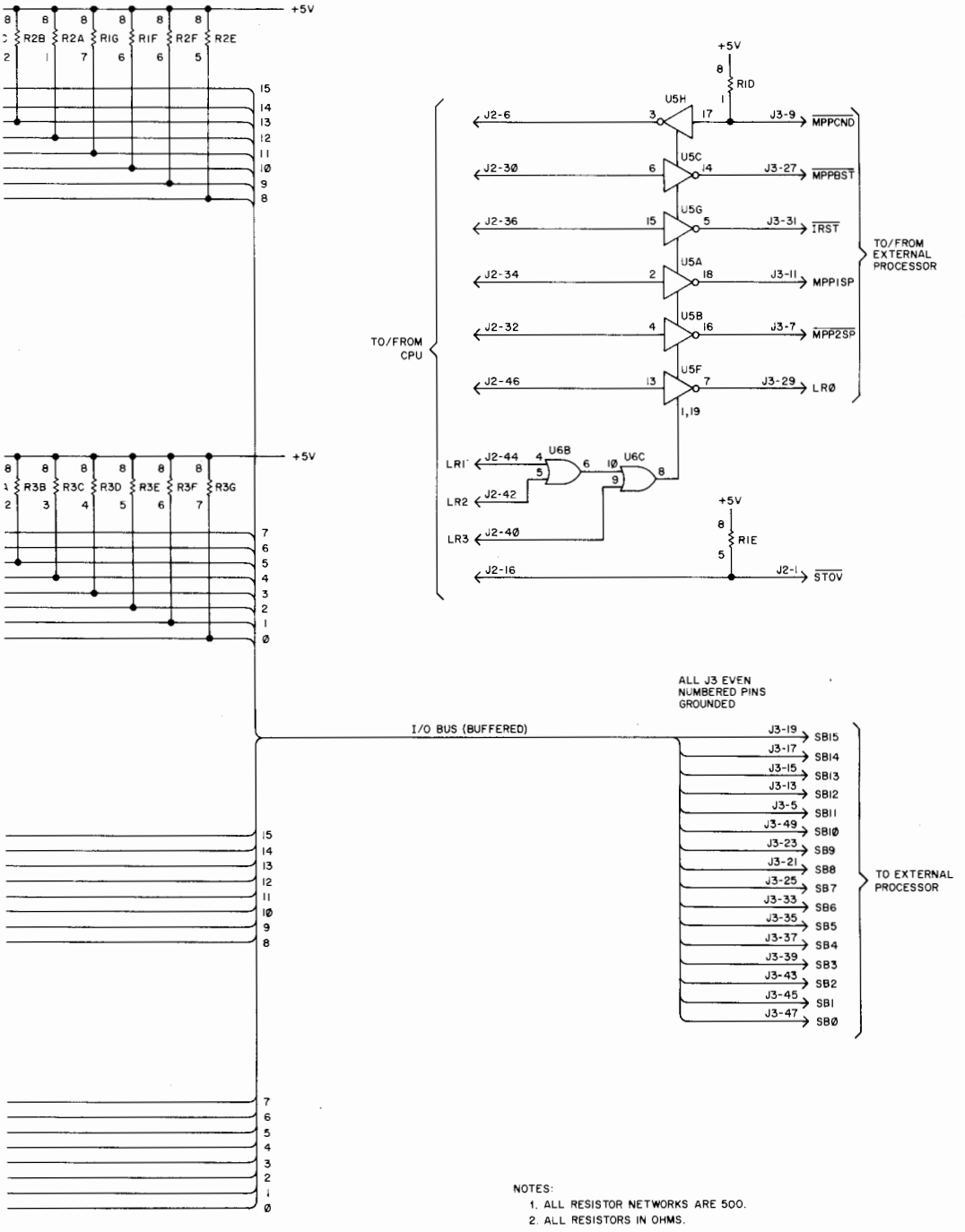
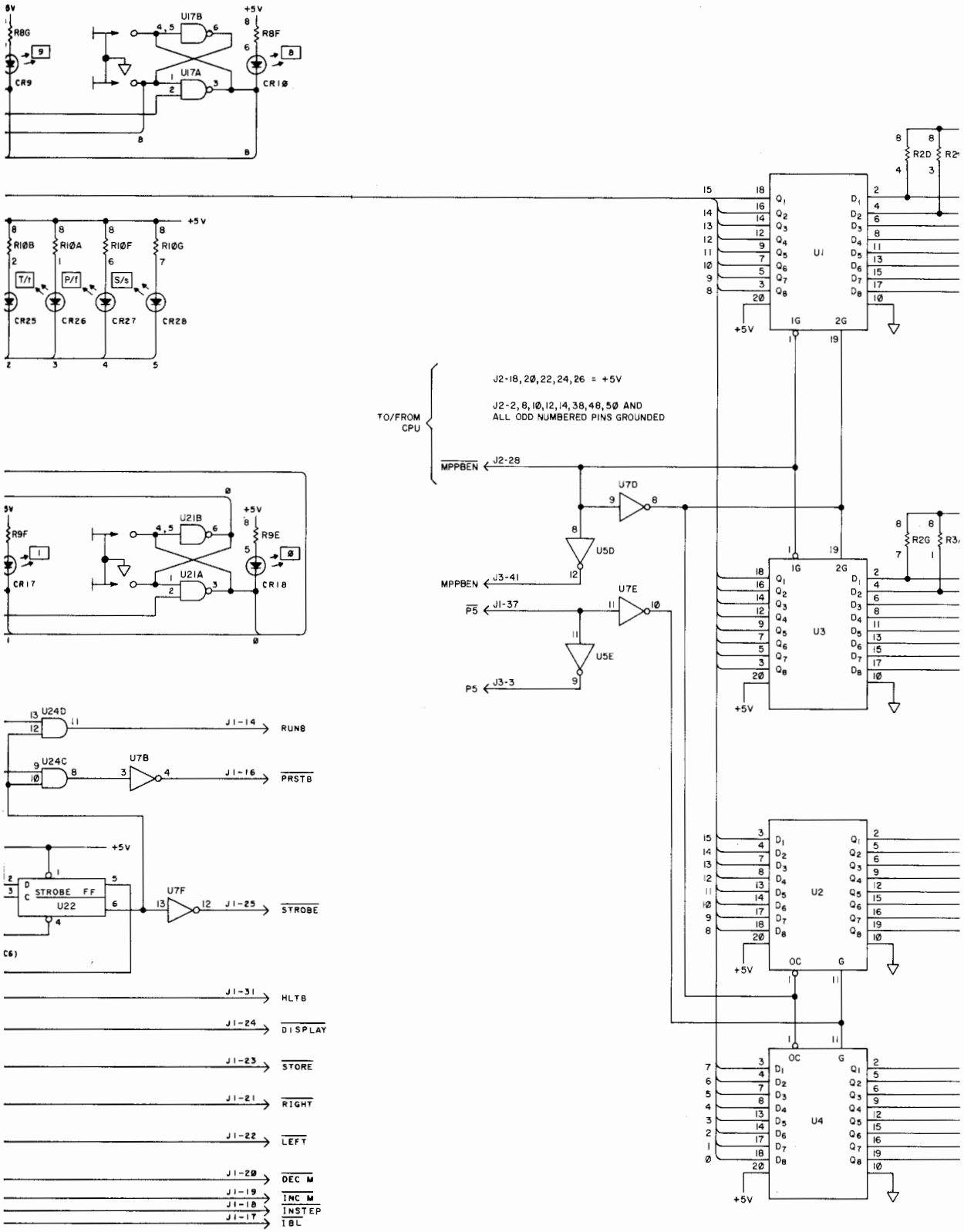
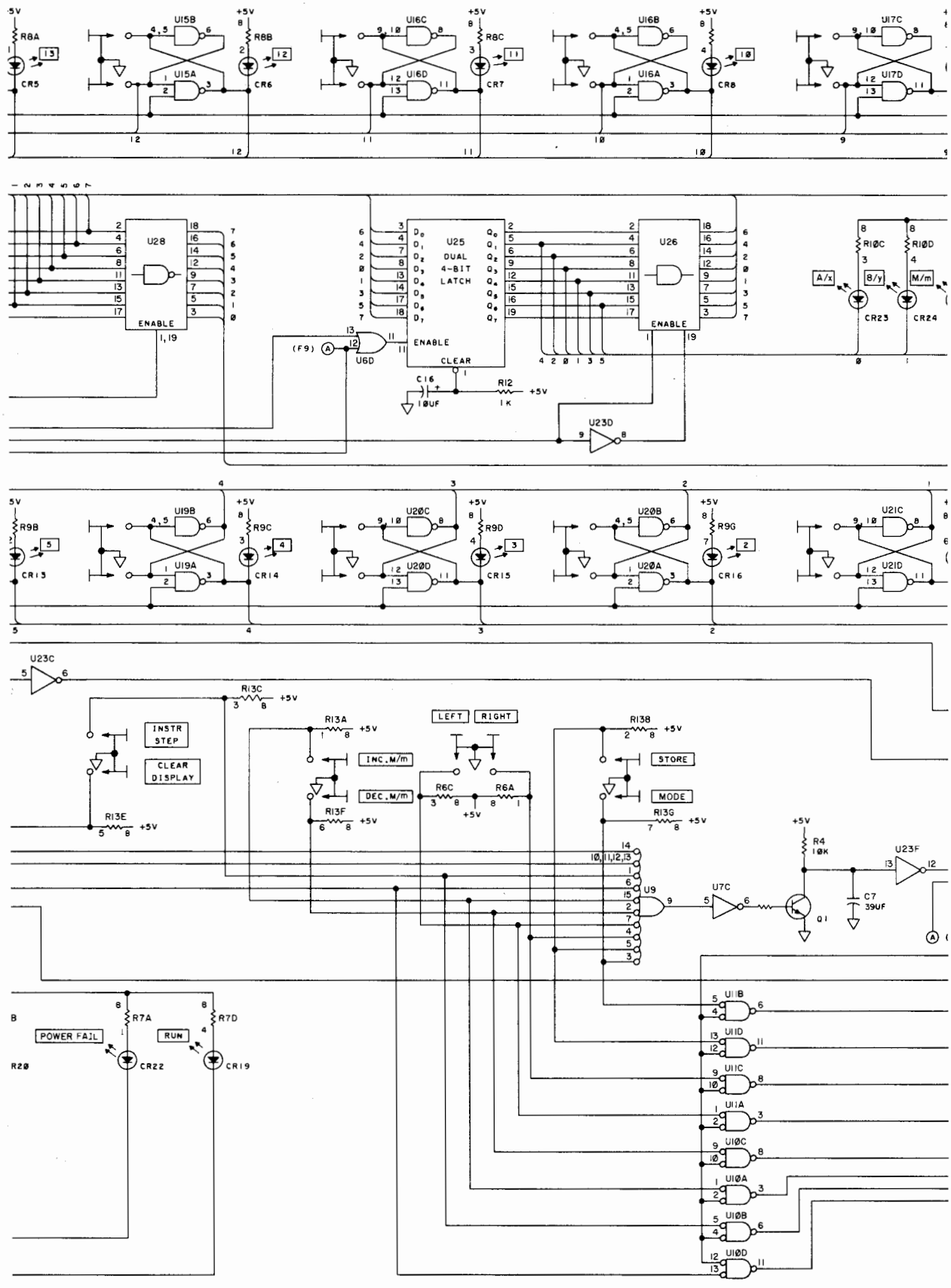


Figure B-1. Operator Panel PCA, Parts Location and Schematic Diagrams


U17B
U17A
R8G
R8F
CR9
CR10
R10B
R10A
R10F
R10G
T/t
P/f
S/s
CR25
CR26
CR27
CR28
U1
U2
U3
U4
R2D
R2G
J2-18,20,22,24,26 = +5V
J2-2,8,10,12,14,38,48,50 AND ALL ODD NUMBERED PINS GROUNDED
TO/FROM CPU
MPPBEN J2-28
U7D
U5D
MPPBEN J3-41
U7E
U5E
P5 J1-37
P5 J3-3
R9F
R9E
CR17
CR18
U21B
U21A
U24D
U24C
U7B
J1-14 RUN8
J1-16 PRSTB
STROBE FF U22
U7F
J1-25 STROBE
J1-31 HLTB
J1-24 DISPLAY
J1-23 STORE
J1-21 RIGHT
J1-22 LEFT
J1-20 DEC M
J1-19 INC M
J1-18 INSTEP
J1-17 IBL
+5V


U15B
U15A
U16C
U16D
U16B
U16A
U17C
U17D
R8A
R8B
R8C
CR5
CR6
CR7
CR8
U28
ENABLE
U25
DUAL
4-BIT
LATCH
CLEAR
U26
U6D
(F9)
C16
10UF
R12
1K
U23D
R10C
R10D
A/x
B/y
M/m
CR23
CR24
U19B
U19A
U20C
U20D
U20B
U20A
U21C
U21D
R9B
R9C
R9D
R9G
CR13
CR14
CR15
CR16
U23C
R13C
R13A
R13B
R13E
R13F
R13G
INSTR STEP
CLEAR DISPLAY
INC.M/m
DEC.M/m
LEFT
RIGHT
STORE
MODE
R6C
R6A
U9
U7C
R4
10K
Q1
C7
39UF
U23F
R7A
R7D
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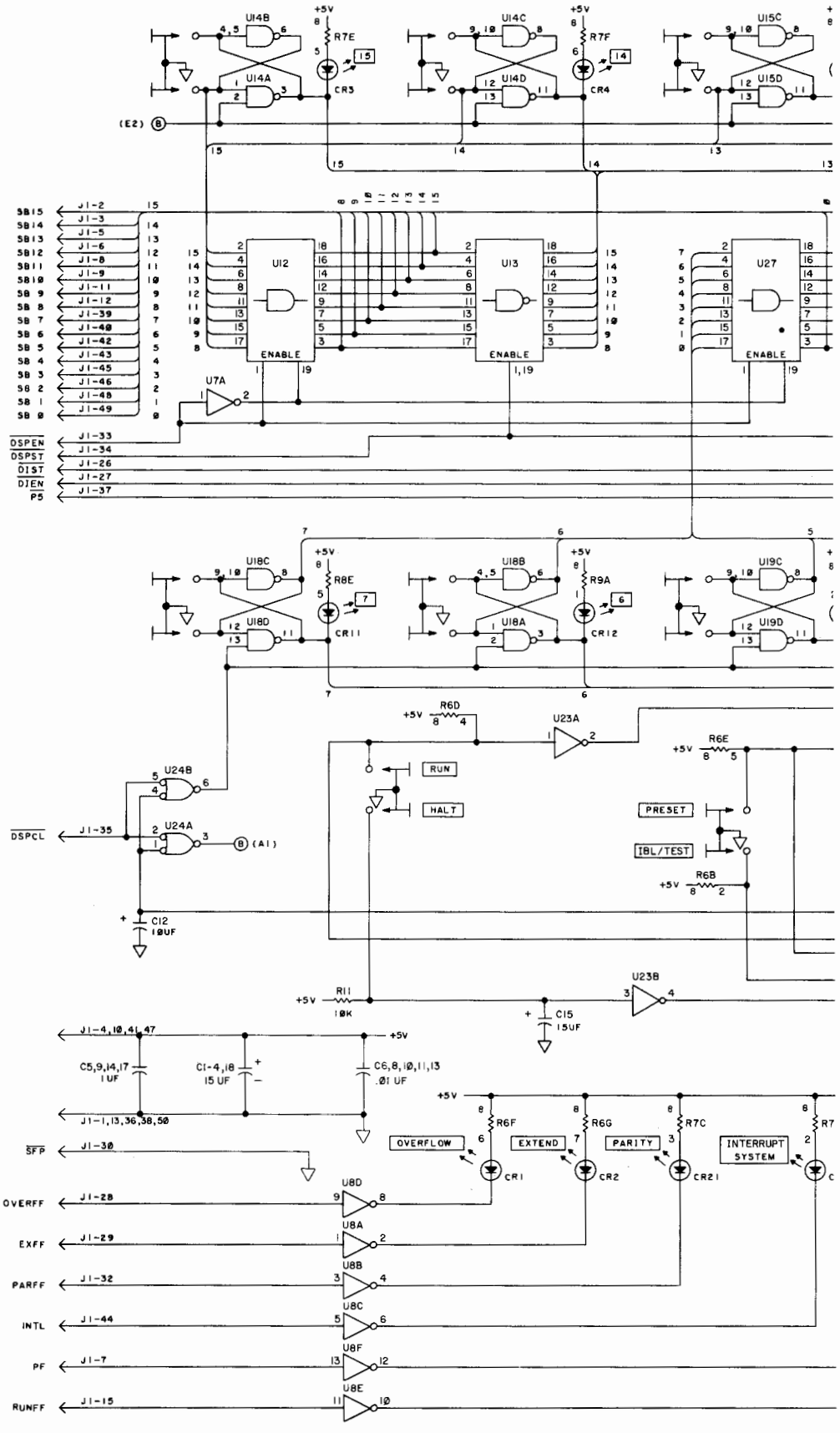
U10C
U10A
U10B
U10D


U14B
U14A
U14C
U14D
U15C
U15D
R7E
R7F
CR3
CR4
(E2) B
SB15
SB14
SB13
SB12
SB11
SB10
SB 9
SB 8
SB 7
SB 6
SB 5
SB 4
SB 3
SB 2
SB 1
SB 0
J1-2
J1-3
J1-5
J1-6
J1-8
J1-9
J1-11
J1-12
J1-39
J1-40
J1-42
J1-43
J1-45
J1-46
J1-48
J1-49
U12
U13
U27
ENABLE
U7A
DSPEN J1-33
DSPST J1-34
DIST J1-26
DIEN J1-27
P5 J1-37
U18C
U18D
U18B
U18A
U19C
U19D
R8E
R9A
CR11
CR12
R6D
U23A
R6E
U24B
U24A
DSPCL J1-35
(A1)
RUN
HALT
PRESET
IBL/TEST
R6B
C12
10UF
R11
10K
U23B
C15
15UF
J1-4,10,41,47
J1-1,13,36,38,50
C5,9,14,17
1 UF
C1-4,18
15 UF
C6,8,10,11,13
.01 UF
SFP J1-30
OVERFF J1-28
EXFF J1-29
PARFF J1-32
INTL J1-44
PF J1-7
RUNFF J1-15
U8D
U8A
U8B
U8C
U8F
U8E
R6F
R6G
R7C
OVERFLOW
EXTEND
PARITY
INTERRUPT SYSTEM
CR1
CR2
CR21

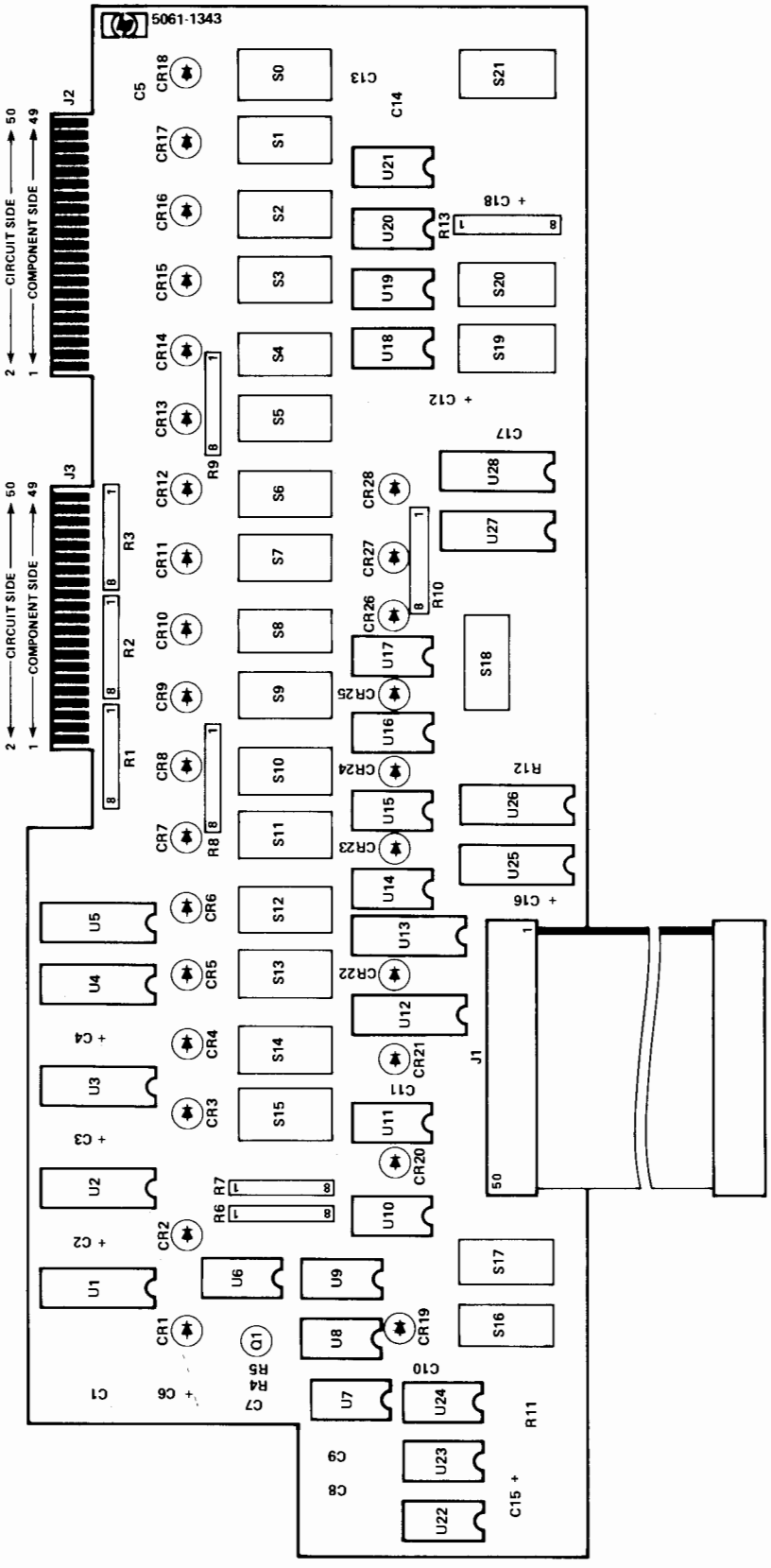

5061-1343
J2
J3
J1
CIRCUIT SIDE
COMPONENT SIDE
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
Q1
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
CR21
CR22
CR23
CR24
CR25
CR26
CR27
CR28
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21

Table B-2. 16K Memory Module Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 7 thru 12, 15	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 – 20%, 100 VDCW	56289	C023F101F103ZS22-CDH
C2 thru 4, 13	0160-3536	CAPACITOR, fxd, mica, 620 PF, 5% 100W VDC	72136	OBD
C5, 6, 22, 24, 27, 31	0180-1835	CAPACITOR, fxd, Ta, 68 μF, 20%, 15 VDC	56289	150D686X0015R2-DYS
C14, 16 thru 21, 23, 25, 26, 28 thru 30, 32	0160-0127	CAPACITOR, fxd, cer, 1 μF, 20%, 25W VDC	56289	5C13C-CML
CR1, 2	1901-0539	DIODE, Schottky, silicon, 20 V max vrm, 1A max	01-00	1901-0539
CR3	1901-1080	DIODE, pwr rect, silicon, 20 V max vrm, 1A max	04713	1N5817
CR4	1902-3092	DIODE, zener, 4.99 V, 0.4W max	15818	CD35620
R1	0698-3132	RESISTOR, fxd, flm, 261 ohms, 1%, 0.125W	19701	MF4C, T-O
R2 thru 7, 10, 11, 13, 15	0757-0442	RESISTOR, fxd, flm, 10K, 1%, 0.125W	19701	MF4C, T-O
R8, 9, 14, 17	0757-0280	RESISTOR, fxd, flm, 1K, 1%, 0.125W	07716	CEA, T-O
R12, 18, 19, 33	0698-3429	RESISTOR, fxd, flm, 19.6 ohm, 1%, 0.125W	19701	MF4C, T-O
R16, 20 thru 32, 34 thru 36	0757-0278	RESISTOR, fxd, flm, 1.78K, 1%, 0.125W	07716	CEA, T-O
R37	0698-0090	RESISTOR, fxd, flm, 464 ohm, 1%, 0.5W	19701	MF7C, T-O
U10, 16, 22, 24, 26	1820-1477	INTEGRATED CIRCUIT, hex tri-state buffer, TTL	18324	N8T95B
U11, 12	1820-1073	INTEGRATED CIRCUIT, quad excl "nor" gate, open collector, TTL	18324	N82S42A
U13	1820-1338	INTEGRATED CIRCUIT, BCD-to-octal decoder, TTL	18324	N82S50A
U14, 15	1820-1288	INTEGRATED CIRCUIT, dual clock driver, TTL	04713	SC25250LK
U17, 23, 25, 27	1820-1476	INTEGRATED CIRCUIT, hex tri-state converter, TTL	18324	N8T96B
U18, 19	1820-0681	INTEGRATED CIRCUIT, quad 2-input "nand" gate, TTL	01295	SN74S00N
U20, 21	1820-0685	INTEGRATED CIRCUIT, triple 3-input "nand" gate, TTL	01295	SN74S10N
U28 thru 95	5080-9781	MEMORY INTEGRATED CIRCUIT, 4K RAM	28480	5080-9781
XW1	1200-0483	SOCKET, elec, IC 14-con, dip sldr term	91506	514-AG11D

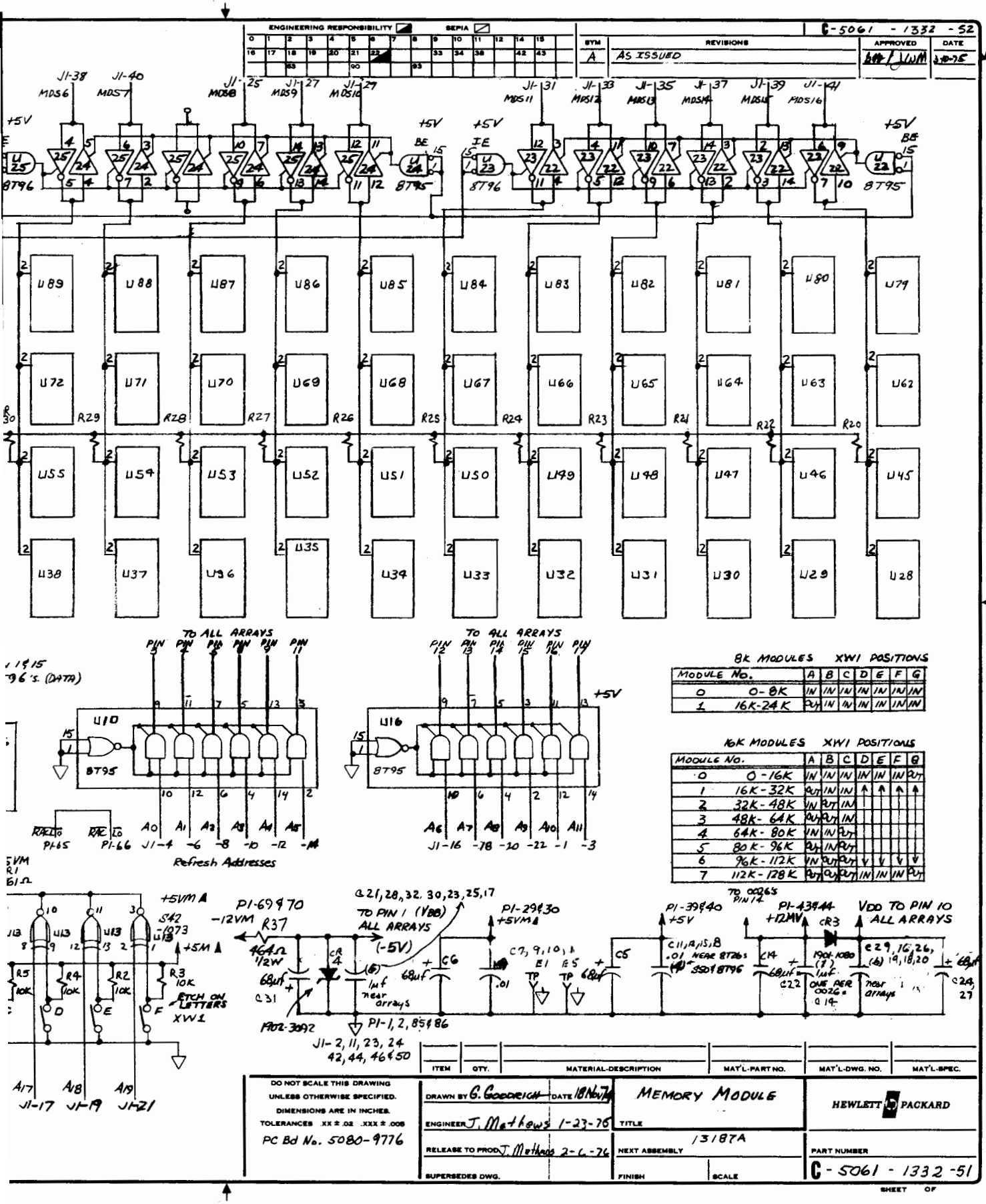
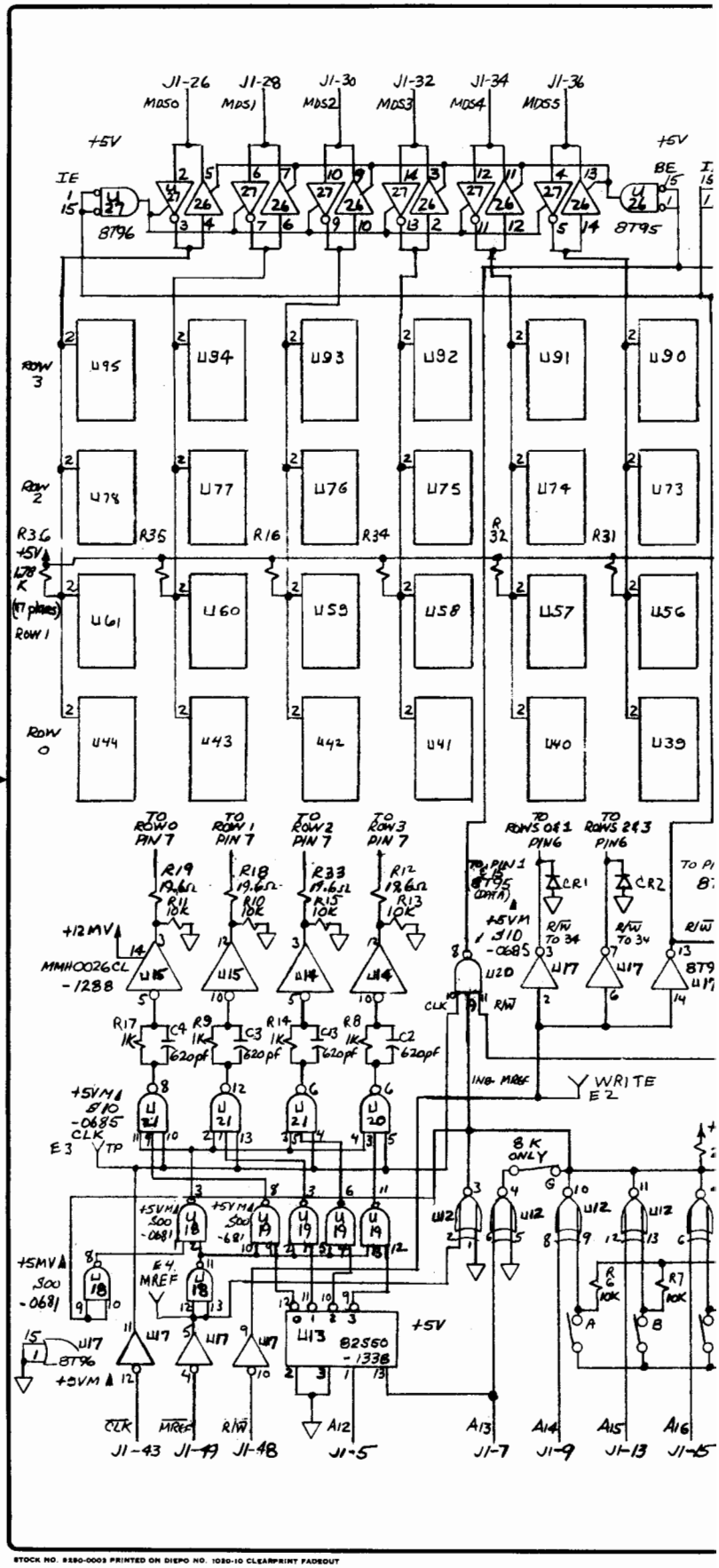


Figure B-2. 16K Memory Module, Parts Location and Schematic Diagrams



STOCK NO. 8280-0003 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

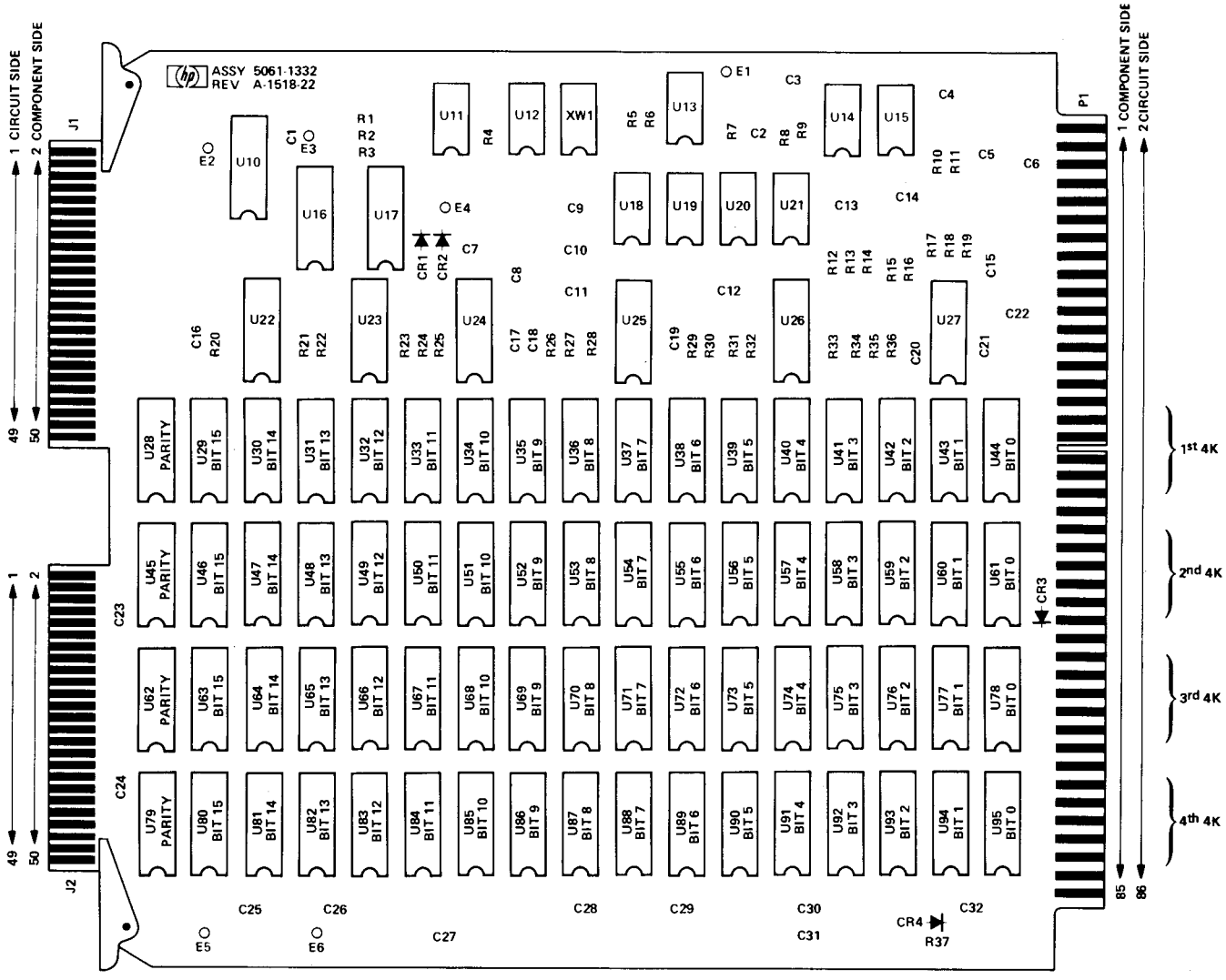


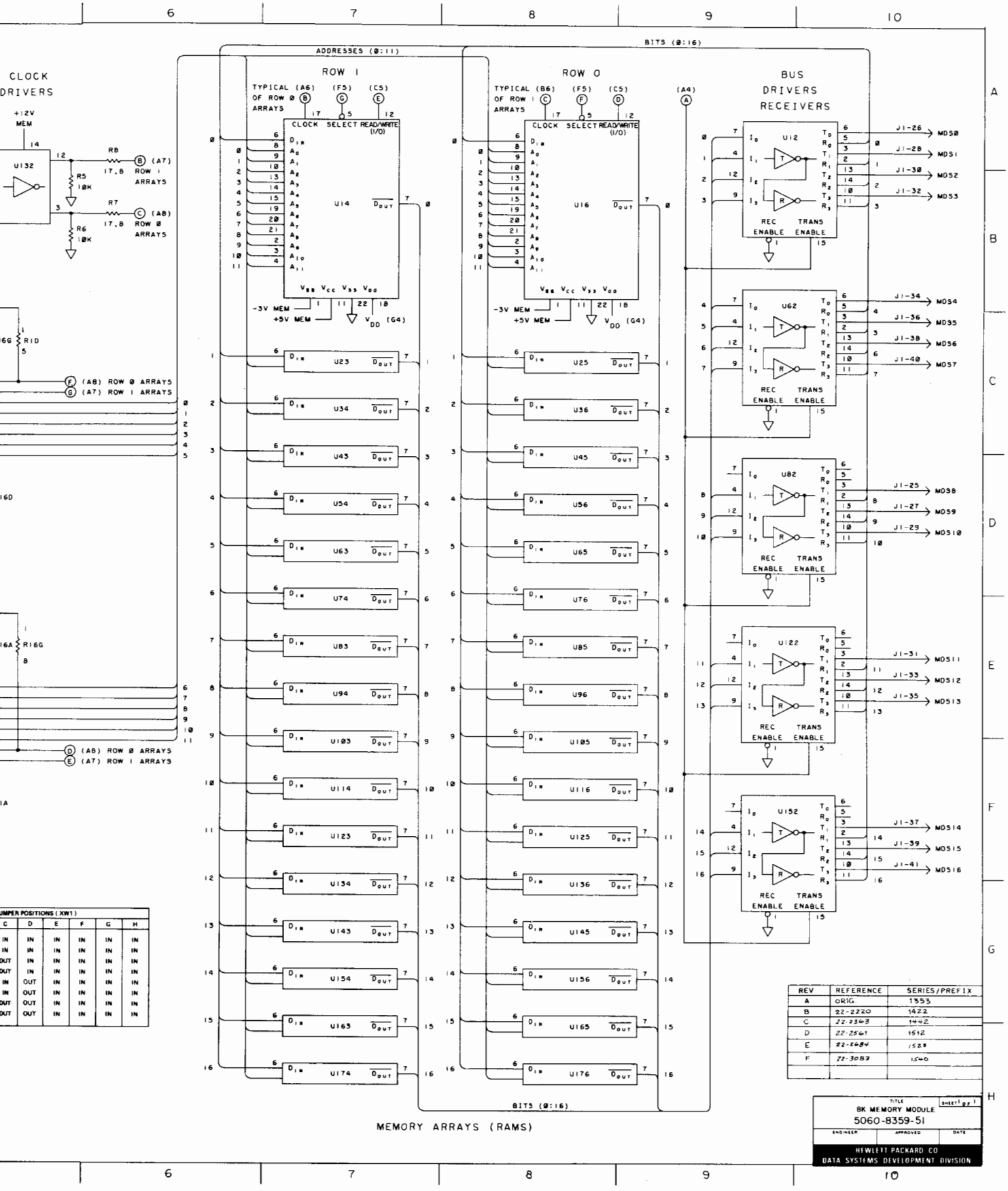
Table B-3. 8K Memory Module Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 2, 4, 9 thru 12, 14 thru 31, 33 thru 35, 38 thru 42	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 – 20%, 100 VDCW	56289	C023F101F103ZS22-CDH
C3, 5 thru 8, 13, 32, 43 thru 47, 52 thru 54	0160-0127	CAPACITOR, fxd, cer, 1.0 μF, 20%, 25 VDCW	56289	5C13C-CML
C36, 37	0160-3539	CAPACITOR, fxd, mica, 820 pF, 5%, 100 VDCW	72136	OBD
C48 thru 51	0180-1835	CAPACITOR, fxd, elec, Ta, 68 μF, 20%, 15 VDCW	56289	150D686X0015R2-DYS
††C55	0160-0127	CAPACITOR, fxd, cer, 1.0 μF, 20%, 25 VDCW	56289	5C13C-CML
††C56 thru 60	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 – 20%, 100 VDCW	56289	C023F101F103ZS22-CDH
*CR1	1902-3030	DIODE, zener, 3.01V, 2%, 0.4W	15818	CD35556
**CR1	1902-3092	DIODE, zener, 4.99V, 2%, 0.4W	15818	CD35620
††CR1	1902-3104	DIODE, zener, 5.62V, 5%, 0.4W	15818	CD35634
CR2	1901-1080	DIODE, pwr rect, silicon, 20V max, 1A max	04713	1N5817
††CR3	1901-0040	DIODE, switching, silicon, 30V, 50 mA	07263	FDG-1088
†R1, 16, 25	1810-0030	RESISTOR NETWORK, met flm, 7 × 1K, 5%	56289	200C1618-CRR
†R2, 3, 9 thru 13, 17	0683-1025	RESISTOR, fxd, comp, 1K, 5%, 0.25W	01121	CB1025
R4	0683-2715	RESISTOR, fxd, comp, 270 ohms, 5%, 0.25W	01121	CB2715
R5, 6, 24	0683-1035	RESISTOR, fxd, comp, 10K, 5%, 0.25W	01121	CB1035
R7, 8	0698-3389	RESISTOR, fxd, flm, 17.8 ohms, 1%, 0.5W	07716	CEC, T-0
††R10, 11, 17	0683-1025	RESISTOR, fxd, comp, 1K, 5%, 0.25W	01121	CB1025
R14	0683-5615	RESISTOR, fxd, comp, 560 ohms, 5%, 0.25W	01121	CB5615
R15	0698-3404	RESISTOR, fxd, flm, 383 ohms, 1%, 0.5W	19701	MF7C, T-0
††R25	1810-0030	RESISTOR NETWORK, met flm, 7 × 1K, 5%	56289	200C1618-CRR
U12, 68, 82, 122, 152	1820-1081	INTEGRATED CIRCUIT, quad line driver/receiver (tri-state), TTL	18324	CG528
*U14, 16, 23, 25, 34, 36, 43, 45, 54, 56, 63, 65, 74, 76, 83, 85, 94, 96, 103, 105, 114, 116, 123, 125, 134, 136, 143, 145, 154, 156, 163, 165, 174, 176	5080-9780	MEMORY INTEGRATED CIRCUIT, 4K RAM	28480	5080-9780
***U14, 16, 23, 25, 34, 36, 43, 45, 54, 56, 63, 65, 74, 76, 83, 85, 94, 96, 103, 105, 114, 116, 123, 125, 134, 136, 143, 145, 154, 156, 163, 165, 174, 176	5080-9785	MEMORY INTEGRATED CIRCUIT, 4K RAM	28480	5080-9785
†U31, 51, 121	1820-0759	INTEGRATED CIRCUIT, 8-bit receiver, non-inverting, tri-state, TTL	28480	1820-0759
††U31, 51, 121	1820-1477	INTEGRATED CIRCUIT, hex tri-state buffer, TTL	18324	N8T96B

Table B-3. 8K Memory Module Replaceable Parts (Continued)

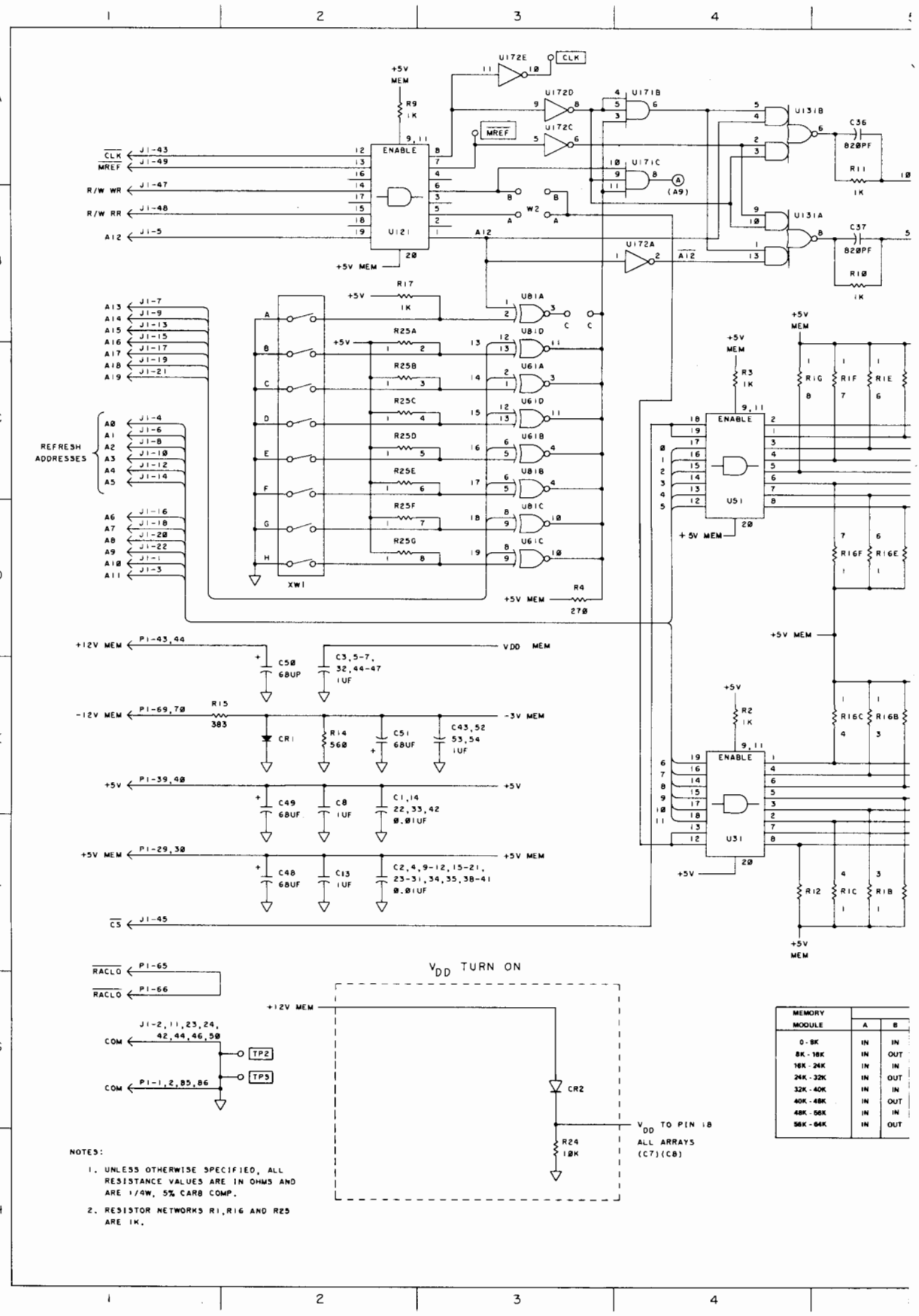
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
U61, 81	1820-1073	INTEGRATED CIRCUIT, quad excl "nor" gate, TTL	18324	N82S42A
U171	1820-0686	INTEGRATED CIRCUIT, triple 3-input "and" gate, Schottky, TTL	01295	SN74S11
U172	1820-0683	INTEGRATED CIRCUIT, high speed hex inverter, TTL	01295	SN74S04N
W2	8159-0005	JUMPER, wire, 22 AWG	00736	L-2007-1
XW1	1200-0482	SOCKET, elec, IC 16-con, dip sldr term	91506	516-AG10D

*PCA Series 1512 only.
**PCA Series 1523 only.
***PCA Series 1523 and above.
†PCA Series 1523 and lower.
††PCA Series 1540 and above.



REV	REFERENCE	SERIES/PREFIX
A	ORIG	1353
B	22-2220	1422
C	22-2363	1442
D	22-2561	1512
E	22-2684	1529
F	22-3083	1540

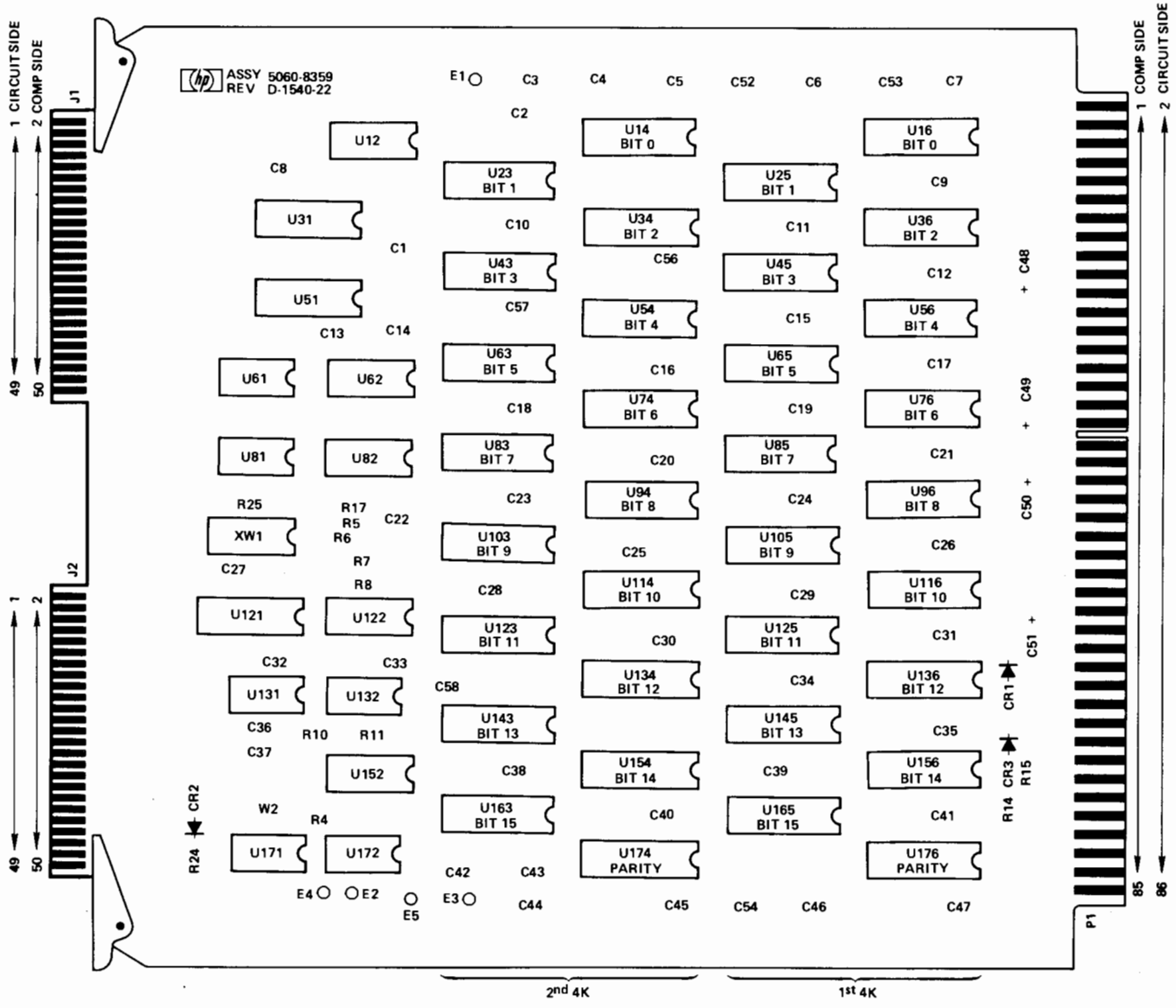
Figure B-3. 8K Memory Module, Parts Location and Schematic Diagrams

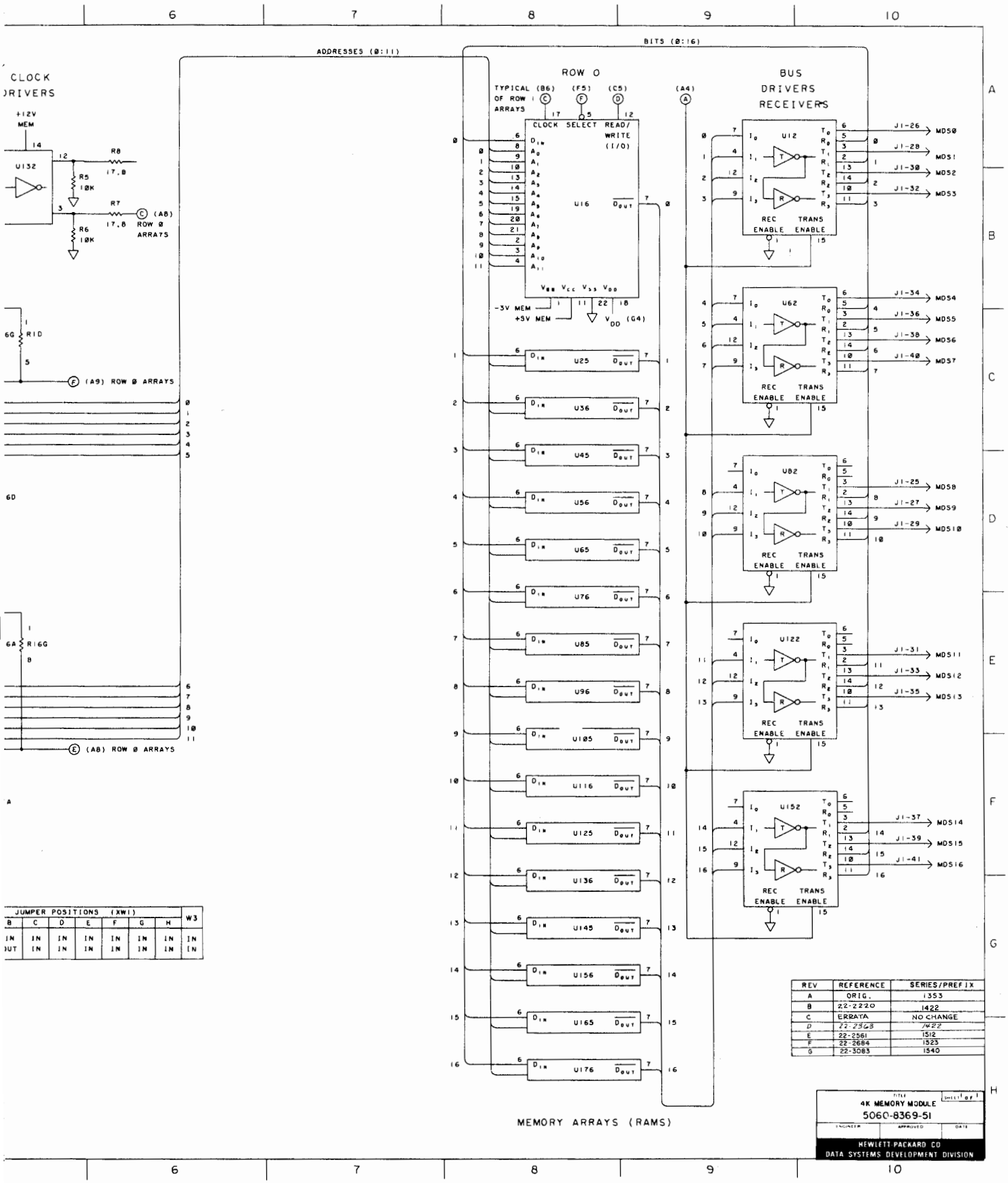


MEMORY MODULE	A	B
0 - 8K	IN	IN
8K - 16K	IN	OUT
16K - 24K	IN	IN
24K - 32K	IN	OUT
32K - 40K	IN	IN
40K - 48K	IN	OUT
48K - 56K	IN	IN
56K - 64K	IN	OUT

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS AND ARE 1/4W, 5% CARB COMP.
2. RESISTOR NETWORKS R1,R16 AND R25 ARE 1K.

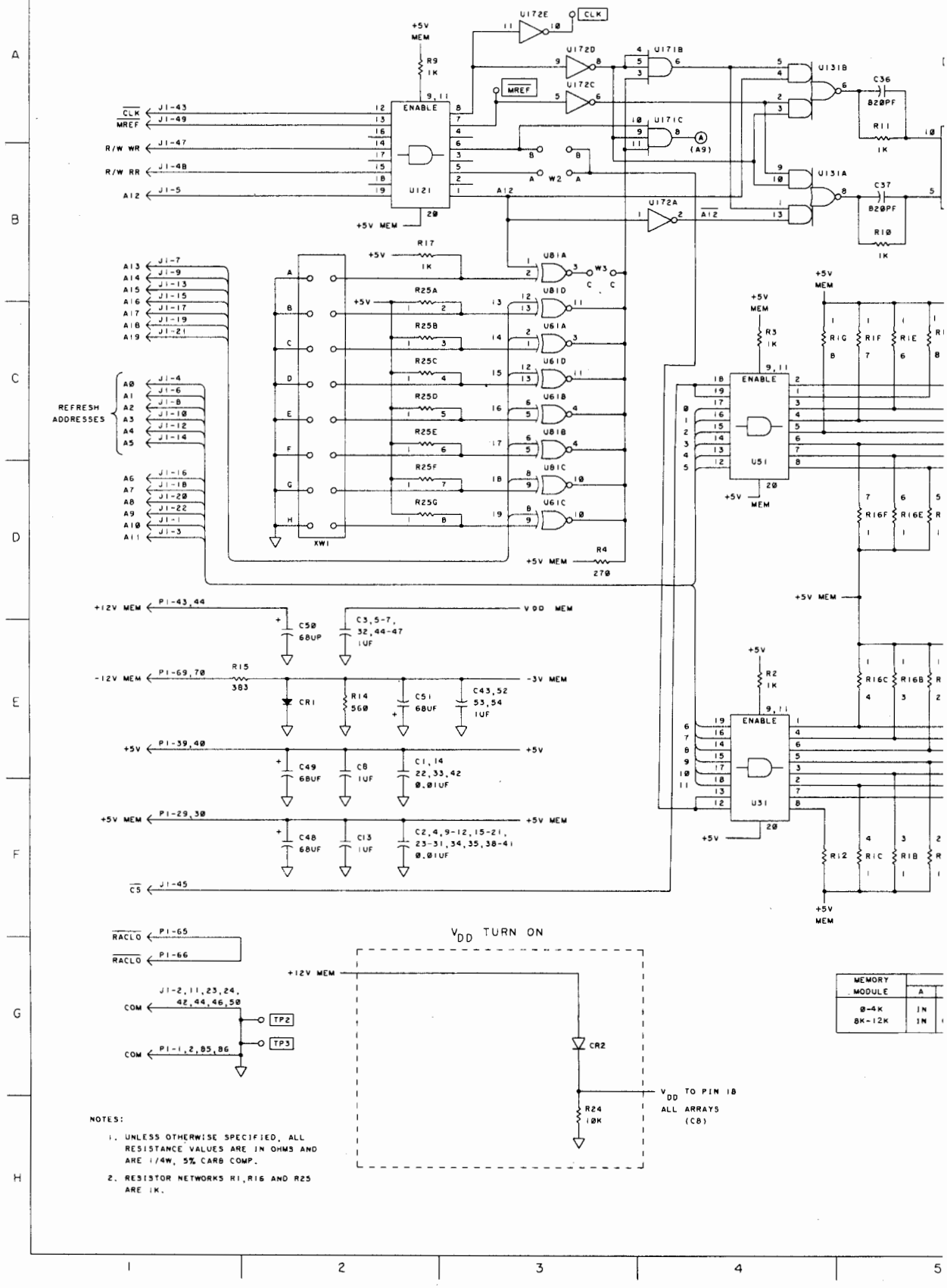




JUMPER POSITIONS (XW1)							W3
B	C	D	E	F	G	H	
IN	IN	IN	IN	IN	IN	IN	IN
OUT	IN	IN	IN	IN	IN	IN	IN

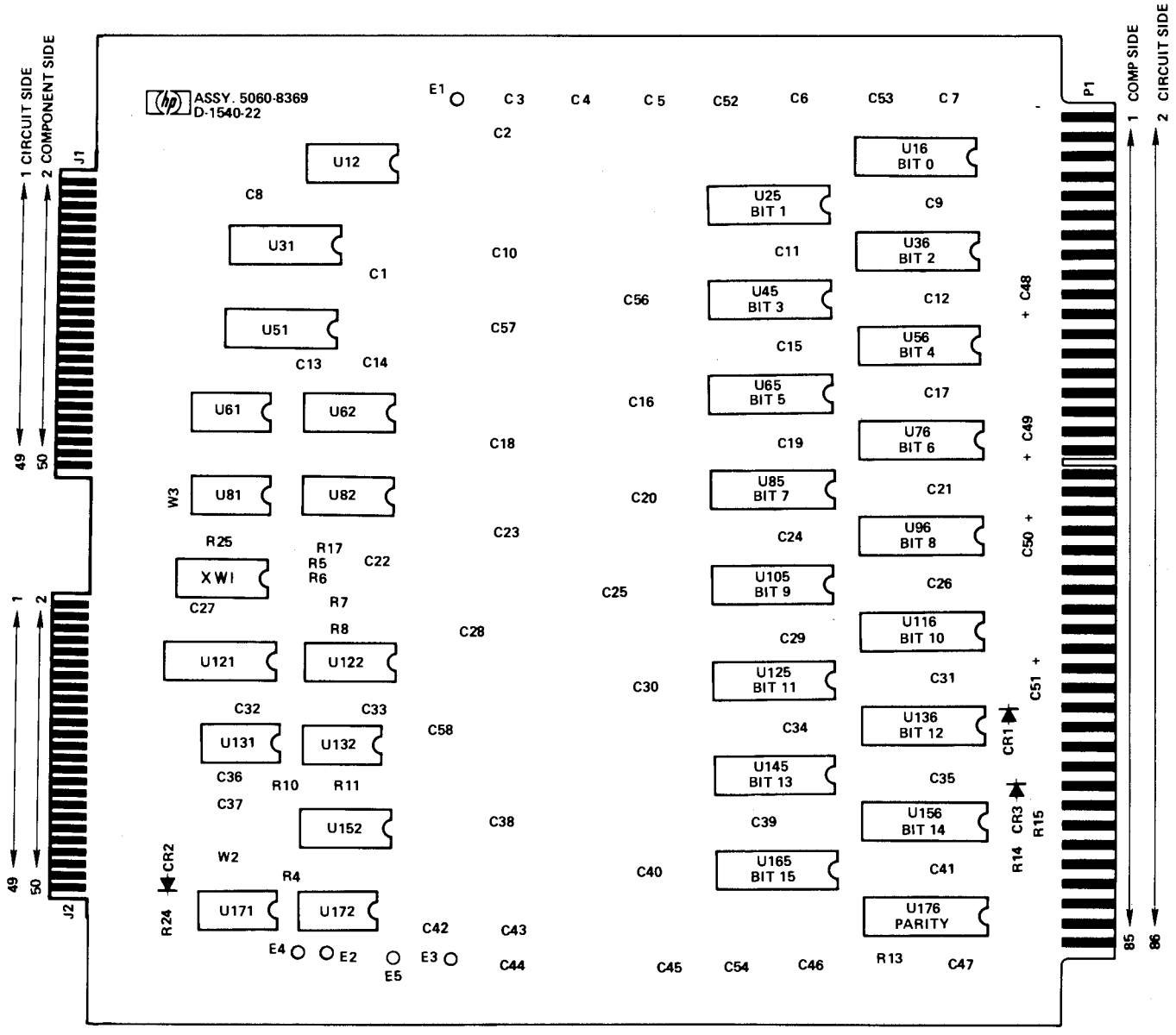
REV	REFERENCE	SERIES/PREFIX
A	ORIG.	1353
B	22-2220	1422
C	ERRATA	NO CHANGE
D	22-2368	1427
E	22-2561	1512
F	22-2684	1523
G	22-3083	1540

Figure B-4. 4K Memory Module, Parts Location and Schematic Diagrams



NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS AND ARE 1/4W, 5% CARB COMP.
2. RESISTOR NETWORKS R1,R16 AND R25 ARE 1K.


ASSY. 5060-8369
D-1540-22
1 CIRCUIT SIDE
2 COMPONENT SIDE
J1
J2
49
50
1
2
P1
1 COMP SIDE
2 CIRCUIT SIDE
85
86
E1
E2
E3
E4
E5
U12
U31
U51
U61
U62
U81
U82
XW1
U121
U122
U131
U132
U152
U171
U172
U16 BIT 0
U25 BIT 1
U36 BIT 2
U45 BIT 3
U56 BIT 4
U65 BIT 5
U76 BIT 6
U85 BIT 7
U96 BIT 8
U105 BIT 9
U116 BIT 10
U125 BIT 11
U136 BIT 12
U145 BIT 13
U156 BIT 14
U165 BIT 15
U176 PARITY
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
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C46
C47
C48
C49
C50
C51
C52
C53
C54
C56
C57
C58
R4
R5
R6
R7
R8
R10
R11
R13
R14
R15
R17
R24
R25
W2
W3
CR1
CR2
CR3