APPENDIX O

WRITEABLE CONTROL STORE

This appendix is identical with the stand-alone diagnostic manual, part no. 12908-90013.

Contents

FIGURE

TABLES

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Section I

INTRODUCTION

1-1. GENERAL

The Writable Control Store (WCS) Diagnostic verifies proper operation of the HP 12908B or HP 12978A Writable Control Store Interface Kit used on HP 2100 series computers that have microprogramming capability. This manual describes the diagnostic structure, the operating procedures required, and results obtained by loading the binary tape and running the program in conjunction with the HP 2000 Computer System Diagnostic Configurator. The general hardware/software environment and the system configuration procedures are described in the *HP 2000 Computer Systems Diagnostic Configuration Reference* manual, part no. 02100-90157.

1-2. HARDWARE REQUIREMENT

The required hardware consists of the following:

a. An HP 2100 Series Computer with a minimum 4K of memory.

b. A paper tape reader to load the program only; the teleprinter paper tape reader can be used.

c. An HP 12908B or HP 12978A Writable Control Store (WCS) Interface Kit. The maximum complement of three WCS modules may be installed and tested. The instructions in the *HP 12908B Writable Control Store Interface Kit Operating and Service* manual, (part no. 12908-90011) must be followed* regarding jumper installation and switch positioning prior to running the diagnostic. The Direct Memory Access (DMA) or Dual Channel Port Controller (DCPC) feature can be used but need not be present.

d. A system console teleprinter is optional but recommended for report and error message output.

1-3. SOFTWARE REQUIREMENT

The required software consists of the following binary object tapes:

a. HP 2000 Computer Systems Diagnostic Configurator (HP product no. 24296-60001) configured for at least a 4K memory.

b. This diagnostic, part number 12908-16001.

c. The Basic Binary Loader (BBL) or Initial Binary Loader (IBL) is used to load the above binary object tapes. The BBL is described in the HP Manual *Basic Binary Loader-Basic Binary Disc Loader-Basic Moving Head Disc Loader* (part no. 5951-1376). The IBL is described in the *HP 21MX Computer Series Reference Manual* (part no. 02108-90002).

*Referenced manual is for 2100A/S computers. For 21MX series computers see the *Microprogramming 21MX Computers Operating and Reference Manual* (part no. 02108-90008).

Section II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

This diagnostic program provides flexible testing of input, output, and control store functions of the Writable Control Store (WCS) Interface Kit. The structure of the program and methods of control, execution, and test selection are discussed in the following paragraphs. Diagnostic message analysis and diagnostic limitations are also discussed. The diagnostic program consists of a series of sections and steps. The sections are:

a. INIT — Initialization section.

b. START — Start section.

c. TST00 — DMA (DCPC) test section.

d. TST01 — WCS address test section.

e. TST02 — WCS data read/write test section.

f. TST03 — Microprogramming test section.

g. TSTMM — Multiple module testing section.

h. TSTSS — Special testing section.

i. TSTLL — Microcode loop test section.

The diagnostic program performs these routines (sections) as described below. Four routines (sections), TST00 through TST03, (tests zero through three) are performed in 22 steps.

SECTION	DESCRIPTION
INIT	The initialization section configures the I/O instructions to the lowest order WCS module select code specified in table 3-1 and saves the select code and control store module number for use during execution.
START	The start section sets variables, trap cell halts in select codes 2_8 through 77_8, and controls execution of the diagnostic according to program options selected in table 3-2.
TST00	Step 1 Checks to insure that the I/O Bus is clear (LIA 0). Step 2 Checks DMA (DCPC) flag circuitry by attempting a two-word transfer using DMA. *NOTE: Throughout this document where DMA is mentioned it should be interpreted to mean DMA or the DCPC.* Step 3 Checks DMA interrupt circuitry by attempting a two-word transfer using DMA with the interrupt system on. *NOTE: If DMA is not present, steps 2 and 3 are skipped.*

SECTION		DESCRIPTION
TST01	Step 4	Writes each location in a WCS module with its own address in ascending order (0_8 through 377_8). Reads each location back and verifies contents. Repeats the process 16_{10} times.
	Step 5	Repeats step 4 writing addresses into WCS in descending order.
	Step 6	Repeats step 4 writing addresses into WCS, alternating addresses in the following order: 0_8, 256_8, 1_8, 257_8, etc.
TST02	Step 7	Writes a data pattern of all "0's" on the entire WCS module. Reads each location back and verifies the contents. Repeats the process 96_{10} times.
	Step 10	Repeats steps 7 with a data pattern of all "1's."
	Step 11	Repeats step 7 with a data pattern of a "0" in a field of "1's" for the 24-bit microword. The "0" is rotated one position each time the process is repeated to check RAM integrated circuits (IC's) pack by pack.
	Step 12	Repeats step 7 with a data pattern of a "1" in a field of "0's." The "1's" is rotated one position each time the process is repeated.
	Step 13	Repeats step 7 with a data pattern of one microword all "0's" with remaining 255_{10} microwords all "1's." Repeats the process 256_{10} times incrementing the address of the all "0's" microword each time until the step is complete. This will ripple a "0" through a field of "1's" within each RAM IC pack.
	Step 14	Repeats step 13 with a data pattern of one all "1's" microword with remaining microwords all "0's."
	Step 15	Writes the data pattern "$101010101010101010101010_2$" at WCS module address 0_8. Complements the pattern and writes it at WCS module address 1_8 Continues writing the pattern (complemented), alternating throughout the entire WCS module. Reads each location back and verifies its contents. Repeats the process 256_{10} times, complementing the pattern at each location each time the process is repeated.
	Step 16	Repeats step 15 using DMA, if present.
TST03	Step 17	Calls a macroinstruction that will map into a microprogram that jumps to another location in the microcode within the current control store module. The microprogram then returns. (End-of-Phase microinstruction (EOP) in the HP 2100.)
	Step 20	Calls a macroinstruction that will map into a microprogram that sets the A-register equal to zero and leaves the B-register untouched.
	Step 21	Calls a macroinstruction that will map into a microprogram that leaves the A-register untouched and performs a logical "and" of the B-register and bits 0 through 9 of the Instructional Register (IR).
	Step 22	Calls the microprogram in step 21 with four different macroinstructions (a single macroinstruction in the 21MX).

NOTE: All of the above microcode resides in the current control store module under test. The microcode exercises all 24 lines to the ROM Instruction Register (RIR) from WCS. A- and B-registers are loaded with all "1's" prior to execution of any microprograms and tested afterwards for successful execution. In the HP 2100 Computer a standard jump table is also loaded into WCS for possible use in TSTMM.

SECTION	DESCRIPTION
TSTMM	If selected, this section will perform TST00 through TST03 sequentially on all WCS modules present, starting with the lowest order WCS module.
TSTSS	If selected, this section will write a specific pattern at a specific address and read it back. The section (routine) loops until the section is deselected.
TSTLL	If selected, this section calls a macroinstruction that places all "0's", all "1's" in the RIR and then returns. (EOP and Inclusive "or' (IOR) in the 2100. The section (routine) loops until the section is deselected.

2-2. TEST CONTROL AND EXECUTION

The diagnostic configurator is loaded and configured first, then this diagnostic is loaded and configured. The diagnostic execution is primarily controlled by the switch register as outlined in section III.

2-3. TEST SELECTION

Combinations of diagnostic sections for testing WCS modules can be selected as outlined in section III and IV of this manual.

2-4. MESSAGE REPORTING

Test sequence and test failure reporting to the operator is provided through a teleprinter (if available) and through the computer Memory Data Register (referred to as the MDR or T-register). Operator input is required via the switch register and the A- and B-registers for test options. If a teleprinter is present, messages to the operator are printed with an H prefix for operating messages and an E prefix for error messages. The meaning of all teleprinter messages and halts are listed in table 4-1. Refer to the table to analyze halt conditions and messages, then press RUN to resume program execution. Most error messages will contain control store module, test, and step numbers (see message H030).

2-5. DIAGNOSTIC LIMITATIONS

The microprogram to be executed in test section 3 (TST03) will have recovery capability in the event of power fail, bad WCS logic, etc. However, the microprogram cannot guarantee recovery back to program control in all cases. If the diagnostic is hung in the microcode, the user has no alternative except to turn power off and determine the source of malfunction.

This diagnostic can only check the module enable circuits that the current WCS card is configured for. To test all module enable circuits, the user must use WCS to replace all possible control store modules, rearranging jumper wires on TB1 or changing switch S1 each time and executing the diagnostic for each module.

All possible ROM addressing is not performed in this diagnostic. This is due to the mapping arrangement of the various computers. The macroinstructions used will not exercise all RAR lines in every case.

This diagnostic program will not execute if any WCS module replaces control store module 0 in the HP 2100 or control store modules $0, 1, 16_8$ or 17_8 in the HP 21MX. The microprogramming test section (TST03) will not execute properly if WCS is being used over a control module which also contains ROM's. This includes Floating Point Options, Fast Fortran or user installed microprograms. The diagnostic will run in other unused control store modules alongside modules containing ROM's. In the HP 2100,

however, any other microcode must preserve the HP Standard Jump Table or section TST03 will not execute properly. TST03 will not execute if the computer is a 21MX and WCS is being used in control store modules 16_8 and 17_8. Those modules are reserved for the Floating Point Option and the Extended Instruction Group.

The multiple module testing section (TSTMM) will not work with more than three WCS modules present.

Section III

OPERATING PROCEDURE

3-1. LOADING AND CONFIGURING

Using the Binary Loader, load the Diagnostic Configurator. Refer to the appropriate *Front Panel Procedures* manual of the computer being used to use the Binary Loader. The loader for the HP 2100 is described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader — Basic Moving Head Disc Loader* (part no. 5951-1376). Loading procedures for the HP 21MX are described in the *HP 21MX Computer Series Reference Manual* (part no. 02108-90002).

Perform the configuration procedure before loading the diagnostic. Procedures for inputting the system hardware configuration parameters are found in the Diagnostic Configurator manual under "Configuring." This diagnostic may then be loaded using the Binary Loader. Details on loading and configuring this diagnostic are contained in paragraph 3-3. Initial loading and configured loading are explained.

3-2. SWITCH REGISTER SELECTIONS

All switch register setting for configuring, selecting options, and running this diagnostic are outlined in tables 3-1 through 3-3. A- and B-register settings are shown in figure 3-1. The above listed tables and the figure are located in the operating instructions.

3-3. OPERATING INSTRUCTIONS

Load, configure and run this diagnostic as outlined below. See paragraph 3-1 for loading references.

a. If a configured diagnostic is available (HP 12908B or HP 12978A WCS and configured diagnostic configurator), go to step d.

b. Load and configure the diagnostic configurator. (See paragraph 3-1 above.)

c. Load the WCS diagnostic binary object tape.

d. Set starting address 000100_8 in the P-register. Set the select code of the lowest order WCS module and control store module number in the switch register as per table 3-1, press PRESET, (INTERNAL and EXTERNAL if present) and press RUN. The program halts with 102074 displayed.

e. Set the program options desired in the switch register (from table 3-2) and press RUN. The program commences execution in START and will operate according to the program options selected. Some of the major program options are summarized as follows:

    1) If program option bit 0 is set, program control passes to the multiple module testing section TSTMM after execution of one pass through sections TST00 through TST03 (or of the current pass).

        a) The program will halt with 102060 displayed. Enter the select code of the next higher order WCS module select code and control store module information in the A-register as per table 3-3. Enter the next higher order WCS module select code and control store module information in the B-register, press RUN. If WCS is not present, clear the B-register, then press RUN.

b) The program halts with 102074 displayed. Set program options from table 3-2 in the switch register, then press RUN. The diagnostic program performs testing on all WCS modules present. Testing starts with the lowest order WCS module and moves sequentially through to the highest module. One pass now includes all modules present. Multiple module testing continues until program option bit 0 is cleared then control returns to START, testing only the lowest order WCS module in START.

NOTE: Section TSTMM will perform testing on up to a maximum of three WCS modules.

2) If program option bit 1 is set, program control passes to the special testing section TSTSS. The program halts with 102063 displayed. Enter the 8-bit WCS module address to be tested (left justified) in the A-register and a 24-bit microword in the right 8 bits of the A-register and the entire B-register. (See figure 3-1.) Press RUN. The program loops, writing and reading the test pattern at the WCS module address specified until program option bit 1 is cleared. Program control then passes back to START.

NOTE: All of the switch register bits, except bit 1, are ignored during execution of this section.

3) If program option bit 9 is set, the program halts with 102075 displayed. Enter the tests desired in the A-register. That is, set bit 0 to run section TST00, bit 1 to run section TST01, etc. A-register bits 4 through 15 are ignored.

4) With the switch register clear, the program will halt (102077) after each pass. The A-register will contain the current pass count. Set program option bit 12 to loop on the entire diagnostic program.

5) If program option bit 6 is set, program control passes to the microcode loop section TSTLL. The program loops on a macroinstruction that calls microprograms which jump to a location in the microcode containing all "0's" then all "1's," and returns (or EOP in the HP 2100).

NOTE: If a jump microinstruction is not working correctly, the microprogram will have unpredictable results.

NOTE: The diagnostic configurator dump routine can be used after operating instruction steps b or c to dump configured binary tapes at either point.

Table 3-1. Program Configuration Switch Register Settings

BITS	FUNCTION
0-5	Enter select code of lowest order WCS module in the mainframe. This must be an octal number greater than 7 and less than or equal to 25.
6-11	Reserved.
12-15	Enter the number of the control store module being replaced by the WCS module; i.e. $0100XX_8$ is module 1, $0500XX_8$ is module 5, etc. (XX_8 equals the select code in bits 0 through 5). Not valid for module 0 in 2100 or 0, 1, 2, 16_8 or 17_8 in 21MX.

Table 3-2. Program Option Switch Register Settings

BIT	MEANING IF SET
0	Execute section TSTMM, after one pass or upon completion of the current pass.
1	Execute section TSTSS.
2	Halt (102050) after each step; the A-register will contain the step number (in octal) where the halt occurs.
3	Repeat the last step (loop on step).
4	Shorten reporting of error message E0XX (XX equals step number 7 thru 16). Causes reporting of E0XX to occur four times and then stop until the next step where E0XX is detected.
5	Shorten reporting of errors by skipping to the next step immediately. (Faster execution than using bit 4.)
6	Execute section TSTLL.
7	Reserved.
8	Suppress tests requiring operator intervention. (Not applicable to this diagnostic. Setting or clearing this bit has no effect on this diagnostic.)
9	Abort current pass and halt (102075). User may specify a new group of tests in the A- and/or B-register, and then press RUN.
10	Suppress non error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS "XXXXXX" will be output before looping unless bit 10 is set or if a teleprinter is not present.
13	Repeat the last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number (in octal) where the halt occurs.

3-4. OPERATOR DESIGN

To reconfigure the diagnostic after execution, halt the computer and commence with step d of the operating instructions. This should only be necessary if the select code of the lowest order WCS module changes from its original configuration.

To restart the program after execution, set the P-register to 2000_8 and commence with step e of the operating instructions.

Table 3-3. Multiple Module Test (TSTMM) Switch Register Settings

BITS	FUNCTION
	A-REGISTER
0-5	Enter the select code of the next higher order WCS module present. This must be an octal number greater than 7 and less than or equal to 25.
6-11	Reserved.
12-15	Enter the number of the control store module being replaced by the WCS module; i.e. $0100XX_8$ is module 1, 0500XX is module 5, etc. (XX equals the select code in bits 0 thru 5.)
	B-REGISTER
0-5	Enter the select code of the highest order WCS module to be tested. This must be an octal number greater than 7 and less than or equal to 25.
6-11	Reserved.
12-15	Enter the number of the control store module being replaced by the WCS module; i.e. $0100XX_8$ is module 1, 0500XX is module 5, etc. (XX equals the select code in bits 0 thru 5.)
NOTE: If only two WCS modules are present, clear the B-register and press RUN.	

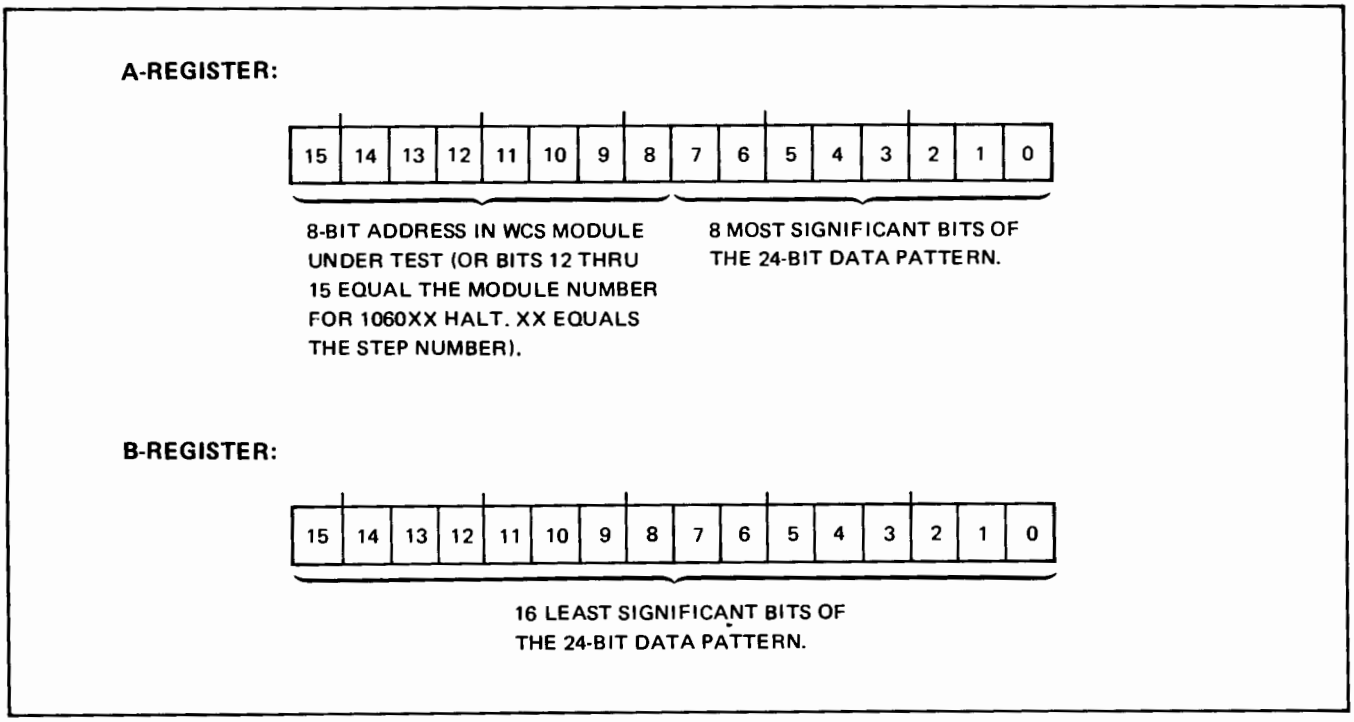

Figure 3-1. A- and B-Register Settings

Section IV

DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

If a trap cell halt occurs, the computer displays 106077 in the display (T-) register and the M-register contains the location of the halt. The cause of the trap cell halt should be determined by the user; after the error is corrected, the diagnostic should be reloaded.

If an error is detected, the program causes one or more messages to be output on the teleprinter (if present) and if appropriate, halts with a halt code displayed in the display (T-) register. All error messages are accompanied by message H030, containing the module, step number and test section where the error occurred. Error messages "E0XX BAD MAC" and "NO MAC", (see table 4-1) where XX means step number 17 through 22, are also accompanied by message H031, giving the A- and B-registers and the macroinstruction used when the error occurred.

Multiple module testing is accomplished through section TSTMM by setting program option bit 0 (see table 3-2). After a series of halts, entering information via the A- and B-registers, all test sections are executed. Testing is performed on the lowest order WCS module, then the next order and so on until all WCS modules present are tested. Testing continues on all modules until program option bit 0 is cleared. The pass count, reported in the pass message, is the number of times testing on all WCS modules has been performed. An asterisk is added to the pass message to indicate this. When this section is deselected, the pass count represents testing on the lowest order module only.

A special looping test is provided by section TSTSS. TSTSS is entered by setting program option bit 1. (See table 3-2.) The program halts with 102063 displayed. The user enters a module address and data pattern in the A- and B-registers, (see figure 3-1) then presses RUN. The program loops on reading and writing the pattern at the address specified until program option bit 1 is cleared.

The diagnostic provides section TSTLL for looping in the microcode. Once it has been determined that there are problems in the microprograms, the user may want to use this section to examine individual RIR or ROM Address Register (RAR) lines. The section loops on a all "0's" microinstruction then on all "1's" and returns. The section is entered by setting program option bit 6 during execution and exited when bit 6 is cleared.

4-2. ERROR INFORMATION MESSAGES/HALT CODES

Table 4-1 contains the information to interpret diagnostic messages and halt codes.

Table 4-1. Diagnostic Messages and Halts

HALT CODE	SECTION	MESSAGE	MEANING
102073	INIT	None	I/O select code entered at configuration invalid. Must be greater than 7_8. Renter a valid select code and press RUN.
102074	INIT	None	Select code entered during configuration valid. Enter program option bits in switch register and press RUN.
102075	START	None	Test selection request resulting from switch register bit 9 being set. Enter the desired group of tests (in the A-/B-register) to be executed and press RUN.
102076	START	None	End of test halt resulting from switch register bit 15 being set (A-register equals the test number). To continue, press RUN.
102077	START	PASS XXXXXX	Diagnostic run complete. A-register contains the pass number in octal. To continue, press RUN. When the program is in section TSTMM, the pass count message gas as asterisk placed at the end of the message to indicate multiple module testing.
106077	None	None	Halt stored in location 2 thru 77_8 to trap an interrupt which may occur unexpectedly because of hardware malfunctions. The M-register contains the I/O slot number which interrupted. Diagnostic may be partially destroyed if a halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.
None	START	12908 WCS DIAGNOSTIC	Introductory message at start of diagnostic.
102001	TST00	E001 IO BUS NOT CLEAR	An LIA 0 did not return all "0's" from the I/O bus.
102002	TST00	E002 NO DMA FLAG	Faulty circuitry did not set the flag at the end of block transfer. Run DMA (DCPC) Diagnostic to determine exact nature of malfunction.
102003	TST00	E003 NO DMA INT	DMA interrupt circuits did not interrupt at end of block transfer. Run DMA Diagnostic to determine exact nature of malfunction.
1020XX	TST01, TST02 or TST03		XX equals the step number.

Table 4-1. Diagnostic Messages and Halts (Continued)

HALT CODE	SECTION	MESSAGE	MEANING
NOTE: The following is for step numbers 7 thru 16 –			
(Note: The following are message print-outs.) E0XX BAD COMPARISON MODULE DATA DATA ADDRESS READ WRITTEN WWW YYY.YYYYYY ZZZ.ZZZZZZ etc.			The data pattern from WCS did not compare with the pattern that was written at WCS module address WWW_8. $ZZZ.ZZZZZZ_8$ is the pattern written. The A-register content equals the 8-bit address and the 8 bits of the data pattern read. The B-register contains the 16 bits of the data pattern (see format shown in figure 3-1). $YYY.YYYYYY_8$ is the data read from WCS. For systems without console devices see halt code 1060XX below.
NOTE: Message is reported in its entirety only once for each time a WCS module content is compared. If there are many errors, subsequent errors report the address and data only.			
NOTE: The following is for step numbers 17 thru 22 –			
1020XX	TST03	E0XX NO MAC	The macroinstruction used to call the test microprogram did not transfer control to the microprogram or, an error occurred in execution of the microprogram. XX equals step number 17 thru 22). H031 is also reported. A- and B-registers content equal the A- and B-registers after execution of the macroinstruction.
1020XX	TST03	E0XX BAD MAC	An error occurred during the execution of the microprogram. XX equals step number (17 thru 22). H031 is also reported. A- and B-registers content equal the A- and B-registers after execution of the macroinstruction.
1020XX	TST03	H031 MAC = 105XX A = YYYYYY SHOULD BE = ZZZZZZ B = WWWWWW SHOULD BE = VVVVVV	XXX = Last 9 digits of failing macroinstruction. YYYYYY = Actual A reg. ZZZZZZ = Expected A reg. WWWWWW = Actual B reg. VVVVVV = Expected B reg.
102016	TST02	E016 DMA NOT COMP	Loading WCS via DMA in step 16 was never performed because DMA did not respond with a flag at the end of transfer. A- and B-registers equal zero.
1060XX	TST01 TST02 or TST03	None	Used for systems without slow output devices after a halt 1020XX. Pressing RUN results in this halt instead of resuming program execution. XX equals the step number. *NOTE: The following is for step numbers 7 thru 16.*

Table 4-1. Diagnostic Messages and Halts (Continued)

HALT CODE	SECTION	MESSAGE	MEANING
			The data pattern read from WCS did not compare with the pattern that was written. A-register contains the module number and the 8 bits of the pattern written on WCS. The B-register contains the 16 bits of the pattern written (see figure 3-1). *NOTE: The following is for step numbers 17 thru 22 –* A macroinstruction did not execute properly. The A-register contains the module number in bits 12 through 15 and the B-register contains the macroinstruction that failed.
102050	TST00 TST01 TST02 TST03	None	Halt after completion of a step. The A-register contains the step number.
102060	TSTMM	None	Set the information listed in table 3-3 in the A- and B-registers then press RUN.
102063	TSTSS	None	Set the WCS module address plus the data pattern in the A- and B-registers (see figure 3-1) then, press RUN.
None	Any	H030 MOD XXXX, TSTYY, STEP ZZ	Error occurred in control store module $XXXX_8$ (0_8 thru 17_8) program routine TSTYY, and step number ZZ (0_8 thru 22_8).
102051	Configuration	None	I/O select code entered at configuration was greater than 25_8. Re-enter the proper select code and press RUN.
102052	Configuration	None	Control store module number entered in the switch register was invalid. Cannot use module 0, 1, 2, 16_8 or 17_8 in the HP 21MX or module 0 in the HP 2100.
102053	Configuration	None	Control store module number entered in the switch register was greater than 3_8 and the computer is a HP 2100. Re-enter correct module number then, press RUN.
102054	TSTMM	None	Module numbers entered are out of order, i.e., the module numbers do not run from lower to higher order. Re-enter module numbers in the correct order.