HP 2100 SHIFT-ROTATE INSTRUCTION TEST

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This diagnostic program checks all the code combinations of the Shift-Rotate Instruction Group as defined in the Consolidated Coding Table. The secondary objective is checking instructions and conditions affecting the overflow register. Also included as a special case is a check of eight individual rotate instruction codes involving the E-register. These instructions are tested individually and not as part of any combination. The D/E (Disable/Enable) fields of these instructions are set to zero. (See Figure SFT-4, Consolidated Coding Table.)

HARDWARE CONFIGURATION

The program runs on any core size HP 2100 computer and does not use a teleprinter.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

This program should be run only after the Memory-Reference Instruction Test and the Alter-Skip Instruction Test as instructions in these groups are used to test the shift-rotate group. The program uses no shift-rotate instructions except for those being tested.

To run the program the user loads the program with the Basic Binary Loader, sets the Starting Address 100_8 and presses RUN. The program now tests all shift-rotate instructions, checking each valid instruction 14 times. First, seven different data patterns are checked in either the A- or B-register depending on the instruction, with the E-register clear, then the seven different data patterns are checked in either the A- or B-register depending on the instruction, with the E-register set.

After execution of each shift rotate instruction, the program checks the contents of the A- or B-register and the E-register and checks that the instruction did or did not skip as expected.

A detected failure results in a halt and an information display. MEMORY DATA contains the coded halt $10200x_8$. x is an octal digit with bit meanings as follows:

bit 0 = 1,A- or B-register error.

bit 1 = 1,E-register error.

bit 2 = 1,Instruction skipped or did not skip as expected.

The information should also be displayed after the error halt:

A-register--Actual A- or B-register result.

B-register--Expected A- or B-register result.

E-register--Actual E-register result.

After RUN is pressed, another halt occurs and this information should be displayed:

MEMORY DATA--Second display halt (102000_8) identification.

A-register--Octal code of failing shift-rotate instruction;
bit 11 of the instruction identifies the register
0=A-register, 1=B-register.

B-register--Original data pattern in the A- or B-register.

E-register--Original contents of the E-register.

Following the second display halt, the program continues if switch register bit 0 is clear. If switch register bit 0 is set, the original values are restored in the E- and A- or B-registers, and another halt (102076_8) occurs. The next instruction executed is the failing instruction. The result can be observed by single stepping.

The program now executes overflow register tests, a string of individual tests. Errors here result in a unique coded error halt. (See Table SFT-2). No provisions are available for repeating overflow register tests.

After all instructions have been tested, the program normally loops continuously until an error is detected. If switch register bit 15 is set, the computer halts with 102077_8 displayed in MEMORY DATA and a 32 bit pass count contained in the A- and B-registers, with the most significant bits in the B-register.

Unexpected Changes In The A- Or B-Registers

If a change occurs in the B-register after executing a skip-rotate instruction involving the A-register or vice versa, the computer halts with 103000_8 displayed in MEMORY DATA if the A-register changed unexpectedly, or with 103001_8 displayed in MEMORY DATA if the B-register changed unexpectedly. The unexpected change is left in the register, and the other register contains the octal code of the shift-rotate instruction. Normally when the operator presses RUN, the program bypasses the other results usually checked. If switch register bit 0 is set, the computer halts with 102076_8 displayed in MEMORY DATA. The failing instruction is the next instruction executed. The results can be observed by single stepping.

A fixed non-symmetrical data pattern of 043210_8 is placed in the register (A- or B-) not expected to change before each skip-rotate instruction is executed.

OPERATING INSTRUCTIONS

a. Load the HP 2100 Shift-Rotate Instruction Test with the Basic Binary Loader.

b. Set Starting Address 100_8.

c. Press RUN.
   The program executes according to the switch register options selected.

Table 1
Switch Register Options

Bit if Set	Meaning
0	Repeat a failing shift-rotate but halt 102076_8 before its execution. (Does not apply to the overflow register tests.)
15	Halt 102077_8 at the end of pass (diagnostic cycle). A pass count is contained in the B- and A-registers (most significant bits in B-register).

Table SFT-2

Summary of Program Halts

MEMORY DATA	Comments
10200X	Shift Rotate Instruction error halt.
102000	Display halt following error halt.
102076	Halt before repeating failing Shift-Rotate instruction.
102077	End of pass halt (A- and B-registers contain the number of passes completed after the halt).
102040	CLO-SOC combination failed.
102041	CLO-SOS combination failed.
102042	STO-SOS combination failed.
102043	STO-SOC combination failed.
102044	STO-SOS,C combination failed.
102045	SOS,C did not clear OV.
102050	A was 077777 and INA did not set OV.
102051	A was 177777 and INA set OV.
102052	Sum of 077777 & 077777 in A did not set OV.
102053	Sum of 100000 & 100000 in A did not set OV.
102054	Sum of 077777 & 100000 in A set OV.
102055	Sum of 177777 & 177777 in A set OV.
102056	Sum of 000000 & 000000 in A set OV.
102060	B was 077777 and INB did not set OV.
102061	B was 177777 and INB set OV.
102062	Sum of 077777 & 077777 in B did not set OV.
102063	Sum of 100000 & 100000 in B did not set OV.
102064	Sum of 077777 & 100000 in B set OV.
102065	Sum of 177777 & 177777 in B set OV.
102066	Sum of 000000 & 000000 in B set OV.
103000	Unexpected change in A-register.
103001	Unexpected change in B-register.

Figure SFT-1
Consolidated Coding Table

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMORY REFERENCE INSTRUCTIONS															
D/I	AND		001	0	Z/C	← Memory Address →									
D/I	XOR		010	0	Z/C										
D/I	IOR		011	0	Z/C										
D/I	JSB		001	1	Z/C										
D/I	JMP		010	1	Z/C										
D/I	ISZ		011	1	Z/C										
D/I	AD*		100	A/B	Z/C										
D/I	CP*		101	A/B	Z/C										
D/I	LD*		110	A/B	Z/C										
D/I	ST*		111	A/B	Z/C										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHIFT-ROTATE GROUP INSTRUCTIONS															
0	SRG		000	A/B	0	D/E	*LS		000	†CLE	D/E	‡SL*	*LS		000
				A/B	0	D/E	*RS		001		D/E		*RS		001
				A/B	0	D/E	R*L		010		D/E		R*L		010
				A/B	0	D/E	R*R		011		D/E		R*R		011
				A/B	0	D/E	*LR		100		D/E		*LR		100
				A/B	0	D/E	ER*		101		D/E		ER*		101
				A/B	0	D/E	EL*		110		D/E		EL*		110
				A/B	0	D/E	*LF		111		D/E		*LF		111
				NOP	000				000		000				000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALTER-SKIP GROUP INSTRUCTIONS															
0	ASG		000	A/B	1	CL*	01	CLE	01	SEZ	SS*	SL*	IN*	SZ*	RSS
				A/B	1	CM*	10	CME	10						
				A/B	1	CC*	11	CCE	11						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC AND INPUT/OUTPUT INSTRUCTIONS															
1	MAC		000	A/B	0										
1	IOG		000	A/B	1	H/C	HLT		000	← Select Code →					
					1	0	STF		001						
					1	1	CLF		001						
					1	0	SFC		010						
					1	0	SFS		011						
				A/B	1	H/C	MI*		100						
				A/B	1	H/C	LI*		101						
				A/B	1	H/C	OT*		110						
				0	1	H/C	STC		111						
				1	1	H/C	CLC		111						
					1	0	STO		001		000			001	
					1	1	CLO		001		000			001	
					1	H/C	SOC		010		000			001	
					1	H/C	SOS		011		000			001	

Notes: 1) * = A or B. Use with bit 11 as Ø (A-Register) or 1 (B-Register).

2) D/I, A/B, Z/C, D/E, H/C coded: 0/1.

3) †CLE: Only this bit is required.

4) ‡SL*: Only this bit and bit 11 (A/B as applicable) are required.