HP 2100 MEMORY PARITY CHECK TEST

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HP 2100 MEMORY PARITY CHECK TEST

This diagnostic confirms proper operation of the Memory Parity Check circuitry for an HP 2100 computer. If an error exists, the program identifies the faulty function. Each error found should be corrected and retested before the next function is tested.

HARDWARE CONFIGURATION

This Memory Parity Check diagnostic requires any core size HP 2100 computer.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

The diagnostic is loaded and configured in two phases:

a. Program configuration is done by switch register settings in Table MP-1.

b. Options to be used for a normal run of the diagnostic are selected by setting the switch register as listed in Table MP-2, then pressing RUN. These settings become an internal switch register. If any option is changed during the run, the internal switch register may be overridden by setting switch register bit 0 or other appropriate bit(s) as listed in Table MP-2.

After the configuration procedures are complete, the SIO System Dump program may be used to make a permanent copy of the configured diagnostic.

If an error is detected, the program halts with a value displayed in MEMORY DATA. (See Table MP-3.) The cause of trap cell halt $1060xx_8$, located in low memory 2_8 -77_8, should be determined before the diagnostic is restarted.

PROGRAM ORGANIZATION

The diagnostic consists of the series of routines described below:

CONF — CONF configures the diagnostic for the proper core memory size and select code (I/O channel) and sets the internal switch register for the options selected at configuration time.

START — START sets trap cell halts in locations 2_8 -77_8. Before INIT starts, the program halts with 102002_8 displayed to allow the user to connect terminal E1 to E2 and E3 to E4 on the Memory Data Control Board.

INIT — INIT loads even parity data into special locations. Because Memory Parity Check requires odd parity data, the incorrect even parity data is used by the following test routines to check the Memory Parity Check circuitry.

TESTA — TESTA confirms that bit 15 of the A-register is not set when the violation register is loaded after power turn-on at the end of INIT, and that a parity error can be detected. If a parity error is detected, TESTA halts, the front panel PARITY ERROR light goes on and 000001_8 is contained in the B-register. If a parity error is not detected, TESTA halts, the PARITY ERROR light remains off, and 102005_8 displayed. When the user presses INTERNAL PRESET after a parity error halt, the PARITY ERROR light on the front panel and the parity bit light on the Memory Data Control board go off. Then switch S2 on the I/O buffer board is set to its INTERRUPT mode and the user presses RUN to advance the diagnostic to the next test.

NOTE: From this point the program runs without operator intervention unless an error occurs.

TESTB — TESTB checks the interrupt ability on detection of a parity error. TESTB must be error-free before the other tests can be made.

TESTC — TESTC tests the ability of a CLF 5 instruction to inhibit parity error interrupts. A CLF 5 instruction is issued to turn off the interrupt circuitry, then an even parity word generated by INIT is accessed. An interrupt should not occur.

TESTD — TESTD tests inhibition of parity error interrupts when protected or non-existent memory is accessed. TESTD attempts to read the contents of the highest location in core (detected by CONF), seen as all zeros (even parity) when the LOADER ENABLE lamp is off. It then attempts to read from non-existent core (if any). A parity error interrupt should not occur in either case.

TESTE — TESTE tests inhibition of parity error interrupts during phase 3 of an STA instruction. An STA instruction is used to write an even parity value into memory. An interrupt should not occur. If an interrupt occurs, the diagnostic halts.

TESTH — TESTH tests priority control by generating an I/O interrupt on the I/O channel selected during program configuration of the diagnostic. That interrupt is immediately followed by a parity error interrupt which inhibits the I/O interrupt. If the I/O interrupt occurs first or the I/O interrupt fails to follow the parity error interrupt (or if neither occurs), the diagnostic halts.

TESTI — TESTI causes certain locations, previously set to even parity by INIT, to extensively exercise the parity tree. For each location TESTI performs the following tests:

a. Is parity error detected?

b. Does interrupt occur?

c. Is the location's address strobed into the Memory Protect violation register?

The routine also checks to see that a read/write type instruction (LDB) does not restore good parity to a location containing a parity error and that a clear/write type instruction (STB) does restore good parity.

END — END halts the diagnostic with 102077_8 displayed.

NOTE: This END routine has provisions for return of execution control to a suitable executive program, if present.

LIMITATIONS

This diagnostic does not analyze errors in the Memory Protect violation register. Such errors can occur because of bit failures in the violation register and/or loss of the strobe pulse from the Memory Parity Check circuitry. If the diagnostic halts with 102007_8 displayed (see Table MP-3), the 2100 Memory Protect Test (HP 24222) program should be executed. The error is identified as either the Memory Parity Check or the Memory Protect circuits.

If the program enters an uncontrollable loop caused by the absence of either the IAK or the ENF functions, it cannot report an error.

MESSAGE ANALYSIS

All halts display a MEMORY DATA value. If data is to be read, that data is displayed in the A-register and, when needed, the B-register. Refer to Table MP-3.

OPERATING INSTRUCTIONS

NOTE: At least one standard I/O board must be installed in an I/O slot, Switch S1 on the I/O Control W/DMA board must be set to the ARS position, and Switch S2 on the I/O Buffer board must be set to the interrupt position.

To Configure The Diagnostic

a. Store all zeros in memory location 5_8.

b. Load the HP 2100 Memory Parity Check Test with the Basic Binary Loader.

c. Set Starting Address 2_8.

d. Specify the program configuration by setting the switch register as listed in Table MP-1, then press RUN. If the settings are correct, the computer halts with 107074_8 displayed.

e. Select the internal switch register options by setting the switch register as listed in Table MP-2, then press RUN. The computer halts with 107077_8 displayed in MEMORY DATA.

NOTE: The external switch register is always selected if switch register bit 0 is set.

To Make A Tape Of The Configured Diagnostic

a. If a High Speed Tape Punch is available, load the SIO Tape Punch driver with the Basic Binary Loader and configure the driver.

b. If a High Speed Tape Punch is not available, load the SIO Teleprinter driver with the Basic Binary Loader and configure the driver.

c. Load SIO System Dump.

d. Set Starting Address 2_8.

e. Set switch register bit 15.

f. Press RUN.

g. A configured HP 2100 Memory Parity Check Test tape is punched. The computer halts with 102077_8 displayed. To make additional copies of the configured Memory Parity Check Test Tape, press RUN.

To Load And Execute The Diagnostic

NOTE: Eliminate step a if continuing from step e, To Configure The Diagnostic.

a. Load the configured Memory Parity Check Test tape with the Basic Binary Loader after storing all zeros in location 5_8.

b. Set Starting Address 100_8.

c. Press INTERNAL and EXTERNAL PRESET.

d. Press RUN. The diagnostic executes according to the options selected.

e. Before INIT starts, the diagnostic halts with 102002_8 displayed. If the parity bit light on the Memory Data Control board is on, a circuit error exists and must be fixed, then the diagnostic is restarted.

   If the light is off:

   1. Turn off the computer power.
   2. Connect E1 to E2 and E3 to E4 on the Memory Data Control board with clip leads.
   3. Turn on computer power.
   4. Set Starting Address 110_8.
   5. Clear the switch register.
   6. Press INTERNAL and EXTERNAL PRESET.
   7. Press RUN.

f. The computer halts at the end of INIT with 102003_8 displayed in MEMORY DATA.

1. Turn off computer power.
2. Remove clip leads installed in step e2, To Load And Execute The Diagnostic.
3. Set switch S2 on the I/O buffer board to the HALT position.
4. Turn on computer power.
5. Set Starting Address 111_8.
6. Clear the switch register.
7. Press INTERNAL and EXTERNAL PRESET.
8. Press RUN.

g. TESTA halts if the board is working properly. At that time the front panel PARITY ERROR and the Memory Data Control board parity bit lights should be on. Press INTERNAL PRESET and check that the PARITY ERROR light and the parity bit light turn off. (If either light does not function as described, check the parity error detect circuitry, then restart the diagnostic.) Then display the B-register, it should contain 000001_8.

h. To select options other than those in the internal switch register, set switch register bit 0. Select the desired options by setting the switch register as listed in Table MP-2.

i. Set switch S2 on the I/O buffer board to INTERRUPT.

j. Press EXTERNAL PRESET.

k. Press RUN.

l. After all tests are completed, the computer halts with 102077_8 displayed. To run the diagnostic again, select desired options and perform steps d through k of the procedure "To Load And Execute The Diagnostic."

Table MP-1

Program Configuration--Switch Register Settings

Switch Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits

0-5	Set to select code of the standard interface board.
6	Set if Memory Protect is not available.
7-15	Spares.

Table MP-2

Options--Switch Register Settings

Switch Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits

0	Set to override the internal switch register and to change an option.
1-11	Spares.
12	Set to halt at the end of a complete diagnostic cycle.
13	Set so that after a complete diagnostic cycle, tests requiring operator intervention in future cycles of the diagnostic are eliminated. (Tests eliminated are INIT and TESTA.)
14-15	Spares.

Table MP-3

Diagnostic Messages

MEMORY DATA	Test	Message
102002	INIT	Perform step e, of the procedure "To Load And Execute The Diagnostic."
102003	INIT	Perform step f, of the procedure "To Load And Execute The Diagnostic."
102004	TESTA	Parity error interrupt indicator (bit 15) not reset by power turn-on.
102005	TESTA	Computer failed to halt on parity error.
102006	TESTB	Parity error did not cause interrupt at address shown in A-register. Interrupt function not working, or parity tree is faulty.
102007	TESTB	Parity error memory address is incorrect. Expected address is in A-register, actual in B-register. Perform Memory Protect Test to determine if source of error is in Memory Protect or Parity Error circuitry.
102010	TESTC	CLF 5 did not inhibit parity error interrupt.
102011	TESTD	A parity error interrupt caused by accessing protected memory.
102020	TESTE	A parity error interrupt caused during phase 3 of an STA instruction.
102027	TESTD	A parity error interrupt caused by accessing non-existent memory.
102040	TESTH	Parity error failed to take priority over I/O interrupt.