HP 2100 DMA DIAGNOSTIC

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HEWLETT hp PACKARD

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The test program for the Direct Memory Access option can be used in two modes. In the Long Test Mode, all functions of the DMA are tested, and any functions specific to the select code under test are tested. The Short Test Mode tests only the functions of the select code being tested. All select codes can be tested by installing the proper register card in the I/O slot for the select code to be tested and changing a diagnostic program option.

HARDWARE CONFIGURATION

This diagnostic test program runs on any HP 2100 computer with at least 4K of memory. To test the DMA thoroughly, a Micro-Circuit Register must be used. Although the test program can run with only a teleprinter, certain restrictions are imposed. (See Program Limitations.) A special edge connector is required for the Micro-Circuit Register.

The Micro-Circuit Register, HP 12566, must have the following jumper configuration:

W1-B W2-A
W3-A W4-B
W5 through W8 - IN
W9-A

The special edge connector must be wired as follows:

A-1	K-9	U-17
B-2	L-10	V-18
C-3	M-11	W-19
D-4	N-12	X-20
E-5	P-13	Y-21
F-6	R-14	AA-22-23
H-7	S-15	BB-24
J-8	T-16	

Connector HP 1251-0332 can be used, with pin 22 shorted to pin 23.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

When a teleprinter is used, the SIO teleprinter driver is loaded and configured before the diagnostic program. Then the diagnostic program is loaded and configured.

A permanent copy of the configured program (and the SIO teleprinter driver, if included) eliminates repeating the configuration steps for subsequent uses of the diagnostic. To make a copy, load the SIO System Dump program and run it before running the diagnostic program.

The Long Test Mode, selected by setting program option bit 7 off, should be done for at least one select code to check all DMA functions; using the Micro-Circuit Register the Long Test Mode requires over three minutes of run time. After operation of the DMA functions is confirmed, the remaining select codes can be checked by the Short Test Mode. In the Short Test Mode functions specific to the select code being tested are checked (SRQ lines to each DMA channel and select code lines generated by each DMA channel).

If an error is detected during operation, the program prints a message on the teleprinter, then halts with a MEMORY DATA value in the DISPLAY REGISTER. (Exceptions to this are trap cell halts $1060xx_8$ located in low memory 2_8-77_8 and halts for which a printed message is not appropriate or necessary.) The cause of any of these halts should be determined by the user before the program is run or restarted.

To repeat any test, set program option bit 13 on after an error halt then press RUN.

To reconfigure after running the program, use the re-start address 111_8 instead of the starting address 2_8.

PROGRAM LIMITATIONS

When the Micro-Circuit Register is not available, the teleprinter interface board can be used; however, 8-bit data transfers are made rather than 16-bit transfers, checking only the eight low-order bits. If the register board is used without the teleprinter, the diagnostic test program tests all sixteen

bits; but errors must be interpreted from MEMORY DATA and the contents of the A- and B-Registers, according to Table DMA-3, after an error halt.

The Short Test Mode, consiting of tests T.17 and T.20, tests only the functions of the select code being tested, so the Long Test Mode should be used on at least one select code.

This diagnostic program does not check the maximum data rate specification of the DMA.

Since each channel is tested individually, no testing of simultaneous operation is done.

PROGRAM ORGANIZATION

This diagnostic program performs the following routines.

CONFIG	Inputs and stores hardware information supplied by the operator through the switch register during configuration time. Also stores selected program options in an internal switch register.
INIT	Sets trap cell halts in locations 2_8-77_8 and prints the start-of-diagnostic message on the teleprinter.
T.1	Tests the DMA flag instructions.
T.2	Tests the ability to enable and disable the interrupt system.
T.3	Tests the DMA interrupt capability by forcing an interrupt, checking the return address for the correct location, and checking the interrupt acknowledge
T.4	Tests the control reset instructions.

T.5 If program option bit 9 is set off, tests the PRESET functions. Before the PRESET test starts, the program halts with 102027_8 in the DISPLAY REGISTER, to allow the user to press INTERNAL and EXTERNAL PRESET.

T.6 Tests DMA interrupt priority. Checks priority of DMA channel 1 (DMA1) over DMA channel 2 (DMA2) and over the I/O select code under test (which contains MCR or teleprinter interface card). Checks ability of DMA PH5 signal to inhibit I/O interrupts. Checks DMA 2 priority over I/O select code under test.

T.7 Tests the ability to set and read the word count registers for all numbers up to the maximum word count (65,535).

T.10 Tests the word count increment function (rollover) by setting the word count registers to minus one and forcing a data transfer which should cause the DMA to interrupt.

T.11 Tests the direct memory address registers by making DMA output transfers from every available location in memory.

T.12 Tests the ability of the DMA to set an interface control flip-flop when bit 15 of the DMA program control word has bet set to a one.

T.13 Tests the ability of the DMA to clear an interface control flip-flop when bit 13 of the DMA program control word has been set to a one.

T.14 Tests the ability of DMA generated signal to clear interface flag after transfer.

T.15 Tests the DMA output capability with all possible 16-bit data patterns and their complements if MCR is used, or with all possible 8-bit patterns and their complements if TTY interface is used.

T.16 Tests the DMA input capability with the same data patterns used in T.15

NOTE: The Long Test Mode (program option bit 7 set off) performs all tests, the Short Test Mode (bit 7 set on) performs only tests T.17 and T.21.

T.17 Used in the Short Test Mode, this routine uses subroutines in T.15 to output one word through each DMA channel.

T.21 Tests the DMA for illegal response to incorrect select codes.

END If program option bit 12 is set on, END prints the end-of-diagnostic message on the teleprinter and halts, or if bit 12 is set off, END restarts the program.

NOTE: This END routine has provisions for return of execution control to a suitable executive program, if present.

OPERATING INSTRUCTIONS

NOTE: This procedure presumes the use of a Micro-Circuit Register. The register card must have jumpers wired as described under HARDWARE CONFIGURATION and must be connected through an edge connector, also described in that section. If the register card is not used, install the teleprinter interface card in the slot to be tested; limitations described will apply.

Table DMA-1

Hardware Configuration--Switch Register Settings

Bits	Function
0-5	Set to the Register Card (or teleprinter select code interface).
6	Set on if teleprinter is not available.
7-15	Spares.

Table DMA-2

Program Options-- Switch Register Settings

Bits	Function
0	Set on to override the internal switch register, to change a program option. This bit has no effect when set on in the internal switch register.
1-5	Spares.
6	Set on to halt at the beginning of the program, to allow entry of a new select code.
7	Set on to use the Short Test Mode, otherwise the Long Test Mode is to be used.
8	Set on if a teleprinter interface card is to be used to test the select code, otherwise the program assumes a Micro-Circuit Register card is to be used.
9	Set on to omit the PRESET test (T.5).
10	Set on to suppress non-error messages.
11	Set on to suppress all messages.
12	Set on to halt the program after a complete cycle.
13	Set on to loop on the current test instead of advancing to the next test.
14	Set on to suppress error halts.
15	Spare.

TABLE DMA-3

Diagnostic Messages

MEMORY DATA	Test	Message*	Comments
(no halt)	INIT.	HØ. START DMA DIAGNOSTIC	Initial Message.
102001	T.1	E1. CLF6 OR SFS6 ERR	DMA1--Test the ability to clear the flag and test the SFS instruction.
102002	T.1	E2. CLF6 OR SFC6 ERR	DMA1--Test the ability to clear the flag and test the SFC instruction.
102003	T.1	E3. STF6 OR SFC6 ERR	DMA1--Test the ability to set the flag and test the SFC instruction.
102004	T.1	E4. STF6 OR SFS6 ERR	DMA1--Test the ability to set the flag and test the SFS instruction.
102005	T.1	E5. CLF7 or SFS7 ERR	DMA2--Test the ability to clear the flag and test the SFS instruction.
102006	T.1	E6. CLF7 OR SFC7 ERR	DMA2-- Test the ability to clear the flag and test the SFC instruction.
102007	T.1	E7. STF7 OR SFC7 ERR	DMA2--Test the ability to set the flag and test the SFC instruction.
102010	T.1	E1Ø. STF7 OR SFS7 ERR	DMA2--Test the ability to set the flag and test the SFS instruction.
102011	T.2	(none)	CLF Ø did not disable interrupts or SFS Ø caused a bad skip.
102012	T.2	(none)	CLF Ø did not disable interrupts or SFCØ did not skip.
102013	T.2	E13. STFØ OR SFCØ ERR	STF Ø did not enable interrupts or SFC Ø caused bad skip.

*"H" Message is informational
"E" Message indicates an error.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102014	T.2	E14. STFØ OR SFSØ ERR	STF Ø did not enable interrupts or SFS Ø did not skip.
102015	T.3	E15. NO D1 INT	Test the interrupt capability of DMA1.
102016	T.13	E16. NO D2 INT	Test the interrupt capability of DMA2.
102017	T.3	E17. D1 RTN ADDR ERR	DMA1--The return address that resulted from the interrupt is incorrect.
102020	T.3	E2Ø. D2 RTN ADDR ERR	DMA2--The return address that resulted from the interrupt is incorrect.
102021	T.3	E21. D1 IAK ERR	DMA1--Interrupt acknowledge failed.
102022	T.3	E22. D2 IAK ERR	DMA2--Interrupt acknowledge failed.
102023	T.4	E23. D1 CLCØ ERR	DMA1--CLC Ø instruction failed to reset the control flip-flop.
102024	T.4	E24. CLC6 ERR	DMA1--Test ability of CLC 6 instruction to clear the control flip-flop.
102025	T.4	E25. D2 CLCØ ERR	DMA2--CLC Ø instruction failed to reset the control flip-flop.
102026	T.4	E26. CLC7 ERR	DMA2--Test ability of CLC 7 instruction to clear the control flip-flop.
102027	T.5	(None)	Press INTERNAL and EXTERNAL PRESET switches, then press RUN.
102031	T.5	(None)	EXTERNAL PRESET failed to set DMA1 flag.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102032	T.5	(None)	EXTERNAL PRESET failed to set DMA2 flag.
102035	T.6	E35. D1-D2 PRIORITY ERR	DMA1 failed to take priority over DMA2.
102036	T.6	E36. D2-IO PRIORITY ERR	DMA2 failed to take priority over I/O select code being tested.
102037	T.6	E37. D1-IO PRIORITY ERR	DMA1 failed to take priority over I/O select code being tested.
102040	T.7	E4Ø. WC1 IS *xxxxxx*, SHOULD BE *xxxxxx*	Word count readback from DMA1 is different from output word. A-Register (press A) contains output word, B-Register (press B) contains input word.
102041	T.7	E41. WC2 IS *xxxxxx*, SHOULD BE *xxxxxx*	Word count readback from DMA2 is different from output word. A-Register (press A) contains output word, B-Register (press B) contains input word.
102042	T.10	E42. NO D1 INT	With interrupt system enabled, DMA1 failed to interrupt after word transfer.
103043	T.10	E43. NO D2 INT	With interrupt system enabled, DMA2 failed to interrupt after word transfer.
102044	T.10	E44. WC1 IS *xxxxxx*, SHOULD BE ZERO	DMA1 word count register was not zero when interrupt occurred. B-Register (press B) contains word count.
102045	T.10	E45. D1 INT LOC IS	DMA1 interrupted from wrong location after transfer. A-Register (press A) contains correct location, B-Register (press B) contains incorrect location.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
103035	T.6	E135. NO I/O INT	No interrupt on I/O select code. Check PRL7 signal.
1060*xx*	All	(None)	Trap cell interrupt. M = memory address when interrupted, *xx* = trap cell location.
107074	CONFIG	(None)	Press LOADER ENABLE button to turn it off then press RUN.
107075	CONFIG & INT	(None)	The select code (switch register bits 5-Ø) is invalid. (Valid codes are 10_8-77_8.) Set the correct select code then press RUN.
107076	CONFIG	(None)	Set internal switch register for desired program options (see Table DMA-2) then press RUN.
107077	CONFIG	(None)	Configuration complete. Use SIO System Dump or set the starting address 100_8, select desired program options, press INTERNAL and EXTERNAL PRESET then press RUN.