PAPER TAPE NO. 24323-16001

CORE MEMORY DIAGNOSTIC

for

hp-2100 SERIES COMPUTERS

reference manual

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *HP 2000 Diagnostic Configurator Manual,* part no. 02100-90157, dated August 1976 or later.

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Memory Diagnostic

Introduction

The Memory Diagnostic checks the memory used in any 2100 series computer.* The diagnostic consists of two tests, a high memory pattern test and a low memory pattern test. The operator selects which of the two tests is to be executed initially by the program address (P-register) setting. After execution of one of the tests, the other test is executed.

This diagnostic operates in any 2100 series computer with a minimum of 4K of memory. It is one of the HP 2000 computer system diagnostics executed in conjunction with the HP 2000 Computer Systems Diagnostic Configurator. Test and error information is communicated to the operator through the Memory Data Register (MDR or T-register), and the A- and B-registers. Operator input is via the switch register.

GENERAL ENVIRONMENT

The general hardware and software environments and system configuration procedures are described in the *HP 2000 Computer Systems Diagnostic Configurator* manual (02100-90157).

Hardware Requirements

1. The diagnostic can be run on any 2100 series computer with a minimum of 4K of memory.
2. Memory Protect feature installed on the computer is optional.
3. A paper tape reader is required to load the program only.
4. A teletype is not used with this diagnostic.

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*Except 21MX series computers.

Software Requirements

The required software consists of the following binary object tapes:

1. HP 2000 Computer Systems Diagnostic Configurator (HP 24296).

2. Memory Diagnostic, part no. 24323-16001.

Loading is performed using the Binary Loader (usually memory resident). See the appropriate *Front Panel Procedures* for the 2100 series computer being used for use of the Binary Loader. The loader is described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader* (HP 5951-1376).

Operating Procedures

Operating procedures are divided into three parts: Preparation for Diagnostic Run, Running the Diagnostic, and Diagnostic HALT codes.

PREPARATION FOR DIAGNOSTIC RUN

Before the tests can be initiated, perform the following actions:

- Load the Diagnostic Configurator
- Configure to available system hardware
- Load the diagnostic
- Dump the configuration for later use (optional)

Loading

Using the Binary Loader, load the Diagnostic Configurator. Perform the configuration procedure (see "Configuring" below) before loading the diagnostic. Then load the Memory Diagnostic using the Configurator. The user may insure that the proper diagnostic is loaded by checking memory location 126_8 for the Diagnostic Serial Number = 102200_8.

Procedures for inputting the system hardware configuration parameters are found in the HP 2000 Computer Systems Diagnostic Configurator manual under "CONFIGURING."

The configuration procedure accepts six groups of parameters. This diagnostic requires only two groups be defined. They are:

- Computer type and options
- Memory size and type

The other parameters may be left undefined (zero).

Computer Type and *Options* and *Memory Size* and *Type* must be carefully determined. These hold significant parameters for the execution of the diagnostic. These parameters vary from one 2100 series installation to the other.

Dumping

Using procedures described in the Diagnostic Configurator manual, the user may dump the configured diagnostic from memory onto paper tape so that the above configuration procedures need not be repeated. The dumped paper tape holding the configured diagnostic can thereafter be loaded via the Binary Loader.

RUNNING THE DIAGNOSTIC

Switch Register Settings

Table 1 gives a summary of switch register options. If switch register bits 0-4 are clear, tests 1 through 4 are executed as individual tests (loop feature will loop on each test individually). If any switch register bits 0-4 are set, these bits determine the tests to be run.

The Random Number Test is run (loops) as long as switch register bit 4 is set.

If switch register bit 5 is set, errors which are not the result of moving a section of the diagnostic program itself and are located above 8K, will be stored in a table beginning at location 1600_8. A failing address will be entered only once in the table. Each error will occupy five consecutive memory locations. The first location holds the failing address, the second holds the correct pattern, the third holds the bad pattern (actual pattern contained at stored memory address), the fourth is a NOP and the last is the number of times an error has occurred at this address. The error table will contain only 4 errors per 4K above 8K and end at 1767_8.

Table 1. Switch Register Settings

Bits	Meaning
0	*Set:* Run Address test.
	Clear: Delete test.
1	*Set:* Run Alternate Word test.
	Clear: Delete test.
2	*Set:* Run Word Pattern test.
	Clear: Delete test.
3	*Set:* Run Bit 0 test.
	Clear: Delete test.
4	*Set:* Run Random Number test.
	Clear: Delete test.
5	*Set:* Store errors in error table (Above 8K; not comparison; 4 per 4K of memory).
	Clear: Leave error table clear.
6	*Set:* Clear error table — start new error table.
	Clear: Accumulate errors in error table.
7	Reserved
8	*Set:* Configurator has not been loaded and configured.
	Clear: Configurator is loaded and configured.
9	Reserved
10	*Set:* Exit currently executing test to restart diagnostic.
	Clear: Diagnostic continues.
11	*Set:* Halt upon restart of Low Memory test.
	Clear: When restarting diagnostic, do not perform halt.
12	*Set:* Loop on diagnostic.
	Clear: Halt 102077_8 and end of pass.
13	*Set:* Loop on selected test.
	Clear: Cycle through selected tests.
14	*Set:* Suppress error halts.
	Clear: Halt on errors.
15	*Set:* Halt 102076_8 at end of selected tests.
	Clear: Cycle through selected tests.

If *switch register bit 6* is set, the error table, established via switch register bit 5, will be cleared upon return to start of diagnostic.

If *switch register bit 8* is set, the diagnostic will not use the configurator parameters but calculates its own and uses only 2100A/S patterns.

If *switch register bit 10* is set, exit is made from currently executing test (in Low Memory test only) to restart the diagnostic.

If *switch register bit 11* is set, a HALT will occur upon return to start of program.

While *switch register bit 13* is set, the current test being executed will repeat (loop).

If *switch register bit 15* is set, the diagnostic program will perform a HALT (MDR = 102076_8) at the end of each test section.

Diagnostic Execution

1. Set the P-register to 100_8 to commence testing in the High Memory test. Set the P-register to 130_8 to commence testing in the Low Memory test.

2. If the Low Memory test is to include the Binary Loader area of memory (the last 100_8 locations), unprotect the loader. This test results in the destruction of the Binary Loader. The user must restore the Binary Loader, using the steps given *Basic Binary Loader — Basic Binary Disc Loader* (HP 5951-1376), after the test is completed.

   Set the Memory Parity Error switch to the Interrupt position if Memory Protect is present. Otherwise, set it to the Halt position.

   If a power failure interrupts the diagnostic, unpredictable results will occur.

3. Press RUN.

   Result: The memory diagnostic executes according to program options selected.

DIAGNOSTIC HALT CODES

The diagnostic communicates to the operator by coded HALTs. The Memory Data Register (MDR or T-register), A-register, and B-register hold information which indicates test procedure and test failure. HALTs fall into two types: information and error HALTs. They are invoked or suppressed according to switch register settings (see Table 1). Table 2 lists the HALT codes and meanings. The second column of the table, headed by *E/I*, indicates whether the HALT is an error HALT, *E*, or an information HALT, *I*.

Table 2. HALT Codes

Octal MDR (A- & B-reg.) HALT Code	*E/I*	Test	Meaning
102005 (A=*xxxxxx*, B=*yyyyyy*)	*I*	Any	This is the HALT which displays status of the table of errors (selected by switch register bit 9); *xxxxxx* is the next available address after the error table entries; *yyyyyy* is the octal number of errors recorded in the table.
102006	*I*	Any	The error table ran over 2000_8. The program is destroyed.
102007 (A=*xxxxxx*, B=*yyyyyy*)	*E*	Any	Parity error was detected in section of memory containing program; *xxxxxx* is memory address; *yyyyyy* is contents of memory. To restore memory, enter correct memory contents into B-register, press RUN.
102013 (A=*xxxxxx*, B=*yyyyyy*)	*E*	Any	Parity error was detected in section of test area; *xxxxxx* is pattern that was written; *yyyyyy* is memory address.
1020*nn* (A=*pppppp*, B=*qqqqqq*)	*E*	1 through 5	Memory Failure: *pppppp* is data written into memory; *qqqqqq* is data read from memory; test given by value of *nn*, where *nn* = 10 means part of the program was moved incorrectly. = 20 means test 1 = 30 means test 2 = 40 means test 3 = 50, 51, or 52 means test 4 = 60 means test 5 Press RUN to obtain failing address.
1020*mm* (A=*xxxxxx*)	*E*	1 through 5	Display of address in error; *xxxxxx* is failing address; *mm* = *nn* + 1 (see preceding HALT code explanation for value *nn*).
102076	*I*	1 through 5	HALT at end of each test.
102077	*I*	Last	Diagnostic has been completed; select options and press RUN to continue.
103004	*E*	Any	Power fail interrupt occurred.
103077	*E*	Any	Nonexistent memory returns other than all 0's.
106077	*E*	Any	Unexpected trap cell interrupt occurred.

Test Section

The Memory Diagnostic consists of five tests: an address test and four pattern tests.

ADDRESS TEST

Test 1 — Address Decoder

The memory location address is stored into each memory test location. Then each location is read back and verified. The compliment of the memory location is then written into memory, read back and verified.

PATTERN TESTS

The following tests exercise memory with worst case patterns. Tests 3 and 4 employ two distinct words, W_1 and W_0, which are stored into memory in blocks according to logic equations operating on memory addresses. The last, test 5, uses random patterns to exercise memory.

Pattern tests 3 and 4 are distinguished from each other by the initial values of W_1 and W_0. They have in common the fact that W_1 and W_0 are selected for entry into memory locations according to a value, R, derived by logic equations given in Appendix A. If the result of the equation is R = 0, W_0 is used for the memory location; otherwise W_1 is used.

Tests 2 through 4 employ a standard test cycle with the following characteristics. Each cell of the pattern written into memory is tested in succession to determine if the data read is the same as that written into it. If correct, the memory contents are complemented and stored back into the memory location. The memory contents are read again, verified and, if correct, complemented and restored. Thus, after verifying the memory location, the original contents are in place. An error HALT is executed whenever an error is detected, if error HALT is not suppressed by the switch register.

Test 2 — Alternate Word Pattern

This test performs two standard test cycles. The first standard test cycle is performed after a pattern is written into memory which alternates between 000000_8 and 177777_8, starting with 000000_8. The second standard test cycle is performed after a pattern is written into memory which alternates, as before, starting with 177777_8.

Test 3 — Word/Row Pattern

This test consists of two standard test cycles. The first standard test cycle is performed after the logic equation in Appendix A is employed to determine blocks of W_1 and W_0 to be written into memory. $W_1 = 177777_8$ and $W_0 = 000000_8$ are used in the first standard test cycle.

The second standard test cycle is performed after W_1 and W_0 are exchanged in the pattern written into memory.

Test 4 – Memory Disturbance Pattern

The first half of this test consists of 16 test repetitions of two standard test cycles each. Between each repetition W_1 is left shifted by 1 bit. The initial value of $W_1 = 000001_8$ and $W_0 = 000000_8$.

The first standard test cycle is performed after the logic equation in Appendix A is employed to determine blocks of W_1 and W_0 to be written into memory. The second standard test cycle is performed after W_1 and W_0 are exchanged in the pattern written into memory.

The second half of this test consists of another 16 test repetitions of two standard test cycles each. Between each repetition W_0 is rotationally left shifted by 1 bit. The initial values are: $W_0 = 177777_8$ and $W_1 = 177776_8$. The first and second standard test cycles execute as above with W_1 and W_0 exchanged on the second.

Test 5 — Random Pattern

This test stores a random pattern into all test locations in memory. Then each location is read and compared to the pattern that was stored there. This test will continue to run until switch register bit 10 is set.

APPENDIX A
Memory Pattern Equations

The pattern used to test memory depends on the particular 2100 series computer being used. A logic equation determines which of two words, W_1 and W_0, are written into each memory location, based on the location address. A different logic equation is used for each 2100 computer.

The equations select one of two word bit configurations, W_1 or W_0. If the result, R, of the equation is 1, W_1 is used; otherwise W_0 is used. Here follows a list of the logic equations by computer used:

Computer	Equation
2116A	$R = \overline{M6} \cdot (\overline{M5 \oplus M0}) + M6 \cdot (M5 \oplus M0)$
2116B	$R = \overline{M7} \cdot (\overline{M1 \oplus M0}) + M7 \cdot (M1 \oplus M0)$
2116C	$R = (\overline{M5 \oplus M6})$
2115A	$R = (\overline{M0 \oplus M6})$
2114A	$R = (\overline{M0 \oplus M6})$
2114B	$R = (\overline{M0 \oplus M6})$
2100A, S	$R = (\overline{M5 \oplus M6})$

The symbols used have the following meaning:

Mn specifies bit *n* of memory address.
Example: M0 means bit 0 of memory address.

$\overline{Mn}$ means complement value of M*n*.
Example: $\overline{M7}$ = 1, if M7 is 0
$\overline{M7}$ = 0, if M7 is 1

$\oplus$ means "exclusive or".

$\cdot$ means "and".

\+ means "or".